Integrated cryogenic electronics to readout large areas SiPMs



Doctoral Dissertation
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Integrated cryogenic electronics to readout large areas SiPMs

DarkSide 20K Experiment

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Alejandro D. Martinez Rojas

Turin, March, 2021

Summary

The current underground astroparticle experiments of looking for rare events, such as Deep Underground Neutrino and DarkSide-20K, are implementing structures to work in cryogenic temperatures. Cryogenic structures require a robust system capable of readout the generated photo-electrons (PEs) in a cryogenic environment.

In the astroparticle experiments, the electronics readout is mainly structured by a front-end circuit. Hitherto, most readout electronics consist of discrete electronics for general-purpose. Discrete electronics must implement additional filters to achieve the desired bandwidth. Furthermore, it requires an off-line digital signal processing to supply the minimum requirement of signal to noise ratio (SNR). Otherwise, the noise level makes the photo-electron reading a complex process due to the large detector capacitor (> 10 nF)

This research activity deals with the modeling and design aspects of the integrated cryogenic electronics in CMOS technology for fast amplification. An integrated electronics might achieves better performance in terms of SNR and cost. The SNR assumption is done due to the improvement of capacitive matching between sensor and electronic, something hard to realize in general-purpose electronics. Also, the integrated electronics becomes a much cheaper option for mass production than discrete electronics. Furthermore, thank to the robust structure of CMOS technology, front-end electronics can be designed with a lifetime longer than 20 years. It is enough time for an experiment such as an underground astroparticle.

The study of front-end electronics in CMOS technology for SiPM readout at cryogenic condition implies a long-term RD on the technology and circuit design. As a result, few structures of a single transistor were tested and analyzed at a cryogenic temperature of 77 K. The results describe the behavior of the main internal parameters, such as low-filed mobility, threshold voltage, transconductance, and so on. The extraction parameter outcomes develop into a key to design the complete integrated electronics architecture precisely.

Besides, the cryogenic operation causes a substantial reduction of the failure mechanisms in MOS structures, such as electromigration, stress migration, time-dependent dielectric breakdown, and thermal cycling. However, the most attractive advantage becomes with a consistent reduction of thermal noise, making the readout of a SiPM area of 24 cm^2 viable. In this experiment, a large area detector is required for a low cabling

and electronic mass, and thus low radioactivity background requirement.

The cryogenic electronics implement a 110 nm CMOS technology. The front-end prototype was developed in two tape-outs. Primarily, the cryogenic electronics (ASIC v1) features 4 fast and low-noise (LN) amplifiers based on Folded Cascode topology with a Class AB amplifier on the output stage. Each low-noise amplifier readout a SiPM quadrant of 6 cm^2. The sensor capacitance presents a value of around 10 nF, which highly depends on the bias voltage of the sensor. The 4-LN amplifiers are connected to a summing amplifier to generate a single-end signal from 24 cm^2 SiPM.

The second tapeout realizes an identical 4-LN and summing amplifier architecture. However, the ASIC v2 incorporates a single-ended to the differential converter. The conversion stage is performed by a fully differential folded cascode structure with common-mode feedback. Besides, the ASIC v2 allows the output signal of cryogenic electronics to be established, as a single-ended or differential signal due to their dedicated power domain. Differential signaling provides the advantage to transport the information from the cryogenic environment to warm data acquisition system by cabling, instead of optical fiber.

Acknowledgements

I would like to dedicate this thesis to Istituto Nazionale di Fisica Nucleare and Ufficio VLSI, which allow the research project to be developed successfully. Furthermore, I want to show a special dedication to my fiancee for her support along my Ph.D. study.

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Chapter 1

Introduction

Historically speaking the cryogenic electronics has always provided attractive features to enhance many scientific and industrial processes. However, this has not been implemented widely in many field. In recent years cryogenic electronics have started to be considered in several research areas, such as deep space, underground astroparticle, imaging, and so on. Cold electronics allows high performances in terms of noise, current drive capability, bandwidth to be achieved due to the thermal interaction reduction at cryogenic temperatures. These advantages make cryogenic electronics a widely explored and developed area shortly.

The thesis is focused on the integrated cryogenic electronics design for the readout of large-area sensors (24 cm^2 Silicon PhotoMultilplier) with optimal performances in terms of the signal to noise ratio, dynamic range, and timing jitter. The cryogenic electronics points to improve the current photodetection system in neutrino and dark matter experiments since most of them implement the pre-amplification stage outside the cryogenic structure. Furthermore, many photodetection systems just readout a small-area sensor due to its large detector capacitance. The small-area detector requires a higher number of the readout electronic chains causing a small increment of radioactive impurity, but important for low-background experiments. The cryogenic prototype

The thesis covers the design and post-implementation simulations of a real-time digital filter. In this digital signal processing stage, the figure-of-merit is enhanced by more than 50 %. The thesis is divided into 5 sections.

Section 2 contains information about the most relevant projects where cryogenic electronics is implemented. Furthermore, describe the current photo-detection systems in underground astroparticle experiments. Section 3 presents the behavior of the CMOS technology and the Silicon PhotoMultiplier at a cryogenic temperature of 77 K.

Besides, the second section owns the experimental results of the CMOS extraction parameters. This step was crucial for the cryogenic electronics design. Section 4 described the transistor-level design and mismatch optimization of ASIC v1. The chapter also includes post-layout and Monte-Carlo simulation. The experimental result of ASIC v1, as the real-time digital filter implementation is described in Section 5. The section shows a couple of peak voltage histograms to describe the cryogenic front-end efficiency. Finally, the last chapter describes a new front-end prototype to readout large-areas sensors, including a single-end to the differential converter. Besides, the new prototype implements a different CMOS technology in comparison to ASIC v1. The section includes preliminary results obtained with a charge injection board, instead of the SiPM.

1.1 Need for Underground Astroparticle experiment

The underground astroparticle physics experiments present two structures, which require cryogenic electronics, such as the Time Projection Chamber (TPC) and the VETO system. The experiment detector operates with noble gas elements, as a result, the element determines the operation temperature of the TPC and VETO. Mainly the astroparticle experiments utilize the Liquid Argon and Liquid Xenon as the scintillator. Hence, cryogenic electronics are required to work at 87 K or 175 K.

Chapter 2

Key developments in cryogenic electronics

Cryogenic electronics design has been implemented in many technological and scientific research in recent years. This chapter illustrates the most important experiments, which the cryogenic electronics contributions have been crucial for its development. The research areas include quantum computing, the deep space mission, fast imaging, and underground astroparticle experiments.

2.1 Cryogenic electronics for general purposes

In recent decades the cryogenic electronics has been applied in several research areas due to its low-temperature advantages. The most well-known research fields are the readout of the superconductive astronomical detectors [1], spacecraft project [2], the operation of qubits in the quantum computers [3] and astroparticle physics experiments [4]. In this study, just space and deep space application, quantum computing, the infrared fast imagining will be deepening in details.

The emerging cryogenic space and deep-space application

Cryogenic electronics has become an attractive environment for space and deep-space projects due to its thermal noise advantages. The cold electronics has been implemented within international projects, such as Lunar and Martian robotics [5] and deep space antenna (Figure 2.1). In the Lunar robotics, the temperature conditions are established down to 43 K due to the Lunar shadowed polar craters [6]. Furthermore, the cryogenic devices must consume a restricted amount of available power due to the limitation of a power supply within the space. Initially many researches have focused on the cryogenic performance of commercial electronics to develops a cryogenic ASIC prototype [7].

As a first step, the reliability of the technologies, such as CMOS or SiGe, has been tested in order to guarantee a high functionality along the time before a full architecture implementation.

For instance, a cryogenic Lunar electronics [6] implements a commercial 0.5 μm SiGe HBT BiCMOS technology. The technology has demonstrated adequate reliability under specific work conditions. The commercial SiGe HBT has sufficiently indicated advanced performance to be considered, as cryogenic technologies to the Lunar space missions. However, the commercial technology requires an own bias and loading changes to make them work at a required cold temperature [7].

On the other hand, CMOS technology develops an optimal carrier mobility increment, current drive capability, thermal noise reduction, and a higher transit frequency. The previous characteristics make the CMOS an attractive technology at cryogenic temperatures. Nonetheless, its flicker noise increases due to the oxide layer between the metal gate and the active conducting channel [8]. The low-frequency noise approximately presents a rise at temperatures lower than 40, affecting the experiments at Helium temperature (4.2 K). Furthermore, CMOS reliability has demostrated to achieve a lifetime more than 20 years [9].

Figure 2.1: Deep space antenna for the future space missions of the European Space Agency (ESA). Picture taken from ESA

The previous technologies have been implemented in any type of electronic circuit. For instance, one of the required cryogenic circuits for space application includes the low noise amplifier (LNA). In the European space agency (ESA), the cryogenic LNA has been implemented for the deep space mission through the ESA technology research program [10]. In this RF project, the cryogenic conditions are necessary to improve the signal-to-noise ratio, which allows the deep space signals to be recognized. At room temperature, the high thermal noise in the receiver makes the signal recognition a complex or an almost impossible process. Thus, the deep-space antenna demands a cryogenic front-end architecture, as shown within Figure 2.2. In this circuit, the LNA was designed by a cryogenically cooled High Electron Mobility Transistor technology (HEMT).

Quantum computing application

Quantum computing (QC) is one of the most attractive projects within these decades. The project has caused a relevant interest from the important electronics industries, such as IBM [12], Intel [13], and for technological industries, such as Google [14] and Microsoft [15]. Quantum computing owns engaging features to be applied in several areas, such as machine learning in which a computer must process the petabytes of unanalyzed data. In the biomedical simulation, QC will allow the complex molecular

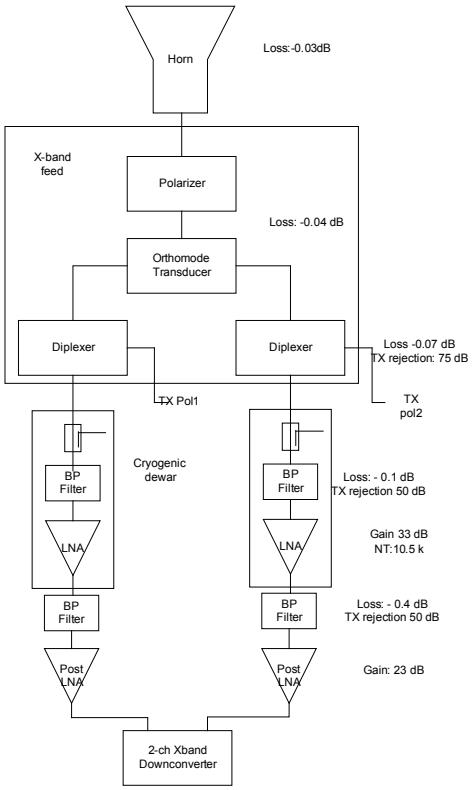

Figure 2.2: Fully schematic of the front-end electronic circuits for space missions. Picture taken from [11]

structure to be created, simulated, and modeled much faster and efficiently. In financial service, the QC could develop complex financial modeling and risk management.

Currently, the computing systems are manipulated by ordinary computers, which implement bits (1s or 0s) as the data unit. The quantum computer implements a quantum mechanical process to control the information. In other words, this new computing method realizes calculations supported by the probability of an object's state before it is measured. Hence, the basic containers of information are changed by the quantum bit or qubit [16]. The quantum units require to be operated at deep cryogenic temperatures in order to remain coherent for a short time [8]. Otherwise, the thermal energy in a qubit could give a motion enough to decoherence any quantum state that has been established previously [17].

In the QC field, the cryogenic electronics may be built by the MOS technology or by the HEMT. The MOS technology is well-known to operate at 4.2 K, therefore the CMOS

could in principle be employed in a fault-tolerant loop [18], [19]. CMOS operation at 4.2 K provides optimal results in terms of transit-frequency, despite the increase of the slope factor and flicker noise at deep cryogenic temperatures [3],[8].

On the other hand, the HEMT technology can work with a low flicker noise at 4.2 K. This technology is fabricated on a heterostructure with a high purity material interface. Experimentally the equivalent input noise voltage of HEMTs at low frequency and Helium temperature is inversely proportional to the square root of their input capacitance C_{gs} [20]. Furthermore, the HEMT transistor can achieve a transit-frequency around 160 GHz [21].

A cryogenic ASIC for quantum computing additionally requires high tested reliability and functionality of each circuit implemented in a prototype. For instance, Figure 2.3 described a complex cryogenic full system prototype working on deep cryogenic temperatures.

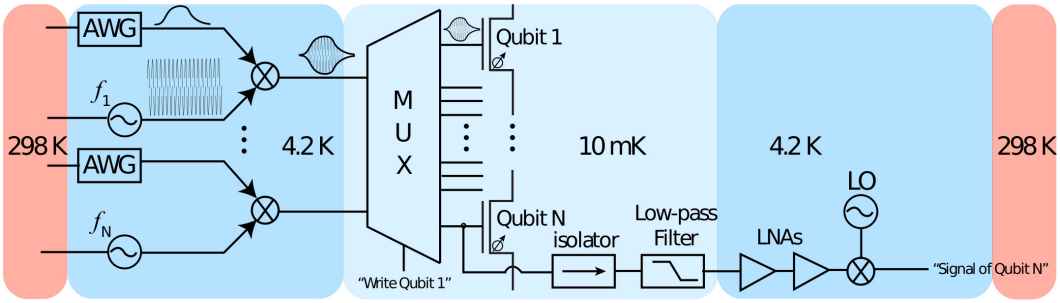

Figure 2.3: Fully schematic of the front-end electronic circuits for controlling and measuring spin qubits. Picture taken from [22]

Imagining application

Imagining application has been popular for the usage of cryogenic electronics. The infrared fast imagining presents a system architecture called linear imager, or in this case, an infrared cryogenic imager. This architecture is formed by a row of hundreds or thousands of IR sensors. In many fast imaging projects, the IR sensors are connected to front-end electronics, which operates at a cryogenic temperature of 77 K. In other words, the IR sensor is monolithically on top of the CMOS read-out circuit [23]. Figure 2.4 illustrates an infrared cryogenic imager including the IR sensor, Read-Out Integrated Circuit (ROIC), and a grid of the active-pixel sensors, which connect the ROIC and IR sensor.

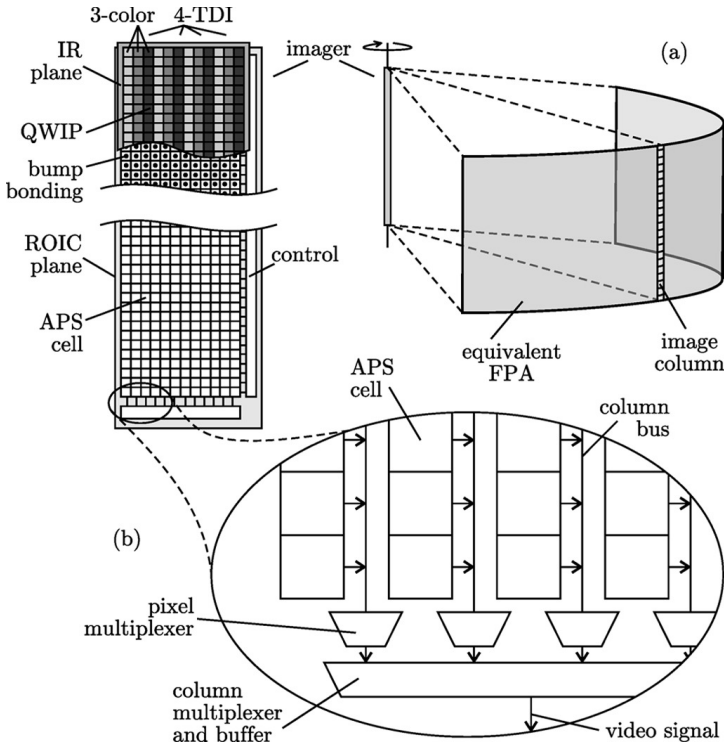

Figure 2.4: CMOS APS Circuits for Hybrid Cryogenic Infrared Fast Imaging schematic. Picture taken from [23]

The Active-Pixel Sensors (APS) are conformed by a silicon photodiode integrated with its readout electronics. The APS works efficiently at cryogenic temperatures of 77 K, 60 K, and 40 K. Inasmuch as cryogenic electronics implements a simple 4-transistors architecture. This topology makes the transistor parameter variation much easier to control at cryogenic temperatures. Furthermore, it provides high reliability at low temperatures due to the circuit simplicity [24].

Military aircraft application

The battle shift and the aircraft in the future will likely exploit the benefit of the cryogenic technologies by implementing cryogenic power converter in generators and motors [25]. This application utilizes the performance benefits of semiconductor power devices at low temperatures. Then, one expects a significant gain in terms of energy dissipation, higher cut-off frequencies, and so on. This could reduce one of the biggest problems of the aircraft related to the electric power consumption and dissipation.

2.2 Cryogenic electronics for underground astroparticle experiments

One of the most important cryogenic applications has been underground astroparticle experiments. These physics projects implement structures for astroparticle detection with an operating temperature of 175 K (Liquid Xenon) and 87 K (Liquid Argon). The searched astroparticle has been the neutrinos and the weakly interactive massive particle (WIMP).

Many countries have been collaborating within international frameworks for astroparticle researches. The underground experiments have been divided into two research areas. Firstly, the neutrino searching, which is conformed by couples of experiments, such as the Deep Underground Neutrino Experiment (DUNE) and the Enriched Xenon Observatory (EXO). Both DUNE and EXO experiments operate at a temperature of 87 K. Secondly, the dark matter searching, which is integrated by several experiments, however, only two of them will be mentioned in this study. The experiments are the XENON and DarkSide project.

2.2.1 Deep Underground Neutrino Experiment

Neutrino is an elementary particle that may hold the key to solving the great mysteries of nature, and this leads to a great effort to understand its role in the universe. The Deep Underground Neutrino Experiment (DUNE) realizes observations through a nucleon decay detector.

A single-phase detector prototype has been designed and implemented in the DUNE framework [26]. This has been the first DUNE 10-kt fiducial mass far detector module with total liquid argon (LAr) mass of 0.77 kt. The ProtoDUNE detector was built at CERN and has become the largest detector for the DUNE experiment so far. ProtoDUNE-SP Far Detector prototype consists of a TPC, a cryogenic electronics (CE), and a Photon Detection System (PDS), implemented all inside a cryostat full of Liquid Argon (LAr).

The cryogenic electronics of the DUNE single-phase TPC is mounted directly to the sensor, therefore the parasitic elements and noise due to the long interconnections are minimized considerably, in comparison to the coaxial connection between the sensor and its corresponding readout electronics outside the cryostat. The cold electronics of ProtoDUNE presents several channels readout with an amplifier, a shaper, a digitizer, a buffer, and a multiplexer circuit [27].

The protoDUNE owns an Anode Plane Assemblies with 2,560 channels readout by 20 Front-End Motherboards. The motherboard architecture, illustrated in Figure 2.5, presents the cryogenic front-end circuit readout a 4-groups of 3 SiPM of 6 mm^2 with a detection efficiency of 41 %. The total sensor readout takes an area of 72 mm^2 [27].

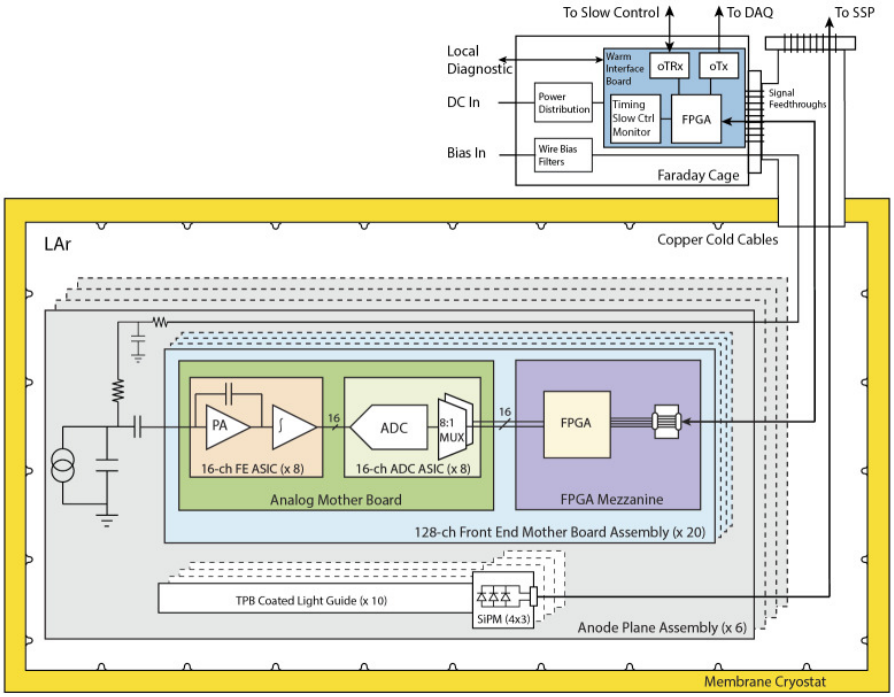

Figure 2.5: ProtoDUNE cryogenic electronics architecture. Picture taken from [27]

2.2.2 Enriched Xenon Observatory

The Enriched Xenon Observatory (EXO) is an experiment in particle physics aiming to detect a neutrino-less double beta decay. The double-beta decay is a second-order weak transition in which two neutrons simultaneously decay into two protons. The EXO experiment tries to observe the hypothetical neutrinoless mode ($0\nu\beta\beta$). The search for $0\nu\beta\beta$ is recognized as the most sensitive probe for the Majorana nature of neutrinos [28], [29].

EXO-200 is a 200-kg detector using Liquid Xenon (LXe). It was designed as a baseline for the future and a larger double beta decay detector. EXO 200 implements an LXe TPC at an operating temperature of 167 K. In this detector, the front-end electronics are

located outside the cryogenic environment and connect to the sensor by cabling. Each channel circuit (a total of 300 channels) is conformed by a low noise charge amplifier, two shapers (integrator and differentiator) stages. Next, the front-end feedthrough a sample-and-hold circuit and a 12 bit, 1 MS/s Analog to Digital Converter [30]. The Front-end architecture, shown in Figure 2.6, readout the photomultiplier tube (PMT).

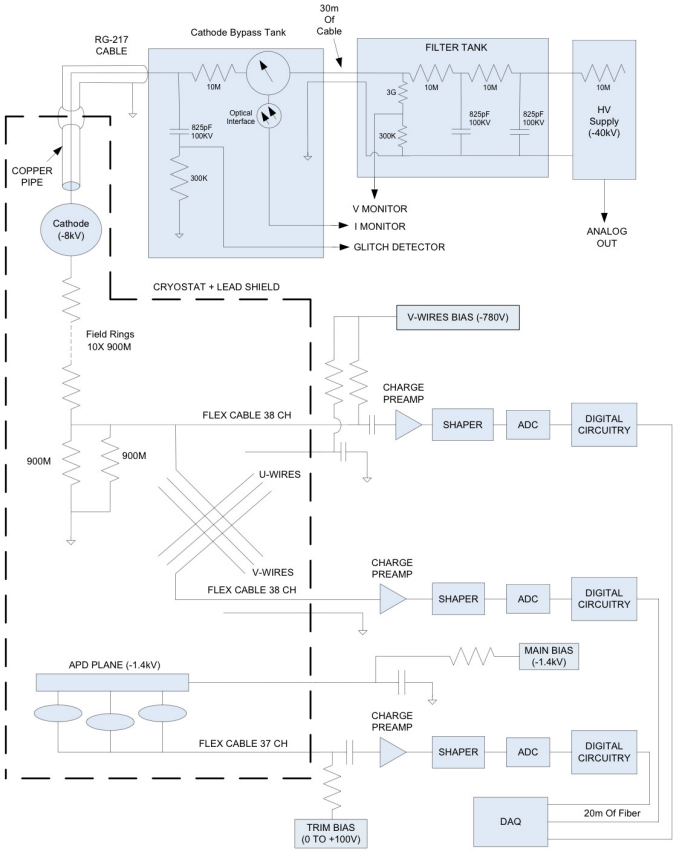

Figure 2.6: TPC biasing and readout electronics systems of EXO-200. Picture taken from [30]

2.2.3 XENON

XENON is a dark matter experiment to detect the nuclear recoils ensuing from the dispersion of the Weakly Interacting Massive Particles (WIMPs) within Liquid Xenon (LXe) [31]. The Xenon experiment has evolved over the years to increase the detection resolution (sensibility). The target of the resolution improvement is to detect the ever-elusive dark matter. The experiment starts with Xenon100, which contains 62 kg of LXe in a time projection chamber (TPC) [31]. Next, the project expected to Xenon1t with a TPC filled with 1 ton of LXe [32]. The last proposal is the construction of the XENONnt to operate a total of 8.3 tonnes of liquid xenon to search for the dark matter particles.

Experiments, such as Xenon100 and Xenon1t, has implemented the photomultiplier tube (PMT) with enhanced response in the vacuum ultraviolet (VUV) regime. Besides, the PMT presents a high photoelectron collection efficiency and high performance at cryogenic temperatures.

Xenon100 presents a data acquisition system that amplifies the 242 PMT signals by a factor of 10 using commercial Phillips 776 NIM amplifiers and then digitized by CAEN VME V1724 Flash ADCs with 10 ns sampling period, 14-bit resolution, 2.25 V full scale, and 40 MHz bandwidth. The front-end electronics (Figure 2.7) implements commercial components, which require additional filters to reduce the typical wide bandwidth of the commercial amplifier. This prototype locates the amplifiers and ADCs in a room temperature environment through 12 m PTFE-coated RG-196 coaxial cables.

On the other hand, the Xenon1t presents an identical front-end structure of Xenon100. The front-end electronics connected to the PMT through a coaxial cable perform a total gain equal to 10 within a warm data acquisition [33]. Finally, the XENONnt project is currently in construction with 496 PMTs for signal read-out.

Xenon dark matter experiment does not include the read-out electronics within the cryogenic environment close to the detector. Hence, the detection efficiency may be reduced due to the physical distance between the sensor and the reading electronics.

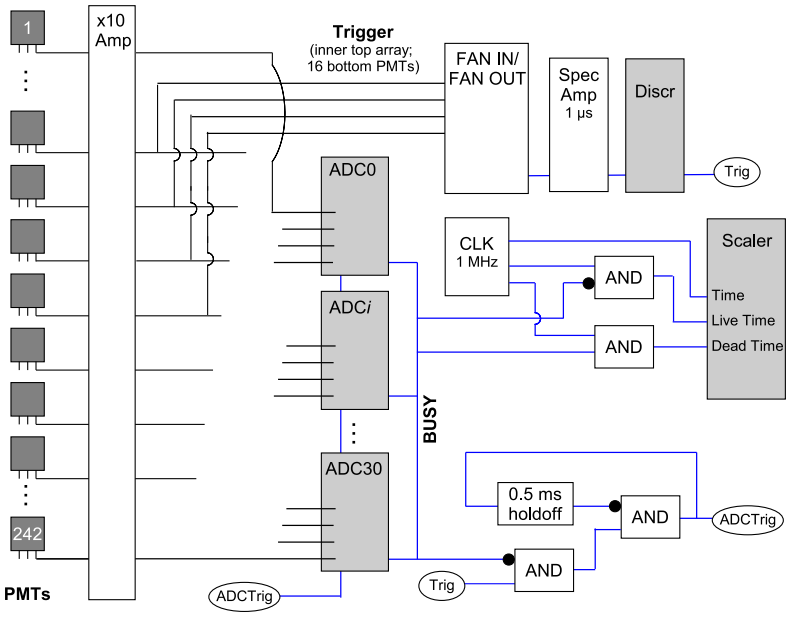

Figure 2.7: Data acquisition schematic for all 242 PMT realized in XENON100 experiment. Picture taken from [31]

2.2.4 DarkSide 50

DarkSide-50 (DS50) is classified as a dark matter experiment for searching the weak interactive massive particles (WIMPs). DS50 was the first physics detector of the DarkSide program. The experiment implements a TPC of 46 kg active volume of Liquid Argon, which has produced the first WIMP search results using a low-radioactivity underground argon [34].

DS-50 contains 38 3" PMTs distributed on the top (19 PMTs) and on the bottom (19 PMTs) of the TPC [35]. The low-gain front-end electronics were mounted directly on the PMT sensor inside the cryogenic environment [36], to reduce the parasitic connections and losses generated by cabling connected to a warm amplification. The cold electronics (Figure 2.8) was designed using a commercial JFET, and a figure of merit to generate a low-noise in the input JFETs and output drive transistor.

The output signal from the cryogenic front-end is guided to the warm data processing area. In this structure, the output analog signal is buffered and digitized, as shown the Figure 2.9. The DS-50 has been used as a baseline for DarkSide20K. The last and bigger prototype of the Darkside collaboration.

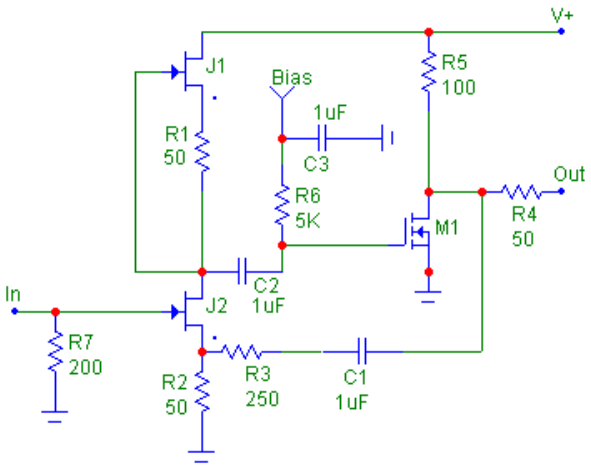

Figure 2.8: Block diagram of the DarkSide 50 Front-End-Module. Picture taken from [36]

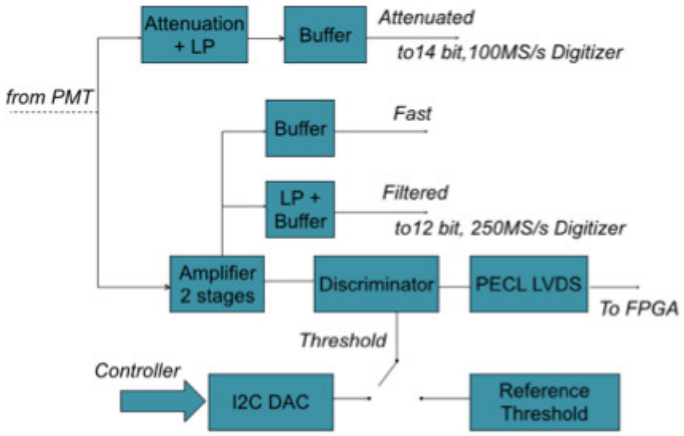

Figure 2.9: Block diagram of the DarkSide 50 Front-End-Module. Picture was taken from [36]

2.3 Cryogenic electronics for DarkSide-20K experiment

Dark matter particles may conform to a large percentage of the matter in the universe with dark energy. Theoretically, the dark martter may be composed of weakly interacting massive particles (WIMPs) [37]. However, the particle does not exist in the Standard Model [38] and has not been directly observed yet at any experiment. The observation of the WIMPs could demonstrate the existence of dark matter and would be a great advance in the mission to know the universe and its origin.

DarkSide 20K is a direct WIMP search using a Time Projection Chamber (TPC) of 20 tonnes of Liquid Argon fiducial mass, shown in Figure 2.10. The LAr TPC is deployed within a Veto system with an octagon Liquid Scintillator Veto (LSV), as shown the Figure 2.10. VETO aims to reject or follow-up closely the non-WIMP events.

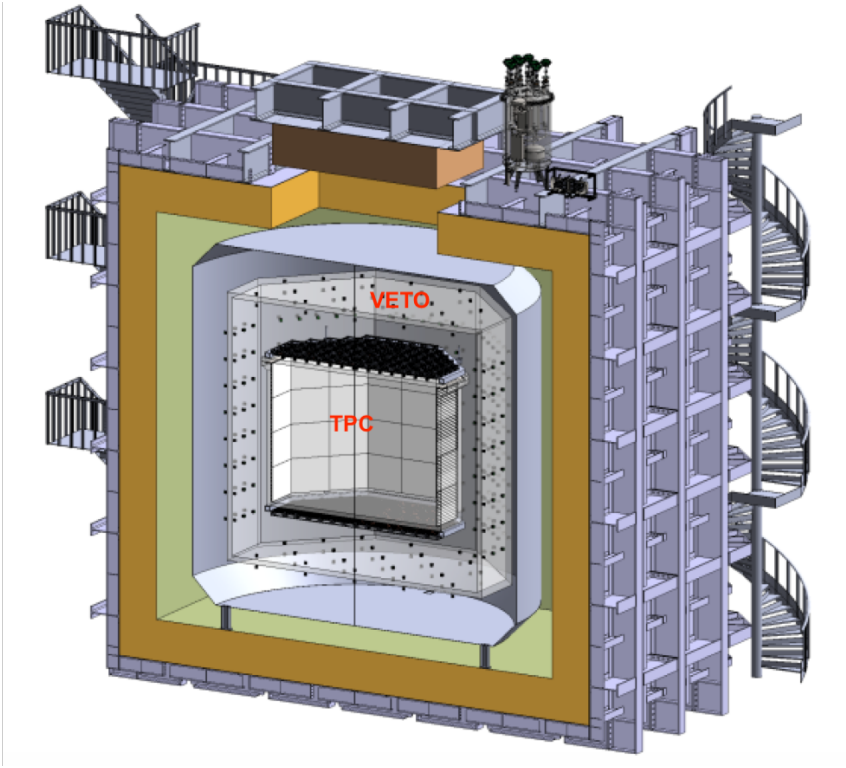

Figure 2.10: Preliminary prototype of DarkSide 20K. The picture was taken from [39]

An event inside the TPC can be produced by electron and nuclei recoil, which release energy within Liquid Argon, then it produces a direct excitation, generating a fast

scintillation signal (S1). The remaining free electrons of recombination are accelerated by an electric field up to be extracted from Liquid Argon. The accelerated electrons excite the Argon gas on the top of the TPC. Then, this generates a secondary scintillation signal, called S2. The S2 acquisition provides the 3D position of particles as shown the Figure 2.11. The 3D position is crucial to figure out how much energy the particles realease in the Liquid Argon.

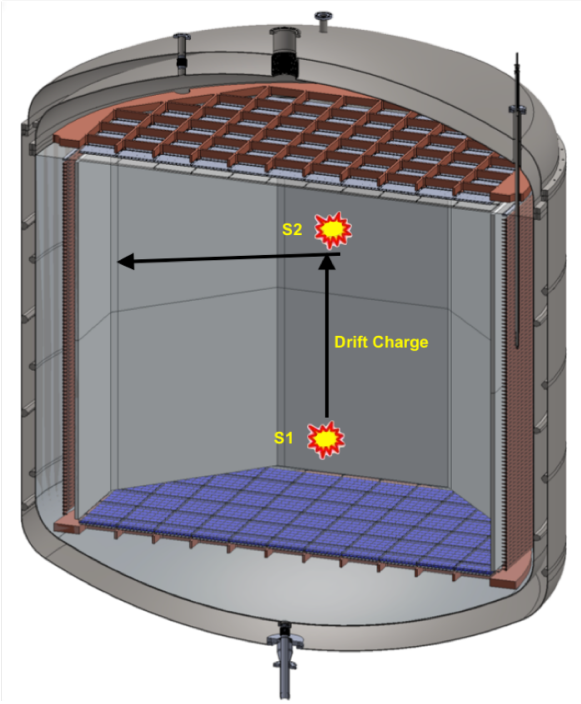

Figure 2.11: Time projection chamber system implemented within DarkSide 20k. Picture taken from [39]

Several photodetection modules (PDMs) are integrated within the walls of the VETO system (shown Figure 2.10) and in the TPC. PDM structures are integrated by a cryogenic front-end electronics mounted on an array of 24 cm^2 SiPM. The analog output signal is transported to the warm data acquisition through the optical fiber. Thus, an optical transceiver is connected to the PDM's signal.

This study is focused on the development of the integrated cryogenic electronics design for the VETO system of the Darkside 20k experiment. VETO structure requires around 3000 PDMs distributed along with the whole structure, as shown the Figure

2.12. The PDM structure is placed on the black point located on the wall of the VETO structure.

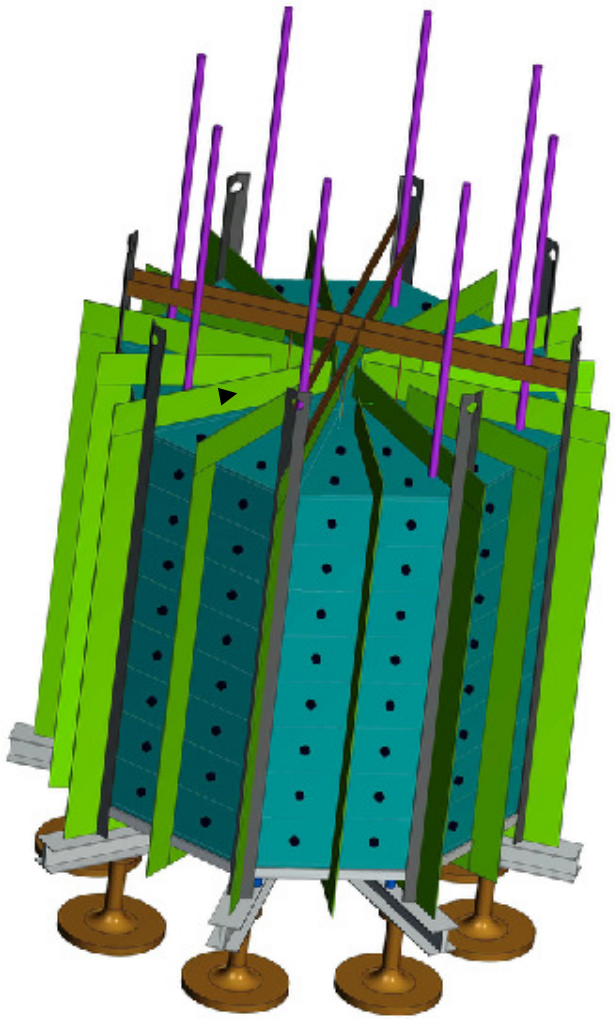

Figure 2.12: VETO system implemented within DarkSide 20k.

Integrated cryogenic electronics for VETO systems implements in a 110 nm CMOS technology. Before the electronic design, careful and deep studies of the single transistor were performed to analyze and comprehend the behavior of technology at 77 K. The temperature of 77 K results from the usage of Liquid Nitrogen (LN) to test the electronics, because LN is much easier and cheaper to implement in the laboratory than Liquid

Argon.

Afterward, the successful results obtained from the first cryogenic electronics prototype have pushed us to realize a second tape-out. The new prototype optimizes the previous results and includes an single-ended to differential converter. Furthermore, the new front-end implements in a new 110 nm CMOS technology. The new CMOS technology implements a 4-metal interconnection, which may cause problems, for instance, a considerable IR drop due to the large interconnection resistivity. It makes the IC layout structure be changed to avoid large IR drops. The idea of the second tape-out is to test a new 110 nm technology ay cryogenic temperatures. The new electronics version presents improvements in terms of the dynamic range and SNR in comparison to ASIC v1. In the ASIC v2, a differential signaling allows the VETO system signal to be led to warm data acquisition by cabling instead of the optical fiber. However, ASIC v2 implements a power domain for the amplification and signal conversion stage. Then, the converter circuit can turn off in the case that only a single-ended output is required.

2.3.1 Conclusion

A couple of underground astroparticle experiments have developed the detector using warm front-end electronics, inducing many parasitic components and losses. Other detector prototypes, such as ProtoDUNE and DarkSide 50, have decided to include the first amplification step inside the cryostat to improve signal efficiency. The previous detectors have designed cryogenic electronics using discrete or commercial components. In the case of DarkSide 20k, the discrete electronics may be big trouble due to the large sensor capacitance (> 10 nF). This new condition demands the inclusion of additional filtering stages and offline signal processing. Otherwise, it becomes complex to achieve an acceptable signal to noise ratio.

Implementing an integrated electronics, the internal parameters of the circuit could be tuned by external bias currents and voltages. The tuning especially allows the input transistors trans-conductance to be modified when the integrated circuit passes from 300 K to 77 K. The biases tunning provides flexibility hard to find in discrete electronics.

Chapter 3

Cryogenic CMOS electronics

The use of CMOS electronics at cryogenic temperatures offers relevant device enhancements in terms of RMS noise, power dissipation, electromigration, and overheating. The reduction of power consumption with respect to 300 K operation for the same or improved performance is particularly significant for digital circuits. [40]. Furthermore, cryogenic operation is mandatory in many fields, ranging from quantum computing [41] to new generation underground detectors for dark matter and neutrino experiments [41].

Unfortunately, cryogenic operation has also several drawbacks. For instance, CMOS technology exhibits a sensitive degradation due to the hot carrier effect. This degradation could be reduced considerably by an optimal transistor design. In this way, the lifetime of transistors is extended more than 20 years. In this chapter the advantages of using a CMOS tecnologies at cryogenic temepratures are discussed, along with the drawbacks and main solutions to circumvent them.

[42].

3.1 Advantages of CMOS electronic at 77 K

CMOS technology performs improvements concerning the carrier mobility, power consumption, thermal noise, transit frequency of a single transistor at a cryogenic temperature of 77 K [43]. Besides, the transistors and metalization do not suffer the effect of electromigration and heating. The behavior of carrier mobility, threshold voltage, slope factor is considered and analyzed in this study.

3.1.1 Carrier mobility

Carrier mobility establishes the effective velocity of electrons or holes under an electric field effect. In this way, scattering mechanisms determine the magnitude of the transistor parameters. The mechanisms allow the momentum and kinetic energy of electrons/holes to be exchanged with the environment [44]. The scattering includes mechanisms as a result of the lattice vibration and charges ionized impurity atoms. All these are represented by the Equation 3.1.

$$\frac{1}{\mu_{eff}} \propto \frac{1}{\mu_{pii}} + \frac{1}{\mu_{vs}} + \frac{1}{\mu_{cc}} + \frac{1}{\mu_{ni}} \tag{3.1}$$

where:

- μ_{eff}, total effective carrier mobility;
- μ_{pii}, phonon and ionized impurity scattering;
- μ_{vs}, velocity saturation scattering;
- μ_{cc}, carrier to carrier collisions scattering;
- μ_{ni}, neutral impurity scattering.

Each scattering mechanism depends on the temperature in different ways, therefore the effective carrier mobility is modified following the strongest mechanism variation and magnitude. Firstly, the phonon scattering contribution is considered:

Phonon scattering

Phonon scattering occurs due to electron-phonon interactions. For instance, the hole scatters because of interacting with crystal vibration. The energy bandgap depends on the lattice constant, which changes with the lattice vibration [45]. The crystal vibration alters the periodic crystal structure by producing a scattering of hole wave. As a result, the carrier mobility of phonon is represented by the equation 3.2 [46].

$$\mu_{ph} = \frac{q\tau_{ph}}{m} \tag{3.2}$$

Where τ_{ph} is the mean free time of phonon scattering. The mean free time highly depends on the inverse of phonon density and the thermal velocity, which converts μ_{ph} into a temperature-dependent variable. Thus, the carrier mobility of phonon due to the temperature is represented by equation 3.3. This parameter considerably increases as the temperature decreases.

$$\mu_{ph} \propto \tau_{ph} \propto \frac{1}{ph_{density} thermal velocity} \propto \frac{1}{T\sqrt{T}} \tag{3.3}$$

Ionized impurity scattering

Ionized impurity is a scattering mechanism produced by the high doping concentration. The high concentration level is typical of scaling down technology to improve its electrical performance [45]. Thus, a consequence of this high doping is a carrier mobility reduction as a result of an increase of scattering center, which interferes with the carrier motion. The electrons or holes can be scattered by either a donor or an acceptor ion [46].

Carrier mobility due to ionized impurity scattering is inversely proportional to the donor or acceptor ion concentrations. However, it is proportional to T, as illustrate the Equation 3.4.

$$\mu_{iie} = \sqrt{\frac{\pi}{m_e}} \frac{64\epsilon_s^2 (2kT)}{q^3 N_{ii}} [\frac{1}{ln(1+x) - \frac{x}{1+x}}] \tag{3.4}$$

Ionized impurity and phonon scattering behavior over temperatures and doping concentration are illustrated in Figure 3.1.

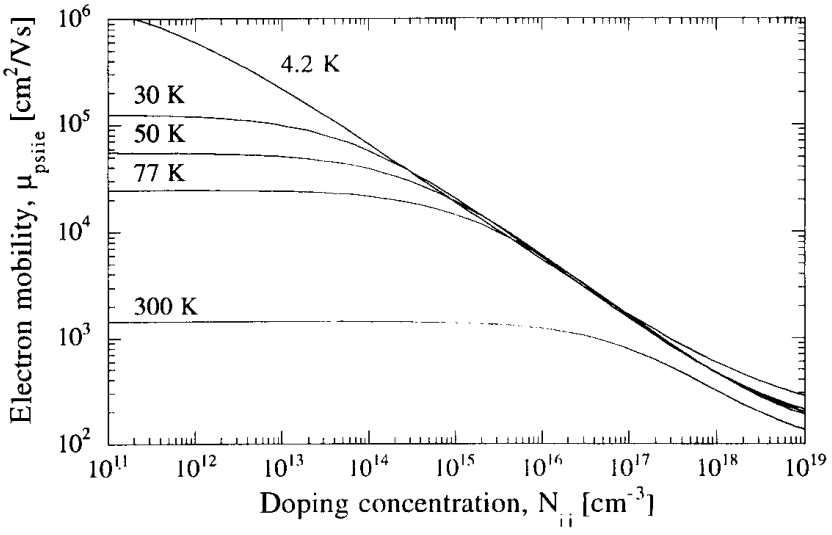

Figure 3.1: Phonon and ionized impurity scattering vs doping concentration at different operation temperatures, graphic taken from [45].

Velocity saturation scattering

CMOS devices under a large applied electric field always present a drift velocity with a saturation around $10^7 \frac{cm}{s}$. Because once the carrier kinetic energy overcomes the optical phonon energy. The devices generate an optical phonon, and consequently losses the kinetic energy [46].

The electron and hole mobility of the velocity saturation perform different temperature variation, as described the Equation 3.5 and 3.6.

$$\mu_{vse} = 10^7 \frac{T}{300}^{-0.87} \qquad \text{[cm/s]} \tag{3.5}$$

$$\mu_{vsh} = 8.37^6 \frac{T}{300}^{-0.52} \qquad \text{[cm/s]} \tag{3.6}$$

Carrier to carrier collisions scattering

Carrier to carrier scattering is a mechanism generated in submicron devices because of high current densities. In other words, the high carrier concentration modifies the formed mobility by the inter-carrier scattering. The optimal model, studied for this process, is described by the Equation 3.7 [47].

$$\mu_{cc} = \frac{2 * 10^{17}/\sqrt{np}}{ln(1 + 8.28 * 10^8 T^2 (np)^{-1/3})} \tag{3.7}$$

Where n and p represent the level of electrons and holes. The scattering is inversely proportional to the temperature.

Neutral impurity scattering

Neutral impurity mechanism affects semiconductor with doping levels below the degeneration level ($10^{18} cm^3$). It becomes a significant factor at temperatures below 125 K. The Equation 3.8 represents the neutral scattering mechanism with its temperature dependence. This model was developed by Erginsoy [48].

$$\mu_{ni} = C_o[\frac{2}{3}\sqrt{\frac{KT}{E_{ni}}} + \frac{1}{3}\sqrt{\frac{E_{ni}}{KT}}] \tag{3.8}$$

Assuming that a large portion of the impurities is ionized, and the operating currents are well below the high-injection. In this condition, the most significant contributors to the effective carrier mobility are the phonon, ionized impurity, and velocity saturation scattering. Then, the effective carrier mobility increases around twice between 300 K and 4.2 K. It is considering an electric field below 10^4, as shown the Figure 3.4.

As a result, the carrier mobility owns a temperature dependence involving all the scattering mechanisms. Hence, the rough carrier mobility equation because of the temperature variation is described by Equation 3.9 [44].

$$\mu_{eff}(T) \propto \mu_{eff}(T_{room})(\frac{T}{300})^{-k_3} \tag{3.9}$$

Where k_3 is a constant, which presents values from 1.2 to 2.

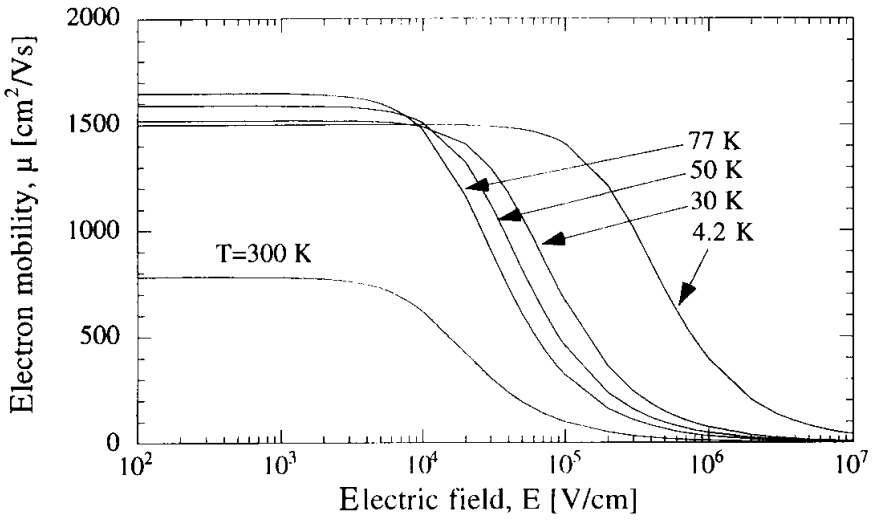

Figure 3.2: Electron mobility vs electric field at different operation temperatures, graphic taken from [45].

3.1.2 Thermal and low frequency noise

Thermal noise is a disturbance caused by thermal agitation of electrons in a conductor [49]. Besides, the thermal noise acquires a random component in their motion, as shown the Figure 3.3. The noise component disappears at absolute zero.

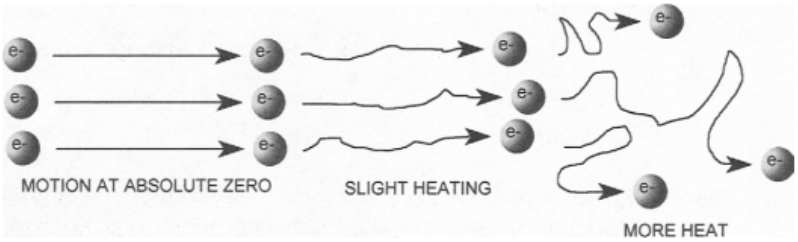

Figure 3.3: Electron response under heating. Picture taken from [49].

The thermal noise spectrum is modeled by Equation 3.10. Where β constant is a bias-dependent parameter, which presents a value of 1/2 in weak inversion and 2/3 in strong inversion [50]. It is possible to infer from the Equation 3.10 that thermal noise is reduced at cryogenic temperatures due to the kT term.

$$S_{Vg} = e_n^2 = \beta \frac{4kT}{g_m} \tag{3.10}$$

On the other hand, low frequency or flicker noise caused by the imperfections in crystalline structure [49]. Flicker noise shows a clear dependence on the overdrive voltage, as shown in its representative Equation 3.11. Considering that there is no a consolidated noise representation, the low-frequency noise has been modeled by two theories. One is the mobility fluctuation ($\Delta\mu$), and secondly, the carrier density fluctuation (ΔN). The carrier density fluctuation theory is validated by using the drain current noise modeled by the Reimbold approximation described by the Equation 3.12 [51].

$$S_{Vg}(f) = \frac{q}{C_{ox}} \frac{\alpha_H}{WLf}(V_{gs} - V_{th}) \tag{3.11}$$

$$\frac{S_I}{I_D^2} = \frac{q^2}{a^2 WLkfT\alpha_{tunn}} \frac{N_T(E_g)}{C_{ox} + C_D + C_{it} + C_i} \tag{3.12}$$

Where C_i is the inversion layer capacitance per unit area, C_D is the corresponding depletion layer capacitance, and $C_{it} = \frac{gNit}{kT}$ represents the interface trap capacitance.

Assuming the two flicker noise theories, a unified flicker noise theory has been developed considering both the density and the correlated mobility fluctuations through the carrier scattering. These aspects provides a normalized drain current noise spectral density represented by the Equation 3.13 [52].

$$\frac{S_I}{I_D^2} = \frac{kT}{WLfT\alpha_{tunn}} (\frac{1}{N} + \alpha_{scatt}\mu)^2 N_T(E_F) \tag{3.13}$$

Afterward, the flicker noise behavior of pMOS structure at different frequencies is illustrated by Figure 3.4. This graph shows the increasing trend of low-frequency noise at temperatures below 80 K and becomes a critical factor below 25 K.

3.1.3 Transit Frequency and Power consumption

Transit frequency or cut-off frequency is a measure of the intrinsic speed of a transistor. It is defined as the frequency where the current gain falls to 1. The transit frequency of a single transistor is computed by the Equation 3.14.

$$f_T = \frac{g_m}{2\pi C_{GS}} \tag{3.14}$$

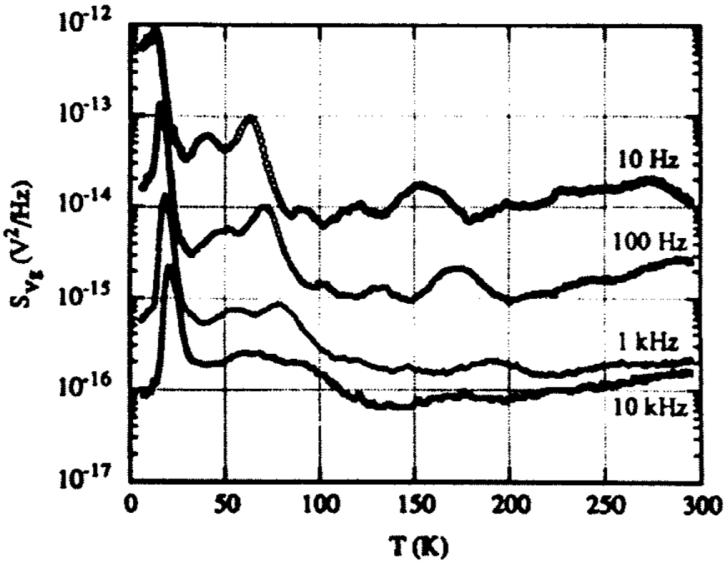

Figure 3.4: LF noise versus temperature scan for a pMOS in a range of 6 - 295 K. Graph taken from [53].

Transit frequency proportionally depends on the transconductance as shown the Equation 3.14. Then, assuming a weak inversion operation the f_T increases at low temperatures by the thermal term kT ($G_m = \frac{I_d}{nV_T}$). The f_T growth follows the factor expressed by the Equation 3.15 considering identical bias current conditions. On the other side, a strong inversion condition modifies the increment ratio of transit frequency, since the cut-off frequency (f_T) will depends on a new factor expressed by the Equation 3.16, which is not linear as in weak inversion condition.

$$f_{T77K} = \frac{T_{300K}}{T_{77K}} \frac{n_{77K}}{n_{300K}} f_{T300K} \tag{3.15}$$

$$f_{T77K} = \sqrt{\frac{\mu_{n_{77k}}}{\mu_{n_{300k}}}} f_{T300K} \tag{3.16}$$

Where the n_{77K} and n_{300K} represent the slope factors at that temperature. T represents the operation temperature in Kelvins. The f_T increment must be analyzed carefully in a full transistor-level design of an operational amplifier, because it could modify the poles and zeros of the circuit, causing an uncontrollable or unknown gain bandwidth and phase margin. As a result, the circuit could be led to an unstable region.

Moreover, the power consumption of a transistor could be reduced by the same factor of the transit frequency (Equation 3.15, 3.16). But in this case, the power reduction is generated by reducing the bias current up to obtain the room temperature transconductance [54]. As a result, the f_T is reduced up to its room temperature value.

3.1.4 Electromigration and series resistance

Electromigration is considered as a flux of atoms in the electrons' flow direction. The atom flux produces structure damage, resistance increases, and electrical failures in the interconnection [55]. Then, the electromigration becomes a crucial factor of circuit reliability, since if a single interconnection fails, the entire device no longer works as required. The phenomenon is rather general and happens in solids, liquids, and gases.

Every metal interconnection presents a maximum current density to avoid electromigration. The maximum current density is reduced substantially by the temperature increases [56]. As a result, the failure probability increases under high-temperature conditions. For this reason, the cryogenic operation condition allows the metal to be handled with a much higher current density. Hence, a much lower probability of the electromigration effect.

On the other hand, the series resistance is composed of the drain, source, and channel resistance of the transistor. Series resistance produces a voltage drop on the transistor, generating power consumption. In other words, drain-source resistances are considered as parasitic components, which increases the power dissipation of the transistor. In cryogenic temperatures, the total series resistance is reduced, and thus, the power consumption for a single transistor either. [57].

3.1.5 Interconnect resistance

Interconnection between the transistors becomes a meaningful factor in integrated circuit design, because their parasitic resistance and capacitance contribute to increase the propagation delay. Cryogenic temperature offers ICs important advantages in terms of interconnecting resistivity. Here, resistivity is significantly reduced in each MOSFET components, as shown in Table 3.1.

Resistance	300 K	77 K	4.2 K
N+ Diffusion	1	0.76	0.72
Polysilicon	1	0.89	0.88
Alluminium	1	0.14	0.05
P-well	1	0.3	10^{-5}

Table 3.1: Normalized resistance over temperatures in CMOS technology. Table is taken from [43]

3.2 Drawbacks of CMOS electronic at 77 K

3.2.1 Hot carrier degradation

Hot carrier (HC) degradation is an important issue related to carrier transport and interactions in thin layers. The main effect of these energetic carriers is to create additional electron-hole pairs close to the drain. These electrons or holes might gain enough kinetic energy due to the electric field acceleration. The achieved kinetic energy will allow potential barriers to be overcome easily. Then, the electrons or holes can reach the Si/SiO interface. As a consequence, a gate current increment and a threshold voltage alteration are generated [58]. A characteristic of hot carriers is its high effective temperatures in comparison to the surrounding lattice carriers [59].

HC effect can be measured by both the variation of drain current, as shown in Figure 3.5 or the increment of drain-bulk current (I_{db}). The I_{db} grows up because electrons are shifted to the drain and holes are collected by the bulk [42].

Moreover, the HC effect must be lowered to guarantee a lifetime of the transistors for longer than 20 years. The reduction is realized by choosing the correct channel length parameter. In this case, the channel must be longer than the minimum channel technological length. Furthermore, HC probability is partially inhibited by reducing the voltage drop within the transistor. In other words, a low drain-source voltage cut lessens the transistor stress considerably, and thus the HC probability [9]. Figure 3.5 shows the lifetime of transistor considering difference channel length.

Afterward, the HC effect is more evident for electrons due to its higher reduction of lattice vibration, and thus the phonon scattering [45]. For this reason, nMOS transistors suffer the HC effect significantly more than the pMOS transistor. For instance, the HC probability of nMOS at 300 K is almost similar to the pMOS at 77 K [9].

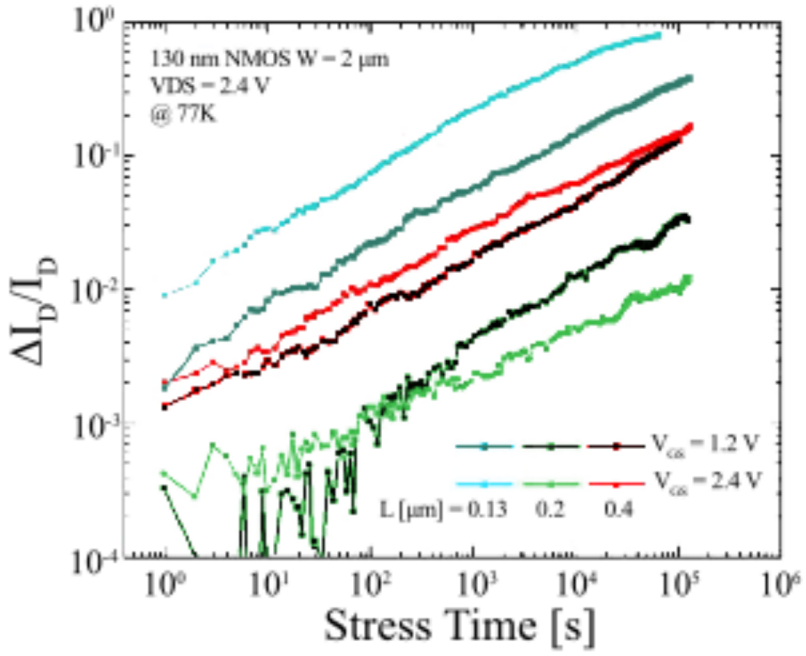

Figure 3.5: Lifetime of transistor 130 nm using different channel length at 77 K. Figure taken from [9]

3.2.2 Threshold voltage

The threshold voltage is defined as the total voltage to support an inversion layer in the MOS structure. In other words, it is the necessary gate-source voltage to form the channel in a MOS structure. For this reason, the threshold voltage is a fundamental parameter to define the operation regime of the transistor, such as sub-threshold, weak inversion, or strong inversion. The threshold voltage is represented by the Equation 3.17. Where, V_{FB} is the flat band voltage, ϕ_F represents the Fermi potential of the bulk, N_A is the acceptor concentration and ϵ_{Si} is the permittivity constant of silicon.

$$V_{th0} = V_{FB} + 2\phi_F + \frac{1}{C_{ox}}\sqrt{2\epsilon_{Si}qN_A 2\phi_F} \tag{3.17}$$

In a cryogenic environment (77 K), the threshold voltage is affected substantially, since it may increase around 100-200 mV depending on the aspect ratio [60]. The V_{th} growth is produced by the silicon bandgap and the Fermi potential ϕ_F, which are temperature dependence (Equation 3.18).

Fermi potential growth is produced by the strong reduction of n_i considering a complete ionization, as shown Figure 3.6, despite its direct dependence on thermal voltage $V_T = \frac{kT}{q}$ [60]. As a result, the threshold voltage partially rises by following the Fermi potential growth, as this provides the most significant magnitude of the V_{th} ascent [45]. Moreover, the ϕ_F growth is too sharp and not substantially accurate. The total variation of ϕ_F may reach values from 0.1 V to 0.5 V depending on N_A, as is described by the Figure 3.18.

$$\phi_F = V_T ln \frac{N_A}{n_i} \tag{3.18}$$

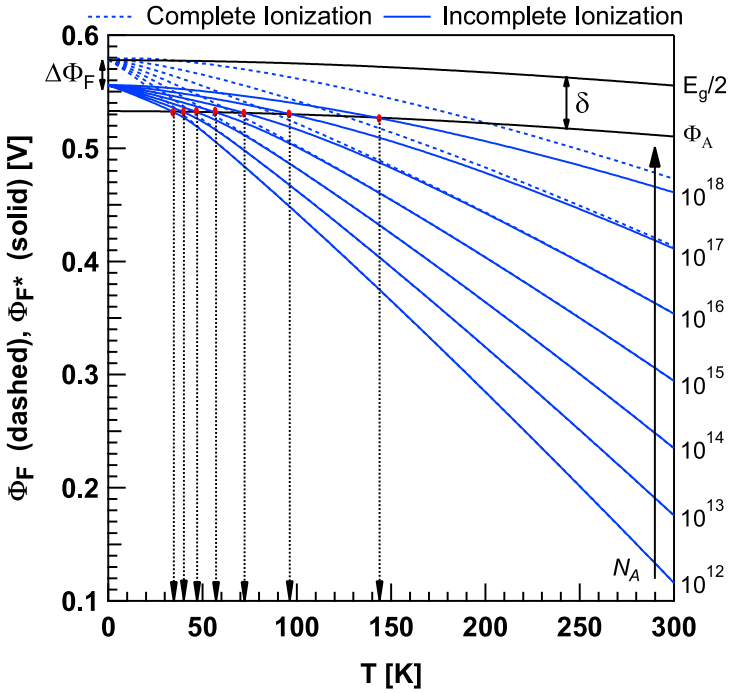

Figure 3.6: Fermi potential in a NMOS transistor over temperature. Figure taken from [60] .

Threshold voltage variation becomes a delicate issue in the low-voltage electronics design, since there are critical paths which require a low threshold voltage to guarantee its functionality [60]. Otherwise, the transistor or circuit may remain off or with low performance. Due to threshold voltage variation, a weak inversion regime becomes an optimal option for operation because of its low require overdrive voltage.

3.3 Key parameters extraction of 110 nm CMOS technology at 300 K and 77 K

CMOS technology presents internal parameter variations between 300 K and 77 K. The parameter variations of single transistors were extracted at both temperature conditions. As a result, the single transistor results were useful to realize the correct transistor-level design of a full architecture at 77 K. Single transistor tests were applied to two different 110 nm technologies. In both technologies, the key parameters, such as threshold voltage, carrier mobility, and mobility attenuation, were extracted from pMOS and nMOS structures.

The extraction parameters were realized utilizing two samples per form factor (W/L). The two sample results were averaged to obtain a final extraction per W/L. The number of tested devices is low since the mean idea was not to realize statistics but to extract an approximated value of each parameter

3.3.1 Threshold voltage extraction

Threshold voltage extraction implements the Extrapolation in Linear Region (ELR) method [61]. The ELR method determines the threshold voltage V_{th} by locating the interception of drain current curve at V_g axis in a linear extrapolation. The extrapolation exploits the drain current slope at the maximum trans-conductance (G_{max}) zone. With this method, the V_{th} result presents a variability of $\pm$25 mV.

The transistor must be in a strong saturation regime of the linear region for the ELR method application. Figure 3.7 (left) describes the current and trans-conductance (g_m) curve over the gate voltage of nMOS transistor at temperatures of 77 K and 300 K. g_m curve illustrates the point with G_{max} in order to generate the linear extrapolation. Indeed, Figure 3.7(right) shows the straight line crossing the zero current axis to locate the approximate V_{th}. From these figures, it is substantially evident how trans-conductance, drain current, and threshold voltage increase from 300 K to 77 K, as is expected.

In order to obtain a generalized analysis of threshold voltage variation, V_{th} was extracted from pMOS and nMOS structures with different aspect ratios and technologies. The V_{th} behavior is described by Figure 3.8, which specifies the two technologies, as Tech 1 and Tech 2. The graph becomes a key result for cryogenic frontier electronic design, because it helps to know the threshold voltage increment and consider it during transistor sizing.

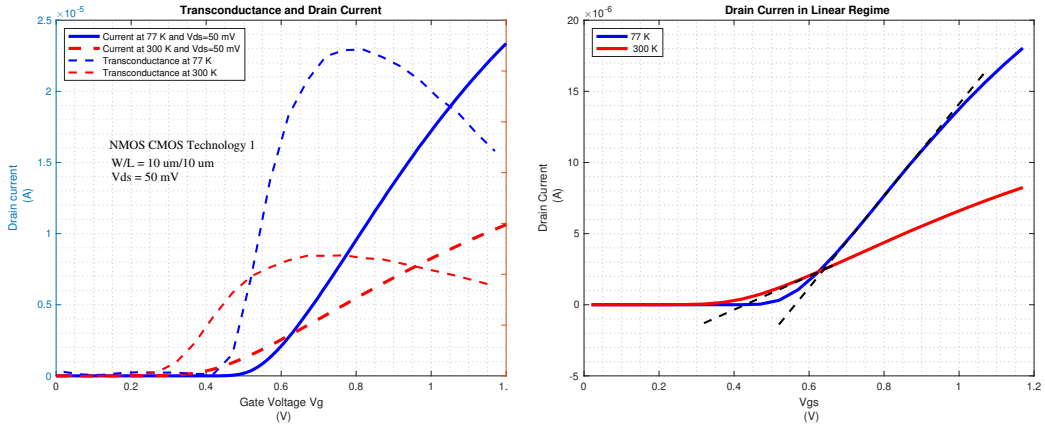

Figure 3.7: Drain Current and Transconductance curve in strong inversion regime of the CMOS linear region (left) and linear extrapolation curve (right).

Single transistor results make evident an expected growth of threshold voltages from 80 mV to 140 mV. Besides, it is possible to infer from the extraction results that the increment of V_{th} is correlated with the channel length due to the, V_{th} growth. It becomes higher in the transistor with a longer channel length, as shown in Figure 3.8.

3.3.2 Low field mobility

Low field mobility (μ_0) is another key parameter since it allows the right transistor sizing to be carried out for a circuit design at a cryogenic temperature of 77 K. Mobility extraction is performed by driving the transistor in a strong inversion regime of the CMOS linear region. This condition is mandatory to realize the correct extraction. The low field mobility extraction method consists of a combination of the drain current expression (Equation 3.19) in the linear region and its derivative expression concerning the gate voltage. Trans-conductance result from the derivative is expressed by the Equation 3.20 [62].

$$I_d = M\frac{(V_{gs} - V_{th})}{1 + \Theta(V_{gs} - V_{th})} \tag{3.19}$$

$$g_m = M\frac{1}{[1 + \Theta(V_{gs} - V_{th})]^2} \tag{3.20}$$

Where, M is equal to $\frac{W}{L}C_{ox}\mu_o V_d$, and Θ represents the mobility attenuation factor.

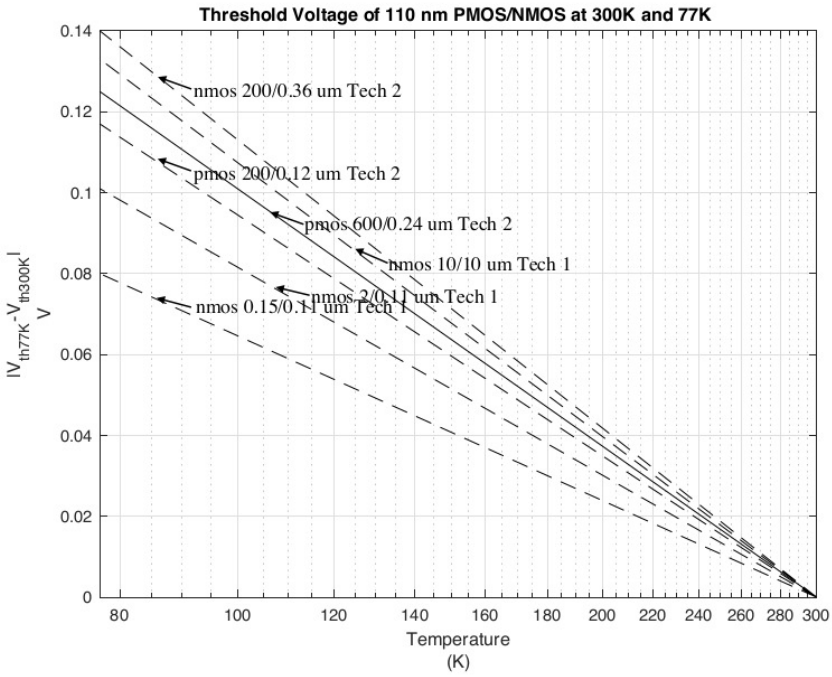

Figure 3.8: Threshold voltage variation at 300 K and 77 K, considering the pMOS and nMOS structure of two 110 nm technologies (Tech1 and Tech 2). The figure only represents the points at 300 K and 77 K. This means the curve does not present a linear behavior in the intermediate temperatures, but just a unification of 2 temperature corners.

Both I_d and g_m strongly depends on the Θ factor. However, this variable is canceled by the combination of Equation 3.19 and 3.20. The equation combination generates a final expression (Equation 3.21) to extract the low field mobility without dependence of mobility attenuation.

$$\frac{I_d}{g_m^{1/2}} = M^{1/2}(V_{gs} - V_{th}) \tag{3.21}$$

μ_0 extraction is implemented by plotting the $\frac{I_d}{g_m^{1/2}}$ expression vs V_{gs}, as shown Figure 3.9. The graph is represented by a linear curve with a maximum slope equal to $M^{1/2}$. From the previous expression, the low field mobility becomes the unique unknown variable, then μ_0 value is achieved by replacing the variables with its foundry value.

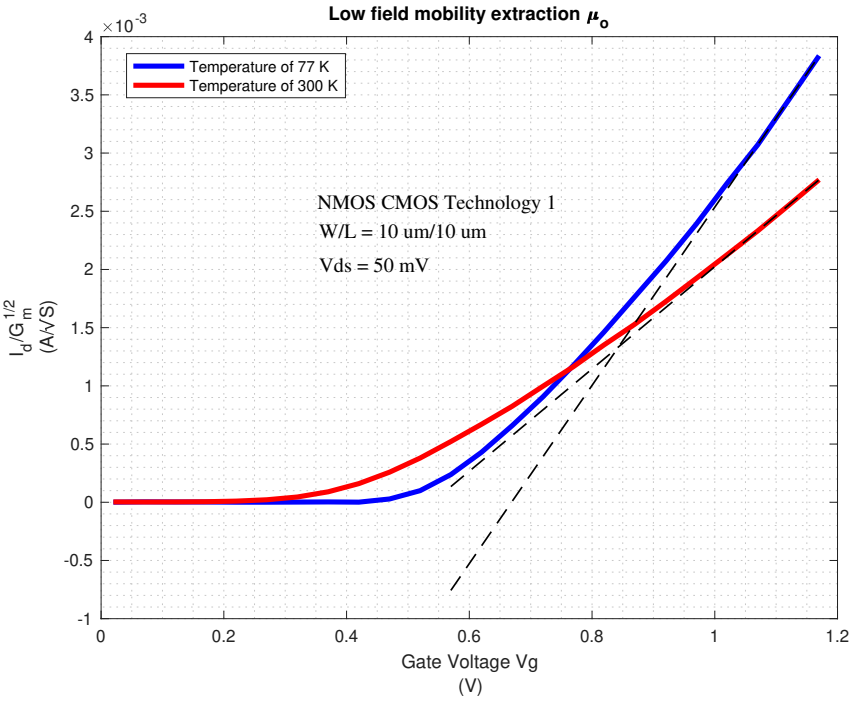

Figure 3.9: CMOS low field mobility extraction at 300 K and 77 K.

Low field mobility, as the threshold voltage, was extracted from a couple of transistors with different aspect ratios and channel lengths. Figure 3.10 provides the μ_0 variation over temperature, which becomes significant information for transistor sizing at 77 K. In this way, the extraction results allow a precise trans-conductance value to be computed at 77 K. Otherwise, the temperature variation may generate a larger trans-conductance in comparison to the expected one. Since the mobility increment was not considered. Thus, an unknown g_m produces an unknown modification of pole and zero frequencies. As a consequence, the frequency spectrum variation leads the circuit to an unstable condition.

On the other hand, the typical ratio of electron and hole mobility($\frac{\mu_n}{\mu_p}$) of 110 nm technology is around 2.6-3 times at 300 K. This ratio remains almost uniform at 77 K, as can be appreciated in Figure 3.10. Besides, carrier mobility presents increments of 1.3 and 1.6 for pMOS. In the meantime, nMOS mobility develops a rise of 1.9 to 2.4 times higher than the mobility at 300 K, a shown Figure 3.11.

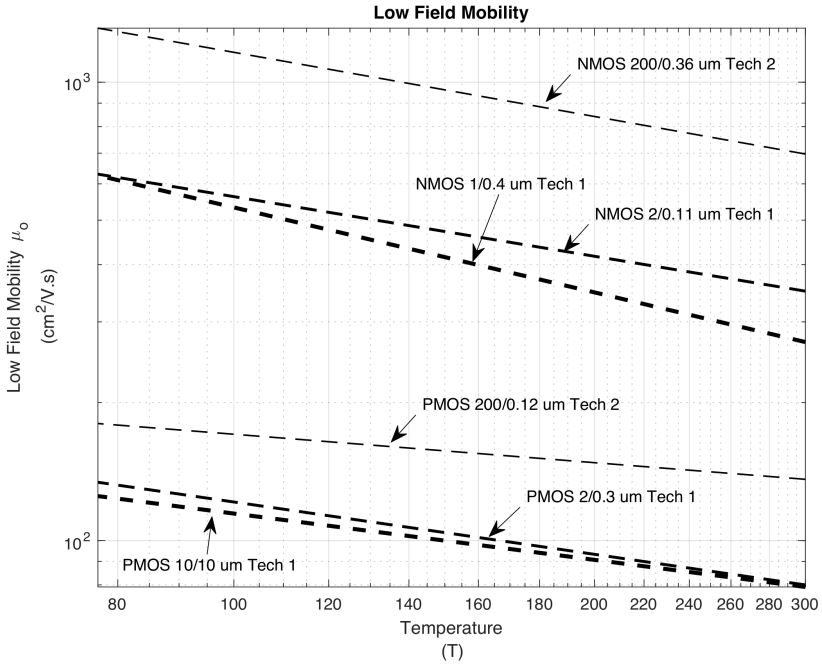

Figure 3.10: Low field mobility extracted from different transistor aspect ratio and technology at 300 K and 77 K. The figure only represents the points at 300 K and 77 K. This means the curve does not present a linear behavior in the intermediate temperatures.

Evidently, the carrier mobility of nMOS substantially performs a higher growth in comparison to the pMOS structure. This result goes according to the CMOS lifetime study [9]. Since the cited study has demonstrated that the nMOS transistors develop a larger hot carrier probability in comparison to pMOS structure due to its elevated phonon scattering at 77 K.

3.3.3 Series resistances

Series resistances (Equation 3.22) are formed by channel, source, and drain resistance. These parasitic components demonstrate an alteration of its value, as the temperature and gate voltage change. In the 110 nm CMOS extraction, the total series resistance decreases as temperature goes down, as shown the channel and drain-source resistance behavior in the Figure 3.13.

$$R_{serie} = R_{channel} * L + R_{drain} + R_{source} \tag{3.22}$$

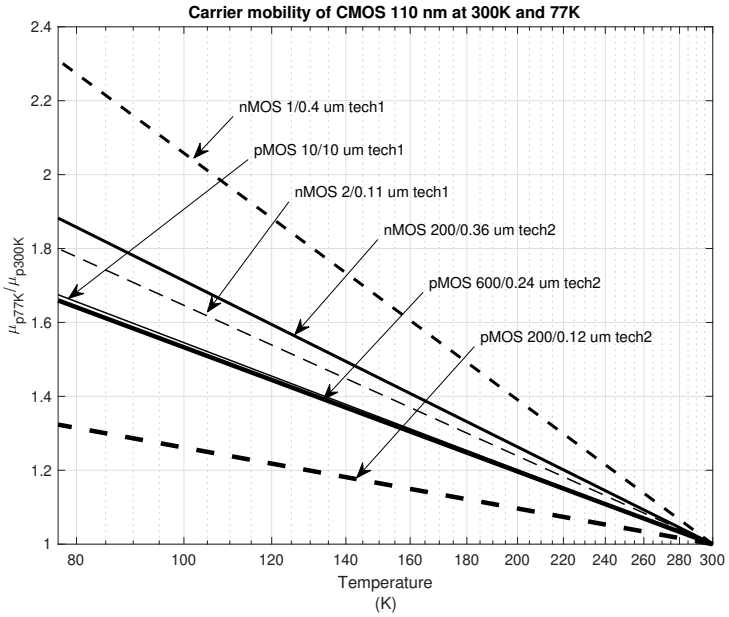

Figure 3.11: Normalized low field mobility in a CMOS technology. The figure just represents two points at 300 K and 77 K. This means the curve does not present any data in the intermediate temperatures.

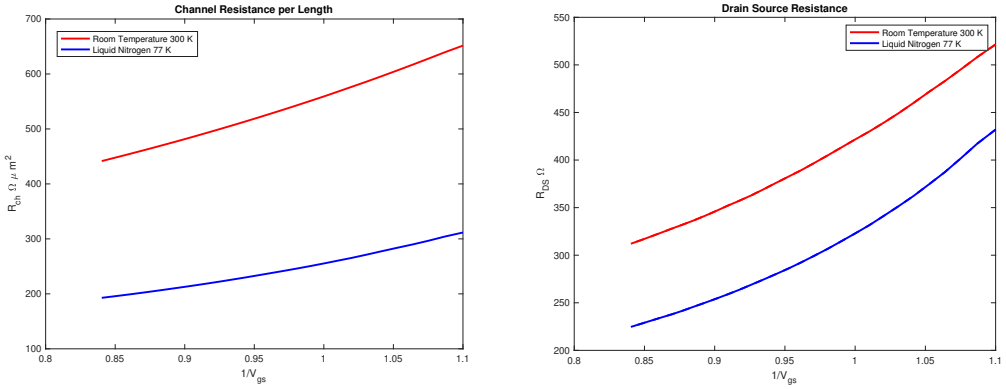

Figure 3.12: Channel per unit length resistance (left) and drain-source resistance (right) at 300 K and 77 K.

Both channel and drain-source resistance show a considerable reduction in a cold environment, as illustrated in Figure 3.12. In both cases, the resistances are almost halved in comparison to the value at room temperature. The series resistance extraction

performed the method presented in the study [57], and in this CMOS technology, the total series resistance is illustraed in Figure 3.13. The extraction technique allows the channel and the drain-source resistance to be analyzed separately.

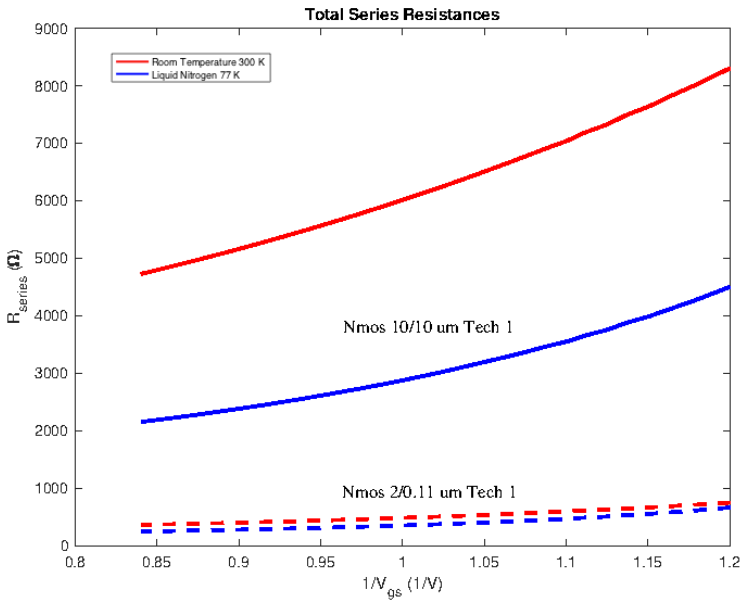

Figure 3.13: Total series resistance at 300 K and 77 K of 2 nMOS transistor with different channel length.

3.3.4 Mobility attenuation

Mobility attenuation is a key parameter generated by the normal field increment. The attenuation causes a reduction of low field mobility, becoming effective mobility. The normal field growth is physical despite the increasing contribution of surface roughness scattering in the carrier mobility. Mobility attenuation (Θ) slightly depends on the temperature, as is described by Figure 3.14 (right). The mobility attenuation extraction was performed by following the Equation 3.23 from [62]. However, the result of Θ is affected by the drain-source resistance (r_{DS}) of the transistor (Figure 3.14 left). Then, in order to isolate the r_{DS} term, the Equation 3.24 is implemented assuming that all variables are known from a previous μ extraction. An accurate mobility attenuation extraction is achieved by excluding the parasitic source/drain resistance, as is illustrated in Figure 3.14 (right).

$$\Theta = \frac{\frac{I_d}{g_m*(V_{gs}-V_{th})} - 1}{V_{gs} - V_{th}} \tag{3.23}$$

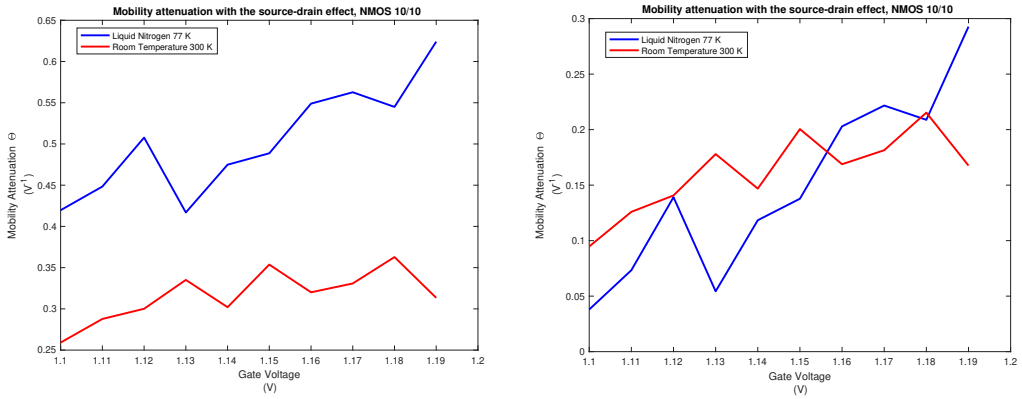

Figure 3.14: Mobility attenuation at 300 K and 77 K with the drain-source resistance effect (left) and without the drain-source resistance effect (right).

$$\Theta = \Theta_o + \frac{W}{L} C_{ox} \mu_o r_{DS} \tag{3.24}$$

3.3.5 Sub-threshold swing and slope factor

The sub-threshold swing (SS) is an outstanding MOSFET figure of merit, as it represents the minimum voltage swing needed to turn on a transistor. The SS establishes the minimum power supply voltages and the minimum power dissipation of a technology. SS provides an essential improvement as the temperature decreases. Since the typical SS parameter varies from 60-80 mV/dec at 300 K to 20-30 mV/dec at 77 K, as described the Figure 3.15. This means CMOS technology reduces the minimum power dissipation in comparison to the performance at 300 K.

On the other side, slope factor (n), defined as $n = 1 + \frac{C_d}{C_{ox}}$, presents a small increment at cold temperatures, as shown the Figure 3.15 (right). Notwithstanding, the n growth becomes a drawback because firstly it contributes to increasing the SS. Secondly, the transconductance of the transistor is slightly reduced by the term nV_T. Hence, the power consumption of transistor is not reduced anymore by the factor $\frac{V_{T300K}}{V_{T77K}}$, but the n ratio

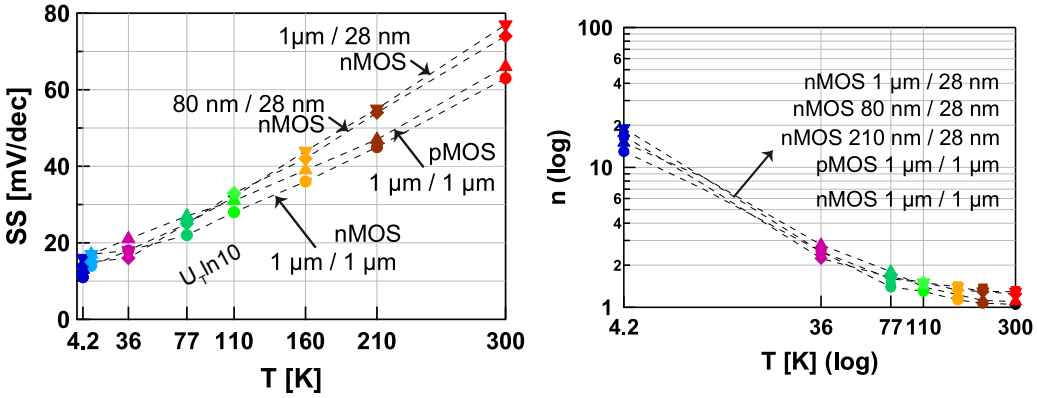

Figure 3.15: Sub-threshold swing (left) and the slope factor (right) behavior on temperature. Figure taken from [63]

is decreased in the power reduction factor. Even though n growth is not a crucial factor at 77 K due to its small variation (1.4), this becomes a relevant issue at 4.2 K in the spice of an increment of 10-20 times.

3.3.6 Normalized trans-conductance for weak and strong inversion regime

Normalized transconductance ($\frac{G_m n V_T}{I_d}$) represents the ratio between the trans-conductance (g_m) and maximum weak-inversion transconductance $g_{max} = \frac{I_d}{nV_T}$. The unity normalized trans-conductance is obtained in the deep week inversion, and start to decrease as the inversion coefficient increases due to the moderate and strong inversion regime, as shown in Figure 3.16.

Figure 3.16 presents the normalized transconductance over inversion coefficient of a 28 nm CMOS technology. In the meantime, Figure 3.17 represents the normalized transconductance of a 110 nm CMOS technology. Both technologies demonstrate that transistors at different temperatures present a selfsame $\frac{G_m n V_T}{I_d}$ at inversion coefficient (IC) lower than 1 (weak inversion regime). In the moderate and strong inversion regime, the figure shows how the velocity saturation effect is reduced as the temperature decreases. As a result, the normalized cryogenic trans-conductance does not go down as fast as the room temperature $\frac{g_m}{id}$.

I_{spec} represents the drain current to guarantee an inversion coefficient equal to 1.

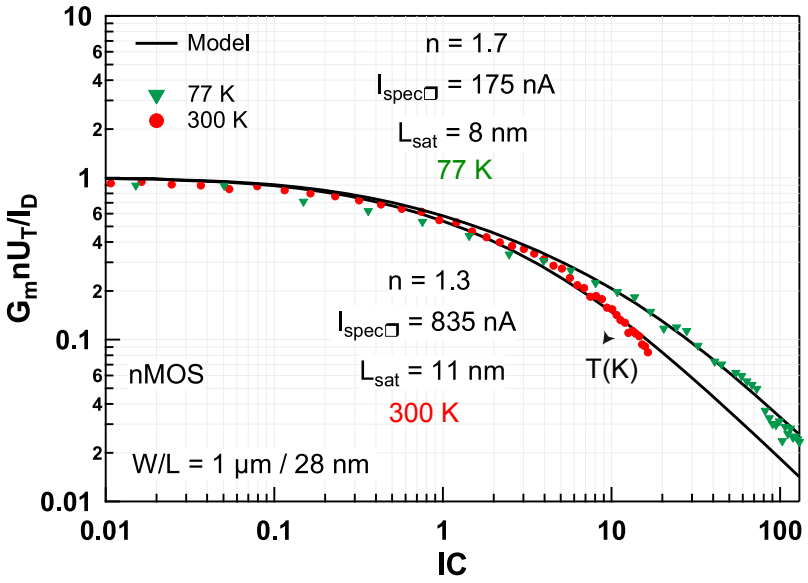

Figure 3.16: Normalized transconductance efficiency of a 28 nm technology over the inversion coefficient, figure taken from [54].

I_{spec} could be modified by changing the aspect ratio of the transistor, as described in the following equation, $I_{spec} = 2n\mu C_{ox}\frac{W}{L}V_T 2$.

3.3.7 Mismatch paramaters

The mismatch is considered as the spatial noise spread over the surface of the chip. The mismatch is modeled by the foundry's parameters to improve the VLSI design. The mismatch is composed of random and systematic contributions. In this case, the systematic term is regulated by the physical variation of device dimensions. The device dimension modifies the total contribution of the threshold voltage and carrier mobility fluctuation due to the process variation. In the meantime, the random mismatch is generated by line edge roughness (LER) and random dopant fluctuation (RDF) in the manufacturing process. Even though some of these are not truly random, they appear random to us as designers, because it's outside our control.

Mismatch scaling factors (A_{Vth} and A_β) exhibit a temperature variation. It increases as the temperature decreases from 300 K to 4.2 K. As a result, the drain-current mismatch increases around 1.2 for strong inversion operation at 4.2 K, assuming a constant $\frac{g_m}{I_D}$ [64]. However, the scaling factor increment due to temperature is almost negligible

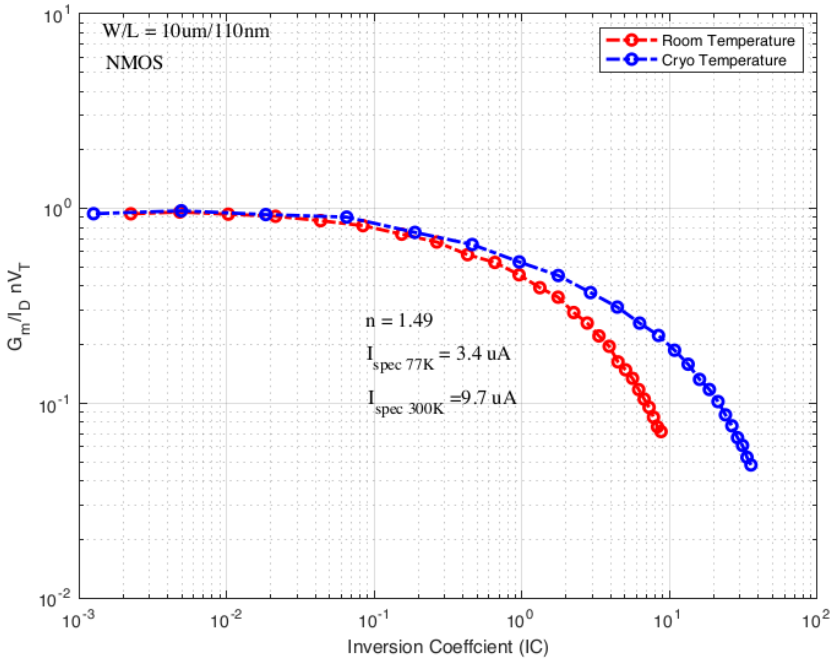

Figure 3.17: Normalized transconductance efficiency over the inversion coefficient, using a 110 nm technology.

in respect to the transistor area dependence, since the mismatch contributors (δV_T and $\delta\beta$) tend to decrease as the device area increases, as shown in Figure 3.18. Hence, transistor sizing must take care of mismatch behavior over the temperature in such a way as to obtain a negligible scaling factor variation. In this case, a circuit topology based on pMOS transistors may develop a reduced scaling factor variability.

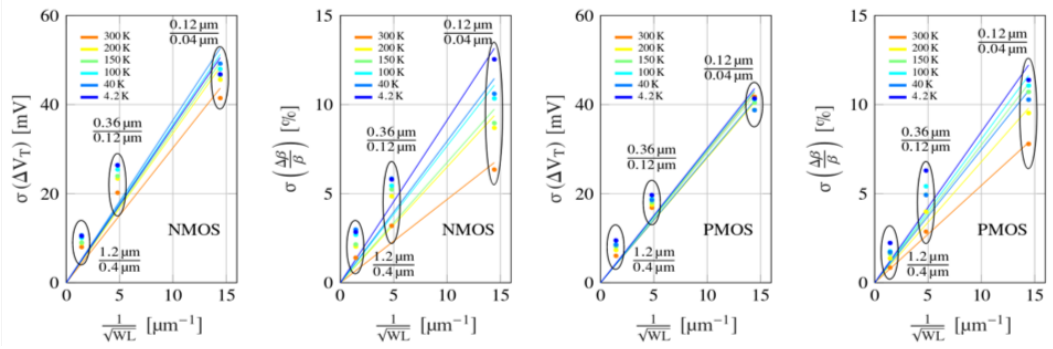

Figure 3.18: Mismatch parameters variation from 300 K to 77 K. Figure taken from [64].

3.3.8 CMOS electronics at 4.2 K

CMOS technology has been implemented to work at a temperature of 4.2 K (Liquid Helium) for important experiments, such as Quantum computing, spacecraft, and so on. At Helium temperature, many features of CMOS technology are enhanced in comparison to the parameters at a temperature of 77 K. However, some parameters do not follow the same improvement, such as the slope factor (n).

- **Carrier mobility and threshold voltage**

  Carrier mobility presents a continuous increment as the temperature decreases. Mobility growth is demonstrated by the trend shown in Figure 3.19. Mobility rise is, as was explained in section 3.3.2, due to the internal scattering variation. Results were extracted using a 28 nm CMOS technology from paper [3]. Threshold voltage owns critical performance at cryogenic temperatures. As it keeps on increasing as the temperature decreases. Thus, the 4.2 K threshold voltage growth becomes 20-40 mV higher than the voltage at 77 K [3].

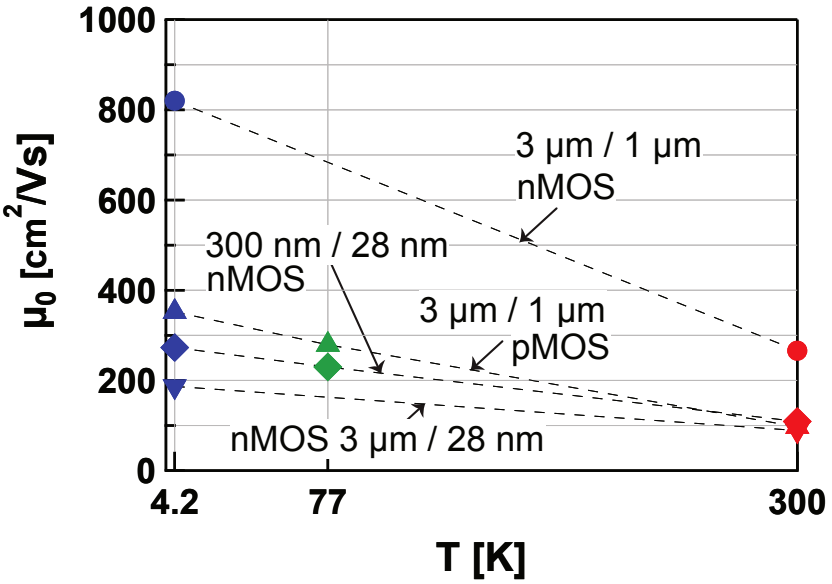

Figure 3.19: Low field mobility from 300 K to 4.2 K extracted from 28 nm CMOS technology [3].

- **Sub-threshold swing, slope factor and noise spectral density**

SS keeps on decreasing up to reach the 15 mV/dec, as shown in Figure 3.15. The SS is an optimal value to obtain a higher I_{on}, a smaller minimum power supply, and power dissipation. However, the slope factor increases around 15 times its value at room temperature. In this condition, the power consumption may not be as low as only assuming the V_T reduction, since the power reduction is now multiplied by this factor as shown the Equation 3.25.

$$PowerReductionfactor = \frac{T_{300K}}{T_{77K}} \frac{n_{77K}}{n_{300K}} f_{T300K} \tag{3.25}$$

RMS noise is a crucial factor in any electronic circuit, and in this case, the thermal noise decreases with the term kT. However, the 4.2 K flicker noise presents a considerable increase of two orders of magnitude in comparison to the 77 K flicker noise. Low-frequency growth happens at 10 and 100 Hz, as shown the Figure 3.4.

Chapter 4

Design of a cryogenic front-end electronics for large area SiPM (ASIC v1)

The cryogenic electronics (CE) presented in this chapter was designed to meet the requirements of the Darkside 20K experiment. This underground astroparticle experiment requires a photodetection module (PDM) working at 87 K. The operation temperature is determined by the scintillator element (Liquid Argon) employed inside the Time Projection Chamber (TPC) and the VETO system. TPC and VETO demand thousands of PDMs to achieve the necessary geometrical coverage. The Photodetection module is composed of a SiPM tile of 24 cm^2 with a total detector capacitance of 10 nF, and cryogenic front-end electronics. PDMs must fulfill the minimum requirements of the experiment and simultaneously maintain good reliability for more than 20 years.

The ASIC v1 must fulfill crucial specifications to be accepted as front-end electronics in the VETO structure. The key parameters are the following:

- **Signal to noise ratio (SNR)** is defined as the ratio between the single PE amplitude, and the RMS noise. The SNR must be higher than 8 to guarantee the noise signal is not misunderstand to the output signal.
- **Dynamic range** is a crucial parameter for VETO system, since the ASIC v1 must provide a readout of 230 PEs linearly.
- **Rising time** is defined as the time required to change from 10% to 90% of its amplitude. In the VETO system is important to guarantee at least 150 ns as the rising time. It would avoid the pile-up effect in the PE output signal.

4.1 Photo-detection system

The Photodetection system of the Darkside 20K experiment is built by thousands of silicon photo-multiplier (SiPM) tiles. The SiPM is a pixelated device made of hundreds or thousands of micro-cells organized in a matrix. Each micro-cell is composed by a single-photon avalanche diode (SPAD) and a passive-quenching resistor (R_q). The SPADs, which operate in Geiger mode, produce between 10^5 and 10^7 avalanche charge carriers per each detected photo-electron (PE). The micro-cells are interconnected in parallel through their anode and resistor, as is illustrated in Figure 4.1(left). The SiPM electrical model is formed by a quenching resistor, a junction capacitor, and a charge gain represented by a current source, as shown in Figure 4.1 (right).

Micro-cell dimensions range from 10 µm to 100 µm with a spectral sensitivities from ultraviolet to infrared, and a peak on the visible wavelength (400 nm – 500 nm). The photo detection efficiency (PDE) achieves peak values higher than 40-50% [65]. The SiPM technology of DarkSide 20k exhibits a maximum PDE at 420 nm approaching 60 % [66].

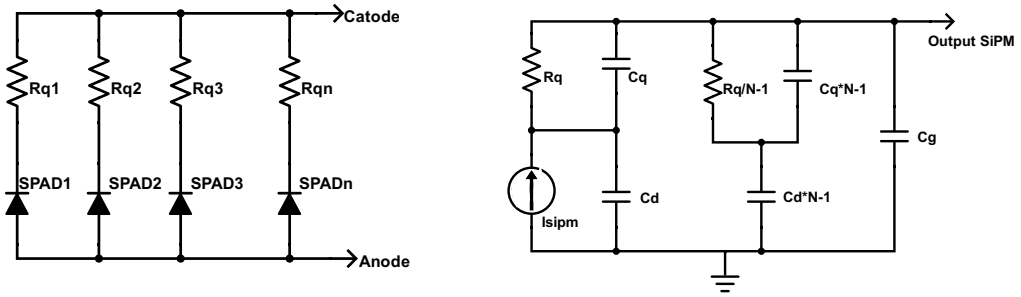

Figure 4.1: Structure of SiPM microcells (left) and SiPM electrical model (right)

SiPM requires a bias voltage higher than the breakdown voltage to generate the internal avalanche. Basically, the target SiPM operation is achieved with an overvoltage between 3 V and 7 V. The overvoltage range allows the PDE and the SiPM gain to be controlled and varied, as it is shown the Figure 4.2 and Figure 4.3 respectively. SiPM prototype was developed by the Fondazione Bruno Kessler (FBK). FBK has designed and produced the sensor focusing on an optimal performance at 87 K.

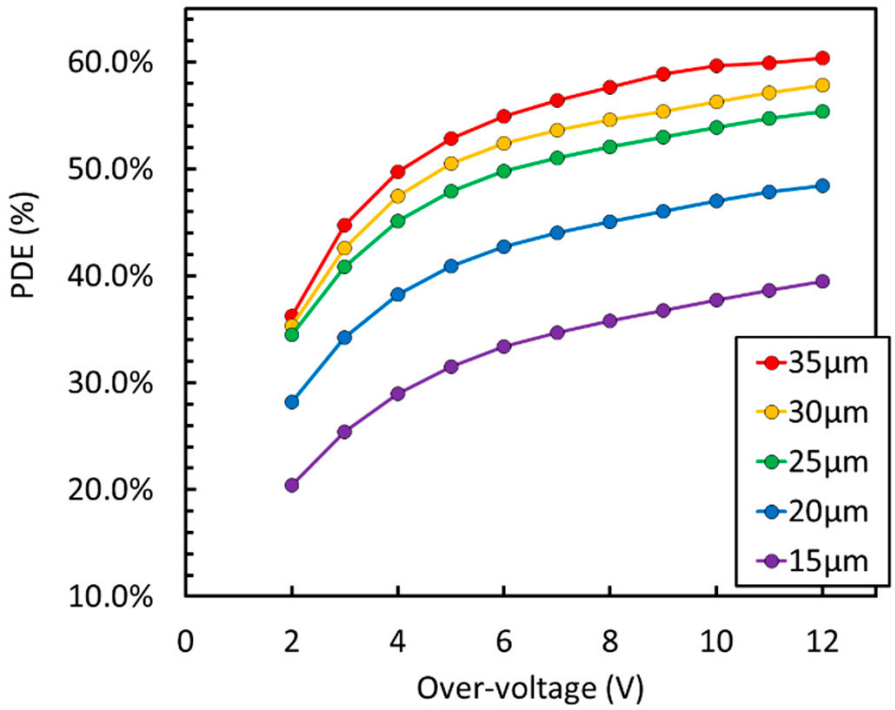

Figure 4.2: Photo detection efficiency for visible light at different overvoltages. Each curve corresponds to a particular size of the SiPM micro-cell. Figure taken from [66]

SiPM operation depends on several internal parameters, such as the gain, quenching resistor, the PDE, afterpulsing probability, and dark count rate. These elements provide a criterion for sensor efficiency. In the Darkside framework, SiPMs run with a NUV-HD silicon photo-multiplier technology with the following features:

- **SiPM Gain & Quenching Resistance**
  SiPM gain sensor is defined as the number of electrons generated by a single photo-electron (PE). SiPM gain strongly depends on the overvoltage and micro-cell dimension, as it is illustrated in Figure 4.3.

  On the other hand, a quenching resistor (R_q) is a necessary element to quench the avalanche in the SPAD. Besides, the value of R_q and the junction capacitance determine the recovery time of the SPAD. This is the time required by the SPAD to be able to acquire a new photon after a previous detection. R_q is made of silicon, therefore the resistance presents a considerable variation on temperature. In this case, the R_q rises by about 5 times between 300 to 77 K [66].

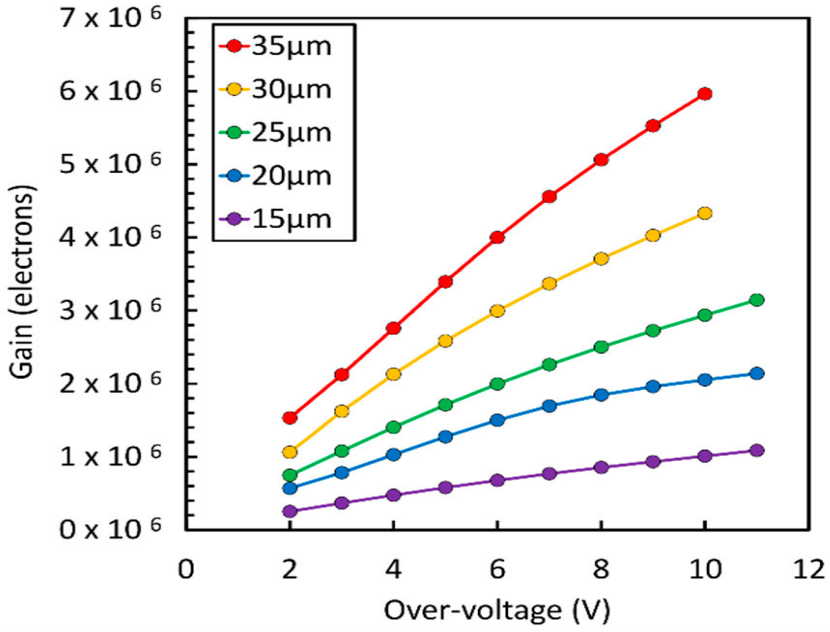

Figure 4.3: SiPM gain vs overvoltage at different micro-cell sizes. Figure taken from [**1**].

- **Afterpulsing & Direct Crosstalk probability**

  Afterpulsing (AP) and direct crosstalk (DiCT) are two undesirsable effects associated to the SiPM operation. The AP and DiCT probability strongly depend on the current density of the avalanche. Hence, the higher the SiPM gain, the higher the current through the diodes, causing an increase of the AP and DiCT probability. The Afterpulsing phenomenon is generated by the carriers trapped in silicon defects during the avalanche charge multiplication. These charges are later released during the SPAD recharging phase. The AP probability presents a considerable increment at 87 K in comparison to the value at 300 K, as it is illustrated in Figure 4.4.

  On the other hand, direct cross-talk is generated during the SiPM operation due to the emitted photons in the avalanche multiplication. These photons may be re-absorbed in neighboring cells or the inactive regions of the same cell originating additional current pulses in the SiPM. The DiCT probability increases as the temperature decreases, as is illustrated by Figure 4.5.

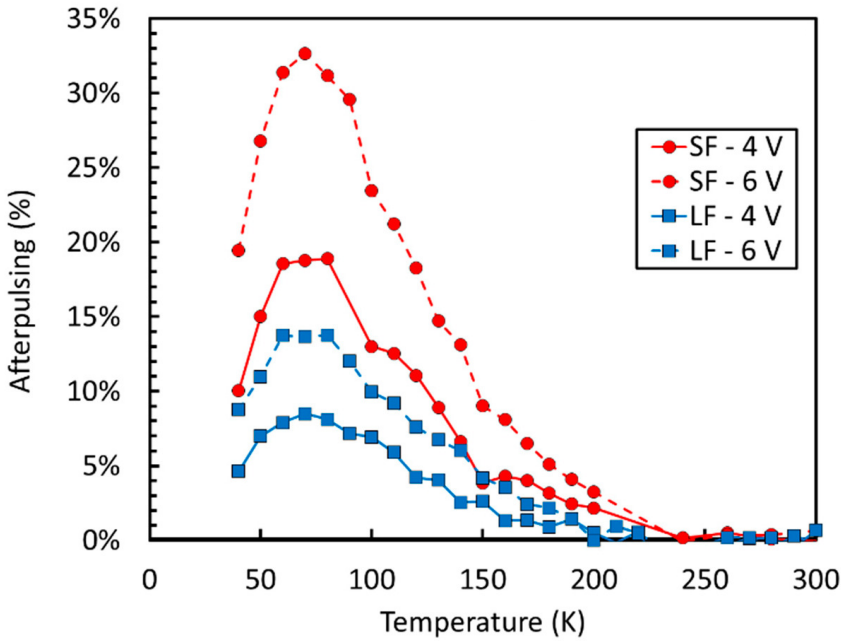

Figure 4.4: Afterpulsing probability vs temperature using a 25 um micro-cell. Figure taken from [66].

- **Dark count rate**

  The dark count is among the most significant noise contributors within the SiPM operation. It is a spurious current pulse produced, even in absence of light, by thermal agitation. Due to thermal energy, a free electron or a hole is generated inside the active region and can trigger an avalanche, and hence an output pulse. The dark count rate refers to the number of such pulses generated in one second. Due to its thermal origin, the dark count rate strongly depends on temperature, as is shown in Figure 4.6.

Front-end integrated electronics was designed for the readout of large-area sensors. In this study, the target SiPM sensor is a tile of 24 cm^2 described in Figure 4.7. NUV-HD-Cryo SiPM [66] was developed by FBK with a quenching resistance of 5 MΩ at 87 K. The sensor has a gain of 2.2×10^6, a junction capacitance of 78 $\frac{pF}{mm^2}$ and a PDE > 50% at 420 nm. The gain and PDE parameters were obtained by applying an overvoltage equal to 5 V.

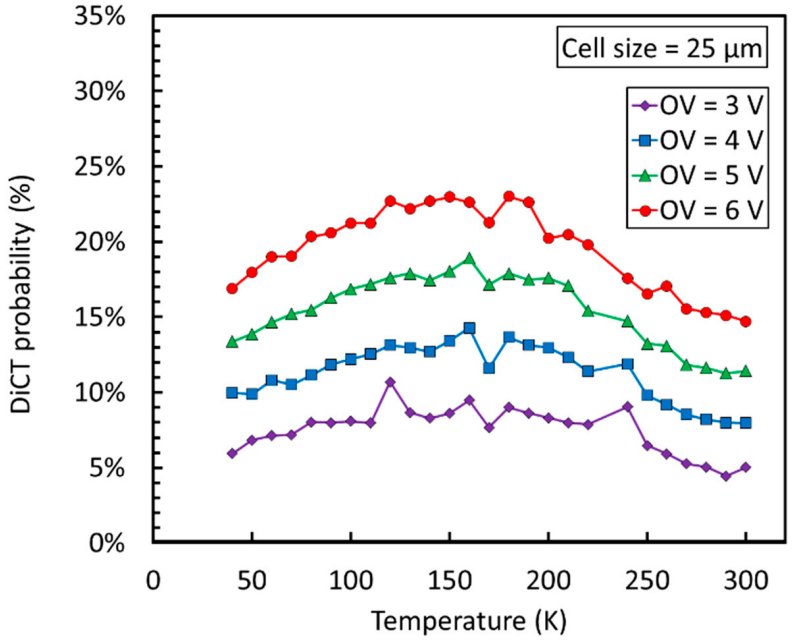

Figure 4.5: Direct crosstalk probability vs temperature. Figure taken from [66].

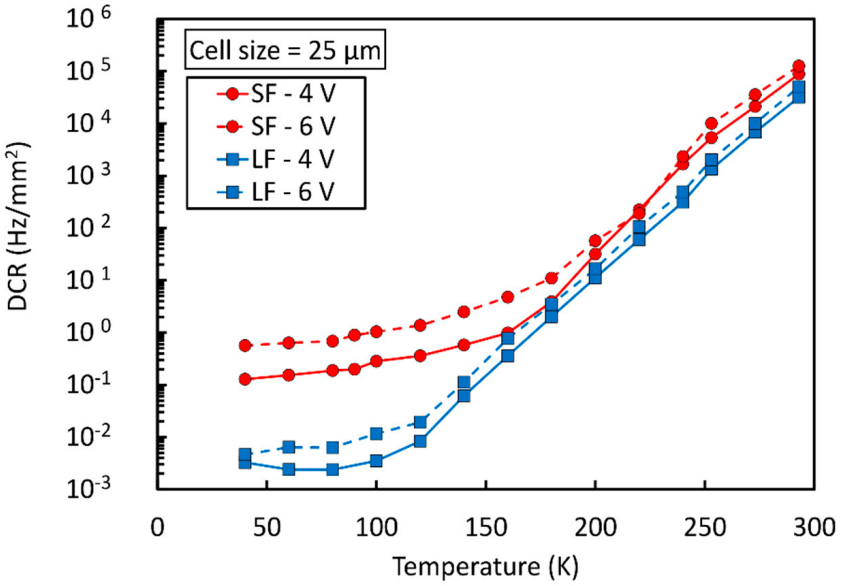

Figure 4.6: Dark count rate vs temperature .Figure taken from [66].

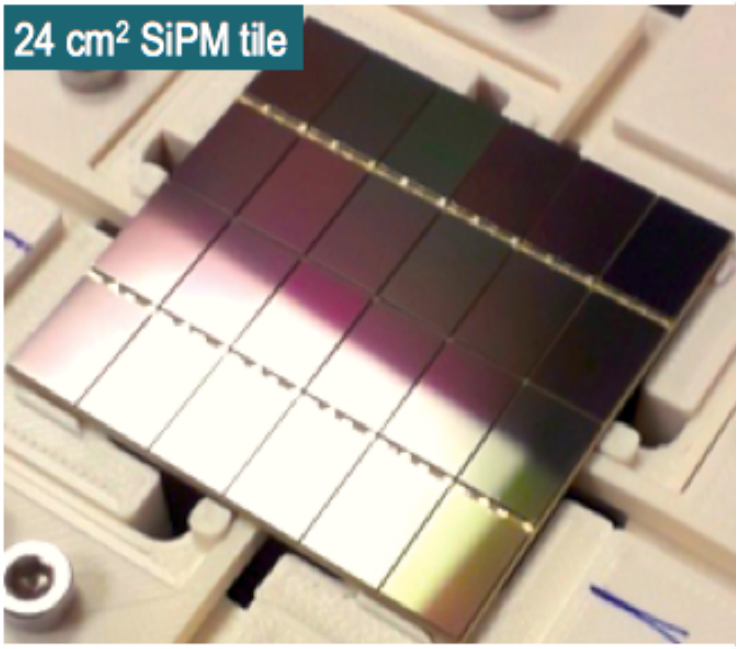

Figure 4.7: 24 cm^2 array of Silicon Photomultipliers. Figure taken from [67].

A SiPM tile of 24 cm^2 is organized in 4-quadrants of 6 cm^2. Each quadrant is set-up by 2-series 3-parallel blocks of 1 cm^2 SiPMs, as shown the schematic of Figure 4.8. This SiPM configuration has been designed to decrease the total detector capacitance, which is estimated to be 7.8 $\frac{nF}{cm^2}$. Then, the total 6 cm^2 quadrant approximately owns 11.7 nF of capacitance. Besides, each SiPM branch (2-series of 1 cm^2 SiPM) employs two large resistors in parallel to guarantee a homogeneous voltage drop across the two SiPM connected in series.

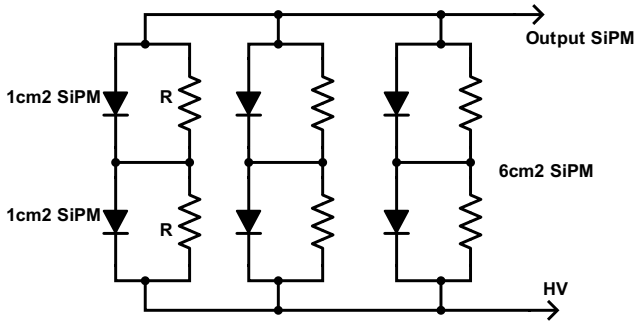

Figure 4.8: 6 cm^2 2-series 3-parallel configuration

4.2 CMOS Front-end integrated electronics

The Front-End (FE) electronics is the first element in the electronic readout chain. The FE block processes the electrical signal (current or voltage) from the sensor, and releases a desired output voltage signal. The output signal must comply with the minimum requirements in terms of amplitude, noise, slew rate, and peaking time. In this study, the Darkside 20K experiment establishes the minimum requirements.

The implemented architecture scheme for the cryogenic front-end is based on the 4-quadrants sensor organization. Then, each input stage is designed to readout a single quadrant of 6 cm^2. The second stage receives the signals from the input stages, summing them up into a single-ended output. The resulting waveform thus represents the readout of a 24 cm^2 sensitive area. Figure 4.9 illustrates the full front-end electronics schematic. Here, each SiPM quadrant connects to a low-noise trans-impedance amplifier (TIA). Next, 4-TIAs output signals feed a voltage summing amplifier.

The trans-impedance amplifier architecture consists of a high-gain voltage amplifier with a resistor connected in feedback. Depending on the application, many different alternatives can be used for the implementation of the core voltage amplifier. For instance, simpler topologies, such as class AB or class D amplifier [68] are employed in high-frequency applications, because a low number of transistors reduces the total parasitic capacitance, thus increasing the available bandwidth.

On the other hand, the Folded cascode, Telescopic cascode, and regulated cascode architectures, that require more transistors, are preferred when a very large DC gain in the core amplifier is mandatory. These architectures include in fact additional stages to enhance the DC gain. Each architecture presents specific figures of merits, such as the bandwidth, dynamic range, DC gain, or common-mode range.

In this study, the four TIAs and the summing amplifier implements a folded cascode (FC) operational trans-impedance amplifier (OTA). This architecture has been chosen as the baseline architecture of FE due to its robustness, large DC gain, and wide common-mode input range (CMIR). Moreover, folded cascode provides a better dynamic range in comparison to a telescopic amplifier [69], a regulated gate cascode [70] or a wide-swing current mirrors architecture.The folded cascode demands a higher power consumption, but this is not a very critical requirement for the experiment, considering also the relatively small channel density. A power consumption of 200 mW/tile can in fact be afforded.

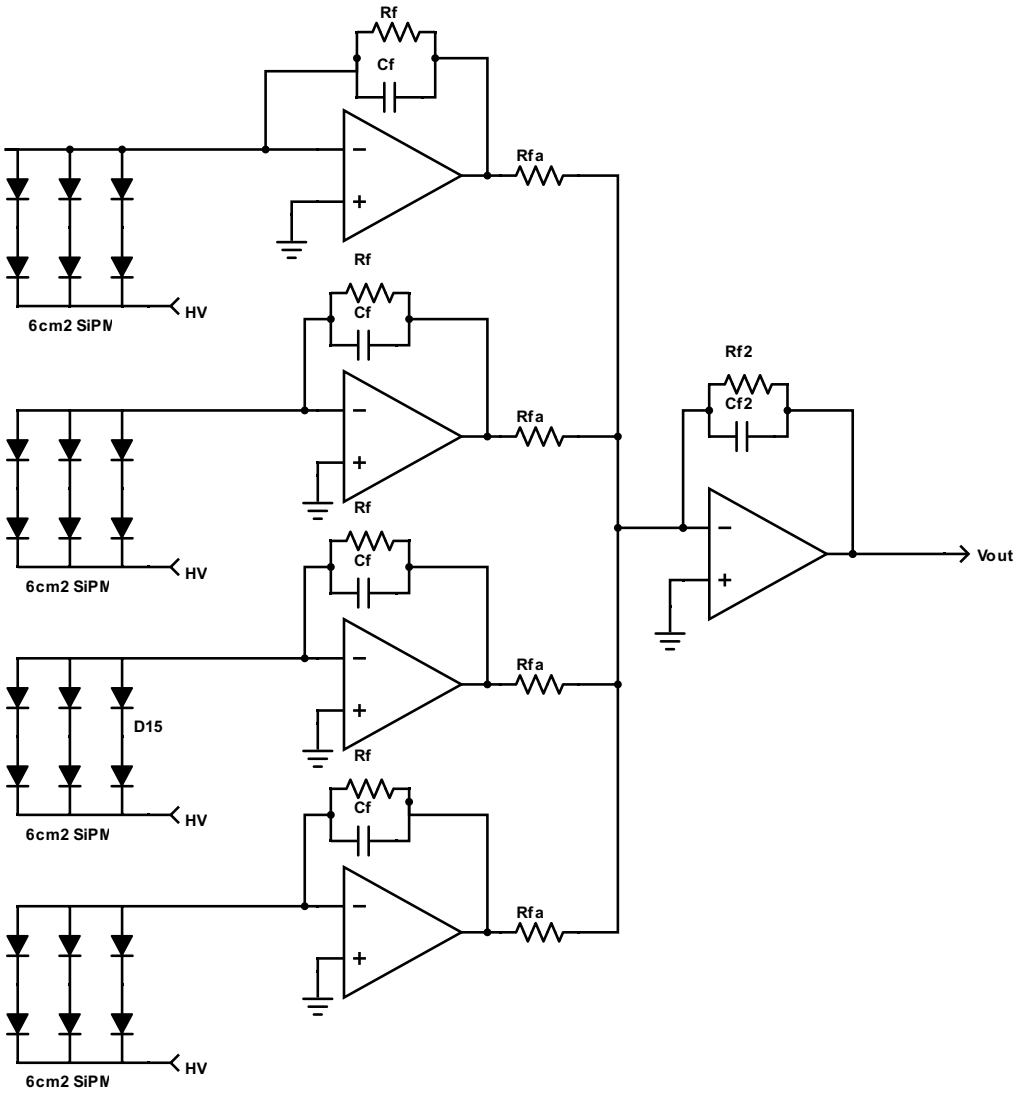

Figure 4.9: Full front-end to readout the 24 cm^2 SiPM tile.

4.3 Transistor-level design of operation amplifier circuits

The transistor-level design schematic of FC OTA is illustrated by Figure 4.10. The architecture adopts a pMOS input topology due to its low flicker noise [58]. Furthermore, pMOS transistors develop a much better performance than their nMOS counterparts in

term of hot carrier and threshold voltage variation at a cryogenic temperature in the range 87 K - 4.2 K [9]. The pMOS input stage is connected to an nMOS cascode stage to form the folded cascode. Besides, the FC amplifier includes a class AB output driver to guarantee a symmetrical slew rate, even processing a large input signal (>250 PEs). The last feature, a source degeneration technique, represented by the resistance (Rs) in Figure 4.10, is implemented in the FC structure. The degeneration resistor is a simple way to linearize the transfer characteristic of the MOS device, guaranteeing better linearity in the circuit, fundamental for a linear readout of the large number of photo-electrons, as VETO structure requires.

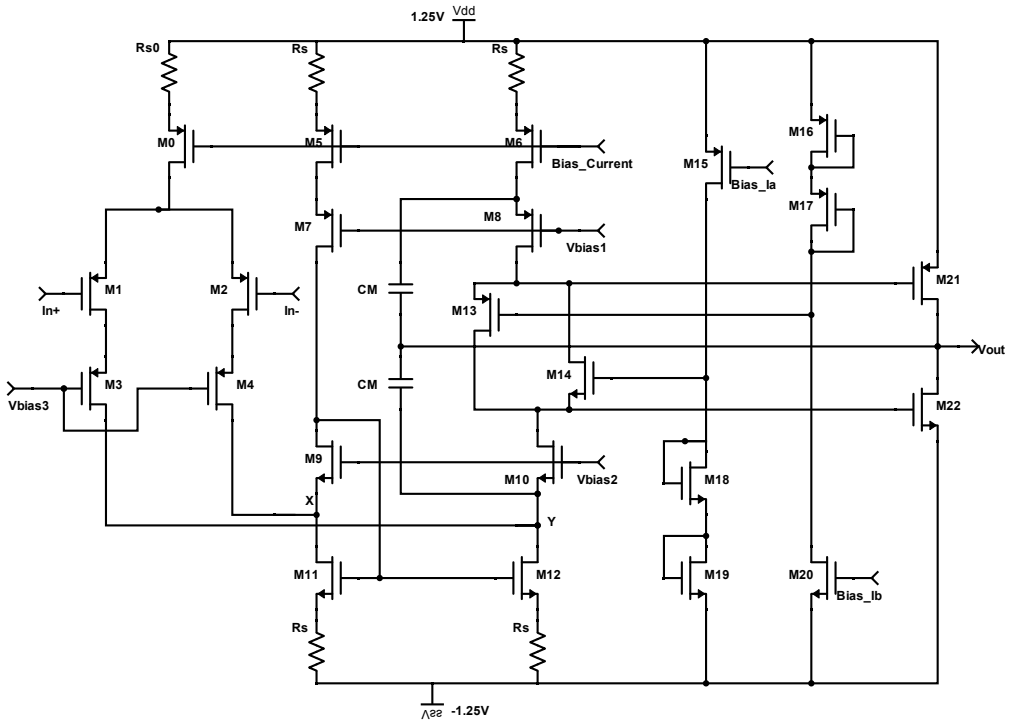

Figure 4.10: Transistor-level circuit of the folded cascode OTA.

The cryogenic environment imposes additional constraints in comparison to room temperature electronics. In particular, cold electronics requires careful design strategies to reduce the device degradation caused by hot carrier effects. The transistor reliability becomes an even more critical issue due to the limited access to cryogenic environments for repairs or changes in the electronics. As a result, a specific transistor sizing

may reduce the hot carrier probability. In this case, transistor sizing has followed two conditions to extend the lifetime of the transistor for more than 20 years. These applied design techniques are based on the results discussed in Chapter 3.2.1.

Firstly, all transistors are sized using a channel length larger than the minimum one allowed by the technology. This is a common practice also for room temperature analog circuit design to avoid excessive flicker noise and degraded output conductance. Additionally, care has been taken to bias all transistors in order to reduce as much as possible the drain-source voltage, thus lowering the electric field across the devices and consequently the hot carrier probability.

An extra critical point of cold electronic design is the reliability of the device models provided by the PDK. The 110 nm technology PDK available for this work is intended for the military temperature range (213 to 423 K) and does not contains models extracted at 87 K. However, the cryogenic electronics design was developed, taking into account the parameter extraction results described in Chapter 3.3. The extraction illustrates the temperature variation of the most critical factors, such as the low field mobility and the threshold voltage.

In this design, low field mobility variations are compensated by adjusting the current biasing. Low field mobility variation considerably affects the transconductance value of each transistor, and hence the overall circuit noise and bandwidth. The bias current is regulated by an external circuit on the PCB. When the temperature is decreased from 300 K to 77 K the bias current is lowered as well to compensate for the mobility increment. This adjustment produces two crucial effects. First, it makes the transconductance of the transistors return to the simulated room temperature value. Second, the current compensation strongly contributes to a reduction in power consumption, because the bias current is halved at a temperature of 77 K. The current reduction is realized by the external port **Bias current** shown in Figure 4.10.

Transistor level circuit was designed by optimizing the following parameters: DC gain, gain bandwidth (GBW), input mismatch (offset voltage), dynamic range, and hot carrier probability. The input transistors are driven in weak inversion to guarantee an identical $\frac{nV_TG_m}{I_d}$ to the room temperature operation, because an identical $\frac{nV_TG_m}{I_d}$ makes easier the current compensation between 300 K and 77 K. Furthermore, a weak inversion regime allows the FE electronics to be designed with a higher DC gain than the moderate or strong inversion regime considering the same power consumption [71].

The second aspect of circuit design becomes the gain bandwidth parameter. The folded cascode amplifier targets a GBW higher than 5 GHz. Next, the minimum aspect

ratio of input transistors, considering the target GBW, was computed by using Equation 6.1. The chosen aspect ratio ($\frac{W}{L}$) was much larger than that obtained in the equation in order to compensate for the capacitive noise. The capacitive noise is generated from the mismatch between sensor capacitance (10 nF) and input transistor capacitance, C_{GS} = kWL. The capacitive noise is described by Equation 4.2.

$$\left(\frac{W}{L}\right)_{1,2} \geq \frac{C_o \times GBW}{2\beta_p \Phi_t e^{\frac{V_{gs}-V_{\mathrm{TH}}}{n\times\Phi_t}}} \tag{4.1}$$

with:

- $\beta_p = \frac{\mu_p C_{ox}}{2}$, μ_p carrier mobility of PMOS and C_{ox}, Silicon oxide capacitance;
- Φ_t, Thermal voltage, 26 mV at 300 K and 6.7 mV at 77 K;
- C_o, Capacitance on the output node;
- n, Slope factor $\frac{C_{ox}-C_{dep}}{C_{ox}}$, C_{dep}, Depletion capacitance;
- Gate source voltage, V_{gs} and Threshold voltage, V_{th};

The drain current of the input transistor is determined by assuming the weak inversion operation and fulfilling the GBW requirement. In this case, the bias current is computed by the Equation 4.3. The transistor dimension are summarized in Table 3 of Appendix I.

$$dV_{Ieq}^2 = \frac{(C_{sensor} + k \times W \times L)^2}{C_{sensor}^2} \frac{1}{2\beta_p (V_{gs} - V_{th}) \frac{W}{L}} \frac{8KT}{3} \tag{4.2}$$

$$I_{M_{1,2}} = 2n\beta_p \left(\frac{W}{L}\right)_{1,2} \Phi_t^2 e^{\frac{V_{gs}-V_{\mathrm{TH}}}{n\times\Phi_t}} \Bigg\} \quad \text{Weak Inversion Current} \tag{4.3}$$

with:

- Capacitive noise, dV_{Ieq};
- C_{sensor}, Detector capacitance;
- $k = \frac{2}{3} C_{ox}$, process variable for saturated device
- K, Boltzmann constant and T, Temperature in Kelvins;

Transistors M_3 and M_4 are driven in strong inversion. The series transistors function is to reduce the drain-source voltage (V_{ds}) over transistors (M_1 and M_2), and then the high kinetic energy from the electrons either. The V_{ds} reduction enhances the transistor lifetime by dropping their stress, as was described in Chapter 3.2.1.

$$\left(\frac{W}{L}\right)_{M_{3,4}} \geq \frac{I_{\mathrm{d}M1,M2}}{\beta_p V_{\mathrm{od}\,M_{3,4}}^2} \tag{4.4}$$

with:

- Drain current, $I_{\mathrm{d}(M1,M2)} = 800\ \mu\mathrm{A}$;
- Over-drive voltage, $V_{\mathrm{od}\,M_{3,4}} \geq 150\ \mathrm{mV}$;

Considering the mismatch contribution equation from [72], [73], and that described by Equation 4.5, the offset voltage is computed. Depending the operation region of transistor, the variance of the gate source voltage can be described by Equation 4.6 (weak inversion) or Equation 4.7 (strong inversion).

$$\Delta V_{gs} = \Delta V_{\mathrm{TH}} - \left(\frac{I_d}{g_m}\right)\left(\frac{\Delta\beta}{\beta}\right)\Bigg\} \quad \text{Mismatch Contribution} \tag{4.5}$$

$$\sigma^2(\Delta V_{gs}) = \sigma^2(\Delta V_{\mathrm{TH}}) + (nV_T)^2\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \tag{4.6}$$

$$\sigma^2(\Delta V_{gs}) = \sigma^2(\Delta V_{\mathrm{TH}}) - \frac{(V_{gs} - V_{TH})^2}{4}\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \tag{4.7}$$

Assuming the variance of gate-source voltage due to the carrier mobility is almost zero, $\sigma(\Delta\beta) \approx 0$, because of its almost negligible contribution on the transistor mismatch. Remaining the mismatch contribution from threshold voltage. Then, the variance of the gate-source voltage difference for both weak and strong inversion is expressed by Equation 4.8.

$$\sigma^2\left(\Delta V_{\mathrm{gs}}\right) = \sigma^2(V_{\mathrm{off}}) \approx \sigma^2\left(\Delta V_{\mathrm{TH}}\right) \tag{4.8}$$

Electronics design has assumed a maximum input offset due to the voltage threshold mismatch of $V_{\mathrm{off},max} < 0.5\ \mathrm{mV}$, since it will be produced in more than 10.000 ICs. Then, the ($V_{\mathrm{off},max}$ guarantees a maximum variation of the output baseline equal to 1.5 mV,

considering a 3σ, and 3 mV for 2x 3σ remaining smaller than the amplitude of 1 PE (4.5 mV for 5 VoV).

The mismatch equation is applied to each transistor of the input branch. In other words, it is included each transistor where the DC input current flows through. Resolving the mismatch equation for each transistor, the offset voltage is represented by Equation 4.9. In this case, the offset equation just considers the transistors $M_{1,2}$, M_{1-6} and $M_{11,12}$ of Figure 4.10.

$$\left.\begin{aligned}\sigma^2(V_{\text{off}}) = \sigma^2(\Delta V_{\text{TH}M_{1,2}}) + \sigma^2(\Delta V_{\text{TH}M_{3,4}}) + \sigma^2(\Delta V_{\text{TH}M_{5,6}}) \\ + \left(\frac{\mu_n}{\mu_p}\right)\sigma^2(\Delta V_{\text{TH}M_{11,12}})\end{aligned}\right\} \quad \text{Offset voltage} \qquad (4.9)$$

Where, $\sigma^2(V_{\text{off}}) = \frac{V_{\text{off},max}}{3}$ and $\sigma^2(\Delta V_{\text{TH}}) = \frac{A_{\text{TH}}^2}{W \times L}$ for both strong and weak inversion operation. A_{TH} is a foundry mismatch parameter. Transistor length condition must be fulfilled to guarantee the largest mismatch contribution are handled by input transistors M_1, M_2, M_3, and M_4, then:

$$\sigma^2(\Delta V_{\text{TH}M_{1,2}}) = \sigma^2(\Delta V_{\text{TH}M_{3,4}}) \qquad (4.10)$$

$$\sigma^2(\Delta V_{\text{TH}M_{1,2}}) > \sigma^2(\Delta V_{\text{TH}M_{5,6}}) \qquad (4.11)$$

$$\sigma^2(\Delta V_{\text{TH}M_{1,2}}) > \left(\frac{\mu_n}{\mu_p}\right)\sigma^2(\Delta V_{\text{TH}M_{11,12}}) \qquad (4.12)$$

Mismatch contributions due to the threshold voltage, $\sigma^2(\Delta V_{\text{TH}}) = \frac{A_{\text{TH}}^2}{W \times L}$, are replacing into Equation 4.10, 4.11 and 4.12, to obtain the optimal channel length for the desired offset voltage. The channel length conditions relate the transistors M_{3-6}, M_{11} and M_{12}, as described the following statements: $L_{3,4} = L_{1,2}$, $L_{5,6} > L_{1,2}$ and $L_{11,12} > \sqrt{\frac{\mu_n}{\mu_p}} \times \frac{A_{\text{TH}n}}{A_{\text{TH}p}} L_{1,2}$.

Previous conditions imply that offset voltage exclusively depends on input transistors mismatch. Thus, the input transistor contribution should be lower than the maximum offset voltage. Assuming a $\sigma^2(V_{\text{off}}) > \sigma^2(\Delta V_{\text{TH}(M_{1,2})}) + \sigma^2(\Delta V_{\text{TH}(M_{3,4})})$ and $\sigma(V_{\text{off}},$

the channel length and width of input transistors are determined by the Equation. 4.13, 4.14.

$$W_{1,2}L_{1,2} > 2\frac{9A_{\mathrm{TH},p}^2}{V_{\mathrm{off},max}^2} \longrightarrow W_{1,2} > \sqrt{2\frac{9A_{\mathrm{TH},p}^2}{V_{\mathrm{off},max}^2}\left(\frac{W}{L}\right)_{1,2}} \tag{4.13}$$

$$L_{1,2} > 2\frac{9A_{\mathrm{TH},p}^2}{W_{1,2}V_{\mathrm{off}\,max}^2} \tag{4.14}$$

Aspect ratio of transistors M_5, M_6, M_{11} and M_{12} are calculated by following Equation 4.15. The W/L results were determined by considering an overdrive voltage $V_{\mathrm{od}} < 100$ mV at 77 K.

$$\left(\frac{W}{L}\right) \geq \frac{I_d}{\beta V_{\mathrm{od}}^2} \tag{4.15}$$

with:

- transistors M_5, M_6, M_7 and M_8, $I_d = 400$ µA and β_p ;
- transistors M_9 and M_{10}, $I_d = 400$ µA and β_n;
- transistors M_{11} and M_{12}, $I_d = 1.2$ mA and β_n;

The third important aspect of the circuit design was to master properly the hot carrier effect. Then, we adopt specific channel length sizing for each transistor in the circuit. First, the channel length of nMOS transistors (M_9, M_{10}) were sized equal to L = 2 µm. This value is an optimal length to reduce hot carrier probability. pMOS version presents a softer hot carrier effect than the nMOS version. Hence, the pMOS channel length might be quite smaller than the nMOS counterpart.

The last aspect of the transistor-level design was stability. The stability is a critical aspect of electronic systems. Indeed, a strong compensation network was introduced to guarantee, at least, a phase margin greater than 60°. To provide the required phase margin, a Miller compensation network was implemented to control the second pole frequency. With reference to Figure 4.10, this pole is determined by the parasitic capacitance of node X and Y. The Miller compensation schematic is depicted in Figure 4.11b. Miller capacitors (C_M) together with the trans-conductance of M_{21} and M_{22} ($g_{m21,22}$) realize the second compensating pole. Miller compensation provides a pole shifting that

is illustrated in Figure 4.11a. In this case, a large Miller capacitance creates a large separation between the first and second pole generating, firstly, a slope of 20 dB/dec which is maintained up to 0 dB frequency and, secondly, an increase in the phase margin.

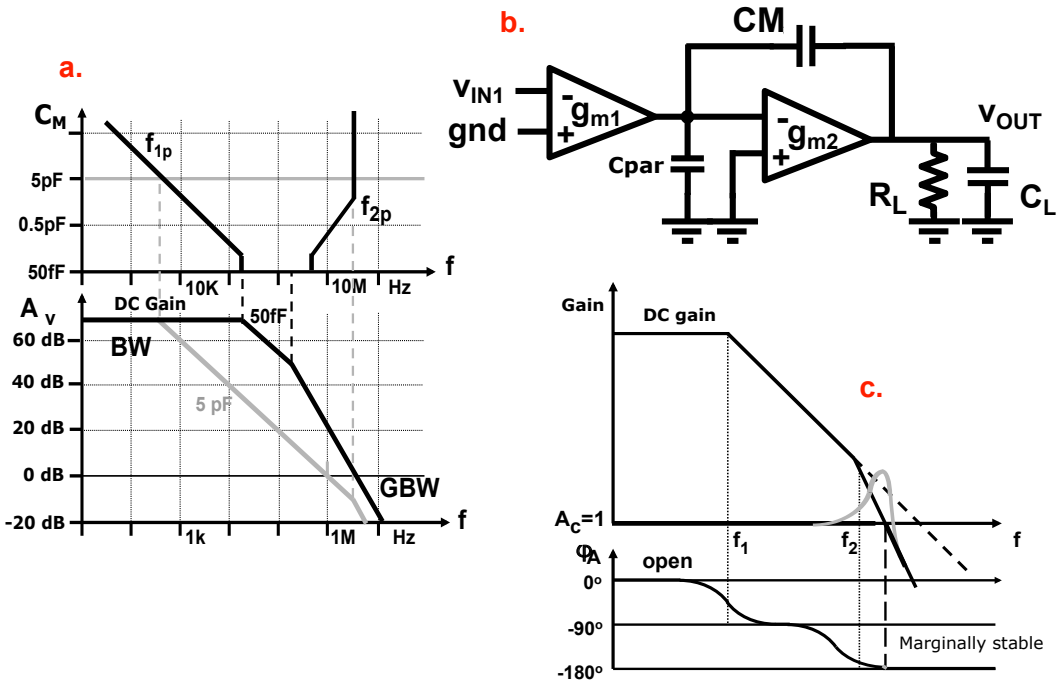

Figure 4.11: Frequency compensation schematic.

A safe phase margin was computed with the following criterion: $\frac{f_{p2}}{GBW} \geq K_{pm} = 3$. This condition guarantees a phase margin larger than 60°. Replacing the second frequency pole, $f_{p2} = \frac{g_{m21}}{2\pi C_M}$, into the previous condition, the aspect ratio equation for M_{21} and M_{22} is achieved, and described by the Equation 4.16 and 4.17.

$$\left(\frac{W}{L}\right)_{21} \geq \frac{(C_M \times GBW \times K_{pm})^2}{4\beta_n I_d} \tag{4.16}$$

$$\left(\frac{W}{L}\right)_{22} \geq \frac{(C_M \times GBW \times K_{pm})^2}{4\beta_p I_d} \tag{4.17}$$

Afterward, the output swing (OS) determines the dynamic range of front-end electronics, i.e. the total number of photo-electrons that can be processed without saturating the output signal. The output swing is given by the Equation 4.18, where Vdd and Vss represent the positive and negative DC supply voltage.

$$OS \leq Vdd + Vss - \sqrt{\frac{I_{dM21}}{\beta_p(\frac{W}{L})_{21}}} - \sqrt{\frac{I_{dM22}}{\beta_n(\frac{W}{L})_{22}}} \tag{4.18}$$

With a gain-bandwidth in the core amplifier larger than 5 GHz, the effective bandwidth of TIA only depends on the feedback components, as shown in Figure 4.12. The values of R_f and C_f are computed to achieve a desired rise time. The rise time value presents a trade-off between noise and pile-up. The longer the rise time, the smaller is the series noise contribution, which is dominant due to the large sensor capacitance. However, the pile-up probability increases, determining a distortion in the output pulse.

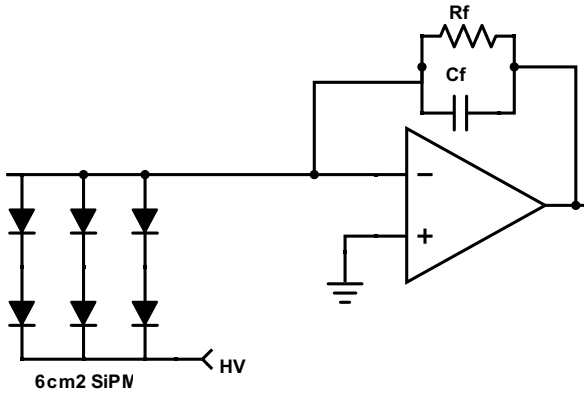

Figure 4.12: Trans-impedance amplifier schematic.

In this ASIC version, I have selected the parameter design in such a way as to achieve a rise time equal to 150 ns. This result guarantees two key requirements of the experiment ($SNR > 8$ and $T_{rise} \leq 150$ ns).

The Transfer function H(s) of the TIA is represented by Equation 4.19. From this equation, the open-loop gain is assumed much higher than 1 and $C_d \gg C_f$. As a result, the bandwidth of the TIA is described by Equation 4.20. In order to achieve a rise time of around 140-150 ns, the target BW must be around 2.5 MHz. Then, feedback resistor

R_f, for a sensor capacitance $C_d = 10nF$, was computed with Equation. (4.20). As a result, the feedback resistor is equal to 90 kΩ.

$$H(s) = \frac{-R_f}{s^2 + s\frac{W_o}{Q} + W_o^2} \tag{4.19}$$

$$W_o = \sqrt{\frac{GBW}{R_f C_d}} \tag{4.20}$$

The summing amplifier stage integrates an identical transistor-level structure of the TIA stage and optimization circuit design. However, the summing stage does not implement large area input transistors, as the TIA structure, because the summing amplifier shall not compensate for the capacitive noise due to the detector capacitance, but it should match with the TIA's output capacitance, much lower than the detector value. The transistor-level design of the summing amplifier is represented in the Table 4 of Appendix II.

Front-end electronics post-layout simulations were carried-out using state-of-the art CAD tools. The SPICE netlist, with the parasitic components, represents the whole layouts structure, shown in Figure 4.13. This figure reports also an additional layout structure to the right which is not related to the work of this thesis. A realistic SiPM electrical model was also implementedfor post-layout simulations. The SiPM parameters of the electrical model were extracted from the target sensor of the experiment in collaboration with FBK [39],[66].

4.4 CMOS electronics post-layout simulations

As explained above, the front-end integrated electronics must fulfill the minimum requirement of the experiment in terms of timing jitter, SNR, and dynamic range. Table 4.1 illustrates the minimum requirements of VETO structure in DarkSide-20K experiment and the simulated results of the relevant figure of merits at both 300 K and 77 K. Simulation results were obtained by reproducing the charge of 1 PE at 5 V of overvoltage. An overvoltage of 5 V will be the minimum bias voltage to operate the SiPM in DarkSide-20K since it guarantees a photodetection efficiency (PDE) higher than 50 % Figure 4.2. From the results, it is evident the RMS noise reduction at 77 K. In this case, the improved noise is highly related to thermal noise reduction. Meanwhile, the variation in the PE amplitude is due to the temperature variation of the quenching resistance,

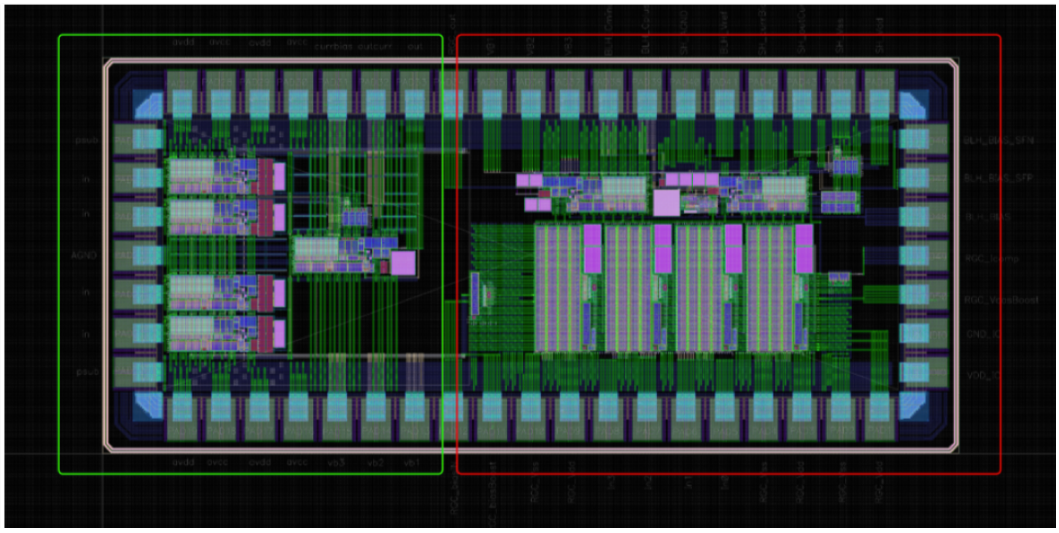

Figure 4.13: Layout structure of the ASIC V1 (green)

that changes from 1.5 MΩ to 5.5-6 MΩ as the temperature decreases.

On the other hand, the power consumption of the circuit (Table 4.1) presents an increment as temperature decreases. The power variation is related to the mismatch of a non-dedicated PDK at 77 K, since as shown Figure 4.14 the simulation needs much more bias current to guarantee an identical experimental transconductance at 77 K. As a result, the bias current increment leads to a power consumtion rise in CAD simulation. The expected power dissipation shall decrease as the temperature falls, assuming identical performance, as explained in Chapter 3.1.3, and demonstrated in Chapter 5. The assumption of the PDK's mismatch is based on Figure 4.14, which demonstrates how the simulated drain current is much smaller than the experimental one, caused by a smaller transconductance. As a result, the simulation at 77 K requires a more bias current to guarantee an identical performance of transistors at a room temperature of 300 K. If the simulation implements the same bias current of experimental setup, the FE performance will decreases as shown Table 5.3. However, the power dissipation would match correctly.

Output signal waveform for a single PE at 300 K is illustrated by Figure 4.15. This graphic represents a transient-noise simulation of 50 wave-samples. Figure 4.16 shows an identical transient-noise simulation of 50 wave-samples, but in this case, at 77 K.

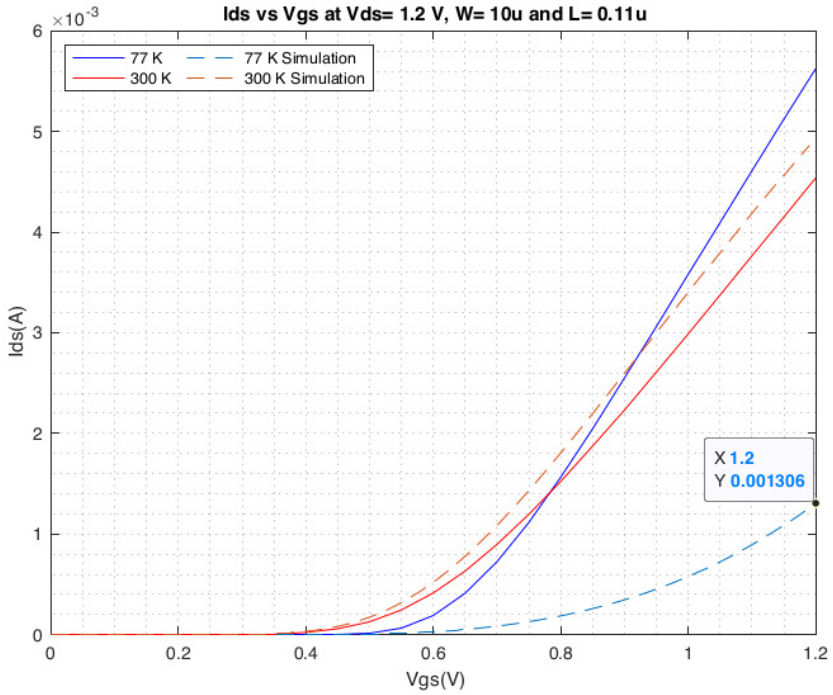

Figure 4.14: Drain current vs gate voltage of nMOS transistor W/L=10/0.11, simulation and experimental results

Parameters	**DS20K requirement**	**Simulation 77 K**	**Simulation 300 K**
V1pe (mV)	NoN	4.15	6.6
Vnoise (mV)	Non	0.46	2.73
SNR	8	9	2.4
Jitter (ns)	50	14	58
Dynamic Range (pe)	230	240	110
Rising time (ns)	150	150	160
Power (mW)	180	110	84

Table 4.1: Simulation results of Front-end electronics at 300 K and 77 K. NoN means there is no any specification for this parameter

The waveform is built by 50 samples of transient-noise simulation. Comparing both figures, the SNR and timing jitter improvements become apparent, and thus the advantages of low-temperature operation.

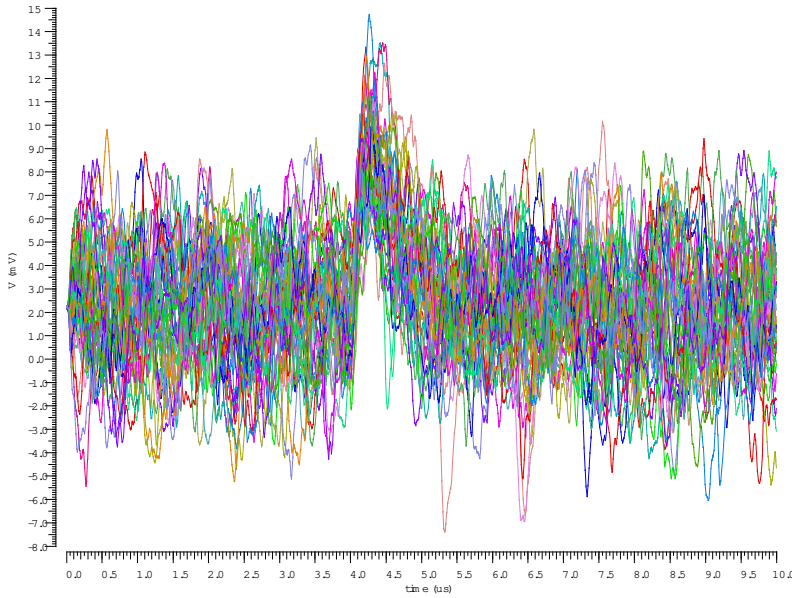

Figure 4.15: Output signal waveform of front-end electronics at 300 K.

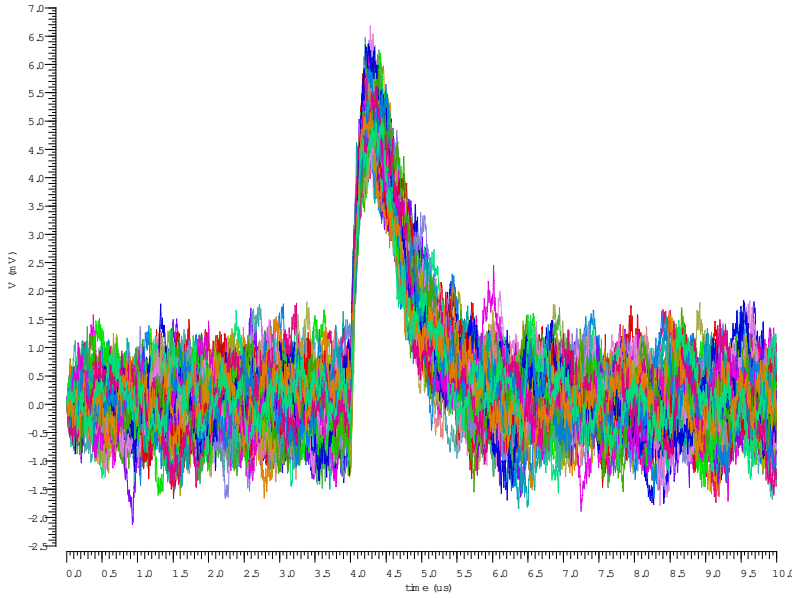

Figure 4.16: Output signal waveform of front-end electronics at 77 K.

4.4.1 Monte Carlo simulation

Monte Carlo simulation is a statistical technique implemented to figure out the uncertainty of variables or parameters from a model. In other words, a Monte Carlo simulation helps to visualize the potential outcomes due to the manufacturing variations. As a result, it creates a better idea of a figure of merit variability.

In an ASIC design, the Monte Carlo simulation describes how the key parameters, such as the input offset voltage and amplitude may fluctuate due to the process parameter variation and rando mismatch between devices. Figure 4.17 (left) illustrates the offset voltage variation of front-end electronics at 300 K. The offset of ASIC v1 was simulated around 384 μV, and DC voltage about 64 μV. The simulated offset is lower than the maximum target offset of 500 μV.

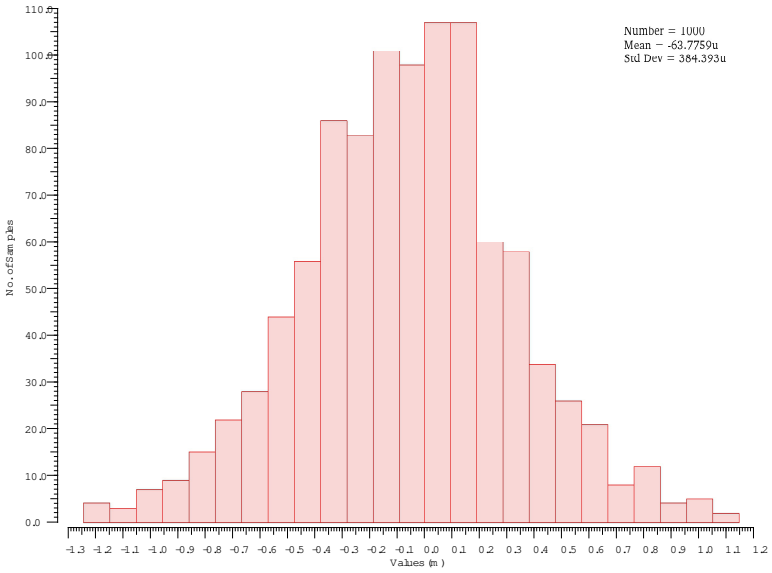

Figure 4.17: Mismatch Montecarlo simulation of input common mode at 300 K.

Monte Carlo simulation at room temperature and the study of mismatch variation over temperature (chapter 3.3.7) were considered to realize an approximation of mismatch at 77 K. This assumption is done considering the Equation 4.21. The input common-mode variation due to the mismatch strongly depends on the ratio $\frac{\mu_n}{\mu_p}$, transistor area and A_{th}. From these terms, the carrier mobility ratio remains almost equal, as was described in Chapter 3.9. The transistor area is constant on temperature.

Hence, only the mismatch parameter A_{th} presents an important variation on temperature. However, the A_{th} contribution becomes negligible in the transistors with a large area, as explained in Chapter 3.3.7.

$$\sigma^2(V_{off}) = \frac{A_{th}^2(T)}{WL_{1,2}} + (\frac{\mu_n}{\mu_p})^2 \frac{A_{th}^2(T)}{WL_{11,12}} \tag{4.21}$$

In the cryogenic ASIC v1, offset voltage is dominated by the pMOS input pair. Then, following the temperature variation of mismatch parameter (Figure 3.18), the large area of input pairs exploits a A_{th} growth lower than 5 % at 77 K. Therefore, the expected offset voltage is roughly identical to the room temperature value. In any case, this is lower than the maximum allowable offset of 500 μV.

Moreover, Monte Carlo simulation was applied to other key parameters of the ASIC v1. As a result, Figure 4.18 illustrates the output baseline fluctuation at 300 K. The baseline variation becomes an essential parameter in our design, given that the mean goal is the mass-production (3000 ICs) for the VETO system (DarkSide20K). Then, a large fluctuation may make that many ICs work with specifications far away from the required performance.

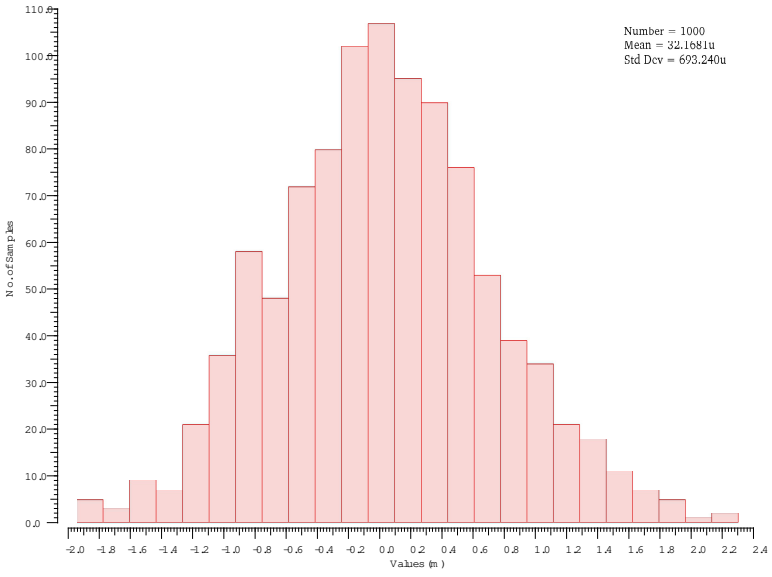

Figure 4.18: Mismatch Montecarlo simulation of output baseline at 300 K.

On the other side, Figure 4.19 represents the amplitude variability due to the random mismatch at 300 K. The single PE amplitude describes a negligible variation due to the mismatch effect. Thus, the amplitude of ASIC v1 will present an adequate uniformity.

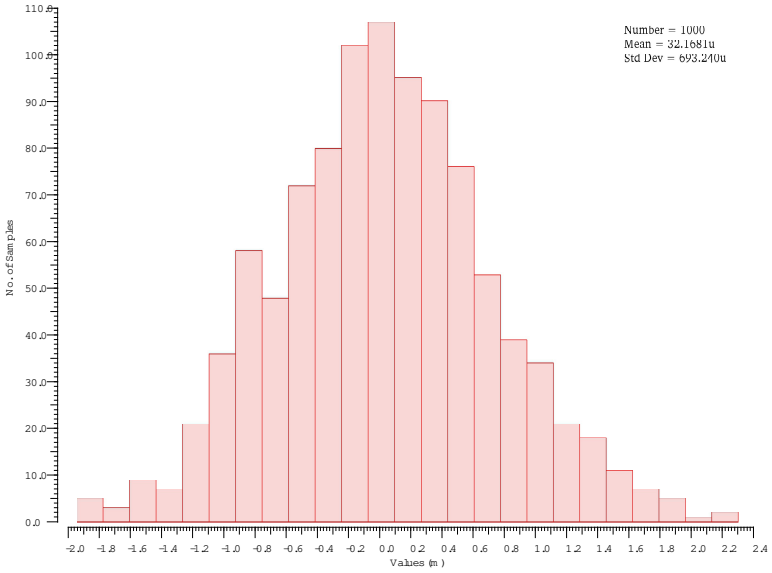

Figure 4.19: Mismatch Montecarlo simulation of output amplitude at 300 K.

Afterward, one of the figures of merit (SNR) presents a deviation illustrated by Figure 4.20. The SNR sigma is equal to 72 m, then a worst-case SNR equal to 9.2. Even though the SNR fluctuates, the result is still substantially higher than the minimum requirement of SNR = 8.

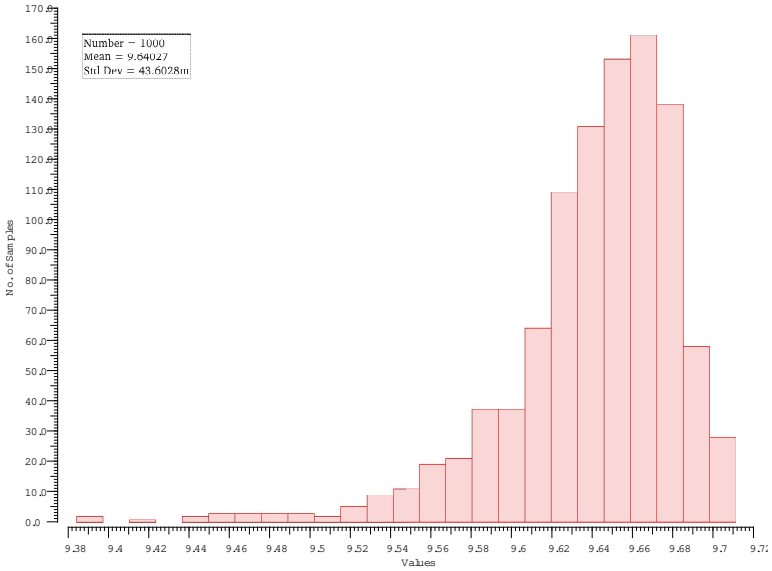

Figure 4.20: Mismatch Montecarlo simulation of signal to noise ratio.

Chapter 5

Experimental results of cryogenic ASIC v1

Cryogenic ASIC v1 was tested in a Liquid Nitrogen bath that provides, under standard atmospheric pressure, a temperature close to that of LAr. The test setup must provide a complete light isolation in order to obtain the optimal experimental results. The large area sensor is in fact sensitive to visible light, and thus the photodetection system might not be able to detect and properly measure the PE generated inside the cryostat.

5.1 Experimental setup for cryogenic electronics

The implemented cryogenic front-end electronic in 110 nm occupies an area of 1 ×2.5 mm^2 including the pad ring structure. The integrated circuit (IC) core was mounted on an FR4 PCB, as shown in Figure 5.1. The ASIC v1 was wire-bonded using Aluminum wires with an approximate length of 3 mm. The bonding points provide external current and voltage biasing. In addition, the PCB interconnects the 4-quadrants of SiPMs (4-input ports) to the 4-TIAs circuit of the front-end IC.

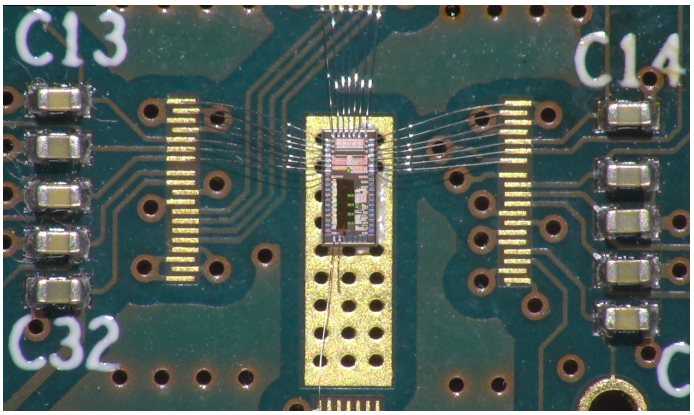

Figure 5.1: Silicon ASIC v1 mounted and wire-bonded on the PCB.

ASIC v1 experimental tests were perforemd at both room and cryogenic temperatures of 77 K. The tests include the Darkside 20K sensor, described in the section 4.1. The SiPM detector employs a CAEN DT1407ET as a power supply unit. The sensor bias voltage was varied in a range from 54 V to 70 V for cryogenic tests. For room temperature measurements, the bias voltage range is from 64 V to 80 V. The bias voltage difference is related to the breakdown voltage reduction as temperature decreases in the SiPM. Front-end electronics power supply (AVDD & AVCC) were externally fed by a TTi QL5647 power supply unit. The power unit hands over a voltage equal to 1.25 V and −1.25 V, respectively.

The cryogenic setup uses a 60 cm height dewar, as illustrated the Figure 5.2. In the setup, the data acquisition is implemented by connecting the analog output inside the dewar to the external digitizer. The dewar contains the Liquid Nitrogen and provide a completely dark environment for correct testing. A dark environment is in fact critical, since non-desired light can compromise the reliability of the measurements and even saturate the cryogenic electronics, causing useless results. Additionally, the dewar

isolates the photodetection system from electromagnetic pick-up. This is necessary because, due to its large area, the SiPM tile could work as an antenna catching the external electromagnetic noise.

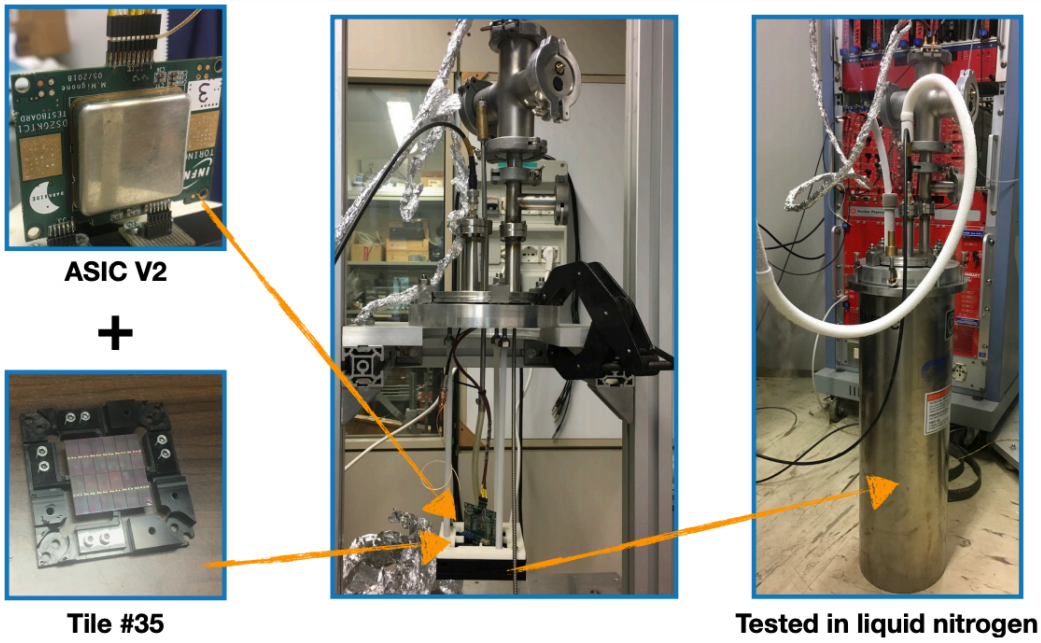

Figure 5.2: Cryogenic setup implemented for the ASIC v1 test.

The cryogenic setup uses an external optical fiber to convey photons from a Hamamatsu pulsed 403 nm laser into the dewar, as shown in Figure 5.3. The optical fiber points to the SiPM detector surface, guaranteeing a high number of PE arrivals, and a low delay. In this way, the PE refraction within the dewear walls is strongly suppressed. The cryogenic front-end output port is connected to a 50 Ω oscilloscope input. A LECROY oscilloscope employs the laser pulse as a trigger since it correlates the generated pulse with the output signal.

The output signal, digitized by an 8-bit ADC, is processed to detect and extract the amplitude of the triggered output signal. The peak voltages are distributed in a voltage histogram, and fitted by several Gaussian curves, as shown in Figure 5.4. From the peak voltage histogram, the SNR represents the ratio between the mean value of first peak and its standard deviation. The Figure 5.5 represents a peak voltage histogram, implementing the new SiPM detector developed within Darkside collaboration, with a 9 VoV. The single PE presents a SNR equal to 17.7. The new detector has been produced

recently, then I have developed a DSP program (Section 5.4) to enhance the SNR of output signal.

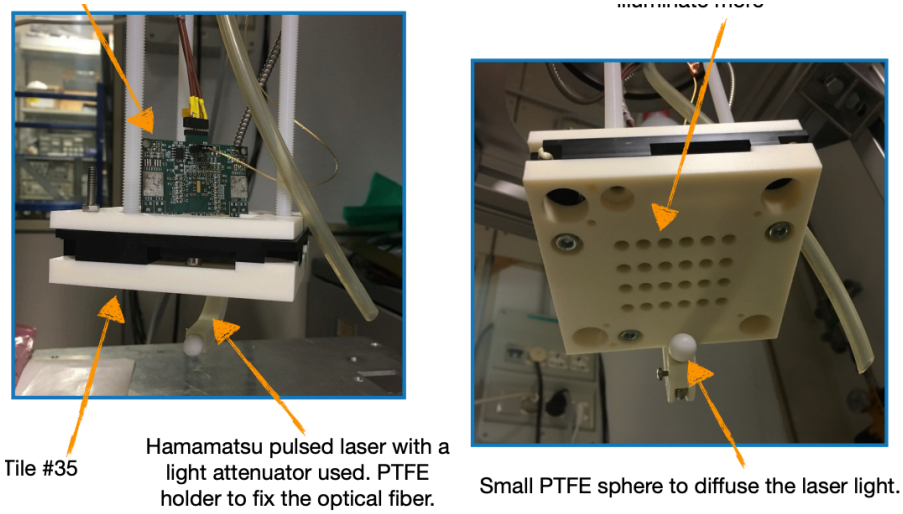

Figure 5.3: Optical fiber location on the cryogenic electronics setup

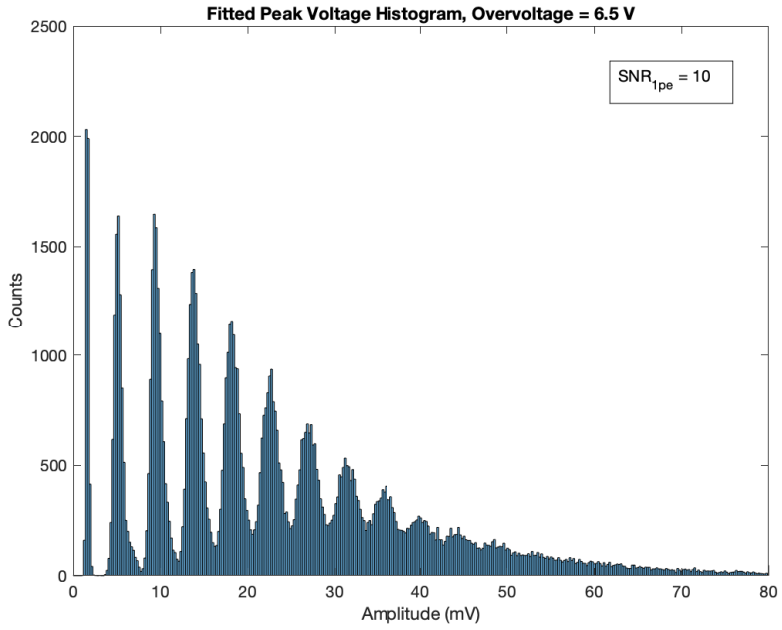

Figure 5.4: Peak voltages histogram of ASIC v1 applying a 6.5 V of overvoltage to SiPM.

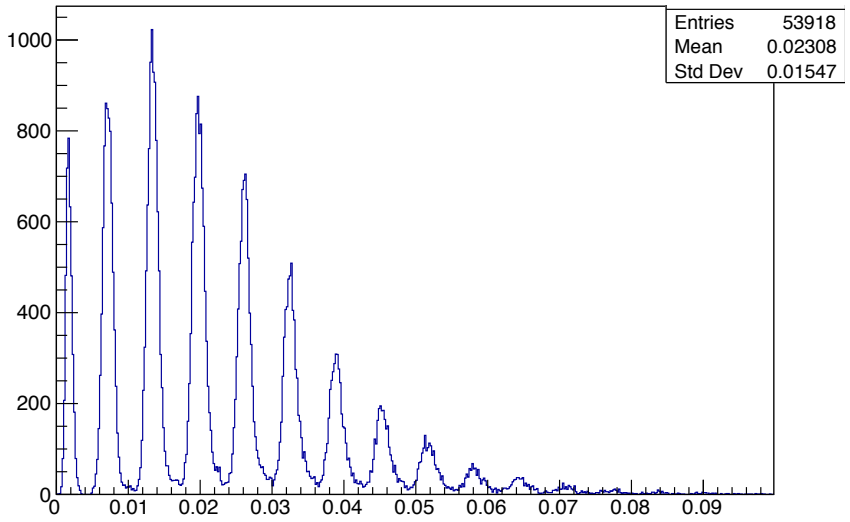

Figure 5.5: Peak voltages histogram of ASIC v1 applying a 9 V of overvoltage to the new SiPM detector. The SNR is equal to 17.7.

5.2 Key parameters of the photon-electron signal

Photo-electronics systems are employed in two different areas of the DarkSide-20K experiment. Firstly, the photodetection module (PDM) is implemented in the time projection chamber (TPC). In this module, the cold electronic must provide a minimum signal-to-noise ratio (SNR $\geq$ 8) and a maximum timing jitter equal to 50 ns. Secondly, the PDM for the VETO structure, which must be integrated by a readout electronics with a dynamic range higher than 200 PEs with an SNR $\geq$ 6. Besides, the rising-edge should be equal to or lower than 150 ns to avoid pile-up.

The following group of parameters has been established as a benchmark, to analyze and determine the efficiency of the cryogenic system. Besides, these are utilized to check the fulfillment of the experiment requirements.

5.2.1 RMS noise

RMS noise is a fundamental parameter in all ICs since this value means how much the undesired signal (random) overlaps the desired signal. Moreover, the RMS noise is necessary to compute the SNR and the timing jitter. Obviously, the lower the RMS noise, the higher the IC performance. The RMS noise was measured by computing the root mean squared of the baseline signal over time. Then, the RMS noise distribution,

with a typical Gaussian curve, is described by Figure 5.6. The mean value of the RMS noise distribution reaches 0.4919 mV at 77 K with a standard variation of 60 μV.

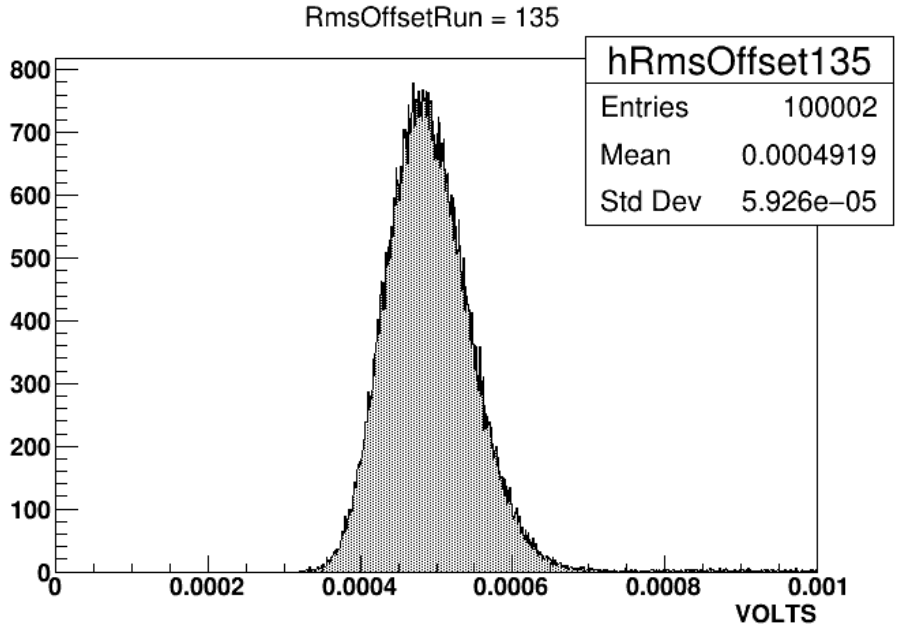

Figure 5.6: RMS noise of the output baseline evaluated 6 us before the pulse.

From room to cryogenic temperatures environment, RMS noise exhibits a reduction around 3 times following the thermal noise contribution ($\frac{4k_BT}{g_m}$). This means the front-end electronics exhibit a considerable dependence on the series noise. The flicker noise variation is almost negligible, as was expected. Furthermore, its expected increment at 77 K is low, as was described in Figure 3.4. The simulation and experimental result of the RMS noise is compared in the Table 5.3.

5.2.2 Signal to noise ratio (SNR)

SNR is one of the primary figures of merit in this study, and it is computed as the ratio between the amplitude of single PE and the RMS noise. However, as shown the Table 5.1 the SNR could be represented by two terms. Primarily, SNR_{rms} represents the theoretical SNR explained previously, the peak voltage of 1 PE over the RMS noise. Secondly, SNR_{peak} represents the ratio between the amplitude of 1 PE and its standard deviation. In this study, the SNR_{peak} is required to be higher than 8 for TPC and 6 for VETO. An SNR > 8 means a 4σ probability (99.999%) that a PE signal is not mistaken as

a peak noise sample. σ_{FE} represents the RMS noise of the system measured from the baseline data. The measurements were realized by applying a bias voltage lower than the SiPM's breakdown voltage. σ_{FE} is used to obtain the SNR_{rms}. σ_{1PE} represents the standard deviation of the peak voltage variation of a single PE, which increases as the SiPM's overvoltage rises due to the increments of injected charge.

Overvoltage (V)	V_{out} **(mv)**	σ_{FE} **(mv)**	σ_{1PE}	SNR_{rms}	SNR_{peak}
4	3.43	0.49	0.49	7.5	7.5
5	4.46	0.49	0.50	9.1	8.7
6	5.30	0.49	0.55	11.0	9.6
7	6.22	0.49	0.60	13.0	10.4
8	7.06	0.49	0.65	14.7	10.9

Table 5.1: Signal to noise ratio table vs overvoltages

Cryogenic ASIC v1 exhibits excellent results in terms of SNR above 4 VoV, as shown in Table 5.1. It must be observed that the SiPM detector cannot be operated by a bias voltage higher than 7 VoV, otherwise the afterpulsing (AP) and direct crosstalk (DiCT) probability increase to more than 40 %, overcoming the maximum allowable AP & DiCT probability acceptable in DarkSide-20k.

A new SiPM prototype developed in the Darkside collaboration allows the overvoltage to be implemented up to 11 V. The new advantage improves the SNR and timing jitter considerably, as shown Figure Table 5.2. Implementing the new SiPM detector, the output signal achieves an excellent SNR achieves value of 22 at 11 VoV. Furthermore, the new detector provides an elevated charge gain in respect to the previous SiPM prototype. As a result, the SNR presents a higher value assuming the idential overvoltage condition.

Overvoltage (V)	V_{out} **(mv)**	σ_{rms}	SNR_{rms}
5	5.29	0.55	9.6
6	6.39	0.55	11.6
7.5	8.10	0.55	14.7
9	9.73	0.55	17.7
11	11.36	0.52	22

Table 5.2: Signal to noise ratio table vs overvoltages using a new SiPM structure

5.2.3 Rising time

Rising-edge is determined by measuring the time taken by the output signal to swing from 10% to 90 % of its amplitude. In the ASIC v1 experimental tests, the rising time was measured to be around 150 ns, as shown in the zoomed Figure 5.7 (bottom). Figure 5.7 (top) illustrates the typical amplified output signal of the SiPM readout. Moreover, from the rising time value, it can be inferred that ASIC v1 develops a bandwidth of about 2 MHz.

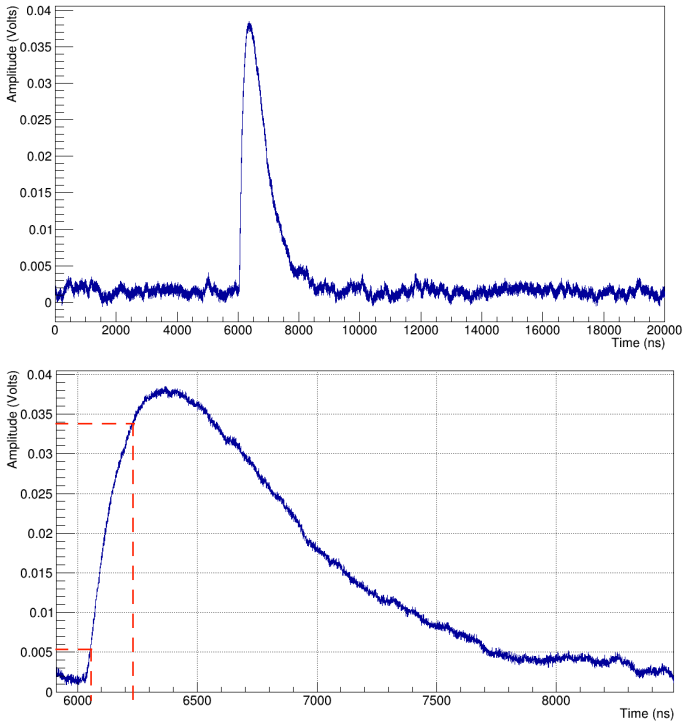

Figure 5.7: Photo-electrons output signal (top), Zoomed photo-electron signal (bottom).

5.2.4 Linearity

Linearity is the capability of an amplifier to maintain a given and constant proportionality between its input and output signals [74]. In electronics design, linearity becomes a relevant test for reliability. Deviation from linearity may in fact induce a strong signal distortion and thus modify or corrupt the measurement results. For instance, if a large number of PEs, 200 PEs, impinge on the sensor, these generate a given amplitude due to

the gain of front-end electronics. However, the theoretical amplitude may be reduced due to the circuit non-linearity, and thus the resulting amplitude will not represent the real number of detected PEs. Figure 5.8 (Top) illustrates the expected linear behavior of the output amplitude as a function of the photo-electron numbers, in this case, up to the 11th PE.

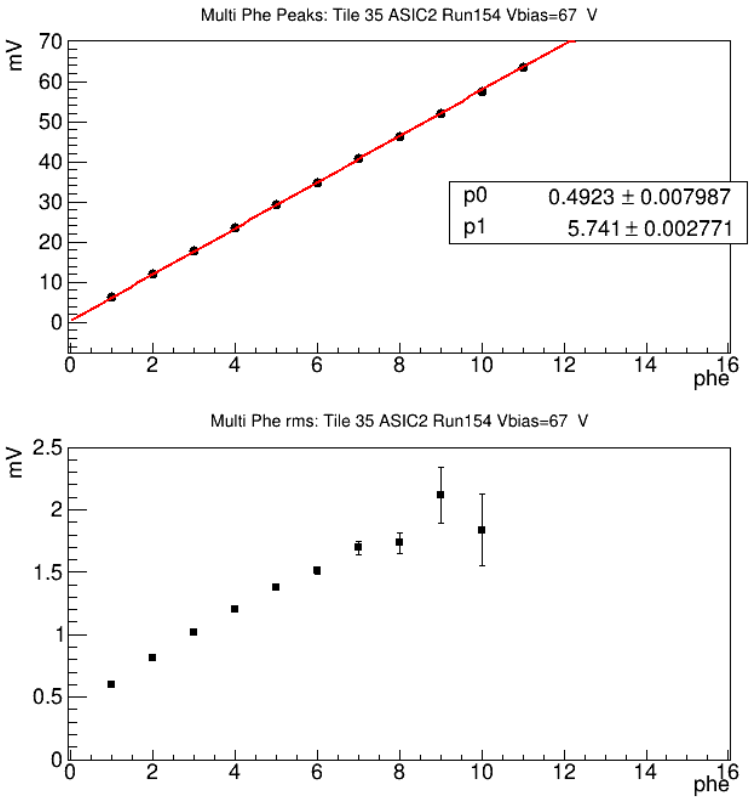

Figure 5.8: Front-end electronic linearity (Top) and RMS noise variation (bottom) over number of photo-electrons.

Figure 5.8 (Bottom) represents instead the standard deviation (σ_n) increment of the nth order of PEs. σ_n growth presents a root square behavior following the $\sigma_n = \sqrt{\sigma_{rms}^2 + n\sigma_{sipm}^2}$ term. Where, the σ_{rms} represents the standard deviation of baseline, and σ_{sipm} is the SiPM resolution in response to the single photo-electron signal.

5.2.5 Dynamic range

Dynamic range is defined as the number of PEs that an amplifier can process without achieving the signal saturation. Experimentally, the designed cryogenic electronics accomplishes a voltage swing around 800 mV, as shown the Figure 5.9. Then, considering a SiPM overvoltage of 4 V, the ASIC v1 can readout more than 220 PEs. However, the dynamic range is reduced up to 170 PEs in case the SiPM overvoltage becomes 5 V.

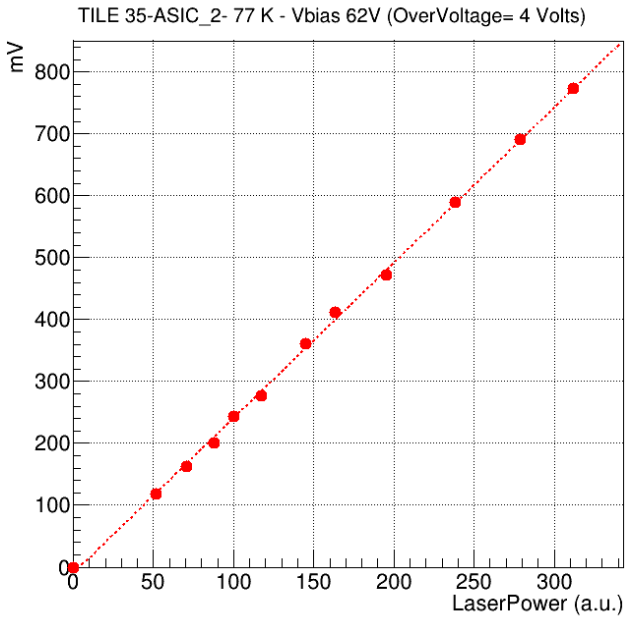

Figure 5.9: Front-end electronic linearity and dynamic range over number of photoelectrons.

Moreover, Figure 5.10 illustrates an overlapping of 4 peak voltage histograms with different scintillation intensities. The dynamic range test has demonstrated how the ASIC v1 is able to process small and large luminosity scintillation events. Large scintillation events are typical of the VETO structure. ASIC v1 can provide a peak voltage histogram with more than 800 mV.

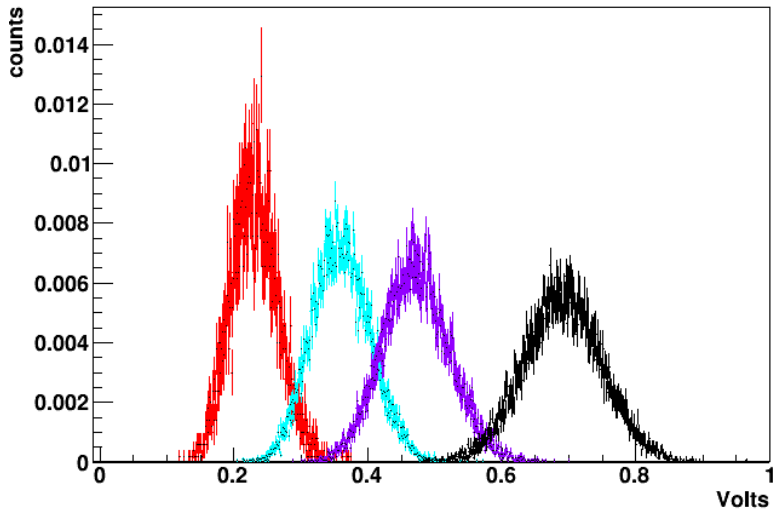

Figure 5.10: Front-end electronic linearity (top) and RMS noise variation (bottom) over number of photo-electrons.

5.2.6 Experimental and simulation results

Comparison of experimental and simulation results becomes an interesting analysis in terms of expected performances at both 300 K and 77 K. Initially, the experimental output signal waveform is compared to the CAD simulation waveform at 77 K, as shown in Figure 5.11. The simulated signal performs a quite similar rising time and amplitude values, as is described by Figure 5.11. The Table 5.3 describes the power comsuption discrepancy between simulation and experimental results. If the bias current tunning is not realized to achieve the desired transconductance, the simulated power would match the experimental power. However, it generates a bad performance as shown Table 5.3.

Moreover, Figure 5.11 highlights a discrepancy within the baseline of both experimental and simulation signal. The offset voltage of the experimental waveform remains in the expected margin variation of 3σ = 1.5 mV due to the mismatch. The baseline mismatch was simulated within Chapter 4.4.1 (Figure 4.18).

In the circuit design and experimental tests, test structures of single transistors results (Chapter 3.3) were highly important and sufficient to obtain the expected and optimal silicon results, as was described in this Chapter.

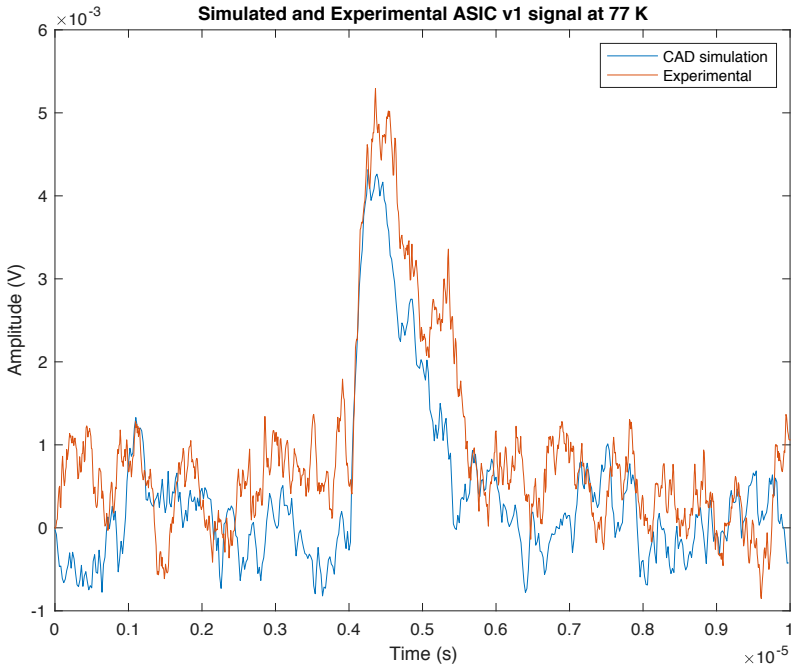

Figure 5.11: Simulated and experimental output waveform at 77 K .

Parameters	**Simulation 77 K**	**No tuned simulation**	**Experimental 77 K**
V1pe (mV)	4.15	4	4.36
Vnoise (μV)	460	530	480
SNR	9	7.7	9.1
Jitter (ns)	14	20	15
Rising time (ns)	150	200	150
Dynamic Range (pe)	240	240	180
Power (mW)	115	67.2	70

Table 5.3: Experimental and simulation results of Front-end electronics at 77 K, applying an overvoltage equal to 5 V.

5.3 Output voltage histogram at different SiPM bias voltages

Peak voltage histogram represents the PE amplitude distribution during a long run acquisition. The histogram illustrates several peaks, which represents the amplitude of n number of PE, as shown in Figure 5.12 (left). Furthermore, PE amplitude is affected by the noise-causing a fluctuation in the magnitude. In this case, each histogram peak is fitted by a gaussian curve (Figure 5.12 right), providing a standard deviation. The amplitude and the standard deviation of the n^{th} order of PE define to the SNR. The SNR can be enhanced by increasing the SiPM bias voltage, as shown the Table 5.1. However, a large increment could lead to an afterpulsing and crosstalk probability rise over the experiment requirements, as it was illustrated in Chapter 4.1.

Initially, the laser intensity was set to the minimum power detectable by the SiPM, since it facilitates the detection of the first n^{th} order PEs, as shown in Figure 5.12. Here, it is illustrated a peak voltage histogram from several acquisitions using the oscilloscope's internal validated trigger. The trigger is turned on by the laser, which allows the correlated PE signal waveform to be collected. Next, the amplitude of each acquired waveform signal is represented by a count in the peak voltage histogram. Each histogram was built by 100.000 output signal waveforms.

Moreover, it is possible to achieve a higher n_{th} order PE by increasing the laser intensity, as shown in Figure 5.4 and in Figure 5.13. In fact, these graphics reach values of 80 - 160 mV. Besides, the two histograms were obtained with different SiPM bias voltages. For instance, Figure 5.4 was obtained by using 6.5 V of overvoltage (VoV), generating a longer gap between peaks in comparison to Figure 5.12. In the meantime, Figure 5.13 was obtained using an overvoltage of 8 V, increasing further the gap between peaks. However, this new bias voltage overcomes the maximum allowable value, causing an excessive increment of afterpulsing and crosstalk probability. As a result, the SNR increment starts to be reduced in comparison to the SNR registered by 7 VoV in Table 5.1. The AP and DiCT generate a wide variability of waveform amplitude, causing a rise in the standard deviation of each peak. Figure 5.14 illustrates the peak voltage histogram implementing the new SiPM detector, which was optimized to improve the charge gain, and to perform overvoltage values up to 11 V.

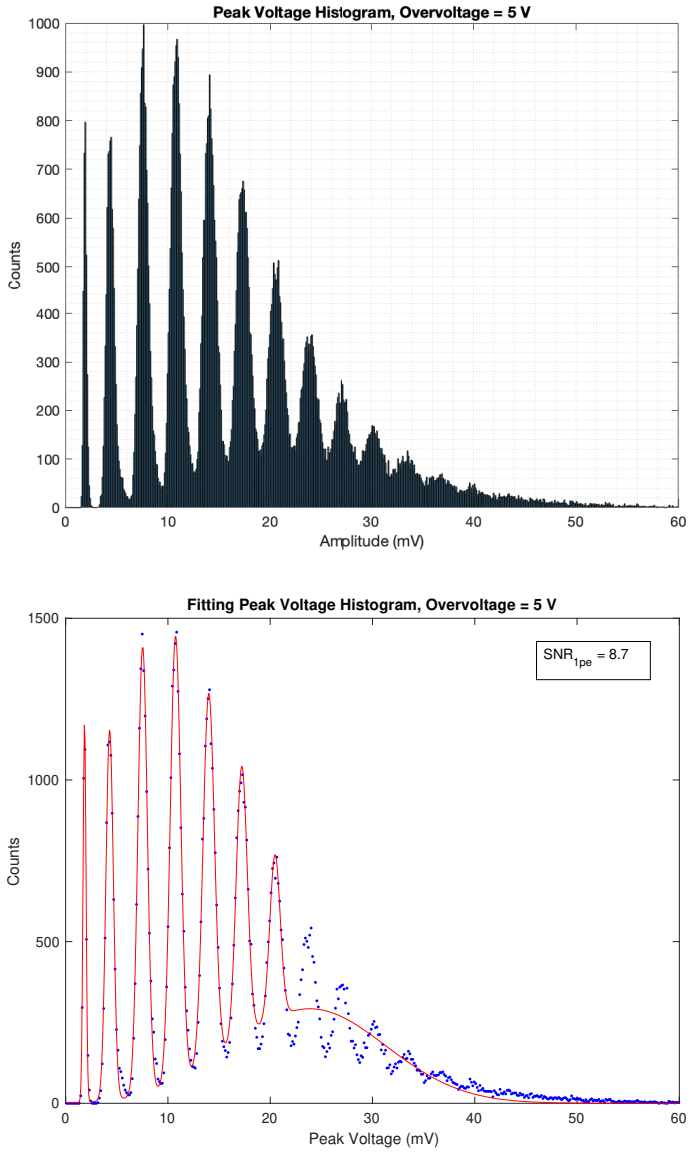

Figure 5.12: Peak voltage histogram with a low laser intensity at 5 VoV (top), and fitted histogram (bottom).

From peak voltage histograms, it has been demonstrated how the cryogenic integrated electronics can efficiently readout, process, and amplify the signal from large area SiPMs, since the first PEs are well-separated from each other. The peak separation guarantees a low probability that the baseline will be misunderstood as a PE arrival.

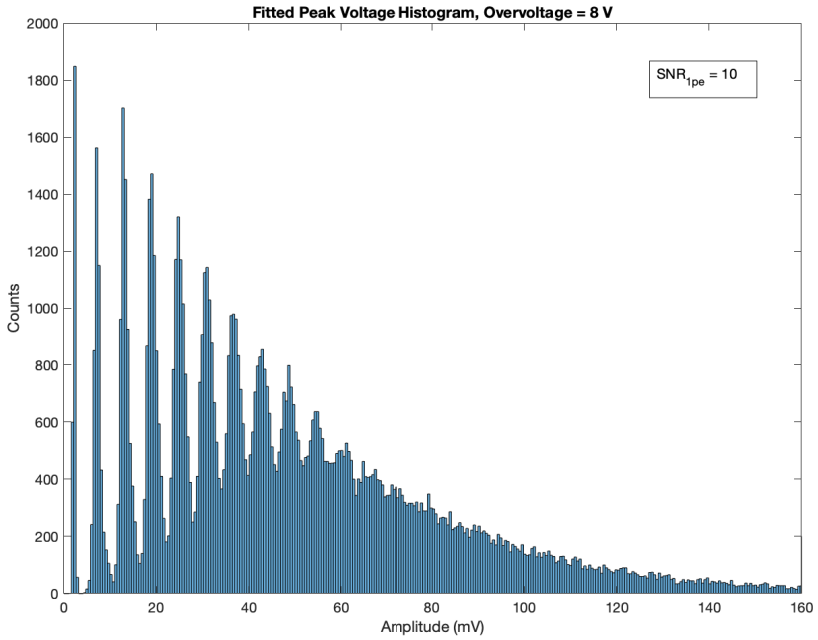

Figure 5.13: Peak voltages histogram with a high laser intensity at 8 VoV.

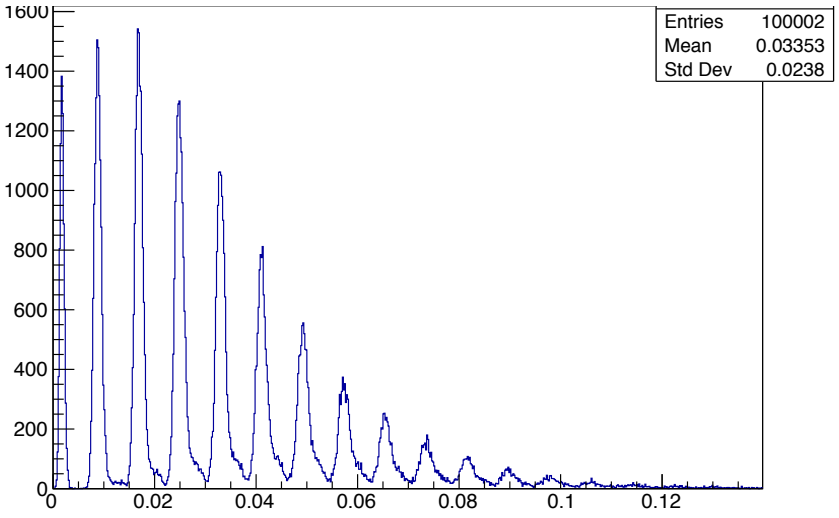

Figure 5.14: Peak voltages histogram of ASIC v1 applying a 11 V of overvoltage to the new SiPM detector.

5.4 Digital filtering for dark matter measurements

Digital signal processing (DSP) has been developed in nuclear physics detection [75] and nuclear spectroscopy [76] in the recent decades. Digital filtering owns several advantages and higher efficiency in comparison to traditional analog signal processing methods. In fact, traditional methods find some limitations to improve the desired signal quality without risking stability. The main aim of this study is to implement a DSP algorithm to enhance by more than 30 %, in real-time, the figure of merit (FOM) of the neutrino and dark matter measurements. In this case, the relevant FOM is the signal to noise ratio (SNR). In turn, this improvement will allow the worst-case condition of the front-end electronics (SNR = 6) to reach the minimum requirement, described by the experiment (SNR = 8 or 4 σ resolution). The digital pulse processing method was implemented using the digital cusp-like or trapezoidal filter [77].

Digital pulse processing (DPP) reduces the proportion of undesired signal over the mean signal. In other words, it minimizes the impact of the noise sources in the cryogenic front-end electronics. The noise sources are divided into parallel noise due to the leakage current provided by the detector, series thermal noise due to the input capacitance, and flicker or low-frequency noise [58]. Even though the front-end integrated electronics works at a temperature of 77 K, the total detector capacitance presents a value of 10 nF. Hence, the series noise contribution plays a very crucial role in limiting the circuit performance. A digital filter that helps in cleaning-up the series white noise from the digitized data in real-time can therefore be of great interest for the application.

On the other hand, the integrated electronics (Figure 1) present a low 1/f noise contribution due to its large transistor area. The the transistor sizing is performed to reduce the hot carrier effect on the one hand, and to maximise the trasconductance on the other. Therefore, very large devices are used in the input stage. Although the flicker noise is negligible at high frequency in this application, the CMOS technology may produce a 1/f noise increment at low temperatures [5]. It is essential to hold the noise increment at a low level, in case of medium to low frequency applications. A digital trapezoidal pulse-shaper was chosen as the structure to build the real-time filter algorithm since it accomplishes a high noise reduction in the case of a series and a parallel noise contribution [78].

Total RMS noise is significantly decreased by setting an optimal shaping/peaking time within the digital trapezoidal filter. For instance, the series noise drops as the peaking time of the trapezoidal waveform increases. However, the parallel noise presents

an opposite behavior [45]. Hence, the shaping time was tuned to obtain optimal performance in terms of series and parallel noise contributions. Furthermore, in a digital filter the shaping time can easily be adapted and optimized according to the particular context. For instance, a long peaking time is preferable in a low rate application. On the other hand, a short shaping time is necessary when the rate is higher. In addition, the trapezoidal filter can be effectively syntesized for real time applications also with moderate clock frequencies. In our implementation, we have used a clock frequency of 125 MHz.

Figure 5.15 illustrates the full schematic for the SiPM readout and signal filtering. The figure includes the 4-inputs cryogenic front-end electronics (Chapter 3), a 14-bit ADC, and the DSP filter implemented on FPGA. The ADC and FPGA are located outise the cold volume and operate a room temperature.

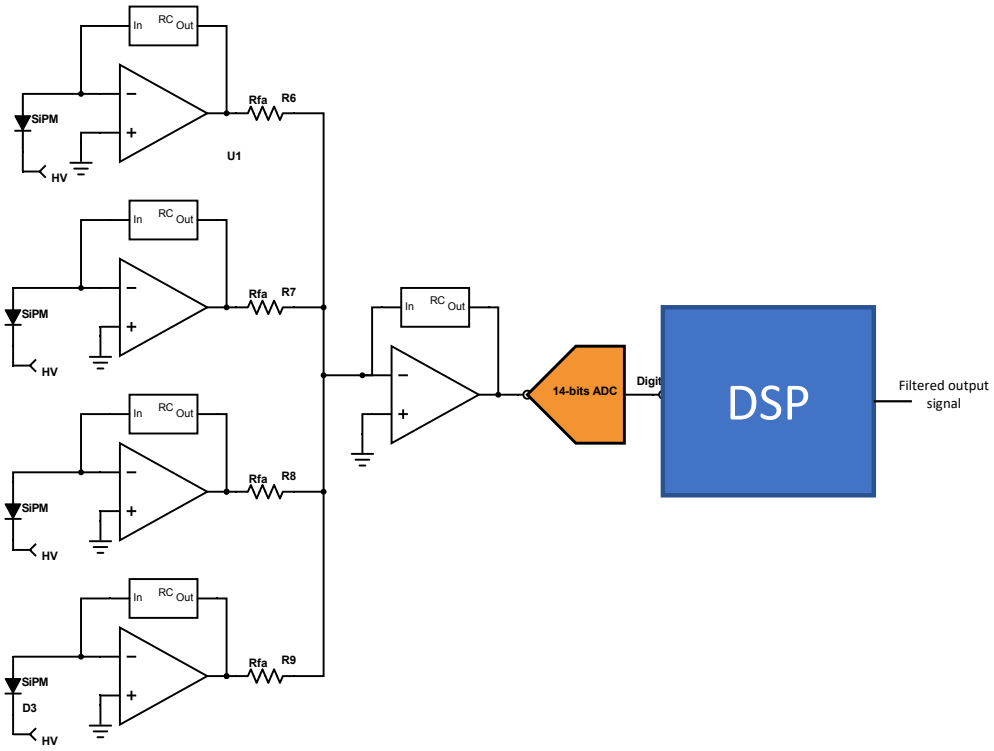

Figure 5.15: Front-end integrated electronics schematic plus an ADC and DSP block

Real-time trapezoidal filter processes and enhances the output signal from the photoelectron detection system and it could be very useful in the DarkSide-20k experiment.

The PE detection is performed by the SiPM sensor and the front-end integrated electronics operating at 77 K, described in Chapter 4.2 and shown in Figure 5.15. The combination of the photodetection module and the digital filter become an important tool in the neutrino [79] and dark matter [67] experiments with large area detectors.

Experimentally, cold electronic provides already good performance in terms of the signal-to-noise ratio. The test results have demonstrated a SNR value of 10 for an overvoltage of 6.5 V, which guarantees a detection resolution higher than 4-sigma. However, the SNR could be critical for bias voltages equal to 3-4 VoV. Then, digital filtering allows the FOM to be enhanced, in the case of 6.5 VoV, up to an SNR $>$ 14, and an SNR $>$ 8 for a 3 VoV condition.

5.4.1 Digital trapezoidal pulse-shaper

The real-time digital filter provides a symmetrical trapezoidal pulse at 125 MSa/s. The sampling frequency was chosen as the best noise reduction from several parametric simulations on Matlab. a clock frequency higher than 125 MHz does not provide advancements in terms of noise reduction in this database, however higher FPGA performance would increase the cost. Figure 5.16 shows the typical analog input waveform (PDM's output signal) at 6 VoV, which presents the following features: a peaking time around 250 ns, a falling-edge of 900 ns, an RMS noise of 550 μV, and a single photoelectron amplitude of 5.3 mV. The previous parameters will be compared against the post-filtering signal in order to check the digital filtering efficiency.

The trapezoidal pulse-shaper schematic is illustrated in Figure 5.17. As the figure illustrates, the pulse-shaper is divided into 4 stages with different purposes within the shaping process. First and second stage are described by Equation 5.1 and 5.2. These are the delay units programmed with a FIFO block, which exhibits a depth of 200 samples. The FIFO depth fixes the total delay of the unit, and consequently the rising and falling edge time of the trapezoidal waveform. In this design, the $Delay_a$ and $Delay_b$ (FIFO) were featured to obtain an optimal peaking time (200 samples $\times$ 8 ns of sampling period) equal to 1.6 μs. The optimal shaping time was chosen, due to its better noise reduction result, from a parametric simulation of the delay time on Matlab. Moreover, the flat zone of the trapezoid's top becomes almost zero by programming both the first and the second stage with the same delay, since the flat zone is determined by the absolute value of the difference between $Delay_a$ and $Delay_b$.

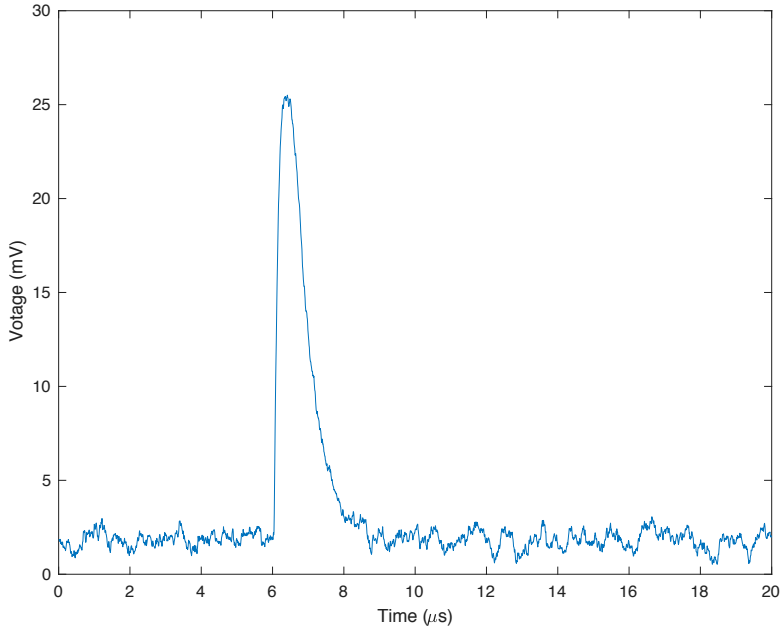

Figure 5.16: Single photo-electron waveform before digitizing

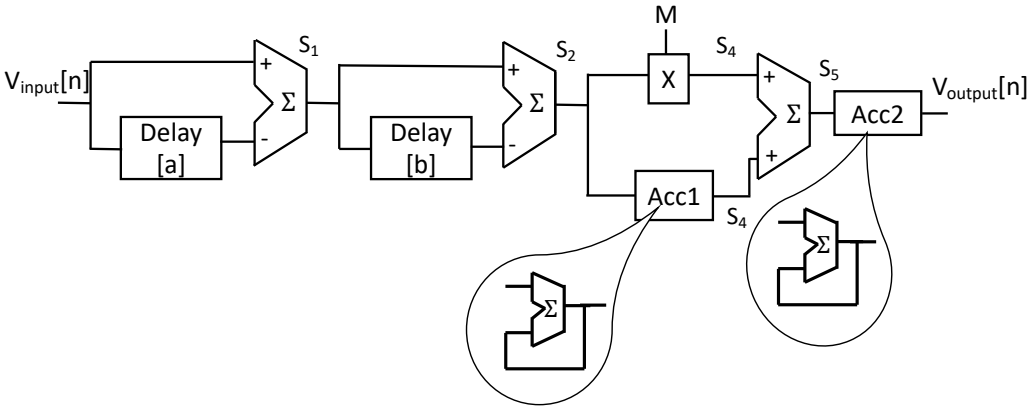

Figure 5.17: Digital trapezoidal filter schematic

Equation 5.3 and 5.4 describe the operation of the third stage. This stage represents a high-pass network on the system, which includes a multiplication factor (M) in one of its branches. M factor is implemented to cancel the exponential term of the analog input

signal. For this reason, the M factor depends on the ratio between the sampling time and decay time constant, as shown by Equation 5.6. The high-pass network deconvolutes the analog output signal, with a decay time constant (τ_{decay}), into a step signal. The output signal of the third stage (S_4) is illustrated in the post-implementation timing simulation (Figure 5.19).

In this digital trapezoidal filter design, the third stage is computed by applying a sampling time (τ_{clk}) of 8 ns and a decay time constant τ_{decay} of 680 ns. Hence, the M factor value is equal to 85, following Equation 5.6. The $Delay_a$, $Delay_b$ and M factor are key parameters, which were set in the digital pulse processing algorithm. The key equations used in the filter design are summarized hereafter.

$$S_1[n] = V_{in}[n] - V_{in}[n - delay1] \tag{5.1}$$

$$S_2[n] = S_1[n] - S_1[n - delay2] \tag{5.2}$$

$$S_3[n] = S_2[n] + S_3[n - 1] \tag{5.3}$$

$$S_4[n] = S_3[n] + M * S_2[n] \tag{5.4}$$

$$V_{output}[n] = S_4[n] + V_{output}[n - 1] \tag{5.5}$$

$$M = \frac{1}{e^{\frac{\tau_{clk}}{\tau_{decay}}} - 1} \tag{5.6}$$

5.4.2 Simulation and implementation tool

Synthesis and place & route process were carried out using the Vivado tool. The synthesis and implementation steps were accomplished by using the Xilinx Kintex-7 FPGA KC705 Evaluation Kit with a clock frequency of 125 MHz. The total on-chip power consumption of the digital trapezoidal filter is equal to 0.198 W. Furthermore, the digital filter implementation occupies a total area smaller than 3 % of the total available area in the FPGA. The digitized signal is supplied by a 14-bits ADC, which samples the analog

signal from the integrated electronics at 125 MSa/s. The ADC output data is synchronized with the FPGA clock to make the input signal and rising-edge clock arrivals to be simultaneous.

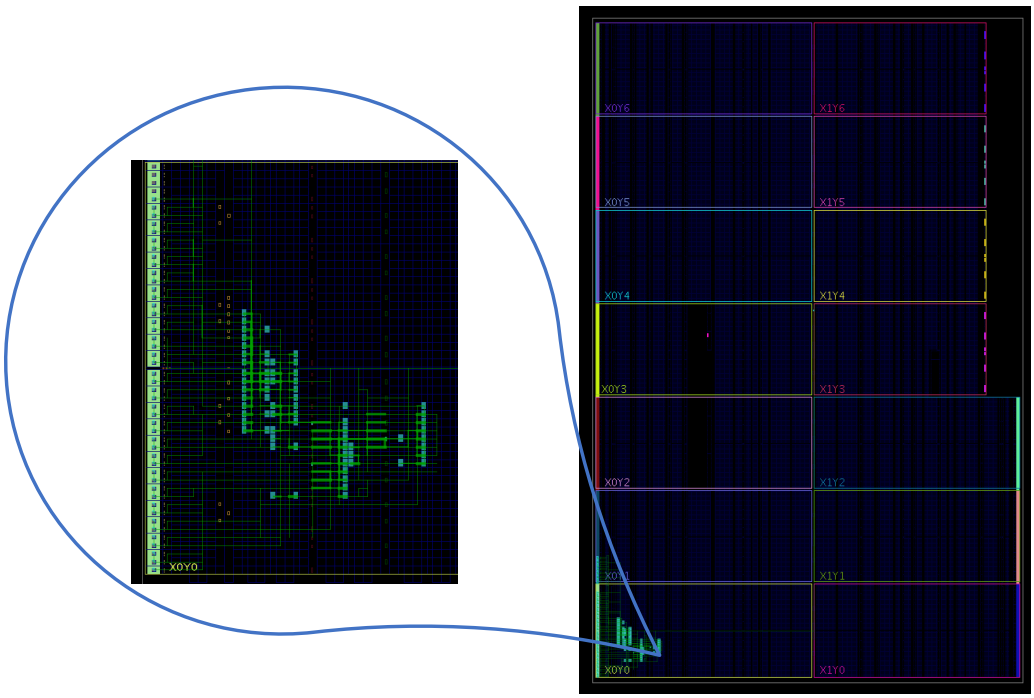

Figure 5.18: Place & Route layout of the digital trapezoidal filter

Post-implementation timing simulation is shown within Figure 5.19. This figure presents the shaped signal waveform stage by stage described by (Figure 5.17). The first signal (V_{in}) represents the digitized signal or initial exponential pulse. S_1 and S_2 respectively represent the output signal from the delay units, S_4 describes the high-pass network output signal. This stage shows how the digitized signal has been converted into a positive and negative step signal. Finally, V_{in} depicts the trapezoidal waveform with a similar amplitude in comparison to the front-end electronics output signal.

1

Figure 5.19: Signal waveform produced on the output of each stage

5.4.3 Filtering post-implementation results

Post-implementation results were realized by processing a database with 25x10^6 samples or 200 ms of data acquisition from the photo-detection module output signal. The experimental database, acquired using the 24 cm^2 SiPM and ASIC v1, is digitized and employed as the input data of the trapezoidal digital filter. A peak voltage histogram was generated to check the efficiency of digital filtering, with the output amplitude before and after real-time digital filtering.

Figure 5.20 illustrates the peak voltage histogram results before digital filtering. For a FOM's analysis, the SNR was divided into two terms in this study, as shown the Figure 5.20. This figure provides the information of SNR_{base} and SNR_{1p}. SNR_{base} represents the ratio between one photo-electron (PE) amplitude and the standard deviation (std) of the baseline. In the meantime, the SNR_{1p} represents the ratio between one photo-electron amplitude and its standard deviation.

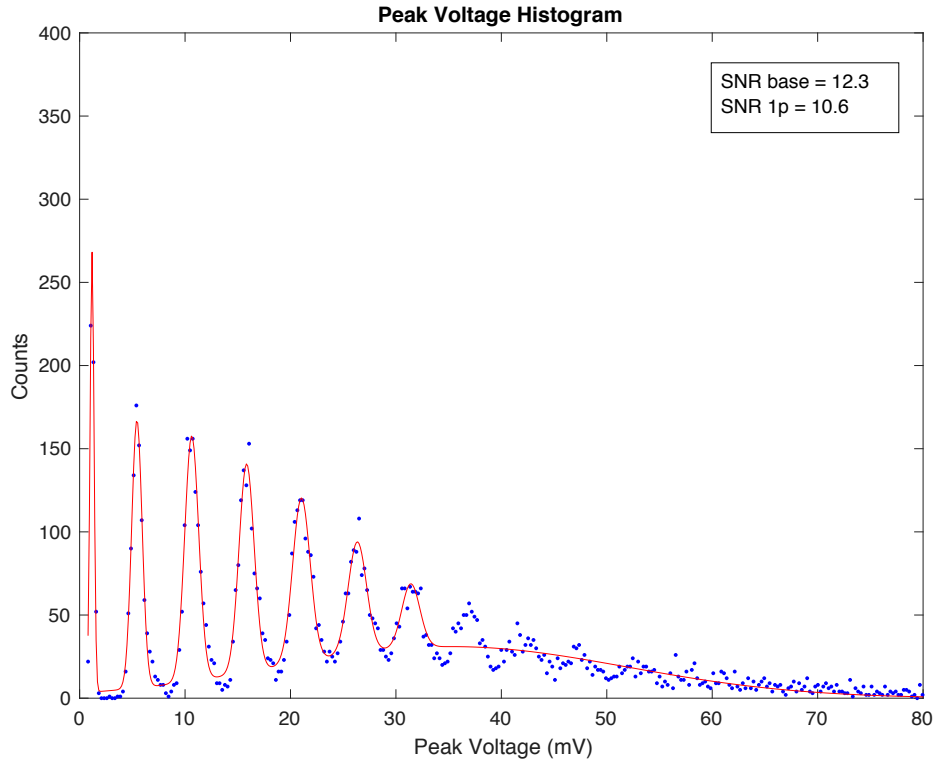

Figure 5.20: Peak voltage histogram of the front-end electronics without filtering.

Integrated electronics initially provide a SNR_{base} equal to 12.3 and a SNR_{1p} equal to 10.6. After trapezoidal pulse-shaper implementation, the FOM was enhanced around 50 % in comparison to the pre-filtering condition. In the post-filtering histogram (Figure 5.21), the gap between the histogram's peaks was further increased, which provides a better resolution for the photon counting. The FOM was improved considerably, as shown the post-filtering parameters SNR_{base} equals to 23 and a SNR_{1p} equal to 15.4.

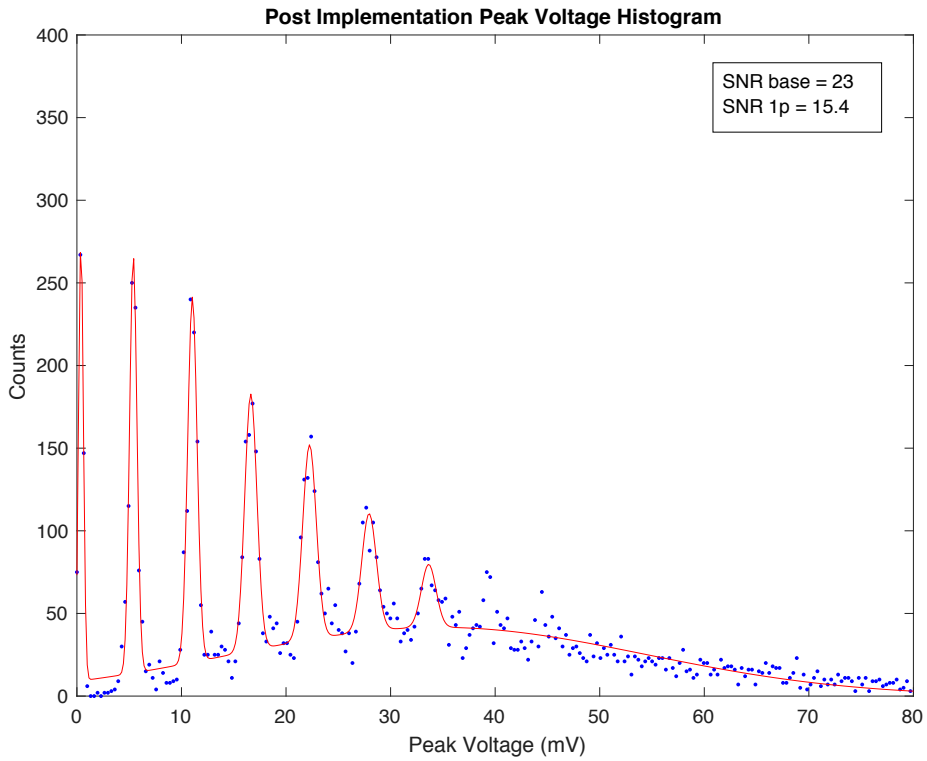

Figure 5.21: Peak voltage histogram after trapezoidal digital filtering.

Chapter 6

Circuit design of cryogenic ASIC v2

CMOS front-end electronics v2 is the second version of DarkSide20K electronics. The new prototype owns an identical architecture of ASIC v1. However, its key parameters, such as dynamic range and SNR. have been further optimized. The new prototype is implemented in a different 110 nm CMOS technology, which has devices with higher threshold voltages. As a consequence, the bias voltage had to be increased from 1.25 V to 1.65 V. The implementation of the ASIC in this particular technology is motivated by the opportunity of incorporating the front-end in a future, larger integrated circuit, whose development is beyond the scope of this thesis. Furthermore, ASIC v2 has integrated a new circuit block to generate a differential output signal. The single-ended to differential converter employs a dedicated power domain, which allows the new IC block to be switched off independently. Two different circuit flavors have been embedded in the same tape-out. One is called ASIC v2 FE 1 and targets a dynamic range higher than 300 PEs with an SNR>8. A second structure (ASIC v2 FE 2) provides a dynamic range of 100 PEs with an enhanced SNR of 12. Both ASIC FE1 and FE2 implements the SiPM electrical model with a bias voltage of 5 VoV to simulate the single PE. The 5 VoV is chosen as the value to guarantee a PDE higher than 50 %.

The two circuit flavours have been designed in view of two kinds of applications. FE 1 is focused on applications with a high number of photo-electron, such as the DarkSide20K VETO detector. The 24 cm^2 SiPM of VETO may detect a maximum of 230 PEs simultaneously. Hence, the front-end electronics should provide an output swing, which allows that number of PE to be processed without saturating. In the meantime, FE 2 is optimized for a low rate photon-counting system, such as a time projection chamber (TPC). In the TPC the PE expected PE range is lower than 1 KHz, but it requires an optimal SNR to guarantee an excellent resolution.

6.1 ASIC v2 architecture and floorplan

One of the key features of ASIC v2 implemented for the readout of 24 cm^2 SiPM DarkSide 20K sensors (Chapter 4.1) is a differential output signal. A differential signalling communication from the cold environments (VETO or TPC detectors) to the warm data acquisition system provides in fact several advantages, because it allows the usage of a simpler and cheaper wire data transfer scheme instead of optical fiber links. Optical fiber is an optimal way to transmit signals between electronic systems. Nevertheless, the response of an optical link might change at low temperatures depending on the protective coating. Hence, the fiber reliability may be affected, causing a serious degradation in the output signal. In fact, an optical attenuation is generated due to axial shrinkage of coating leading to a very significant micro bending loss [80].

ASIC v2 (Figure 6.1) implements a 4-inputs plus a summing voltage architecture, similar to ASIC v1. However, this prototype has adopted a new 110 nm CMOS technology (Tech 1). Internal parameters of new technology transistors were measured and reported in the test structure section (Chapter 3.3). Hence, the transistor sizing of ASIC v2 was performed considering the new process parameters extracted from the new CMOS technology (Tech 1). Furthermore, ASIC v2 differential output signal allows the output baseline to be shifted from 0 V up to $\pm$0.8 V. Baseline variation is carried out by external voltages ($V_{ref_{pos}}$&$V_{ref_{neg}}$) of output stages (Ao1, Ao2). Output stages implement a single-ended folded cascode architecture. Ao1 & Ao2 have been implemented as a non-inverting topology, to maintain an invariant polarity from the fully differential amplifier outputs.

ASIC v2 tape-out includes two front-end electronics designs flavours (FE1 and FE2). Both flavours implement a similar transistor-level design of each internal block (TIA, summing, and converter stage). However, the TIA stage of each version presents different close-loop and Miller compensation components, causing different gain and bandwidth value. For instance, the TIA stage of FE 1 was designed to generate a bandwidth of around 3 MHz. As a result, the feedback components (R_f and C_f) presents a design value of 90 $k\Omega$ and 2 pF respectively. On the other hand, the TIA stage of FE 2 was focused on generating an optimal shaping time to maximize the SNR. In this prototype, the shaping time was chosen around 300 ns from a parametric simulation. Then, this leads to adopt feedback components $R_f = 180k\Omega$ and $C_f = 2pF$). Also, ASIC v2 FE1 (the lowest close-loop gain) presents stronger Miller compensation due to its high sensibility to instability.

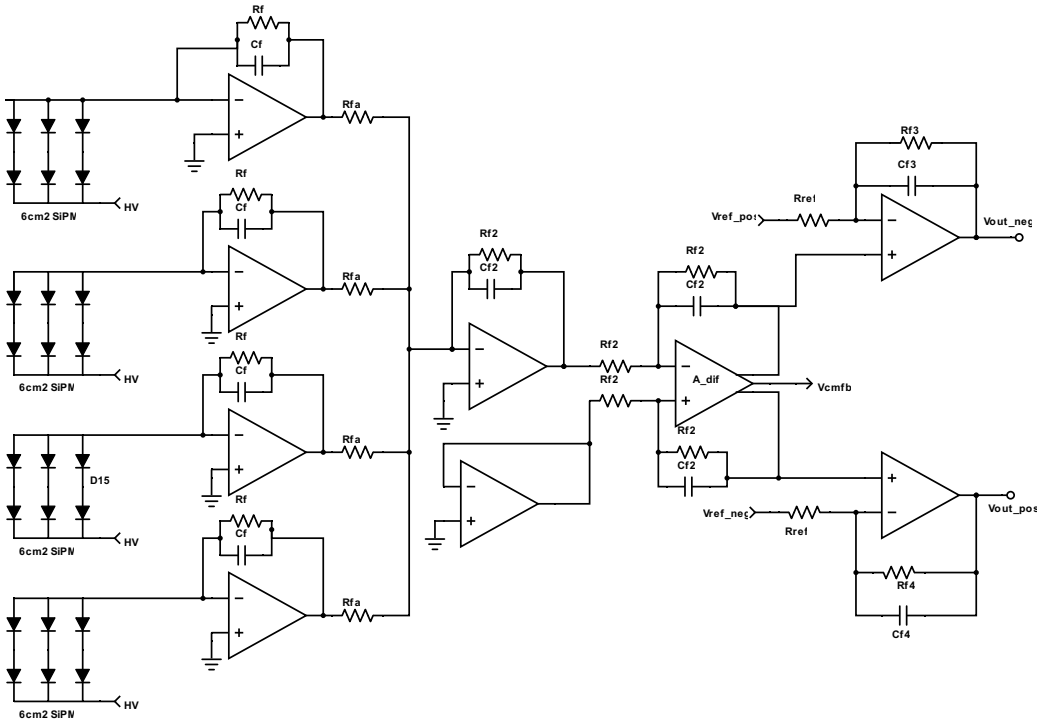

Figure 6.1: Full front-end for the readout of 24 cm^2 SiPM tile with differential outputs.

In summary, the TIA design process concentrates on the key differences between the two integrated circuits which affect the dynamic range, SNR, and rise time. The sizing of the transistors and passive components non affecting those parameters is identical between the two implemented flavours.

6.1.1 Fully differential folded cascode amplifier

In the following, we discuss the transistor-level design of the fully differential amplifier. (A_{dif}) The input stage features a pMOS input transistor connected to a nMOS cascode stage, as highlighted in Figure 6.2. In cryogenic electronics designs, the pMOS input configuration offers better reliability than its nMOS counterpart in terms of robustness to hot carrier degradation effects. Hence, all circuits in this study implement the pMOS input topology. Transistors M3 and M4 work as cascodes and they reduce the voltage drop over transistors M1 and M2, because a large voltage drop significantly increases the hot carrier probability due to the increase of transistor stress.

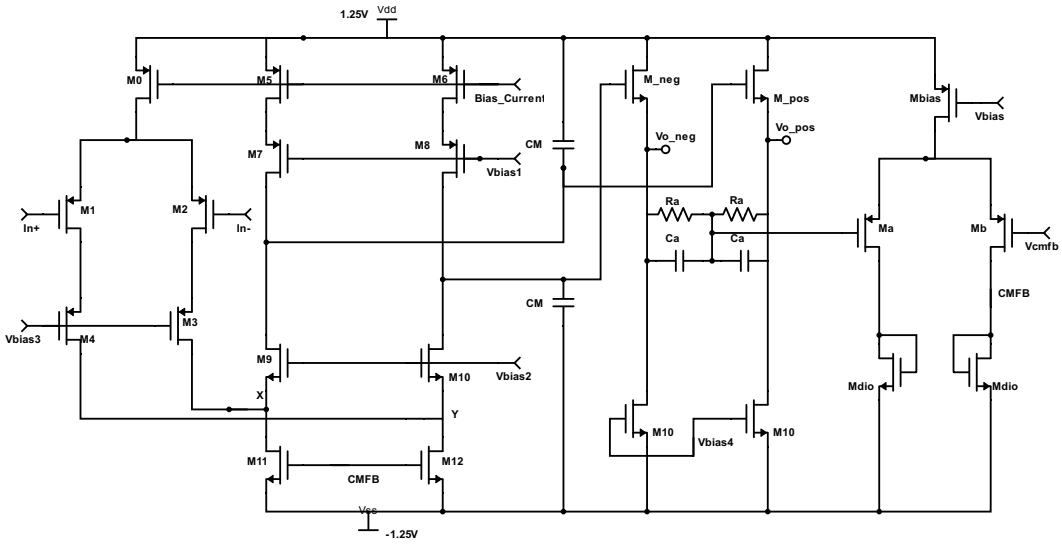

Figure 6.2: Transistor-level circuit of fully differential Folded Cascode with Common mode feedback.

The commom-mode feedback (CMFB) integrates a low gain amplifier, which works as a comparator (M_a, M_b). In this circuit, the CMFB structure regulates the gate voltage of transistors M_{11} and M_{12} to set an output baseline equal to zero (0 V). For instance, if the output common-mode increases more than the desired baseline (V_{cmfb}), the comparator increases the feedback voltage by sinking more current through transistor M_b and the CMFB voltage increases the current of transistors M_{11} and M_{12}. Hence, the output DC voltage in decreased, pushing the output common mode voltage back towards the desired value set by V_{cmfb}. Besides, the control voltage of the CMFB comparator arrives from the voltage divider (R_a), made of two equal resistors. In this case, the control voltage is a medium value between the positive and negative differential output baseline (V_opos and V_oneg). The common-mode reference voltage is filtered through capacitors (C_a).

6.1.2 Transistor-level design sizing

Transistor-level design sizing was performed by applying the Pelgrom equation 3.3.7 to guarantee a minimum offset voltage. Initially, a maximum allowable offset of 0.5 mV and two design techniques to reduce the hot carrier probability were established as a minimum requirement for cryogenic operation. Furthermore, ASIC v2 circuit sizing

has been based on the extracted parameters of the technology (chapter 3.3).

Input transistors (M_1, M_2) work in weak inversion to initially guarantee an identical $\frac{nV_TG_m}{I_d}$ factor at room and cryogenic temperature, as shown Figure 3.16. Furthermore, this operation condition consumes less power than strong inversion, considering a similar trans-conductance. The identical $\frac{nV_TG_m}{I_d}$ factor condition provides a manageable way to modify the trans-conductance through bias current. This step is fundamental to compensate G_m when the circuit changes the operation temperature from 300 K to 77 K. G_m compensation is done by bias current variation, applying the following condition: $I_{ratio} = \frac{n_{300K}V_{T300K}}{n_{77K}V_{T77K}}$.

M1 and M2 sizing is based on the target gain bandwidth (GBW > 100 MHz), which is applied in Equation (6.1) to calculate their minimum aspect ratio. The chosen aspect ratio is substantially larger than the computed one since it guarantees a better capa GBW. Also, the largest transistors area enhances the noise performance, because it strongly suppresses the flicker noise contribution [71]. After the aspect ratio calculation, Equation (6.2) is used to compute the necessary bias current to keep the transistor in weak inversion and provide the desired gain bandwidth.

$$\left(\frac{W}{L}\right)_{1,2} \geq \frac{C_o \times GBW}{2\beta_p V_T e^{\frac{V_{gs}-V_{\mathrm{TH}}}{n\times V_T}}} \geq 1mm/0.4um. \tag{6.1}$$

$$I_{M_{1,2}} = 2n\beta_p \left(\frac{W}{L}\right)_{1,2} V_T^2 e^{\frac{V_{gs}-V_{\mathrm{TH}}}{n\times,V_T}} \Bigg\} \quad \text{Weak Inversion Current} \tag{6.2}$$

Final aspect ratio of M_1 and M_2 was set to $\frac{4000}{0.4}\mu m$. Transistors M_3 and M_4 work in a strong inversion regime, then the aspect ratio of each one is obtained by applying Equation 6.3. The complete transistor sizing of the fully differential amplifier is reported in Table 7 of Appendix II.

$$\left(\frac{W}{L}\right)_{M_{3,4}} \geq \frac{I_{\mathrm{d}M1,M2}}{\beta_p(V_{\mathrm{gs}} - V_{\mathrm{th}})^2} \tag{6.3}$$

with:

- Drain current, $I_{\mathrm{d}(M1,M2)}$ = 500 µA;
- $\beta_p = \frac{\mu_p C_{ox}}{2}$, μ_p carrier mobility of PMOS and C_{ox}, Silicon oxide capacitance;
- V_T, Thermal voltage, 26 mV at 300 K and 6.7 mV at 77 K;
- C_o, Capacitance on the output node;
- n, Slope factor $\frac{C_{ox}-C_{dep}}{C_{ox}}$, C_{dep}, Depletion capacitance;

Mismatch equation (Equation 6.4) was employed assuming a $\Delta\beta = 0$ due to its low effect on total mismatch, even at cryogenic temperature of 77 K [64]. Then, mismatch contributions depend on transistor area (W, L) [72], as described the Equation 6.5. This expression contains the mismatch contribution of transistors where the bias current of the input branch flows. This includes the transistors M_{1-6} and $M_{11,12}$, as illustrates the schematic (Figure 6.2).

$$\sigma^2\left(\frac{\Delta I_d}{I_d}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \left(\frac{g_\mathrm{m}}{i_d}\right)^2 \sigma^2\left(\frac{\Delta V_\mathrm{TH}}{V_\mathrm{TH}}\right)\Bigg\} \quad \text{Mismatch Contribution} \tag{6.4}$$

$$\left.\begin{aligned}\sigma^2(V_\mathrm{off}) = \sigma^2(\Delta V_{\mathrm{TH}M_{1,2}}) + \left(\frac{g_{\mathrm{m}\,M_{3,4}}}{g_{\mathrm{m}\,M_{1,2}}}\right)^2 \sigma^2(\Delta V_{\mathrm{TH}M_{3,4}}) \\ + \left(\frac{g_{\mathrm{m}\,M_{5,6}}}{g_{\mathrm{m}\,M_{1,2}}}\right)^2 \sigma^2(\Delta V_{\mathrm{TH}M_{5,6}}) + \left(\frac{g_{\mathrm{m}\,M_{11,12}}}{g_{\mathrm{m}\,M_{1,2}}}\right)^2 \sigma^2(\Delta V_{\mathrm{TH}M_{11,12}})\end{aligned}\right\} \quad \text{Offset voltage} \tag{6.5}$$

In the mismatch transistor distribution, the transistor-level sizing was focused on concentrating the total mismatch on the input transistors M_1, M_2, M_3, and M_4 due to its large aspect ratio. Then, to satisfy the design criteria, the following requirement must be fulfilled:

$$\sigma^2(\Delta V_{\mathrm{TH}M_{1,2}}) = \left(\frac{\mu_p}{\mu_p}\right)^2 \sigma^2(\Delta V_{\mathrm{TH}M_{3,4}}) \tag{6.6}$$

$$\sigma^2(\Delta V_{\mathrm{TH}M_{1,2}}) > \left(\frac{\mu_p}{\mu_p}\right)^2 \sigma^2(\Delta V_{\mathrm{TH}M_{5,6}}) \tag{6.7}$$

$$\sigma^2(\Delta V_{\mathrm{TH}M_{1,2}}) > \left(\frac{\mu_n}{\mu_p}\right)^2 \sigma^2(\Delta V_{\mathrm{TH}M_{11,12}}) \tag{6.8}$$

Mismatch contribution of each transistor $\sigma^2(\Delta V_{\mathrm{TH}})$ is equivalent to the factor $\frac{A_{\mathrm{TH}}^2}{W \times L}$. This assumption is true if most sources of systematic offset has been eliminated, then the mismatch is mostly dominated by $\frac{A_{\mathrm{TH}}^2}{W \times L}$. In this mathematical statement, the A_{TH} represents a foundry mismatch parameter. $\frac{A_{\mathrm{TH}}^2}{W \times L}$ term is included into the Equation 6.6, 6.7, 6.8. As a result, it is possible to extract the optimal channel lengths for transistors (M_{3-6}), (M_{11}) and (M_{12}) in such a way to fulfill the previous equation conditions.

Solving the previous equations, the optimal channel length for transistors is achieved by applying the following conditions: $L_{3,4} = L_{1,2}$, $L_{5,6} > L_{1,2}$ and $L_{11,12} > \sqrt{\frac{\mu_n}{\mu_p}} \times \frac{A_{\mathrm{TH}n}}{A_{\mathrm{TH}p}} L_{1,2}$. $L_{11,12}$ presents a more complex channel lenght condition because these transistors own a different CMOS topology than input transistors (M_1 and M_2). Then, the optimal channel length must be scaled by the carrier mobility ratio between nMOS and pMOS.

Implementing the previous channel length conditions, we force that offset voltage exclusively depends on input transistors sizing. Hence, input transistors were sized to set the random mismatch lower than maximum allowable offset. In this case, the $\sigma^2(V_{\mathrm{off}}) > \sigma^2(\Delta V_{\mathrm{TH}(M_{1,2})}) + \sigma^2(\Delta V_{\mathrm{TH}(M_{3,4})})$ and $\sigma(V_{\mathrm{off}}) = \frac{V_{\mathrm{off},max}}{3}$. Then, the channel length for the input transistor is determined by the Equation 6.9, 6.10.

$$W_{1,2} > \sqrt{2 \frac{9 A_{\mathrm{TH},p}^2}{V_{\mathrm{off},max}^2} \left(\frac{W}{L}\right)_{1,2}} \tag{6.9}$$

$$L_{1,2} > 2\frac{9A_{\mathrm{TH},p}^2}{W_{1,2}V_{\mathrm{off}\,max}^2} \tag{6.10}$$

$$L_{5,6} > L_{1,2} \tag{6.11}$$

$$L_{11,12} > \sqrt{\frac{\mu_n}{\mu_p}} \times \frac{A_{\mathrm{TH}n}}{A_{\mathrm{TH}p}} L_{1,2} \tag{6.12}$$

M_5 - M_{12} aspect ratio were calculated, with Eq. (6.13), considering an overdrive voltage $V_{\mathrm{OD}} < 150$ mV and a bias current equal to the input transistors. The results of transistor sizing are described in Table **??** of Appendix **??**.

$$\left(\frac{W}{L}\right) \geq \frac{I_{\mathrm{d}M1,M2}}{\beta(V_{\mathrm{gs}} - V_{\mathrm{th}})^2} \tag{6.13}$$

with:

- transistors M_5, M_6, M_7 and M_8, $I_d = 500$ µA and β_p ;
- transistors M_9 and M_{10} ($I_d = 500$ µA), M_{11} and M_{12} ($I_d = 1$ mA) and β_n;

Moreover, transistors (M_{pos} and M_{neg}) implement two source follower circuits, which are necessary to avoid excessive loading on the output signal. M_{pos} and M_{neg} work in strong inversion with a bias current equal to 100 uA. These transistors were sized considering an overdrive voltage lower than 150 mV. This voltage preserves the signal swing of the previous stages. Finally, a voltage divider is built considering two resistors equal to 10 $k\Omega$ to avoid a large voltage attenuation. Additionally, the resistors were designed with a long length (> 100 μm) to reduce the mismatch variation. Otherwise, the voltage divider might not provide a precise partition in its middle point. Capacitors (C_a) present a value of 2 pF, which is large enough to filter the noise generated by the resistors.

6.1.3 Transistor-level design of buffer stages

Non-inverter output stages implement a single-end folded-cascode configuration with a class AB output driver. The driver generates a symmetrical slew rate, as the TIA and the summing amplifier structure explained in chapter 4.3 and shown in Figure 6.3.

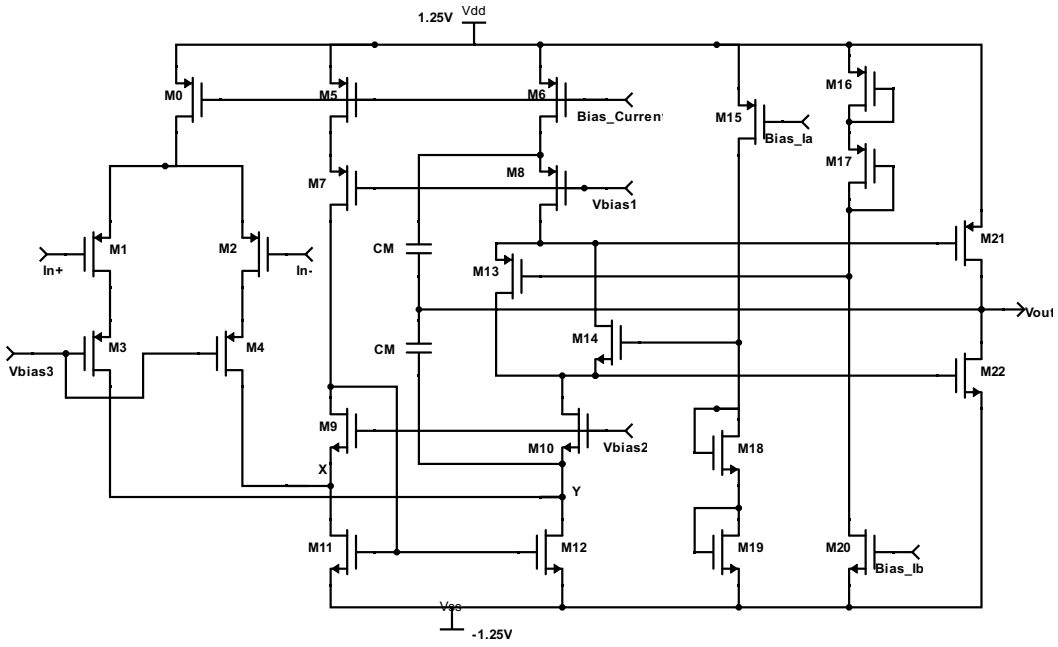

Figure 6.3: Transistor-level circuit of output stage ($Vout_{neg}$ and $Vout_{pos}$).

The core op-amps are used in a non-inverting configurations that provide a closed-loop gain equal to 2. The transistors have been sized to provide a maximum mismatch of 0.5 mV, like for the other stages. Output stages were devised to be able to shift the output baseline. This feature allows the baseline to be set from 0 V to 0.8 V, depending on the application. In the case of exploiting the maximum dynamic range, as in our case, the baseline must be fixed on the top (800 mV) for a negative pulse. As a result, the system will perform an output swing equal to 1.6 V with a fully differential waveform. The transistor-level design was performed by following the same optimization steps realized in the Section 6.1.2. However, the input transistor areas implement a smaller dimension, in such a way to develop a good match to the fully differential output capacitance. The aspect ratio of the transistors are reported in Table 6 of Appendix **??**.

6.1.4 ASIC v2 layout structure

The layout floor-plan allocates ASIC v2 FE 1 and FE 2 on the silicon chip in such a way that both can use the same printed circuit board (PCB). From Figure 6.4, it is just necessary to turn 180° to operate FE 1 or FE 2. Both ASIC v2 FE1 and FE2 occupy an equivalent area. Transistor distribution on the layout follows a couple of design techniques to reduce the systematic mismatch. Otherwise, the experimental mismatch will be much higher than the expected one calculated with the mismatch equations.

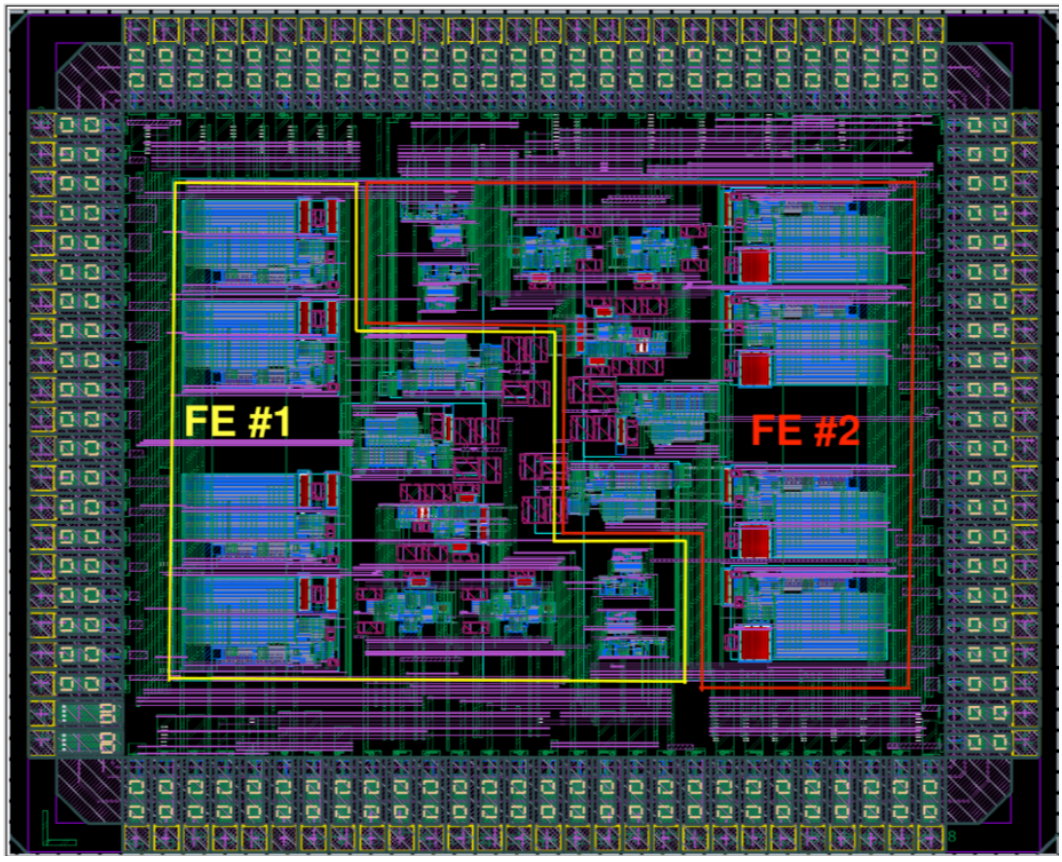

Figure 6.4: Layout structure of ASIC V2, including Front-End 1 and 2

Primarily, transistor pairs were implemented using the interdigitated configuration to reduce the systematic mismatch and keep the parasitic capacitance equal in transistor pairs [72]. Secondly, transistor orientation was fundamental to generate a good match within current mirror transistors. In this case, the mirror transistor orientation must be realized in such a way the DC currents run in parallel, as shown in Figure 6.5. Besides,

transistor were placed close enough to mitigate the differences introduced by the spatial parameter variation. These are caused by stochastic effects related to microscopic fluctuations of device properties.

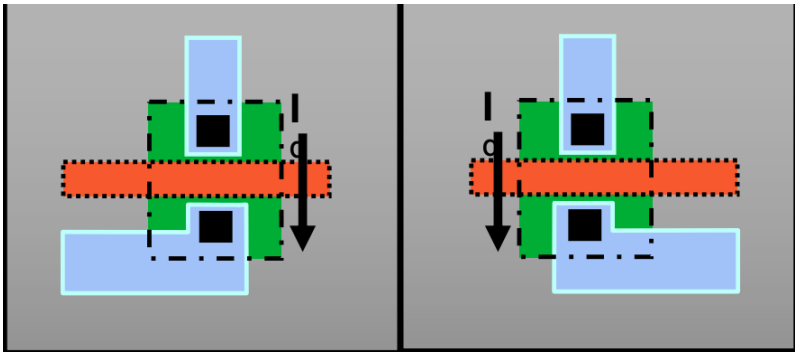

Figure 6.5: Current mirror orientation to generate a good matching.

6.2 ASIC simulation

ASIC v2 post-layout simulations were performed by using a CAD tool with a 110 nm CMOS process design kit (PDK). Post-layout simulations have employed a HSPICE netlist generated from the layout. The netlist includes the parasitic elements (capacitance and resistance) due to the metal interconnection of layout structure (Figure 6.4). Furthermore, CMOS simulations include realistic SiPM performance, which was highly effective within ASIC v1 simulations.For both ASIC v2 FE 1 and FE2, simulations were done to characterize output signals and mismatch results, as described in Table 6.1.

The simulation table contains the most crucial parameters to describe the front-end electronics performance. Table 6.1 results were obtained by simulating a current signal waveform from the SiPM, and a SiPM overvoltage equal to 5 VoV. Besides, the single-ended results were obtained by switching off the differential converter stage, in case a single-end output signal is required for ASIC v2. The simulated value of power consumption at 77 K, as ASIC v1 simulation, is higher than the simulated value at 300 K. However, the experimental result is lower than the room temperature value, in this case, 75 mW. This was explained in Chapter 3.1.3 and demonstrated in the experimental result of ASIC v1.

Parameters	Simulation Single-Ended 77 K FE#1	Simulation Differential 77 K FE#1	Simulation Single-Ended 77 K FE#2	Simulation Differential 77 K FE#2
V1pe (mV)	3.6	5.1	11.7	17.2
Vnoise (mV)	0.51	0.64	1.31	1.8
SNR	7.1	8	8.9	9.5
Jitter (ns)	8.7	13	13.5	17
Dynamic Range (pe)	310	305	100	90
Power (mW)	100	140	100	140
Rising Time (ns)	70	134	143	161

Table 6.1: Simulation results of ASIC v2 FE1 and FE2 at 77 K.

6.2.1 Post-layout simulation for a single PE

Single photo-electron simulation becomes a significant test to analyze the performance of the circuit and its ability to comply with the project requirements. Figure 6.6 illustrates a single-ended signal waveform for both prototypes FE1 and FE2. In this simulation, the differential converter was turned off to obtain the single-ended waveform.

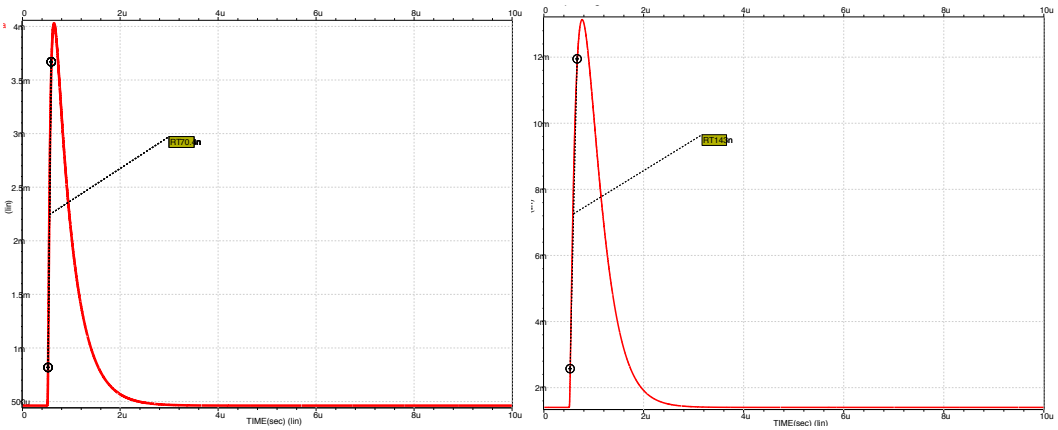

Figure 6.6: Single-ended output waveform of Front-End 1 (left) and Front-End 2(right)

Next, connecting the differential converter stage, it is possible to acquire the differential output signal from FE 1 and FE 2, as shown in Figure 6.7. In this case, the whole ASIC v2 is turned on, and the power consumption in simulation reaches the value of 140 mW. However, experimental power consumption is much lower, as it was demonstrated by ASIC v1 in Table 5.3.

Figure 6.7 illustratively describes the differences between FE 1 and FE 2, in terms of peaking time and signal amplitude. As it was explained in chapter 6.1.1, FE 1 was focused on achieving a much higher dynamic range, as a consequence, the PE amplitude is much smaller than FE 2. In the meantime, FE 2 primary goal was boosting the SNR, as a result, it presents a longer peaking time than FE 1. Peaking time, equal to 280 ns, was chosen as the optimal shaping time to minimize both parallel and series noise contributions.

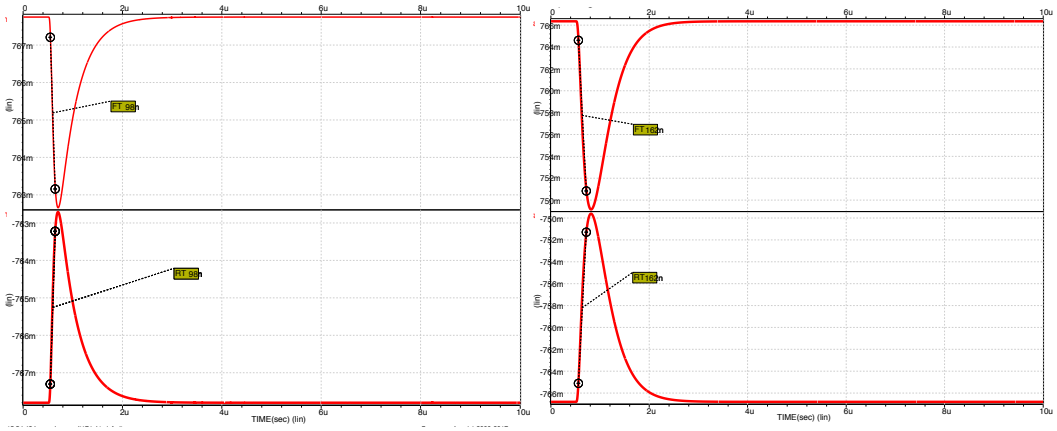

Figure 6.7: Differential output signal of ASIC FE 1 (left) and FE 2 (right) at 77 K

6.2.2 Monte Carlo simulations of ASIC v2

Montecarlo simulation statistically provides the probability of the outcomes, in the CMOS process, due to the effects of random variables. In this random process characterization, 2000 different simulations were run to analyze the variability of each component involved in the system. In this prototype as in ASIC v1 either, Montecarlo simulation becomes a fundamental step in our design because of the mass production purpose for the VETO system. Mismatch analysis of ASIC v2 on both process and mismatch variation has been performed by launching a random mismatch Monte Carlo of 2000 runs at 300 K to analyze how the input offset of IC varies over 2000 samples.

Front-end electronics 1 and 2 perform a similar offset voltage as it is expected despite the equal transistor-level design. Offset voltage achieves a variability around 460 μV rms, as is illustrated by Figure 6.8 at 300 K. The mean offset voltage result provides 740 μV for both FE 1 and FE 2 prototype. As ASIC v1 operates, the pMOS input pairs

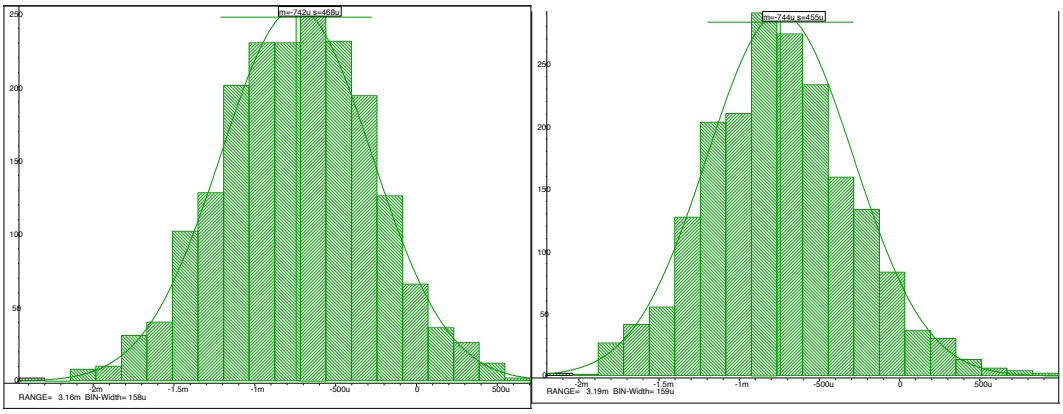

Figure 6.8: Montecarlo simulation of input offset FE 1 (left) and FE 2 (right) at 300 K.

dominate the offset voltage, then the input offset variability presents a narrow increment lower than 5 % roughly at 77 K. Hence, the expected offset voltage ($< 480\ \mu V$) is certainly lower than 500 μV, as from design.

In addition, Monte Carlo simulation was applied within single-ended output baseline. The results provides the information about how much the baseline voltage could be shifted among of 2000 ICs. In this case, single-ended output baseline of FE 2 presents a larger variation in comparison to the FE 1 due to its larger closed-loop gain. Figure 6.9 presents the baseline deviation for both prototypes. From mismatch simulations, FE 1 develops a total variability of 990 μV rms from a signal amplitude of 3.6 mV.

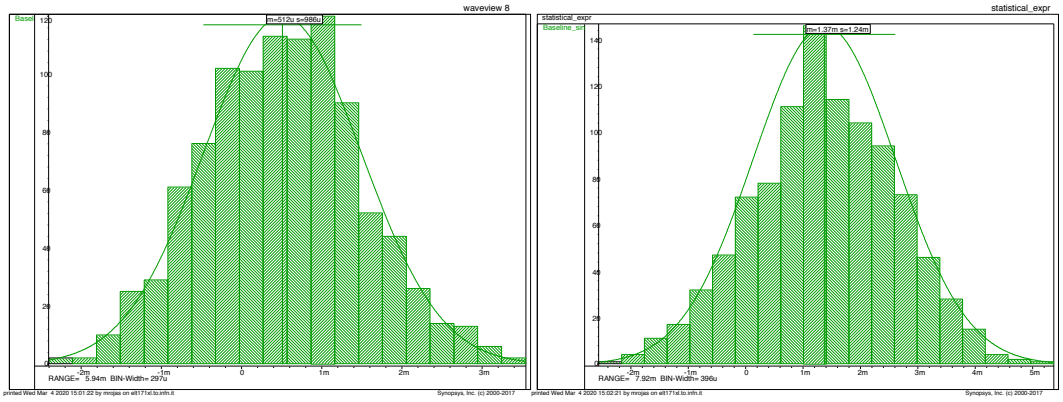

Figure 6.9: MonteCarlo simulation of single-ended output baseline of ASIC FE 1 (left) and FE 2 (right) at 77 K.

In the meantime, FE 2 provides a standard deviation equal to 1.24 mV from an amplitude of 11.7 mV. The mean output baseline is fixed in both cases around -70 μV. Monte Carlo simulation was not applied to the differential output baselines, since these could be shifted externally. Hence, every IC could be set to have a well defined output baseline.

Finally, mismatch and process Monte Carlo simulation also evaluate the amplitude variation of FE 1 and FE 2 within different ICs . Simulation results illustrate a negligible single-ended amplitude variance, as shown the Figure 6.10. In this case, FE 1 performance a V_{1pe_mean}=3.36 mV and a V_{1pe_std}= 3.73 μV and FE 2 presents a V_{1pe_mean}=11.2 μV and a V_{1pe_std}= 14.1 μV. Considering the differential output amplitudes, FE 2 provides a variance of 33.7 μV. This means that assuming 4σ (99.6 % of ICs), the amplitude exhibits a maximum variation of 130 μV from 16.4 mV. In other words, the mismatch and process variation does not affect the gain of integrated electronics.

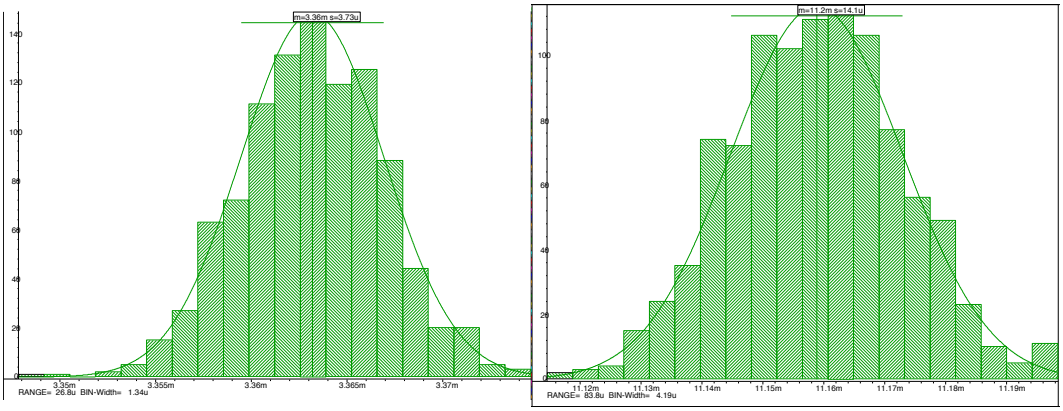

Figure 6.10: MC single ended amplitude of Front-End 1 (left) and Front-End 2 (right) at 77 K.

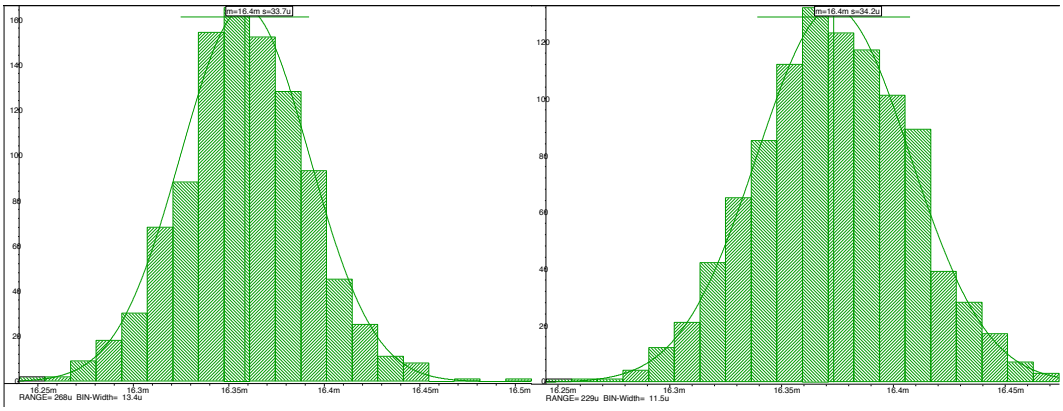

Figure 6.11: Montecarlo simulation of differential output signal of Front-End 1(left) and Front-End 2 (right) at 77 K

6.3 Experimental results of ASIC V2 - Front-end 2

Cryogenic ASIC v2 was the last submitted integrated circuit to read out a large area of SiPM. Initially, the integrated circuit, designed with a different 110 nm technology in comparison to ASIC v1, has been characterized using a charge injection board. The injection board was designed with the equivalent components of 24cm^2 SiPM. Besides, the board is divided into 4-channels, which represents the 4-quadrants of SiPM. The cryogenic tests are performed using the Liquid Nitrogen element due to its closeness to LAr temperature under normal atmospheric pressure.

The current ASIC v2 cryogenic setup does not demand a light isolation environment to obtain optimal experimental results, as we are not including the SiPM sensor in these initial experimental tests. In this case, we can only implement an equivalent electrical circuit to generate the typical SiPM pulse signal. The injection charge board provides 4-outputs for each input channel of ASIC v2. The initial setup, which includes the ASIC v2, PCB, and the injection charge board, is illustrated in Figuree 6.12.

The initial experimental results of ASIC v2 are described in Figure 6.13. The figure illustrates the differential output signal applying an input charge equivalent to 30 PEs, through the injection charge board. The differential waveform allows the first inconvenient of ASIC v2 to be observed. The positive pulse presents a limited baseline to 200 mV. Shortly it will be explained in detail.

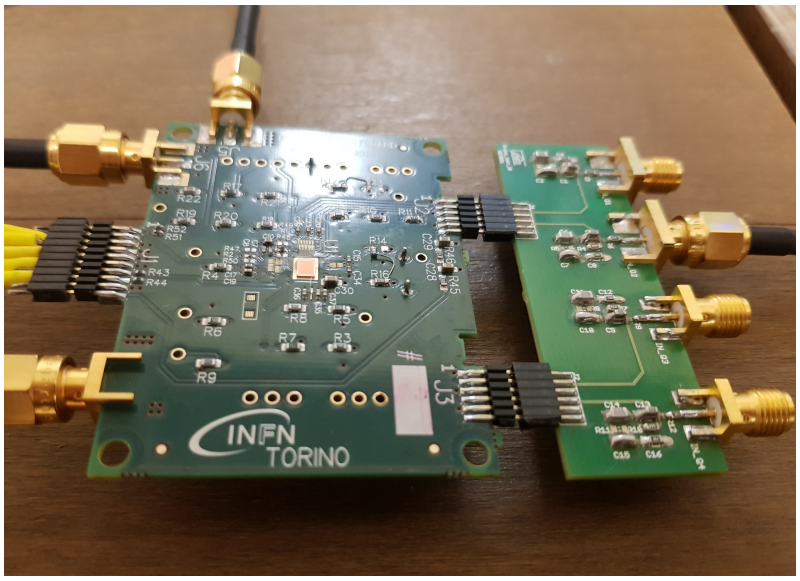

Figure 6.12: Integrated circuit ASIC V2 and the charge injection board.

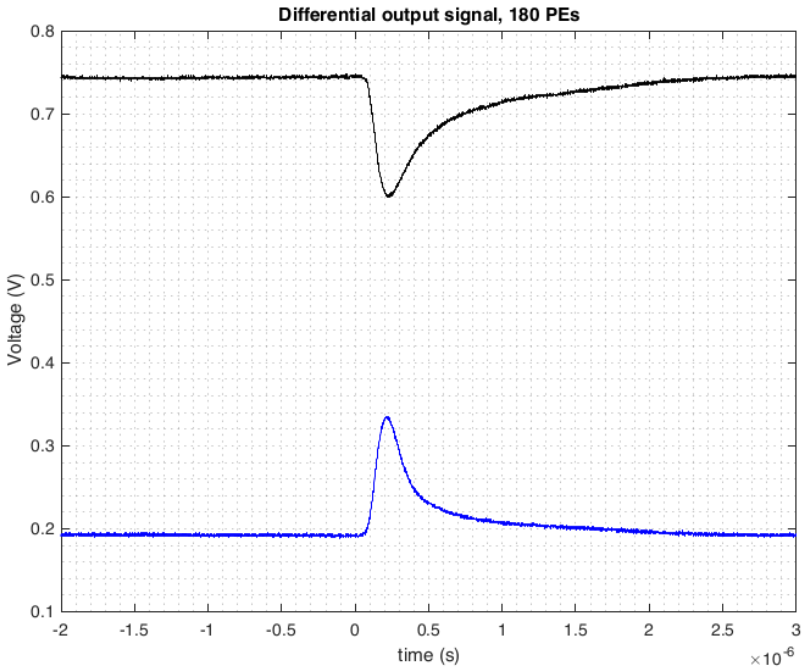

Figure 6.13: Differential output signal using the charge injection board with equivalent charge of 30 PEs at 77 K.

6.3.1 Key parameters of the front-end electronics

This section discusses the experimental results of ASIC v2 FE2 using the charge injection board. The delays due to the pandemic outburst of 2020 did not give enough time to perform extensive cryogenic testing with both ASIC v2 FE1 AND FE2. Furthermore, cryogenic testing with the SiPM demands to transfer the electronics to an external laboratory. In this case, a complete setup is found at INFN Genova Section.

The most important parameters, such as single PE amplitude, RMS noise, signal-to-noise ratio, rising time, and dynamic range of ASIC v2 are described in this section. The key parameters, such as SNR, rising time and dynamic range allow us to figure out how this new 110 nm technology behaves at 77 K in comparison with ASIC v1 technology. Hence, each key parameter will be compared to ASIC v1 performance. In this case, the ASIC v1 results used in the comparison were acquired employing the charge injection board as the input structure.

6.3.2 RMS noise

RMS noise is a fundamental parameter in all ICs since this value means how much the undesired signal (random) overlaps the desired signal. Besides, the RMS noise allows the SNR and the timing jitter to be measured. The RMS noise was measured by computing the standard deviation baseline over time. Figure 6.14 (right) illustrates the RMS noise distribution by fixing an average value of around 300 μV for the single-ended stage. Figure 6.14 (left) represents the RMS distribution of ASIC v1 of 0.4919 mV at 77 K. In this case, this is not a comparison about RMS noise behaviors due to the different DC gains, but only a description of the noise level in each structure.

Moreover, Figure 6.15 describes the RMS noise distribution of the whole electronics chain. In other words, it considers the RMS noise on the differential output signal. The distribution presents an average value of 340 μV.

Finally, a frequency spectrum was acquired in order to analyze the noise behavior over frequency. Figure 6.16 illustrates the Fast Fourier Transform applied to both single-ended and differential output baseline.

There are two important aspects of the frequency spectra. Firstly, the differential signal develops a lower bandwidth in comparison to the single-end signal, causing a rising time increment, as described in section 6.3.4. Furthermore, the low-frequency gain of the differential stage is around 9 dB higher than the single-ended frequency spectrum. It matches with DC gain of the differential converter equal to 3.

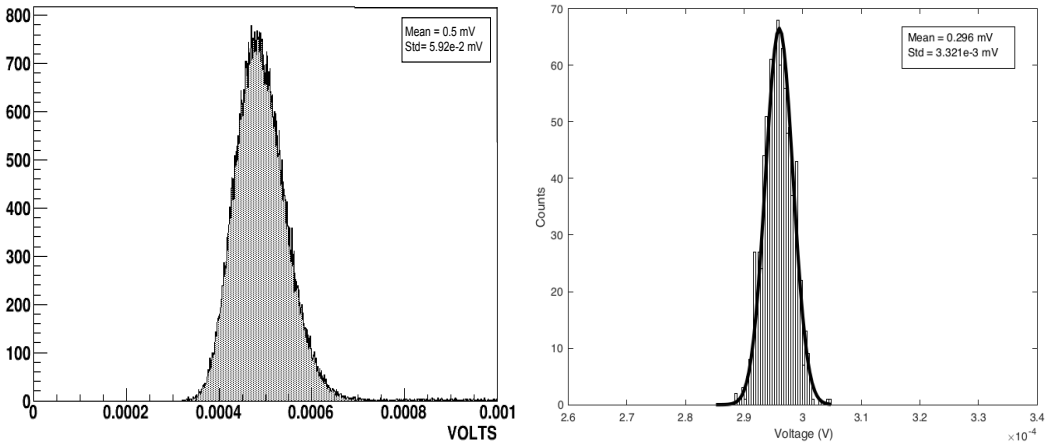

Figure 6.14: Experimental RMS noise distribution of ASIC V1 structure (left) and ASIC V2 (right) at 77 K.

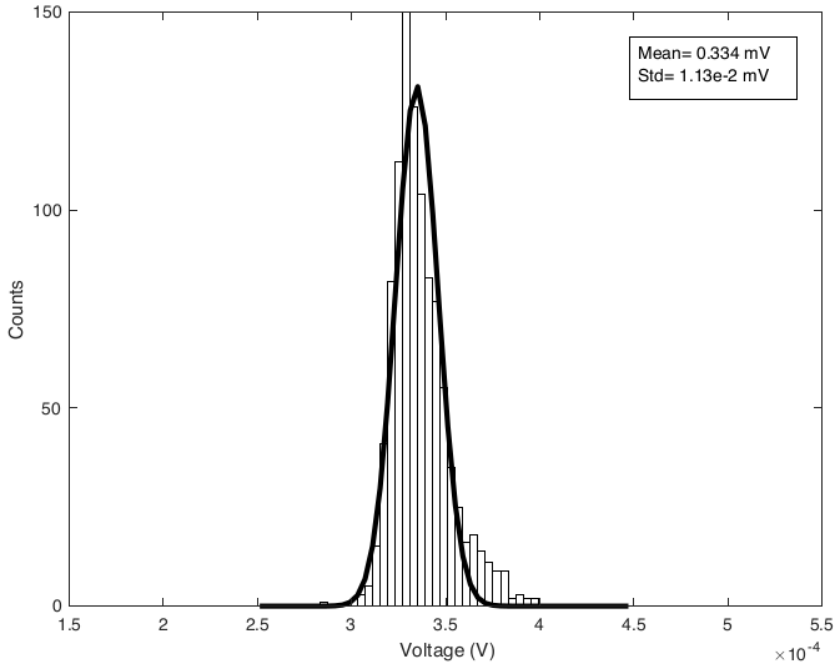

Figure 6.15: Experimental RMS noise distribution from differential output of ASIC v2 at Liquid Nitrogen temperature.

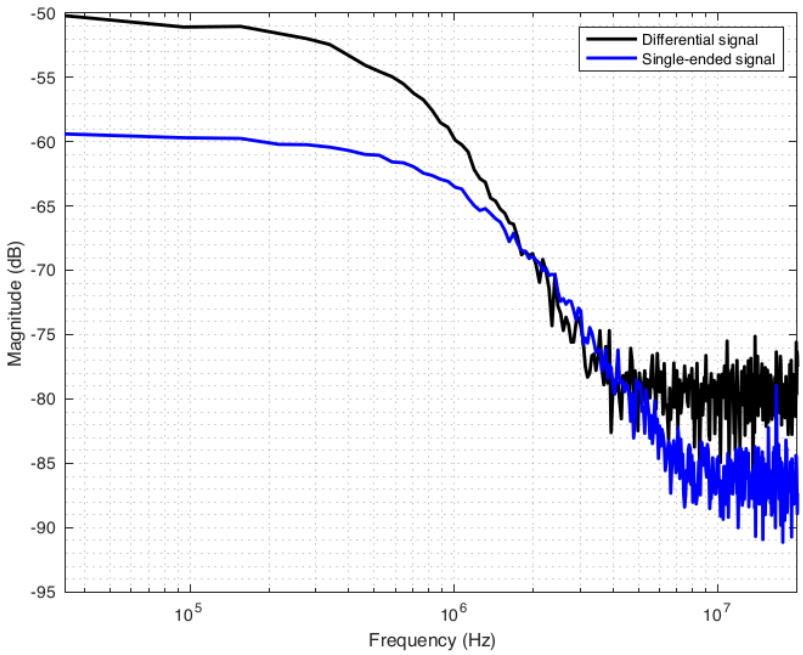

Figure 6.16: Frequency spectrum of single-ended and differential output at 77 K.

6.3.3 Signal to noise ratio

SNR is the most important parameter in this study since it determines how readable the single PE could be on the output port. Theoretically, it is the ratio between the amplitude of single PE and the RMS noise. In chapter 4, the SNR was represented by two terms. One was the SNR_{rms}, and a second was SNR_{peak}. However, this section only considers the SNR_{rms}, since we are not using the SiPM sensor, then we cannot appreciate the sensor effect in the SNR results.

The cryogenic ASIC v2 exhibits a discrete results in terms of SNR using the charge injection board, in this case, simulating the charge of 5 V of overvoltage. The FoM presents a value of 7.7 for the single-ended structure. The value increases around 15 % for the differential output, achieving an SNR of 8.8. The SNR value can be modified depending on the experiment requirements. For instance, the SNR could achieve a value of 10 by applying an overvoltage equal to 7 V. However, it would reduce the dynamic range, as the PE amplitude increases as well. Sensor operation over 7 VoV could increase afterpulsing (AP) and direct crosstalk (DiCT) probability to an undesirable value, more than the critical value of 40 %.

6.3.4 Rising time

Rising time and dynamic range are important parameters, which demonstrates how fast the electronics systems are. Furthermore, it describes how many PEs the ASIC can readout simultaneously without saturating the output signal.

Primarily the rising-edge is determined by measuring the time between 10% and 90 % of the output signal amplitude. The characterization tests of ASIC v2 provides a rising time value of 50 ns for the single-ended structure as it can be appreciated by Figure 6.17 (right) . It is much lower than the ASIC v1 performs a rising time of 90 ns using the injection board. However, the leading edge becomes quite longer in the differential outputs. The final rising time is established around 80 ns, as shown in Figure 6.18 respectively. These figures illustrate the typical output signal of SiPM readout. Moreover, it can be inferred from the rising-edge of ASIC v1 that it develops a rough bandwidth of 3-4 MHz. It is smaller in comparison to the ASIC v2, which is set around 7 MHz.

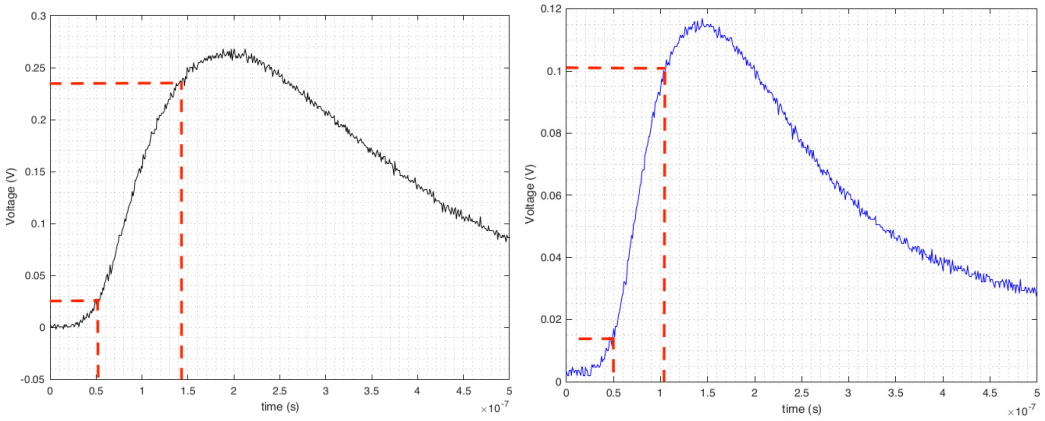

Figure 6.17: Single-ended rising time of ASIC v1 (left) and ASIC v2 (right).

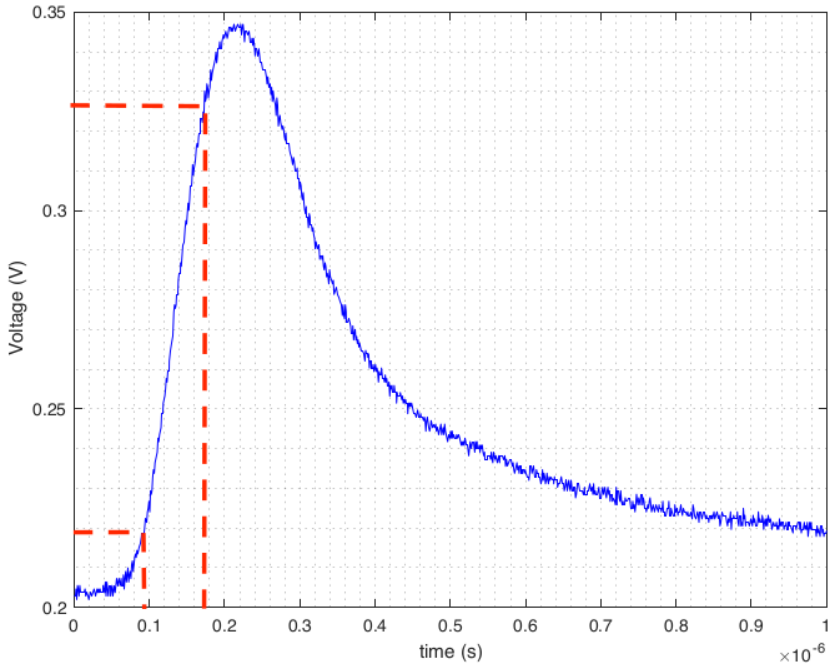

Figure 6.18: Rising-edge time of ASIC v2 differential signal.

6.3.5 Dynamic range

The dynamic range is defined as the number of PEs that an amplifier can process without saturating the signal. The second prototype, ASIC v2 with a new 110 nm technology, has not demonstrated optimal results in terms of dynamic range, because the output swing has been reduced considerably at 77 K, as shown Figure 6.19.

Here, the output swing changes from 1 V at 300 K to 200 mV at 77 K unexpectedly. The differential stage also presents an output swing reduction due to, probably, the reduction of the common-mode range. The common-mode range limitation restricts the output signal to be between 0.2 and 0.8 V, as shown in Figure 6.19. This is an unfortunate drawback of this 110 nm technology, considering a power rail between -1.65 V and 1.65 V. Thus, considering a SiPM overvoltage of 5 V, the differential signal of ASIC v2 can readout around 180-200 PEs. However, the dynamic range is reduced as SiPM overvoltage increases.

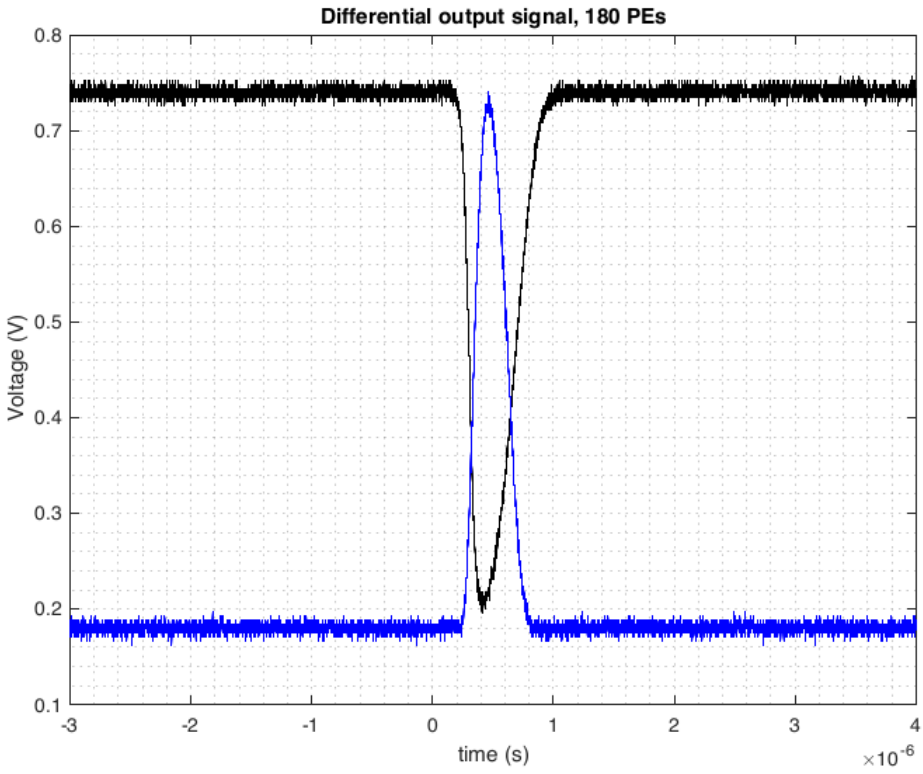

Figure 6.19: Differential output signal with the maximum number of PE on the input before saturation. This waveform provides the information about the dynamic range, in this case 184 PEs.

A second disadvantage of a common-mode range reduction is the loss of DC gain. It causes that the single PE amplitude becomes much smaller than it is expected. To measure the DC gain reduction, both ASIC v1 and v2 implement the charge injection board at the same input charge, which allows the output signal waveform of circuits to be compared. The epxerimental output signal are described in Figure 6.20, and clearly shows the DC gain loss in the ASIC v2. The key parameters of front-end electronics are detalied in Table 6.2, which contains both data of ASIC v1 and ASIC v2.

The experimental results show how the ASIC v2 is substantially faster than ASIC v1, considering a difference in signal-to-noise ratio. However, the dynamic range of ASIC v2 is reduced considerably in comparison to the expected value. The reduction is around 60-70 %. Overall, the single-ended signal remains at 87 PEs in respect to the expected 300 PEs. The differential output exposes a dynamic range equal to 184 PEs

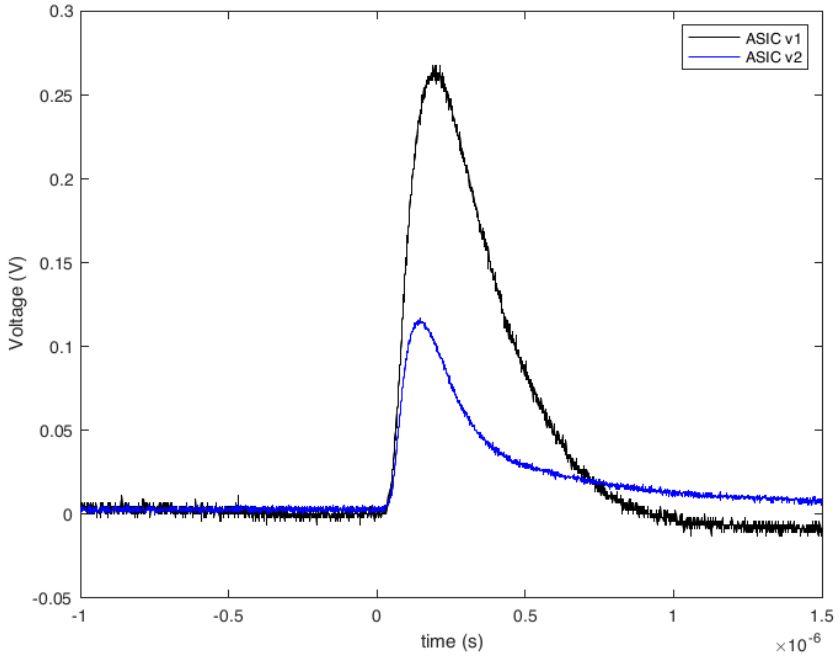

Figure 6.20: Single-ended output signal of ASIC v1 and ASIC v2 at 77 K.

	ASIC v1	ASIC v2 single-ended	ASIC v2 differential
Vout (mV)	260	120	155
Noise (mV)	0.49	0.3	0.34
SNR	473	400	441
Rising time (ns)	150	50	80
Peaking time (ns)	260	90	160
V1pe (mV)	4.46	2.3	3
SNR 1pe	9.1	7.7	8.8
Dynamic Range (PE)	180	87	184

Table 6.2: Key parameters of ASIC v1 and ASIC v2 implementing the charge injection board with the same input charge from Liquid Nitrogen tests. The single PE parameters are extrapolated from the ASIC v1 results at 5 VoV.

by forcing the output signal through Vref, otherwise, the positive output pulse remains off. Besides, the dynamic range assumes an overvoltage equal to 5 V.

6.3.6 DC gain and output swing issues

A hypothesis of the DC gain reduction might be due to, primarily, the unknown and considerable increment of threshold voltage in non-extracted parameter transistors, because the parameter extraction, such as threshold voltage in Chapter 2, were just developed in the 1.2 V transistor. However, we also employed 3.3 V transistors in ASIC v2. Structurally the 3.3 V transistors are different than 1.2 V in terms of the threshold voltage, for instance, the 3.3 V threshold voltage is 200 mV larger than the 1.2 V transistor, increasing the probability to put the transistor in the linear region at cryogenic temperatures. As a consequence, ASIC v2 would provide a reduced DC gain. A second example, to reaffirm the hypothesis, was the improvement of DC gain when a higher DC supply was applied to ASIC v2. Initially, the DC supply was $\pm$1.25 V providing an ultra-low DC gain, 20 mV, instead of the expected 180 mV. Then, increasing the DC supply up to $\pm$1.65 V, the output signal achieves 120 mV instead of 180 mV. The DC supply cannot be rose more than this. Otherwise, the power consumption becomes enormous, and the circuit could not work properly, since it is moving away from its DC operating point.

Secondly, the IR drop on the metal interconnects increases the probability that the transistors operate in the linear region because it reduces the total common-mode range. In this case, a current of 55 mA and 80 mA flows through VDD/VCC equal to 1.25 V and 1.65 V respectively. Besides, the 4-metal technology increases the probability of a considerable IR drop, since its resistance is higher than the 8-metal CMOS technology of ASIC v1.

Extracting the metal interconnection resistance and DC power supply cabling, each TIA block of the ASIC v2 receives an effective voltage of 1.18 V - 1.14 V, losing between 140-220 mV for the whole range (2.5 V), as shown Figure 6.21. The IR drop increases the hypothesis of a common-mode range reduction causing a DC gain loss. Increasing the VDD and VCC to 1.65 V, the DC current through metal interconnection increases. The IR drop in the whole DC range is 234mV - 327 mV, remaining an effective VDD around 1.5 V. At this voltage level, the circuit presents a better DC gain than using a DC power supply of 1.25 V, but the circuit sinks much more current than this was designed, causing a non desired operation.

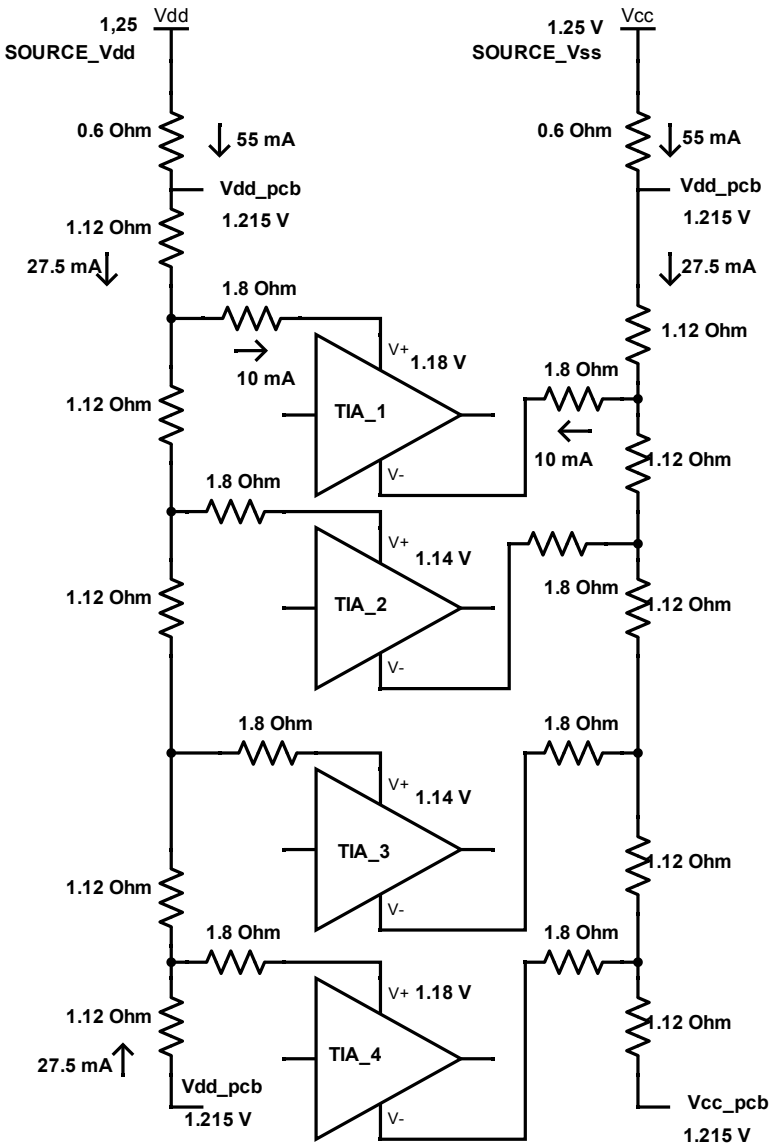

Figure 6.21: Schematic of the IR drop over the power supply interconnection applying a Vdd=1.25 V. The metal resistances were computed from the layout structure.

On the other hand, the output swing range reduction may be related to a large mismatch of common-mode feedback. The common-mode circuit presents an unbalance DC compensation in the differential outputs node ($V_o neg$ and $V_o pos$), which can cause the limitation of the positive pulse baseline (Figure 6.19). The previous nodes present

a baseline equal to 50 mV and -350 mV respectively. The differential outputs are connected to output buffers with a gain equal to 3. The output buffer with a negative baseline remains off since the input offset (-350 mV) is multiplied by 3. Then, in order to turn on the negative buffer, the circuit stage must be forced externally by (V_{ref}pos) of Figure 6.1. The external voltage can compensate for the negative offset partially. As a result, the output buffer stage works with a baseline located at 200 mV instead of -750/-800 mV, as shown in Figure 6.19.

A possible solution for the DC gain loss is to first size the metal interconnection much larger to guarantee a low IR drop. Secondly, the transistor-level design must implement 1.2 V transistors since 3.3 V develops a large threshold voltage, which is highly critical for cryogenic operation.

On the other hand, modifying the common-mode feedback may solve the output swing problem. A new architecture, which allows the common-mode to be compensated externally by an injection charge, must be implemented. In this way, the common-mode could be tuned externally at cryogenic temperature. Another solution may be to change the folded cascode architecture for the fully differential amplifier. In this case, a balanced topology, as a fully differential telescopic, could be an ideal and simple solution for cryogenic operation.

Conclusion

This thesis has studied the development of a cryogenic integrated circuit to readout large areas sensor, such as SiPM, in underground astroparticle experiments. The electronics design in this study completes the cryogenic photodetection system in the astroparticle experiment, enhancing the detection and processing efficiency in comparison to the current neutrino and dark matter experiments. These experiments implement the pre-amplification stage outside the low-temperature area, then the front-electronics is usually placed at room temperature, as described in Chapter 2.1.

The ASIC v1 developed an excellent performance in terms of signal-to-noise ratio, providing a value equal to 10.4 applying a sensor over-voltage of 7 V, as described the Table 5.1. The SNR results from a total front-end RMS noise of 0.59 V. Furthermore, the ASIC v1 presents a range of photo-electron readout between 130 and 220 PEs. The dynamic range is a key parameter in the application, such as VETO, because each photodetection module (24 cm^2) waits for around 200 PEs, as the highest arrival rate during its operation. Then, the ASIC v1 covers the dynamic range requirement by the VETO structure of DarkSide-20K. The cryogenic electronics develops a rising time around 150 ns, as shown in Figure . The timing remains inside the range of maximum allowable rising time (140-160 ns) to avoid a pile-up effect in the output signal.

The ASIC v2 develops a good SNR with an injection charge similar to the generated charge by the SiPM at 5 V. The SNR presents a value of 7.7 and 8.8 for single-ended and differential signals respectively. The SNR could be enhanced further by increasing the sensor bias up to 7 V. The ASIC v2 has not been tested with the 24 cm^2 SiPM yet, but it will be the next step in the experimental test. Furthermore, the new front-end presents an excellent rising time, guaranteeing a fast signal. However, it has accomplished a limited dynamic range, with a maximum PE readout equal to 184 PEs, as shown in Table 6.2. It is substantially lower than the expected 300 PEs. Thus, the dynamic range

reduction may be related to the unbalanced baseline voltage regulation by the common-mode feedback circuit (CMFB) and the unknown threshold voltage increment into the 3.3 V transistors. The CMFB's outputs present a baseline at 0 V and -350 mV, causing limitation on the negative side, as shown in Figure 6.19. The future steps of ASIC v2 are to modify the CMFB circuit to guarantee excellent compensation and implement 1.2 V transistors in the whole structure.

Finally, digital signal processing (DPS) may be the last stage of a full electronics readout chain, since the DPS structure allows the experiment data to be enhanced in terms of RMS noise, data conversion, and reduction into the desired output format. In this study, the DSP structure can improve the figure-of-merit of the ASIC v1 further than 50 %. The peak SNR increases from 10.6 to 15.4 in the post-implementation timing simulation. The SNR increment is an excellent result as the first DSP prototype.

The cryogenic integrated circuit and the digital signal processing become the baseline of a full readout system (pre-amplification, digitization, and data processing) in future large-area sensor experiments. Furthermore, it allows the photodetection and processing system to be bonded on the sensor directly, reducing the long and parasitic connection, as happens with the discrete electronics currently.

Finally, the ASIC v1 has been chosen as the electronics baseline for the VETO structure in the DarkSide-20K experiments, since it fulfills the most critical requirements, such as SNR, rising time, and dynamic range. Furthermore, this electronics system could be an excellent readout system for the next-generation dark-matter and neutrino experiments. Overall the astroparticle experiment with large-area SiPM photosensors for light detection. On the other hand, digital signal processing (DSP) provides the option to generate a complete readout electronics chain, including pre-amplification, digitization, and DSP in future and ambitious plans.

Appendix I

Aspect Ratio of the TIA amplifier - ASIC v1

Transistor	Aspect Ratio		Value
	W (μm)	L (μm)	
M0	250	3	
M1,M2	12000	0.4	
M3, M4	1000	0.4	
M5, M6	200	3	
M7, M8	200	0.26	
M9, M10	200	1	
M11, M12	200	10	
M13	150	2	
M14	50	2	
M15	12.5	0.5	
M16	60	2	
M17	120	2	
M18	40	2	
M19	20	2	
M20	20	0.5	
M21	600	2	
M22	200	2	
R_{s0}	5	5.3	125 Ω- 2 parallel
R_s	5	5.3	250 Ω
C_M	70	60	4 pF - 2 parallel

Table 3: Transistor characterization of Folded Cascode for TIA

Aspect Ratio of the summing voltage amplifier

Transistor	Aspect Ratio		Value
	W (μm)	L (μm)	
M0	250	3	
M1,M2	12000	0.4	
M3, M4	1000	0.4	
M5, M6	200	3	
M7, M8	200	0.26	
M9, M10	200	1	
M11, M12	200	10	
M13	150	2	
M14	50	2	
M15	12.5	0.5	
M16	60	2	
M17	120	2	
M18	40	2	
M19	20	2	
M20	20	0.5	
M21	600	2	
M22	200	2	

Table 4: Transistor characterization of Folded Cascode for TIA

Appendix II

Aspect Ratio of the TIA amplifier - ASIC v2

Transistor	Aspect Ratio		Value
	W (μm)	L (μm)	
M0	500	3	
M1,M2	32000	0.4	
M3, M4	1000	0.4	
M5, M6	250	3	
M7, M8	200	0.26	
M9, M10	200	2	
M11, M12	720	5	
M13	150	1	
M14	50	1	
M15	12.5	0.5	
M16	120	2	
M17	240	2	
M18	40	2	
M19	20	2	
M20	20	0.5	
M21	900	1	
M22	300	1	
R_{s0}	5	5.3	125 Ω- 2 parallel
R_s	5	5.3	250 Ω
C_M	70	60	4 pF - 2 parallel

Table 5: Transistor characterization of Folded Cascode for TIA

Aspect Ratio of the summing voltage amplifier - ASIC v2

Transistor	Aspect Ratio		Value
	W (μm)	L (μm)	
M0	200	3	
M1,M2	2000	0.4	
M3, M4	1000	0.4	
M5, M6	200	3	
M7, M8	200	0.26	
M9, M10	200	2	
M11, M12	720	5	
M13	150	1	
M14	50	1	
M15	12.5	0.5	
M16	120	2	
M17	240	2	
M18	40	2	
M19	40	2	
M20	20	0.5	
M21	750	1	
M22	250	1	
R_{s0}	5	5.3	250 Ω
R_s	5	5.3	250 Ω
C_M	70	60	4 pF - 2 parallel

Table 6: Transistor characterization of Folded Cascode of summing amplifier ASIC v2

Aspect Ratio of the fully differential amplifier - ASIC v2

Transistor	Aspect Ratio		Value
	W (μm)	L (μm)	
M0	300	3	
M1,M2	420	0.4	
M3, M4	200	0.4	
M5, M6	150	3	
M7, M8	80	0.4	
M9, M10	200	2	
M11, M12	50	5	
M_{neg}	300	1	
M_{pos}	300	1	
M10	60	1	
M_{bias}	120	2	
M_a	240	2	
M_b	40	2	
M_{dio}	40	2	
R_a	4	41	10 kΩ- 4 series
C_a	22.5	22.5	0.5 pF
C_M	44.5	70	3 pF - 2 parallel

Table 7: Transistor characterization of Folded Cascode for TIA

Aspect Ratio of the converter output stages - ASIC v2

Transistor	Aspect Ratio		Value
	W (μm)	L (μm)	
M0	200	3	
M1,M2	420	0.4	
M3, M4	200	0.4	
M5, M6	100	3	
M7, M8	80	0.26	
M9, M10	200	2	
M11, M12	50	5	
M13	150	1	
M14	50	1	
M15	12.5	0.5	
M16	120	2	
M17	240	2	
M18	40	2	
M19	40	2	
M20	20	0.5	
M21	1200	1	
M22	400	1	
R_{s0}	5	5	112 Ω- 2 parallel
R_s	5	5	224 Ω
C_M	29.5	60	2 pF

Table 8: Transistor characterization of Folded Cascode for TIA

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