Limit-cycle free digitally controlled power converter

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Control of switch-mode power converters is nowadays preferably performed digitally due to more advantages, but digitally controlled converters could cause steady-state limit-cycle oscillations (LCOs) due to inherent quantization effect of analog to digital converter (ADC) and digital pulse width modulator (DPWM), that are a major concern. The mitigation of these problems has been a topic of extensive research and design guidelines for LCO-free operation have been formulated, i.e., the resolution of DPWM should be higher than that of ADC [1], (i.e., $NDPWM > NADC$). Meeting above guideline, unfortunately, results either in a limited DC accuracy and/or in increased cost and complexity especially for converters operating at high switching frequency (MHz range).

In this proposed work, an innovative technique intended to increase the resolution of the DPWM for LCO-free operation is analysed and experimentally evaluated. More precisely, the novel Dyadic Digital PWM (DDPWM) is adopted as a systematic approach to achieve accurate LCO-free operation in a digital control converter at negligible cost by effectively increasing the resolution of DPWM [2].

A DC-DC Boost converter is considered to validate the approach proposed in the work. The converter is operated efficiently over a range of the input voltages in continuous-conduction-mode (CCM) and supply a constant current to the external load. The voltage mode (VM) digital PID control algorithm is considered. The block diagram is shown in Fig.1. The design specifications are listed in Table 1.

Referring to the HDL implementation of the digital controller (i.e., PID compensator and DDPWM controller), the obtained values of K_p, K_i and K_d are scaled and quantized for $N_{ADC} = 4\ bits\ and\ N_{DPWM} = 8\ bit$. The value obtained from PID compensator is separated in $N = 4$ MSB's given to DPWM and $M = 4$ LSB's given to DDPM as shown in figure 2. The DDPWM output, which architecture is shown in Fig.2, is a square wave signal whose duty cycle is modulated between two adjacent quantized levels is then used to drive switches of the boost converter. Simulation tools, i.e., Simulink and Modelsim are used for the simulation of boost converter and digital controller, respectively.

It is shown in Fig.3 that, in case of only-DPWM there is low frequency limit-cycle oscillations at the output voltage v_o, The $4\text{-}bit$ duty cycle is not constant since controller is not able to drive error to zero-error bin [3]. While in case of DDPWM (see Fig.4), there is no limit-cycles oscillations at output voltage. The $8\text{-}bit$ duty-cycle is constant since controller is now able to drive output to zero-error bin.

More details and results will be given in the oral presentation.

References

[1] A.V.Peterchev, S.R. Sanders, "Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters", IEEE Transactions on Power Electronics, Vol. 8, No. 1, pp. 301-308, Jan. 2003.
[2] P.S. Crovetti, "All-Digital High Resolution D/A Conversion by Dyadic Digital Pulse Modulation", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 63, No. 3, pp. 573-584, March. 2017
[3] L.Corradini, D. Maksimovic, P.Mattavelli, R.Zane, "Digital Control of High-Frequency Switched-mode Power Converters", Wiley-IEEE Press, 2015.

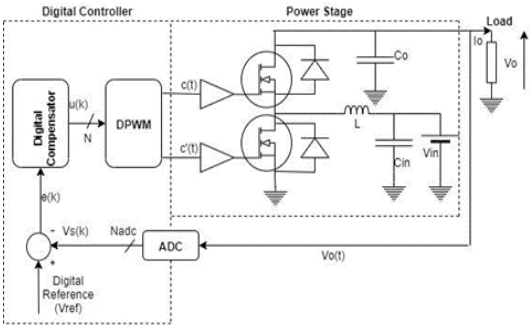

Figure 1 - Block Diagram of Boost Converter and PID Controller

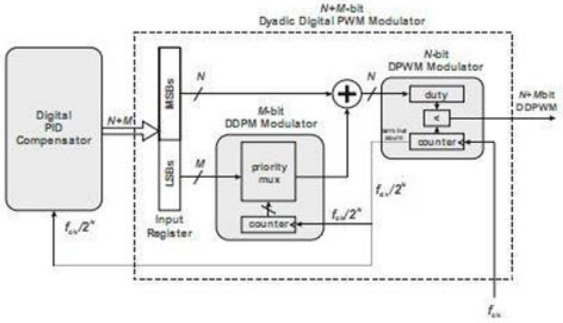

Figure 2 - DDPWM Architecture

Input Voltage V_{in}	$7-10\ Volts$
Output Voltage Vo	12 Volts
Input Capacitor C_{in}	$1uF, r_c = 2m\Omega$
Inductor L	$900nH, r_L = 8m\Omega$
MOSFET R_{on}	$24m\Omega$
Diode R_{on}	$24m\Omega$
Output Capacitor C_o	$3uF, r_c = 40m\Omega$
Load Resistor R_L	$25\Omega - 30\ \Omega$

Table 1 - Boost Converter specifications

$clock\ frequency\ f_{clk}$	$50\ MHz$
$switching\ frequency\ f_{sw}$	$3.125\ MHz$
K_p	[0110111]
K_i	[01001011101]
K_d	[010100001111]
N_{ADC}	5
$N_{DPWM} + N_{DDPM}$	$4+4$

Table 2 - Digital Controller Specifications

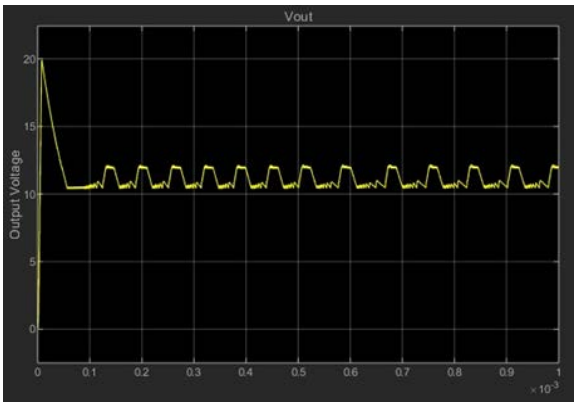

Figure 3 - Boost converter output Voltage v_o with DPWM showing LCOs

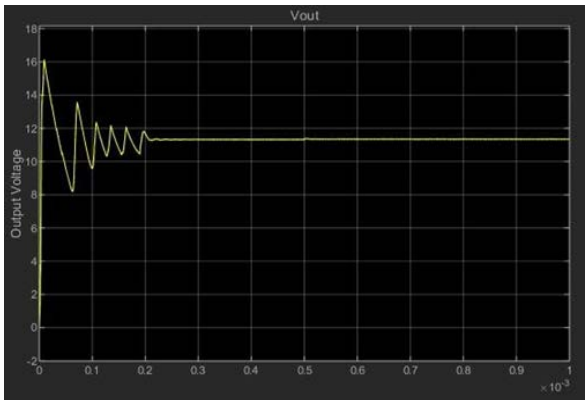

Figure 4 - Boost converter output Voltage v_o with DDPWM with no LCOs