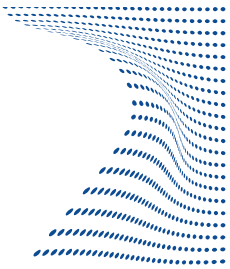
Enhanced Electrical and Reliability Testing of Power Semiconductor Devices

# Polytechnic University of Turin

Doctoral School - 33rd Cycle





Dissertation for the doctoral program in:

Electrical, Electronics and Communications Engineering with curriculum in "Electronic Devices"

# Enhanced Electrical and Reliability Testing of Power Semiconductor Devices

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March 15, 2021

# *Abstract*

## Enhanced Electrical and Reliability Testing of Power Semiconductor Devices

by Davide Cimmino

Before the last two decades, power electronics was strictly related to electrical engineering, and relegated to applications ranging from medium to high powers, such as industry drives, railway traction and power supplies. But with the increasing demand for electricity and the diffusion of modern consumer products related to power management, the whole grid comprehending generation, transmission, distribution and use of electric energy, gained remarkable visibility along with the engineering field of power electronics, with the goal of maximizing the efficiency, versatility and reliability of the supply chain, as well as the integration of renewable power sources into this continuously evolving organism. This PhD thesis, carried out at the Polytechnic of Turin and sponsored by a Vishay Intertechnology Inc. scholarship, focuses on the performance and lifetimes of power semiconductor devices, when electrical and environmental testing conditions apply high stress to the devices beyond current standards, especially in terms of reliability. Part I gives a brief introduction on the major definitions in the field of reliability testing, focusing on the terms involved in the following sections, along with an overview of current and possible future trends in the field of reliability testing. In part II, the standard High Temperature High Humidity Reverse Bias (H3TRB) reliability test for power semiconductor devices, also known as Temperature Humidity Bias (THB) test, is performed at high voltage in order to investigate and analyze peculiar failure modes generated by the combination of high reverse bias voltage and humidity. The results led to the publication of 3 research papers during the doctoral program. The main topic of part III is the study and development of a high-current on-wafer Forward Voltage Drop (VF) drop measurements system for power semiconductor diodes. The methodology involves the design, characterization, evaluation and further improvement of a dedicated testing setup with the objective of performing measurements without inducing any degradation in the devices under test. Eventually, part IV is dedicated to the evaluation of the cosmic ray ruggedness of power semiconductor devices. The testing has been performed in agreement with the JEDEC standard JEP151, and the experimental work involved the development of dedicated testing boards, for the following test campaign at the “ISIS Neutron and Muon Source” of the “Rutherford Appleton Laboratory” in Didcot, United Kingdom.