Guest Editorial: Special section on emerging trends and computing paradigms for testing, reliability and security in future VLSI systems

Guest Editors' Introduction: Special Issue on Emerging Trends and Computing Paradigms for Testing, Reliability and Security in Future VLSI Systems

Stefano Di Carlo, *Senior Member, IEEE,* Peilin Song, *Member, IEEE,* and Alessandro Savino, *Member, IEEE*

With the rapid advancement of computing technologies in all domains (i.e., handheld devices, autonomous vehicles, medical devices, and massive supercomputers), testability, reliability and security of electronic systems are crucial issues to guarantee safeness of human life. Emerging technologies coupled with new computing paradigms (e.g., approximate computing, neuromorphic computing, in-memory computing) are together exacerbating these problems posing significant challenges to researchers and designers. To address this increased complexity in the hardware testing/reliability/security domain, it is imperative to employ design and analysis methods working at all levels of abstraction, starting from the system level down to the gate level.

In this context, the selected papers span from the important field of the yield analysis and modeling, which is becoming fundamental for the manufacturing of modern technologies to the error detection, correction and recovery when the new devices are operative on field. At the same time, papers do not forget that the fault tolerance can be achieved by a cross-layer approach to the dependability that includes the analysis of the effect of faults and the techniques and methodologies to deploy more resilient devices by means of hardening of the design. Eventually, the dependability of the systems is nowadays deeply linked with the security aspects, including the impact on the design trade-offs and the test and validation.

The IEEE VLSI Test Symposium (VTS) invited the highest ranked papers to be included in this special issue of IEEE Transactions on Emerging Technologies in Computing (TETC) in 2020. All aspects of design, manufacturing, test, monitoring and securing of systems affected by defects and malicious attacks are covered by the accepted paper.

It is our great pleasure to publish this special issue containing 12 high-quality papers covering all aspects of the emerging trends on testing and reliability:

- In *FTxAC: Leveraging the Approximate Computing Paradigm in the Design of Fault-Tolerant Embedded Systems to Reduce Overheads* by Aponte-Moreno, Alexander; Restrepo-Calle, Felipe; Pedraza, Cesar, the design of Fault Tolerant systems is exploited by means of approximate computing techniques to reduce the implicit overhead of the common redundancy.
- In *A Statistical Gate Sizing Method for Timing Yield and Lifetime Reliability Optimization of Integrated Circuits* by Ghavami, Behnam; Ibrahimi, Milad; Raji, Mohsen, the reliability of CMOS devices is improved tackling the joint effect of process variation and transistor aging.
- In *3D Ring Oscillator based Test Structures to Detect a Trojan Die in a 3D Die Stack in the Presence of Process Variations* by Alhelaly, Soha; Dworak, Jennifer; Nepal, Kundan; Manikas, Theodore; Gui, Ping; Crouch, Alfred, the issue of Trojan insertion into 3D integrated circuits has been explored from the use of in-stack circuitry and various testing procedures point of view, showing their detection capability.
- In *Defect Analysis and Parallel Testing for 3D Hybrid CMOS-Memristor Memory* by Liu, Peng; You, Zhiqiang; Wu, Jigang; Elimu, Michael; Wang, Weizheng; Cai, Shuo; Han, Yinhe, a new parallel March-like test is proposed to test CMOS Molecular architectures.
- In *Attacks toward Wireless Network-on-Chip and Countermeasures* by Biswas, Arnab Kumar; Chatterjee, Navonil; Mondal, Hemanta; Gogniat, Guy; DIGUET, Jean-Philippe, Wireless Network-on-Chip security vulnerabilities are described and their countermeasures proposed.
- *A Novel TDMA-Based Fault Tolerance Technique for the TSVs in 3D-ICs Using Honeycomb Topology* (by Ni, Tianming; Yang, Zhao; Chang, Hao; Zhang, Xiaoqiang; Lu, Lin; Yan, Aibin; Huang, Zhengfeng;

- *M. Shell was with the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332. E-mail: see http://www.michaelshell.org/contact.html*
- *J. Doe and J. Doe are with Anonymous University.*

Manuscript received April 19, 2005; revised August 26, 2015.

Wen, Xiaoqing) proposes a chain-type time division multiplexing access (TDMA)-based fault tolerance technique showing huge area overheads reduction.

- In *Design and analysis of secure emerging cryptohardware using HyperFET devices* by Delgado-Lozano, Ignacio María; Tena-Sánchez, Erica; Núñez, Juan; Acosta, Antonio J., Power Analysis attacks against FinFET device have been tackled by incorporating HyperFET devices to deliver a x25 factor security level improvement.
- In *Detection, Location and Concealment of Defective Pixels in Image Sensors* by TAKAM TCHENDJOU, Ghislain; SIMEU, Emmanuel, image sensors are empowered with online diagnosis and self-healing methods to improver their dependability.
- In *Defect and Fault Modeling Framework for STT-MRAM Testing* by Wu, Lizhou; Rao, Siddharth; Taouil, Mottaqiallah; Cardoso Medeiros, Guilherme; Fieback, Moritz; Marinissen, Erik Jan; Kar, Gouri Sankar; Hamdioui, Said, a framework to derive accurate STT-MRAM fault models is described, together with its employment to model resistive defects in interconnect and pinhole defects in MTJ devices, allowing test solutions for detecting those defects.
- In *Online Safety Checking for Delay Locked Loops via Embedded Phase Error Monitor* byHuang, Shi-Yu; Chu, Wei, the Automotive Safety Integrity Level (ASIL) is targeted by proposing a phase error monitoring scheme for Delay-Locked Loops (DLLs).
- In *Protecting Memories against Soft Errors: The Case for Customizable Error Correction Codes* by Li, Jiaqiang; Reviriego, Pedro; Xiao, Li; Wu, Haotian, the memory protection is supported by a tool able to automate the error correction code design.
- In *Autonomous Scan Patterns for Laser Voltage Imaging* by Tyszer, Jerzy; Cheng, Wu-Tung; Milewski, Sylwester; Mrugalski, Grzegorz; Rajski, Janusz; Trawka, Maciej, authors demonstrates how to reuse on-chip EDT compression environment to generate and apply Laser Voltage Imaging-aware scan patterns for advanced contactless test procedures.

We sincerely hope that you enjoy reading this special issue, and would like to thank all authors and reviewers for their tremendous efforts and contributions in producing these high-quality articles. We also take this opportunity to thank the IEEE Transactions on Emerging Topics in Computing (TETC) Editor-in-Chief (EIC) Prof. Cecilia Metra, past Associate Editor Ramesh Karri, the editorial board, and the entire editorial staff for their guidance, encouragement, and assistance in delivering this special issue.