Ka-band MMIC GaN Doherty Power Amplifiers: Considerations on Technologies and Architectures

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Invited paper

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***Abstract* — This paper presents a comparison of two sample GaN technologies, one on Silicon and the other on Silicon Carbide substrate, when applied to the design of an integrated Doherty power amplifier. Two different target applications are considered, namely the satellite Ka-band downlink (17.3–20.3 GHz) and terrestrial communications in the n257 FR2 5G band (26.5–29.5 GHz), with different specifications but similar absolute frequency range. Considerations are made highlighting advantages and disadvantages of the two technologies for the design of high frequency MMIC Doherty Power Amplifiers in the presented scenarios.**

***Keywords* — Doherty, GaN, power amplifiers, satellite, 5G.**

I. Introduction

The increasing demand of communication links with high capacity is driving the development of highly efficient Power Amplifiers (PAs) operating at microwave and mm-waves [1]. Efficient amplification with non-constant envelope modulations requires the adoption of specific solutions, a popular one at sub-6 GHz frequencies being the Doherty PA (DPA) [2], [3]. Its implementation at higher frequency is challenging due to the intrinsically lower gain of the transistors, which calls for multi-stage architectures, and the need of combining power on-chip to achieve the targeted performance, which also complicates the architecture. A further challenge is to maintain wideband operation. When power levels around 5–10 W are required, both for terrestrial and space applications, GaN MMIC DPAs are appearing [4], [5]. The high power density of GaN allows to realize simpler matching networks reducing the MMIC area. GaN HEMTs are available both on Si and SiC substrates. GaN-SiC has higher thermal conductivity, lower losses and higher power density, while GaN-Si is less expensive and more easily integrable with the digital part of the transceiver. Therefore, the choice of the technology is not always immediate.

In this work, two GaN technologies (Si or SiC substrate) are compared in terms of their suitability to design a MMIC DPA for Ka-band applications. Two scenarios are considered, namely satellite and terrestrial, and consideration are made on the feasibility and the complexity of the architecture achievable by each of the two technologies based on the specifications. One of the analyzed cases is then investigated in terms of frequency behaviour, comparing different DPA architectures and suggesting an approximate method to select the most appropriate one for the targeted band.

II. Technologies and design specifications

Two technologies are compared, namely a GaN-Si and a GaN-SiC HEMT process, which are assumed to have similar gate length and therefore to be suitable for the same frequency range of operation (up to Ka-band). The process parameters of interest for the present considerations are summarized in Table 1. They are meant to be representative of the process category and not specific of a given technology. Both have similar current density and output parasitics per unit length (periphery), but GaN-SiC can sustain higher voltages and therefore provides higher power density compared to GaN-Si.

The targeted applications for this analysis are the Ka satellite downlink and the terrestrial FR2 5G band. A DPA suitable for satellite downlink should deliver around 10 W output power on the 17.3–20.3 GHz band, considering the supply voltage derating imposed by the space requirements [6]. The FR2 5G band n257 covers a similar frequency range of 3 GHz (26.5–29.5 GHz) but no derating needs to be applied, since the component lifetime is less critical, and a lower power level is required (of the order of 5 W for a single PA).

The drain supply voltage V_{DD} and the corresponding current density $\mathcal{I}_{\mathrm{MAX}}$ indicated in Table 1 refer to the maximum ratings of the two technologies, i.e. do not consider any derating that may be applied in specific applications. A 25% derating on V_{DD} will be considered for the satellite application, which reduces the achievable maximum power density $\mathcal{P}_{\mathrm{out,MAX}}$ by the same amount.

Table 1. Parameters of the sample GaN processes.

Substrate	$\mathcal{P}_{\mathrm{out,MAX}}$ (W/mm)	V_{DD} (V)	$\mathcal{I}_{\mathrm{MAX}}$ (mA/mm)	$\mathcal{C}_{\mathrm{out}}$ (fF/mm)
Si	2.5	15	666	500
SiC	4	25	640	500

III. Power budget

The power budget considerations that guide the design of a DPA are presented focusing on the final stage only (i.e. neglecting whether the PA needs to have driver stages) and assuming a standard 6 dB DPA adopting identical main and auxiliary devices. This is a simplifying assumption which limits the scope of the analysis and allows to make

comparisons. Of course this topology may not be the optimum choice for either application, but the same considerations can easily be extended or adapted to a different DPA configuration. Also, when the required output power level cannot be reached with a single device, the possibility to combine power at device or at the PA level exists [7]. In this case, it is assumed that a DPA is formed adopting a single device for main and auxiliary, and several DPAs are then combined (on chip) to reach the power target. This is somewhat arbitrary, but similar considerations would apply for combination at device level. To account for the power combination in a quantitative way, a combination efficiency is defined as

$$\eta_{\mathrm{c},N} = \frac{P_{\mathrm{L}}}{\sum P_{\mathrm{out,DPA}}} = (\eta_{\mathrm{c},2})^{L} = (\eta_{\mathrm{c},2})^{[\log_2(N)]}, \quad (1)$$

assuming that N DPAs are combined and only two-way combinations are implemented, like in a corporate amplifier (see Fig. 1), each having $\eta_{\mathrm{c},2}$ =93% (i.e. 0.3 dB losses). Therefore, only combinations of $N = 2^L$ DPAs in L levels are allowed. η_{c} has an impact on the maximum power and, as a consequence, on the efficiency. It is reasonable to assume that the effect on the achievable efficiency is due to a reduction of the RF power only, while the DC power is unchanged, i.e.

$$\eta_{\mathrm{drain}} = \frac{P_{\mathrm{L}}}{P_{\mathrm{DC}}} = \frac{\eta_{\mathrm{c},N} \sum P_{\mathrm{out,DPA}}}{P_{\mathrm{DC}}} \quad (2)$$

and $\eta_{\mathrm{drain,MAX}} = 78.5\% \cdot \eta_{\mathrm{c},N}$ for tuned load class B devices.

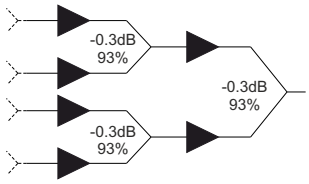

Fig. 1. Scheme of the considered power combination structure and corresponding combination efficiency.

A. Satellite application

For the satellite application around 18.8 GHz, the maximum transistor periphery available providing a reasonable gain is considered to be 0.8 mm. The 25% V_{DD} derating makes the maximum power density $\mathcal{P}_{\mathrm{MAX}}$ equal to 1.87 W/mm and 3 W/mm for GaN-Si and GaN-SiC, respectively. Therefore, a total periphery of 5.34 mm and 3.34 mm is required. Assuming a 0.8 mm device is used for the main and auxiliary, GaN-Si requires the combination of 4 DPAs, whereas GaN-SiC can almost reach the target power with only 2 DPAs. As summarized in Table 2, the achievable efficiency will be lower for the GaN-Si case as a consequence of the higher complexity of the architecture, N=4 being an upper bound for the number of reasonable on-chip combinations.

B. Terrestrial application

For the terrestrial application around 28 GHz, the maximum transistor periphery is lowered to 0.6 mm, to account for the higher operating frequency and consequent inherently lower gain of the active devices. No derating needs to be applied; therefore, the power densities used for the power budget are those reported in Table 1. Targeting a 5 W PA requires an overall active periphery of 2 mm and 1.25 mm if GaN-Si and GaN-SiC are adopted, respectively. Adopting a 0.6 mm device for the main and auxiliary branches, GaN-Si requires the combination of 2 DPAs, while a single DPA in GaN-SiC can achieve 4.8 W, which almost meets the power requirement. Therefore, also in this case, GaN-SiC allows to avoid one level of output power combination, with a beneficial effect on the maximum achievable efficiency, as shown in Table 2. If GaN-Si is adopted power combination cannot be avoided, but one could select a device with slightly smaller periphery.

Table 2. DPAs architecture and performance at design frequency.

		N	W_{main} (mm)	P_{L} (W)	$\sum P_{\mathrm{out_{DPA}}}$ (W)	η_{max} (%)	R_{opt} (Ω)
Sat.	Si	4	0.8	10.4	12	68	43
	SiC	2	0.8	8.9	9.6	73	73
Ter.	Si	2	0.6	5.5	6	73	75
	SiC	1	0.6	4.8	4.8	78.5	130

Table 2 also reports the optimum load of the individual active device with periphery W_{main}, computed as

$$R_{\mathrm{opt}} = \frac{2V_{\mathrm{DD}}}{I_{\mathrm{MAX}}} = \frac{2V_{\mathrm{DD}}}{W_{\mathrm{main}}\mathcal{I}_{\mathrm{MAX}}}, \quad (3)$$

according to the tuned load class B assumption. This can give an indication of the difficulty to achieve wideband operation with the corresponding architecture. The 4-DPA GaN-Si architecture is the less favourable in terms of area occupation, losses and efficiency, but it is the one where the optimum impedance level is closer to 50 Ω. Therefore, it is reasonable to expect that it will be comparatively easy to maintain proper Doherty operation with the targeted performance over a wide bandwidth. On the contrary, the single DPA in GaN-SiC is very favourable in terms of architecture simplicity, area, losses and efficiency, but it works with quite a high impedance level, which will make the realization of wideband matching networks much more challenging. For the two intermediate cases, the optimum load is still relatively close to 50 Ω, although higher. Considerations on the specific design will suggest whether it is more convenient to combine power at DPA level or at device level, which would halve the optimum load impedance, but will make it more complicated to control the load modulation [7]. However, the bandwidth achievable by a DPA strongly depends on the topology adopted for the output combiner, which in turn is related to the strategy adopted to compensate for the device parasitic effects. Making general considerations is not trivial, and the specific design constraints need to be considered for the case under study.

IV. Bandwidth considerations

Simplified linear analyses can be helpful to give an initial estimation of the achievable bandwidth for a target

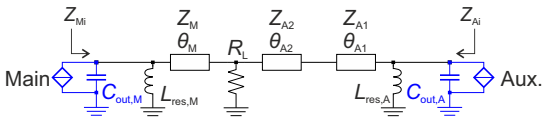

Fig. 2. Scheme of the analyzed DPA combiner, where the active devices are represented by controlled current sources with a shunt parasitic $C_{\rm out}$.

performance (or the performance achievable on a targeted band). We focus on the simplest case analyzed in Sec. III, the single-device GaN-SiC DPA for terrestrial 5G applications. The typical peak-to-average power ratio (PAPR) used in 5G systems is around 8-9 dB, therefore the 6 dB DPA architecture previously used as a comparison benchmark can be thought as sub-optimum in terms of output back-off (OBO) efficiency, at least at the design frequency. It is interesting to investigate if this consideration is valid also on a wider bandwidth (specifically on the n257 FR2 5G band), or if a simpler architecture that is not optimum at single frequency can provide a better performance.

To this aim, a 6 dB and a 9 dB two-way DPAs based on the same combiner topology are analyzed according to the method described in [8]. The selected combiner includes a $\lambda/4$ impedance inverter on the main and two $\lambda/4$ sections on the auxiliary, as shown in Fig. 2. This topology is suitable to realize any generic N-dB DPA and allows to choose freely $R_{\rm L}$ thanks to the degree of freedom provided by the double $\lambda/4$ section on the auxiliary. The design formulas for a N-dB DPA are:

$$Z_{\rm M} = \sqrt{kR_{\rm opt,M}R_{\rm L}} \qquad \frac{Z_{\rm A2}}{Z_{\rm A1}} = \sqrt{\frac{kR_{\rm L}}{R_{\rm opt,M}}} \tag{4}$$

where $N = 10\log_{10}(k)$, $L_{\rm res} = 1/(\omega_0^2 C_{{\rm out},i}), i = {\rm M, A}$ is a shunt inductance that resonates the parasitic output capacitance of the active device at the design frequency f_0, $\omega_0 = 2\pi f_0$, and $Z_{\rm M}$, $Z_{\rm A1}$, $Z_{\rm A2}$ have 90° electrical length at f_0.

Fig. 3 reports the DPA performance estimated with the adopted simplified analysis versus frequency, assuming $f_0 = 28$ GHz and $R_{\rm L} = 50\,\Omega$ in both cases. The saturated power and efficiency are very similar for the 6-dB and 9-dB DPAs over the whole band. On the contrary, the performance at 9 dB OBO is quite different. The 9-dB DPA is clearly optimum at f_0, but it is more narrowband. The OBO efficiency and power drop quite significantly at the band edges, reaching lower values than those provided by the 6-dB DPA, although it is sub-optimum at f_0. Similar considerations hold for the gain compression, which is far more severe for the 9-dB DPA. This behaviour is due to several factors, among which the higher impedance transformation ratio and the higher parasitic capacitance of the auxiliary (doubled periphery) in the 9-dB DPA. It should be kept in mind that these considerations are simply preliminary guidelines, which neglect a number of essential factors in the realization of a MMIC DPA at these frequencies, such as the need of inserting driver stages. Moreover, a very simple combiner topology is used for this comparative analysis, but this is not optimized for wideband behaviour. Other techniques may be applied to achieve a more wideband operation [9].

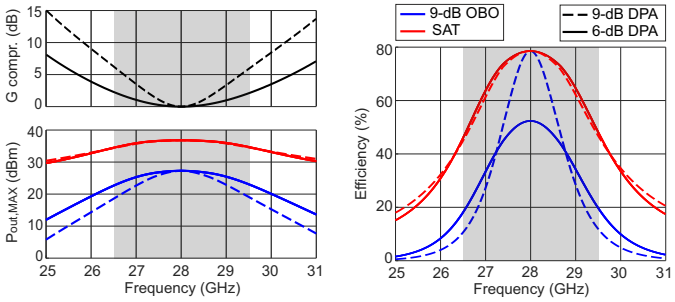

Fig. 3. Estimated performance of the 6-dB (solid) and 9-dB (dashed) DPAs at saturation and at 9-dB OBO vs frequency, with FR2 n257 5G band shaded.

Finally, when a high efficiency is required not only at one specific OBO point but across the whole dynamic range, a possibility is to realize a three-way DPA [10].

V. Conclusion

Two sample GaN technologies have been compared in terms of suitability to design an MMIC Doherty power amplifier for satellite Ka-band and 5G FR2 communications. Considerations have been made on feasibility and complexity of the architecture enabled by each technology, focusing on output power target and on behaviour versus frequency.

References

[1] V. Camarchia *et al.*, "A Review of Technologies and Design Techniques of Millimeter-Wave Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2957–2983, 2020.

[2] A. Grebennikov and S. Bulja, "High-Efficiency Doherty Power Amplifiers: Historical Aspect and Modern Trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190 –3219, Dec. 2012.

[3] R. Quaglia *et al.*, "A 4-W Doherty Power Amplifier in GaN MMIC Technology for 15-GHz Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 4, pp. 365–367, April 2017.

[4] V. Valenta *et al.*, "High-gain GaN Doherty power amplifier for Ka-band satellite communications," in *IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Jan 2018, pp. 29–31.

[5] R. Quaglia *et al.*, "Source/Load-Pull Characterisation of GaN on Si HEMTs with Data Analysis Targeting Doherty Design," in *2020 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Jan 2020, pp. 1–3.

[6] C. Ramella *et al.*, "Thermal-aware GaN/Si MMIC design for space applications," in *2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*, 2019, pp. 1–6.

[7] A. Piacibello *et al.*, "GaN Doherty MMIC Power Amplifiers for Satellite Ka-band Downlink," in *2020 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)*, 2020, pp. 1–3.

[8] J. J. M. Rubio *et al.*, "Design of an 87% Fractional Bandwidth Doherty Power Amplifier Supported by a Simplified Bandwidth Estimation Method," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1319–1327, March 2018.

[9] V. Camarchia *et al.*, "Integrated Doherty power amplifiers for satellite systems: challenges and solutions," in *2019 IEEE Topical Workshop on Internet of Space (TWIOS)*, Jan 2019, pp. 1–4.

[10] H. Zhang *et al.*, "A 50W Highly Linear 3-Way Integrated Wideband Doherty PA for Small-Cell Application," in *2018 48th European Microwave Conference (EuMC)*, 2018, pp. 1229–1232.