Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging

4. Simulation and Experimental Results

In this section, the harmonic attenuation achieved by the designed *LCL* filter and the current control performance of the AFE converter are verified by means of simulation and experimental testing.

The converter-side and grid-side inductors share the same design (i.e., $L = L_f$), which is obtained from an internally developed optimization procedure taking into account a wide database of core geometries, core materials and wire formats/sizes [57]. The adopted loss and thermal models are described in [58].

The resulting inductor design features two stacked EE 6527 cores in XFlux 60µ powder material from Magnetics [59], with an 18-turn winding of enameled round wire, as illustrated in Figure 12a. The powder material simultaneously provides high saturation flux density and low relative permeability (i.e., $\mu_r = 60$ in the present case), enabling an extremely compact inductor realization. In particular, the low permeability property allows to drastically reduce or even eliminate the air gap between the two core halves. In this way, the inductance value is no longer affected by the gap mechanical tolerance and the unwanted high-frequency winding losses caused by the air gap fringing field (e.g., present in ferrite core implementations) are avoided. However, the complete flux density range of the material (i.e., 0–1.6 T) is not exploited, due to the intrinsic soft saturation characteristics of powder materials [59]. In the present case the inductor is designed to operate between 191 µH in no-load conditions and 151 µH at $I_{max} = 61.5$ A, as illustrated in Figure 12b, utilizing only a 0–0.6 T interval to avoid excessive inductance variation during the fundamental line cycle. As a further note, a round wire with large cross-section is used since winding losses are completely dominated by the low-frequency (i.e., 50 Hz) current component. Therefore, the inductor optimization procedure aims to minimize the overall wire DC resistance, clearly avoiding winding arrangements with low window utilization such as litz wire implementations.

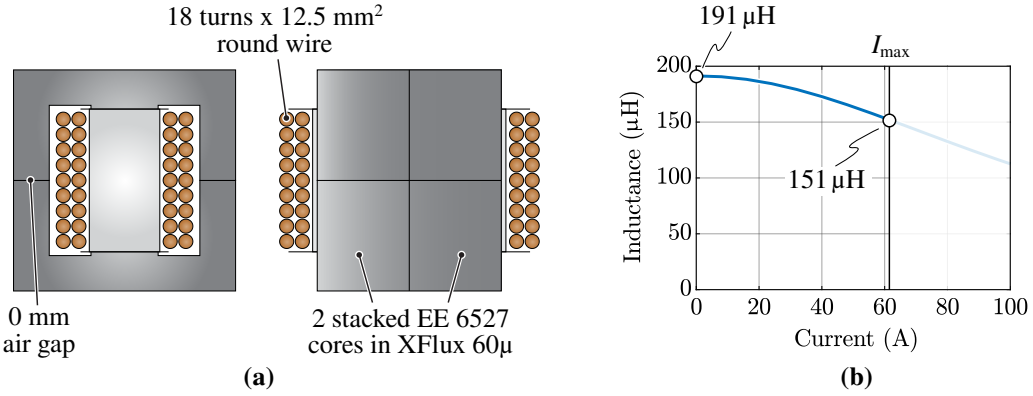

Figure 12. Schematic representation of the designed inductor ($L = L_f$) (**a**) and differential inductance value dependence on the DC-bias current (**b**), which highlights the soft saturation characteristic of the selected powder core material.

The AFE converter prototype, including the 3-level unidirectional T-type rectifier and the *LCL* filter, is shown in Figure 13. The rectifier (see Figure 7) employs 650 V Si MOSFETs switching at 20 kHz and 1200 V Si fast-recovery diodes. The AFE also includes an EMI filter consisting of a three-stage differential-mode filter (including the *LCL* stage) and a two-stage common-mode filter. Figures 13a,b provide a closer view of the realized filter inductors ($L = L_f$) and the selected filter capacitors (C_f), highlighting the size difference between them.

It is worth noting that the converter prototype is a 60 kW unit consisting of two three-phase sub-units in parallel. In the present case, only one 30 kW three-phase unit is operated and the boost inductors of the other unit are exploited as grid-side filter inductors (L_f).

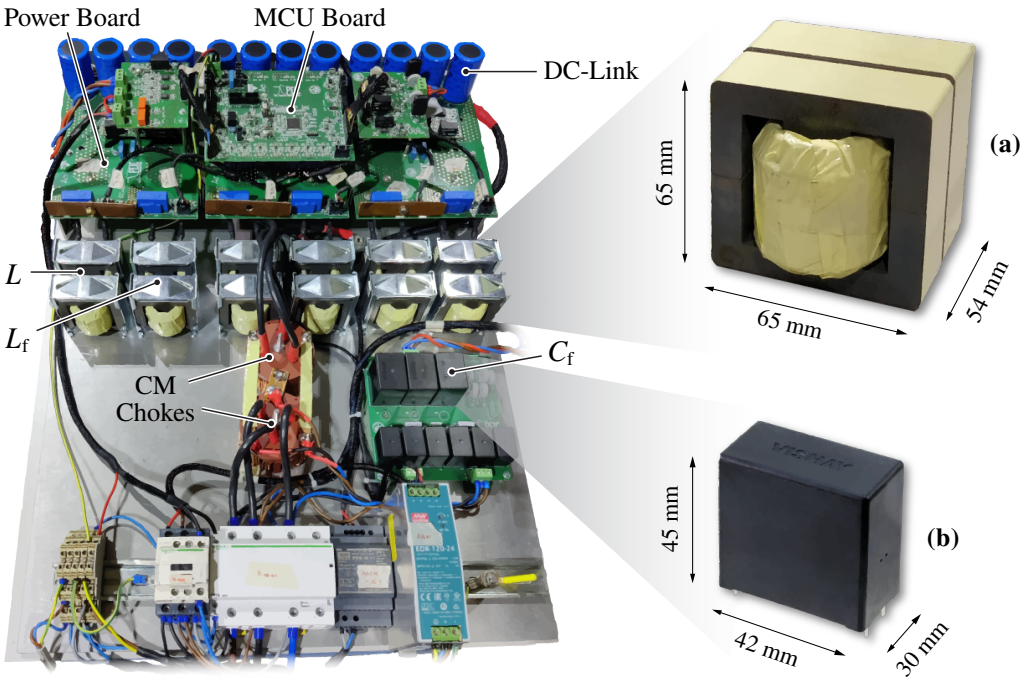

Figure 13. Overview of the active front-end (AFE) prototype utilized for the experimental tests, with highlight of (**a**) the realized inductor ($L = L_f$) and (**b**) the selected capacitor (C_f).

4.1. Filter Transfer Functions

The only LCL filter transfer function that can be directly measured is $Y(s)$, which represents the inverse of the filter impedance seen from the converter side. This impedance is measured with the setup illustrated in Figure 14, where a Hioki 5352-50 LCR meter is adopted for the task.

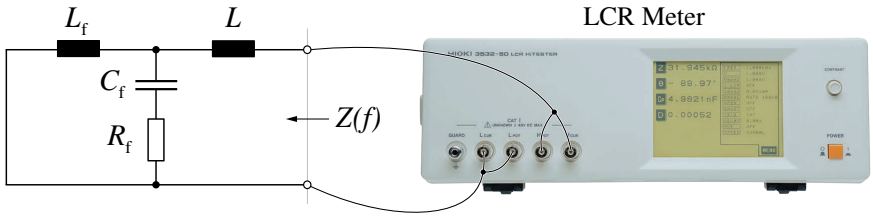

Figure 14. Experimental setup utilized to measure the value of $Y = 1/Z$ (see Figure 15a).

The transfer functions Y, Y_c and Y_f of the designed LCL filter are analytically calculated with the parameters reported in Figure 10 according to (1), (2) and (3), respectively. These transfer functions are illustrated in Figure 15 for both the undamped ($R_f = 0$) and the damped ($R_f = 0.8\,\Omega$) cases. The measurement results of Y are reported in Figure 15a for comparison purposes, where a close match with the analytical model is observed. A slight asymptotic deviation between the two transfer functions is mainly attributable to the inductance value of 191 µH at zero DC-bias current (i.e., the measurement condition), which differs from the design value of 175 µH. Another discrepancy is observed around the two resonance frequencies f_f and f_0, where the experimental results show a stronger damping of the resonance peaks. This is caused by the unmodeled parasitic AC resistance of the filtering elements, mostly given by the inductors (i.e., winding and core losses). In particular, this high-frequency resistance contribution helps to damp the filter resonance, thus improving the converter closed-loop current control stability without generating additional losses at the grid frequency, as opposed to R_f.

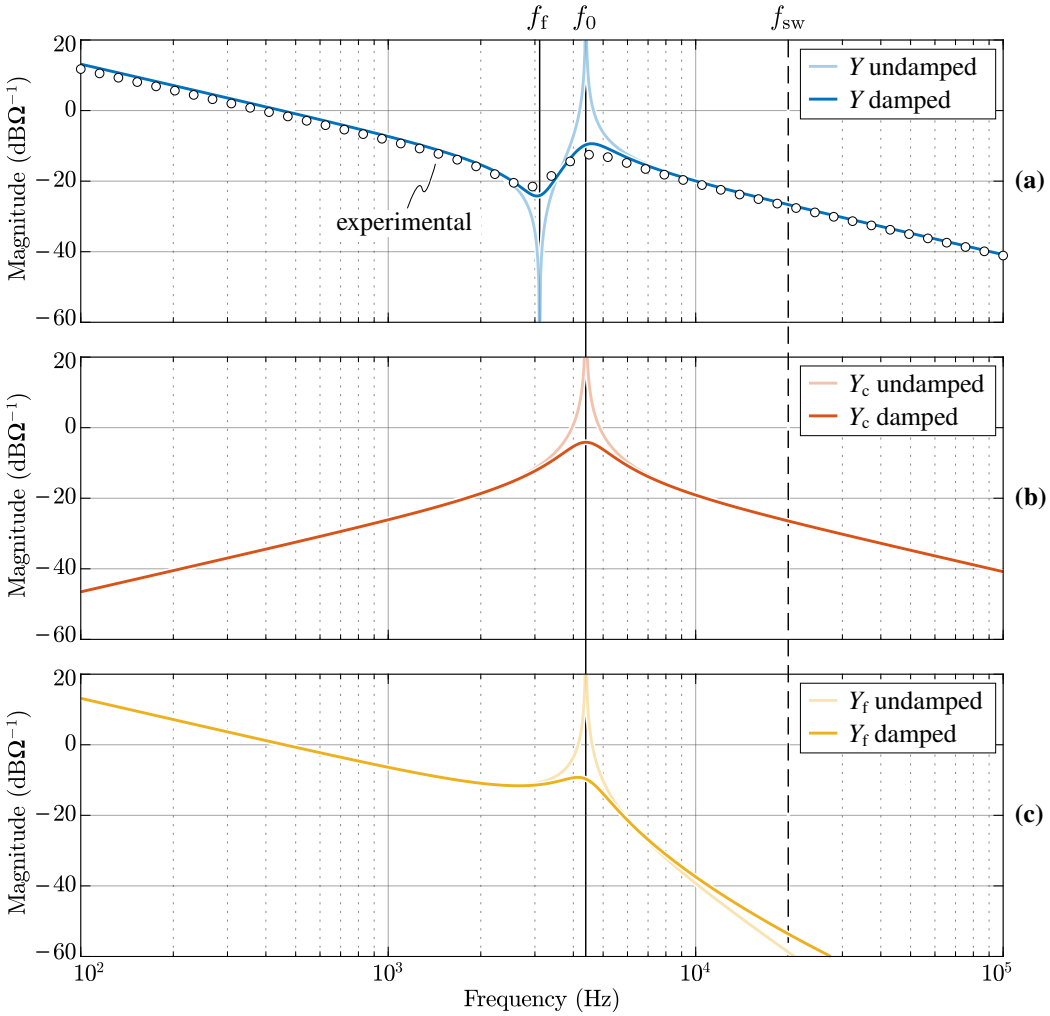

Figure 15. Analytical *LCL* filter transfer functions (**a**) Y, (**b**) Y_c and (**c**) Y_f, with and without passive damping (i.e., $R_f = 0.8\,\Omega$ in the damped case). The value of Y measured experimentally is reported for comparison purposes in (**a**).

4.2. Filter Attenuation

The filter attenuation performance is verified experimentally by measuring the current injected into the grid and assessing its harmonic distortion.

The experimental setup consists of a grid emulator connected at the input of the *LCL* filter, emulating the European low-voltage grid (i.e., $U = 230\,V_{RMS}$, $f = 50\,Hz$), and an electronic load connected at the output of the DC-link, emulating the DC/DC stage of the battery charger (i.e., the load). Since the AFE is directly connected to the grid emulator, this setup emulates a stiff grid with negligible inner impedance (i.e., SCR $\approx \infty$), representing a worst case scenario from the filtering perspective.

The measurements are performed with a Teledyne LeCroy 500 MHz, 12-bit, 10 GS/s, 8-channel oscilloscope, employing isolated high-voltage differential probes for voltage measurements and standard current probes for current measurements.

The experimental grid-side and converter-side current waveforms in nominal stationary conditions (i.e., $I = 61.5\,A$ and $V_{dc} = 800\,V$) are illustrated in Figure 16. The ripple attenuation provided by the *LCL* filter is evident, achieving a current THD of 1.2%. A slight distortion of the grid-side current is observed in proximity of the current zero crossings, as the T-type rectifier briefly enters the discontinuous conduction mode. This distortion is limited by the converter closed-loop control, which must be tuned to achieve high disturbance rejection performance [10].

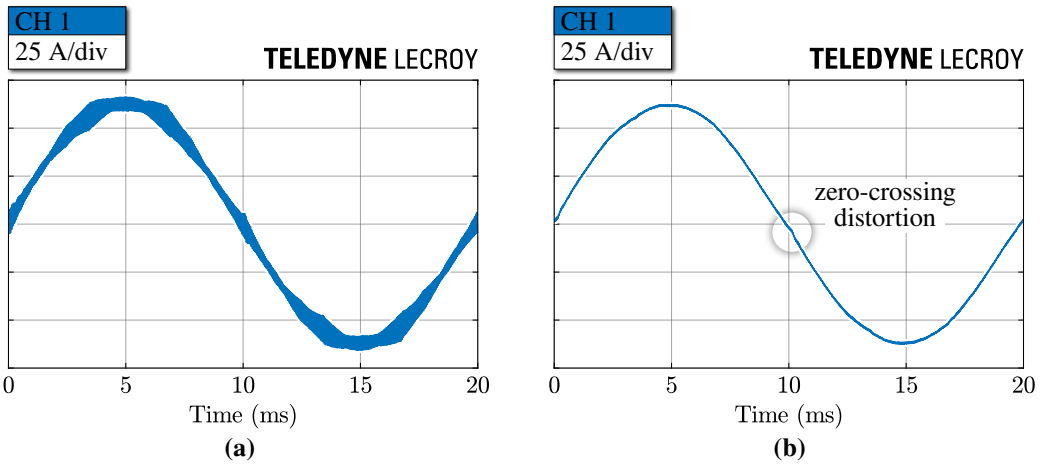

Figure 16. Experimental converter-side current i (**a**) and filtered grid-side current i_f (**b**) at $I = 61.5\,\text{A}$ and $V_{dc} = 800\,\text{V}$. Zero mid-point current modulation (ZMPCPWM) is adopted [20].

The filtered grid current spectrum is calculated by means of a DFT and the results are reported in Figure 17. It is observed that all harmonics comply with the IEEE 519 limits. In particular, the worst-case current harmonic at the design frequency $f_d = 19.6\,\text{kHz}$ is attenuated with a 20% margin.

The slight current distortion related to the converter unidirectional operation generates several low-frequency harmonics, nevertheless they are limited by the closed-loop current control. Moreover, a group of harmonics is visible around the resonance frequency $f_0 = 4.39\,\text{kHz}$, as the filter transfer function Y_f tends to amplify the local harmonics (see Figure 15c). These harmonics are effectively limited by the filter passive damping.

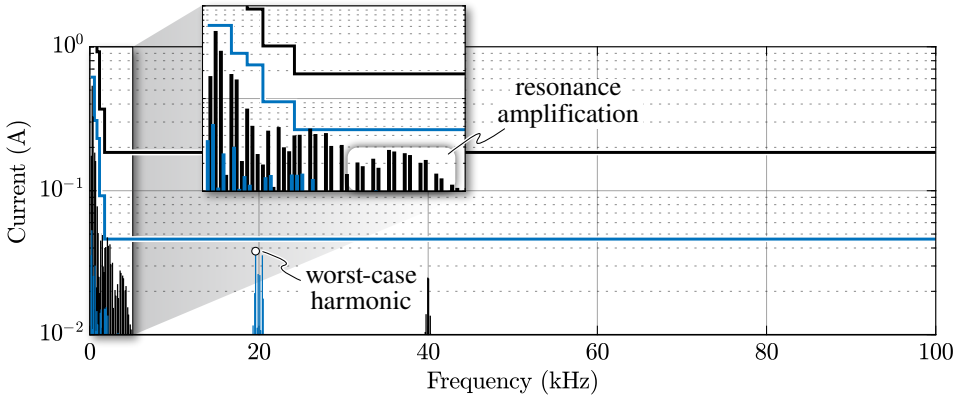

Figure 17. Experimental filtered grid-side current i_f spectrum compared with IEEE 519 odd-order (black) and even-order (blue) harmonic limits. The worst-case harmonic at the design frequency is indicated and the amplification effect around the filter resonance frequency f_0 is highlighted.

It is worth noting that with increasing grid impedance (i.e., $L_g > 0$), the high-frequency filtering results can only improve, as the filter corner frequency f_0 reduces and the asymptotic attenuation increases. Moreover, the high-frequency current harmonics are independent on the load, as they only depend on the PWM voltage harmonics. Therefore, the high-frequency (i.e., asymptotic) attenuation performance of the designed *LCL* filter can be considered successfully verified in all operating conditions.

The low-frequency harmonic distortion, highlighted in Figure 17, depends on the converter load and is thus analyzed further. In particular, when operating at light load, the closed-loop current control is not able to perfectly compensate the large zero-crossing distortion related to DCM operation. This phenomenon leads to higher current THD at lighter loads, as illustrated in Figure 18a. It is important to keep in mind that the *LCL* filter is designed to comply with the operational constraints reported in Section 3, taking advan-

tage of the AFE modular structure shown in Figure 7. Specifically, the converter modularity allows to turn-off selected modules at light load (i.e., $P_{min} = 0.5\,P$), thus ensuring the high-power operation of the remaining modules. Figure 18b shows that the current THD is limited below 5% between 20% and 100% of the nominal power (i.e., 6–30 kW), achieving acceptable distortion over the complete design operating range of the converter module.

Another quantity affected by the converter load is the power factor, as illustrated in Figure 18b, where both the displacement power factor ($\cos\varphi$) and the total power factor (PF) are shown. The relation between the two is straightforward:

$$\mathrm{PF} = \frac{\cos\varphi}{\sqrt{1+\mathrm{THD}^2}} \tag{16}$$

The adopted control strategy, schematically represented in Figure 19, does not compensate for the reactive current generated by the filter capacitors, thus leading to non-unity cosφ operation. This feature, already taken into account during the design phase (i.e., see constraint ⑥), is directly related to the unidirectional operation of the active rectifier, which is not able to produce/absorb any significant amount of reactive power without affecting the input current distortion. Additionally, in this case, the adopted modular structure allows to maintain high power factor values at light load by turning off selected modules and ensuring the high-power operation of the remaining modules. Overall, Figure 18b shows that the total power factor stays above 0.995 between 40% and 100% of the nominal power (i.e., 12–30 kW), thus complying with the design restriction ⑥.

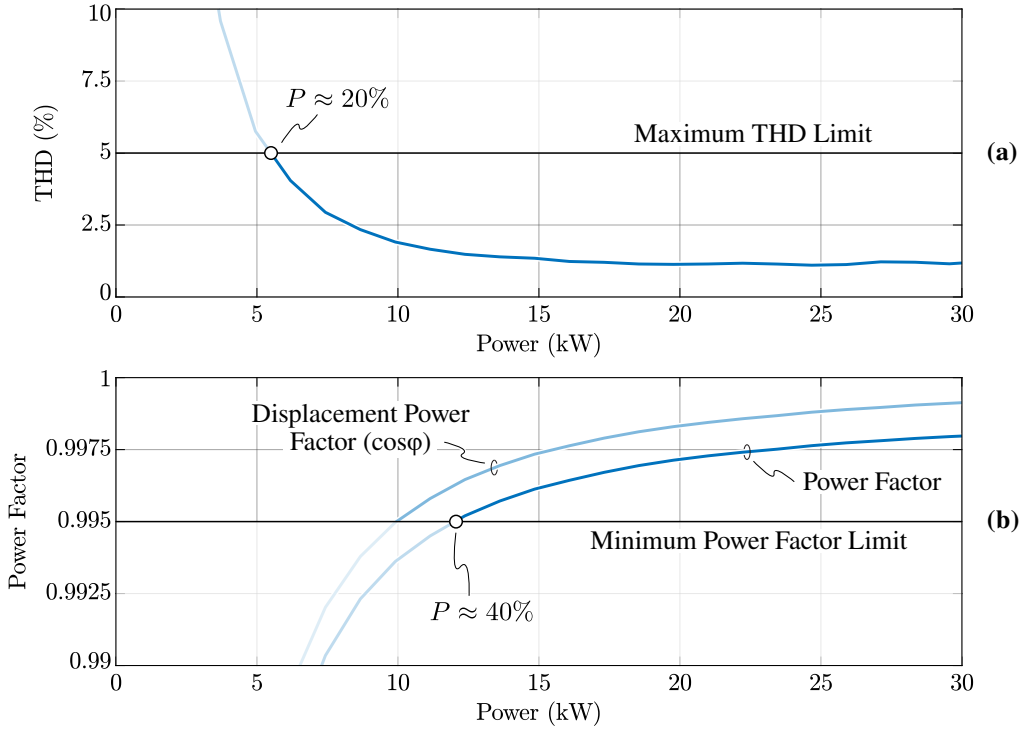

Figure 18. Experimentally measured grid-side current total harmonic distortion (THD) (**a**) and power factor (**b**) as functions of the transferred power. The maximum THD limit and the minimum power factor requirement are indicated.

4.3. Converter Control Stability and Dynamic Response

The performance of the converter closed loop control is assessed experimentally with the hardware setup previously described. A conventional voltage-oriented control scheme is adopted [10,22,23,30] and is schematically illustrated in Figure 19.

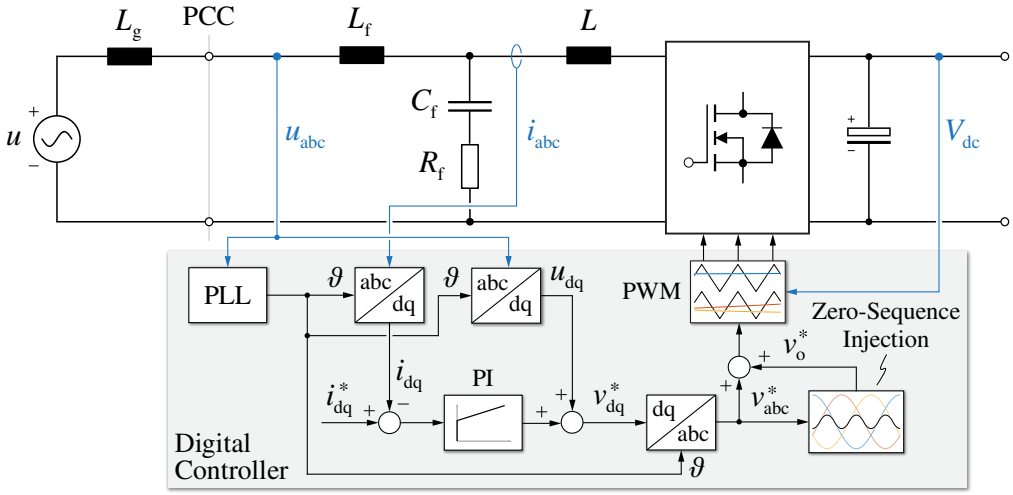

Figure 19. Simplified overview of the converter closed-loop current control: the digital controller schematic is highlighted in grey.

The rotating dq frame is exploited to obtain zero stationary error with a simple PI controller. The PCC voltages are measured to achieve the reference frame synchronization with the grid, which is performed by a phase locked loop (PLL). These voltages are passed through a resonant filter (i.e., the PLL itself) and are then fed forward in the current control loop, to unburden the integral part of the PI regulator. The digital sampling and update process is performed once per switching period ($f_s = f_{sw} = 20\,\text{kHz}$), however the current feedback values are obtained by means of oversampling (32 samples per switching period) and averaging, in order to improve the measurement reliability and thus the control performance around the current zero-crossings. In fact, conventional sampling does not yield the correct average current value when discontinuous conduction mode is encountered [60], thus inhibiting the accuracy of the current control and leading to increased low-frequency distortion.

The digital implementation of the control introduces three main delay components, which reduce the achievable control bandwidth and/or decrease the closed-loop stability margin [23]. The first delay contribution is directly related to the digital processing, which generates one sampling period delay ($T_s = 1/f_s$) between the measured quantities and the control signal output. The second component is linked to the PWM modulator, which introduces a zero-order hold (ZOH) effect with a T_s duration . Finally, the last contribution derives from the current oversampling and averaging process, which results in a moving-average delay of $T_s/2$. The complete dq current control block diagram is illustrated in Figure 20.

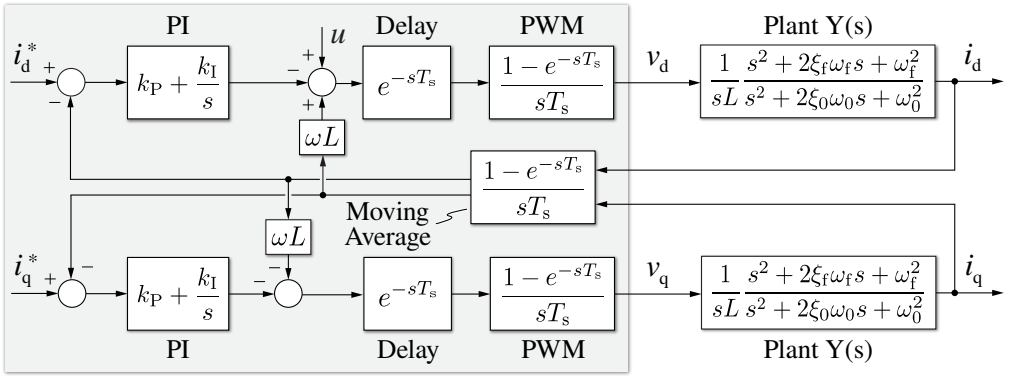

Figure 20. Complete block diagram of the i_d and i_q current control loops [10], including the plant transfer function $Y(s)$.

Since the *LCL* filter transfer function Y behaves as a pure inductance (i.e., $L_{\text{tot}} = L + L_{\text{f}} + L_{\text{g}}$) up until the first resonance frequency f_{f} (see Figure 4a), the current control tuning can be performed in a conventional way. The PI regulator is tuned to achieve a 60° phase margin [10], setting the open-loop cross-over frequency f_{c} to 850 Hz and positioning the PI zero five times lower ($f_{\text{z}} = f_{\text{c}}/5$) to achieve good disturbance rejection capabilities. Since the grid inductance L_{g} is not known in general, the tuning is performed as

$$\begin{cases} k_{\text{P}} = 2\,\pi\,f_{\text{c}}\,(L + L_{\text{f}}) \\ k_{\text{I}} = 2\,\pi\,f_{\text{z}}\,k_{\text{P}} \end{cases} . \tag{17}$$

The current control open-loop transfer function is derived analytically and its magnitude and phase Bode plots are illustrated in Figure 21, for different values of grid inductance L_{g}. Three situations are considered, namely an infinitely stiff grid ($L_{\text{g}} = 0$ pu, SCR $= \infty$), a typical grid for an EV fast charging connection ($L_{\text{g}} = 0.01$ pu, SCR $= 100$) and a reasonably weak grid ($L_{\text{g}} = 0.05$ pu, SCR $= 20$).

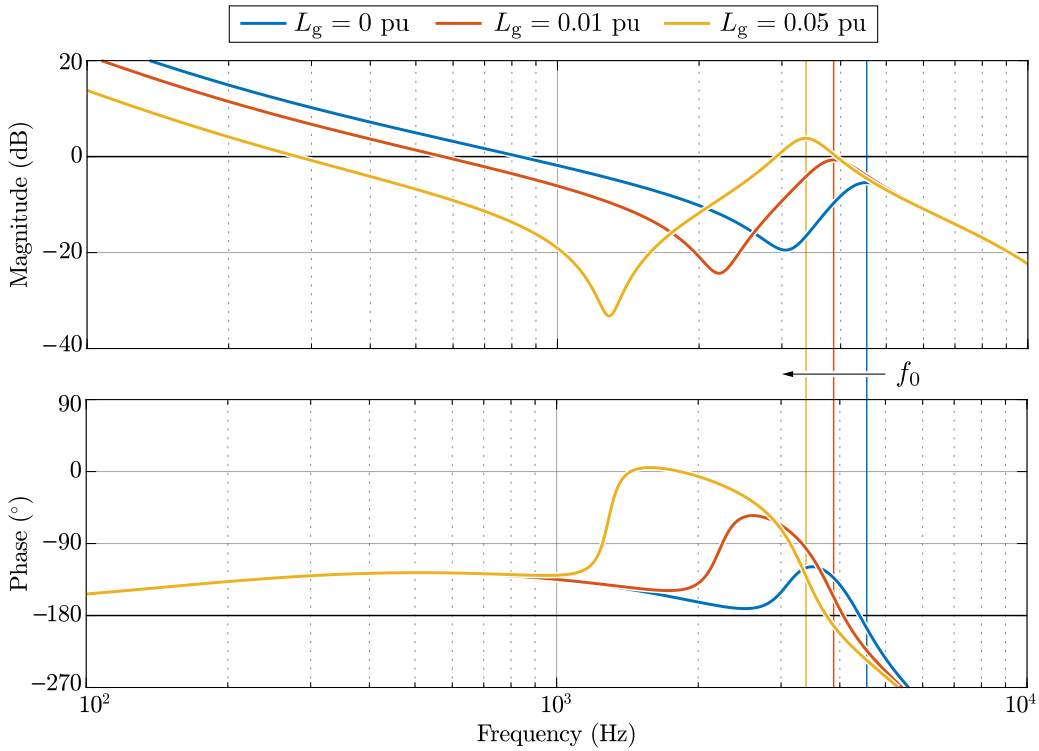

Figure 21. Bode plots of the analytical i_{d} and i_{q} compensated loop gains for different values of grid inductance L_{g}. The PI controllers are tuned according to (17).

In general, to achieve the closed-loop current control stability, the magnitude of the open-loop system transfer function has to be lower than 0 dB when its phase crosses −180° (Nyquist criterion) [25]. From Figure 21 it is observed that the system gain margin decreases for higher values of L_{g} (i.e., lower SCR), as the system resonance frequency f_0 reduces and the peak magnitude increases. Theoretically, the stability limit is reached around $L_{\text{g}} \approx 0.05$ pu (SCR ≈ 20). Figure 21 also shows that a larger L_{g} simultaneously reduces the converter bandwidth and the distance between f_{c} and f_{z}, thus decreasing the low-frequency phase margin and leading to a more nervous control response.

To experimentally verify the closed-loop control stability, the converter response to a reference current step is tested. Different values of grid inductance are emulated by inserting three-phase power inductors between the converter and the grid emulator, approximately achieving $L_{\text{g}} = 0$ pu (i.e., no inductor), $L_{\text{g}} \approx 0.01$ pu and $L_{\text{g}} \approx 0.05$ pu.

The results of the tests are illustrated in Figure 22, where the reference step response of both the converter-side current i and the grid-side current i_f are reported. It is observed that the control loop is stable in all conditions, however the converter-side current shows a damped high-frequency oscillation for large values of L_g.

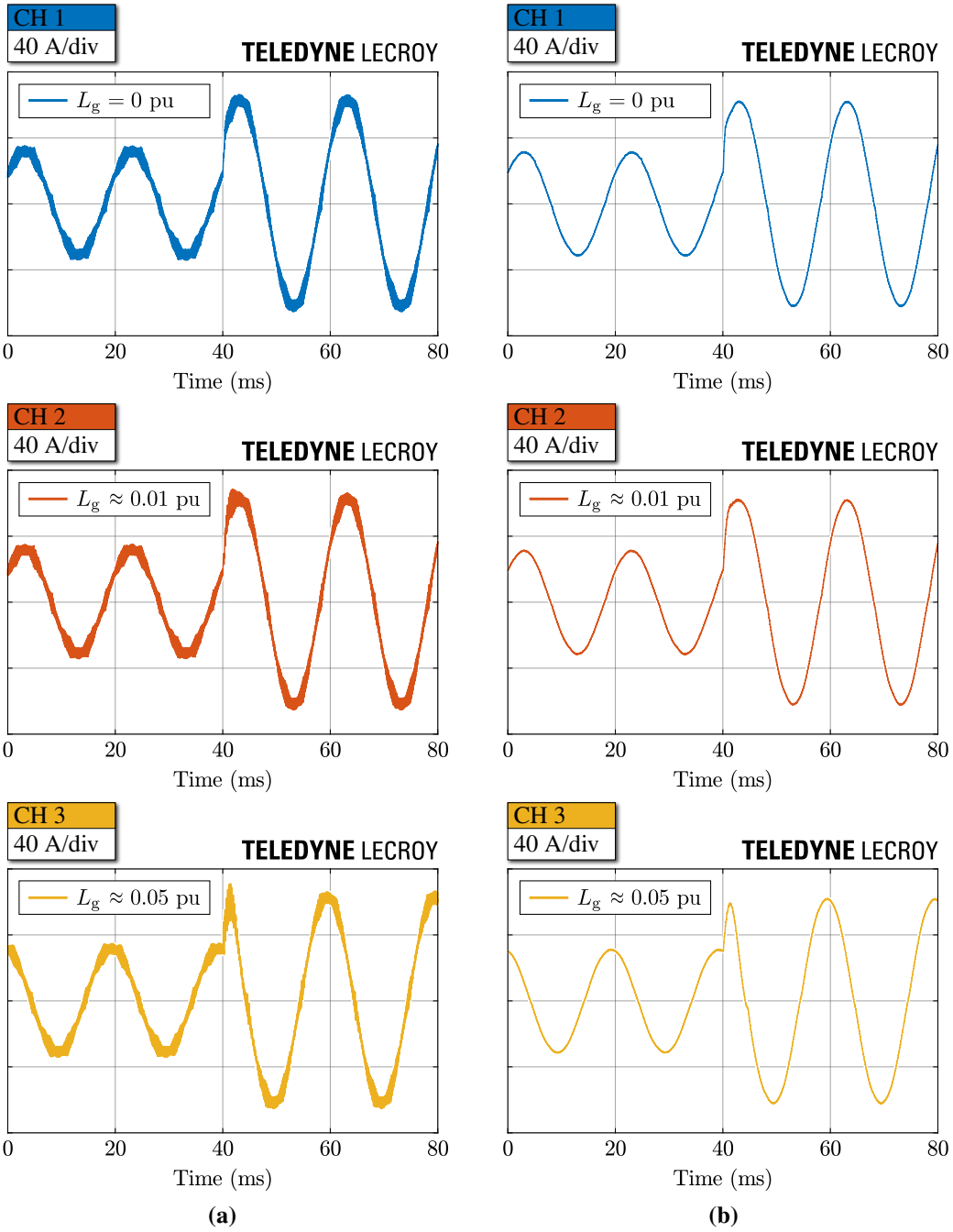

Figure 22. Experimental current control loop step response between 50% and 100% load for different values of grid inductance L_g: (**a**) converter-side current i and (**b**) grid-side current i_f.

This is better highlighted in Figure 23, where the step response of the converter-side currents is reported on the d-axis of the rotating dq frame. The value of i_d is obtained from the digital-to-analog converter (DAC) of the microcontroller unit (MCU), therefore it is discretized in time (i.e., with a T_s periodicity) and is characterized by a large noise content. Figure 23 shows that higher grid inductance values cause at the same time a slower response (i.e., lower bandwidth), a higher overshoot (i.e., lower phase margin) and

an increased high-frequency oscillation (i.e., lower gain margin at the phase cross-over frequency). All of these aspects could already be observed from the open-loop control transfer functions analysis previously reported (see Figure 21), nevertheless they have been verified experimentally.

The current reference step responses reported in Figure 23 show that the stability margin is still not reached for $L_g = 0.05$ pu, as expected instead from the small-signal transfer function analysis. This is mainly due to the unmodeled AC resistance components of the system, which increase the damping of the resonance peaks (see Figure 15a) and thus lead to a wider control stability range.

In conclusion, the closed-loop current control stability is achieved for all grid SCR values up to 20 (i.e., weak grid connection). Therefore, the proposed *LCL* filter design and optimization procedure can be considered successfully validated.

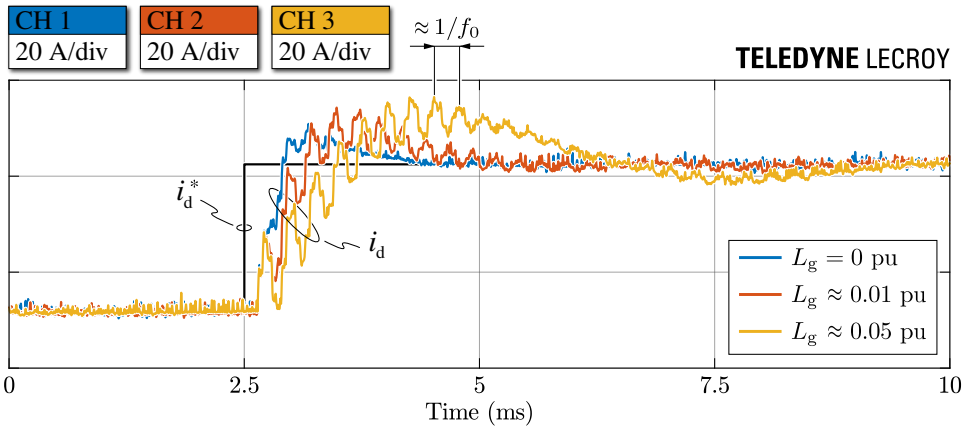

Figure 23. Experimental d-axis current control loop step response between 50% and 100% load for different values of grid inductance. The value of i_d is obtained from the DAC of the MCU (i.e., as a voltage value between 0 and 3.3 V) and then rescaled, thus showing a high amount of noise.

5. Conclusions

This work has presented a complete analysis, design and optimization procedure of a three-phase *LCL* filter for the active front-end unit of a modular EV ultra-fast battery charger. The proposed novel design methodology is based on the graphical representation of the filter design space in the (C_f, L_{tot}) plane. By translating the constraints on the filter parameters into analytical equations, the design space boundaries are identified and the *LCL* filter design minimizing the total required inductance (i.e., optimizing the filter size/loss trade off) can be selected.

This design procedure has been applied to the AC-side filter of a 30 kW, 20 kHz T-type unidirectional rectifier for ultra-fast charging applications. The functionality of the selected optimal *LCL* filter has been first verified in simulation, by checking the filter transfer functions and their effect on the current harmonic attenuation and the system stability. In particular, the *LCL* filter impedance (seen from the converter side) has been experimentally measured, showing an accurate matching with the analytical expectations and thus providing a preliminary validation of the attenuation capabilities of the filter. Then, the *LCL* filter has been tested together with an active rectifier prototype, to verify both the filter attenuation performance and the converter closed-loop current control stability. The current spectrum at full load has been shown to comply with the international technical standards, achieving results well within the prescribed limits, both for even and odd harmonics. The system stability has been finally verified with different values of grid impedance, emulating various grid point connections. Therefore, the proposed novel design methodology has been successfully validated.

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