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***Abstract*— Nanomagnet logic (NML) uses dipolar magnetic coupling between nanomagnets to efficiently perform non-volatile logical operations. As the basis logic element, the three-input minority gate, is the simplest threshold logic function, recent work has explored the potential for increased logical expressivity with a nanomagnet threshold logic family that reduces area, delay, and energy costs. However, as such previous work was limited to a single layer of nanomagnets, only negative input weights could be provided, thus limiting circuit expressivity and efficiency. This paper therefore proposes multilayer nanomagnet threshold logic systems that provide both positive and negative weights by leveraging multilayer structures that produce both ferromagnetic and anti-ferromagnetic dipolar coupling. The availability of both positive and negative weights drastically increase logical expressivity, and the feasibility of the proposed multilayer nanomagnet threshold logic system is demonstrated through micromagnetic simulations. A single seven-input gate is shown to perform more than 86 distinct logic functions, reducing the number of gates and clock cycles required for complex logic circuits by as much as 67%.**

***Index Terms*— Multilayer logic, nanomagnet logic, perpendicular magnets, threshold logic.**

I. Introduction

NANOMAGNET logic (NML) represents logical states with a nonvolatile magnetization [1], providing opportunities for in-memory computing that cannot be achieved with charge-based CMOS devices that require a power supply to maintain logical states. Each nanomagnet in an NML system is fabricated with two stable magnetic anisotropy directions that represent logical 1 and 0, allowing them to execute the Boolean logic operations by using their stray magnetic fields to influence nearby nanomagnets. While initial research on NML focused on in-plane magnetic anisotropy, the focus has recently shifted to perpendicular anisotropy due to its simpler clocking, superior scalability, and tolerance to process variations [2]. Analyses suggest that NML can achieve power efficiencies that outperform equivalent CMOS circuits [3].

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Conventional NML logic gates are composed of three input nanomagnets placed adjacent to an output nanomagnet in the same layer, with the resulting logic state of the output nanomagnet equivalent to the direction of the minority of the magnetic fields from the three input nanomagnets [4]. As this minority gate is a simple example of a threshold logic function, single-layer threshold NML has been shown to enable significant improvements in NML efficiency. Previous research has also found that NML devices with perpendicular anisotropy can be integrated into a monolithic 3D NML structure with additional input nanomagnets above or below the output nanomagnet [5] [6]. Furthermore, NML gates in multiple layers can be connected to one another by 3D vias, where the logic states propagate vertically [7].

This paper therefore leverages this 3D perpendicular NML in the context of threshold logic to propose 3D threshold NML gates that provide additional inputs above and below the output nanomagnet, and both positive and negative weights. With five inputs in the same layer as the output, one in the layer above the output, and one below, these seven input nanomagnets have four input configurations that enable 86 distinct logic functions to be realized by a single gate. 3D NML threshold logic circuits enhance the logical expressiveness of NML gates, and therefore improve circuit performance while decreasing area usage and energy consumption.

II. Background: Perpendicular Nanomagnet Logic

A. Structure and Signal Propagation

In perpendicular NML, information is encoded by each nanomagnet's magnetization vector, which is stable when perpendicular to the plane [8]. This behavior can be exhibited by magnetic materials such as CoPt that have large magneto-crystalline anisotropy [9]. As the perpendicular anisotropy is intrinsic to the crystal structure of the material, the easy axis of such nanomagnets does not depend on their shapes or sizes.

An artificial nucleation center (ANC) is defined on one of the sides of the nanomagnets as in Fig. 1(a), by either ion beam irradiation or by locally changing the thickness and shape of the material. The purpose of the ANC is to create asymmetric coupling among neighboring nanomagnets, with the ANC area having a weaker influence on neighboring nanomagnets. This ANC enables the propagation of logic signals as depicted in Fig. 1(b), where a single global sinusoidal magnetic field is applied to the circuit to cause signal propagation along a row of nanomagnets [10]. When the sum of the stray

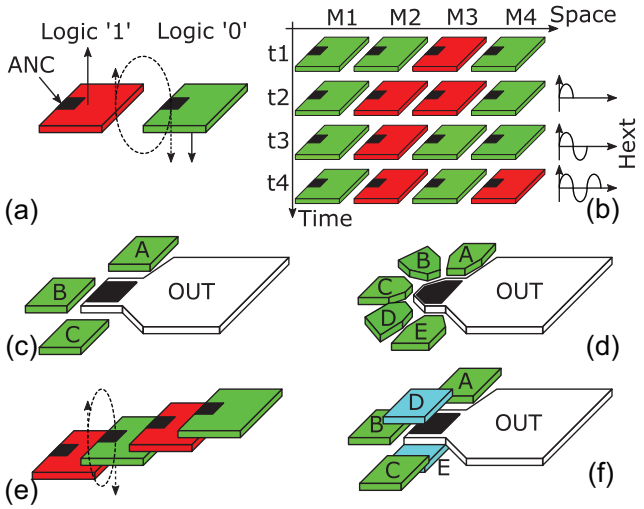

Fig. 1. (a) Nanomagnets with out-of-plane magnetization store the digital values '0' and '1'. ANCs provide asymmetric coupling among neighboring nanomagnets. (b) A sinusoidal global magnetic field is applied to propagate logic signals through the circuits. (c) A three-input minority gate is obtained through field-coupling among neighboring nanomagnets. (d) The number of inputs can be increased to perform multi-input threshold logic gates, such as a five-input minority gate. (e) Nanomagnets can be coupled vertically to create 3D logic circuits. (f) Five-input 3D NML gate with three input nanomagnets on the same plane as the output nanomagnet, one input nanomagnet above the output, and one input nanomagnet below the output.

field generated by neighboring nanomagnets and the global magnetic field is higher than the critical magnetization of the ANC, a nanomagnet switches state [11]. ANC fabricated with lower critical magnetization can further decrease the power consumption of external clock field.

B. pNML vs iNML

NML was originally designed with rectangular nanomagnets with in-plane anisotropy (iNML) resulting from the nanomagnet shape [2]. While NML has been experimentally demonstrated, fabrication imprecision and thermal noise create errors that inhibit the scaling of iNML to large systems [12], [13]. iNML is further challenged by the need for clock signals to periodically force specific regions of a circuit into an unstable state, increasing the complexity of the fabrication process as well as the circuit area and energy [14], [15].

The recent introduction of perpendicular magnetic anisotropy in pNML resolves important challenges facing iNML. As perpendicular anisotropy is a bulk effect independent of nanomagnet shape, it is significantly more tolerant to process variations [16]. The error rate is further reduced by avoiding the unstable iNML states, and pNML's use of a single global magnetic clocking field simplifies the fabrication process and enables efficiency improvements [17].

C. Single-Layer Nanomagnet Logic

Logic gates are formed by coupling neighboring nanomagnets, as shown in the conventional three-input minority logic gate of Fig. 1(c), where three input nanomagnets are placed around the nucleation center of an output nanomagnet. The output nanomagnet switches only if the output is equal to the minority of the inputs [18]. The concept can be extended by adding additional nanomagnets, as in the five-input minority gate of Fig. 1(d) [1] [19]. However, the number of inputs cannot be increased *ad infinitum*, as additional inputs require a decrease in nanomagnet size and/or increase in distance from the output, thereby reducing the coupling strength through which the input nanomagnets drive the output nanomagnet.

D. Single-Layer Nanomagnet Threshold Logic

Threshold logic sums the weights of multiple binary inputs and compares that to a predetermined threshold value [20]. If the threshold is surpassed, the output is '1'; otherwise, the output is '0'. Standard threshold logic functions can be represented mathematically as follows:

$$f(x_1, x_2, \ldots, x_n) = \begin{cases} 1, if \sum_{i=1}^{n} x_i w_i \geq T \\ 0, otherwise \end{cases} \quad (1)$$

where x_i are the binary inputs, w_i are the respective weights of the inputs, and T is the threshold. Each binary input, x_i, is multiplied by its weight, w_i; all of the weighted inputs, $x_i w_i$, are summed together and compared to the threshold. Threshold logic is advantageous as it permits the representation of complex Boolean logic with far fewer gates than required with conventional combinations of AND, OR, *etc*. For example, a three-input majority function of $f = x_1x_2 + x_2x_3 + x_1x_3$ would – with conventional CMOS logic – require three AND gates (to compute x_1 and x_2, x_2 and x_3, and x_1 and x_3) and two OR gates that compute the OR of the three results of the AND gates. This five-gate circuit can be reduced to a single three-input threshold logic gate with input weights of one and a threshold of two.

The minority function performed by conventional NML gates is the simplest threshold logic function: the threshold is -2 and each of the three inputs have weights of -1. Recently, threshold NML gates were proposed in which the nanomagnet sizes and the distances between the input nanomagnets and the output nanomagnet nucleation site were used to perform various threshold functions [1]. However, as all of the input nanomagnets provide stray magnetic fields opposite to the direction of the inputs, all of the inputs in such planar threshold NML gates necessarily provide negative weights; positive weights cannot be provided. Furthermore, the planar geometric structure of the system limits the number of inputs that can efficiently be applied. Solutions to overcome these limitations are proposed in section III.

E. Multi-Layer Nanomagnet Logic

Recent research has experimentally demonstrated that signals can be propagated vertically through nanomagnets on different layers [21], as shown in Fig. 1(e). It is therefore possible to perform 3D multi-layer NML with input nanomagnets on different planes. Fig. 1(f) depicts a five-input NML gate, where two inputs are placed on different planes. By exploiting this mechanism, it is possible to build logic gates with seven inputs. These logic gates have nearly the same area as gates with a lower number of inputs while implementing logical functions of significantly greater complexity.

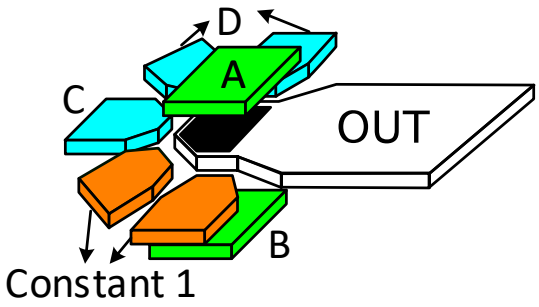

Fig. 2. Seven-input nanomagnet threshold logic gate. Two constant inputs (orange), single-weighted input C (blue), and double-weighted input D (blue) are in the same layer as the output. Inputs A and B (green) are placed above and below the ANC (black) of the output nanomagnet, respectively. This logic gate performs function No. 4 of Table I.

III. Multi-Layer Nanomagnet Threshold Logic

The ability to fabricate NML circuits in three dimensions enables efficient 3D threshold NML gates. Leveraging the high efficiency of threshold logic, this third dimension increases the number of input signals to each logic gate while also providing the critical capability of implementing both positive and negative weights.

Whereas the coupling between input and output nanomagnets in the same layer is anti-ferromagnetic (the magnetic field applied by the inputs on the outputs is in the direction opposite to the magnetization of the inputs), the ferromagnetic coupling between nanomagnets in different nanomagnet layers drives the output magnetization towards the same direction as the input magnetization. Therefore, while the in-plane interactions are represented as negative weights within threshold logic circuits, the vertical interactions across multiple layers are represented as positive weights. This ability to provide both negative and positive weights drastically increases the range and utility of the threshold functions performed by these multi-layer nanomagnet threshold logic gates.

Each input nanomagnet's weight, which is determined by the influence it has on the ANC, is a function of its size and its distance from the ANC. Two or more inputs can be connected to the same signal and be considered as the same input with an increased weight, broadening the range of logical expressiveness of the threshold system. Input nanomagnets can also be readily fabricated without the ANC area that fixes their magnetization in a manner that is not impacted by the clock and time-dependent behavior.

Nanomagnets in multi-layer NML can thus exhibit four distinct influences on an output nanomagnet: nanomagnets in the same layer provide anti-ferromagnetic coupling; input nanomagnets above or below the output provide ferromagnetic coupling; input nanomagnets with variable states provide time-dependent magnetic coupling; and input nanomagnets with fixed magnetization provide constant coupling. Input nanomagnets on the same plane as the output nanomagnet provide negative weights, while nanomagnets above or below the output provide positive weights. While the standard summation of the weighted inputs, $x_i w_i$, is performed, the threshold T is calculated as the minimum magnetic field to achieve positive magnetization of the output nanomagnet:

$$T = \frac{1 + \sum_{i=1}^{n} w_i}{2} \tag{2}$$

While the full range of threshold logic functions can be implemented by a continuous range of nanomagnet sizes and placements, uniform weights and sizes are preferred in order to ensure system robustness under practical fabrication limitations. While it may be possible to consider theoretical threshold gates with hundreds of inputs that performs millions of different functions, the precision required to implement such gates is not experimentally practical. This paper assumes a limitation of seven inputs as shown in the example of Fig. 2, where five input nanomagnets are in the same layer as the output nucleation site and two input nanomagnets are in different layers (one above and one below).

The use of up to seven inputs of four different types enables the computation of 86 distinct nanomagnet threshold logic functions. Several selected logic gates are included in Table I with reference to the magnet labels of Fig. 3. In this table, negative numbers indicate antiferromagnetic coupling from nanomagnets that are in the layer as the output, while positive numbers indicate ferromagnetic coupling from nanomagnets that are above or below the output. Numbers in constant column indicate constant inputs.

IV. Micromagnetic Simulation Results

A. Micromagnetic Geometry and Parameters

To verify the feasibility of implementing a 3D threshold nanomagnet logic gate, micromagnetic simulations of the structure of Fig. 3 have been performed via mumax[3] [22] with the CoPt parameters of Table II. The geometry is designed to ensure that all nanomagnets provide roughly equal dipolar coupling on the ANC, with maximum field magnitudes between 7 mT and 9 mT. As shown in Fig. 4, clocking is provided by a sinusoidal external magnetic field with a peak amplitude of 70 mT and period of 10 ns [1].

TABLE I
SELECTED NANOMAGNET THRESHOLD LOGIC FUNCTIONS

Function #	Logic Function	Threshold	Input Weight					Magnets						
			A	B	C	D	Constant	M1	M2	M3	M4	M5	M6	M7
1	(ABC)'=NAND3	0	-1	-1	-1		2	A	B	C	0	0		
2	C'+AB'	0	1	-1	-3		2	B	C	C	C	1	A	0
3	(A+B+C+D)'=NOR4	-3	-1	-1	-1	-1	-3	A	B	C	D	0	1	1
4	(BC'+AC'+AB)D'	-1	1	1	-1	-2	-2	D	D	C	1	1	A	B

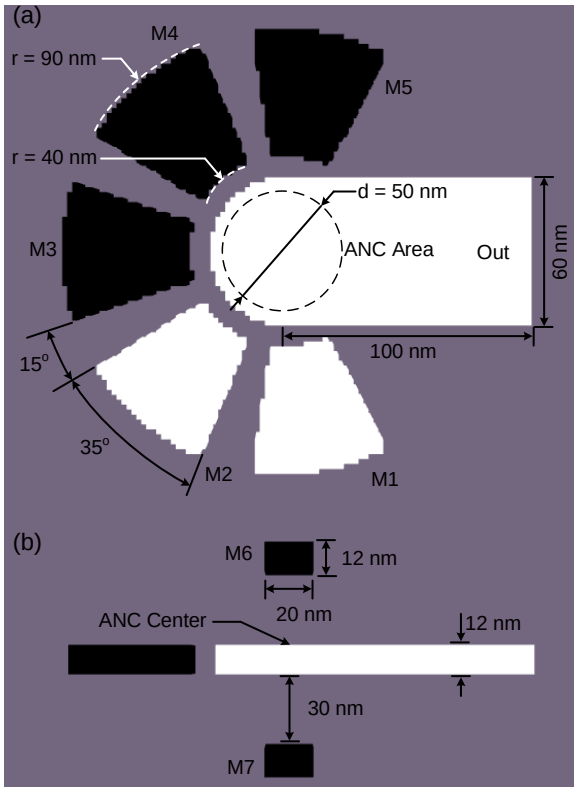

Fig. 3. Dimension parameters of the Mumax³ simulation structure. (a) Top view. (b) Side view. M1-M7 represents the label of each input magnet.

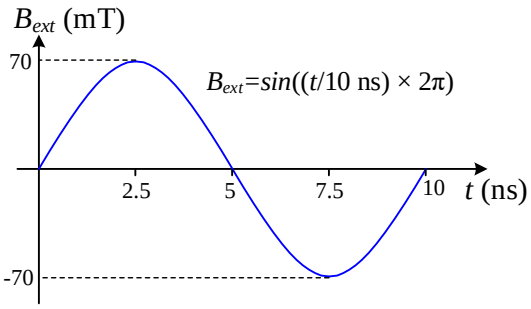

Fig. 4. Sinusoidal external magnetic field.

TABLE II
MICROMAGNETIC SIMULATION PARAMETERS

Parameters	Value
Saturation magnetization (Ms)	7.23×10^5 A/m
Exchange stiffness (Aex)	1.3×10^{-11} J/m
Damping constant (alpha)	0.5
Uniaxial anisotropy (Ku)	3.6×10^5 J/m^3
ANC uniaxial anisotropy (Ku)	1.45×10^5 J/m^3
Temperature (T)	300 K
Cell size	$2 \times 2 \times 2$ nm^3

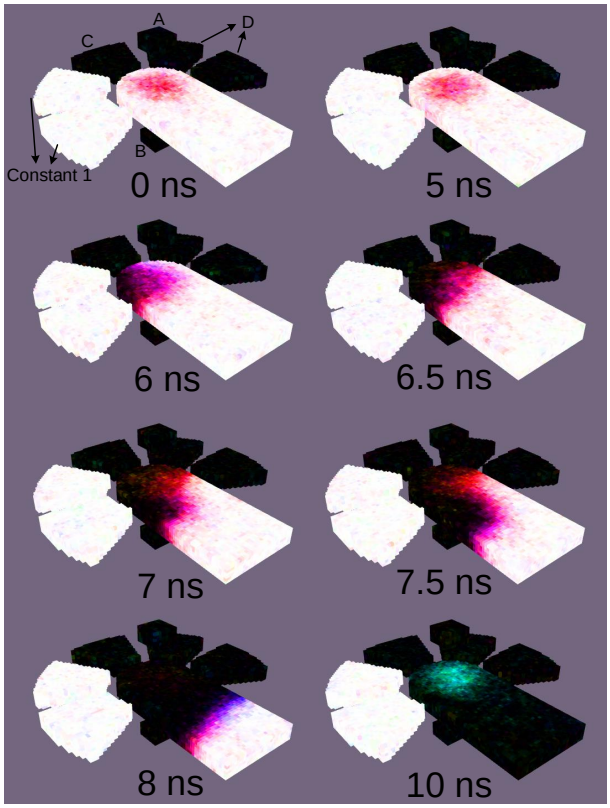

Fig. 5. Simulation results for No. 4 gate in Table I with logical input A = 0, B = 0, C = 0, D = 0 with clock cycle of 10 ns. To verify robustness to thermal noise, this simulation was performed at 300 K with ten different thermal seeds, achieving similar results in each run.

B. Micromagnetic Simulation Results

To demonstrate the functionality of this seven-input nanomagnet threshold logic gate, function No. 4 of Table I has been selected for micromagnetic simulations, as it contains all four types of influences: ferromagnetic coupling, antiferromagnetic coupling, fixed input signals, and time-dependent input signals. The most challenging switching condition, with the weighted sum of the inputs one below the logic gate threshold, is described below.

This condition is shown in the simulation of Fig. 5, where all four of the binary input signals provided by the five input nanomagnets have negative magnetization (black) representing binary 0, while the two fixed nanomagnets have positive magnetization (white) representing binary 1. Three of the nanomagnets in the same layer as the output nanomagnet have negative magnetization, thereby providing dipolar coupling on the output nanomagnet in the positive direction. The remaining four nanomagnets provide dipolar coupling on the output nanomagnet in the negative direction. The output nanomagnet therefore switches from the positive to the negative direction, as the weighted sum of the input and fixed signals (-2) is less than the threshold of this logic gate (-1).

As seen in Fig. 5, the magnetization of the output nanomagnet is unchanged in the first half of the clock cycle (0-5 ns), as the sinusoidal external clocking magnetic field is working against the majority of the input nanomagnets. As the external magnetic field is in the negative direction during the second half of the clock cycle (5-10 ns), the combination of this clock field and the dipolar coupling from the input nanomagnets is sufficient to overcome the coercivity of the output nanomagnet. The switching initiates at the ANC, and gradually propagates through the entire output nanomagnet via domain wall motion.

The propagation of the magnetic domain wall through the

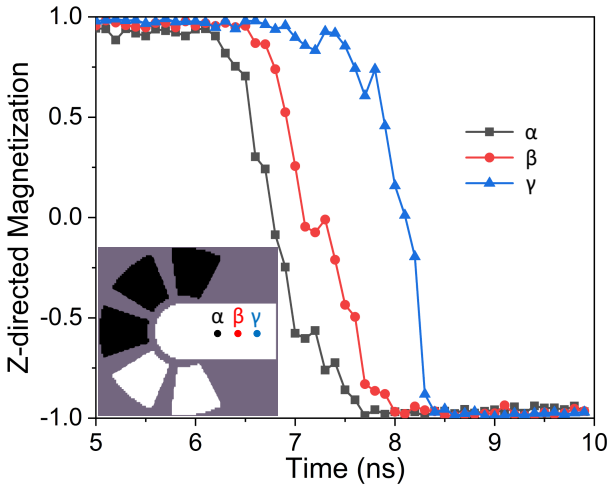

Fig. 6. Domain wall propagation through the output nanomagnet.

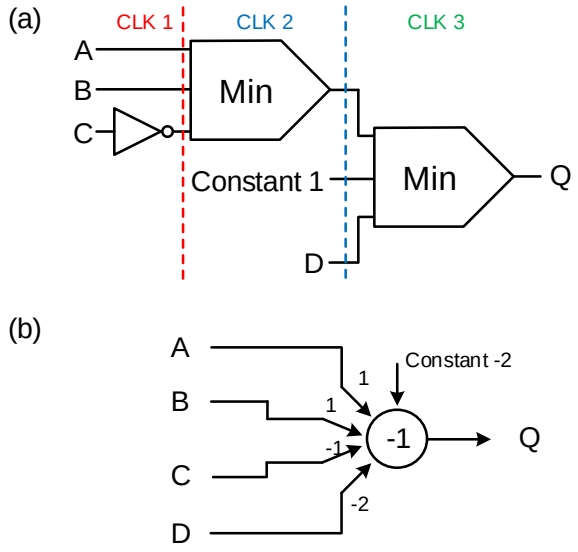

Fig. 7. Logic function #4 of Table I implemented by (a) single-layer threshold nanomagnet logic and (b) multi-layer threshold nanomagnet logic.

output nanomagnet is illustrated in Fig. 6 by tracking the magnetization of three points (α, β, γ) located at regular intervals from the ANC. As the output nanomagnet initially has positive magnetization and switches negative, the z-directed magnetization of each point switches from +1 to -1. α, the point closest to the ANC, can be seen to first have a change in magnetization at roughly 6.5 ns, followed by β at roughly 6.75 ns, and γ at roughly 7.5 ns. By the end of the clock cycle at 10 ns, all three points have completed their magnetization reversal and reached stable non-volatile states.

V. Computational Efficiency

As threshold logic enables complex logical operations by each logic gate, the high expressiveness of this multi-layer nanomagnet threshold logic family enables enormous reductions in circuit area, delay, and energy. The additional inputs further increase the logical expressiveness, while the use of multiple layers intrinsically enables both positive and negative weights, thereby enabling signal inversion without an inverter gate. When used in clocked perpendicular NML, inversion requires a complete clock cycle.

This multi-layer nanomagnet threshold logic family therefore enables significant reductions in the number of logic gates required to perform logical expressions. As each logic gate in perpendicular nanomagnet logic requires a clock cycle for switching [16], this reduction in gate count results in significant reductions in delay and energy consumption.

As illustrative examples, this section demonstrates the reductions in area and clock periods achieved by multi-layer nanomagnet threshold logic for logic function No. 4 of Table I and a 4-to-1 multiplexer. In comparison to single-layer nanomagnet threshold logic, the number of gates can be reduced by 67% and 62%, respectively, while the number of clock cycles can be reduced by 67% and 60%, respectively. Similar reductions can be achieved for other logic gates, with this multi-layer structure providing increasing advantages as the complexity of logic functions increase. For larger circuits with effective logic synthesis, gate count and clock cycle reductions greater than 70% are expected. In addition to improving the efficiency of non-volatile logic circuits, these highly-expressive threshold gates are intriguing for neuromorphic computing with non-volatile threshold functions [23].

A. Minority-NOR Gate

Fig. 7 illustrates the threshold nanomagnet logic circuit required to perform minority-NOR logic function No. 4 of Table I using both single- and multi-layer nanomagnet threshold logic. As can be readily observed in the figure, the single-layer circuit requires two additional logic gates due to its inability to provide both positive and negative weights. The additional inverter require additional clock cycle. In total, the single-layer structure requires three logic gates and three clock cycles (divided by dashed lines), while the multi-layer structure requires only one of each.

B. 4-to-1 Multiplexer

The 4-to-1 multiplexers of Fig. 8 also exemplify the hardware reductions that can be achieved with multi-layer threshold nanomagnet logic. As discussed previously, the availability of both positive and negative weights enables the circuit of Fig. 8(b) to circumvent the need for dedicated inverter gates to perform the inversion intrinsic to the logical multiplexing function. Multi-layer threshold nanomagnet logic thus permits the realization of the 4-to-1 multiplexer with five gates in two stages, while the single-layer structure requires 13 gates in five stages (divided by dashed lines).

VI. Conclusion

This paper proposes threshold logic with multiple nanomagnet layers in order to provide both positive and negative input weights. This advance enables a drastic increase in the logical expressivity of each gate, as a single seven-input gate can perform 86 distinct logic functions. This functionality is thoroughly demonstrated via micromagnetic simulation, and

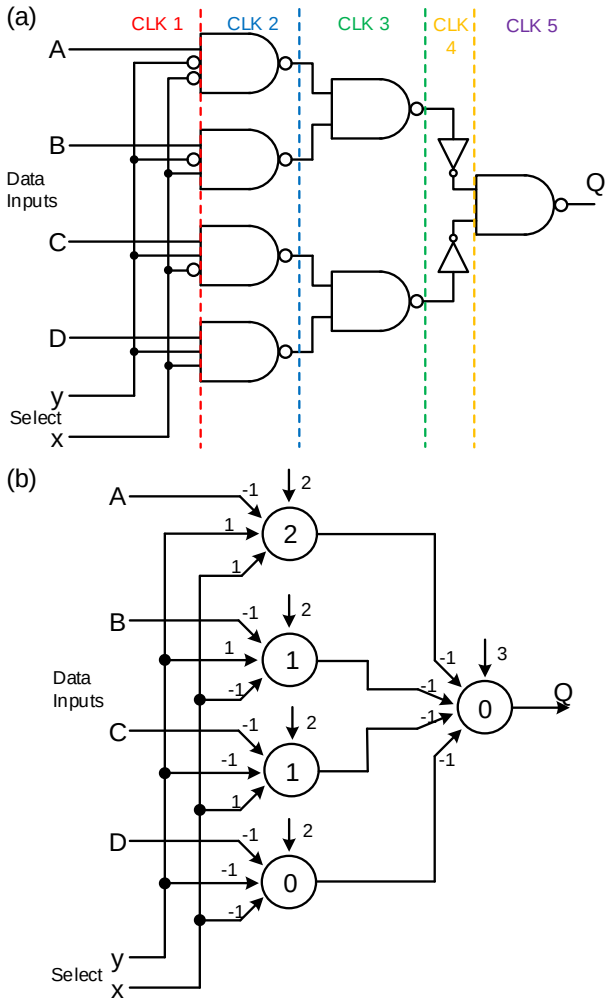

Fig. 8. 4-to-1 multiplexer implemented by (a) single-layer threshold nanomagnet logic and (b) multi-layer threshold nanomagnet logic.

the circuit- and system-level benefits are explored. In particular, this multilayer nanomagnet threshold logic system can improve the gate count and number of clock cycles required for complex logic operations by a factor of three, thus greatly increasing the ability of logic systems based on nanomagnets to enable a future generation of energy-efficient non-volatile computing systems. Additionally, the simulation results also show the potential of optimizing and increasing the number of inputs which will further improve the functionality and flexibility of the NML threshold gate.

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