Estimation of the Internal Junction Temperatures of Resin Encapsulated IGBT Power Modules

Estimation of the Internal Junction Temperatures of Resin Encapsulated IGBT Power Modules

Matteo Gregorio, Fausto Stella, Radu Bojoi
Dipartimento Energia 'Galileo Ferraris'
Politecnico di Torino, Italy
matteo.gregorio@polito.it, fausto.stella@polito.it
radu.bojoi@polito.it

Fabio Pagani
Prima Electro S.p.a.
Moncalieri, Italy
fabio.pagani@primaelectro.com

***Abstract*—Power electronics converters used in applications requiring high reliability require an accurate thermal management for each component. Therefore, several methods for the estimation of the junction temperature of power devices are reported in the literature, having different features in terms of sensitivity, linearity and calibration process. Nevertheless, state of the art technologies in power modules packaging, such as the resin encapsulation technology, have shown that junction temperature estimation is still an open issue. In such modules, the lack of physical access to the die has led a growing interest in estimation methods based on thermo-sensitive electrical parameters. This paper proposes a non-invasive method for the junction temperature estimation of high current resin encapsulated IGBT power modules. The proposed solution is suitable for the thermal model validation of industrial converters thanks to the off-the-shelf components and the easiness of implementation.**

***Index Terms*—Junction temperature monitoring, thermo-sensitive electrical parameters (TSEP), on-state voltage, IGBT.**

I. Introduction

Nowadays, power electronic converters are widely used in industry and emerging applications, such as transportation electrification, more-electric-aircraft and energy production from renewable energy sources. High efficiency, high reliability and high power density solutions require a proper thermal management at both system and component levels [1], [2]. Consequently, many attempts have been made by power modules manufacturers to develop packaging techniques able to mitigate the failure mechanisms [3], [4]. For instance, the direct potting resin encapsulation and the insulated metal baseplate (IMS) technology offers an enhanced thermal cycling capability due to a closest coefficient of thermal expansion between the copper and the resin isolator [5]. By contrast, the presence of the solid resin makes the dies inaccessible for most of the methods for the junction temperature measurement.

The knowledge of the junction temperature is crucial for the thermal management of the power electronics and therefore it has to be measured or estimated during both prototyping and final working conditions. Several methods for the junction temperature measurement [6] are well known in both literature and industry and the most suitable solution depends specifically on the required needs.

As the most common way to measure a temperature is to use thermistors or thermocouple, the manufacturers usually integrate thermistors as NTC or PTC inside the power modules. However, this solution provides a measure that can be far from the real junction temperature of each switch inside a module, due to the remoteness of the thermistor respect to the switches.

A possible alternative is to predict the junction temperature using thermal models provided by the manufacturers in datasheet [7]. However, these thermal models are often inaccurate since they refer to a single switch in the module and do not take into account the thermal coupling between the devices inside the module. Furthermore, these parameters are usually too conservative, leading to an overestimation of the junction temperature. Improved thermal models like the ones presented in [8]–[11] can be used to overcome the above limits. Conversely, these models rely either on numerical methods to solve thermal problems, as finite-element simulation (FEA), or to experimental characterization. In the former case, a comprehensive knowledge of the power module in terms of layout, material composition and dimensions, is essential. However, all these parameters are not always available. In the latter case, a dedicated test rig is mandatory to characterize the thermal impedance of each device at a time. In both procedures, the output is a matrix of impedance that correlates the losses with the junction temperature and its dimension depends on the number of devices.

Therefore, a method to estimate every junction temperature of a power module is of great interest especially for thermal characterization, real time estimation and prognostic [3], [12], [13]. Many solutions have been presented in literature [6], such as optical methods, physical contact methods and electrical methods.

Optical methods [14] are based on sensors such as optical fibers and infra-red camera. The infra-red camera can provide a temperature map of the whole module and therefore can detect both the hot spot and the average temperature of each die, and the spatial resolution is high. In contrast, the optical fibers can detect the temperature of a low spatial region and so in presence of large surface die area they provide a punctual value that is no longer the average of the switch. However, in both solutions the dielectric gel inside the module has to be removed as the die must be seen by the optical sensor. Therefore, high voltage operation is not guaranteed anymore. For this reason, the optical methods fit well during prototyping

phase but cannot be adopted for real time estimation in real operating conditions.

Physical contact methods [15] use sensors as thermocouples applied directly on the die surface. Despite their good precision, it is not trivial to guarantee the electrical insulation between the dies and the sensor while ensuring a good thermal coupling. As the introduction of the thermal sensor can strongly affect the reliability of the power device, this solution is usually avoided.

Electrical methods take advantage of the component itself by exploiting the correlations among the junction temperature and the thermo-sensitive electrical parameters (TSEPs) [16] as the on-state voltage, the internal gate resistor R_{Gi} [17], the saturation voltage $V_{CE,sat}$ [18], and the threshold voltage V_{TH}. Thereby, the junction temperature estimation is simply performed using voltage and current probes, without intrusive modifications inside the module. However, the electrical methods have some drawbacks. As example, the estimated temperature represents the area average value inside the die [19] and therefore no information about the peak temperature can be extracted. Moreover, for high current devices consisting of paralleled dies, there is no chance to assess the temperature distribution among them. Depending on the adopted TSEPs, there are strong variations in terms of linearity, sensitivity, calibration process and easiness of implementation. Despite of their drawbacks, the electrical methods represent an attractive solution for industrial applications, where the optical and physical contact methods are often impracticable.

The auxiliary circuitry required for the junction temperature estimation can be included directly into the gate driver stage, thus the online estimation can be performed both during prototyping phase and final working conditions. Besides that, prognostic analysis of the power module can be carried out [20].

In the literature, several solutions about the integration of the sensing circuitry in the gate driver of the converter are reported [21]–[23]. Conversely, if the online temperature estimation is not essential, the auxiliary circuitry can be an external component plugged into the converter as an add-on, for instance during prototyping. This approach allows to validate the thermal management of the resin encapsulated power modules where the dies are not accessible.

It is worth noticing that both approaches share the same supplemental circuitry and estimating methodology.

The aim of the paper is to propose a test procedure for the junction temperature estimation of IGBT resin encapsulated modules employed in industrial converters without integrated sensing circuitry inside the module. The temperature estimation is based on the on-state collector-emitter voltage detection using a compact external board, under high current conditions. Thereby, the junction temperature can be estimated during the converter operations and so the module thermal management can be validated during prototyping [24]. As previously stated, if the on-state sensing circuitry is embedded in the gate driver stage, the temperature estimation can be extended to online estimation and prognostics analysis.

The paper is organized as follows: *Section II* describes the reference hardware adopted in the paper and introduces the fundamental steps for the junction temperature estimation (calibration, data analysis and estimation). *Section III* describes the calibration process, *Section IV* defines how the results of the calibration process are manipulated to obtain a reverse look-up table while *Section V* shows some experimental results obtained with an IGBT module. *Section VI* present the conclusion of the paper.

II. Reference Setup

In this paper, an industrial three-phase IGBT converter has been taken as reference. The main features of the converter are listed in Table. Ia and Table. Ib.

TABLE I: Converter and module ratings.

(a)

Converter		
S_{nom}	68	kVA
V_n	400	V_{rms}
f_{sw}	4	kHz

(b)

Module		
V_{CES}	1200	V
I_C	200	A
V_{GES}	±20	V
T_{Jop}	-40 to +150	$^{\circ}C$
$V_{CE,sat}$	2.00	V

The proposed methodology has been implemented on a standard IGBT power module filled with insulating gel. A second power module identical to the first but without the insulating gel has been used to validate the proposed solution using a thermal camera.

As shown in Fig. 1, the proposed procedure involves three different steps: calibration, data analysis and temperature estimation. All these steps can be performed for any industrial inverter with no need of dedicated gate drivers and other integrated sensing devices, making the proposed procedure very attractive for industry. In the following section all steps are described.

III. Calibration Process

The aim of the calibration process is the extraction of the $V_{CE,i}$ ($I_{C,i}$,$T_{j,i}$) maps, where $V_{CE,i}$, $I_{C,i}$ and $T_{J,i}$ are respectively the ON-state voltage, the current and the junction temperature of the i-th IGBT.

The calibration process is performed directly on the 3-phase power converter embedding the power module under test (MUT). The converter load is a dedicated three-phase inductor and the ON-state voltages V_{CE} and the gate-emitter voltages V_{GE} of the devices are measured with six external boards communicating with a DSP controller board, as shown in Fig. 2(a).

The calibration process consists of a sequence of current ramps flowing into two devices at a time, so at different heatsink temperatures the full module can be characterized with three pulses. Fig. 3 shows the switches sequence during the calibration process.

As depicted in Fig. 4, it is worth noticing that the ascending part of the current ramp allows the IGBTs characterization

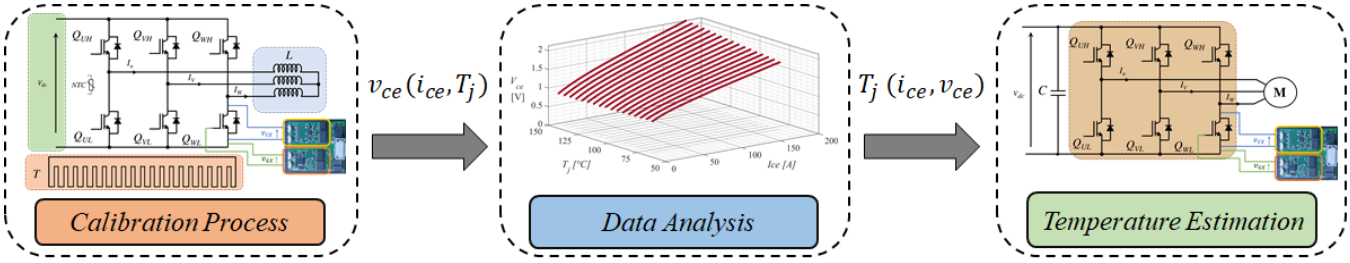

Fig. 1: Steps for the junction temperature estimation: calibration, data analysis and temperature estimation.

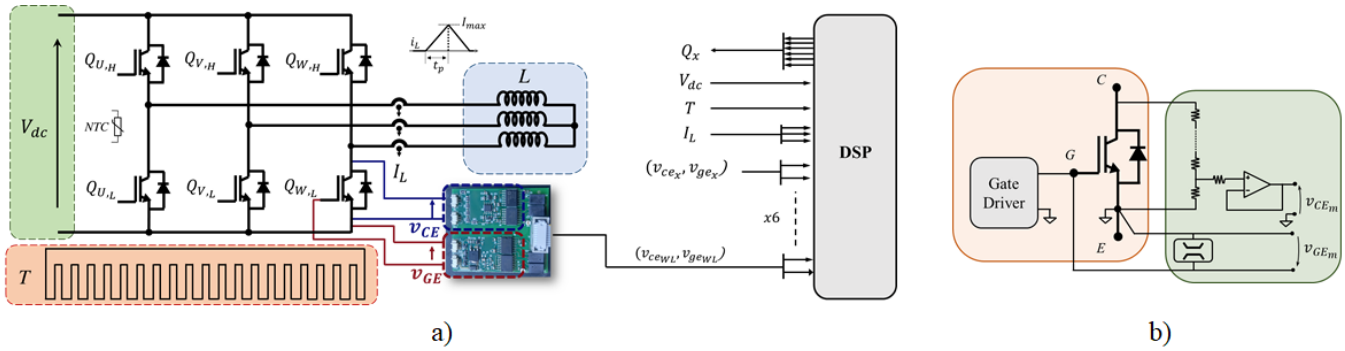

Fig. 2: (a) Proposed calibration setup, (b) ON-state acquisition circuitry.

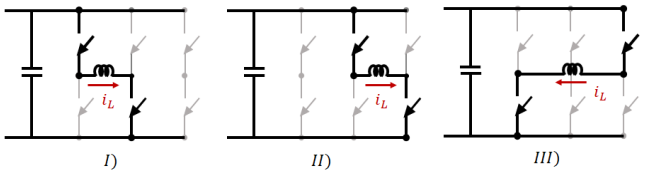

Fig. 3: Schematics of current pulses.

while the descending parts their relatives FWDs. Given the ramp time t_p, the peak current ramp value I_{max} depends on the input supply voltage V_{dc} and the inductance value L. The V_{dc} and L shall be properly selected according to specific criteria illustrated in the following section.

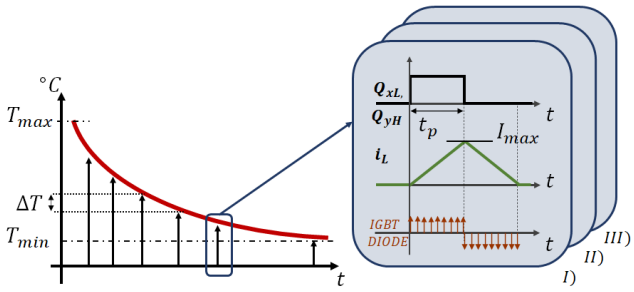

Fig. 4: Schematics of the testing procedure.

The calibration process can be summarized in the following steps:

1) *Heating Phase:* The heat-sink is heated up until the maximum temperature needed is reached
2) *Current Ramp Phase:* A current ramp is set for each device of the MUT, so $V_{CE,i}$,$I_{C,i}$ can be measured
3) *Cooling Phase:* the heat-sink is cooled down to the following target temperature

Steps 2 and 3 are repeated until the lowest target temperature is reached.

The main challenges of the current ramp phase are the ON-state voltages and temperatures measurement. A further issue is introduced by the MUT internal layout since their parasitic resistances and inductances impose strict constraints during the current ramp phase. Therefore, the ON-state voltages measurement, the temperatures measurement, the MUT internal layout effect and the data results of the calibration process are described in detail in the following parts of the paper.

A. ON-State Measurement

The ON-state voltage sensitivity of IGBTs is in the range of -1 to +4 mV/°C and depends strongly on the current value [25]. Due to the low voltage sensitivity, the most critical task is the design of the V_{CE} measurement circuitry. The system has to be able to measure properly very low voltages with a resolution of millivolts while protecting itself against the DC-link voltage during the device OFF-state. For these reasons, several solutions have been proposed in literature specifically for IGBTs or MOSFETs [26]–[31]. According to the requirements of each application, the V_{CE} monitoring should be select considering the minimum resolution needed, the measuring range, the maximum sample rate and the bandwidth.

The adopted measurement circuit is shown in Fig. 2(b) and consist of a voltage divider and an operational amplifier. The benefits are the extremely simple structure, that requires few

additional components, and the mitigation of the uncertainty due to the presence of the clamping circuitry during the ON-state period. In contrast, the output signal is more susceptible to noise due to the low voltage signal coming from the resistor divider. This solution permits to measure both the V_{CE} and the forward voltage V_D of the FWD.

The measuring circuit has the following ratings: measuring range ±3.7V, 16-bit resolution, 1.5MSa/s, 15µs of maximum delay. The delay is the interval of time between the turn-on transition of the IGBT and the steady-state value of the corresponding digital output signal. The delay is introduced by the acquisition circuitry and is consistent with the industrial low switching frequency converters wherein the switching period can be several hundreds of microseconds.

The gate voltage level strongly affects the device ON-state characteristics hence V_{GE} is measured. In order to ensure a constant V_{GE} during all working conditions, a gate voltage clamp circuitry is integrated in the measuring board. Moreover the clamping voltage is adjustable thus the MUT can be characterized under different V_{GE}.

B. Temperature Measurement

The accuracy of the junction temperature estimation process is strongly dependent on the temperature measurement during the calibration process. Therefore, a homogeneous temperature distribution inside the MUT and a limited IGBT self-overheating during the current pulses must be both ensured.

The homogeneous temperature distribution is guaranteed by a slow heating phase of the heatsink. As a result, the NTC inside the module is representative of all IGBTs [22]. Furthermore, three thermocouples are placed under the baseplate in correspondence of the three dies to track temperature during the whole calibration process.

The self-overheating must be evaluated a priori using the thermal model provided in the datasheet. During the current ramp only the conduction loss term contributes to the losses so it can be easily estimated. The maximum over heating depends on the peak current I_{max} and the pulse length t_P. For this reason, t_P must be selected in order to limit the overheating below the required threshold. The worst-case condition corresponds to the maximum conduction losses, when the IGBTs are at the maximum junction temperature. For instance, the maximum self-overheating of the MUT at $T_J = 150\ °C$ and characterized with pulses of $t_P = 500\mu s$ and $I_{max} = 200A$, is lower than $1°C$.

C. Module Layout

The internal module layout may affect the temperature estimation. The module lead resistance indicated in the datasheet includes the bonding wire, the DBC copper and the terminal resistances for a single switch. The lead resistance has a non-negligible value and can affect the ON-state voltage measurement mainly at high current. Moreover, during the converter working condition the die temperature may be extremely different from the bonding wires and the terminals, leading to an inaccurate temperature estimation [25]. This limitation

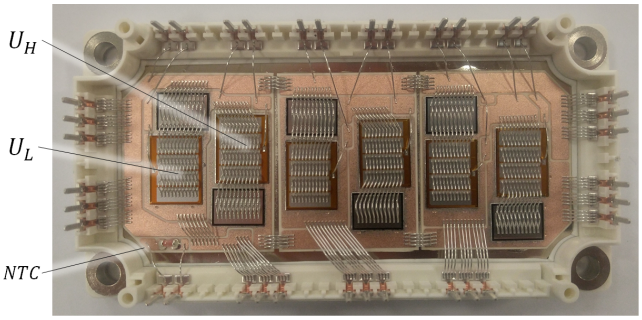

Fig. 5: Module under test (MUT).

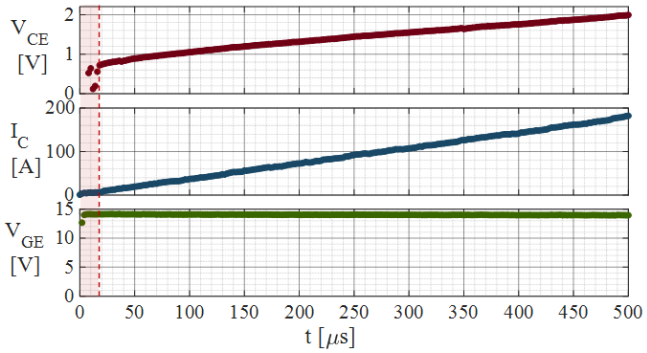

Fig. 6: Acquisition signals at $115°C$: from the top the voltage V_{CE}, the current I_C and the voltage V_{GE}.

can be overcome if the sensing terminals are present (e.g. the Kelvin terminal) that can reduce the path shared by the sensing circuitry and the power traces.

Fig. 5 shows the MUT. The low-side switches present both collector and emitter signal terminals so the effect of the lead resistance is sharply reduced, while the collector connection of the high-side switches is the power terminal of the DC-link upper rail.

Similarly, the stray inductance introduces an offset in the voltage measurement that is proportional to the $\frac{di}{dt}$. This effect can be meaningful during the calibration process whereas during the temperature estimation process may have less influence in case of a low current ripple.

In conclusion, the power module layout has a non-negligible effect on the junction temperature estimation process and it cannot be easily evaluated. The pulse period t_P should be selected as a tradeoff between the self-overheating of the device and the offset in the voltage measurements.

D. Results of the Calibration Process

The experimental results obtained for a single device are shown in Fig. 6. The variables are acquired with a timescale of 2µs. The first samples are not considered to eliminate the influence of the oscillation produced by the switching transients. Fig. 7 shows the results obtained for a single device where the calibration has been performed from $150°C$ to $50°C$.

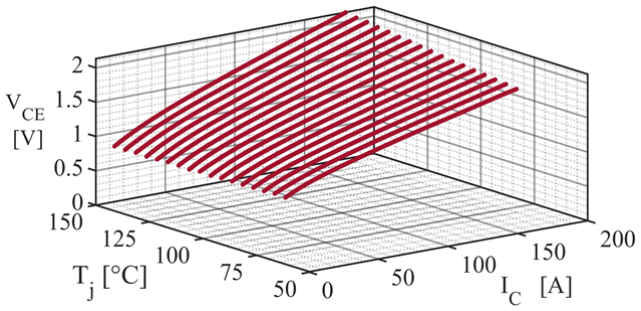

Fig. 7: The V_{CE} map for low side IGBT.

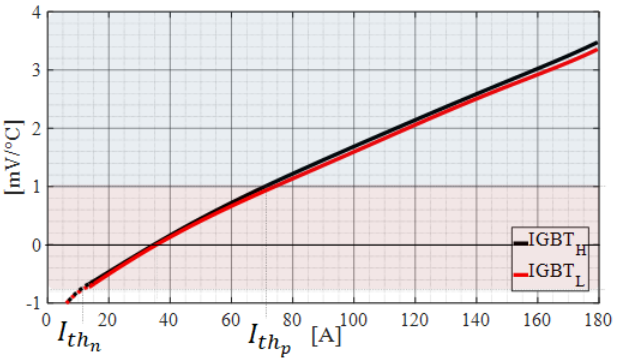

Fig. 8: Average sensitivity curve for high-side and low-side IGBTs.

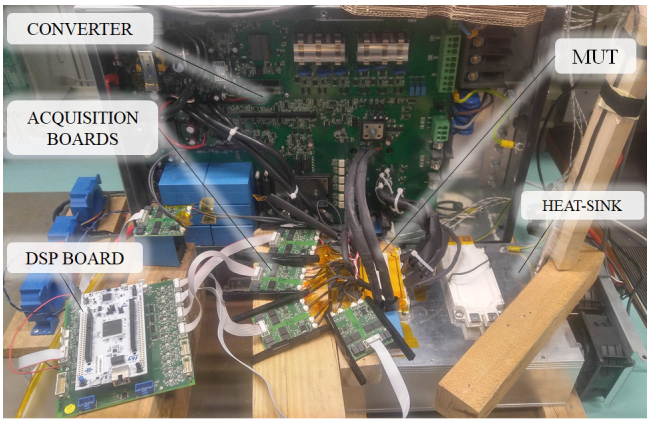

Fig. 9: Experimental setup.

IV. Data Analysis

The $V_{CE}(I_C, T_J)$ maps derived by the calibration process must be elaborated to obtain the $T_J(V_{CE}, I_C)$ look-up tables that can be used in a real application.

Thanks to the high frequency sampling rate, the raw data can be interpolated in order to reduce the measurement noise, then the sensitivity analysis is performed. As expected, for the ON-state characteristic there is a specific current value I_C at which the temperature coefficient changes its sign. This is reflected in the sensitivity curves for low side IGBT and high side IGBT that are shown in Fig. 8. It must be underlined here that the points for current values below $10A$ are not considered and they correspond to the first samples that are excluded in Fig. 6.

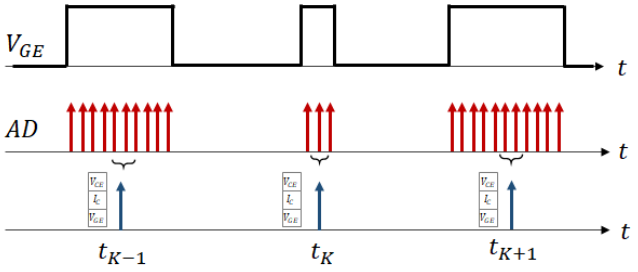

Fig. 10: Acquisition process.

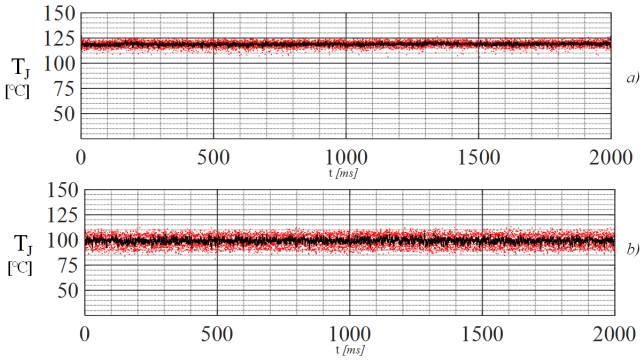

Fig. 11: Experimental results under DC load current condition. a) Estimated junction temperature at $130A$, istantaneous (red) and filtered at 200Hz (black). b) Estimated junction temperature at $85A$, istantaneous (red) and filtered at 200Hz (black).

The current range between the negative threshold $I_{th,N}$ and the positive threshold $I_{th,P}$ has sensitivity close to zero, while for higher current values the sensitivity increases. It is worth noticing that $I_{th,P}$ is correlated to the resolution of the ON-state measurements, higher voltage resolution sensing allows a lower threshold current $I_{th,P}$ and therefore an extended temperature estimation range.

Finally, a look-up table is extracted for each IGBT.

V. Temperature Estimation

The junction temperature estimation is carried out with the testing configuration shown in Fig. 9. The MUT and the heat-sink are detached from the converter board in order to provide an access to the dies, therefore the estimated temperature can be compared to the physical contact methods or optical methods. A MUT without dielectric gel has been selected, the dies have been painted, and their emissivity has been calibrated. The MUT is controlled by the converter board and the acquisition boards sample the currents and the voltages across the devices that will be used for the offline temperature estimation. The sampling process starts whenever each acquisition board detects a rising edge in the gate voltage and lasts until the falling edge, as depicted in Fig. 10. In this time interval, the V_{CE},I_C and V_{GE} signals are acquired with a timescale of $2\mu s$, and the junction temperature estimation is performed by using the middle samples that correspond to the positive and negative vertices of the PWM carrier. Thereby, the measuring circuit can reach its steady-state and none switching

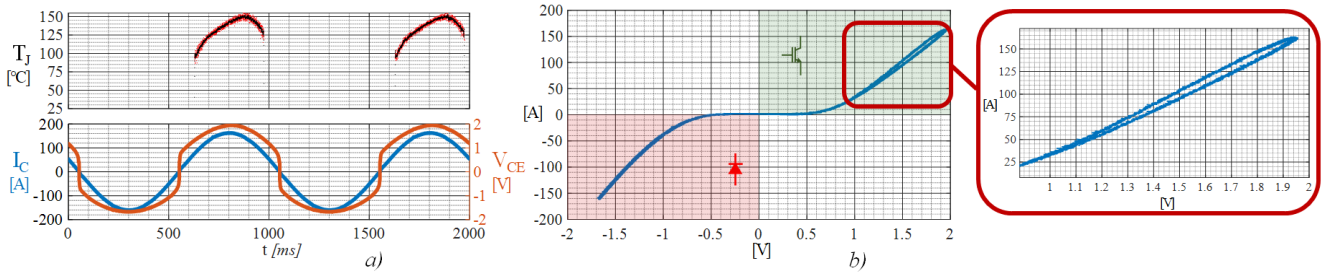

Fig. 12: Experimental results under sinusoidal load current condition of $160A_{pk}$ and f = 1Hz: a) Top: estimated junction temperature, istantaneous (red) and filtered at 200Hz (black). Bottom: V_{CE} and I_C. b) Forward characteristic of the IGBT and FWD.

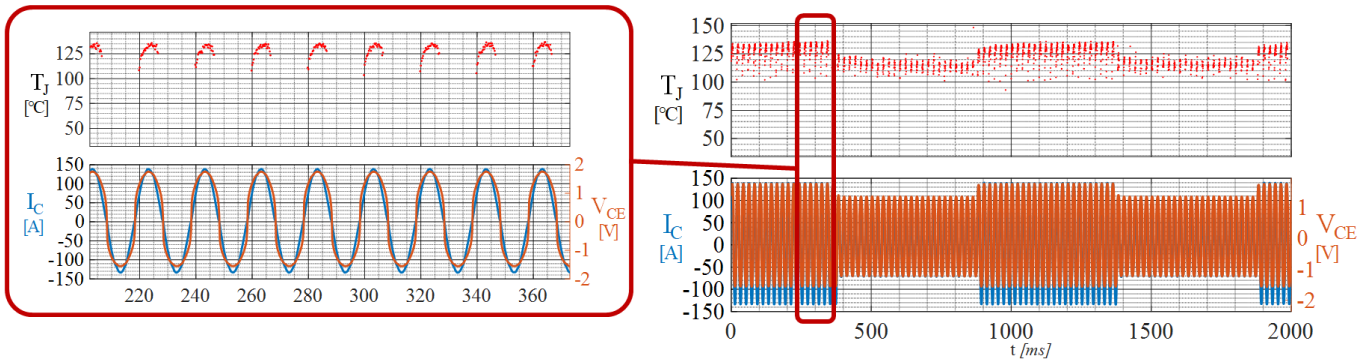

Fig. 13: AC cycle load current condition from $160A_{pk}$ to $70A_{pk}$, f = 50Hz. Top: estimated junction temperature. Bottom: V_{CE} and I_C.

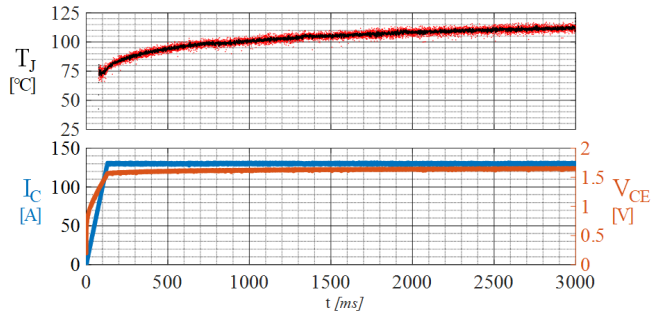

Fig. 14: Experimental results under DC load current condition of $130A$. Top: estimated junction temperature, istantaneous (red) and filtered at 200Hz (black). Bottom: V_{CE} and I_C.

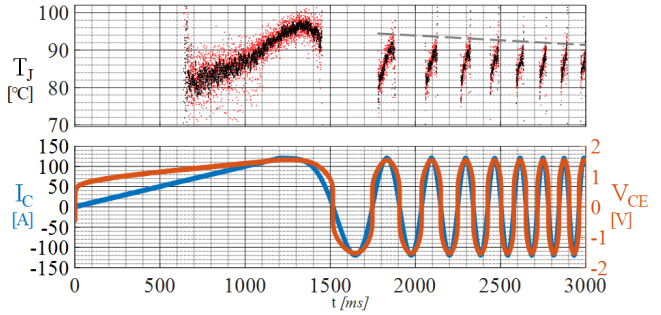

Fig. 15: I/f control with $130A_{pk}$. Top: the estimated IGBT junction temperature, the istantaneous (red) and filtered at 200Hz (black). Bottom: the V_{CE} and the I_C.

transient occurs during these samples. The outcome of this process is a signal sampled at the switching frequency.

The whole process has been validated by imposing a DC current and by comparing the estimated temperature with the average surface temperature measured with a thermal camera. Fig. 11 shows the estimated temperature at high (a) and low (b) DC currents. It is worth noticing that the junction temperature is affected by a noise that depends on the current value according to the sensitivity curves of Fig. 8. The instantaneous junction temperature presents a noise limited within $\pm 10°C$ of range at $85A$ of output current and it shrinks to $\pm 5°C$ when the current rises to $130A$.

The estimated junction temperature of a device under low frequency operating point is shown in Fig. 12(a). As expected, the temperature is available only in a limited interval of time when the output current is higher than the minimum threshold $I_{th,P}$, thus the peak temperature can be estimated while no information about its minimum can be drawn. Although the maximum power losses in the IGBT is in correspondence of the peak current, the peak junction temperature is delayed with respect to the current and is due to the MUT thermal impedance. Fig. 12(b) shows the ON-state characteristic. The first quadrant exhibits a hysteresis phenomenon explainable by the self-heating of the IGBT, while the third quadrant shows the forward characteristic of the FWD. Accordingly, the system is able to measure properly the forward voltage of the FWDs and may be adopted for the estimation of the diode junction temperature.

The transient and the steady state thermal models of the MUT can be evaluated during the prototyping phase. Fig. 13 shows the estimated junction temperature under DC load condition of $130A$. In Fig. 14 the junction temperature is estimated for an AC ($50Hz$) current during a load cycle of period $1s$. Thanks to the high sample rate (at the switching frequency) the system is able to estimate the temperature during both the fundamental frequency ($50Hz$) and the load cycle ($1Hz$).

The response of a I/f control is shown in Fig. 15. The maximum temperature and the cycle span exhibit a slight decrease with the raising of the frequency, due to the thermal impedance of the MUT.

VI. Conclusion

The paper proposes a methodology for the junction temperature estimation of IGBT modules. The proposed methodology can be used to validate the thermal models of resin encapsulated power modules during the prototyping. The estimated junction temperature is available only at high current condition and provides insight about the average temperature of the dies. Nevertheless, these limits do not affect the value of the proposed methodology since the thermal module management needs to be validated at the worst-case operating conditions. The easiness of implementation and the limited additional hardware makes this solution suitable for industrial applications and when the direct junction temperature measurement is unfeasible. The complete process is described from the calibration step, the data analysis, and the estimation phase. The results are provided with a three-phase industrial converter under given transient and steady-state condition. As previously discussed, the estimation process can be carried out for any converter topology. The results of the proposed methodology are shown for offline temperature estimation. Nevertheless, this methodology can be extended to online temperature estimation if the ON-state circuitry is integrated in the converter board.

Acknowledgment

The authors would like to thanks Gianluca Rondine and Alessandro Roveri for the technical assistance and the useful discussions.

References

[1] K. Ma, A. S. Bahman, S. Beczkowski, and F. Blaabjerg, "Complete loss and thermal model of power semiconductors including device rating information," *IEEE Transactions on Power Electronics*, vol. 30, pp. 2556–2569, May 2015.

[2] H. Wang, K. Ma, and F. Blaabjerg, "Design for reliability of power electronic systems," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, pp. 33–44, 2012.

[3] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2413–2426, 2015.

[4] F. Hou, W. Wang, L. Cao, J. Li, M. Su, T. Lin, G. Zhang, and B. Ferreira, "Review of packaging schemes for power module," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 223–238, 2020.

[5] S. Asada, S. Kondo, Y. Kaji, and H. Yoshida, "Resin encapsulation combined with insulated metal baseplate for improving power module reliability," in *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, pp. 1–5, 2016.

[6] D. L. Blackburn, "Temperature measurements of semiconductor devices - a review," in *Twentieth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, pp. 70–80, 2004.

[7] Semikron, "Calculating Junction Temperature using a Module Temperature Sensor," AN 20-001 Application Note, 2020.

[8] Y. Zhang, H. Wang, Z. Wang, and F. Blaabjerg, "Simplified multi-time scale thermal model considering thermal coupling in igbt modules," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 319–324, 2019.

[9] A. S. Bahman, K. Ma, and F. Blaabjerg, "Thermal impedance model of high power igbt modules considering heat coupling effects," in *International Power Electronics and Application Conference and Exposition*, pp. 1382–1387, 2014.

[10] Zhaohui Luo, Hyungkeun Ahn, and M. A. E. Nokali, "A thermal model for insulated gate bipolar transistor module," *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 902–907, 2004.

[11] M. Musallam and C. M. Johnson, "Real-time compact thermal models for health management of power electronics," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1416–1425, 2010.

[12] Yichao Yuan, Dawei Xiang, and Chen Ning, "Self-calibration for igbt junction temperature measurement in power converter," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pp. 3125–3130, 2016.

[13] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-time temperature estimation for power mosfets considering thermal aging effects," *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 1, pp. 220–228, 2014.

[14] M. H. M. Sathik, J. Pou, S. Prasanth, V. Muthu, R. Simanjorang, and A. K. Gupta, "Comparison of igbt junction temperature measurement and estimation methods-a review," in *Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, pp. 1–8, 2017.

[15] W. Brekel, T. Duetemeyer, G. Puk, and O. Schilling, "Time resolved in situ tvj measurements of 6 . 5 kv igbts during inverter operation," in *PCIM Europe Conference*, pp. 808–813, 2009.

[16] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—a review," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 3081–3092, 2012.

[17] N. Baker, L. Dupont, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "Ir camera validation of igbt junction temperature measurement via peak gate current," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3099–3111, 2017.

[18] J. Zhang, X. Du, Y. Yu, S. Zheng, P. Sun, and H. Tai, "Thermal parameter monitoring of igbt module using junction temperature cooling curves," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 10, pp. 8148–8160, 2019.

[19] M. Montaine, M. Hanke, and U. Scheuermann, "Direct 2-way coupled electro-thermal simulation of temperature and current distribution in power devices," in *PCIM Europe Conference*, pp. 1–8, 2018.

[20] B. Wang, J. Cai, X. Du, and L. Zhou, "Review of power semiconductor device reliability for power converters," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 101–117, 2017.

[21] P. Ghimire, K. B. Pedersen, A. R. d. Vega, B. Rannestad, S. Munk-Nielsen, and P. B. Thogersen, "A real time measurement of junction temperature variation in high power igbt modules for wind power converter application," in *8th International Conference on Integrated Power Electronics Systems (CIPS)*, pp. 1–6, 2014.

[22] F. Stella, G. Pellegrino, E. Armando, and D. Daprà, "Online junction temperature estimation of sic power mosfets through on-state voltage mapping," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3453–3462, 2018.

[23] A. Alghassi, S. Perinpanayagam, M. Samie, and T. Sreenuch, "Computationally efficient, real-time, and embeddable prognostic techniques for power electronics," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2623–2634, 2015.

[24] I. Trintis, P. Ghimire, S. Munk-Nielsen, and B. Rannestad, "On-state voltage drop based power limit detection of igbt inverters," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1–9, 2015.

[25] L. Dupont and Y. Avenas, "Evaluation of thermo-sensitive electrical parameters based on the forward voltage for on-line chip temperature measurements of igbt devices," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4028–4035, 2014.

[26] R. Gelagaev, P. Jacqmaer, and J. Driesen, "A fast voltage clamp circuit for the accurate measurement of the dynamic on-resistance of power transistors," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 1241–1250, 2015.

[27] M. Guacci, D. Bortis, and J. W. Kolar, "On-state voltage measurement of fast switching power semiconductors," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 2, pp. 163–176, 2018.

[28] M. Denk and M. Bakran, "Igbt gate driver with accurate measurement of junction temperature and inverter output current," in *PCIM Europe Conference*, pp. 1–8, 2017.

[29] Yong-Seok Kim and Seung-Ki Sul, "On-line estimation of igbt junction temperature using on-state voltage drop," in *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242)*, vol. 2, pp. 853–859 vol.2, 1998.

[30] Y. Yang, Q. Zhang, and P. Zhang, "A novel on-line igbt junction temperature measurement method based on on-state voltage drop," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, pp. 1–6, 2019.

[31] S. Bęczkowski, P. Ghimre, A. R. de Vega, S. Munk-Nielsen, B. Rannestad, and P. Thøgersen, "Online vce measurement method for wear-out monitoring of high power igbt modules," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1–7, 2013.