Losses and thermal considerations on an IPOS structure with 20kW high-frequency planar transformers

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Alessandro La Ganga, Sergen Reyhan, Roberto Re, Jeanne-Marie Dalbavie, Paolo Guglielmi.

***Abstract*—Nowadays power electronics is looking for more integrated and compact insulated DC/DC converters. Electrical machines, like transformers, have a fundamental role in those kinds of converters. One of the main integration issue is the thermal aspect due to the power losses. Moreover, in an insulated DC/DC converter the bulkiest device is the transformer. Based on the high frequency power application the adopted transformer could be planar or litz wounded technology. In this work a single phase planar transformer for high power application has been investigated. An IPOS structure connecting many planar transformers has been performed to cope with the limitations that a single component gives. An experimental set-up adopting a SiC H-bridge power module feeding the different transformer structure. A power losses comparison among different structures has been realized. Indeed, the comparison is made connecting the H-bridge to a: single phase planar transformer, IPOS with 2 transformers, IPOS with 5 transformers, IPOS with 6 transformers and IPOS with a 10 transformers. The paper proposes thermal simulations for the IPOS made by 10 transformers and experimental results.**

***Index Terms*—High Frequency Transformer, IPOS, SST, power losses, SiC.**

I. Introduction

In electric energy conversion, electrical machines have a fundamental role. An energy conversion chain includes at least an electrical machine and a power converter. Based on the application and the electrical energy waveform, can be define different kind of conversion: AC/DC, AC/AC, DC/DC or $DC/AC/DC$. Due to the AC stage, the last solution it can be defined as indirect DC/DC conversion. In those applications the AC stage include an High Frequency Transformer **(HFT)** to guarantee the galvanic insulation. This converter topology is called as Solid State Transformer **(SST)**. Indeed, SSTs are becoming the most suitable converters in all applications in which a galvanic insulation is required. The adoption of HFTs allows to reduce converter sizing [1] [2]. The wide utilization of this converter topology is due to the adoption of Wide Band Gap (WBG) devices such as: Silicon Carbide (SiC) and Gallium Nitride (GaN). These devices allow to move the switching frequency up to hundreds of *kHz*. In low power applications, all HFTs are designed as planar transformer. By increasing the application power, HFTs technology move towards wounded transformer [3]. The main drawback in wounded transformer is the high leakage inductance value. Resonant capacitors need to be connected at the input of each transformer phase. Moreover, planar HFTs have a better power density [4]. The most known SST converter structures are Single Active Bridge (SAB) and Dual Active Bridge (DAB). Both structures include a H-bridge converter at the HFT primary side. At the secondary HFT side a diode bridge and a H-bridge respectively. Into converters adopting WBG the high switching frequency lead to fast commutations. Indeed, voltage slew rate exceed tens of $kV/\mu s$. Consequently, in HFTs equivalent electric model the parasitic capacitance should be taken into account [5]. Those stray capacitors define the leakage current path across the insulator between two turns. Into planar transformers capacitance are given by turns-turns and layer-layers paths. Layers surface is larger than two coupled turn's surfaces. This leads to an increasing of the parasitic capacitance into a HFT. Hence, into high frequency applications the capacitive reactance is no more negligible [6]. Galvanic insulation could be no more guaranteed for the high frequency currents. For planar HFTs, currents through the insulator and proximity effect increase the power losses impacting on thermal aspect [7]. This is an upper limit for the converter switching frequency. Despite of in some applications, connecting many transformers could be useful to increase the output power [8] and the operating switching frequency.

In this paper a power losses evaluation of a 20 kW planar transformers has been done. In Fig. 1 the electrical equivalent model of the 20 kW planar transformer is shown. In Section II some consideration on the HFT highlights the losses contributions in SST converters. To cope with the limit of the single HFT, structure based on different HFTs connections have been investigated. In Section III a generic IPOS structure is presented. In Section IV thermal simulation results of an IPOS-10 structure is presented. In Section V a power losses comparison between 20 kW planar transformers and many IPOS structures have been carried out.

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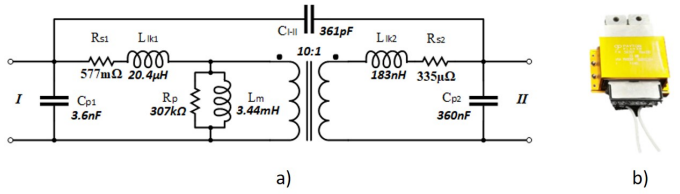

Fig. 1. Equivalent electrical model (a) of the adopted HFT (b)

II. HFT LOSSES CONSIDERATIONS

The choice of the core material, the winding shape and the cooling system are the output of the design of an electrical machine. Power losses and thermal behavior follow those choices. A required compactness makes the HFT design critical. In this case, even the thickness of the insulation layers impacts on the HFT losses. The knowledge of the different loss contributions allow to understand the power and thermal limit of the machine. The total power loss of a power transformer can be divided in three main components according to equation (1).

$$P_{\text{loss}} = P_{\text{core}} + P_{\text{cu}} + P_{\text{ins}} \tag{1}$$

The first component P_{core} is given by the core losses that are generally evaluated through the Steinmetz's equation [9].

$$P_{core} = K_1 \, f^{\text{k}_2} \, B^{\text{k}_3} \tag{2}$$

where f is the working frequency, B is the peak magnitude flux density and K_1, k_2, k_3 are coefficients depending on the core material. Typically adopted material for the construction of HFT core is ferrite. P_{Cu} represents the copper losses which have been expressed in [9] with the generic relationship.

$$P_{\text{Cu}} = \frac{R_{\text{ac}}}{R_{\text{dc}}} \frac{\rho \, l}{A} I^2_{\text{RMS}} \tag{3}$$

Where $\frac{R_{\text{ac}}}{R_{\text{dc}}}$ is the ac-resistance coefficient. The first definition is provided by [10]. ρ is the resistivity of the material, l and A are respectively the length and the cross area of the winding. The *RMS* value of the current is I_{RMS}. The equation (3) defines copper losses under sinusoidal waveform excitation. Square input waveform should be considered for HFTs in SST converter. [11] provides a more general definition of the copper losses under square wave operation (4) by means of the expression.

$$P_{Cu} = \sum_{i=1}^{\infty} \Big\{ I^2_{\text{p,i}} \sum_{j=1}^{M} [R_{\text{p,j}} \, \sqrt{i}\phi_{\text{j}} \, Q(\sqrt{i}\phi_{\text{j}}, m_{\text{j}})] + I^2_{\text{s,i}} \sum_{k=1}^{N} [R_{\text{s,k}} \, \sqrt{i}\phi_{\text{k}} \, Q(\sqrt{i}\phi_{\text{k}}, m_{\text{k}})] \Big\} \tag{4}$$

Where, $R_{\text{p,j}}$ and $R_{\text{s,k}}$ are primary and secondary winding resistance respectively, $\sqrt{i}\phi_{\text{j}}$ is the skin effect in function of the harmonic order, $Q(\sqrt{i}\phi_{\text{j}}, m_{\text{j}})$ is a function depending on the skin effect and the Magnetomotive Force among the transformer windings.

Insulation losses (P_{ins}) are typically negligible in low-power low-frequency applications. However, this contribute must be taken into account in high-power medium-frequency applications. An analytical description of this loss factor is defined in [12] as:

$$P_{\text{ins}} = C_{\text{o}} \sum_{n=1}^{\infty} \varepsilon_{\text{r}}^{"} (2\pi n f) V^2_{\text{n,RMS}} \tag{5}$$

Where C_{o} is the capacitance between two turns or layers, ε is the permittivity of the material, f is the fundamental frequency and $V_{\text{n,RMS}}$ is the applied voltage between the two layers. The sensitivity analysis of the different parameters of equation (5) allows to weight their impact on the P_{ins}. This weight is qualitatively summarized in Table I.

TABLE I
PARAMETERS EFFECTING THE INSULATION LOSSES

Parameters	**Symbol**	**Impact**
Duty cycle	D_{c}	Low
Voltage slope	T_{r} T_{f}	Medium
Switching frequency	f	High
DC Voltage	V_{DC}	High
permittivity	$\varepsilon_{\text{r}}^{"}$	High

III. IPOS STRUCTURE

The aim of this section is the description of some common structures shared among many HFTs. The idea is to build an equivalent power transformer compliant with the specifications of the application. The equivalent voltage ratio is a combination of the single HFT's ratio. In electrical power system having nominal frequency of 50 Hz/60 Hz the power transformers are often connected putting inputs and outputs respectively in parallel. This kind of connection does not modify the starting voltage ratio of the single transformer which becomes the equivalent voltage ratio of the resulting equivalent transformer. In a SST converter different kind of transformer connections could be adopted:

- IPOP: Input Parallel Output Parallel;
- ISOS: Input Series Output Series;
- IPOS: Input Parallel Output Series;
- ISOP: Input Series Output Parallel.

Among the listed topologies, the series connection of one side, affects the equivalent voltage ratio. In particular, the IPOS configuration modifies only the secondary side voltage. Adopting six HFT with 10:1 ratio, the IPOS-6 equivalent voltage ratio is 10:6 ($t = 1.67$). As an example, a SAB converter adopting an IPOS structure made by n-HFT is shown in Fig. 2.

Following this codification, the present paper proposes the analysis of four structures named: *IPOS-2*, *IPOS-5*, *IPOS-6*, *IPOS-10*. All IPOS configurations are considered based on 20 kW planar HFTs.

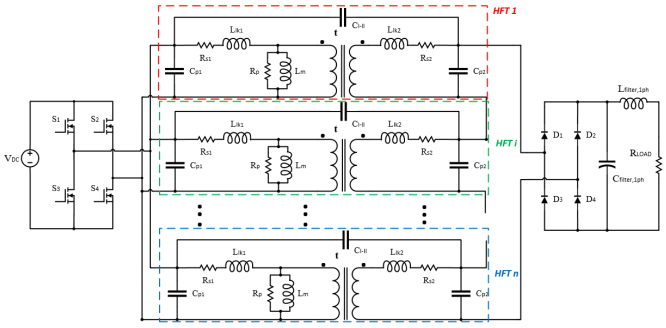

Fig. 2. SAB converter adopting a generic IPOS structure made by n-HFT

IV. Thermal Simulation

A simple and modular heat sink is designed for an IPOS-10 structure. The heatsink material is aluminium. At full power, the transformer's datasheet suggests keeping the ferrite core temperature at around 35 °C. The goal of the present analysis is to evaluate the final temperature achieved by the IPOS-10 structure. Simulations in steady state condition are performed with the software **COMSOL multiphysics**. The main input of the simulation is the total power loss of the single HFT. The HFT efficiency given by the datasheet at nominal condition is 99.5%. All simulation data are listed in Table II. In a simulation environment, under those conditions and without coolant into the heatsink pipe, the IPOS-10 final temperature is 70 °C. This result is consistent with Fig. 10.a) in which, during open-circuit test, the single HFT core achieves 50 °C. In consequence of this core temperature, the power rate of each transformer is derated under 20 kW. Hence, a fluid cooling system has be adopted.

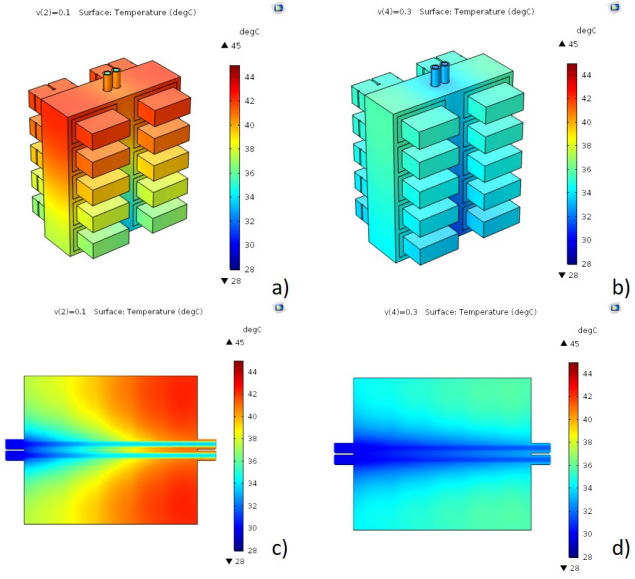

Fig. 3. IPOS-10 thermal simulations performed into COMSOL Multiphysics. a)IPOS-10 3D thermal simulation with 0.1 m/s; b)IPOS-10 3D thermal simulation with 0.3 m/s; c) section view of an IPOS-10 in a thermal simulation with 0.1 m/s; b) section view of an IPOS-10 in a thermal simulation with 0.3 m/s.

In Fig. 3 thermal simulations with a coolant inside the heatsink pipes are shown. All simulations assume not electrical conductive water, as coolant, under laminar flow.
The simulation goal is to achieve a uniform temperature distribution across the entire structure performing simulations with different coolant speed. In Fig. 3a) and Fig. 3c) the temperature gradient across the structure is about 10 °C while the highest temperature is 44 °C. In Fig. 3b) and Fig. 3d) the temperature distribution over the structure is uniform at 36 °C.

TABLE II
THERMAL SIMULATION DATA

IPOS-10		
Parameters	**Symbol**	**Value**
Power transformer losses	P_{loss}	100 W
Input liquid temperature	T_{wa}	30 C
Liquid speed	u_{wa}	$from$ 0 m/s to 0.3 m/s
Pipe diameter	d	8 mm

V. Power Losses Evaluation: Experimental Results

The goal of this section is the evaluation and comparison of the power losses between a single HFT and the IPOS-n structures. As underlined in Section II the HFT losses are affected by switching frequency, voltage slew rate and DC-link voltage level. To achieve a proper losses evaluation, a converter with WBG device should be adopted. The experimental set-up adopted in this paper for this evaluation is based on an H-bridge SiC power module [13] feeding the HFT or IPOS-n structure under test. The safe Operating Area (SOA)of the H-bridge switches is limited within 1.2 kV and 100 A. The scheme in Fig. 4 shows the three main devices required for the power tests: a DC source, a DC/AC conversion stage and the Device Under Test (DUT). A 1000 V DC voltage source with a current capability up to 30 A is connected to the H-bridge input. The DUT in Fig. 4 is a generic IPOS-n. The IPOS-n structure is based on a 10:1 ratio planar HFT. In all tests, the primary side (high-voltage side) is connected in parallel, whereas the secondary side (high-current side) is connected in series.

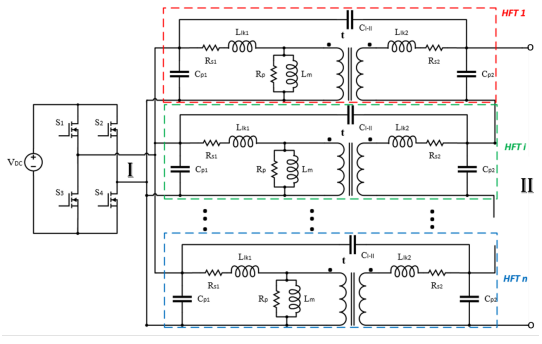

Fig. 4. Scheme for the open circuit test with IPOS-n structure

Different structures have been tested. Section III explains how the voltage ratio changes in a generic IPOS structure. DUT's equivalent ratio are listed in Table III.

TABLE III
EQUIVALENT DUT VOLTAGE RATIO

Parameters	Symbol	Value
HFT	t	$10:1=10$
IPOS-2	t_2	$10:2=5$
IPOS-5	t_5	$10:5=2$
IPOS-6	t_5	$10:6=1.67$
IPOS-10	t_{10}	$10:10=1$

Transformer characterization requires open circuit and short circuit tests. Those two tests have been performed for all DUTs. In Fig. 5a) open-circuit test waveforms are shown. The voltage ratio is verified for all DUTs and magnetization currents are equally distributed among all HFTs into the IPOS structure. The saturation condition of the iron core depends on the product V s (Volts per second). To show the DUTs limits the open circuit test was carried out in the most critical condition from the point of view of saturation, i.e. at low frequency (40 kHz). In Fig. 5b), short-circuit test waveforms are shown. In this case, the equivalent transformer ratio of the IPOS-5 structure is verified by means of the currents ratio. DC-link voltage corresponds to the short-circuit voltage. Clearly, this voltage changes proportionally with respect to the switching frequency. In Fig. 5b), the short-circuit voltage for the IPOS-5 at 100 kHz is $V_{cc} = 35$ V, about the 5% of the rated DC-link voltage. In the short citcuit test the phase current of the DUT and therefore of the converter is the nominal one. In this case, the limit is given by the high switching frequency with rated current. The commutation changes (the soft switching transition time increases) as the number of HFT connected in the DUT increases.

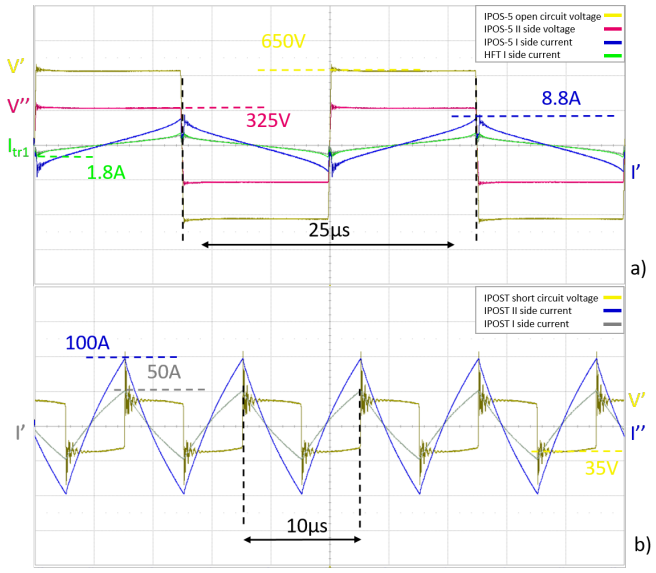

Fig. 5. IPOS-5 power test waveforms. a)Open circuit test: $V'V''$ $300V/div$ I' $10A/div$ I_{tr} $5A/div$ $5\mu s/div$ b)Short circuit test: $I'I''$ $50A/div$ V' $50V/div$.

From the insulation point of view, one important aspect is the voltage slew rate during the commutation. In Fig. 6 the difference between a single HFT and all IPOS-n structure is shown.

For an IPOS-n, voltage slew rate appears reduced compared with the single HFT. This slew rate auto-mitigation of an IPOS-n structure is a positive effect from the losses point of view. At the same time, the electrical stress into the transformer's isolation is reduced. Power tests have been performed at different switching frequencies. In Fig. 7, results in open-circuit condition are reported. Connecting many HFTs modifies the losses trend. The result indicates that, by increasing the number of the transformers of the IPOS-n structure, the losses minimum moves toward higher frequencies.

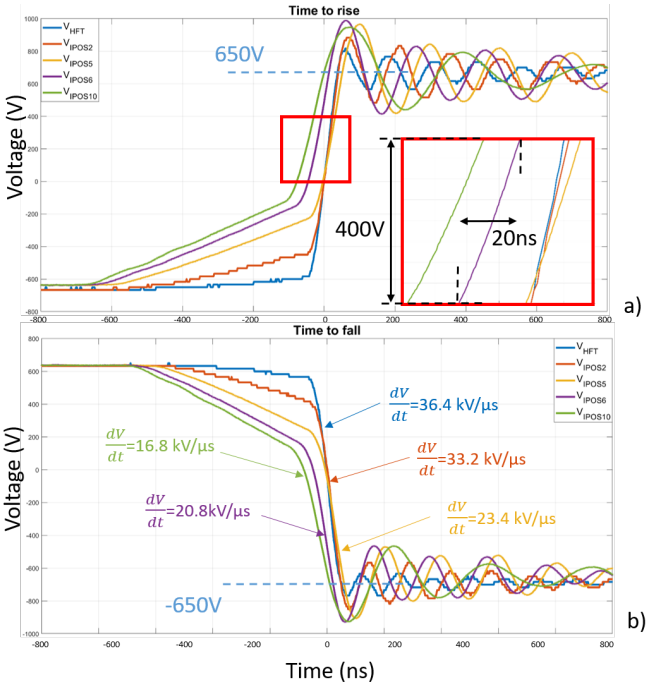

Fig. 6. Primary Voltage at 100 kHz a)rising edge ; b)falling edge.

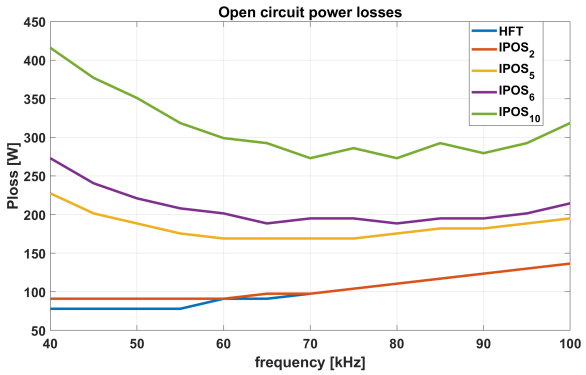

Fig. 7. Power losses result in open circuit test.

For example, the minimum in the IPOS-5 structure losses is achieved in the range from 60 kHz up to 75 kHz. For the IPOS-10 this range moves from 70 kHz up to 80 kHz.
In Fig. 8, the losses related to the short-circuit test are showed. Power losses trend is almost constant in the whole frequency range.
For a proper power losses comparison all DUTs power losses

are divided by the respective IPOS-n nominal power. Fig. 9 highlight an important aspect about IPOS-n structures. In fact, power losses in an IPOS with two or more HFT are reduced compared with a single HFT case. Despite of losses decrease adding many HFTs into the structure, there is an optimum number of devices to be connected to the structure. This optimum number of HFTs corresponds to the minimum losses value achievable with an IPOS-n structure. From the short-circuit test results, the optimal IPOS structure is made by 6 HFTs. However, in all IPOS structures the efficiency gain is about 0.5%. Increasing the switching frequency is more appropriate the use of an IPOS structure instead of a single HFT.

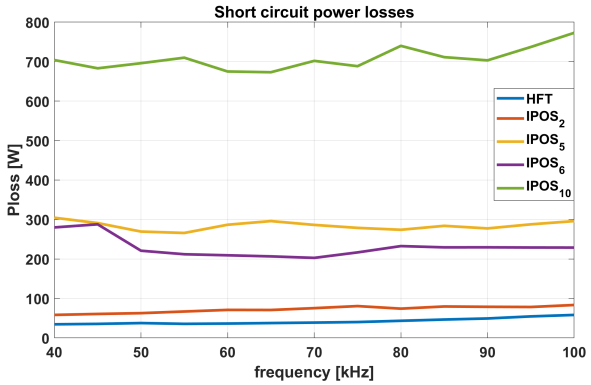

Fig. 8. Power losses result in short circuit test.

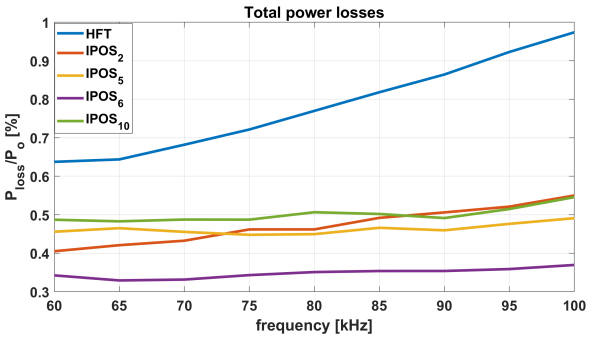

Fig. 9. Total Power losses in per unit; $P_{\rm b} = 20$ kW$/n$, where n is the number of transformers connected into IPOS structure.

A complete *IPOS-n* structure definition includes the following data: the magnetization current (I_0), the short-circuit voltage ($V_{\rm cc\%}$) and the power factor in short-circuit condition($cos\varphi_{\rm cc}$). The first extract parameter is the short-circuit voltage for each topology. This parameter is a percentage of the nominal voltage. Results show a $V_{\rm cc\%}$ value close by the $3.5 - 5\%$ among all IPOS structures. IPOS connection changes the reactive behavior of the structure. The output series connection changes the total IPOS leakage inductance. The input parallel connection increases the input capacitance contribution compensating the whole IPOS inductive behavior. This aspect is pointed out from the IPOS-n power factor ($cos\varphi_{\rm cc}$). This parameter increases with the number of HFTs connected into the IPOS structure.
All data test and results of the *IPOS-n* evaluation are listed in Table IV. Fig. 11 shows the experimental test bench for the open circuit and short circuit tests.

VI. Conclusions

Starting from the HFT losses definition, this paper carried out some consideration about the losses and the thermal behavior of an IPOS-n structure adopting 20 kW planar HFTs. The comparison between a single planar HFT and many IPOS structures lead to the definition of minimum losses working point. The efficiency gain between HFT and an IPOS-n is about 0.5%. Moreover, the adoption of many devices increases the converter efficiency even at 100 kHz. This allow to achieve higher switching frequency and consequently, a higher power density of the converter. Indeed, this work is focused on SST converter topologies in which HFT is the bulkiest device. Results can be applied to all applications in which a galvanic insulation is required.

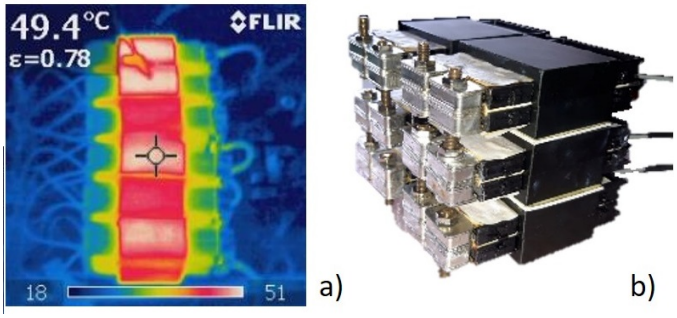

Fig. 10. a) Thermal image of the IPOS-6 under open circuit test condition; b)IPOS assembly with 6 HFTs

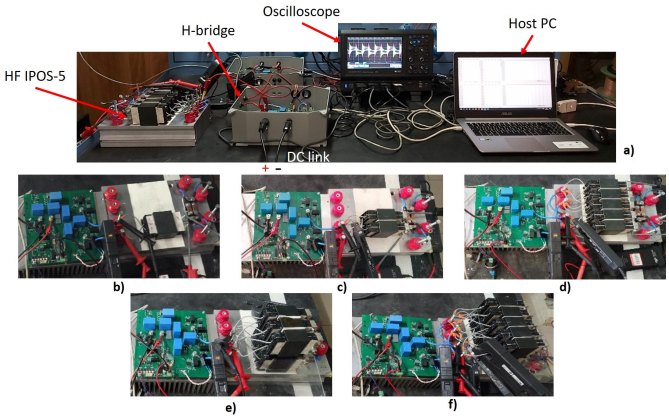

Fig. 11. a) Experimental test bench; b) HFT power set-up; c) IPOS-2 power set-up; d) IPOS-5 power set-up; e) IPOS-6 power set-up; f) IPOS-10 power set-up.

TABLE IV
POWER TEST REFERENCE DATA

HFT		
Parameters	**Symbol**	**Value**
Switching frequency	f_{sw}	$40\ \mathrm{kHz} - 100\ \mathrm{kHz}$
Open circuit DC Voltage	V_{DC}	650 V
Magnetizing current	$I"_{0,\mathrm{RMS}}$	1.6%
Secondary side short circuit current	$I"_{\mathrm{RMS}}$	60 A
Short circuit voltage	$V_{\mathrm{cc}\%}$	5.8%
Power factor	$cos\varphi_{\mathrm{cc}}$	0.02
IPOS-2		
Parameters	**Symbol**	**Value**
Switching frequency	f_{sw}	$40\ \mathrm{kHz} - 100\ \mathrm{kHz}$
Open circuit DC Voltage	V_{DC}	650 V
Magnetizing current	$I"_{0,\mathrm{RMS}}$	2.6%
Secondary side short circuit current	$I"_{\mathrm{RMS}}$	60 A
Short circuit voltage	$V_{\mathrm{cc}\%}$	3.7%
Power factor	$cos\varphi_{\mathrm{cc}}$	0.054
IPOS-5		
Parameters	**Symbol**	**Value**
Switching frequency	f_{sw}	$40\ \mathrm{kHz} - 100\ \mathrm{kHz}$
Open circuit DC Voltage	V_{DC}	650 V
Magnetizing current	$I"_{0,\mathrm{RMS}}$	5.8%
Secondary side short circuit current	$I"_{\mathrm{RMS}}$	60 A
Short circuit voltage	$V_{\mathrm{cc}\%}$	4.8%
Power factor	$cos\varphi_{\mathrm{cc}}$	0.15
IPOS-6		
Parameters	**Symbol**	**Value**
Switching frequency	f_{sw}	$40\ \mathrm{kHz} - 100\ \mathrm{kHz}$
Open circuit DC Voltage	V_{DC}	650 V
Magnetizing current	$I"_{0,\mathrm{RMS}}$	7.2%
Secondary side short circuit current	$I"_{\mathrm{RMS}}$	60 A
Short circuit voltage	$V_{\mathrm{cc}\%}$	3.5%
Power factor	$cos\varphi_{\mathrm{cc}}$	0.17
IPOS-10		
Parameters	**Symbol**	**Value**
Switching frequency	f_{sw}	$40\ \mathrm{kHz} - 100\ \mathrm{kHz}$
Open circuit DC Voltage	V_{DC}	650 V
Magnetizing current	$I"_{0}$	9%
Secondary side short circuit current	$I"_{\mathrm{RMS}}$	60 A
Short circuit voltage	$V_{\mathrm{cc}\%}$	4.3%
Power factor	$cos\varphi_{\mathrm{cc}}$	0.4

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VII. BIOGRAPHIES

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