A Closed Loop Delay Compensation Technique to Mitigate the Common Mode Conducted Emissions of Bipolar PWM Switched Circuits

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Michele Perotti, *Student Member, IEEE* and Franco Fiori, *Member, IEEE*

***Abstract*—This paper presents the design of a new closed loop technique that reduces the common mode conducted emission. It can be applied to any kind of switching circuit in which couples of outputs are modulated by a bipolar PWM signal. It is based on the compensation of the delay between complementary output switching edges, using a simple sensing circuit and a low computational effort software algorithm, which is implemented in a microcontroller driving the switching circuit. One of the main advantages of the proposed solution is the reduction of the disturbance energy, without affecting the system efficiency. The technique is practical to implement, and the measurements performed on a power inverter prototype confirm the theoretical analysis outcomes about the reduction of the conducted emission in the lower-to-medium frequency range.**

***Index Terms*—Electromagnetic interferences (EMI), common mode (CM) emissions, closed loop delay compensation, motor drives, bipolar PWM.**

I. Introduction

POWER switching circuits are widespread in most electronic systems. The related research activity mainly focuses on the production of more efficient and reliable circuits. Besides this, the Electromagnetic Compatibility (EMC) of the system with the surrounding environment is also a major challenge in the design of such circuits. In particular, electronic units, like power inverters or converters, must comply with tight electromagnetic (EM) emission limits [1], [2]. Such power circuits generate high *dv/dt* and *di/dt* edges, which give rise to electromagnetic interferences (EMI). In recent years, such an issue has become critical, since the new semiconductor devices are characterized by shorter rising/falling times and they can be driven at higher switching frequencies. All of this is reflected in an increased generation of the conducted EMI [3], [4], i.e. the disturbances that propagate through the power supply cables [1], [2]. Such emissions are regulated by several standards, like CISPR 16 [5] for household appliances or CISPR 25 [6] for automotive modules.

A common approach for limiting the conducted EMI is to insert a filter at the power supply input of the circuit. Such a filter is designed to attenuate the common mode (CM) and the differential mode (DM) emissions independently. The CM component propagates from the power supply cables to the system chassis; the DM, instead, is due to the disturbance currents entering the positive power supply terminal and leaving from the negative one [1], [2]. In particular, the components used to attenuate the CM emission, usually are a CM choke and some capacitors, each one connected between the power lines and the chassis. In power circuits, usually such filters are cumbersome, heavy and expensive. An approach for reducing the CM choke dimensions, is based on the optimal design of its magnetic core, considering both the attenuation required and the core saturation issues [7]. Moreover, the CM choke geometry is not easy to design, since parasitic elements, which can be estimated through 3D simulation [8], like the interwinding capacitances, reduce its effectiveness.

In order to gain more flexibility in EMI reduction, several software techniques, like spread spectrum modulation (SSM), were developed. The SSM approach consists in modulating the switching frequency of the circuit, with the purpose of spreading the energy of each harmonic of the emission spectrum over a wider frequency band. Different modulation methods can be employed, as reported in [9], [10]. The current research activity aims to improve the performance of the SSM control schemes, by addressing issues like the frequency accumulation [11]. This derives from the digital generation of the switching frequency: if it is not immediately updated, some frequency values can be imposed twice (frequency accumulation). Chen *et al.*, proposed the immediate frequency update through a DDS, solving the non-uniform distribution of the switching frequency, but at the cost of an increased system complexity. Other improvements to SSM are given in [12]. Despite the valuable reduction of the harmonics peak value, it is worth underlining that the disturbance energy remains unchanged.

Given that the EM emission delivered by power circuits deals mostly with the parasitic currents induced by the fast switching nodes, [13] envisaged a possible mitigation of the conducted emissions for those circuits comprising power nodes switching opposite, by means of a tight alignment of rising and falling edges. The effectiveness of the proposed approach was proved measuring the conducted emissions of a prototype, which allowed a case by case alignment of the switching waveforms. The present work shows the evolution of the idea proposed in [13], to make it robust against load and parasitic variations as well as the variation of the circuit parameters from sample to sample.

The paper is organized as follows. In Section II the EMI generation of bipolar PWM switched circuits is presented and

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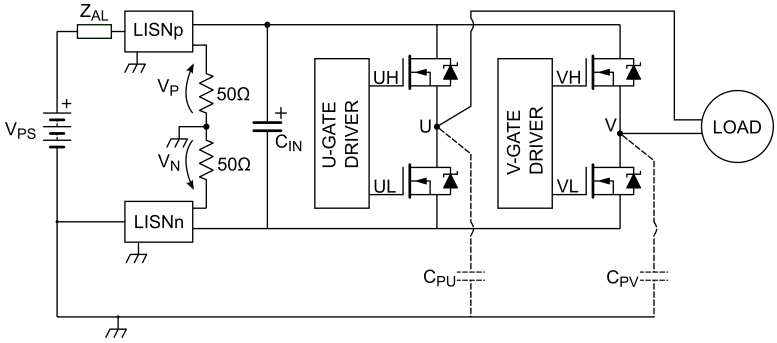


Fig. 1: Single-phase inverter schematic.

the output delay compensation effect on the CM EMI spectrum is shown. Section III presents the delay compensation controller architecture, and, in Section IV, the technique is implemented on a particular switching circuit: the Brushless DC motor driver. The system was prototyped and conducted emission measurements were performed. The results were collected and are discussed in Section V. Compared with the results of the preliminary investigation, the proposed delay compensation control further reduces the CM EMI. Conclusions are drawn in Section VI.

II. Conducted Emissions of Bipolar PWM Switched Circuits

The circuits used to transform the voltage from DC to AC or to convert the DC voltage, in most of cases are switched using pulse width modulation (PWM) scheme. Such a modulation generates high *dv/dt* and *di/dt* transients, giving rise to the conducted emissions. These emissions are limited by international standards, which require the measurement of the disturbance flowing through the power supply cable, to qualify the electronic system. These measurements should be performed using a well-defined power supply impedance, with the aim of producing repeatable results. To this purpose, the power supply is provided through two line impedance stabilization networks (LISNs), as prescribed in CISPR25. The LISNs and the electronic system that should be characterized, are placed on a conductive reference plane. The conducted emissions are usually described referring to the common mode (CM) component and to the differential mode (DM) one. The first is due to the current flowing through the parasitic capacitances coupling the power modules to the reference plane. The second is the switching current flowing through the power supply cables, which is not filtered by the input capacitor. Both the CM and the DM flow in the 50 Ω LISN impedances, to be sensed by the EMI receiver.

An example of switching circuit is the single-phase inverter, shown in Fig. 1. The CM EMI is generated mainly by the voltages at the output terminals, which show high *dV/dt* transient. Such voltage variations to ground make the interfering current to flow through the parasitic capacitances C_{PU} and C_{PV}. The choice of the PWM scheme can influence the generation of the conducted emissions [14]. Indeed, the use of the bipolar PWM modulation would reduce these high frequency currents, since the current injected in C_{PU} by a low-to-high transition can

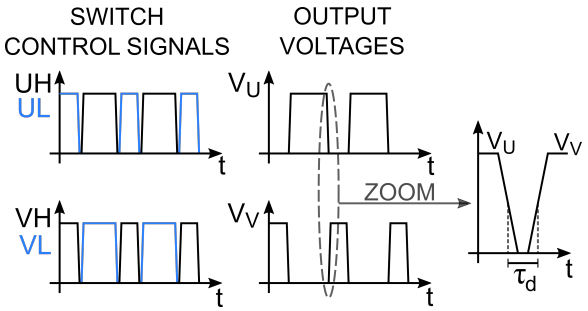


Fig. 2: Gate signals and output signals. Due to delays introduced mainly by the gate drivers, in most of cases the output edges are not aligned.

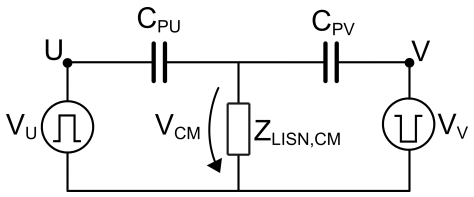


Fig. 3: Common Mode EMI equivalent circuit.

be collected locally by the parasitic capacitance C_{PV} referred to the output voltage switching opposite, and vice versa. This principle can be applied to any circuit including couples of output nodes switching oppositely.

Actually, the output voltage waveforms are not complementary to one another due to a delay, τ_{d}, introduced mainly by the gate drivers, as shown in Fig. 2. Such a delay is one of the main causes of the CM conducted emissions when a bipolar PWM is used.

For each bipolar PWM switched couple, the generation of the CM conducted EMI can be modeled with the circuit of Fig. 3. Therefore, the CM EMI spectrum envelope can be expressed as:

$$V_{CM}(jn\omega_0) = V(jn\omega_0)\cdot D(jn\omega_0)\cdot H(jn\omega_0) = V(jn\omega_0)\cdot\left(1+e^{-jn\omega_0\left(\frac{T}{2}+\tau_d\right)}\right)\cdot\frac{j\omega Z_{\mathrm{LISN,CM}}C_{\mathrm{p}}}{1+2j\omega Z_{\mathrm{LISN,CM}}C_{\mathrm{p}}}, \quad (1)$$

where $V(jn\omega_0)$ is the spectra of the trapezoidal voltage of the output node, with PWM period T, $D(jn\omega_0)$ is the contribution of the delay τ_{d} and $H(jn\omega_0)$ is the transfer function of the high-pass filter made of the parasitic ca-

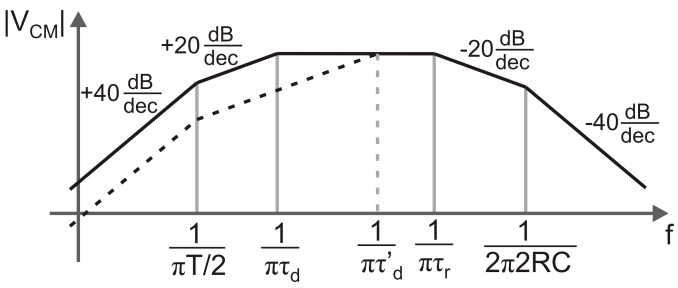


Fig. 4: Common mode voltage spectrum envelope.

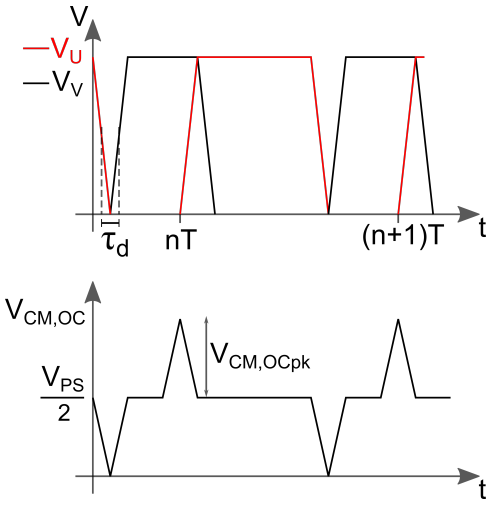


Fig. 5: Open circuit common mode voltage.

pacitances $C_{\rm p} = C_{\rm PU} = C_{\rm PV}$ and the LISN impedance $Z_{\rm LISN,CM} \approx 25\Omega$. On the basis of (1), the CM disturbance can be reduced minimizing the term $D(jn\omega_0)$. This can be obtained compensating the delay $\tau_{\rm d}$: if this quantity tends to zero, the $D(jn\omega_0)$ is minimized and the CM disturbance is lowered. The spectral envelope of (1) is reported in Fig. 4. If $\tau_{\rm d}$ is reduced to $\tau'_{\rm d}$, the respective pole is shifted at higher frequency, reducing the EMI spectra up to this new frequency pole. In preliminary tests the delay $\tau_{\rm d}$ was compensated adjusting manually the PWM parameters [13]. Since several commercial gate drivers present a strong variability in the input-output delay, which can be above one hundred ns, a closed control loop is needed to compensate $\tau_{\rm d}$. The design of such a system requires the measurement of the delay $\tau_{\rm d}$: in the next paragraph the output average voltage is analyzed and related to $\tau_{\rm d}$, in order to be used as feedback quantity.

A. Common mode output voltage

The first two terms in (1) represent the output CM voltage. Such a voltage, in the time domain, can be expressed as the average value of the output switching voltages

$$V_{\rm CM,OC}(t) = \frac{V_{\rm U}(t) + V_{\rm V}(t)}{2}. \tag{2}$$

Assuming the two switching output voltages complementary, i.e. $\tau_{\rm d} = 0$ns, $V_{\rm CM,OC}$ is constant and no disturbances are observed at the LISN terminals. Instead, if $\tau_{\rm d} \neq 0$ ns, some voltage peaks are present, as shown in Fig. 5. These spikes are

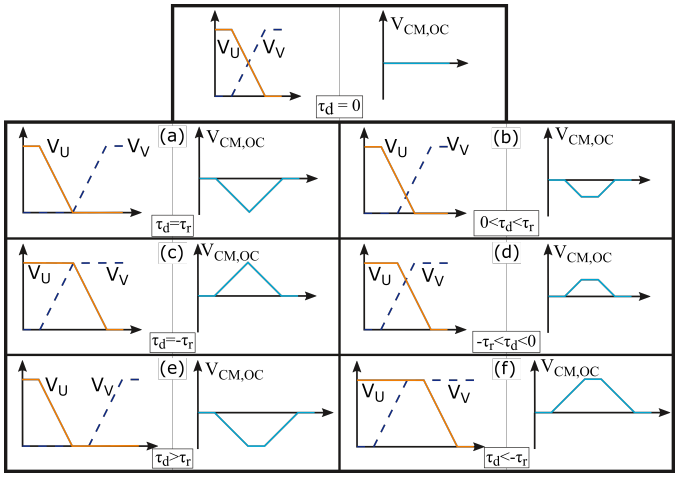


Fig. 6: Open circuit common mode voltage shapes according to the delay τ_d.

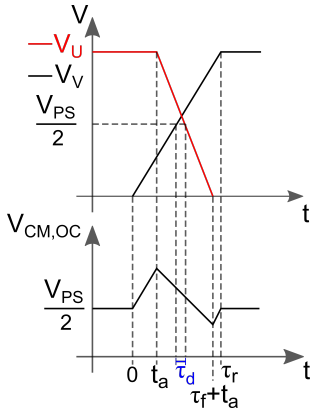


Fig. 7: Effect of the $\tau_{\rm r}/\tau_{\rm f}$ mismatch on the voltage $V_{\rm CM,OC}$.

responsible for the conducted CM EMI, and they are different in amplitude and polarity depending on $\tau_{\rm d}$, as shown in Fig. 6. As long as the delay is lower than the rising/falling time $\tau_{\rm r}$, the magnitude of such voltage peaks depends upon $\tau_{\rm d}$ as

$$V_{\rm CM,pk} = \frac{V_{\rm PS}}{2}\frac{\tau_{\rm d}}{\tau_{\rm r}}, \tag{3}$$

and it saturates to $V_{\rm PS}/2$ for $\tau_{\rm d} > \tau_{\rm r}$.

B. Effect of rising and falling time mismatch

In actual applications, the rising and the falling times of the switching edges are not equal, they often differ due to several factors: parasitics mismatch, current re-circulation, asymmetries of the load. If the transition times are different, some CM EMI is generated even if the output voltages are aligned. In these cases the voltage $V_{\rm CM,OC}$ changes as shown in Fig. 7. There are two peaks for each commutation, a positive one and a negative one. In this case, in order to find the best alignment of the output voltage edges to reduce the CM EMI, it is possible to compute the normalized energy of the AC component of the $V_{\rm CM,OC}$ voltage shown in Fig. 7. The delay $\tau_{\rm d}$ can be expressed as

$$\tau_{\rm d} = t_{\rm a} - \frac{\tau_{\rm r} - \tau_{\rm f}}{2}, \tag{4}$$

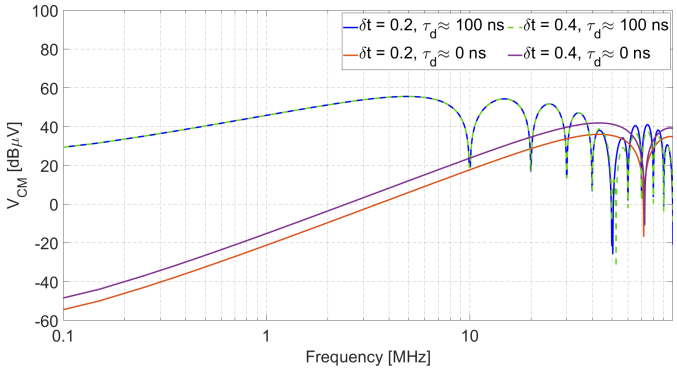


Fig. 8: Effect of δt_t on the CM spectrum with $\tau_\mathrm{d} = 100\,\mathrm{ns}$ (blue and green curves) and with $\tau_\mathrm{d} = 0\,\mathrm{ns}$ (red and violet curves).

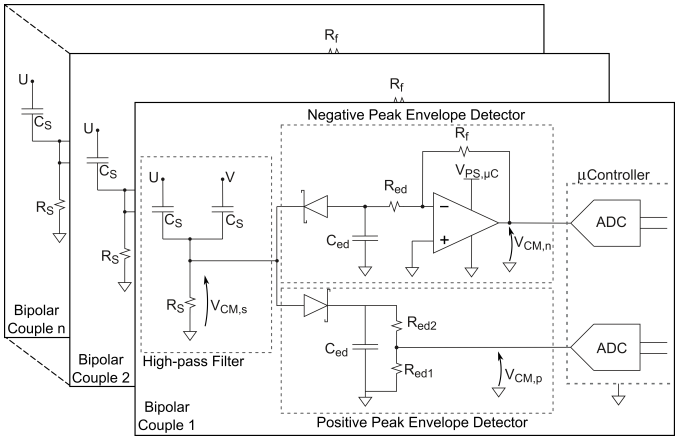


Fig. 9: Signal conditioning circuit for common mode voltage sensing.

and considering t_a as a parameter, the signal energy is given by

$$\mathcal{E}_\mathrm{s} = \int_0^{\tau_\mathrm{r}} \left| V_\mathrm{CM,OC}(t) - \frac{V_\mathrm{PS}}{2} \right|^2 dt = \left(\frac{V_\mathrm{PS}}{2\tau_\mathrm{r}}\right)^2 \left[\left(\frac{t_\mathrm{a}^3}{3} + \frac{(\tau_\mathrm{r} - \tau_\mathrm{f} - t_\mathrm{a})^3}{3} \right) \left(1 + \frac{\tau_\mathrm{f}}{\tau_\mathrm{r} - \tau_\mathrm{f}} \right) \right]. \quad (5)$$

From this equation it turns out that the minimum of the signal energy is obtained at $t_\mathrm{a} = (\tau_\mathrm{r} - \tau_\mathrm{f})/2$, i.e. that is for $\tau_\mathrm{d} = 0$. In this case, the positive and the negative peaks of the voltage $V_\mathrm{CM,OC}$ show the same magnitude.

In order to estimate the influence of the difference between τ_r and τ_f on the CM emissions, the average transition time ($t_\mathrm{t,avg}$) and the transition time mismatch (δt_t)

$$t_\mathrm{t,avg} = \frac{\tau_\mathrm{r} + \tau_\mathrm{f}}{2}, \qquad \delta t_\mathrm{t} = \frac{|\tau_\mathrm{r} - \tau_\mathrm{f}|}{t_\mathrm{t,avg}}, \quad (6)$$

are defined. Referring to these parameters and assuming $t_\mathrm{t,avg} = 20\,\mathrm{ns}$, the analysis of the two-leg system shows that a variation of δt_t of $\pm 10\%$ causes an increment of the CM emissions of about 6 dB. A comparison of the emission spectra is provided in Fig. 8. The blue and green curves were obtained with $\tau_\mathrm{d} = 100\,\mathrm{ns}$, whereas the red and violet ones with $\tau_\mathrm{d} = 0\,\mathrm{ns}$, using δt_t equal to 20% and 40%, respectively. In practice, the edge asymmetry reduces the effectiveness of the proposed solution slightly. In order to develop a closed loop technique, the magnitude of such voltage spikes, should be acquired by the microcontroller, as shown in the next Section.

III. Delay Compensation Loop

The control of the switching circuits in modern applications resides in the microcontroller. The electrical quantities used as feedback in the control loops, should be sampled by the ADC, which is inside the microcontroller. As mentioned in the previous Section, in this study the feedback quantity is the common mode output voltage $V_\mathrm{CM,OC}$. Its peaks are as narrow as a few ns; therefore, the ADC sampling rate, which is often equal to a few Msps, does not allow a reliable sampling of such voltages. In order to address this issue and to acquire the peaks amplitude, a conditioning circuit, connected to each bipolar switching couple, should be designed. Such a circuit, which is shown in Fig. 9, is composed of three blocks: a high-pass filter and two envelope detectors. The high-pass filter is used to obtain the common mode voltage of the output waveforms, rejecting the DC component, which has no use for CM EMI. The two output nodes are thus connected to two equal capacitors, which terminate on a common resistor. The filter components C_S and R_S are chosen in order to filter up to $f_\mathrm{t} = 100\,\mathrm{kHz}$ and to avoid loading the output nodes. Therefore, the C_S capacitance value can be chosen arbitrarily in the order of hundreds of pF. The resistance value turns out to be:

$$R_\mathrm{S} = \frac{1}{2\pi f_\mathrm{t} C_\mathrm{S}}. \quad (7)$$

The signals at the output of the high-pass filter, $V_\mathrm{CM,s}$ are voltage spikes, which can be as narrow as a few ns. Since such a signal cannot be sensed directly by the microcontroller, two envelope detectors, one for the positive peaks and the other for the negative ones are connected to the filter output. These circuits are indicated in the schematic of Fig. 9 as the "Positive peak envelope detector" and the "Negative peak envelope detector", respectively.

Both envelope detectors are designed in order to have a reasonably fast decay constant with respect to the PWM period. In the designed circuit, a decay constant close to $T/10$ was chosen. Moreover, the voltage at the output of each envelope detector should be scaled to the input range of the microcontroller ADC. This is obtained with a voltage divider for the positive peak envelope detector, and with an attenuating inverting amplifier for the negative one. The operational amplifier should have a high slew rate in order to follow the input signal.

The capacitor C_ed is chosen to be lower than C_s. Thus, R_ed is given by:

$$R_\mathrm{ed} C_\mathrm{ed} \approx \frac{T}{10} \rightarrow R_\mathrm{ed} \approx \frac{T}{10} \frac{1}{C_\mathrm{ed}}. \quad (8)$$

Based on (8), the resistors R_ed1, R_ed2 of the positive envelope detector should be such that:

$$R_\mathrm{ed} = R_\mathrm{ed1} + R_\mathrm{ed2}. \quad (9)$$

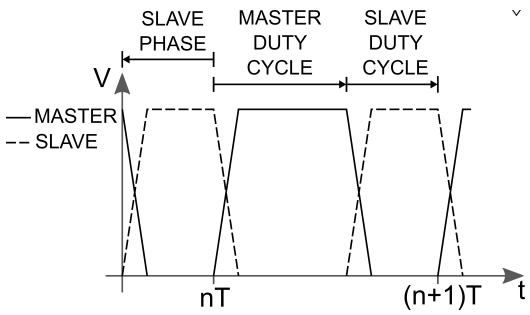


Fig. 10: PWM parameters definition. In continuous line the Master output voltage, in dashed line the Slave one.

Furthermore, the scaling factor is chosen as:

$$\frac{V_{\mathrm{ADC\ max}}}{V_{\mathrm{CM,pk\ max}}} = |K| = R_{\mathrm{ed1}}/R_{\mathrm{ed}}. \tag{10}$$

For the negative envelope detector, the impedance seen in parallel to the capacitor should be equal to R_{ed}, as well. Therefore, the inverting amplifier input series resistance is equal to that value. The feedback resistance, instead, is designed using the same scaling factor of the positive branch:

$$|K| = R_{\mathrm{f}}/R_{\mathrm{ed}}, \tag{11}$$

so $R_{\mathrm{f}} = R_{\mathrm{ed1}}$.

The two voltages $V_{\mathrm{CM,p}}$ and $V_{\mathrm{CM,n}}$ are provided to the input of two independent ADCs of the microcontroller. The relation between the maximum of $V_{\mathrm{CM,p}}$, $V_{\mathrm{CM,n}}$ and the sampled voltages $V_{\mathrm{ADC,p}}$ and $V_{\mathrm{ADC,n}}$ are:

$$V_{\mathrm{ADC,p}} = V_{\mathrm{CM,p,pk}} \frac{R_{\mathrm{ed}}}{R_{\mathrm{ed1}}} e^{\frac{t_{\mathrm{s}}}{R_{\mathrm{ed}} C_{\mathrm{ed}}}} + V_{\gamma}, \tag{12}$$

$$V_{\mathrm{ADC,n}} = V_{\mathrm{CM,n,pk}} \frac{R_{\mathrm{ed}}}{R_{\mathrm{ed1}}} e^{\frac{t_{\mathrm{s}}}{R_{\mathrm{ed}} C_{\mathrm{ed}}}} + V_{\gamma}, \tag{13}$$

where t_{s} is the time interval between the commutation time and the sampling time, V_{γ} is the diode forward voltage.

The next Section presents how these voltages are used in the delay compensation loop controller.

A. Delay Compensation Algorithm

As seen in the previous paragraph, the microcontroller samples the conditioned signals and it adjusts the PWM parameters through a finite state machine in order to compensate τ_{d}. In order to obtain the delay compensation, for each couple of outputs, one output is defined as the Master, while the other as the Slave. The Master leg has null phase with respect to the PWM generation ramp and a duty cycle defined by the load controller, while the Slave has a duty cycle equal to (1-*D*) and its phase value is set in order to obtain the complementary output waveform. In order to compensate the delay τ_{d}, the control acts only on the Slave's phase and duty cycle parameters, whose definition is shown in Fig. 10. The actions required on such parameters are reported in Table I. The correction terms are saved in two accumulation variables, for each couple of outputs: one for the duty cycle, corr*x*.dc and one for the phase, corr*x*.ph, where the letter *x* is substituted by the number that identifies the couple.

TABLE I: Delay Compensation Truth Table

	Positive peak	**Negative peak**
Master rising	Decrease	Increase
Slave falling	Duty Cycle	Duty Cycle
Master falling	Decrease	Increase
Slave rising	Phase	Phase

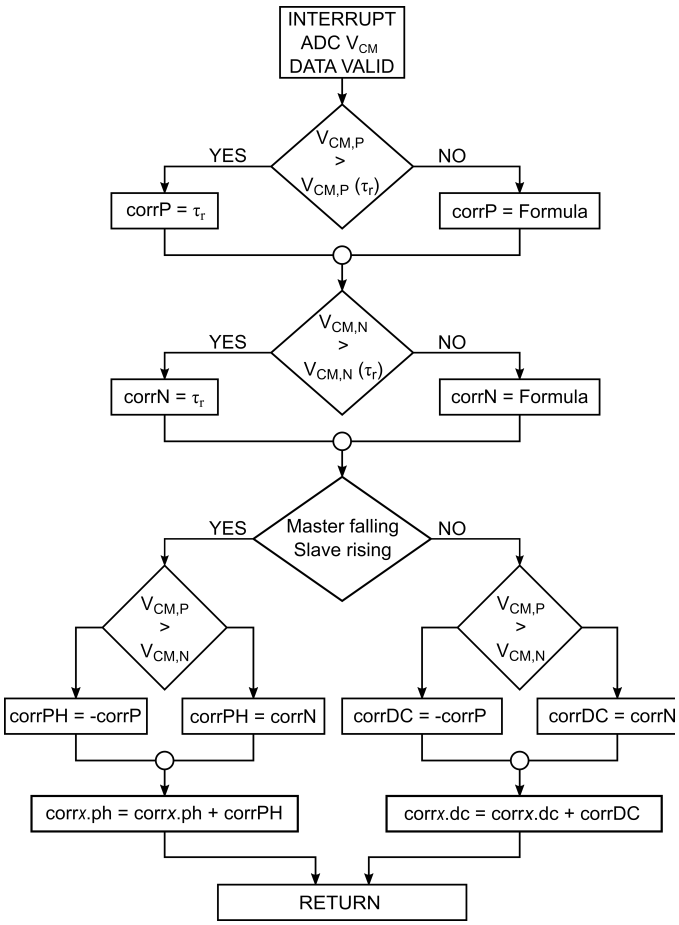


Fig. 11: Delay compensation algorithm flow chart.

The flow chart for the compensation of the output delay is shown in Fig. 11. Once the ADC conversion finishes, the level of the measured voltage peak leads to two cases for computing the correction term. In the first case the measured voltage indicates that the delay magnitude is greater or equal to the rise time, as in the cases (a), (c), (e) and (f) of Fig. 6 (left branches of the first two conditional statements)); the correction term in these cases will be equal to the rise time. Otherwise, the measured voltage indicates that the delay magnitude is lower than the rise/fall time, as shown in the cases (b), (d) of Fig. 6 (right branches of the first two conditional statements); the correction in these cases can be computed with a proportional relation derived in (3) and (12-13), i.e.:

$$\tau_{\mathrm{d}} = \left[\left(\frac{R_{\mathrm{ed}}}{R_{\mathrm{ed1}}} \cdot V_{\mathrm{ADC}} \cdot e^{\frac{t_{\mathrm{s}}}{R_{\mathrm{ed}} C_{\mathrm{ed}}}} + V_{\gamma} \right) \cdot \tau_{\mathrm{r}} \right] / \left(\frac{V_{\mathrm{PS}}}{2} \right). \tag{14}$$

The above equation is denoted as *Formula* in the flow chart. Then, the controller identifies the commutation event, between

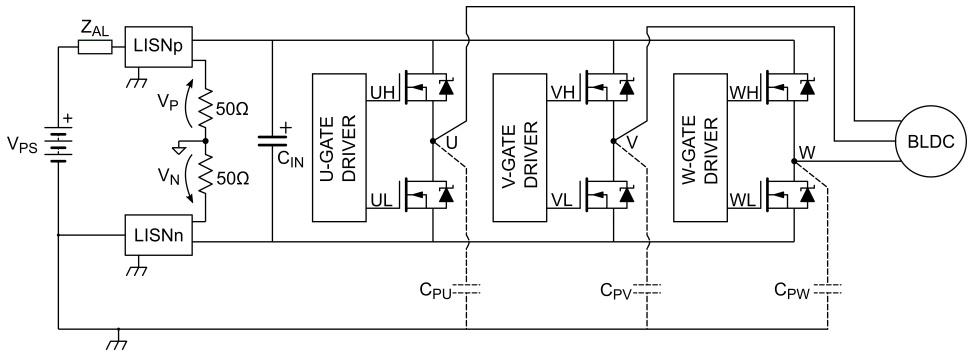


Fig. 12: Three-phase inverter schematic driving a BLDC motor.

the two present within a PWM period, related to the measured peak: Master rising/Slave falling or Master falling/Slave rising. According to the greater value between the measured $V_{\mathrm{CM,P}}$, $V_{\mathrm{CM,N}}$, in order to identify whether the measured peak is positive or negative, it assigns the previously derived corrections, *corrP* or *corrN*, to the phase correction variable, *corrPH*, or to the duty cycle correction variable, *corrDC*, as shown in the flow chart, using Tab. I. Thus, the correction is added to the respective accumulation variable in each PWM cycle.

If the transition times are not equal, as shown in Fig. 7, two peaks are generated at each commutation. In this case the control algorithm, according to the flow chart, is designed to obtain $V_{\mathrm{CM,p}} = V_{\mathrm{CM,n}}$, which minimizes the generated EMI.

Once the delay compensation control has been designed, it should be tested on a bipolar switched module. A specific application of the proposed technique is proposed in the following section, using as a reference circuit an inverter employed as brushless DC motor driver.

IV. Case of study: Three-phase inverter driving a BLDC motor

Among the applications of bipolar switched PWM circuits, the brushless DC (BLDC) motor drivers have gained popularity in recent years, in particular for their employment in the automotive field. Indeed, such motors provide both higher reliability and power density with respect to synchronous motors. BLDC motors are driven by three trapezoidal voltage waveforms, $\bar{V}_{\mathrm{U}}$, $\bar{V}_{\mathrm{V}}$ and $\bar{V}_{\mathrm{W}}$, obtained using a six-step modulation. The amplitude of such waveforms can be varied modulating the DC voltage using a three-phase inverter, shown in Fig. 12. Each inverter leg is composed of two nMOS, driven by a dual-output gate driver. For each step of the control, two out of three legs are modulated with bipolar PWM, while the third is left floating, and its output voltage shows an oscillating behavior due to the back electromotive force (BEMF).

Since for each step only two out of three legs are active, such an application is suitable for the validation of the proposed technique. The circuit used for the CM sensing should be slightly modified. Since only two of the three outputs are modulated and the third shows an almost constant voltage, the high-pass filter section of the sensing circuit comprises three capacitors connected to the three output nodes. Therefore,

TABLE II: Designed Component Values

Component	Value
C_{S}	680 pF
R_{S}	2.2 kΩ
C_{ed}	100 pF
R_{ed}	18.2 kΩ
R_{ed1}	9.1 kΩ
R_{ed2}	9.1 kΩ

considering the three phase inverter driving a BLDC motor, (2) can be written as:

$$V_{\mathrm{CM,OC}}(t) = \frac{V_{\mathrm{U}}(t) + V_{\mathrm{V}}(t) + V_{\mathrm{W}}(t)}{3}. \tag{15}$$

The DC voltage remains equal to $V_{\mathrm{PS}}/2$, while the maximum CM peak voltage magnitude becomes equal to $V_{\mathrm{PS}}/3$, because of the presence of the third leg floating voltage. Therefore, the delay can be evaluated as:

$$\tau_{\mathrm{d}} = \left[\left(\frac{R_{\mathrm{ed}}}{R_{\mathrm{ed1}}} \cdot V_{\mathrm{ADC}} \cdot e^{\frac{t_{\mathrm{S}}}{R_{\mathrm{ed}} C_{\mathrm{ed}}}} + V_{\gamma}\right) \cdot \tau_{\mathrm{r}}\right] / \left(\frac{V_{\mathrm{PS}}}{3}\right). \tag{16}$$

The circuit elements can be designed referring to the expression provided in Section III. The values obtained for the prototype we developed are listed in Tab. II.

About the compensation algorithm, at each BLDC control step the leg with a duty cycle *D* greater than 0.5 is defined as Master, while the other active leg is defined as Slave. Therefore, the two compensation accumulation variables, corr*x*.dc and corr*x*.ph, belong to the control step: thus, *x* = 1...6 represents the step number. Using this control strategy, the compensation variables are stored and recalled promptly each time the BLDC control finite state machine changes the active step.

Fig. 13 shows how the two control loops, one for the BLDC motor speed control and the other for the delay compensation, are integrated in the same system. The BLDC control loop is made up of the two cascaded controllers: a speed controller and a current controller. Their respective feedback variables are the rotor speed and the load current, the outputs are the phase and the duty cycle for both Master and Slave legs.

The delay compensation controller is independent from the above mentioned ones, as shown also in Fig. 13. It's

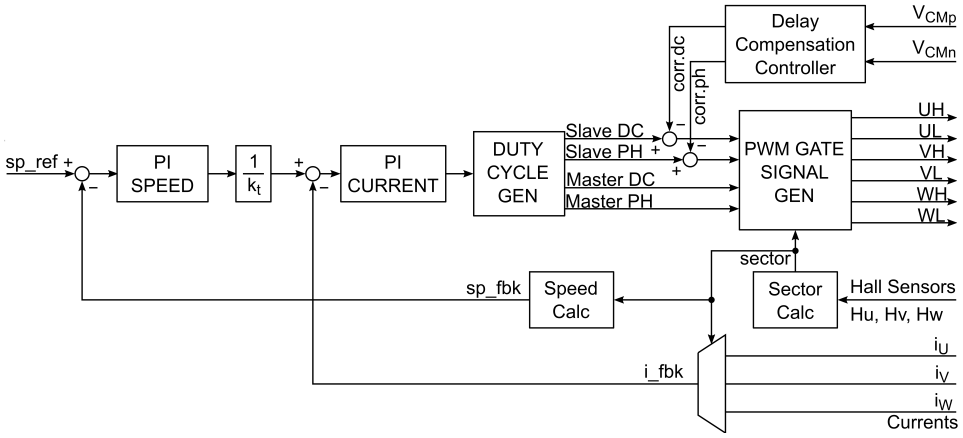


Fig. 13: Block scheme of the integration between the control loops of the load and of the delay compensation.

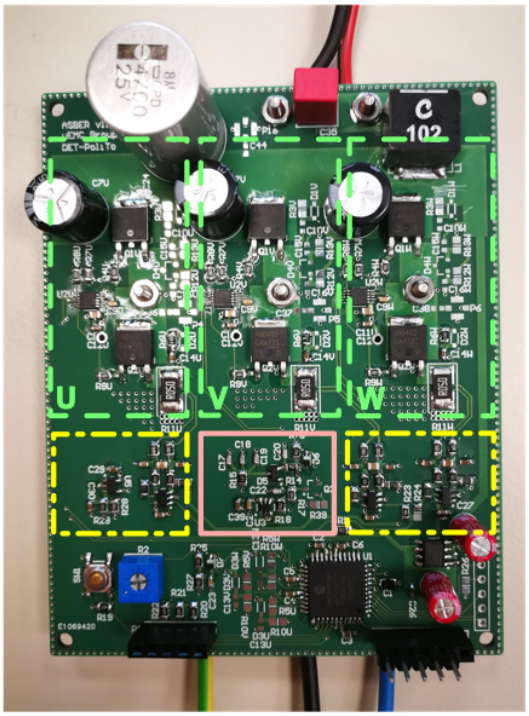


Fig. 14: BLDC motor driver PCB. The main PCB blocks are highlighted: in the dashed boxes the three inverter legs; in the dashed-dotted boxes the current sensing circuits; in the continuous box the delay compensation sensing circuit. The microcontroller and its power supply regulator are located in the lower part of the board.

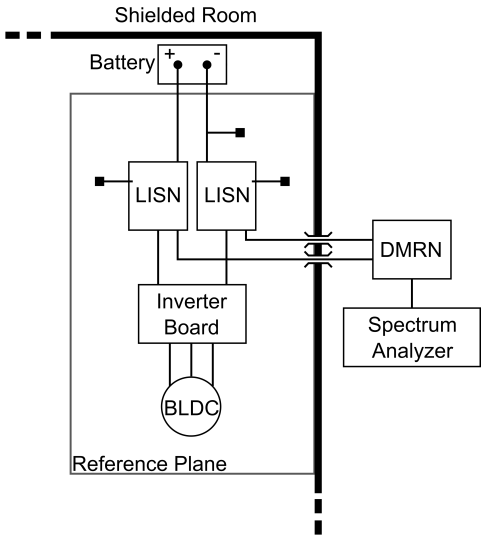


Fig. 15: Test bench layout top view.

outputs are added to the main controller output before being provided to the PWM gate signal generator. In principle, such a correction could affect the speed signal, but actually it is promptly compensated by the speed control loop.

In the section that follows the proposed delay compensation technique is validated experimentally.

V. Experimental results

In order to check the effectiveness of the proposed technique, a power inverter comprising the delay compensation circuitry has been designed and prototyped. The designed power module is shown in Fig. 14. The BLDC driver was supplied by a battery, providing $V_{\mathrm{PS}} = 12\,\mathrm{V}$, and it drove a 600 W BLDC motor used for radiator cooling. A DM second order filter was placed at the power supply input in order to reject completely the DM conducted EMI. The three legs of the inverter were made of two 40 V nMOS each, with low on-resistance, to limit the power dissipation. The nMOS of each leg were driven by a dual 1.6A gate driver with independent gate control, the LM5102 from TI [15]. The microcontroller chosen for this design was the dsPIC33EP128GS704 from Microchip [16]. It is supplied at 3.3 V, it has 1.04 ns resolution in modifying the PWM duty cycle and phase parameters. The ADC input voltage range is 0-3.3 V. Since the $V_{\mathrm{CM,p}}$ and $V_{\mathrm{CM,n}}$ peak magnitudes were in the range 0-4 V (0-$V_{\mathrm{PS}}/3$), assuming that over-voltage can be present at the output nodes, the scaling factor K magnitude was chosen to be 0.5. The block diagram of the test bench used to perform the EMC tests is sketched in Fig. 15. The battery providing the 12 V supply voltage was connected to two LISNs, as prescribed by CISPR 25 for remotely grounded equipment [6], whose chassis was

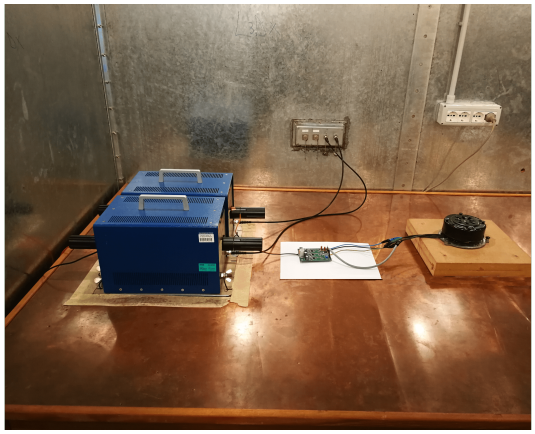


Fig. 16: Test bench.

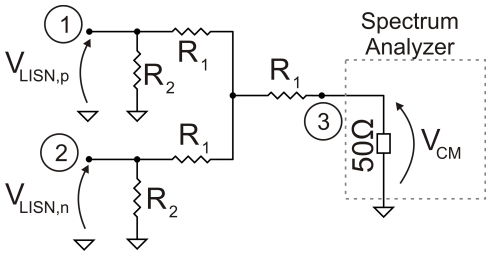
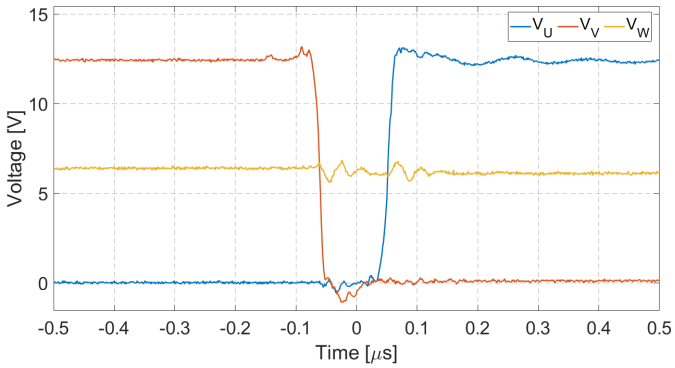
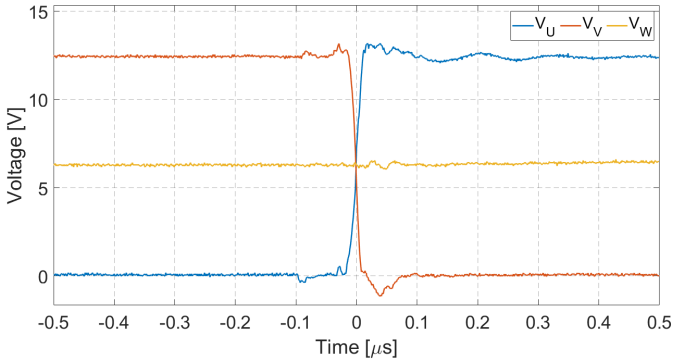


Fig. 17: Common mode voltage sensing network.



(a) τ_d=*100 ns, delay control loop not active.*



(b) $\tau_d \approx$*0 ns, delay control loop active.*

Fig. 18: Output voltages, V_U, V_V, V_W, measured in time domain with the delay control loop not activated (a) and activated (b).

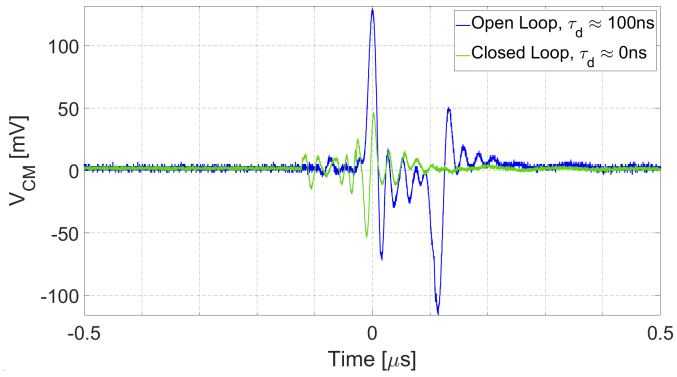


Fig. 19: Measured CM voltage at the output of the DMRN network.

contacted to a copper reference plane. The BLDC driver and the load were isolated from the reference plane by means of a paper sheet and a 50 mm thick wooden board, respectively. The test bench was set up in a shielded room in order to prevent the measurements from being corrupted by external interference. The test setup is shown in Fig. 16. The EMI signal at the output of each of the two LISNs was summed in order to measure only the CM voltage. The circuit used to perform such an operation was a passive differential mode rejection network (DMRN) [17], which schematic is shown in Fig. 17. Ports 1 and 2 were connected to the LISN_p and LISN_n outputs, respectively, whereas port 3 was connected to a spectrum analyzer [18]. The V_{CM} voltage at the output of the DMRN is scaled by a factor 0.536 (-5.4 dB), which is compensated in the measurement post-processing phase.

The conducted emission measurements were performed on the system considering two cases. The first, in which the delay compensation control loop was disabled; in this case three measurements have been carried out: with $\tau_\text{d} \approx 200$ ns, $\tau_\text{d} \approx 100$ ns and $\tau_\text{d} \approx 50$ ns. The second, in which the control loop was activated, meaning that the delay was compensated every PWM period. The output voltages for the two test conditions are reported in Fig. 18. It is possible to see that in the closed loop case the τ_d delay is fully compensated. The CM voltage at the output of the DMRN, is shown in Fig. 19. It can be seen that the disturbance is strongly reduced by the technique. The emission measurements were performed in the frequency ranges 150 kHz-30 MHz and 30 MHz-108 MHz, as prescribed in the standard. The results of the measurements carried out with the motor running at 400 rpm, with an average load current of 2 A are shown in Figs. 20 and 21. Looking at the measured spectra, from 150 kHz to 30 MHz the delay compensation control loop reduces the conducted CM EMI in the whole frequency range. Referring to the average delay case of $\tau_\text{d} \approx 100$ ns, the CM EMI presents a maximum reduction of 17 dB at 4 MHz. This result was obtained without CM filter neither at the PCB nor at the connector level.

In the frequency range from 30 MHz to 108 MHz the technique is not as efficient as in the lower part of the spectra, but the emissions are not worsened. This is due to the residual delay between the outputs, as explained in Section II, and to the asymmetries of the complementary switching waveforms.

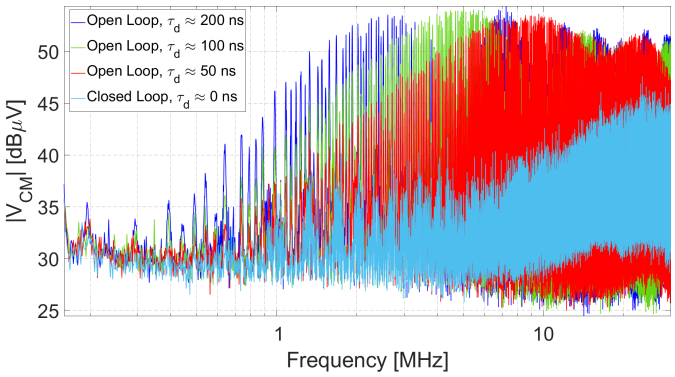


Fig. 20: Measurement results in the frequency range 150 kHz–30 MHz, with the motor running at 400 rpm. The blue, green and red spectra are referred to the delay control loop not activated, with $\tau_{\mathrm{d}} = 200\,\mathrm{ns}, 100\,\mathrm{ns}, 50\,\mathrm{ns}$, respectively. The light-blue spectra is the one obtained with the delay compensation loop activated.

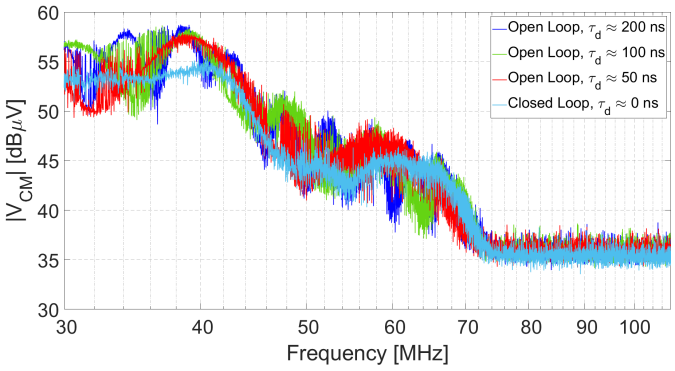


Fig. 21: Measurement results in the frequency range 30 MHz–108 MHz, with the motor running at 400 rpm. The blue, green and red spectra are referred to the delay control loop not activated, with $\tau_{\mathrm{d}} = 200\,\mathrm{ns}, 100\,\mathrm{ns}, 50\,\mathrm{ns}$, respectively. The light-blue spectra is the one obtained with the delay compensation loop activated.

VI. Conclusion

In this work, a closed loop software solution to mitigate the conducted emission of power switching circuits has been proposed. It can be used in power circuits featuring complementary power switching nodes because it implements an adaptive fine zeroing of the time delay, which is introduced by the gate drivers and the interconnects of the power sections. This goal was accomplished with a simple and low cost sensing circuit and an appropriate control algorithm. Since only the output voltages are aligned and the dead time between the gate signals of a single leg is always present and unchanged, no cross conduction, thus no safety issues, can occur.

In order to validate the closed loop delay compensation technique, a three-phase inverter driving a 600 W BLDC motor was prototyped. The designed system included both the motor control circuitry and the one used to reduce the CM EMI. The proposed approach has been demonstrated to be effective in reducing the CM EMI up to 30 MHz, with reduction peaks up to 17 dB. The proposed approach, unlike the SSM one, allows one to reduce the energy of the CM conducted emission effectively. Since these two software solutions are independent, they could be both used in the same system for a further reduction of the EM emission level.

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