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***Abstract*— We propose a workflow for the analysis and mitigation of 3D ICs to Single Event Transient by upsizing the sensitive transistors. The workflow is applied to 45-nm 3D LUT and the results show a 37% reduction in failure rate.**

Keywords—3D IC, Single Event Transient, Gate Sizing.

I. INTRODUCTION

Since the development of the transistor and its implementation in Integrated Circuits (ICs), the semiconductor industry has made huge improvements in the performance and power consumption by device scaling, following Moore's law. Moore's law observes that the number of transistors that fit on an IC doubles approximately every two years. However, as the device size decreases, the demand for performance kept growing and traditional scaling was not enough to follow Moore's law [1]. This has led to the introduction of 3D ICs as a new direction in the semiconductor device research.**Error! Reference source not found.**. 3D ICs are integrated circuits which implementation is distributed among several layers connected by short, vertical, and fine-grained vias [3]. In fact, by stacking multiple silicon layers with vertical connections by Through Silicon Vias (TSVs), 3Ds are the most promising candidate for high performance and low power computing by offering higher integration density, less power dissipation, and higher achievable clock frequency. Additionally, the overall system-on-chip cost and performance can be optimized by dedicating different functionalities to different tires layers [4].

Given all the potential benefits of 3D integration, it is essential to understand the key challenges that are holding back the technology from completely ruling the semiconductor industry. One of the main issues is the reliability of 3D ICs [5]. Decreasing the size of transistors makes the devices more vulnerable to soft errors. Soft errors are caused by the particles interacting within the device and releasing their energy. The released energy might create a voltage pulse known as Single Event Transient (SET) at sensitive nodes which might propagate and reach to the storage element and change the logic state of the circuit. However, due to the novelty of this technology, few studies have been dedicated to evaluate the sensitivity of these devices to radiation-induced soft errors [6]. On the other hand, considering 2D ICs, several transient error mitigation techniques have been proposed [7][8]. Gate sizing is a simple yet effective soft error mitigation technique [9]. Increasing the size of the gate's transistors is increasing the output capacitance of which charging/discharging results in an SET of the hit gate [10].

The main contribution of this work is to propose an approach for the analysis and mitigation of 3D ICs regarding radiation-induced transient errors. This approach is based on a toolchain composed of our developed tool, Rad-Ray, which is able to mimic the effect of radiation particles interacting within a given 3D device and computing the generated SET pulse features and location of the affected transistors in different tiers. The tool is integrated with the commercial electrical simulation tool, HSPICE, that allows to inject SET pulses in multiple nodes of the circuit and evaluate the dynamic failure rate. As a second part of the toolchain, a mitigation solution is proposed which acts by resizing the vulnerable transistors which increase node capacitance and decrease the sensitivity regarding SET. The proposed workflow has been applied to 3D 4-inputs LUT which shows the reduction of 37% of Error Rate.

This paper is organized as follows: Section II is providing background on 3D ICs. Section III describes the developed workflow in detail. Section IV elaborates on the experimental results. Finally, Section V reports the conclusion and future works.

II. BACKGROUND

The 3D-integration technology process consists in stacking several portions of an integrated circuits vertically with fine-grain 3D interconnections **Error! Reference source not found.**. 3D ICs are made by layers of 2D chips placed on separate layers stacked on top of each other which leads to the shorter interconnections, lower delay, and faster clock frequency. Figure 1 shows a 3D Integrated Circuits section with two tires.

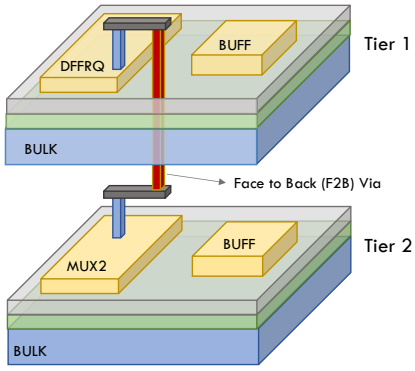

Fig. 1. An example of a 3D Integrated Circuits section with two tiers and a Face to Back (F2B) interconnection via between a MUX2 and a DFFRQ cell.

In order to design an efficient 3D LUT usable on 2-tires 3D FPGAs, a 4 inputs LUT has been designed. In this design, a cascade of 2-inputs MUXes were placed at tire 1 while configuration memory (CM) was placed close to the inputs of the first 2-inputs MUX level in tier 2. Each CM's output pin was connected to the respective MUX configuration inputs using a face-to-back interconnection via as represented in Figure 1.

III. The Analysis and Mitigation Workflow

In order to analyze the sensitivity of the circuit under the test and apply an efficient mitigation approach, we developed the workflow represented in Figure 2. The analysis phase starts by developing an electrical model of the LUT. The electrical netlist and the 3D layout of the design are provided to Rad-Ray, our developed tool for simulating the passage of a radiation particle through several layers of the device and generating multiple SETs in multiple layers. Rad-Ray interfaces with electrical HSPICE fault injection to evaluate the failure rate caused by SETs injected in the affected transistors of the design. The mitigation phase relies on increasing the size of the vulnerable transistors, leading to the reduction of the amplitude and duration of the generated SET source pulse and eventually to the reduction of the failure rate.

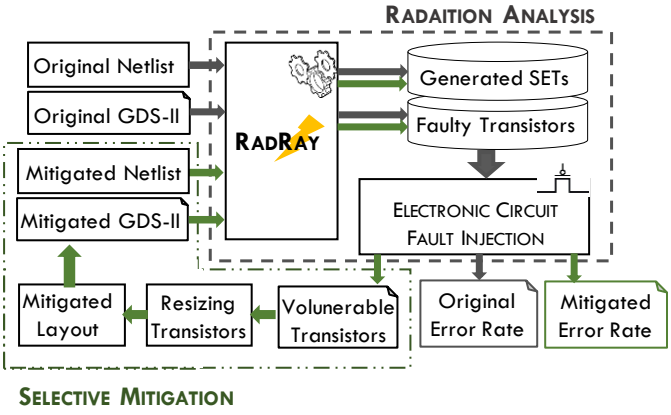

Fig. 2. The developed radiation effect analysis and mitigation workflow.

A. Rad-Ray Radiation Analysis

As a first stage, we developed an electrical model of 4-inputs LUT. The 3D layout description of the circuit has been developed using the commercial k-layout tool and it has been extracted in terms of Graphic Data System-II (GDS-II). The original GDS file and with the netlist of the design have been provided to Rad-Ray. Rad-Ray is an in-house developed tool for simulating the passage of the radiation particles through the silicon matter of modern integrated circuits including 3D ICs. Considering 3D ICs, Rad-Ray simulates the passage of one single particle through multiple layers of the device and computes the loss of energy in each layer, and reports the generated transient voltage pulse response in different layers due to the single particle incident. As a result, Rad-Ray reports the list of generated SET pulses in terms of amplitude and duration of the pulse and the location of the faulty transistors. More details about Rad-Ray tool are provided at [11].

B. Electrical Fault Injection

As a result of Rad-Ray analysis, the generated SET pulses, in terms of duration and amplitude, and the locations where the pulses have been generated are reported. Please notice that as a result of one single striking particle, multiple SETs in multiple layers might be generated and reported by Rad-Ray in the SET database. Figure 3 represents the 3D LUT in which memory cells which compose the configuration memories are placed in tire 1 and MUXes constructing the LUT are placed in tier 2. The figure represents that as an effect of one single incident particle, two transistors on two different tiers have been affected.

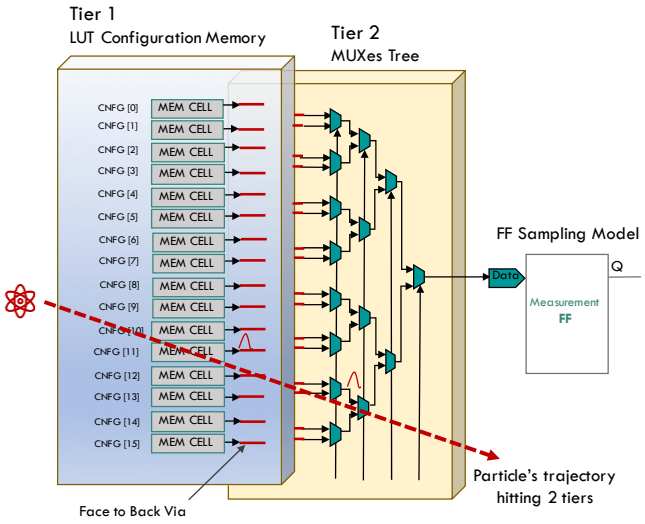

Fig. 3. The developed 3D LUT model and the view of a single particle generating multiple SETs on two different layers.

The electrical fault injection environment developed in HSPICE uses this information to inject multiple SET pulses in the affected transistors on different layers and propagate the injected SETs to the output of the LUT in order to identify if the injected SETs create an error in the output of the LUT.

To emulate the SET pulse, the original netlist of the LUT has been automatically modified by inserting a transient voltage source connected to the affected node of the transistor in the netlist corresponding to the physical location identified by Rad-Ray. In order to verify whether the SET propagating to the output of the LUT is traversing also other resources reaching the output of the circuit and create an error, we connected the output of the LUT to a measurement Flip-Flop, as represented in Figure 3. The generated pulses inside the LUT might propagate until the output of the LUT and *Data* Signal of the FF. However, depending on the features of the generated pulses, location of the incident, and the internal transistors that have been affected, the pulses might filter or broaden in terms of duration of the pulse or have a reduction of the amplitude while propagating. Therefore, the propagated pulse in the *Data* signal of the *FF* might not fulfill the requirement of the technology to be captured and creates an error in the overall functionality of the circuit. Using this

setup, it is possible to classify the SETs which becomes errors and report the Dynamic Error Rate of the LUT. Moreover, the transistors of the design have been classified. Not all the transistors in which the SET pulse is generated are identified as vulnerable ones. Depending on the physical location of the transistor on the layout of the design, some transistors are facing stronger SET pulses in terms of the duration and amplitude of the pulse which leads to the stronger pulse at the output of the LUT with higher probability to be captured by storage element and create a failure. These vulnerable transistors have been reported to the mitigation phase of the workflow.

C. *MUX2 resizing*

As a result of the analysis phase, the vulnerable transistors of the design have been provided to the mitigation phase. Mitigation phases act by upsizing the vulnerable transistors in order to increase the node capacitance. Increasing the node capacitance leads to shorter and narrower SETs in terms of amplitude and duration of the pulse. Therefore, the generated pulse has less probability to fulfill the requirement of the technology and be captured by the storage element. We decided to apply the mitigation to the most critical region of the MUX2 which consists on the MUX select signal node. For the considered node, we doubled the area of the sensitive location identified by the MUX heatmap, as depicted in Figure 5.a. The original and the new layout are illustrated in Figure 4.a and 4.b respectively.

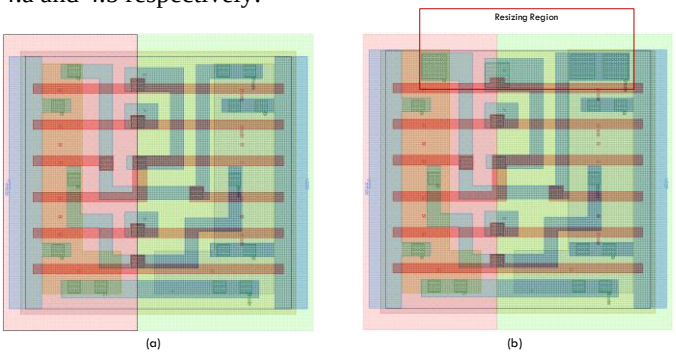

Fig. 4. The MUX2 in-cell resize on the Select signal nodes: the original MUX layut (a) and the resized one (b).

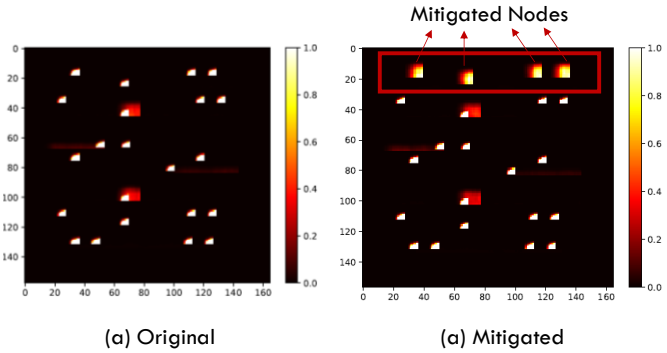

Fig. 5. The MUX's SET sensitivity heat-map (a) Original (b) Mitigated.

Figure 5 represents an accurate heatmap of the most sensitive volumes of the single MUX cell in which the voltage values are normalized between 0 to 1 volt. As it can be observed, the mitigated nodes of the design show less sensitivity with respect to the original one.

IV. Experimental Results

In order to evaluate the SET sensitivity of the 3D LUT, the electrical design of the LUT has been developed using FreePDK physical library at 45 nm and adopting the electrical Predictive Technology Model (PTM) of 45 nm for bulk CMOS. Using the commercial K-layout tool, the layout description of the circuit has been extracted in terms of Graphic Data System-II (GDS-II). The netlist and layout of the circuit have been provided to the Rad-Ray tool together with the radiation profile to perform the radiation analysis. The radiation analysis has been performed applying the Heavy Ion profile related to the UCL facility [12]. The characteristic of the analyzed particles is reported in Table I.

TABLE I . Heavy ion particles analyzed by the Rad-Ray analysis tool

Ion	DUT Energy [MeV]	Range [μm Si]	LET [MeV/mg/cm^2]
$^{13}C^{4+}$	131	269.3	1.3
$^{40}Ar^{12+}$	379	120.5	10.0
$^{58}Ni^{18+}$	582	100.5	20.4
$^{124}Xe^{35+}$	995	73	62.5

We performed a simulation of 10,000 particles for each Ion affecting physical 3D description of the LUT under the analysis. The Rad-Ray radiation analysis results are reported in Figure 6, where the static and dynamic cross-section of the LUT for different Heavy Ion are shown. The experimental analysis shows that the dynamic cross-section of the mitigated MUX is 1.81 times smaller than the original one on the average. Interestingly, the static cross section of the original MUX is lower than the mitigated one. This aspect is related to the greater number of smaller transient pulses catched by the wider sensitive nodes area.

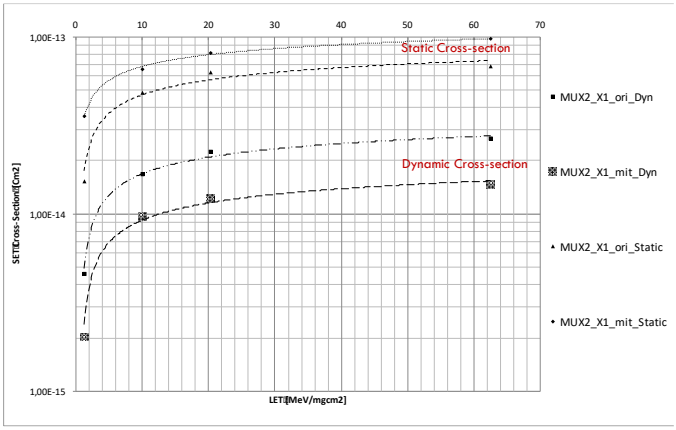

Fig. 6. Single Event Transient Cross-Section [cm^2] for static radiation analysis of 45 nm 3D LUT.

As a result of the Rad-Ray, the location and features of the generated SET pulse in the LUT have been identified. The original electrical netlist has been modified in order to inject SET pulses in the MUXs of the LUT. The output of the measurement FF has been observed in order to identify whether the injected SET propagates to the output of the LUT

and if the pulse that reached to the input of the FF is sufficient in terms of amplitude and duration to create a failure in the output of the measurement FF. Moreover, as a result of the injection phase, the vulnerable transistors have been identified. Vulnerable transistors are defined as the transistors which create failure at the output of the FF in a case that they are the location of source SET pulses. The vulnerable transistors have been used in the mitigation phase. The mitigation acts by upsizing the vulnerable transistors in order to increase the capacitance of the node. Considering the LUT under the study, the transistors driving the 4 inputs of the LUT are defined as the most sensitive one. Therefore, the size of these transistors has been doubled with respect to the original one. Figure 5 represents the Dynamic Error Rate as the percentage of the failures with respect to the number of injected SET pulses for both the original and mitigated versions. It shows a reduction of the failure rate for the mitigated version while the area and power consumption overheads represented in Table II are negligible.

TABLE II Comparison between original and mitigated LUT4

Circuit Version	Area Usage [μm^2]	Power Usage [μW]
Original	31.28	0.4348
Mitigated	32.14	0.4549

Figure 7 represents the SET cross-section for the original and mitigated version considering particle with the highest energy, *Xe*. As it can be observed, by upsizing the sensitive transistors, the rate of generating small SETs is increasing while the middle and high SETs are decreasing. To elaborate more, since by increasing the size of the transistors, the surface exposed to radiation is increasing, a higher amount of radiation particles, and accordingly, a higher number of SET pulses are expected. However, since the capacitance of the vulnerable nodes increased, the same particle that can generate a strong pulse (medium-high) in the original version, in the mitigates version can generate a smaller pulse.

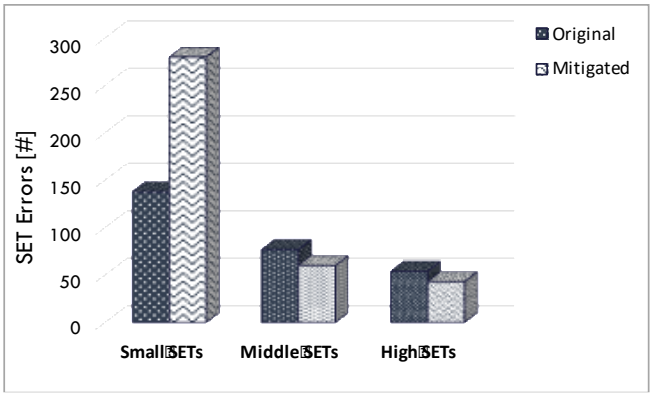

Fig.7. SET Cross-Section Comparison between original and mitigate version considering the energy of particle *Xe*

Therefore, the number of small SETs in the mitigated version increases while the number of middle and high SETs are lower in the mitigated version. The smaller pulse will propagate through the LUT netlist and the pulses arriving in the input of the measurement FF are smaller concerning the original version which leads to the lower probability to fulfill the requirement of the technology and be captured by the storage element.

V. Conclusions and Future Work

In this paper, we applied a selective mitigation technique on the vulnerable transistors of the MUXes of 3D LUT placed in tier 1 which reduces the failure rate for 37% with negligible area overhead.

As a future work, we plan to propose a new 3D layout which increases the Single Event Transient mitigation capabilities acting on the other region of the 3D LUT without affecting the area and power overhead.

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