Design strategy of a 2.8–3.6 GHz 20W GaN Doherty power amplifier

Design strategy of a 2.8–3.6 GHz 20 W GaN Doherty power amplifier

Ardit Veshaj[1], Anna Piacibello[1,2], Chiara Ramella[1], Abbas Nasri[1], Vittorio Camarchia[1], Marco Pirola[1]
[1]*Dept. Electronics Telecommunications, Politecnico di Torino*, Torino, Italy
[2]*Dept. Electronics Telecommunications and M.E.C.S.A., Politecnico di Torino*, Torino, Italy
arditveshaj@hotmail.com, anna.piacibello@polito.it

***Abstract*—This paper presents the design of a 20 W GaN Doherty Power Amplifier working in the range 2.8 GHz–3.6 GHz. The design strategy adopted for the design of the Doherty output combiner is discussed, which consists in embedding the device parasitics into the latter, implemented as a multi-stage quarter-wavelength transformer, in order to achieve wideband behaviour. The saturated output power ranges from 42 dBm to 44 dBm, with a corresponding drain efficiency in excess of 47%. The efficiency at 6 dB of output back-off is higher than 42% over the whole frequency band, and the small-signal gain is higher than 10 dB. Due to the discrepancies of the measured scattering parameters compared to the simulated ones, which could not be corrected with post-tuning, a redesign of the prototype is ongoing.**

***Index Terms*—RF power amplifier, efficiency, Doherty, back-off, 5G**

I. Introduction

One of the most critical building blocks of a radio transceiver is the power amplifier (PA), responsible of boosting the modulated signals before transmission, as it consumes a large part of the energy dissipated by the entire radio system. The performance of the PA can indeed dominate the overall transmitter performance, not only in terms of conversion efficiency, but also concerning linearity, reliability, yield, heat dissipation, size and eventually cost.

PA topologies maximizing efficiency at saturation are not suited for present complex modulation schemes. In this case average efficiency can be restored resorting to system level solutions like envelope tracking or outphasing [1]. However, circuit level solutions like the Doherty PA, either single [2] or dual input [3], [4] are today very popular in the base station market because require less additional circuitry. Furthermore, the linearity of the stage must be kept under control since PA inherently linear without any additional linearisers are often required [5].

In this work a 20 W GaN Doherty power amplifier is designed at 3.5 GHz, targeting the FR1 5G-new radio frequency band. One of the major issues affecting the DPAs, namely the limited bandwidth, is optimised by ad-hoc design solutions. A first demonstrator is fabricated in hybrid technology, but a considerable frequency shift hampers its complete characterisation in the targeted frequency band. Despite that, preliminary measured results are presented while the redesign is ongoing.

II. Design

A single-input DPA is designed at 3.5 GHz adopting two identical active devices, namely the 10 W packaged GaN transistors (CGH40010F) from Wolfspeed Inc., according to the scheme of Fig. 1. The main device is biased in class-AB (V_{DS} = 28 V, I_{D} = 70 mA), while the auxiliary device is biased in class-C (V_{DS} = 28 V, V_{GS} = -7.0 V). Unconditional stability of the devices is ensured both in-band and at low frequency by means of a parallel R-C circuit in series to the gate (R = 33 Ω and C = 3.3 pF) together with a 50 Ω resistance on the gate bias line.

A multi-stage transmission line (TL) based combiner is adopted to achieve wideband operation. To ensure the required impedance inversion on the main branch, and provide matching to 50 Ω, three quarter-wavelength transformers are adopted. Conversely, two quarter-wavelength transformers on the auxiliary path enforce the required matching without any impedance inversion. Moreover, to overcome one of the main limitations of the DPA i.e. its narrow bandwidth, the output parasitics of the active devices are embedded into the Doherty output combiner. This also eliminates the need of offset lines, which often represent another bandwidth limiting factor in DPAs. The output reactive parasitic elements are modelled with a parallel capacitance $C_{\mathrm{DS}} = 1.3\,\mathrm{pF}$ and a series inductance $L_{\mathrm{D}} = 0.66\,\mathrm{nH}$ for the main device and $L_{\mathrm{D}} = 0.85\,\mathrm{nH}$ for the auxiliary. C_{DS} and L_{D} are embedded in the first quarter-wavelength transformer of the output matching network, which was first designed as a π-network adding a series inductance (L_{series}) and a shunt capacitance ($C_{\mathrm{shunt}} = C_{\mathrm{DS}}$) and finally implemented in distributed form, as shown in Fig. 2. The characteristic impedance $Z_{\infty,\mathrm{emb}}$ of the transformer is derived from [6]:

$$Z_{\infty,\mathrm{emb}} = \frac{1}{\omega_0 C_{\mathrm{DS}}} = \omega(L_{\mathrm{D}} + L_{\mathrm{series}}) = 35\,\Omega. \qquad (1)$$

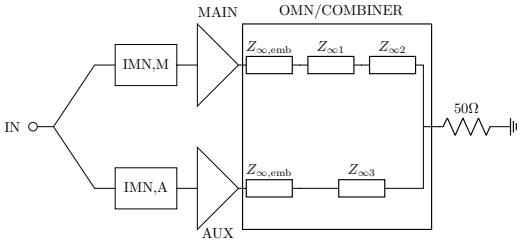

Fig. 1. Block diagram of the complete DPA under design.

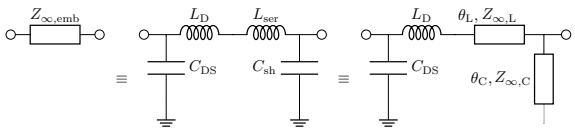

Fig. 2. Embedding of the drain parasitics into the output matching/combiner.

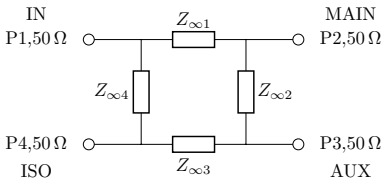

Fig. 3. Circuit schematic of the input branchline.

The capacitance C_sh is transformed into a open stub of 30° at 3.5 GHz, in order to short circuit the third harmonic, while the second harmonic is shorted by properly designing the drain bias line.

From theoretical calculations, the optimum load at the intrinsic drain plane is 25 Ω for both devices at saturation. According to 6 dB DPA operation, the optimum load for the main in back-off is 50 Ω. The characteristic impedances $Z_{\infty,1}$, $Z_{\infty,2}$, $Z_{\infty,3}$ of the other $\lambda/4$ TLs are chosen according to [7] in order to achieve wideband matching and maintain the proper load modulation:

$$R_{\mathrm{main,load}} = \frac{Z^2_{\infty,\mathrm{emb}}}{Z^2_{\infty,1}} \frac{Z^2_{\infty,2}}{R_\mathrm{L}} \tag{2}$$

The optimum input impedances determined from source-pull simulations for the main and auxiliary are $Z_{\mathrm{in,main,opt}} = (4.5 - j13)\,\Omega$, and $Z_{\mathrm{in,aux,opt}} = (4.5 - j10)\,\Omega$, respectively. The input matching networks are designed according to the lowest in-band ripple criterion [8].

The circuit will be fed by a single RF input source, thus requiring an input power splitter able to provide the proper power splitting ratio k between main and auxiliary. Adopting identical devices and V_DS for the two stages calls for an uneven power splitting, in this case:

$$k = \frac{P_{\mathrm{in,main}}}{P_{\mathrm{in,aux}}} = 0.69 \tag{3}$$

The uneven power splitting is achieved with a branchline coupler, providing isolation between the two branches and introducing a 90° phase delay at the auxiliary input with respect to the main. Such phase difference compensates the phase delay introduced by the output impedance transformer. The coupler is made of four quarter-wavelength transmission lines arranged as shown in Fig. 3, with characteristic impedances chosen to achieve the desired power splitting ratio k:

$$Z_{\infty1} = Z_{\infty3} = Z_0\sqrt{\frac{k}{1+k}} = 33.9\,\Omega \tag{4}$$

$$Z_{\infty2} = Z_{\infty4} = Z_0\sqrt{k} = 41.5\,\Omega. \tag{5}$$

III. Performance

A. Simulations

The designed DPA is implemented in microstrip on a FR4 substrate with 0.8 mm thickness and 4.6 dielectric constant. The resulting simulated small-signal performance is shown in Fig. 4. The input and output return losses are better than 10 dB in the 3–3.8 GHz, while the simulated gain is higher than 10 dB from 2.7 GHz to 3.6 GHz. Accordingly, the large signal CW simulations are performed over the 2.8–3.6 GHz frequency range. The simulated performance versus input power is shown in Fig. 5, while the behaviour versus frequency is presented in Fig. 6. The saturated output power ranges from 42 dBm to 44 dBm, with a corresponding drain efficiency in excess of 47%. The efficiency at 6 dB of output back-off is higher than 42% over the whole frequency band. The small-signal gain is higher than 10 dB, as expected from the scattering parameters simulations. The simulation results are almost aligned with the state of the art for 5G applications in the upper sub-6 GHz band [9].

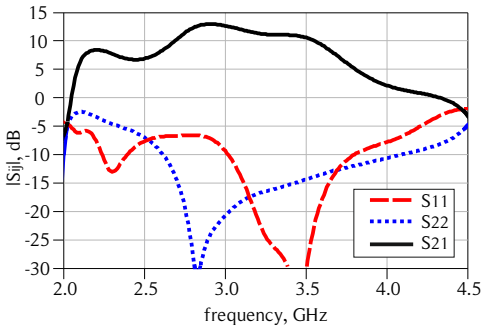

Fig. 4. Simulated scattering parameters.

B. Measurements

The prototype is fabricated, assembled and mounted on an aluminum carrier. Its photograph is reported in Fig.7.

The small-signal characterisation is reported in Fig. 8. A significant frequency shift is visible, especially on S_{21}, compared to simulations. As a consequence, the realised amplifier is not suitable to fully cover the targeted frequency band. Since the

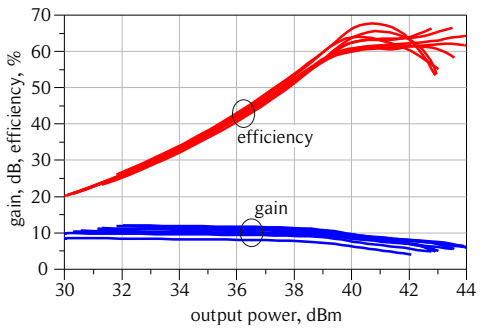

Fig. 5. Simulated drain efficiency and gain versus output power from 2.8 GHz to 3.6 GHz.

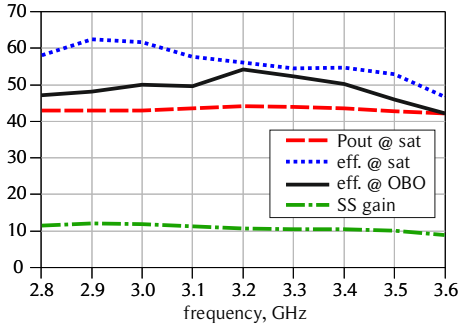

Fig. 6. Simulated CW performance versus frequency.

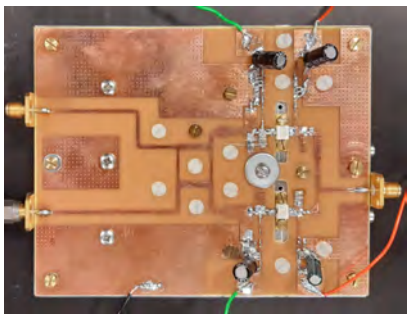

Fig. 7. Photograph of the realised prototype.

discrepancy could neither be ascribed to inaccuracies in the discrete components nor to the mounting process, and could therefore not be recovered by post-tuning, a re-design is in progress. To verify the behaviour of the output combiner in

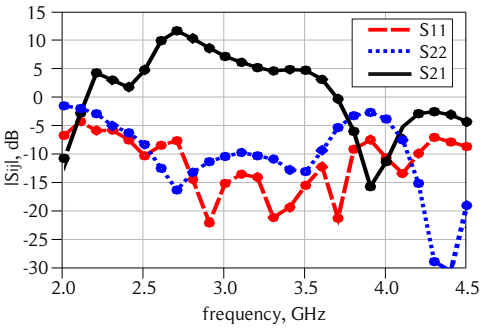

Fig. 8. Measured scattering parameters.

the expected working band, a large signal CW characterisation has also been performed at 2.8 GHz (the peak gain frequency point from small-signal characterization). The output power, drain efficiency and gain versus input power of the DPA, reported in Fig. 9, clearly indicate the proper Doherty behaviour, suggesting that the output combiner is enough robust to process variations to assure the correct load modulation also in presence of the large inaccuracy experienced in the present manufacturing. This is probably not the case for the input branchline which, apart from a very narrow frequency range, cuts the gain of the stage to few dBs, hampering any further large signal tests of the DPAs.

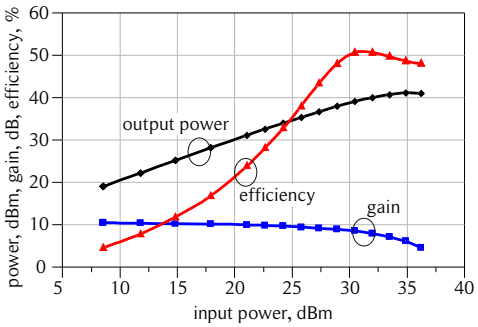

Fig. 9. Measured CW performance versus input power at 2.8 GHz.

Conclusion

The design of a GaN Doherty Power Amplifier targeting 20 W and a 6 dB back-off high-efficiency region in the range 2.8–3.6 GHz has been presented. Wideband behaviour is achieved thanks to the embedding of the device parasitic elements into the Doherty output combiner and its implementation as multi-stage quarter-wavelength transformer. The simulation results are almost aligned with the state of the art for the 5G applications. However, due to the discrepancies of the measured scattering parameters compared to the simulated ones, which could not be corrected with post-tuning, a redesign of the prototype is ongoing.

References

[1] A. Piacibello, R. Quaglia, M. Pirolaf, and S. Cripps, "Design of an S-Band Chireix Outphasing Power Amplifier Based on a Systematic Bandwidth Limitation Analysis," in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, 2018, pp. 186–189.

[2] J. H. Qureshi, W. Sneijers, R. Keenan, L. C. N. deVreede, and F. van Rijs, "A 700-W peak ultra-wideband broadcast Doherty amplifier," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1–4.

[3] A. R. Qureshi, M. Acar, J. Qureshi, R. Wesson, and L. C. N. de Vreede, "A 112 W GaN dual input Doherty-Outphasing Power Amplifier," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, pp. 1–4.

[4] A. Piacibello, R. Quaglia, V. Camarchia, C. Ramella, and M. Pirola, "Dual-input driving strategies for performance enhancement of a Doherty power amplifier," in *2018 IEEE MTT-S International Wireless Symposium (IWS)*, 2018, pp. 1–4.

[5] R. Quaglia, V. Camarchia, M. Pirola, J. J. M. Rubio, and G. Ghione, "Linear GaN MMIC Combined Power Amplifiers for 7-GHz Microwave Backhaul," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 11, pp. 2700–2710, Nov 2014.

[6] J. J. Moreno Rubio, V. Camarchia, R. Quaglia, E. F. Angarita Malaver, and M. Pirola, "A 0.6–3.8 GHz GaN Power Amplifier Designed Through a Simple Strategy," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 6, pp. 446–448, June 2016.

[7] C. Monzon, "A small dual-frequency transformer in two sections," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 4, pp. 1157–1161, April 2003.

[8] D. E. Dawson, "Closed-form solutions for the design of optimum matching networks," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 1, pp. 121–129, Jan 2009.

[9] J. Zhou, W. Chen, L. Chen, and Z. Feng, "3.5 -GHz High-Efficiency Broadband Asymmetric Doherty Power Amplifier for 5G Applications," in *2018 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, May 2018, pp. 1–3.