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ALL-OPTICAL FREQUENCY ENCODED DIBIT-BASED PARITY GENERATOR USING REFLECTIVE SEMICONDUCTOR OPTICAL AMPLIFIER WITH SIMULATIVE VERIFICATION*

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Abstract. *High-speed signal computation and communication are an essential part of modern communication that increases optical necessity. Therefore, researchers developed different types of digital devices in the all-optical domain. Due to the versatile gain medium of reflective semiconductor optical amplifiers (RSOAs), it has various important applications in passive optical networks. In comparison with semiconductor optical amplifier (SOA), RSOAs exhibit better gain performance because of their double pass property. Therefore, RSOA shows better switching properties. In this communication, co-propagation scheme of RSOA is used to design and analyze a frequency encoded dibit-based parity generator. Taking the advantages of RSOA like high switching speed, low noise, high gain, and low power consumption, the proposed design achieves these qualities. This design simulated in MATLAB and simulated outputs accurately verify the truth table.*

Key words: *Optical communication, Reflective semiconductor optical amplifier, Frequency encoding, Dibit-based logic system, Parity generator.*

1. INTRODUCTION

The photon becomes more popular for information transmission [2, 3]. Photons can carry information at a superfast speed. Therefore, the researchers are very interested to design photon-based devices [4, 5] instead of electron-based devices. The data signal can be transmitted in long-range using different types of encoding techniques [6-8]. The frequency encoding [9-13] technique is more reliable in long-range signal propagation. In optical communication, the adder [1, 14-16], subtractor [17], comparator [9, 18], parity generator are basic components for arithmetic, decision-making circuits, logic units [19-25], and memory units [11].

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These are the basic building blocks of optical data processors. In the frequency encoding concept [1], the digital logic states '0' and '1' are indicated by frequencies υ_1 and υ_2 respectively. In communication and data storage systems, the parity generator is a very essential device. In the last decade, researchers are working for parity generators.

From the literature survey, it is found that the even/odd parity generator units are not designed in a single device and also dibit-based logic and frequency encoding scheme is also first time implementation. In this communication, a frequency encoded dibit-based even/odd parity generator in the all-optical domain, using add/drop multiplexer (ADM) and reflective semiconductor optical amplifier (RSOA) is devised. From the previous version [1], we adopted the logic of SUM from the design of a half adder using RSOA and ADM. In half-adder design [1], two input dibit-based logic is used but in this proposed design, we have implemented three inputs dibit-based logic. So the operation of the three inputs dibit-based logic is much more complicated than the previous version [1]. This proposed design is a single device for the even/odd parity generator units and it has no extra control terminal. As a result, the devised design reduces the space of the device as well as simultaneously generates even and odd parity. Introducing the dibit-based logic in this design, one can be expected a high degree of parallelism. The frequency encoding and dibit-based systems reduce also the bit error problems and enhance the speed of operation in long-range transmission. Since RSOA has ultrafast switching property with low noise, so the proposed design operates at ultrafast speed. In the results and discussion section, the proposed design is compared with the other designs [26, 28, 33, 36] which are given in Table 3.

The remaining part is structured as follows: Related works are described in Section 2. The working principle of RSOA and ADM are described in Section 3. Section 4 describes the operation scheme of the proposed parity generator. The simulation experiment of the proposed model is described in Section 5. The results and discussion of the proposed system are presented in Section 6. Finally, the conclusions with potential future works are given in Section 7.

2. RELATED WORKS

The researchers are working for parity generators during the past several years. Some of these legendary works are discussed here. Chowdhury et al. [26] have introduced a design of 4-bit parity generator and checker using non-linear material-based switches. Using spatial light modulator and Savart plate a parity generator and parity checker has been reported by Ghosh [27]. Dimitriadou et al. [28] have introduced a 4-bit parity generator and checker. They used a high-speed switch to design the parity generator. This high-speed switch is based on Quantum-Dot-SOA-based MZI and their design is verified through numerical simulation. This design is based on the modified trinary number system. A micro-ring-resonator (MRR)-based parity generator and checker have been reported by Rakshit et al. [29] and it also verified using numerical simulation. Mehra et al. [30] have introduced an SOA-MZI-based 7-bit parity generator and checker circuit. This design is simulated at high-speed 120 GHz. Bhattacharyya et al. [31] have reported a 4-bit parity generator using an SOA-assisted Sagnac switch and the design is verified through numerical simulation. Kumar et al. [32] have reported a parity checker using the electro-optic effect in MZI. Using the MATLAB software, results are obtained and

optiBPM software is used for verification of the implementation of this design. Wang et al. [33] have reported parity checker in the all-optical domain and the works implemented in the nanoscale-integrated chip. Plasmonic Metal-Insulator-Metal (MIM)-based parity generator has been reported by Singh et al. [34]. This design is simulated in MATLAB. Kaur et al. [35] have proposed an SOA-MZI-based 3-bit parity generator and checker and also transfer matrix method (TMM) based time-domain simulation is done for this design. Nair et al [36] have introduced an SOA-MZI-based 3-bit parity generator and checker in the all-optical domain. They used the tree architecture concept to design their work. Maji et al. [37] have proposed a design of a 4-bit parity generator and checker using a reflective semiconductor optical amplifier. They have introduced a single device in which even/odd parity generator units are designed but they have used an extra control terminal to switch between the even-odd parity units.

3. Working Principle of RSOA and ADM

As mentioned in the introduction, the basic key components of the proposed design are RSOA and ADM. Now, the working principle of these two is logically explained in this section. So, one pump signal (strong) and a probe signal (weak) are injected into the input signals of SOA but a high power probe beam is obtained at the output. This design is based on cross gain modulation (XGM) [1, 38]. Therefore, it is called RSOA. A high reflective (HR) and an anti-reflective (AR) coating are placed in the two facets of RSOA [1, 22, 25, 38-41]. It has a very versatile high gain medium so it has various important applications in passive optical networks (PON). Here, the frequency corresponding to the wavelengths of the probe signals is in the C-band (1535-1570 nm). The saturation power of RSOA may be used within 5-20 dBm [1, 9, 43].

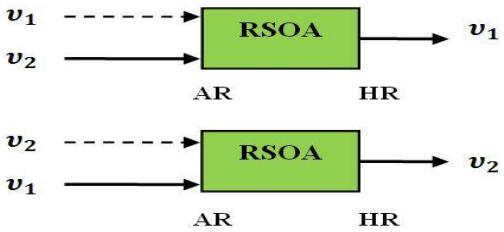

Fig. 1 Block diagram of RSOA

An add/drop multiplexer (ADM) [41-43] is very popular as a frequency selector. If we consider, the frequencies, υ_2 and υ_1 are injected into the bias and input port of ADM respectively, then at the output frequency, υ_1 is obtained whereas nothing at the drop port. If we consider the same frequency, υ_1 (or υ_2) into the input and bias port then ADM reflects the input signal, υ_1 (or υ_2) at the drop port by the circulator whereas nothing is obtained at the output. The schematic diagram of ADM is given in Fig. 2. RSOA and ADM are used to develop different devices such as multiplexer, adder, comparator, etc. [1, 9-10, 41].

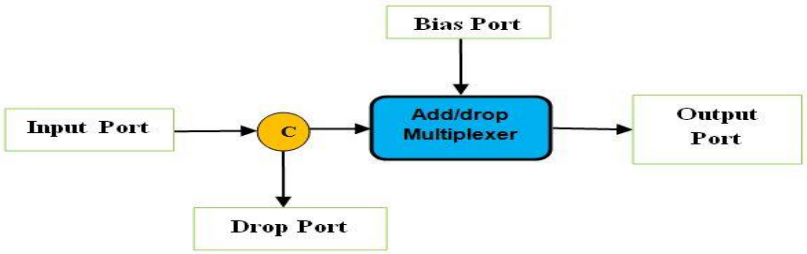

Fig. 2 Block diagram of ADM

4. PROPOSED SCHEME OF OPERATION OF THE THREE-BIT PARITY GENERATOR

In this section, the 3-bit parity generator and its operational scheme is proposed. Here, A, B, and C are the frequency encoded dibit-based inputs whose parity will be generated. The Boolean expression of even and odd parity generators are

$$Y_{even} = A \oplus B \oplus C \tag{1}$$

$$Y_{odd} = \overline{A \oplus B \oplus C} \tag{2}$$

The schematic diagram of this design is given in Fig. 3. In this proposed design, frequency encoding technique and dibit-based logic are opted. Mukhopadhyay [44] first reported the dibit-based representation technique. According to this representation technique [1, 9-10, 42-44], two consecutive bit positions are chosen to represent a digit. Here, digital logic states '0' and '1' are represented by the dibits '01' and '10' respectively. Since the proposed design is frequency encoding, so two different frequencies υ_1, and υ_2 when placed side by side as ''υ_2 υ_1'' indicates the logic state '1' and ''υ_1 υ_2'' indicates the digital logic state '0'. Here, we adopted the logic of SUM from the design of half adder [1] using RSOA and ADM. In half-adder design, two inputs dibit-based logic are used but in this proposed design, we have implemented three inputs dibit-based logic. So the operation of the three inputs dibit-based logic is much more complicated than the previous version [1]. The operation of the proposed designs is based on the Eqs. 1-2. Now, the operation scheme of the proposed frequency encoded dibit-based parity generator describe in the following cases.

4.1. Case-I (When all the inputs are the same)

In this case, $A^{/}=\upsilon_1$, $A^{//}=\upsilon_2$, $B^{/}=\upsilon_1$, $B^{//}=\upsilon_2$, $C^{/}=\upsilon_1$, $C^{//}=\upsilon_2$ frequencies are injected into the input terminals. Therefore, υ_1 frequencies are obtained from the RSOA-3, RSOA-2, and RSOA-1. The outputs of RSOA-2 and RSOA-1 are injected into A4 (ADM-4) as input and bias signals. Since both the frequency, of A4 is the same then frequency, υ_1 is obtained at the drop port through the circular. This frequency, υ_1 acts as a pump signal of RSOA-5 and probe signal frequency, υ_1 so the output of RSOA-5 is frequency, υ_1. This frequency, υ_1 acts as an input signal of A5 (ADM-5) and its biasing signal is υ_1 which is the output frequency of RSOA-3. Since both the frequencies of A5 (ADM-5) are the

same then A5 reflects the input signal, υ_1 at the drop port. This frequency, υ_1 works as a pump signal of RSOA-7. Therefore, the output of RSOA-7 is frequency, υ_1. One part of this frequency directly shows the dibit output $Y'_{\mathbf{even}}$ and another part acts as an input of A6 (ADM-6) which is biased by the signal of frequency, υ_2. Therefore, A6 selects the input signal of frequency, υ_1 to the output and this output frequency, υ_1 works as the pump signal of RSOA-8. This yields υ_2 at the dibit output terminal, $Y''_{\mathbf{even}}$. Finally, the dibit outputs υ_1 and υ_2 are obtained at the output terminals, $Y'_{\mathbf{even}}$ and $Y''_{\mathbf{even}}$ respectively, which indicates the digital logic state '0' and the dibit outputs υ_2, υ_1 are obtained at the dibit output terminals, $Y'_{\mathbf{odd}}$ and $Y''_{\mathbf{odd}}$ which altogether indicates the digital logic state '1'. Therefore, when inputs, A=0, B=0, and C=0 then the outputs show even parity, $Y_{\mathbf{even}}$=0 and odd parity, $Y_{\mathbf{odd}}$ =1.

Similarly, when $A'=\upsilon_2$, $A''=\upsilon_1$, $B'=\upsilon_2$, $B''=\upsilon_1$, $C'=\upsilon_2$, and $C''=\upsilon_1$ are taken as input signals to the device then the dibit outputs υ_1, υ_2 are obtained at the dibit output terminals, $Y'_{\mathbf{even}}$ and $Y''_{\mathbf{even}}$ respectively which altogether indicates the digital logic state '0' and the dibit outputs υ_2, υ_1 are obtained at the dibit output terminals, $Y'_{\mathbf{odd}}$ and $Y''_{\mathbf{odd}}$ which altogether indicates the digital logic state '1'. Therefore, when inputs, A=1, B=1, and C=1 then the outputs show even parity, $Y_{\mathbf{even}}$=0 and odd parity, $Y_{\mathbf{odd}}$ =1.

4.2. Case-I I (When one input is different)

Here, $A'=\upsilon_2$, $A''=\upsilon_1$, $B'=\upsilon_1$, $B''=\upsilon_2$, $C'=\upsilon_2$, and $C''=\upsilon_1$ are applied as the input signals of the device. Therefore, frequencies, υ_2, υ_1, and υ_2 are obtained at the outputs of RSOA-3, RSOA-2, and RSOA-1 respectively. The outputs from RSOA-2 and RSOA-1 are injected into the A4 (ADM-4) as input and biasing signals respectively. Since both the frequencies of A4 are not the same then the input signal is selected by the A4 at the output. This frequency, υ_1 acts as a pump signal of RSOA-4 and its probe signal is υ_2 so the output of RSOA-5 is υ_2. This frequency, υ_2 acts as an input frequency of A5 (ADM-5), and the output frequency, υ_2 of RSOA-3 works as biasing frequency. Since both the frequency of A5 (ADM-5) are the same then A5 reflects the input signal of frequency, υ_2 at the drop port. This frequency, υ_2 works as a pump signal of RSOA-7. Therefore, the output of RSOA-7 is frequency, υ_1, one part of this frequency directly shows the dibit output $Y'_{\mathbf{even}}$ and another part acts as an input of A6 (ADM-6) which is biased with the frequency, υ_2. Therefore, A6 selects the frequency, υ_1 at the output, and this output frequency, υ_1 acts as pump signal of RSOA-8 which gives υ_2 at the dibit output terminal, $Y''_{\mathbf{even}}$. Finally, the dibit output υ_1 and υ_2 are obtained at the output terminals, $Y'_{\mathbf{even}}$ and $Y''_{\mathbf{even}}$ respectively, which indicates the digital logic state '0' and the dibit outputs υ_2 and υ_1 are obtained at the dibit output terminals, $Y'_{\mathbf{odd}}$ and $Y''_{\mathbf{odd}}$ which altogether indicates the digital logic state '1'. Therefore, when inputs, A=1, B=0, and C=1 then the outputs show even parity, $Y_{\mathbf{even}}$=0 and odd parity, $Y_{\mathbf{odd}}$ =1.

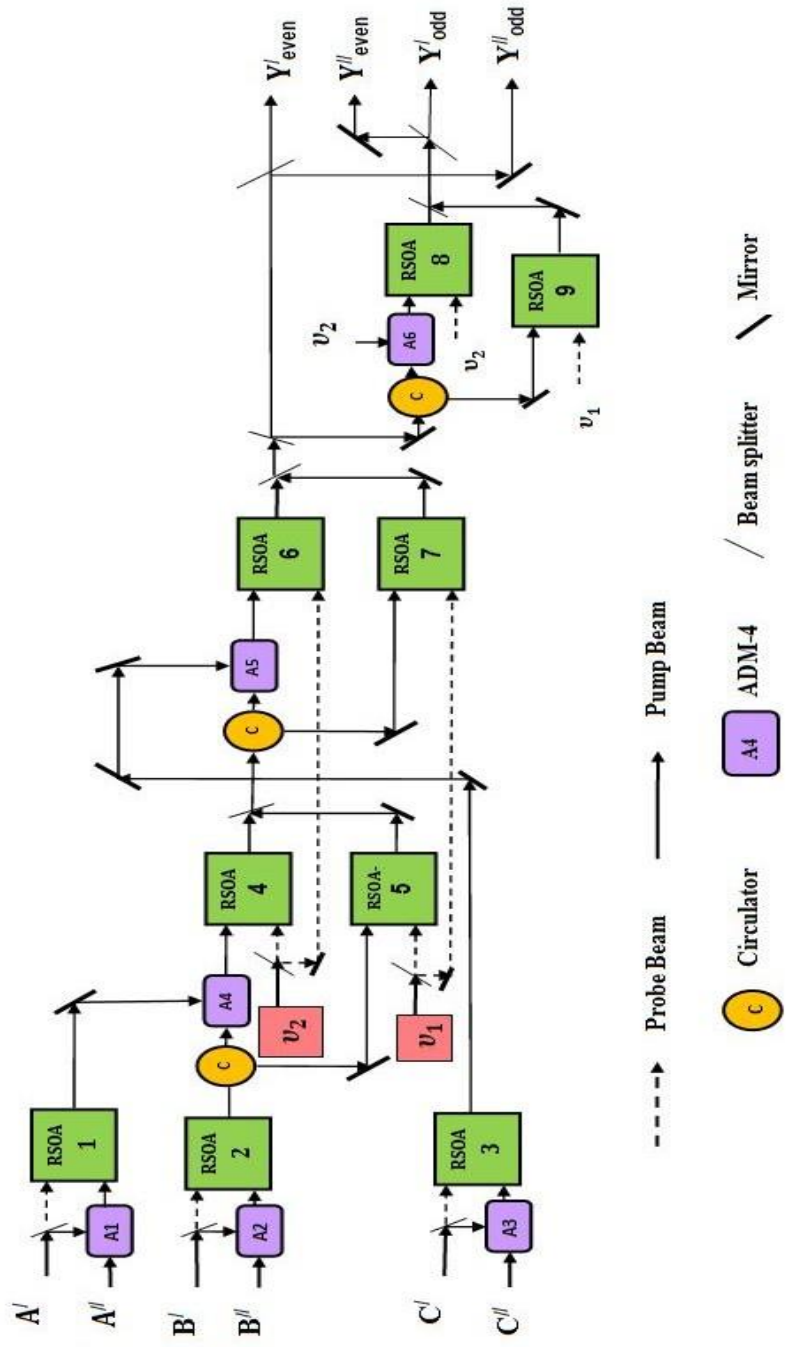

Fig. 3 Schematic diagram of proposed parity generator

Similarly, when $A^{/}=\upsilon_1$, $A^{//}=\upsilon_2$, $B^{/}=\upsilon_2$, $B^{//}=\upsilon_1$, $C^{/}=\upsilon_2$, and $C^{//}=\upsilon_1$ are taken as input signals to the device then the dibit outputs υ_1, υ_2 are obtained at the dibit output terminals, $Y^{/}_{\mathbf{even}}$ and $Y^{//}_{\mathbf{even}}$ respectively which altogether indicates the digital logic state '0' and the dibit outputs υ_2, υ_1 are obtained at the dibit output terminals, $Y^{/}_{\mathbf{odd}}$ and $Y^{//}_{\mathbf{odd}}$ which altogether indicates the digital logic state '1'. Therefore, when inputs, A=0, B=1, and C=1 then the outputs show even parity, $Y_{\mathbf{even}}$=0 and odd parity, $Y_{\mathbf{odd}}$ =1. In this way, other outputs can be obtained and these are given in Table 1.

Table 1 Frequency encoded truth table of proposed design

Dibit Input						Dibit Output			
Input (A)		Input (B)		Input (C)		Even parity (Y_{even})		Odd parity (Y_{odd})	
$A^{/}$	$A^{//}$	$B^{/}$	$B^{//}$	$C^{/}$	$C^{//}$	$Y^{/}_{even}$	$Y^{//}_{even}$	$Y^{/}_{odd}$	$Y^{//}_{odd}$
υ_1	υ_2	υ_1	υ_2	υ_1	υ_2	υ_1	υ_2	υ_2	υ_1
υ_1	υ_2	υ_1	υ_2	υ_2	υ_1	υ_2	υ_1	υ_1	υ_2
υ_1	υ_2	υ_2	υ_1	υ_1	υ_2	υ_2	υ_1	υ_1	υ_2
υ_1	υ_2	υ_2	υ_1	υ_2	υ_1	υ_1	υ_2	υ_2	υ_1
υ_2	υ_1	υ_1	υ_2	υ_1	υ_2	υ_2	υ_1	υ_1	υ_2
υ_2	υ_1	υ_1	υ_2	υ_2	υ_1	υ_1	υ_2	υ_2	υ_1
υ_2	υ_1	υ_2	υ_1	υ_1	υ_2	υ_1	υ_2	υ_2	υ_1
υ_2	υ_1	υ_2	υ_1	υ_2	υ_1	υ_2	υ_1	υ_1	υ_2

5. Simulation of The Proposed Parity Generator

In the previous section, the operational scheme of the proposed design is explained theoretically. Now, we discuss the simulation model of the proposed design. Using MATLAB (R2018a) software, the proposed design of the parity generator is verified. RSOAs and ADMs are programming on the basis of their characteristics using MATLAB language. If frequencies, υ_1=193.5 THz (wavelength=1550 nm) and υ_2=194.1 THz (wavelength=1545 nm) are considered as the probe signal and pump signal then, 193.5 THz is obtained at the output port whereas 194.1 THz is obtained at the output port when υ_1=193.5 THz (wavelength=1550 nm) and υ_2=194.1 THz (wavelength=1545 nm) are considered as the pump and probe signals. If frequencies, υ_1=193.5 THz and υ_2=194.1 THz are considered as the input and biasing signals then, ADM selects the input signal (193.5 THz) at the output whereas nothing is obtained at the drop port. If the same frequencies are injected at the biasing and input port then, ADM reflects the input signal at the drop port whereas output gives nothing. By the use of these considerations, this design is simulated.

In Figs. 4, and 5, dibits <193.5><194.1> and <194.1><193.5> indicate the digital logic states '0', and '1' respectively. From Fig. 4, the dibits <193.5><194.1>, <194.1><193.5> and <193.5><194.1> are injected into the dibit inputs 'A', 'B' and 'C' terminals of the device respectively. As a result, <194.1><193.5> and <193.5> <194.1> are obtained as dibit even parity, $Y_{\mathbf{even}}$ and dibit odd parity, $Y_{\mathbf{odd}}$ at the output terminals respectively. Dibits <194.1><193.5>, <194.1><193.5>, and <193.5><194.1> are injected into the dibit inputs 'A', 'B', and 'C' terminals respectively. As a result, <193.5><194.1> and <194.1><193.5> are obtained as dibit even parity, $Y_{\mathbf{even}}$ and dibit odd parity, $Y_{\mathbf{odd}}$ at the output terminals

respectively. <194.1><193.5>, <194.1><193.5>, and <194.1><193.5> are injected into the dibit inputs 'A', 'B' and 'C' terminals respectively. Therefore, <194.1><193.5>, and <193.5><194.1> are yielded as dibit even parity, Y_{even} and dibit odd parity, Y_{odd} at the output terminals respectively. Similar way, other outputs are obtained corresponding to the applied inputs. All the dibit output waveforms corresponding to the dibit input waveforms are given in Fig. 5. The results of the simulation are discussed in the next section.

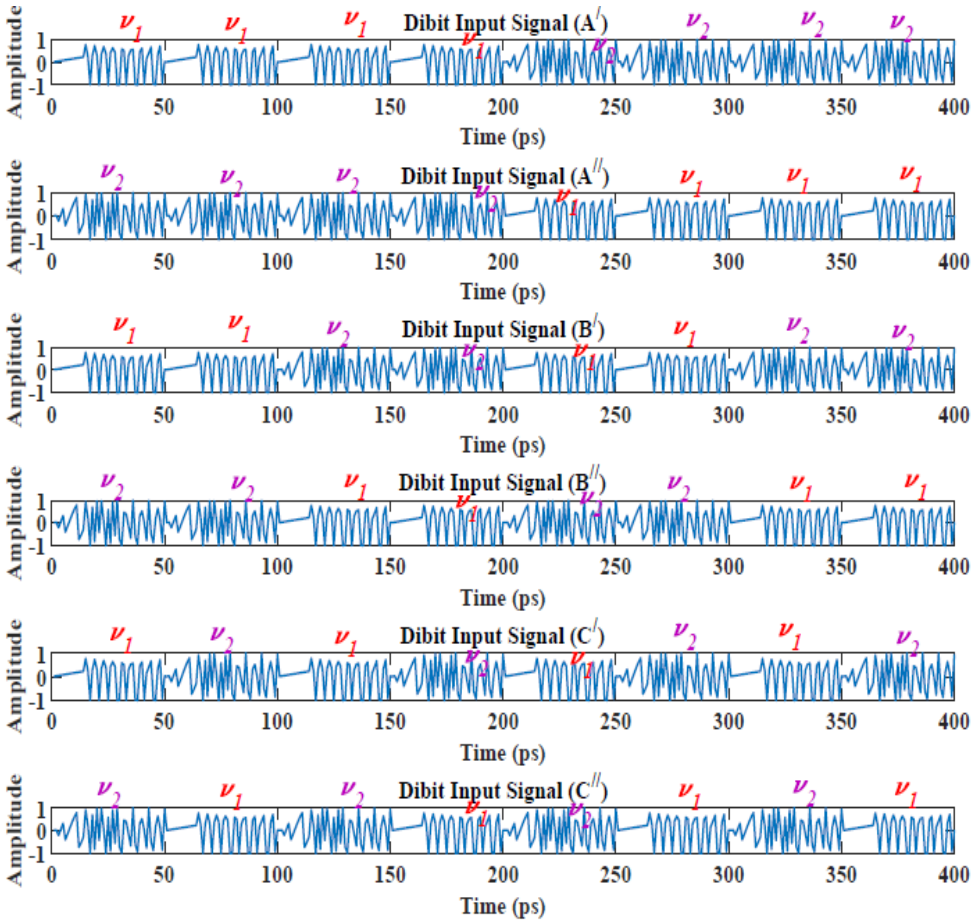

Fig. 4 Dibit input signal waveforms of parity generator

6. Results and Discussion

In this section, the theoretical interpretation and the simulation results are discussed. In this design, two signals with different frequencies, υ_1=193.5 THz and υ_2=194.1 THz are injected into the 50 ps time intervals to the input. The input and output signal waveforms are given in Figs. 4 and 5. The simulation (given in Table 2) verifies the parity generator results.

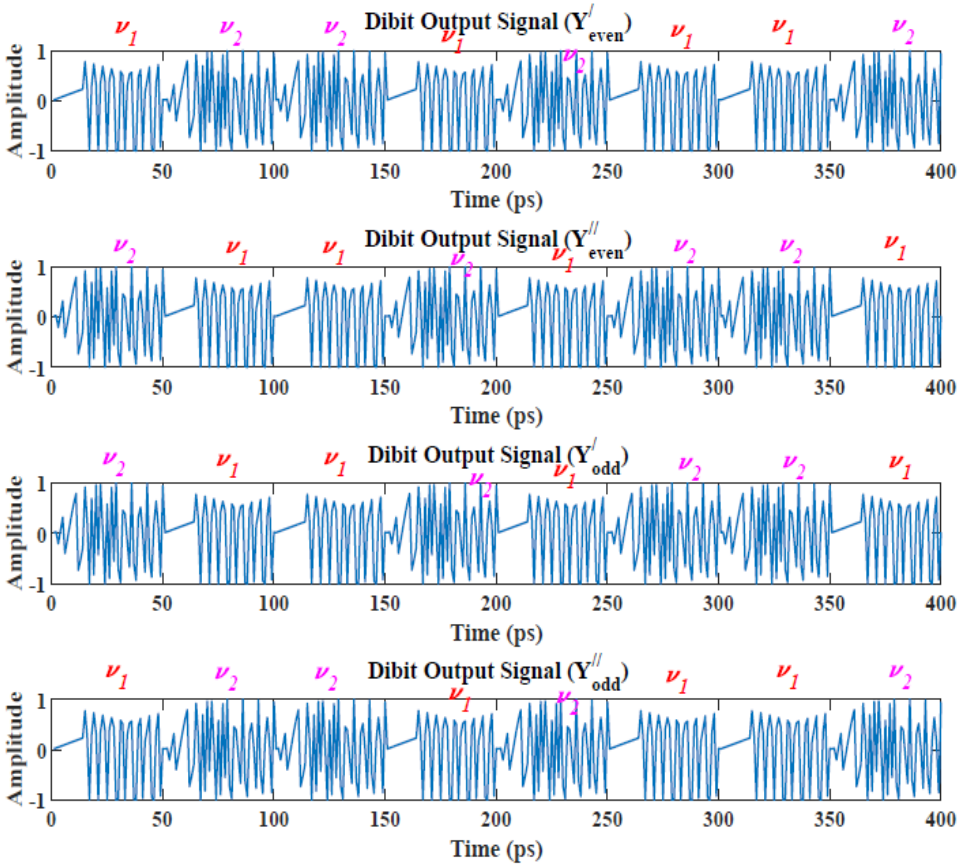

Fig. 5 Dibit output signal waveforms of parity generator

In the first 50 ps, we applied "υ_1 υ_2" in A, "υ_1 υ_2" in B, and "υ_1 υ_2" in C that indicates A=0, B=0, and C=0. After simulation with these data, we obtained $Y'_{even}=\upsilon_1$, $Y''_{even}=\upsilon_2$, and $Y'_{odd}=\upsilon_2$, $Y''_{odd}=\upsilon_1$ that indicates $Y_{even}=0$, and $Y_{odd}=1$. In 50-100 ps, we applied "υ_1 υ_2" in A, "υ_1 υ_2" in B, and "υ_2 υ_1" in C that indicates A=0, B=0, and C=1. After simulation with these data, we obtained $Y'_{even}=\upsilon_2$, $Y''_{even}=\upsilon_1$, and $Y'_{odd}=\upsilon_1$, $Y''_{odd}=\upsilon_2$ that indicates $Y_{even}=1$, and $Y_{odd}=0$. In 100-150 ps, we applied "υ_1 υ_2" in A, "υ_2 υ_1" in B, and "υ_1 υ_2" in C that indicates A=0, B=1, and C=0. After simulation with these data, we obtained $Y'_{even}=\upsilon_2$, $Y''_{even}=\upsilon_1$, and $Y'_{odd}=\upsilon_1$, $Y''_{odd}=\upsilon_2$ that indicate $Y_{even}=1$, and $Y_{odd}=0$. In 150-200 ps, we applied "υ_1 υ_2" in A, "υ_2 υ_1" in B, and "υ_2 υ_1" in C that indicates A=0, B=1, and C=1. After simulation with these data, we obtained $Y'_{even}=\upsilon_1$, $Y''_{even}=\upsilon_2$, and $Y'_{odd}=\upsilon_2$, $Y''_{odd}=\upsilon_1$ that indicate $Y_{even}=0$, and $Y_{odd}=1$. In 200-250 ps, we applied "υ_2 υ_1" in A, "υ_1 υ_2" in B, and "υ_1 υ_2" in C that indicates A=1, B=0, and C=0. After simulation with these data, we obtained $Y'_{even}=\upsilon_2$, $Y''_{even}=\upsilon_1$, and $Y'_{odd}=\upsilon_1$, $Y''_{odd}=\upsilon_2$ that indicate $Y_{even}=1$, and $Y_{odd}=0$. In 250-300 ps, we applied "υ_2 υ_1" in A, "υ_1 υ_2" in B, and "υ_2 υ_1" in C that indicates A=1, B=0, and C=1. After simulation with these data, we obtained $Y'_{even}=\upsilon_1$, $Y''_{even}=\upsilon_2$, and $Y'_{odd}=\upsilon_2$, $Y''_{odd}=\upsilon_1$ that indicates $Y_{even}=0$, and $Y_{odd}=1$. In 300-350 ps, we applied "υ_2 υ_1" in A, "υ_2 υ_1" in B, and "υ_1 υ_2" in C that indicates A=1, B=1, and C=0. After simulation with these data, we obtained $Y'_{even}=\upsilon_1$, $Y''_{even}=\upsilon_2$, and $Y'_{odd}=\upsilon_2$, $Y''_{odd}=\upsilon_1$ that indicates $Y_{even}=0$, and $Y_{odd}=1$. In 350-400 ps, we applied "υ_2 υ_1" in A, "υ_2 υ_1" in B, and "υ_2 υ_1" in C that indicates A=1, B=1, and C=1. After simulation with these data, we obtained $Y'_{even}=\upsilon_2$, $Y''_{even}=\upsilon_1$, and $Y'_{odd}=\upsilon_1$, $Y''_{odd}=\upsilon_2$ that indicate $Y_{even}=1$, and $Y_{odd}=0$. After the verification of the simulation results (given in Table 2), and the truth table (Table1), it is interpreted that the proposed design works accurately. A comparative study with previous work is given in Table 3.

Table 2 Simulation results of proposed parity generator (all the frequencies are in THz range)

Time (ps)	Dibit Input						Dibit Output			
	Input (A)		Input (B)		Input (C)		Even parity (Y_{even})		Odd parity (Y_{odd})	
	A'	A''	B'	B''	C'	C''	Y'_{even}	Y''_{even}	Y'_{odd}	Y''_{odd}
0-50	193.5	194.1	193.5	194.1	193.5	194.1	193.5	194.1	194.1	193.5
51-100	193.5	194.1	193.5	194.1	194.1	193.5	194.1	193.5	193.5	194.1
101-150	193.5	194.1	194.1	193.5	193.5	194.1	194.1	193.5	193.5	194.1
151-200	193.5	194.1	194.1	193.5	194.1	193.5	193.5	194.1	194.1	193.5
201-250	194.1	193.5	193.5	194.1	193.5	194.1	194.1	193.5	193.5	194.1
251-300	194.1	193.5	193.5	194.1	193.5	194.1	193.5	194.1	194.1	193.5
301-350	194.1	193.5	194.1	193.5	193.5	194.1	193.5	194.1	194.1	193.5
351-400	194.1	193.5	194.1	193.5	194.1	193.5	194.1	193.5	193.5	194.1

Table 3 Comparative Study with previous work

Work	Simulation of bit pattern given	RSOA used or not	Even and Odd parity generator in one device	Without Extra Control Signal	Dibit logic used or not
Ref. [26]	No	No	No	No	No
Ref. [28]	Yes	No	No	No	No
Ref. [33]	Yes	No	No	No	No
Ref. [37]	Yes	Yes	Yes	No	No
Proposed Work	Yes	Yes	Yes	Yes	Yes

7. CONCLUSIONS

In this communication, RSOA and ADM are utilized to design a frequency encoded dibit-based 3-bit parity generator. In this devised design, input dibit control units pass the error-free dibit logic that decreases the bit-error problems and enhances the operational speed. So, it promotes reliable and faithful operation. MATLAB software is used to simulate and verify the devised design. Furthermore, a comparative study with parity generators designed using different nonlinear materials has been conducted. This design is a single device for the even/odd parity generator units and it has no extra control terminal. As a result, the devised design reduces the space of the device as well as simultaneously generates even and odd parity. By introducing the dibit-based logic in this design, a high degree of parallelism can be expected. The frequency encoding and dibit-based systems also reduce the bit error problems and enhance the speed of operation in long-range transmission. In the future, we intend to develop a higher bit parity generator and checker. We also intend to use the proposed design in the full adder, cryptographic systems, and in the development of binary to gray code converter devices in the future.

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