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ORIGINAL ARTICLE

A Nine-Level Switched-Capacitor Step-Up Inverter with Low Voltage Stress

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Abstract
This paper proposes a nine-level switched-capacitor step-up inverter (9LSUI) which can achieve a quadruple voltage gain with single dc source. Differing from other switched-capacitor inverters, the voltage stress of switches is effectively reduced due to the elimination of H-bridge, and the peak inverse voltage of all switches is kept within $2V_{dc}$. In addition, the proposed inverter is able to integrate inductive load, and the capacitor voltage self-balancing can be achieved without any auxiliary circuits. Moreover, the topology structure can be flexibly extended to raise the output levels, and the peak inverse voltage of switches can remain constant with the increase of sub-modules in the extended structure. Comprehensive comparisons are performed to verify the outstanding advantages of the proposed inverter. Finally, the steady-state and dynamic performance of the proposed inverter is validated through an experimental prototype, and the experimental results are provided to prove the theoretical analysis.

Keywords Multilevel inverter · Switched-capacitor · Voltage gain · Low voltage stress · Self-balancing

1 Introduction

Nowadays, multilevel inverters (MLIs) have been widely applied in many areas, such as electric vehicles (EVs), flexible ac transmission systems and motor drives [1–3]. Comparing with the conventional two-level inverter, MLIs work better in: reducing the dv/dt on switches; improving output power quality; reducing electromagnetic interference; requiring smaller filters [4].

In general, traditional MLIs are classified into three categories: neutral-point-clamped (NPC) [5, 6]; flying capacitor (FC) [7, 8]; cascaded H-bridge (CHB) [9, 10]. NPC and FC inverters can obtain the desired output voltage by using clamping diodes and floating capacitors. However, the challenge of balancing the capacitor voltage complicates the control strategy along with the increase of the output levels. The CHB inverters consist of H-bridge units, which have the advantages of modular, scalable design and simple control. However, these topologies require multiple dc sources and have no voltage gain, which can limit the applications [11].

Furthermore, the dc sources such as photovoltaic panels, fuel cells and batteries of electric vehicles have low voltage [12], and conventional multilevel inverters suffer from the lack of voltage gain and the unbalance of capacitor voltage. In order to overcome these problems, a dc-dc boost converter is inserted into the front end of the inverter [13]. However, the cascade device will raise power losses and reduce the efficiency of the inverter [14]. To improve the boosting capability, the Z-source techniques have been used in MLIs. However, the extra inductors can increase the volume and cost of inverters. Moreover, the number of output levels has been limited [15–17].

Another solution is the switched-capacitor multilevel inverters (SCMLIs) which have no requirement for magnetic components such as inductors and transformers. SCMLIs are able to achieve multilevel output and boost

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voltage through a switched-capacitor circuit. In addition, the capacitor voltage can be self-balanced without any auxiliary circuits. The step-up switched-capacitor inverter proposed in [18] can output five-level voltage with single dc source. The other single input SC inverter proposed in [19] for high-frequency application employs two capacitors to generate nine-level output voltage. However, the maximum output voltage is only twice the input voltage. The nine-level SC inverter proposed in [20] also has a twice voltage gain.

In order to promote the voltage gain, a generalized inverter has been proposed in [21] to obtain a higher output voltage. Similarly, to increase the flexibility of SCMLIs regarding the output levels and voltage gain, two extendable SCMLIs have been proposed in [22] and [23]. The step-up inverter in [22] reduces the number of power switches, but the ability to integrate inductive loads is lost. For the SC inverter proposed in [23], the capacitors can be charged by a binary asymmetrical pattern, which can significantly raise the number of output levels. However, one of the common shortcomings of the above inverters is that the use of a back-end H-bridge increases the total voltage stress of devices.

The high peak inverse voltage (PIV) of switches can limit the applications of inverters. The accumulation of voltage stress can be avoided by cascading multiple SC inverters [24]. However, multiple isolated dc sources and numerous power components are needed. In addition, the SCMLIs proposed in [25] and [26] eliminate the back-end H-bridge to reduce the PIV. However, both inverters employ numerous switches, which is not conducive to simplify the control strategy, and will lead to an increase of power losses. In [27], a nine-level quadruple-boost inverter with an inherent ability to reverse the polarity of the output voltage has been presented. However, there are two switches that need to withstand the peak value of the output voltage. The step-up SC inverter proposed in [28] reduces the total standing voltage (TSV) of switches. However, numerous capacitors will lead to an increase of system volume and weight.

Considering the aforementioned challenges, this paper proposes a nine-level switched-capacitor inverter (9LSUI) with low voltage stress. The eminent characteristics of the proposed 9LSUI are as follows:

(1) Nine-level output voltage can be achieved with only two capacitors and single dc source.
(2) The proposed inverter has a quadruple voltage gain with low voltage stress.
(3) The PIV of each switch is kept within $2V_{dc}$, which can significantly reduce the TSV of inverter.
(4) An extendable structure in which the PIV of all switches can be kept within $3V_{dc}$.
(5) Capacitor voltage can be self-balanced without involving additional controls.

Next section introduces the circuit design and modulation strategy of the proposed inverter. Section 3 presents the comparison between the proposed topology and other inverters. Section 4 demonstrates the steady-state and dynamic experimental results, and conclusion is obtained in Sect. 5.

2 Proposed 9LSUI

2.1 Circuit Design

Figure 1 depicts the proposed 9LSUI, in which ten power switches $S_1 \sim S_{10}$ and two capacitors C_1 and C_2 constitute the SC unit to achieve a multilevel output and voltage boost. Additionally, the complementary switch pairs (S_L, $\overline{S}_L$) and (S_R, $\overline{S}_R$) constitute two half-bridges to reverse the polarity of the output voltage. The proposed inverter employs single dc source which is set as V_{dc}. All switches are equipped with an anti-parallel diode except for S_{10}. Capacitors C_1 and C_2 can be charged to V_{dc} and $2V_{dc}$, respectively. The inverter can output nine levels: $0, \pm V_{dc}, \pm 2V_{dc}, \pm 3V_{dc}, \pm 4V_{dc}$. Hence, the proposed topology achieves a quadruple voltage gain.

The proposed inverter has an excellent characteristic of low voltage stress. As shown in Fig. 1, X is the ratio of PIV to V_{dc}, which can visually indicate the maximum stress of each switch. It can be seen that the PIV of most switches is V_{dc}, only switches $S_8 \sim S_{10}$, S_R and $\overline{S}_R$ withstand the voltage $2V_{dc}$ which is half of the peak output voltage. Therefore, it is worth noting that the features of high boosting factor and low voltage stress make the topology fit for medium and high-power applications with low input voltage.

2.2 Operating Principle

The operating principle of switches and capacitors are shown in Table 1. Where "0" and "1" indicate the off and

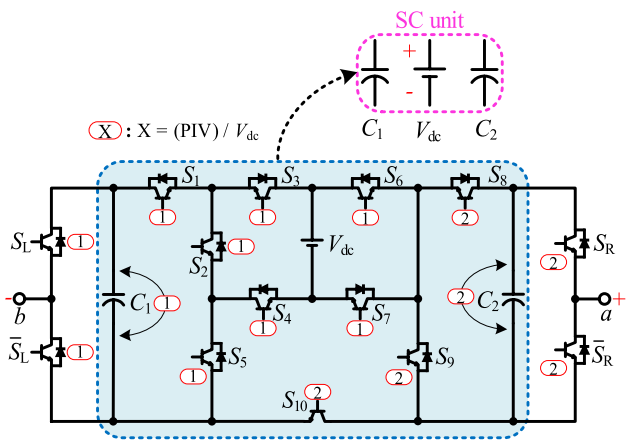

Fig. 1 Topology of proposed 9LSUI

Table 1 Switches and capacitors states

States	Levels	Switches	Capacitors
		$S_1S_2S_3S_4S_5S_6S_7S_8S_9S_{10}S_LS_R$	C_1, C_2
1	$4V_{dc}$	1 1 0 1 0 1 0 0 1 0 0 1	D, D
2	$3V_{dc}$	1 0 1 1 1 1 0 0 1 0 0 1	C, D
3	$2V_{dc}$	1 1 0 1 0 1 0 1 0 1 0 1	D, C
4	V_{dc}	1 0 1 1 1 1 0 1 0 0 0 1	C, –
5	0	1 0 1 1 1 1 0 1 0 0 1 1	C, –
6	$-V_{dc}$	1 1 0 1 0 1 0 1 0 1 1 0	D, C
7	$-2V_{dc}$	0 1 1 0 1 0 1 0 1 0 1 0	D, –
8	$-3V_{dc}$	1 0 1 1 1 0 1 1 0 0 1 0	C, D
9	$-4V_{dc}$	0 1 1 0 1 0 1 1 0 0 1 0	D, D

on states of switches, "C", "D" and "–" denote the charging, discharging and idle states of capacitors.

Detailed nine operating states and current paths of the proposed inverter are demonstrated in Fig. 2, where the blue highlight and purple highlight lines are the charging current paths of capacitors and the reverse current paths. It can be seen that capacitor C_1 can be charged to V_{dc} in parallel with dc source when the output voltages are 0, V_{dc} and $\pm 3V_{dc}$. Capacitor C_2 can be charged to $2V_{dc}$ in parallel with dc source and capacitor C_1 when the output voltages are $2V_{dc}$ and $-V_{dc}$. The connections of the dc source and capacitors can be changed through the ON/OFF states of switches, so as to achieve nine-level output voltage and quadruple voltage gain.

2.3 Modulation Strategy

Various modulation techniques have been applied to multilevel inverters. In this paper, the phase disposition pulse width modulation (PD-PWM) is selected for the proposed 9LSUI due to its simplicity and low total harmonic distortion (THD) [28].

As shown in Fig. 3, eight carrier signals $e_1 \sim e_8$ are compared with a sinusoidal reference signal e_s to generate eight pulse signals $u_1 \sim u_8$. The gate drive signals $v_{GS1} \sim v_{GSR}$ of the switches can be obtained through the logical combination of $u_1 \sim u_8$. The logical combination can be expressed as

$$v_{GS1} = v_{GS4} = u_6 + \overline{u}_7 \cdot u_8, \tag{1}$$

$$v_{GS2} = (u_1 + \overline{u}_2) \cdot u_3 + \overline{u}_5 \cdot (u_7 + \overline{u}_8), \tag{2}$$

$$v_{GS3} = v_{GS5} = (\overline{u}_1 \cdot u_2 + \overline{u}_3) \cdot (u_5 + \overline{u}_6), \tag{3}$$

$$v_{GS8} = \overline{v}_{GS9} = \overline{u}_2 \cdot (u_6 + \overline{u}_7), \tag{4}$$

$$v_{GS6} = \overline{v}_{GS7} = u_6, \tag{5}$$

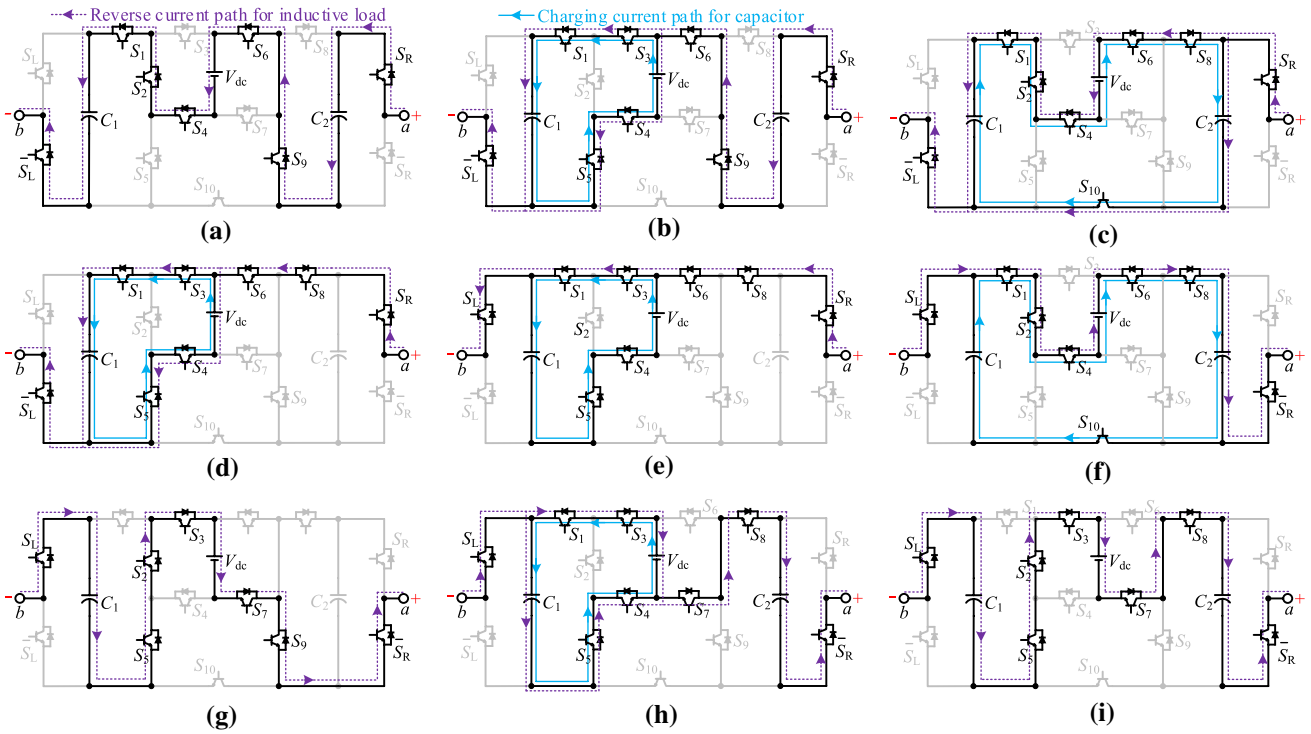

Fig. 2 Current paths for nine output levels. **a** $+4V_{dc}$; **b** $+3V_{dc}$; **c** $+2V_{dc}$; **d** $+V_{dc}$; **e** 0; **f** $-V_{dc}$; **g** $-2V_{dc}$; **h** $-3V_{dc}$; **i** $-4V_{dc}$

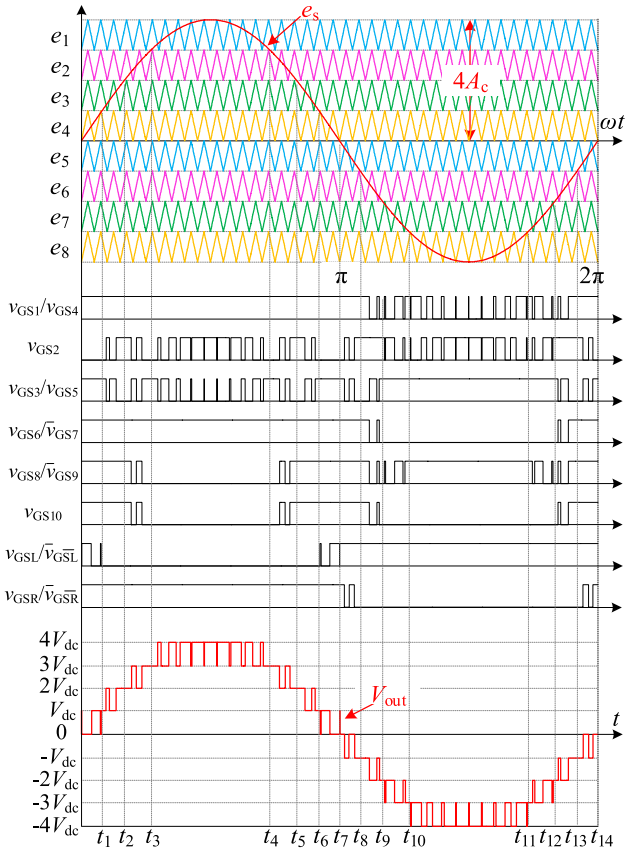

Fig. 3 PD-PWM method schematic

$$v_{GS10} = \overline{u}_2 \cdot u_6, \tag{6}$$

$$v_{GSL} = \overline{v}_{GS\overline{L}} = \overline{u}_4, \tag{7}$$

$$v_{GSR} = \overline{v}_{GS\overline{R}} = u_5, \tag{8}$$

The modulation index M for the 9LSUI is defined as

$$M = \frac{A_s}{4A_c}, \tag{9}$$

where A_s and A_c are the amplitudes of the reference signal and carrier signals. The range of M is $0 < M \leq 1$. The inverter can output different levels with the change of M between 0 and 1.

3 Capacitance and Power Losses

3.1 Design of Capacitor

The voltage fluctuation range of capacitors should be maintained within an acceptable range to improve voltage quality. The capacitor voltage ripple is related to the maximum continuous discharge of the capacitor. Therefore, the effect of the capacitor voltage ripple on the output voltage can be reduced effectively when the proper value of the capacitance is selected.

It can be seen from Fig. 2 and Table 1, C_1 will be in discharging state when output voltages are $-V_{dc}$ and $-2V_{dc}$ in the negative half cycle, and C_2 will be in discharging state when the proposed 9LSUI outputs $-3V_{dc}$ and $-4V_{dc}$. As shown in Fig. 3, the maximum continuous discharging intervals of C_1 and C_2 are $[t_7, t_{10}]$ and $[t_9, t_{12}]$. In fact, C_1 and C_2 are in alternate charging and discharging for part of the time in these two intervals, such as C_1 in the interval $[t_7, t_8]$. The most extreme case that ignores the charging time of capacitors is considered in the following analysis. The time t_7, t_9, t_{10} and t_{12} in Fig. 3 are calculated as follows

$$t_7 = \frac{1}{2f_s}, \tag{10}$$

$$t_9 = \frac{\pi + \arcsin\left(\frac{1}{2M}\right)}{2\pi f_s}, \tag{11}$$

$$t_{10} = \frac{\pi + \arcsin\left(\frac{3}{4M}\right)}{2\pi f_s}, \tag{12}$$

$$t_{12} = \frac{2\pi - \arcsin\left(\frac{1}{2M}\right)}{2\pi f_s}, \tag{13}$$

where f_s is the frequency of the sinusoidal reference wave. Assuming the load is pure resistive. Therefore, the maximum continuous discharging amount ΔQ_{C1} of C_1 within $[t_7, t_{10}]$ can be calculated as

$$\Delta Q_{C1} = \int_{t_7}^{t_{10}} I_{load} \sin(2\pi f_s t) dt. \tag{14}$$

The maximum continuous discharging amount ΔQ_{C2} of C_2 within $[t_9, t_{12}]$ is calculated as

$$\Delta Q_{C2} = \int_{t_9}^{t_{12}} I_{load} \sin(2\pi f_s t) dt, \tag{15}$$

where I_{load} is the amplitude of the load current. Assuming $k\%$ is the constant describes the maximum acceptable voltage ripple, the capacitances of C_1 and C_2 can be determined as

$$C_1 \geq \frac{\Delta Q_{C1}}{k\% \cdot V_{dc}}, \tag{16}$$

$$C_2 \geq \frac{\Delta Q_{C2}}{k\% \cdot 2V_{\mathrm{dc}}}. \tag{17}$$

3.2 Calculation of Losses

3.2.1 Switching Losses

The switching losses of MLIs occur during the turn-on and turn-off period of power switches due to the inherent switching delay [23]. It is known that the voltage and current of switches exhibit a linear approximation during the switching period. Therefore, the turn-on losses ($P_{\mathrm{sw,on},i}$) and the turn-off losses ($P_{\mathrm{sw,off},i}$) of the i-th involved power switch can be calculated by

$$\begin{aligned} P_{\mathrm{sw,on},i} &= f_{\mathrm{sw}} \int_0^{t_{\mathrm{on}}} v_{\mathrm{s}}(t) i_{\mathrm{s}}(t) dt \\ &= f_{\mathrm{sw}} \int_0^{t_{\mathrm{on}}} \left(\frac{V_{on,i}}{t_{\mathrm{on}}} t \right) \left(-\frac{I_{\mathrm{on},i}}{t_{\mathrm{on}}} (t - t_{\mathrm{on}}) \right) dt, \\ &= \frac{1}{6} f_{\mathrm{sw}} V_{on,i} I_{\mathrm{on},i} t_{\mathrm{on}} \end{aligned} \tag{18}$$

$$\begin{aligned} P_{\mathrm{sw,off},i} &= f_{\mathrm{sw}} \int_0^{t_{\mathrm{off}}} v_{\mathrm{s}}(t) i_{\mathrm{s}}(t) dt \\ &= f_{\mathrm{sw}} \int_0^{t_{\mathrm{off}}} \left(\frac{V_{off,i}}{t_{\mathrm{off}}} t \right) \left(-\frac{I_{off,i}}{t_{\mathrm{off}}} (t - t_{\mathrm{off}}) \right) dt, \\ &= \frac{1}{6} f_{\mathrm{sw}} V_{off,i} I_{off,i} t_{\mathrm{off}} \end{aligned} \tag{19}$$

where f_{sw} is the switching frequency, v_{s} and i_{s} present the voltage and current of switch when the switching state changes, $V_{\mathrm{on},i}$ and $V_{\mathrm{off},i}$ are the on-state and off-state voltage of the i-th switch, $I_{\mathrm{on},i}$ and $I_{\mathrm{off},i}$ are the on-state and off-state current that across the i-th switch, t_{on} and t_{off} are the time of turn-on and turn-off. Therefore, the total switching losses P_{sw} of the proposed inverter can be obtained as

$$P_{\mathrm{sw}} = \sum_{i=1}^{14} \left(P_{\mathrm{sw,on},i} + P_{\mathrm{sw,off},i} \right). \tag{20}$$

3.2.2 Conduction Losses

The conduction losses are related to the parasitic resistance of power devices in current paths, including the conduction resistance R_{on} of switches, the internal resistance R_{D} of anti-parallel diodes and the equivalent series resistance R_{ESR} of the capacitors.

The equivalent resistance for each level is listed in Table 2. According to Fig. 3 and Table 2, in the interval [0, t_1], the load current flows through three switches and three diodes (four switches and two diodes) when the output voltage is 0 (V_{dc}). Therefore, the energy loss E_{loss1} during the interval [0, t_1] can be calculated as

Table 2 Equivalent resistance for each level

Output level	Equivalent parasitic resistance
0	$3R_{\mathrm{on}} + 3R_{\mathrm{D}}$
$+V_{\mathrm{dc}}$	$4R_{\mathrm{on}} + 2R_{\mathrm{D}}$
$-V_{\mathrm{dc}}$	$3R_{\mathrm{on}} + 4R_{\mathrm{D}}$
$\pm 2V_{\mathrm{dc}}$	$6R_{\mathrm{on}} + R_{\mathrm{D}} + R_{\mathrm{ESR}}$
$\pm 3V_{\mathrm{dc}}$	$5R_{\mathrm{on}} + R_{\mathrm{D}} + R_{\mathrm{ESR}}$
$\pm 4V_{\mathrm{dc}}$	$7R_{\mathrm{on}} + 2R_{\mathrm{ESR}}$

$$\begin{aligned} E_{\mathrm{loss1}} = \int_0^{t_1} i_{\mathrm{load}}^2 \Bigg[(3R_{\mathrm{on}} + 3R_{\mathrm{D}}) \frac{A_{\mathrm{s}} \sin(2\pi f_s t)}{A_{\mathrm{c}}} + \\ (4R_{\mathrm{on}} + 2R_{\mathrm{D}}) \left(1 - \frac{A_{\mathrm{ref}} \sin(2\pi f_{ref} t)}{A_{\mathrm{c}}} \right) \Bigg] dt, \end{aligned} \tag{21}$$

where i_{load} is the load current, R_{on} is the conduction resistance of switches and R_{D} is the internal resistance of anti-parallel diodes.

Similarly, the conduction losses in other inverters ([t_1, t_2]-[t_{13}, t_{14}]) are also can be calculated according to Eq. (21). The total conduction losses P_{cond} as the proposed 9LSUI can be calculated as

$$P_{\mathrm{cond}} = \sum_{i=1}^{14} E_{\mathrm{loss}i} \times f_s, \tag{22}$$

where f_{s} is the frequency of the sinusoidal reference wave.

3.2.3 Capacitor Ripple Losses

The ripple loss P_{rip} is caused by the voltage fluctuation of capacitor. The voltage ripple $\Delta V_{\mathrm{rip},Ci}$ of the capacitor C_i is obtained by

$$\Delta V_{\mathrm{rip},C_i} = \frac{1}{C_i} \int_{t-}^{t+} i_{C_i}(t) dt, \tag{23}$$

where $i_{Ci}(t)$ is the current across capacitor, the interval [t-, t+] is the discharging period of C_i. For the proposed 9LSUI, [t_8, t_9] and [t_9, t_{12}] are the maximum discharging intervals of C_1 and C_2. The ripple losses P_{rip} can be calculated as

$$P_{\mathrm{rip}} = \frac{f_{\mathrm{s}}}{2} \sum_{i=1}^{2} C_i \Delta V_{\mathrm{rip},Ci}^2. \tag{24}$$

Therefore, the total losses P_{loss} of the proposed 9LSUI can be calculated as

$$P_{\text{rip}} = \frac{f_s}{2} \sum_{i=1}^{2} C_i \Delta V_{\text{rip},Ci}^2. \tag{25}$$

Finally, the efficiency of the nine-level inverter can be expressed as

$$\eta = \frac{P_{\text{o}}}{P_{\text{o}} + P_{\text{loss}}} = \frac{P_{\text{o}}}{P_{\text{o}} + P_{\text{sw}} + P_{\text{cond}} + P_{\text{rip}}}, \tag{26}$$

where η and P_{o} are the efficiency and output power of the proposed inverter.

4 Topology Extension and Comparisons

The proposed 9LSUI can be extended with multiple SC units, which can generate more output levels and achieve higher voltage gain. In order to further evaluate the superiority of the proposed topology, a comprehensive analysis and comparison with other recently SCMLIs have been implemented.

4.1 Extended Structure

The extended structure of the proposed 9LSUI is shown in Fig. 4. It can be seen that each two SC units are in a back-to-back connection through a power switch pairs P_{i1} and P_{i2} ($i = 1, 2, \ldots, n\text{-}1$). Notice that these switch pairs have a complementary operation with each other to avoid the short-circuit problem. In the extended topology, n dc sources are used and the voltage is V_{dc}. Therefore, the number of capacitors (N_{Cap}) and switches (N_{SW}) can be expressed as

$$N_{\text{Cap}} = 2n, \tag{27}$$

$$N_{\text{SW}} = 12n + 2. \tag{28}$$

In this configuration, the voltage of the capacitor C_{i1} remains as V_{dc} and the capacitor C_{i2} is charged to $2V_{\text{dc}}$. The PIV of P_{i1} and P_{i2} is kept within $3V_{\text{dc}}$ in the extended structure. Therefore, the number of output levels (N_{L}), the peak value of the output voltage ($V_{\text{o, max}}$) and the TSV for the switches can be obtained as:

$$N_{\text{L}} = 8n + 1, \tag{29}$$

$$V_{\text{o,max}} = 4n \cdot V_{\text{dc}}, \tag{30}$$

$$\text{TSV} = (19n - 2) \cdot V_{\text{dc}}. \tag{31}$$

4.2 Comparison of Nine-level Inverters

In this section, to evaluate the performance of the proposed 9LSUI, a comprehensive comparison with other topologies is made in Table 3. The comparison focuses on the numbers of dc sources (N_{Source}), capacitors ($N_{\text{Capacitor}}$), switches (N_{Switches}) and diodes (N_{Diodes}). Furthermore, the PIV of semiconductors (switches and diodes), the TSV_{pu} of semiconductors, the voltage gain and the use of H-bridge are also considered. The terms related to TSV_{pu} and voltage gain are defined as

$$\text{TSV}_{\text{pu}} = \frac{\text{TSV}}{V_{o\_\text{max}}}, \tag{32}$$

$$\text{Voltage Gain} = \frac{V_{o\_\text{max}}}{V_{\text{dc}}}. \tag{33}$$

where V_{o_max} and V_{dc} are the maximum output peak voltage and the dc input voltage.

According to Table 3, the proposed inverter requires minimum capacitors, which helps to reduce the volume and weight of the inverter. Moreover, compared with other inverters, the proposed topology employs single dc source and two capacitors to achieve quadruple voltage gain,

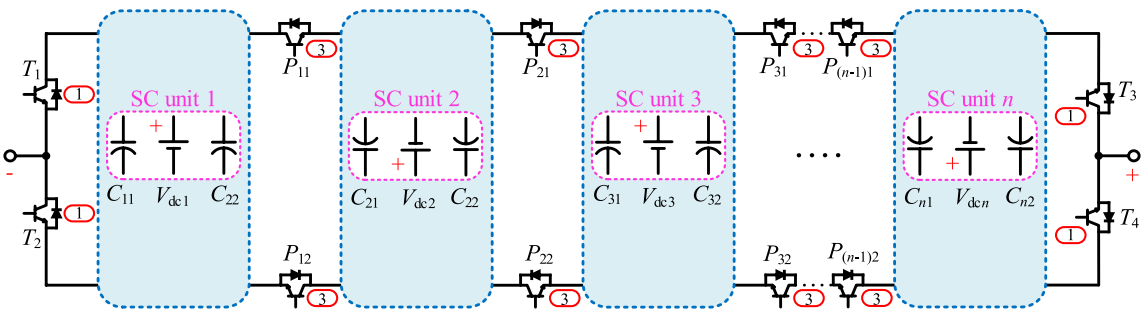

Fig. 4 Extended structure of the proposed 9LSUI

while the boosting factor in [19] and [20] is 2. Although the inverters in [22] and [23] use fewer switches, they all require H-bridge to shift output voltage polarity. Moreover, the large number of diodes used in [22] may limit its capacity of integrating inductive loads.

The PIV of the switches is important role to evaluate the performance of MLIs. The comparison shows that the PIV of the switches is only $2V_{dc}$. Although the inverter in [25] has lower PIV, the use of numerous switches will lead to a high cost. A significant feature of the proposed inverter is low TSV_{pu}, which also credits to the low PIV of switches. The inverter in [28] has the lowest TSV, but the use of four capacitors increases the volume and cost.

The comparison between the suggested extended structure and other inverters is performed at the output levels of $(2\ m+1)$ or m. Table 4 and Fig. 5. show the comparison results, the proposed extended structure employs less components (capacitors, switches and diodes). Moreover, the proposed structure does not need extra diodes and has the minimum TSV_{pu}. In a word, the proposed topology has obvious advantages in promoting voltage gain, reducing the number of components and voltage stress of the switches.

5 Simulation and Experiment Analysis

5.1 Simulation Results

In order to examine the performance of the proposed inverter, a simulation model of nine-level switched-capacitor inverter is established in MATLAB/Simulink. The simulation parameters are shown in Table 5.

The simulation results are shown in Fig. 6. It can be seen that the proposed inverter can output nine-level voltage and

Table 3 Comparison of single-phase nine-level inverters

Items	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[28]	Proposed
N_{Source}	1	1	1	1	1	2	1	1	1
$N_{Capacipor}$	2	2	3	3	2	2	3	4	2
N_{Switch}	9	10	13	8	9	12	19	8	14
N_{Diode}	2	1	0	6	1	2	0	4	0
PIV($\times V_{dc}$)	2	2	4	4	4	2	1	2	2
TSV_{pu}	5.75	7	6.25	8	6.25	5.5	4.75	4	4.75
Voltage Gain	2	2	4	4	4	2	4	4	4
H-Bridge	YES	YES	YES	YES	YES	YES	NO	NO	NO

Table 4 Comparison of the proposed extended topologies with other inverters when output (2 m + 1) levels

Parameters	[18]	[20]	[21]	[24]	[25]	[29]	[30]	[31]	Proposed
N_{Source}	$m/2$	$m/4$	1	$m/2$	1	2	$m/3$	$m/3$	$m/3$
$N_{Capacipor}$	m	$m/2$	m-1	$m/2$	m-1	m-2	2 $m/3$	m	$m/2$
N_{Switch}	3 m	2 m+2	3 m+1	3 m	5 m-1	2 m+2	8 $m/3$	10 $m/3$	3 m+2
N_{Diode}	m	$m/4$	0	$m/2$	0	m-2	2 $m/3$	0	0
PIV($\times V_{dc}$)	2	2	m	2	m	m	3	1	3
TSV_{pu}	5	(7 m-8)/m	(7 m-3)/m	5.5	(5 m-1)/m	(7 m-6)/m	5.33	5.33	(4.75 m-2)/m

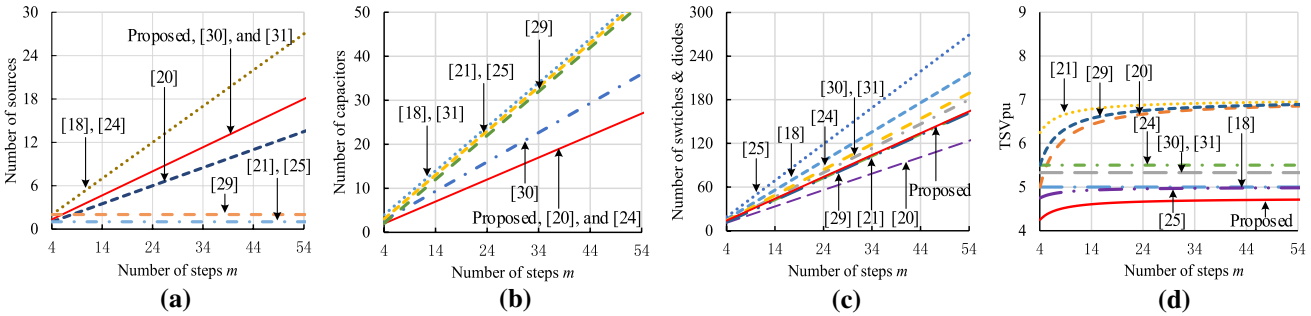

Fig. 5 Comparison of different SCMLIs. **a** number of sources; **b** number of capacitors; **c** number of switches and diodes; **d** TSV_{pu}

Table 5 Simulation Parameters

Items	Values
Input voltage (V_{dc})	30 V
Capacitors (C_1, C_2)	2200 μF
Triangle carrier frequency	2 kHz
Reference wave frequency	50 Hz
Modulation index(M)	0.9
Resistive-inductive load	25 Ω & 15 mH

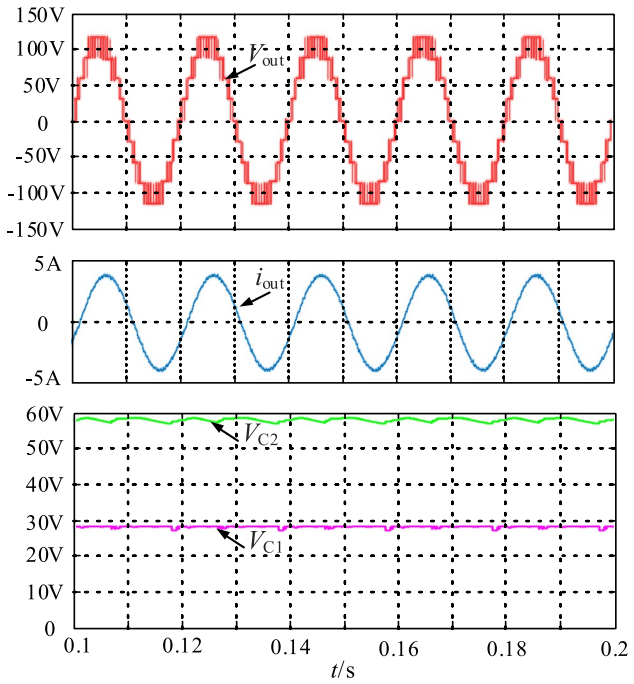

Fig. 6 Simulation results of output voltage, load current, and capacitor voltage

achieve a quadruple voltage gain. The capacitor voltages are self-balanced with low voltage ripple.

When the modulation index is 0.9, the Fast Fourier Transform (FFT) of the output voltage is shown in Fig. 7. It can be seen that the THD is 15.18%, and the 40th harmonic component is larger than the others because the carrier frequency is 2 kHz. The low THD can also simplify the design of the filter.

5.2 Experimental Results

To verify the practicability and effectiveness of the proposed 9LSUI, an experimental prototype has been built as shown in Fig. 8. The components and parameters of the model are shown in Table 6. The experiments examine the steady-state

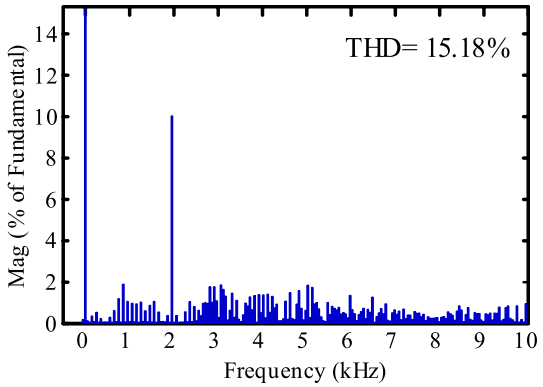

Fig. 7 THD of the output voltage

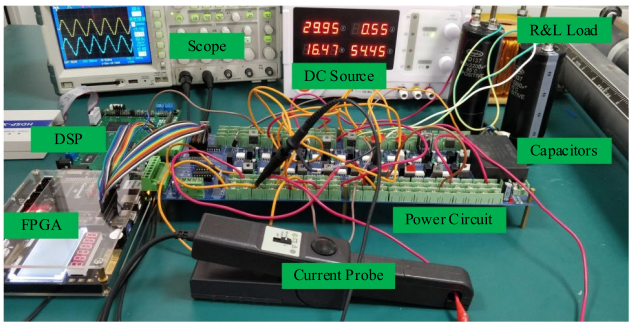

Fig. 8 Picture of the experimental prototype

Table 6 Experimental parameters

Items	Values
Driver	UCC27516
Current probe	Tektronix A622
Input voltage (V_{dc})	30 V
Capacitors (C_1, C_2)	2200 μF
Output frequency (f_o)	50 Hz
Resistive load (R)	50 Ω
Resistive-inductive load (R & L)	25 Ω & 15 mH

performance and dynamic responses of the proposed topology under several different conditions.

Figure 9 shows the steady-state experiment results and efficiency curve. The output voltage and load current are shown in Fig. 9a. It can be seen that the amplitude of output voltage is 120 V, which verifies that the proposed inverter can achieve a voltage gain of 4. Figure 9b presents the output voltage and load current when the inductive load is integrated. The load current appears as a sinusoidal waveform due to low THD. The voltages of

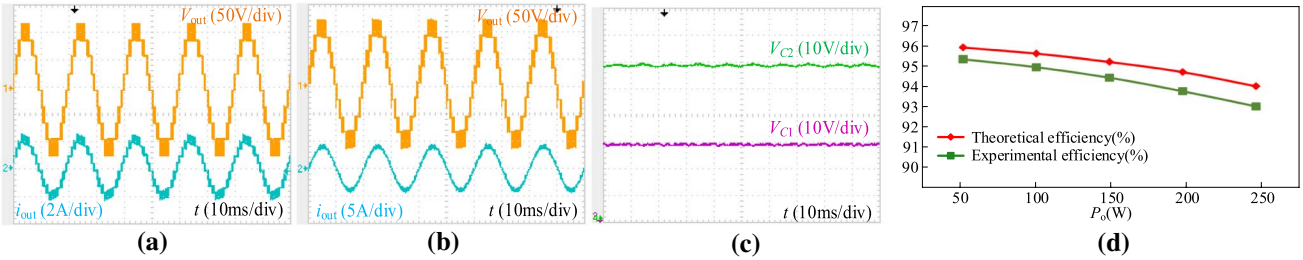

Fig. 9 Steady-state experimental results and efficiency curve. **a** output voltage and current with a pure resistive load; **b** output voltage and current with a resistive-inductive load; **c** capacitor voltages; **d** efficiency curve of the proposed topology

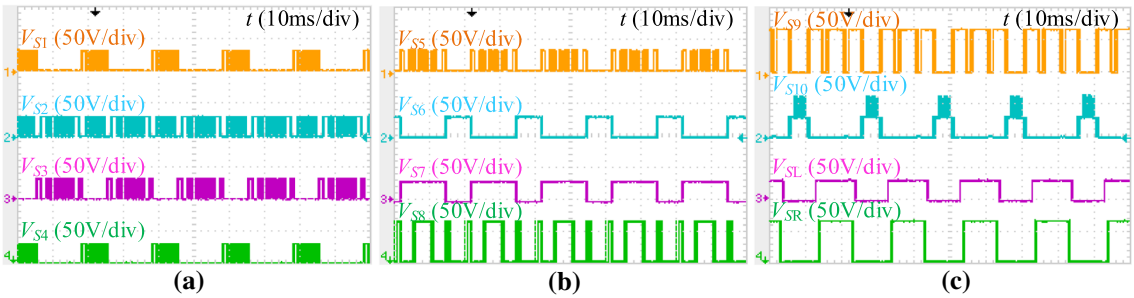

Fig. 10 Experimental results of stress voltages. **a** switches S_1-S_4; **b** switches S_5-S_8; **c** switches S_9-S_R

Table 7 Steady-state experimental results

Items	Values
Input voltage (V_{dc})	30 V
Voltage of capacitor C_1	28.66 V
Voltage of capacitor C_2	57.65 V
Output frequency (f_o)	50 Hz
Number of output levels	9
Voltage gain	4(V_{dc})
PIV of $S_1 \sim S_7$, S_L and $\overline{S}_L$	30 V
PIV of $S_8 \sim S_{10}$, S_R and $\overline{S}_R$	60 V

C_1 and C_2 under the R & L load are shown in Fig. 9c. It can be observed that C_1 and C_2 are charged to 28.66 V and 57.65 V. Moreover, the capacitor voltage fluctuates periodically within 5 V, which verifies the self-balancing ability of the proposed inverter. Figure 9d shows the theoretical efficiency and experimental efficiency of the proposed inverter under different output power. It can be seen that the 9LSUI has a great performance.

Figure 10 shows the voltage stress of different switches. The peak inverse voltages of the switches $S_1 \sim S_7$, S_L, and $\overline{S}_L$ are V_{dc}, and the peak inverse voltages of the switches $S_8 \sim S_{10}$, S_R, and $\overline{S}_R$ are $2V_{dc}$. Table 7 presents the steady-state experimental results. The experimental results are in good agreement with the previous theoretical analysis, which proves that the proposed inverter has the characteristics of low voltage stress across switches.

Figure 11 and Table 8 present the dynamic experimental results with the change of M. Figure 11a–c show the dynamic responses when the modulation ratio M varies from 0.9 to 0.7, 0.7 to 0.4 and then 0.4 to 0.2. It can be seen that the number of output levels will reduce with the decrease of M. Meanwhile, the amplitude of the load current also decreases accordingly. The waveforms quickly reach new steady-states after these changes, which is in good agreement with the theoretical analysis and design requirements.

Figures 12a, b are the dynamic responses when the dc source varies from 10 to 30 V and from 30 to 10 V. In Fig. 12, the amplitude of the output voltage gradually rises from 40 to 120 V when the input voltage increases. Meanwhile, the

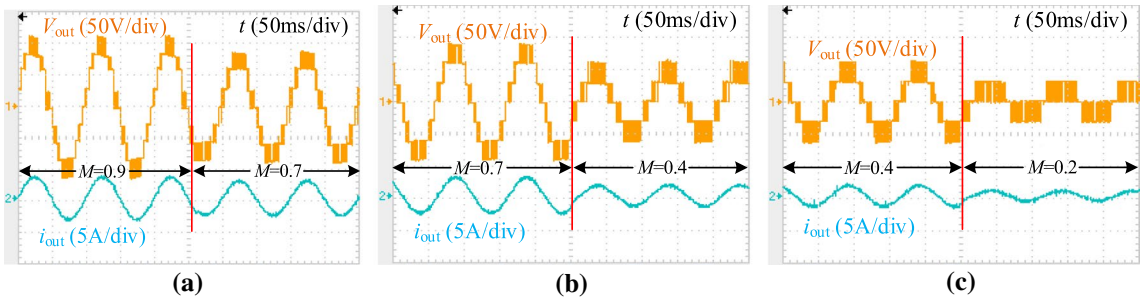

Fig. 11 Dynamic experimental results with change of **a** M from 0.9 to 0.7, **b** M from 0.7 to 0.4 and **c** M from 0.4 to 0.2

Table 8 Dynamic experimental results with change of M

M	Number of levels	Output voltage levels
0.2	3	±30 V, 0
0.4	5	±60 V, ±30 V, 0
0.7	7	±90 V, ±60 V, ±30 V, 0
0.9	9	±120 V, ±90 V, ±60 V, ±30 V, 0

voltage of C_1 rises from 10 to 30 V, and the voltage of C_2 rises from 20 to 60 V. It can be seen from Fig. 12b that the variations of load current and voltage are opposite to the ones in Fig. 12a when the input voltage decreases. Figures 12c, d are the dynamic responses when the load varies from no-load to resistive load (50 Ω), and then to resistive-inductive load (50 Ω-15 mH). The output voltage remains constant, and the load current varies instantaneously with the change of load, and then reaches a new steady-state.

In summary, the experimental results of the proposed 9LSUI validate the previous theoretical analysis. The capacitor voltage self-balancing can be achieved under steady-state and dynamic conditions, which verifies the practicability and effectiveness of proposed inverter.

6 Conclusion

The paper presents a switched-capacitor step-up inverter, which can generate nine output levels and achieve quadruple voltage gain without H-bridge. In addition, the proposed 9LSUI has voltage-self-balance ability without any auxiliary circuits, and the peak inverse voltage of all switches is kept within $2V_{dc}$. Moreover, the extended structure of the proposed inverter can generate more output levels, while the PIV of all switches is kept within $3V_{dc}$. The comparison results with other inverters show that the proposed inverter has the advantages of reducing the components, raise the voltage gain, and lowering the TSV of devices. An experimental prototype is implemented to verify the effectiveness and feasibility of proposed 9LSUI.

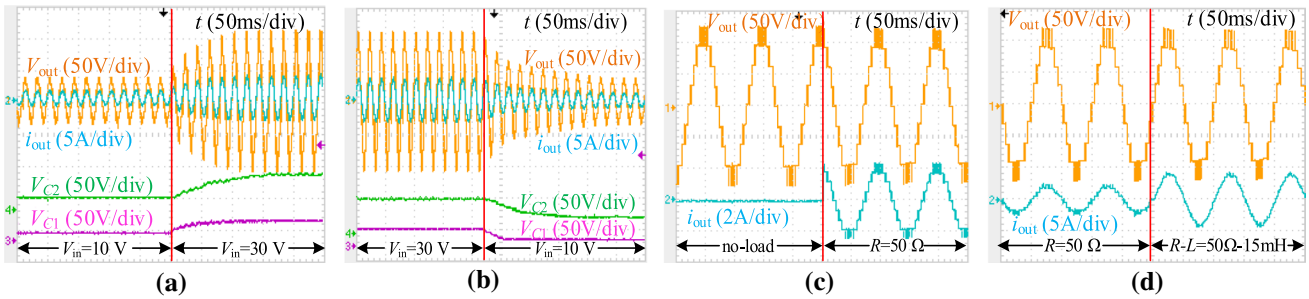

Fig. 12 Dynamic experimental results. **a** dc input voltage V_{dc} changes from $V_{in}=10$ V to $V_{in}=30$ V. **b** dc input voltage V_{dc} changes from $V_{in}=30$ V to $V_{in}=10$ V. **c** the load changes from no-load to $R=50$ Ω. **d** the load changes from $R=50$ Ω to R-$L=25$ Ω-15 mH

The experimental results indicate that the proposed topology performs well in different conditions.

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