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ORIGINAL ARTICLE

A modular switched-capacitor multilevel inverter featuring voltage gain ability

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Abstract
This article presents a modular switched-capacitor multilevel inverter which uses two capacitors and a single dc source to obtain triple voltage gain. It is worth noting that the inherent inversion capacity removes the H-bridge, which can efficaciously diminish the voltage stress of switches, and the maximum voltage stress (MVS) on devices is kept within $2V_{dc}$. Additionally, the proposed topology is able to integrate inductive load, and the capacitor voltage self-balancing can be achieved. Moreover, the modular structure also has an expandable topology which can generate more levels and raise the voltage gain by using multiple switched-capacitor units, meanwhile the voltage stress on power switches can be kept within $2V_{dc}$. Furthermore, comprehensive analysis and comparison with other multilevel inverters have been implemented to certify the superiority of the proposed topology. Finally, the steady-state and dynamic performance of the proposed topology is examined through a seven-level inverter prototype, the validity and practicability of the topology are verified by simulations and experiments.

Keywords Multilevel inverter · Switched-capacitor · Voltage gain · Voltage stress

1 Introduction

To achieve net-zero carbon emission, the use of renewable energy like solar energy and wind energy is increasing. The conversion of DC to AC is an important interface for the photovoltaic power generation system. The DC voltage produced by the panels is low, which needs an inverter with a voltage boosting capability to meet the applications of medium voltage systems.

Multilevel inverters (MLIs), which are composed of power switches, capacitors and other components, can generate multiple voltage levels with low total harmonic distortion and also play a crucial role in energy conversion systems including photovoltaic power generation [1–3]. Conventional MLIs can be divided into three types: diode-clamped multilevel inverter [4, 5], flying capacitor multilevel inverter [6, 7] and cascaded H-bridge multilevel inverter [8, 9]. However, the diode-clamped MLIs employ a lot of clamping diodes to obtain multilevel output, and the flying capacitor MLIs need numerous clamping capacitors which need a complex control strategy to achieve the voltage-self-balance. Cascaded H-bridge MLIs can obtain multilevel voltage by utilizing multiple isolated sources, which leads to an increase in cost and limits the application scenarios. It is noteworthy that the modular multilevel converters have come to be emerging multilevel voltage converter topology due to their modularity and superb performance. However, the capacitor voltage balancing strategies are complex [10].

To overcome the gaps of the above-mentioned converters, the switched-capacitor multilevel inverters (SCMLIs) have been the popular method, which has the advantages of reducing the dv/dt on switches, voltage-self-balance, low switching frequency, and so on [11, 12]. The SCMLIs can obtain voltage gain using a switched-capacitor technique, and the polarity of the output voltage can be changed through the H-bridge structure [13–15]. The switched-capacitor inverter proposed in [13] can achieve seven-level output, which uses fewer power devices than the traditional multilevel inverter

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and reduces the voltage fluctuation of the capacitor. The work [15] also proposes a 7-level inverter with self-voltage balancing, which can integrate inductive loads. However, the above SCMLIs only output a limited number of levels and achieve a low boosting factor. Some expandable SCMLIs with H-bridge are proposed successively [16–18]. The expandable SCMLIs with two different topologies are proposed in [17]. The inverter can be extended by employing n units to increase boosting factor. A new inverter topology structure is proposed based on switched capacitor (SC) cell in [18], which can be expanded to obtain more output levels and the capacitor voltage is self-balanced as well.

The above designs have a common demerit of using an H-bridge to change voltage polarity, which leads to power switches sustain the crest value of output voltage. Therefore, the switched-capacitor inverter proposed in [19] can output seven-level without H-bridge, and maximum voltage stress is kept within $2V_{dc}$ which can efficaciously lower the total standing voltage (TSV). Furthermore, a nine-level SCMLI is proposed in [20]. The inverter can make sure that the peak reverse voltage of switches is kept within V_{dc}, and a voltage gain of 2 is obtained. With the development of research, expandable multilevel inverters without H-bridge have been proposed [21, 22]. The topology proposed in [21] has a novel structure of switched-capacitor, and numerous voltage levels can be obtained to improve the boosting factor. However, the maximum voltage stress of power switches is the peak of output voltage. The switched-capacitor inverter proposed in [22] can boost input voltage with reduced power switches, and the voltage of all capacitors is self-balanced without using other circuits. The topology removed H-bridge because of the inherent polarity generation circuit since the voltage stress is also reduced.

The H-bridge is replaced by two half-bridges on both sides of the inverters to diminish the stress on switches [23–25]. The inverter proposed in [23] set an appropriate ratio of dc sources to significantly increase the output levels. However, the stress of some switches also is the maximum value of output voltage, the same issue can be found in [24]. The inverter proposed in [25] has low voltage stress on switches, but numerous devices are employed to reduce voltage stress.

In this study, a 7-level modular switched-capacitor inverter is proposed, the topology can obtain triple voltage gain with two capacitors. Additionally, the maximum voltage stress (MVS) of switches is kept within $2V_{dc}$, and the inverter can achieve the inversion process without H-bridge. Moreover, the capacitor voltage can be self-balanced which simplifies the control strategy. Based on the above analysis, a comprehensive comparison has been carried out, which is summarized in Table 1.

2 Configuration and operation principle

In this section, the working principle of the switched-capacitor is given following the introduction of the topology. On this basis, a bidirectional switched-capacitor module is submitted. Then the proposed SCMLI is formed through the combination of the modules.

2.1 Switched-capacitor module

To reduce the stress on switches and obtain the boosting factor, Fig. 1a shows a bidirectional switched-capacitor module of the proposed topology. The switched-capacitor module is presented in the shadow square. It can be seen

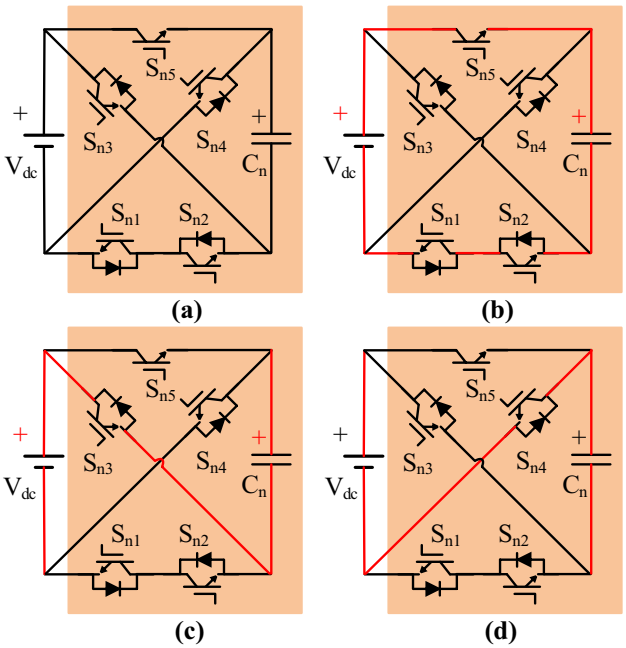

Fig. 1 Switched-capacitor modules

Table 1 Comparison between the previous topologies and the proposed topology

The gaps of previous topologies	The method of proposed topology
High MVS of switches: in topologies [13, 14, 18]	The MVS of all switches is kept within $2V_{dc}$
Multiple dc sources are employed: in topologies [16, 23, 24]	Single dc source is used
Low voltage gain: in topologies [11, 19, 20]	A triple voltage gain is obtained
Complex control of capacitor voltage: in topologies [6, 7, 10]	The capacitor voltage is self-balanced

that the switched-capacitor module is composed of five switches and one capacitor, in which S_{n1}–S_{n4} are switches with anti-parallel diodes and S_{n5} is the switch without an anti-parallel diode. When switches S_{n3} and S_{n4} are turned off but other power switches are turned on, the capacitors C_n can be charged in parallel with the dc source, as shown in Fig. 1b. When the switches S_{n3} are turned on and other switches are turned off, the capacitors C_n are discharged in series with the dc source, as shown in Fig. 1c. Similarly, the switches S_{n4} are turned on and other switches are turned off in Fig. 1d, and the capacitors C_n are discharged by the dc source, but the polarity of the output voltage is opposite to the state of Fig. 1c. Obviously, the maximum voltage stress of switches S_{n3} and S_{n4} are kept within $2V_{dc}$, and the MVS of other switches are kept within V_{dc}. Thus, the total standing voltage (TSV) of the presented module is expressed as:

$$\mathrm{TSV} = 2V_{dc} + 2V_{dc} + 3V_{dc} = 7V_{dc}. \quad (1)$$

Therefore, the proposed switched-capacitor module can achieve twice the voltage gain and effectively reduce the voltage stress of switches.

2.2 Proposed topology

Figure 2 presents a generalized SCMLI. It can be seen that the topology is composed of multiple switched-capacitor modules which can raise the output levels and obtain a higher boosting factor. To facilitate analysis, this study takes the proposed seven-level inverter as the instance in Fig. 3a, which can achieve the capacitor voltage self-balancing and obtain triple voltage gain with two capacitors. The H-bridge is eliminated due to the inherent inversion capacity. The seven working modes of the inverter are shown in Fig. 3b–h when the output levels are: $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$ and 0.

2.3 Operating principle

The working state of the 7-level topology is presented in Table 2, wherein the bold values are the alternative operating states which can obtain the same output voltage level, "C", "D", and "–" demonstrate the charging, discharging, and idle modes of the capacitors, respectively.

The working principle of the inverter is analyzed as shown follows:

(1) $V_{out} = 3V_{dc}$: When the switches S_{13} and S_{23} are turned ON, capacitors C_1 and C_2 can be charged to V_{dc}, as shown in Fig. 3b. Then output voltage $3V_{dc}$ is synthesized by turning ON the switches S_1 and S_4.

(2) $V_{out} = 2V_{dc}$: When the switches S_{11}, S_{12} and S_{23} are turned ON, capacitor C_1 is discharged in series with capacitor C_2, as shown in Fig. 3c. Then output voltage $2V_{dc}$ can be synthesized by turning ON the switches S_1 and S_4.

(3) $V_{out} = \pm V_{dc}$: When the switches S_{11}, S_{12}, S_{15}, S_{21}, S_{22} and S_{25} are turned ON, capacitors C_1 and C_2 can be charged to V_{dc}, as shown in Fig. 3d, f. The output voltage V_{dc} is synthesized by turning ON the switches S_1 and S_4, while the negative output voltage $-V_{dc}$ can be obtained by turning ON switches S_2 and S_3.

(4) $V_{out} = 0$: When the switches S_{11}, S_{12}, S_{15}, S_{21}, S_{22} and S_{25} are turned ON, capacitors C_1 and C_2 can be charged to V_{dc}, as shown in Fig. 3e. Zero output level is synthesized by turning ON switches S_1 and S_3.

(5) $V_{out} = -2V_{dc}$: When the switches S_{14} and S_{24} are turned ON, capacitor C_1 is discharged in series with capacitor C_2, as shown in Fig. 3g. Then output voltage $-2V_{dc}$ can be synthesized by turning ON the switches S_1 and S_3.

(6) $V_{out} = -3V_{dc}$: When the switches S_{14} and S_{24} are turned ON, capacitors C_1 and C_2 can be discharged in series with dc source, as shown in Fig. 3h. The output voltage $-3V_{dc}$ can be synthesized by turning ON the switches S_2 and S_3.

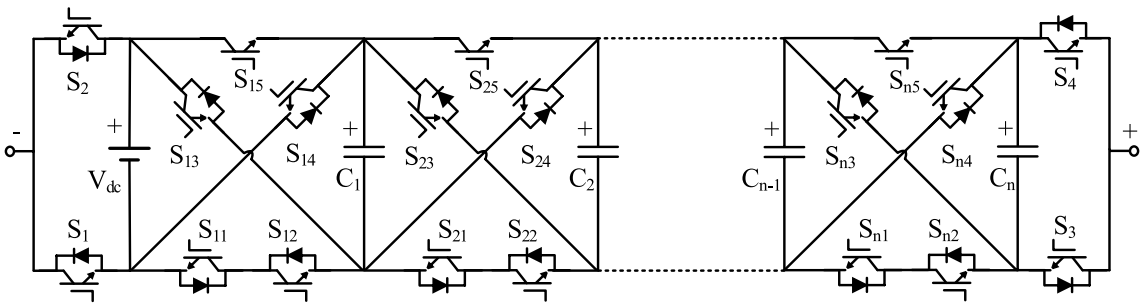

Fig. 2 Proposed generalized SCMLI

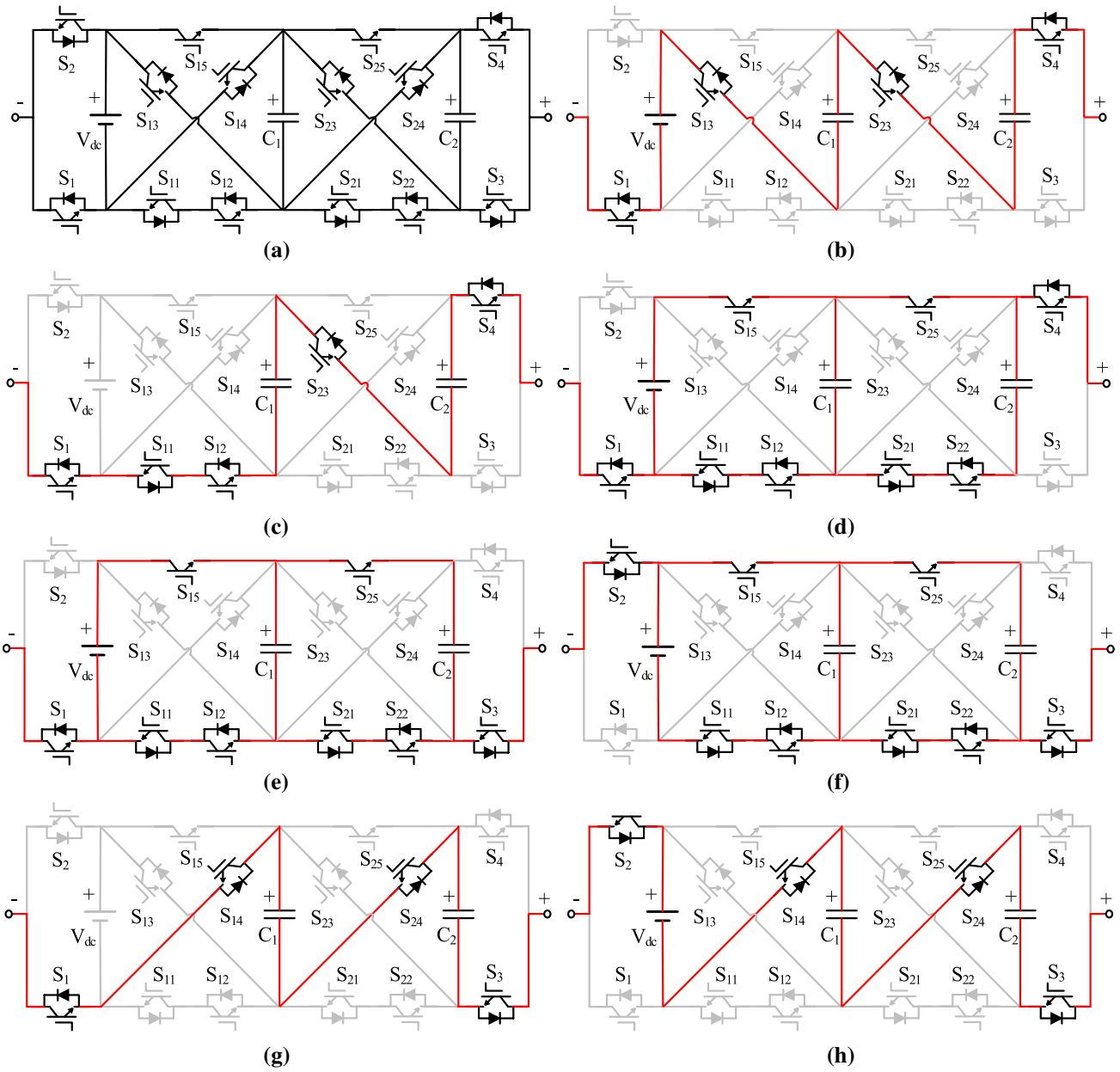

Fig. 3 Proposed 7-level inverter: **a** topological structure; **b**–**h** the working states of the inverter: $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$

3 Modulation strategy

Various modulation techniques have been applied to multilevel inverters, including space vector modulation, multicarrier modulation, selective harmonic elimination modulation. In this article, the phase disposition pulse width modulation (PD-PWM) is selected for the proposed topology due to the convenience and low total harmonic distortion (THD).

The modulation principle of a proposed 7-level inverter can be seen in Fig. 4. There are six triangular carriers e_1–e_6 with equal amplitude A_c and frequency f_c, and a sinusoidal reference wave with the amplitude A_{ref} and frequency 50 Hz (f_o). These triangular carriers are compared with reference waves to engender six pulse signals u_1–u_6. According to the working states, the logical groupings of switches are shown in Fig. 5.

In the PD-PWM strategy, the modulation index is dependent on the amplitude of triangular carriers and sinusoidal wave. Thus, the modulation index M varies between 0 and 1, which can be expressed as:

Table 2 Operating states of the proposed topology

Modes	On-state switches	Capacitors C_1, C_2	Levels
1	S_1, S_{13}, S_{23}, S_4	D, D	$3V_{dc}$
2	S_1, S_{11}, S_{12}, S_{23}, S_4	D, D	$2V_{dc}$
3	**S_1, S_{11}, S_{12}, S_{15}, S_{23}, S_4**	**C, D**	
4	**S_1, S_{11}, S_{12}, S_{21}, S_{22}, S_4**	**–, D**	V_{dc}
5	**S_1, S_{11}, S_{12}, S_{15}, S_{23}, S_3**	**C, –**	
6	S_1, S_{11}, S_{12}, S_{15}, S_{21}, S_{22}, S_{25}, S_4	C, C	
7	S_1, S_{11}, S_{12}, S_{15}, S_{21}, S_{22}, S_{25}, S_3	C, C	0
8	S_2 , S_{11}, S_{12}, S_{15}, S_{21}, S_{22}, S_{25}, S_3	C, C	$-V_{dc}$
9	**S_2, S_{11}, S_{12}, S_{15}, S_{21}, S_{22}, S_3**	**C, –**	
10	**S_1, S_{11}, S_{12}, S_{24}, S_3**	**–, D**	
11	**S_2, S_{11}, S_{12}, S_{15}, S_{24}, S_3**	**C, D**	$-2V_{dc}$
12	S_1, S_{14}, S_{24}, S_3	D, D	
13	S_2, S_{14}, S_{24}, S_3	D, D	$-3V_{dc}$

$$M = \frac{A_{ref}}{3A_c}, \tag{2}$$

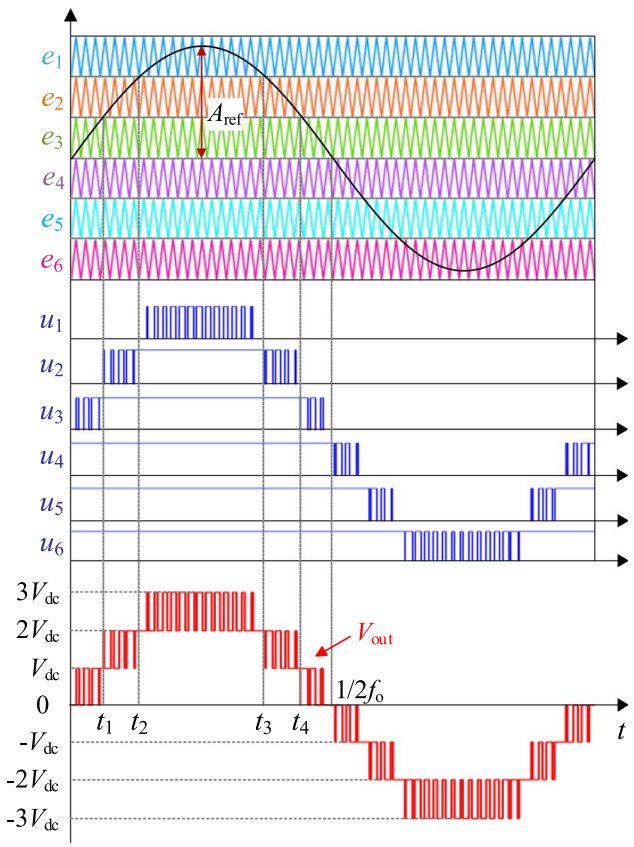

Fig. 4 Modulation principle of the proposed inverter

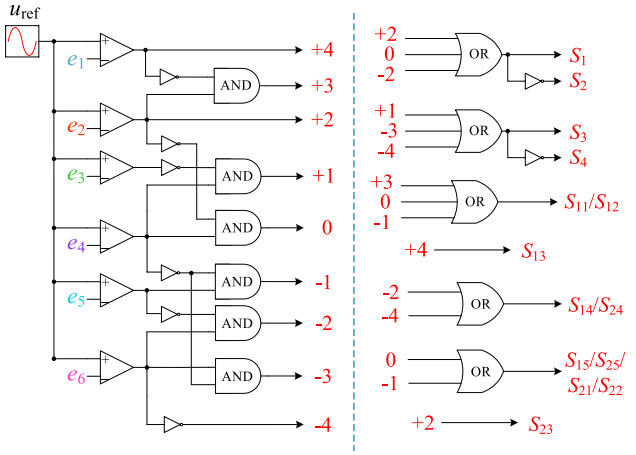

Fig. 5 Modulation logic of the 7-level inverter

where A_{ref} and A_c are the amplitudes of the reference signal and carrier signals. The topology can output different levels with the change of M between 0 and 1.

In Fig. 4, the instants t_i ($i = 1, 2, 3, 4$) are the intersection points of sinusoidal reference wave and triangular carriers, which are expressed as:

$$t_1 = \frac{\arcsin\left(\frac{1}{3M}\right)}{2\pi f_o}, \tag{3}$$

$$t_2 = \frac{\arcsin\left(\frac{2}{3M}\right)}{2\pi f_o}, \tag{4}$$

$$t_3 = \frac{\pi - \arcsin\left(\frac{2}{3M}\right)}{2\pi f_o}, \tag{5}$$

$$t_4 = \frac{\pi - \arcsin\left(\frac{1}{3M}\right)}{2\pi f_o}, \tag{6}$$

where f_o is the frequency of output voltage. When M is set to 0.9, the proposed inverter can obtain a seven-level voltage and achieve triple voltage gain.

4 Analyses of capacitance

The proposed multilevel inverter has a self-voltage balancing ability without any auxiliary circuits. The capacitors C_1 and C_2 are charged to V_{dc} in parallel with dc source in each cycle, which is can be seen in Table 2 and Fig. 3.

The capacitance in the multilevel inverter is important to achieve multilevel output and voltage gain. Additionally, the voltage ripple of capacitors should be maintained within an acceptable range to enhance the quality of output voltage. The quality of output voltage is affected by capacitor voltage ripple, and the maximum continuous discharge has a bearing on the voltage ripple. Therefore, the capacitor voltage ripple is diminished efficaciously by choosing the appropriate capacitance.

Based on the operating principle and modulation strategy, it can be observed that capacitors C_1 and C_2 have the same operating states. Both capacitors can be discharged at $\pm 3V_{dc}$ and $\pm 2V_{dc}$ levels, and be charged at $\pm V_{dc}$ and 0 levels. Therefore, the maximum discharging interval of capacitors C_1 and C_2 is $[t_1$–$t_4]$.

The capacitor voltage ripple is mainly affected by the maximum discharging amount. The output voltage and load current of the topology have the same phase under resistive load, the maximum value of load current is the middle of the integration period, and the discharge capacity of the capacitor is the largest. The output voltage and current have different phases under inductive load, the peak value of the load current is not the middle of the integration period, which reduces the discharge capacity of the capacitor. Therefore, the capacitance value calculated by the pure resistive load condition is applicable to inductive load. As can be seen from Fig. 4, the maximum continuous discharging amount ΔQ_C of C_1 and C_2 within $[t_1$–$t_4]$ can be calculated as:

$$\Delta Q_C = \int_{t_1}^{t_4} \frac{V_o}{R} \sin(2\pi f_o t) \mathrm{d}t, \tag{7}$$

where V_o is the output voltage, R is the load resistance and f_o is the frequency of output voltage.

As shown in Fig. 4 the output voltage V_o is $2V_{dc}$ at intervals $[t_1, t_2]$ and $[t_3, t_4]$, and the output voltage V_o is $3V_{dc}$ at interval $[t_2, t_3]$. Therefore, a further calculation can be given as:

$$\Delta Q_C = \frac{V_{dc}(2\cos 2\pi f_o t_1 + \cos 2\pi f_o t_2 - \cos 2\pi f_o t_3 - 2\cos 2\pi f_o t_4)}{2\pi f_o R}. \tag{8}$$

When $k\%$ is presumed the constant that describes the maximum acceptable voltage ripple, capacitances of C_1 and C_2 can be determined as:

$$C_1 = C_2 \geq \frac{\Delta Q_C}{k\% \cdot V_{dc}}. \tag{9}$$

The size of the capacitor is usually set according to the principle that the capacitor voltage ripple is not more than 10% of the rated voltage of the capacitor, then the capacitance is calculated by:

$$C_1 = C_2 \geq \frac{\Delta Q_C}{0.1 \cdot V_{dc}}, \tag{10}$$

where V_{dc} is the voltage of capacitors C_1 and C_2.

5 Comparison

To validate the merits of the proposed topology, this study compares and analyzes a total number of components, MVS and TSV in combination with the characteristics of the traditional multilevel inverters [5, 8], the expandable SCMLIs [11, 16, 18] and the new switched-capacitor inverters [20, 22, 25]. For the convenience of comparison, Table 3 gives the specific values of the number of devices in various comparison topologies, the maximum voltage stress MVS and the total standing voltage TSV of switches.

For the convenience of comparison, the output levels of all inverters are set to $2n+1$. The input voltage is uniformly V_{dc} if only a single dc source is employed. The following is

Table 3 Comparison of the proposed inverter and other structures ($2n+1$ levels)

Iterms	[5]	[8]	[11]	[16]	[18]	[20]	[22]	[25]	Proposed
Levels	$2n+1$	$2n+1$	$2n+1$	$2n+1$	$2n+1$	$2n+1$	$2n+1$	$2n+1$	$2n+1$
Voltage gain	1	n	1.5	n	n	2	n	n	n
DC source	V_{dc}	$n(V_{dc}, 2V_{dc})/3$	$nV_{dc}/3$	V_{dc}	V_{dc}	$nV_{dc}/4$	$nV_{dc}/2$	V_{dc}	V_{dc}
Capacitors	$2n$	No	$2n/3$	$n-1$	$n-1$	$n/2$	$n/2$	n	$n-1$
Switches	$4n$	$3n$	$10n/3$	$2n+2$	$n+4$	$3n$	$2n+2$	$5n$	$5n-1$
Diode	$4n^2-2n$	No	No	$n-1$	$2n-2$	No	$n/2$	No	No
H-bridge	No	No	No	Yes	Yes	No	No	No	No
MVS	$V_{dc}/2$	$3V_{dc}$	V_{dc}	nV_{dc}	nV_{dc}	V_{dc}	$4V_{dc}$	$2V_{dc}$	$2V_{dc}$
TSV	$(2n^2+n)V_{dc}$	$6nV_{dc}$	$10nV_{dc}/3$	$(8n-4)V_{dc}$	$(n^2+9n)V_{dc}/2$	$11nV_{dc}/4$	$(6n-4)V_{dc}$	$(7n-2)V_{dc}$	$(7n-3)V_{dc}$

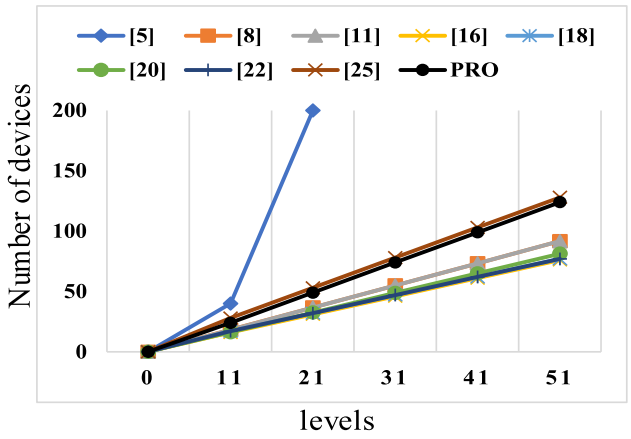

Fig. 6 Comparison of total components

the detailed analysis of the topology in the existing literatures and the topology proposed in this study.

5.1 The total components

Figure 6 gives the comparison of the total components including switches, diodes and dc sources. for some existing inverters and the proposed inverter. It is not hard to see that the number of total components of the proposed inverter is less than the MLIs proposed in [5, 25]. The inverters in [8, 11, 20, 22] utilize multiple dc sources to obtain more output levels, which leads to an increase in cost and limits the application scenarios. The topologies proposed in [16, 18] employ H-bridge to alter the polarity of output voltage, while voltage stress on switches will increase with the growth of output levels. Comparing with the number of total devices of the SCMLIs, the proposed inverter only uses a dc source to achieve boosting factor of 3 and also reduces the voltage stress on switches which can be kept constant in the extended structure.

5.2 MVS

On the basis of the above study of the proposed working principle, the MVS of switches S_{n3} and S_{n4} are $2V_{dc}$, and the MVS of other switches are V_{dc}. Figure 7 shows the comparison results of MVS values between the existing inverters and the proposed inverter. As the growth of output levels, the voltage stress on power switches is still kept within $2V_{dc}$, which is a significant advantage of the proposed switched-capacitor topology.

Although the inverters proposed in [16, 18] utilize less devices, the MVS on power devices will raise with the growth of levels, which leads to the MVS of switches being the amplitude of output voltage. With the increase in output levels, the MVS in other topologies can be kept constant. For the extended topology, the topology proposed in [5] has lower values of MVS, but numerous clamping diodes are employed to achieve multilevel output, which needs a complex control strategy to achieve self-voltage balance. The MVS of the inverters proposed in [11, 20] can be kept within V_{dc} in the extended structure, but the voltage gain of the inverter proposed in [11] is 1.5, and the inverter proposed in [20] has a voltage gain of 2.

The proposed 7-level topology can obtain triple voltage gain, and the MSV of all power switches can be kept within $2V_{dc}$, which can efficaciously reduce the total standing voltage. Although MVS of the inverters proposed in [8, 22] can be kept constant with the growth of voltage levels, multiple dc sources are employed to raise output levels and the MVS on switches is higher than the proposed topology. Moreover, the topology proposed in [25] uses more devices to obtain constant voltage stress. Therefore,

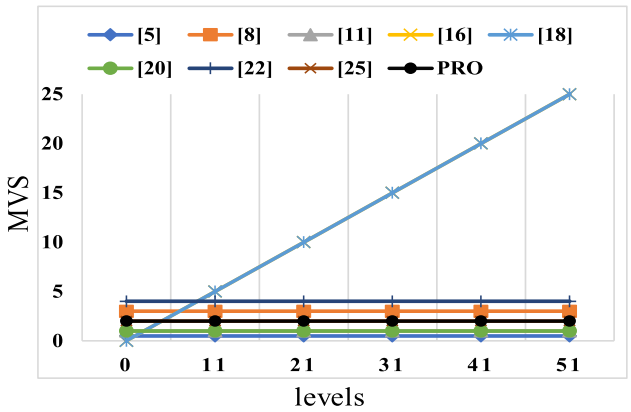

Fig. 7 Comparison of MVS

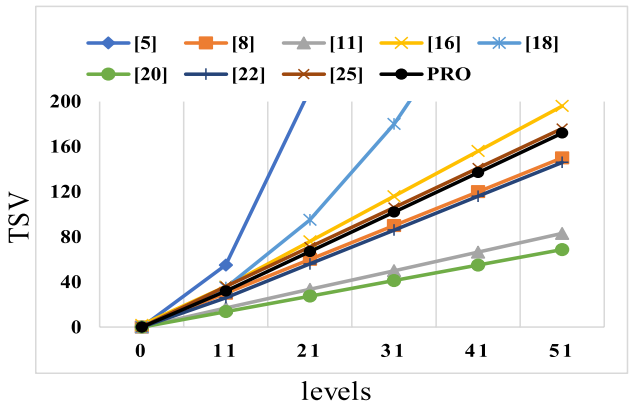

Fig. 8 Comparison of TSV

the proposed inverter has great potential in the fields of medium and high voltage.

5.3 TSV

Figure 8 shows a comparison of the TSV values between the previous literatures and the topology proposed in this study. According to the chart, the TSV of several topologies increases with the growth of output levels. The TSV of the proposed inverter is greatly decreased in contrast to other inverters, which can effectively reduce the switching losses during the operation of the inverter and increase the service life of the power switches.

It can be seen from the above comparisons that the inverters proposed in [11, 20] have lower values of TSV, which is beneficial to improve the efficiency of inverters. However, the voltage gain cannot be raised with the increase in output levels, and the application scenarios will be limited. The inverters proposed in [8, 22] also have lower values of TSV, and the boosting factor can be raised in extended topology. However, multiple dc sources are utilized to raise output levels, which leads to an increase in cost and limits the application scenarios. The TSV of the inverters proposed in [16, 18] is higher due to the use of an H-bridge, which results in the peak value of the output voltage on switches. And the inverter in [25] has higher TSV because more switches and capacitors are employed.

Compared with the above-mentioned inverters, the proposed topology has a higher boosting factor. Although the proposed inverter uses lots of switches, it does not involve other components. In addition, the MVS on switches of the proposed inverter is kept constant with a single dc source, since the topology is applicable to medium and high voltage systems. Therefore, although the proposed topology uses many switches, it still has advantages in improving the boosting factor and reducing the stress on switches compared to previous MLIs.

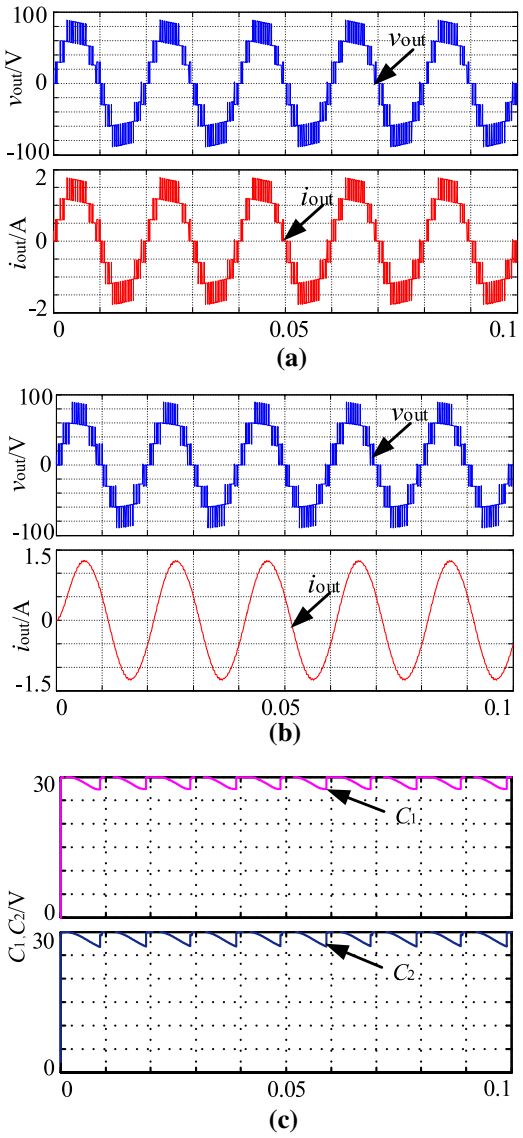

Fig. 9 Simulation results: **a** output voltage and current under pure resistive load; **b** output voltage and current under resistive–inductive load; **c** voltage of capacitors

Table 4 Simulation components

Components	Values
DC source	30 V
Capacitances, C_1 and C_2	2200μF
Triangle carriers frequency	2 kHz
Output frequency	50 Hz
Modulation index	0.9
Loads	50 Ω & 50 Ω–15 mH

6 Simulation and experiment analysis

6.1 Simulation results

According to the above analysis, the feasibility of the proposed inverter has been checked with different conditions. The simulation model of the proposed topology is carried out in MATLAB/Simulink environment. Simulation components have been given in Table 4. According to Eq. (10) and simulation parameters, the capacitance value should

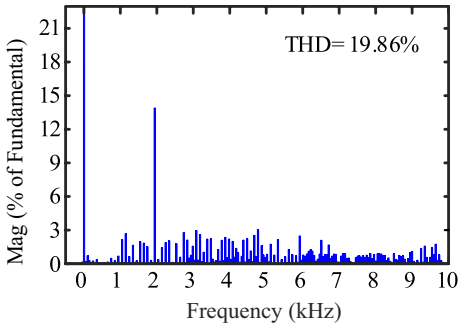

Fig. 10 THD of the output voltage

Table 5 Experimental components

Components	Values
Optocoupler-driver	TLP250
Switches (MOSFET)	SPP20N60C3
Current probe	Tektronix A622
Input DC voltage	30 V
Capacitances, C_1 and C_2	2200μF
Output frequency	50 Hz
Modulation indexes	0.9, 0.6, 0.3
Loads	50 Ω & 50 Ω–15 mH

be greater than 1758 μF, so the capacitor is chosen to be 2200 μF to assure that capacitor voltage ripple can be within the required range.

Figure 9 gives the simulation results, and the waveform diagram of output voltage and load current under pure resistive load are presented in Fig. 9a. It is not hard to see that the proposed topology can generate seven-level voltage and achieve a triple voltage gain. When the resistive-inductive load is used, Fig. 9b gives the waveform diagram of output voltage and load current. As shown in Fig. 9b, the load current is a sinusoidal wave. It is obvious that the inverter can carry both inductive and pure resistive loads.

The voltage ripple of capacitors C_1 and C_2 is given in Fig. 9c. The capacitor voltages can be self-balanced with low voltage ripple. And the fluctuation range is between 27 and 30 V, which satisfies the design requirements of the capacitor voltage ripple range. Figure 10 presents the Fast Fourier Transform of the proposed topology when the modulation index is 0.9.

The THD of the inverter is 19.86%, and 40th harmonic component is higher than the others since the carrier frequency is 2 kHz. The low THD can also simplify the design of the filter.

6.2 Experimental results

To validate the feasibleness of topology, this study evaluates the proposed inverter through a small experimental prototype. Table 5 shows the basic components required in the experiment.

The inverter is experimentally verified under different load conditions, and then the experimental results are analyzed. An experimental prototype of a 7-level inverter has been implemented to validate its effectiveness, as shown in Fig. 11a. Figure 11b presents a waveform diagram of output voltage and current. It's obvious that the topology can obtain a seven-level output waveform when a load is purely resistive, the amplitude of output voltage can reach 90 V. Load current is also a seven-level waveform and the maximum load current is about 1.8 A, which is consistent with the theory.

Figure 11c gives the output voltage and load current under resistive-inductive load. It's obvious that the inverter can output a seven-level staircase wave. The levels are ±90 V, ±60 V, ±30 V and 0, respectively. The load current is a sinusoidal wave which works stably. Figure 11d shows the voltages of capacitors C_1 and C_2, which fluctuate around 29 V. It is not hard to see that capacitor voltages can achieve self-balancing, and voltage ripple is kept within 3 V, which is in good argument to the above analysis. Figure 11e gives the currents of capacitors C_1 and C_2, which behave similarly and change periodically. A peak current will appear when the capacitor is charged. It can be seen from Fig. 11e that currents amplitude of capacitors C_1 and C_2 are similar in magnitude, which is within 10 A. The above are graphs of the steady-state experiment. All in all, when the inverter starts to work, the output voltage and load current can be kept stable, meanwhile the steady-state performance is also very good.

Figure 11f, g present the output voltage and current under variable output frequency. For the experimental waveforms whose output frequency varies between 50 and 200 Hz, the proposed inverter responds immediately, and the waveform after the change is stable, which satisfies the normal working conditions of the inverter.

Figure 11h, i show waveform diagrams of output voltage and current with variable modulation indexes. The proposed inverter has a quick response and works normally. Therefore, the proposed inverter has a good dynamic performance. When the frequency and modulation degree of the inverter change greatly, the inverter can still respond quickly and work normally.

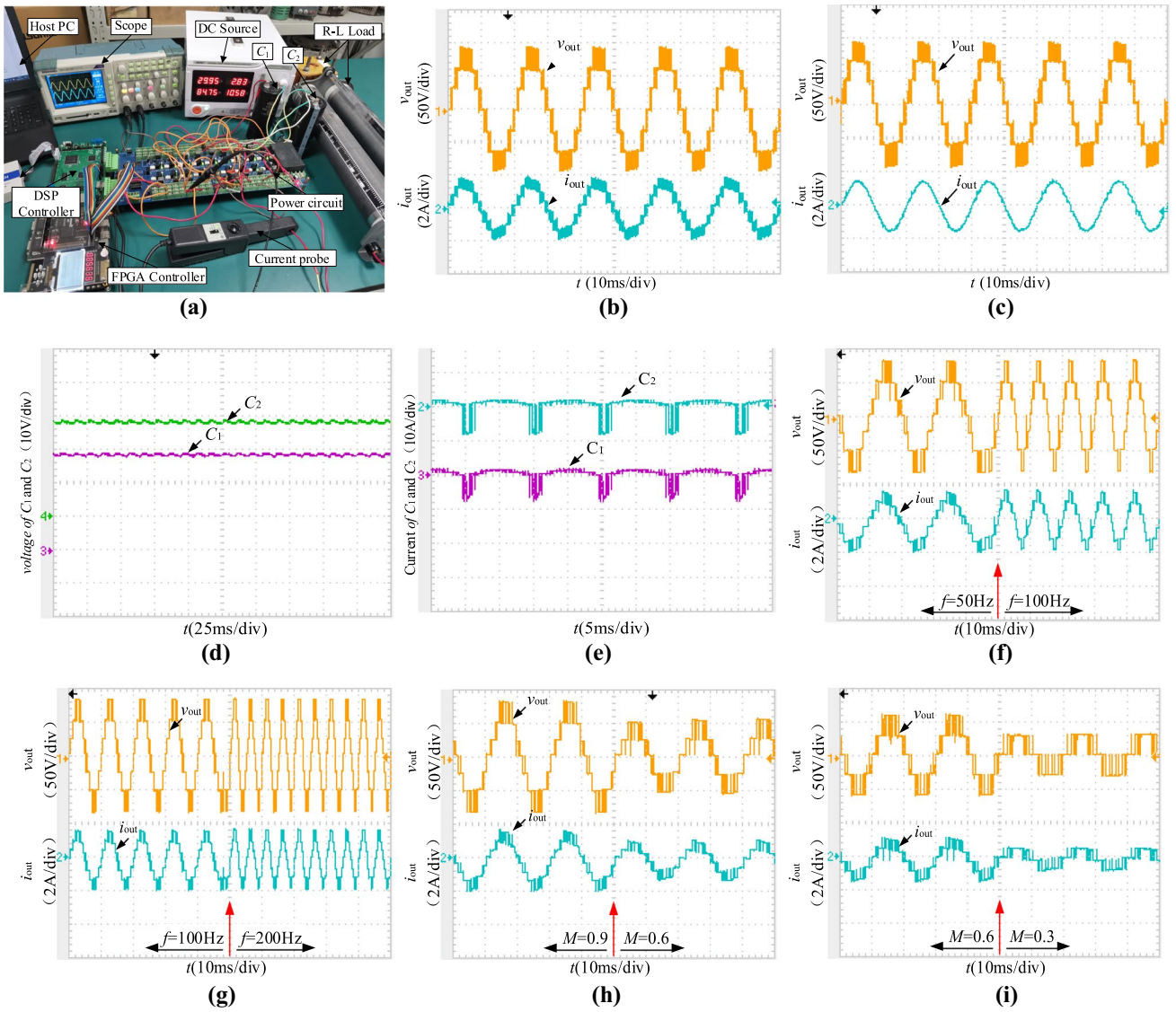

Fig. 11 Experimental results: **a** experimental prototype; **b** output voltage and current under pure resistive load; **c** output voltage and current under resistive–inductive load; **d** voltage of capacitors; **e** current of capacitors; **f**, **g** output voltage and current under different output frequency; **h**, **i** output voltage and current under different modulation indexes

7 Conclusion

This article proposes a modular switched-capacitor inverter which employs a single dc source. The inverter can generate seven-level and obtain triple voltage gain. Moreover, the maximum voltage stress on switches can be kept within $2V_{dc}$ due to the elimination of H-bridge. The capacitors can be charged to V_{dc} in each cycle since voltage-self-balance ability is conducive to simplify the control strategy. Furthermore, the proposed inverter can be flexibly extended to achieve more levels and a higher boosting factor by adding switched-capacitor units. When the boosting factor is n, the output levels are $2n+1$ and the MVS of switches is still $2V_{dc}$. Simulations and an experimental prototype have been carried out to examine the practicability of the inverter. The results signify that the topology works well with variable situations.

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