Master's Thesis

Design of Phase-Locked Loop with Switched Capacitor Loop Filter and Source Switched Charge Pump

Switched Capacitor Loop Filter 와 Source Switched Charge Pump 를 이용한 Phase-Locked Loop 의 설계

by

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February, 2022

Department of Electrical and Computer Engineering
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Seoul National University

Design of Phase-Locked Loop with Switched Capacitor Loop Filter and Source Switched Charge Pump

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이 논문을 공학석사 학위논문으로 제출함
2022 년 2 월

서울대학교 대학원
전기·정보공학부
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이용재의 석사 학위논문을 인준함
2022 년 2 월

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Design of Phase Locked-Loop with Switched Capacitor Loop Filter and Source Switched Charge Pump

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A Thesis Submitted to the Department of
Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for the Degree of
Master of Science
at
SEOUL NATIONAL UNIVERSITY

February, 2022

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Abstract

This thesis proposes a low integrated RMS jitter and low reference spur phase-locked loop (PLL) using a switched capacitor loop filter and source switched charge pump. The PLL employs a single tunable charge pump which reduces current mismatch across wide control voltage range and charge sharing effect to get high performance of reference spur level. The switched capacitor loop filter is adopted to achieve insensitivity to temperature, supply voltage, and process variation of a resistor. The proposed PLL covers a wide frequency range and has a low integrated RMS jitter and low reference spur level to target various interface standards. The mechanism of switched capacitor loop filter and source switched charge pump is analyzed.

Fabricated in 40 nm CMOS technology, the proposed analog PLL provides four-phase for a quarter-rate transmitter, consumes 6.35 mW at 12 GHz using 750 MHz reference clock, and occupies an 0.008 mm^2 with an integrated RMS jitter (10 kHz to 100 MHz) of 244.8 fs. As a result, the PLL achieves a figure of merit (FoM) of -244.2 dB with high power efficiency of 0.53 mW/GHz, and reference spur level is -60.3 dBc.

Keywords : phase-locked loop (PLL), source switched charge pump, switched capacitor loop filter, voltage-controlled oscillator (VCO), phase noise, reference spur

Student Number : 2020-24729

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Chapter 1

Introduction

1.1 Motivation

As the requirement of data rate increases, high-frequency clock generation is required for a high-speed link, and the jitter performance of a high-speed clock becomes more critical. The PLL achieves clock generation of high speed serial interface at the transmitter (Tx), so low jitter PLL is essential for high-speed serial link. With the emergence of next-generation interface standards (PCI Express Gen 6 and OIF-CEI), more accurate and faster clock generation is required for serial links.

All-Digital Phase-Locked Loop (ADPLL) occupies a large portion of the state-of-the-art PLLs[1], because of its portability, small area, and low process-voltage-temperature variation. However, the design difficulty of high-resolution time to digital converter (TDC) still exists, and quantization noise of analog to digital converting

blocks is challenge in designing ADPLL. Also, clock domain crossing should be considered carefully because loop delay of up and down update path is quite large and clock frequency of digital block is usually different from the frequency of others. For this reason, analog charge pump PLL (CPPLL) is still being researched and takes some portions of the state-of-the-art PLLs. Analog PLL doesn't need digital blocks, so it saves a large area of digital blocks, but instead, it requires passive elements (resistor and capacitor). Of course, it is free from quantization noise, so design difficulty is diminished. LC oscillator has been much more researched recently due to its noise performance. However, the large area of the inductor, its narrow frequency range, and the difficulty of generating multi-phase becomes challenging. Because of these matters, high-speed ring oscillator based PLLs have been reported [1]. Also, as CMOS technology shrinks, the performance of ring based VCO is enhanced regarding frequency range and power dissipation [2]. As a result, this thesis presents analog ring-based PLL with switched capacitor loop filter and source switched charge pump. The proposed PLL achieves -244.2 dB of a figure-of-merit (FoM) with a power efficiency of 0.53 mW/GHz and reference spur level -60 dBc.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, clock generation in the serial link, the backgrounds of PLL, and its loop analysis are explained. Then, the operation of each block and its conventional schematics are described.

In Chapter 3, the PLL with switched capacitor loop filter and source switched charge pump is introduced. A specific implementation of each block (PFD, charge pump, VCO, post VCO amplifier, and frequency divider) and its operation principle are demonstrated.

Based on the designs of Chapter 3, the measurement results are described in Chapter 4. The phase noise (integrated RMS jitter), reference spur level, and peak-to-peak jitter of PLL are measured. Measured performances are compared with the state-of-the-art PLLs in the comparison table.

Chapter 5 summarizes the proposed designs and concludes this thesis.

Chapter 2

Backgrounds

2.1 Clock Generation in Serial Link

Serial link is a link that data is transmitted from the transmitter (Tx) part to the receiver (Rx) part. Figure 2.1 shows a block diagram of serial links, including Tx, channel, and Rx. Parallelized data from the pattern generator is serialized at a serializer (SER) of the Tx, and the driver (DRV) drives serial data. This data passes through the channel, and a deserializer (DES) makes serial data parallelized after equalizing. All of these processes are processed by the clock of serial link. Clock forwarded system that transmits clock signals through the channel is still being researched. Still, usually clock of Tx is generated by PLL using a slow reference clock (Ref CLK), and the clock of Rx is generated by the clock and data recovery (CDR).

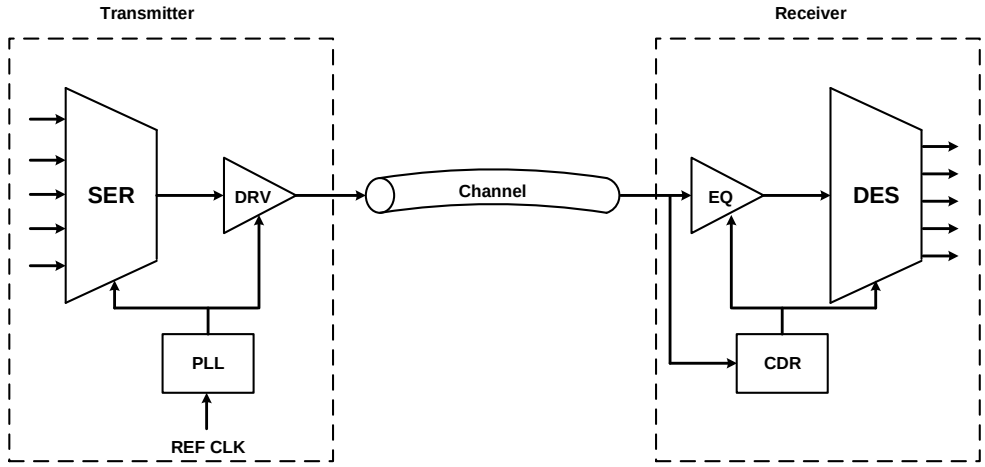


Figure 2.1 Basic block diagram of serial link.

Nowadays, as the data rate increases, a high clock frequency is required, and its accuracy and efficiency become more important. So the importance of PLL that filters noise, multiplies the frequency of the input reference clock, and delivers the clock signal to the serializer is increasing. In the aspects of the performance of the PLL, jitter is one of the essential factors in the PLL, and it is associated with the accuracy of the PLL. There are several standards of serial link, for example, PCI Express and OIF-CEI. So clock speed and RMS jitter of the PLL should satisfy the spec of serial link standards. To sum up, clock generation at Tx in the high-speed serial link is usually done by the PLL, and high frequency and accuracy of PLL should be guaranteed as the requirement of data rate increases. The basic operation and fundamental architecture of the PLL is described in Chapter 2.2.

2.2 PLL Building Blocks

2.2.1 Overview

A basic block diagram of the CPPLL is shown in Figure 2.2. A phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a frequency divider make up a classical PLL. The PFD checks the positive edge of the reference clock and the feedback clock (divided clock) and delivers an up or down (error) signal to the charge pump. The charge pump changes the error signal to the charge, which is delivered to the loop filter. The output voltage of the charge pump is determined by the loop filter that roles a kind of low pass filter composed of an RC network. This output voltage decides the frequency of the VCO and the frequency of the VCO's output, namely, the frequency of the output clock is divided by the divider. And then, this divided signal (feedback signal) is fed into the PFD, compared with the reference clock. Through the operation of the divider, the PLL's output frequency is the multiplication of the frequency of the reference clock and the dividing factor of the frequency divider. Thus, the PLL is a negative feedback loop that compares the reference clock and divider output. In the after chapters, the detailed operation and simplified schematics of each block are described. Subsequently, based on the operation of each block, loop analysis of the PLL is investigated.

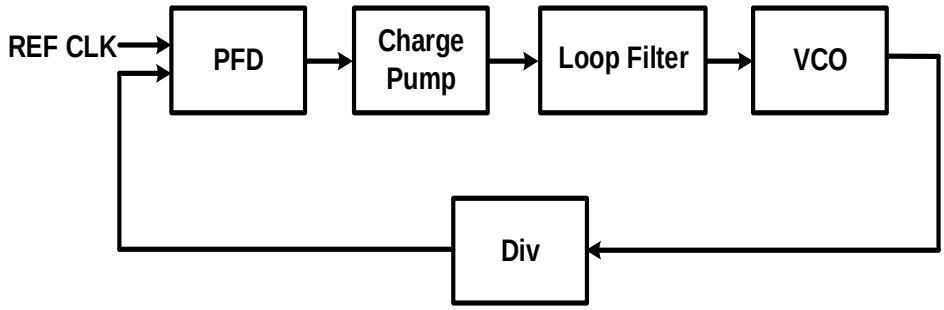


Figure 2.2 Basic block diagram of CPPLL.

2.2.2 Phase Frequency Detector

As mentioned before, a PFD compares the positive edge of the reference clock and the divided feedback clock. It produces an up and down signal that equals a mismatch between the input reference clock and the divided signal. A conventional schematic of the PFD is depicted in Figure 2.3. When the input reference precedes to the divided signal, the up signal goes up first as the input reference clock approaches its positive edge, and the down signal becomes high as the divided feedback clock approaches its positive edge [3]. After both up and down signals become high, both signals become low because the reset signal, the output of AND gate, is fed into flip-flops. The same applies to the case of the down signal. Therefore, the pulse width of error signals is ratable to the phase error between the reference signal and the divided feedback clock. Figure 2.4 represents a timing diagram of the PFD. These error signals are transmitted to the charge pump. The normalized net output (UP-DN) of PFD – phase error curve is shown in Figure 2.5. In actual implementation, to avoid the appearance of the reset signal before the up and down signals are going high at a locked state, an intended

delay is inserted at the reset signal path.

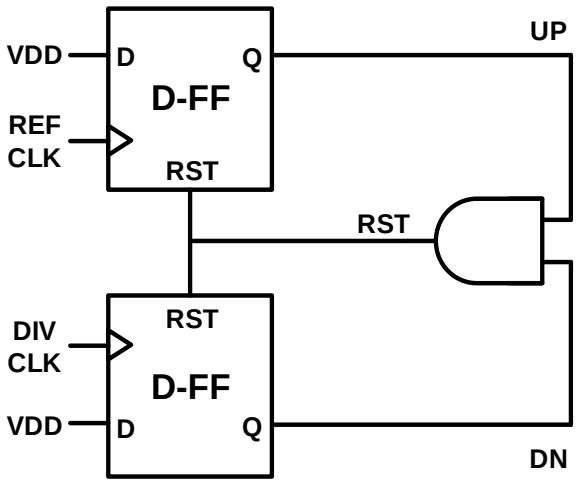


Figure 2.3 Conventional schematic of PFD.

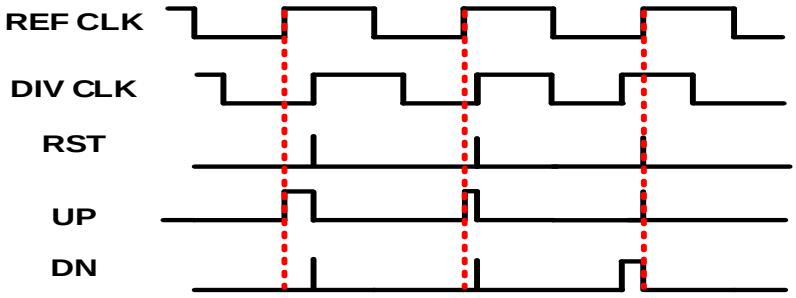


Figure 2.4 Timing diagram of PFD.

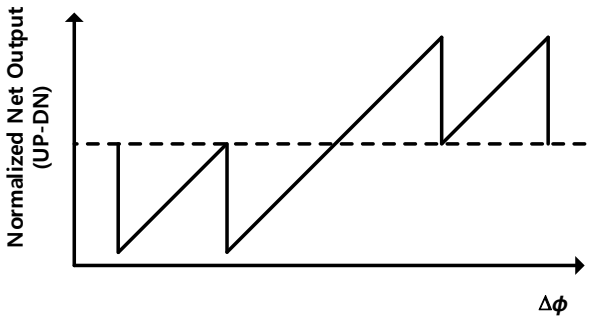


Figure 2.5 Normalized net output (UP-DN) – Phase error curve.

2.2.3 Charge Pump and Loop Filter

A charge pump converts the up or down signal to charge. Thus, it produces a kind of current pulse to a loop filter. As mentioned before, the polarity and pulse width of the error indicator is proportional to the phase difference of the reference and feedback clock. The ideal schematic of the charge pump and RC filter is depicted in Figure 2.6. Design considerations and issues will be described in Chapter 3.3, and the role of the loop filter is explained in Chapter 2.3. When designing the charge pump, up and down current mismatch should be considered because the mismatch between up and down current degrades the performance of the PLL, and this current should be almost equal over wide control voltage range.

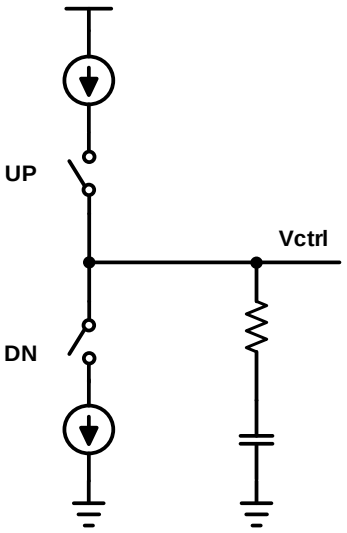


Figure 2.6 Ideal schematic of charge pump and 2nd order loop filter.

2.2.4 Voltage Controlled Oscillator

A voltage controlled oscillator is a clock (oscillating signal) generator whose frequency is regulated by an analog control voltage (Vctrl). Frequency – Vctrl curve of VCO is shown in Figure 2.7, and its slope means a gain of VCO, K_{VCO}. If the gain of VCO is large, it means that VCO covers a wide range of frequency instead of sacrificing the sensitivity to a ripple of the control voltage.

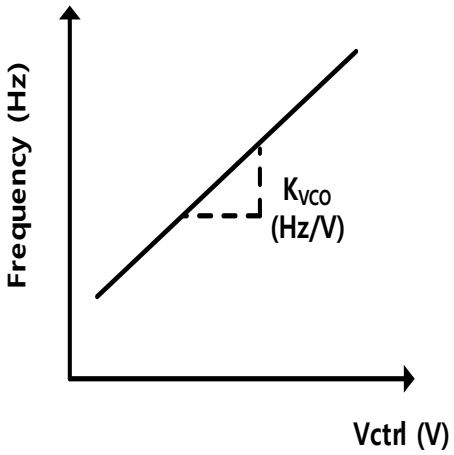


Figure 2.7 Frequency – Vctrl curve of VCO

Power consumption of VCO occupies most of the power consumption of PLL, and the primary source of PLL jitter is the phase noise of VCO, so the performance of PLL is determined by the performance of VCO. Thus, the thoughtful design of VCO is the most important when designing the PLL.

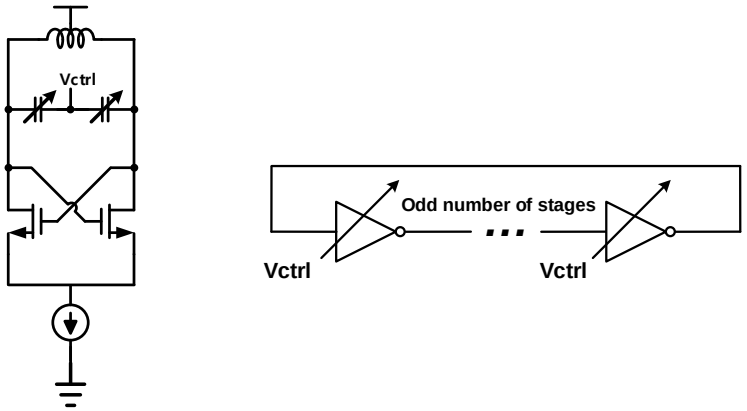
There are two typical and prevalent types of oscillator topology, ring oscillator, and LC oscillator. Characteristics of each oscillator are compared in Figure 2.8. The size of the inductor is quite large, so the size of the LC oscillator is much larger than the ring oscillator. And its tuning range is narrower than the ring oscillator. To speed up the data rate, a multi-phase clock (half rate, quarter rate, and octa rate) is used in the high-speed link, so the multi-phase generation of PLL is important. However, in the case of the LC oscillator, it isn't easy to generate multi-phase.

On the other hand, despite these disadvantages, phase noise performance and frequency of the LC oscillator are far superior to those of the ring oscillator [3]. Conventional schematics of the LC oscillator and ring oscillator are depicted in Figure

2.9. In the LC oscillator case, the capacitance of the oscillator is determined by the charge pump output, and as the capacitance is modified, the frequency of the oscillator is changed.

	Ring oscillator	LC oscillator
Size		
Phase noise		
Frequency tuning range		
Multi phase generation		
Frequency		

Figure 2.8 Characteristics comparison of ring oscillator and LC oscillator.



(a) (b)

Figure 2.9 Conventional schematics of (a) LC VCO and (b) Ring VCO.

Unlike LC VCO using the resonance of inductor and capacitor, ring-type VCO consists of multi-stages delay elements like an inverter. Thus, ring-type VCO can generate multi-phase easily. There are two representative types of ring-type VCO, capacitance tuning and current tuning. Figure 2.10 shows two kinds of schematics. The operation principle of the capacitance tuning VCO is that as the control voltage changes, the capacitance of each inverter output node is modified, and the delay of each stage is changed. Otherwise, in the current tuning case, if the current changes as the control voltage are modified, the node of each inverter output is charged or discharged at a different speed, so the frequency is changed. Specific implementation, design consideration, and the phase noise of VCO are described in Chapter 3.

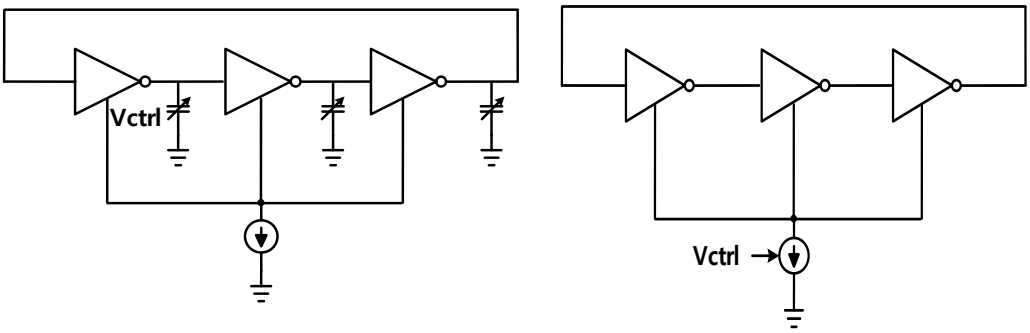


Figure 2.10 Schematics of two types ring VCO. (a) capacitance tuning, (b) current tuning

2.2.5 Frequency Divider

A frequency divider is an optional PLL block that divides the frequency of the

input clock signal. As it will be mentioned in Chapter 2.3, if the target frequency of PLL output is identical to the frequency of the reference clock, the PLL does not need the frequency divider. However, if the frequency of the input reference is lower than the target speed of the PLL, PLL should require the frequency divider, and the loop dynamics of the PLL are changed. Thus, the dividing factor of the divider is determined by the relationship between the frequency of the input reference clock and the frequency of the PLL output clock.

2.3 PLL Loop Analysis

In this chapter, based on the backgrounds mentioned in the previous chapter, s domain modeling of each block and whole loop dynamics of PLL is explained. Figure 2.10 depicts a diagram of linear model of the PLL in the s domain. In addition, modeling of each block and the open-loop transfer function are described.

The PFD contrasts the phase mismatch between the reference clock and the divided feedback clock, and this error signal is fed to the charge pump. The current of the charge pump, I_{CP}, occurs only when the up or down error signal is logic high before the reset signal. So the net transfer function of the PFD and the charge pump is $\frac{I_{CP}}{2\pi}$ (A/rad) [3].

Recalling Chapter 2.2.3, as a series connection of a resistor and a capacitor make up the loop filter, so the transfer function ($Z_{LF}(s)$) that converts the current to the Vctrl is $R + \frac{1}{sC}$ (A/V). The resistor takes the role of ensuring stability (phase margin), and the capacitor acts as an integrator tracking the frequency error [3].

The role of VCO is converting the control voltage to the frequency. However, in the linear model, because the output of the VCO is the phase, not the frequency, the transfer function of the VCO is expressed as an integrator, $\frac{K_{VCO}}{s}$. At this expression, the unit of K_{VCO} is rad/s/V.

The role of the frequency divider is dividing the frequency of PLL output, in other words, multiplying the output clock period. The input timing error of the divider appears as it is at the output of the divider. Due to the multiplied period, in the aspect of the phase, its effect seems to be reduced by the dividing factor of the frequency divider.

Thus, the transfer function of the divider can be expressed as $\frac{1}{N}$ [3]. As shown in Figure 2.11, the system of the PLL is a negative feedback system, so the transfer function of the frequency divider $\frac{1}{N}$ takes a role of feedback factor of this system.

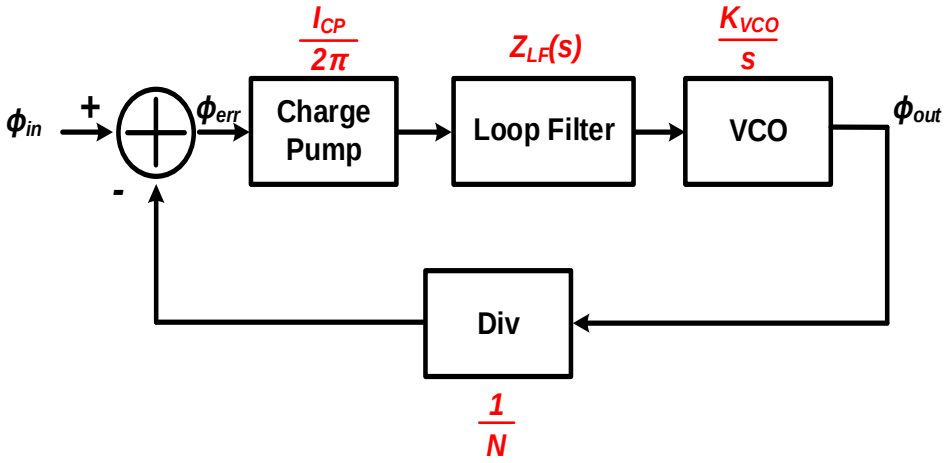


Figure 2.11 Diagram of PLL linear model in s domain.

Now, based on the transfer functions of each block, the open-loop transfer function of the system can be defined, and analysis about PLL bandwidth and stability is presented.

The open-loop transfer function of the PLL is stated by recalling the transfer functions of each block,

$$T(s) = \frac{I_{CP}\cdot\left(R+\frac{1}{sC}\right)\cdot K_{VCO}}{s\cdot 2\pi\cdot N} = \frac{I_{CP}\cdot K_{VCO}(1+sRC)}{s^2\cdot 2\pi\cdot C\cdot N}, \quad (2.1)$$

And, the closed-loop transfer function of the PLL is stated as

$$H(s) = \frac{N \cdot T(s)}{1+T(s)} = \frac{N \cdot \frac{I_{CP} \cdot K_{VCO} \cdot (1+sRC)}{s^2 \cdot 2\pi \cdot C \cdot N}}{1+\frac{I_{CP} \cdot K_{VCO} \cdot (1+sRC)}{s^2 \cdot 2\pi \cdot C \cdot N}} = N \frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}, \quad (2.2)$$

where ζ is the damping factor of the system and ω_n is the natural frequency of the system. The damping factor ζ is expressed as,

$$\zeta = \frac{\omega_n \cdot R \cdot C}{2} = \frac{\sqrt{I_{CP} \cdot K_{VCO} \cdot C} R}{2\sqrt{2\pi \cdot N}}, \quad (2.3)$$

and the natural frequency ω_n is expressed as

$$\omega_n = \sqrt{\frac{I_{CP} \cdot K_{VCO}}{2\pi \cdot C \cdot N}}. \quad (2.4)$$

A zero of the system,

$$\omega_z = \frac{1}{RC}. \quad (2.5)$$

is obtained from the transfer function, and if assuming $\omega_c \gg \omega_z$,

$$\omega_c \approx \frac{I_{CP} \cdot K_{VCO} \cdot R}{2\pi \cdot C \cdot N}, \quad (2.6)$$

where ω_c is the bandwidth of the PLL equal to the unity gain frequency of the open-loo. Through this, we can also get a phase margin

$$\text{PM} = \tan^{-1}(\omega_c \cdot R \cdot C) = \tan^{-1}(\frac{\omega_c}{\omega_z}), \quad (2.7)$$

which means the phase difference between -180 ° and the phase at the unity gain frequency [3], ω_c, and the phase margin is closely related to the stability of the system. Note that the bandwidth and the phase margin of the PLL are the most important parameters when designing the PLL. A method of deciding these parameters is discussed after explaining the jitter transfer of each block.

All the blocks of the PLL can be the jitter sources. The input jitter of the reference clock, the PFD, the charge pump, and the frequency divider is low pass filtered with the bandwidth of the PLL ω_c. On the other hand, the input jitter of the VCO is high

pass filtered with the bandwidth of the PLL ω_c [3]. Thus, if the bandwidth of the PLL is low, it rejects the noise of the reference clock, the PFD, the charge pump, and the frequency divider, but the noise of the VCO is degraded compared to the higher bandwidth case [4]. So the optimal value of the bandwidth should be determined considering the effect as mentioned above. Usually, the bandwidth of the PLL should be set around 1/10 of the reference clock frequency (equal to the update frequency of the PFD) [5].

Chapter 3

PLL with Switched Capacitor Loop Filter and Source Switched Charge Pump

3.1 Design Consideration

In this thesis, the PLL with switched capacitor loop filter and source switched charge pump is proposed. To support the high-speed interface standards, the target frequency of the PLL is 12 GHz, and it generates four phases of the clock to support the quarter rate transmitter. To remove the effect of the resistor thermal noise and retain the precision of the parameters in the loop filter, switched capacitor loop filter

is adopted. The reference spur, one of the critical factors that represent the performance of the PLL, is the spur located at the frequency as far away from the center frequency (PLL output frequency) of the spectrum by the frequency of the clock, and it is monitored at the power spectral density of the PLL clock. It is an unintended spur, so the lower reference spur level means better performance. It occurs due to the leakage current of the loop filter, up/down current mismatch of the charge pump, and the charge sharing effect [6], [7]. To reduce the reference spur and current difference of the charge pump, source switched charge pump is proposed. For the quarter rate transmitter, ring-type VCO with current tuning is used to generate four phases easily.

3.2 Proposed Architecture

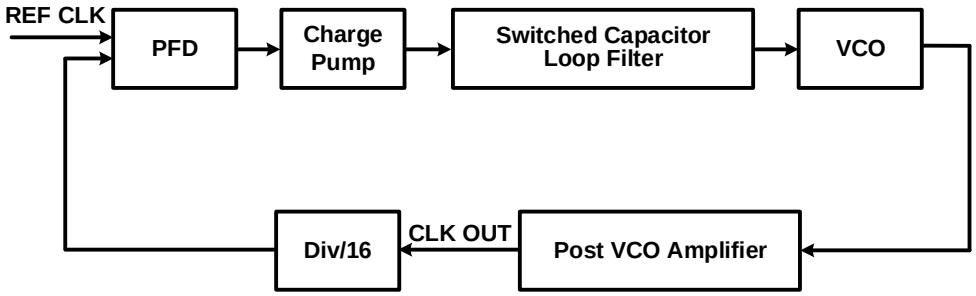


Figure 3.1 Block diagram of proposed PLL.

The block diagram of the proposed PLL with switched capacitor loop filter and source switched charge pump is depicted in Figure 3.1. The PLL comprises the PFD, the source switched charge pump, the switched capacitor loop filter, the VCO, the post VCO amplifier, and the frequency divider. As shown in Figure 3.1, the dividing factor of the divider is 16, and the target frequency of the PLL is 12GHz, so 750 MHz reference clock is the input of the PLL. As mentioned before, to support the quarter rate transmitter, the VCO generates four phases of a 12 GHz clock.

The PFD contrasts the reference clock and divided clock and delivers down or inverted up signal to the charge pump because the up signal path of the charge pump requires the inverted up, not the up signal. It is because that the input of the up path is the PMOS, not the NMOS.

The source switched charge pump changes the phase error to the current pulse.

However, because of the channel length modulation effect, as the output voltage of the charge pump is changed, the current of the charge pump may also be modified. To eliminate this effect, the source switched charge pump with reducing the mismatch of the up and down current technique is applied.

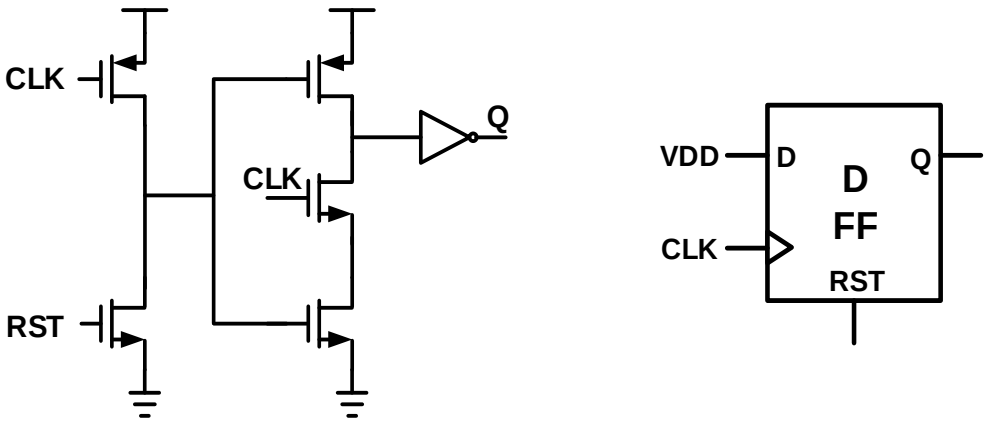
Instead of placing the resistor at the loop filter, the switched capacitor is adopted. To operate the switched capacitor, a non-overlapping clock is generated by the divided input reference clock.

To produce four phases, two-stage differential ring oscillator with current tuning is adopted. Due to its structure, the output of the VCO is not full swing (ground to the supply voltage), and its common level is not half of the supply voltage. So post VCO amplifier that consists of AC coupled resistive feedback inverter comes after the VCO. To divide the output clock by the factor of 16, four series dividers by 2 divide the output clock by 16, and it is fed to the PFD.

3.3 Circuit Implementation

3.3.1 Phase Frequency Detector

A PFD contrasts the positive edge of the input clock and the divider output, as mentioned before. A flip-flop of the PFD adopts the true single-phase clock (TSPC) flip-flop topology to reduce the delay of the clock path and avoid the issue of the intended delay of the reset path accordingly [8]. Figure 3.2 shows the adopted schematic of flip-flop for the PFD and its equivalent model of D flip-flop. When the input clock's positive edge occurs, the flip-flop output becomes high, and as the reset signal becomes high, the output is reset to low. The schematic of the PFD is drawn in Figure 3.3. The PFD generates the inverted up signal, not the up signal, because the



(a) (b)

Figure 3.2 Schematic of (a) the TSPC flip-flop for the PFD and equivalent model of D flip-flop.

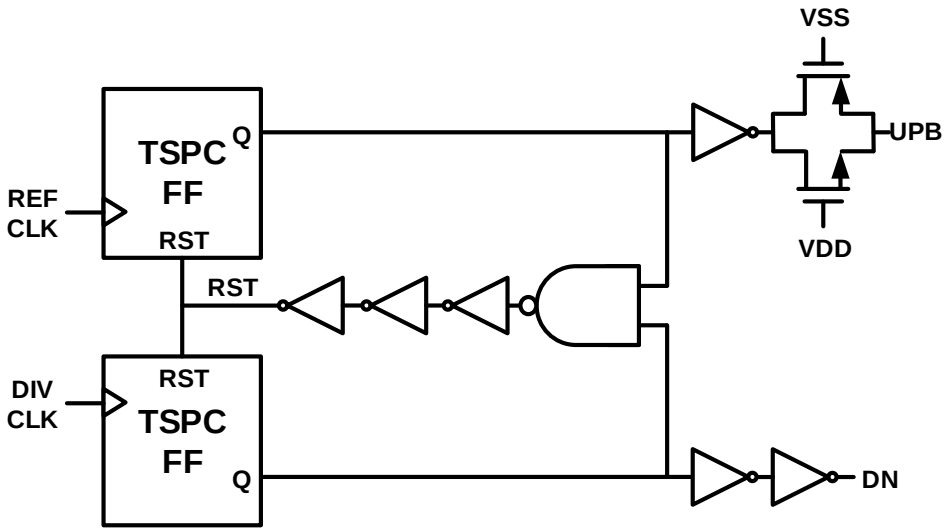
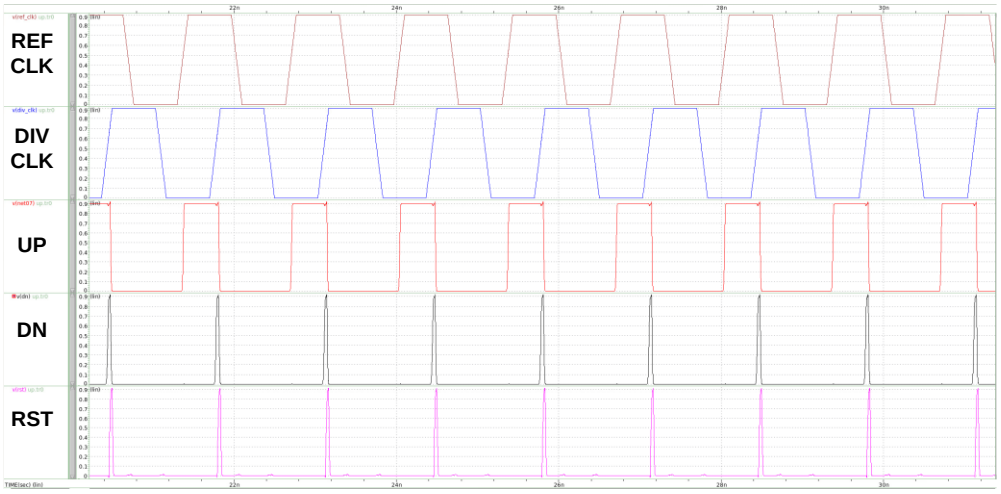


Figure 3.3 Schematic of the PFD with the TSPC FF.

source switched charge pump requires the inverted up signal. And the delay of the inverted up signal and the down signal should be equal, so the transmission gate with proper sizing is added at the inverted up signal path. The PFD simulation results are given in Figure 3.4. It represents that when the reference clock precedes, the up signal becomes high and keeps high as the reset occurs after the down signal becomes high. On the contrary, when the divided feedback clock precedes, the down signal becomes high and keeps high as the reset signal becomes high after the up signal goes high. Figure 3.5 shows the normalized net output (UP-DN) of the PFD – phase error curve. It represents the phase detection range and the locking point that the phase error becomes zero.



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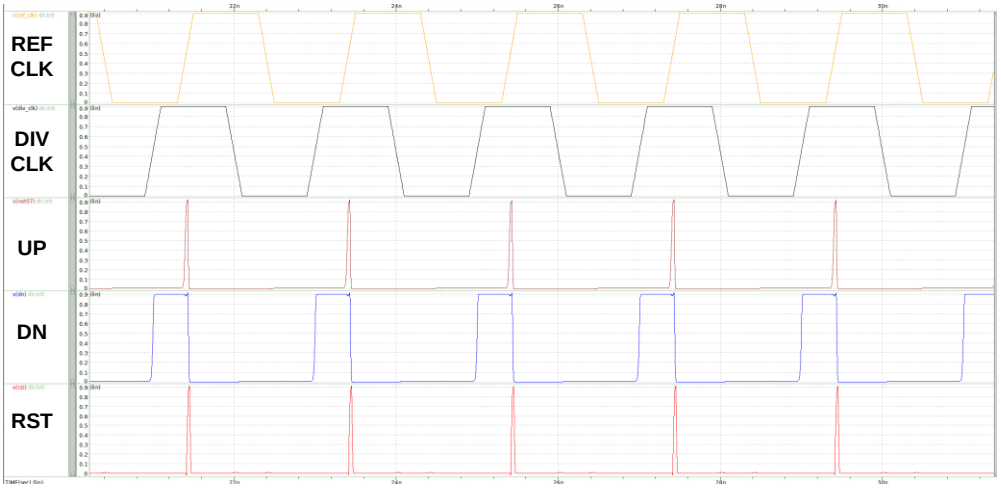


(b)

Figure 3.4 Simulation results of the PFD, (a) the reference clock leads (b) the reference clock lags.

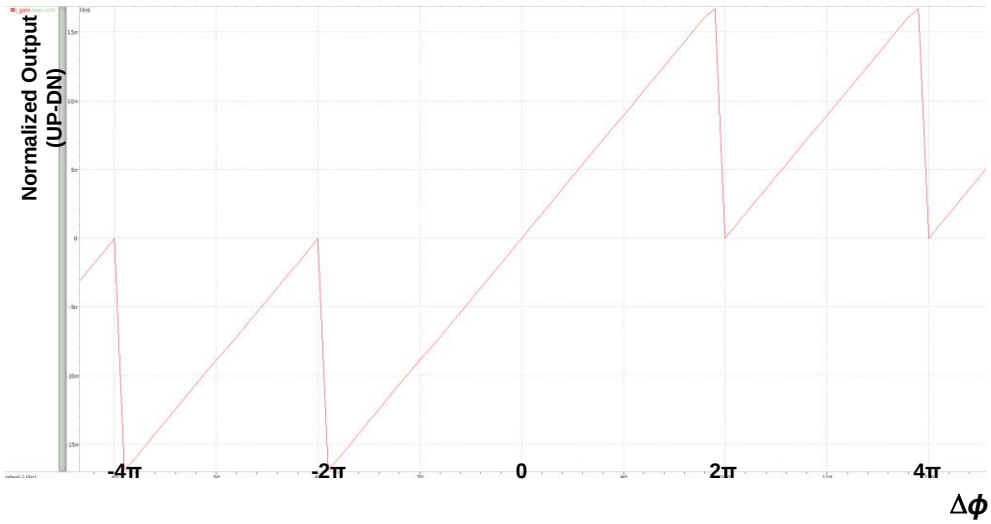


Figure 3.5 Normalized output (UP-DN) of the PFD – phase error curve.

3.3.2 Source Switched Charge Pump

The proposed source switched charge pump is shown in Figure 3.6. As mentioned before, in analog CP PLL, equivalent current between the up and down current of the charge pump is vital to reduce static phase error and reference spur level. The proposed charge pump keeps up and down current equal across broad control voltage range exploiting op-amps and replica-feedback biasing circuits [9]. Dual compensation loop using op-amps keeps up and down current equal despite the presence of the channel length modulation. This topology makes up and down current not only identical but also the constant, so that it helps reduce the reference spur level, the static phase error and is well applied to the PLL loop dynamics due to the accurate current

across the wide control voltage range. V_{integ} means the integral voltage of the switched capacitor loop filter, and it is better to input this voltage to a negative input of the op-amp to avoid the effect of voltage drop (proportional voltage) of the loop filter. The node of V_{integ} will be shown in Chapter 3.3.3. As voltage drop of the loop filter occurs every reference clock cycle due to static phase error, using integral voltage to the op-amp input improves the charge pump's performance. The current path is sliced with 3 unit slices to control the charge pump current coarsely, and an external voltage bias of the charge pump V_{n1} and another bias voltage of the amplifier can handle the current finely for adjusting loop bandwidth of the PLL [2]. As stated before, the charge pump current I_{CP} affects the loop bandwidth and the phase margin. The larger I_{CP} makes the higher bandwidth and the larger phase margin, but it degrades the noise performance related to IR noise (voltage drop at resistor occurred every reference cycle). So, the proper current should be determined considering the other parameters and the given environment, such as the power budget or the active area. Also, to obtain loop stability of the charge pump, a capacitor is added at V_{n2} and V_{p2} nodes, respectively. It plays the role of bypass capacitors at bias voltage generated from the op-amps of the feedback loop. The charge pump current across the whole voltage range is shown in Figure 3.7. It shows the current matching across 0.2 V ~ 0.7 V, and the current is almost constant within this range.

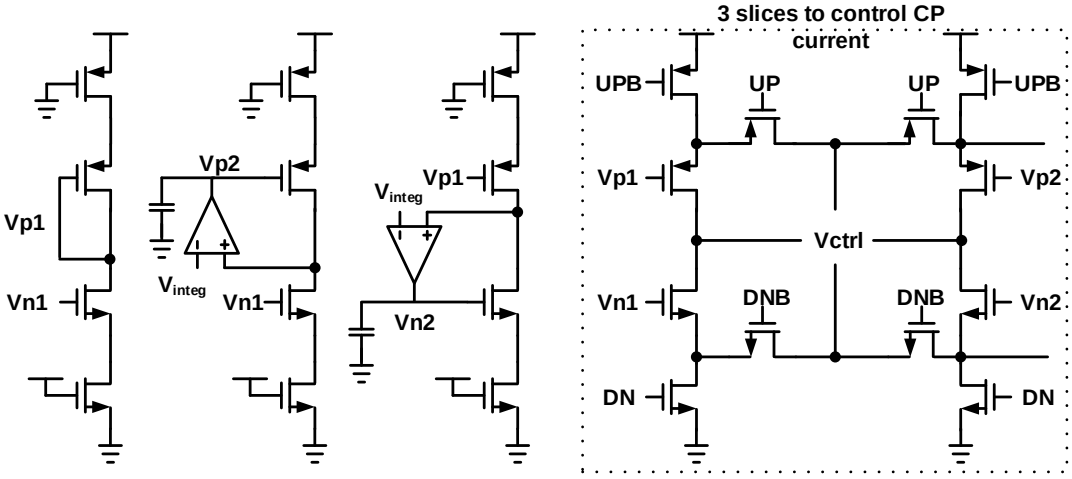


Figure 3.6 Schematic of the proposed source switched charge pump.

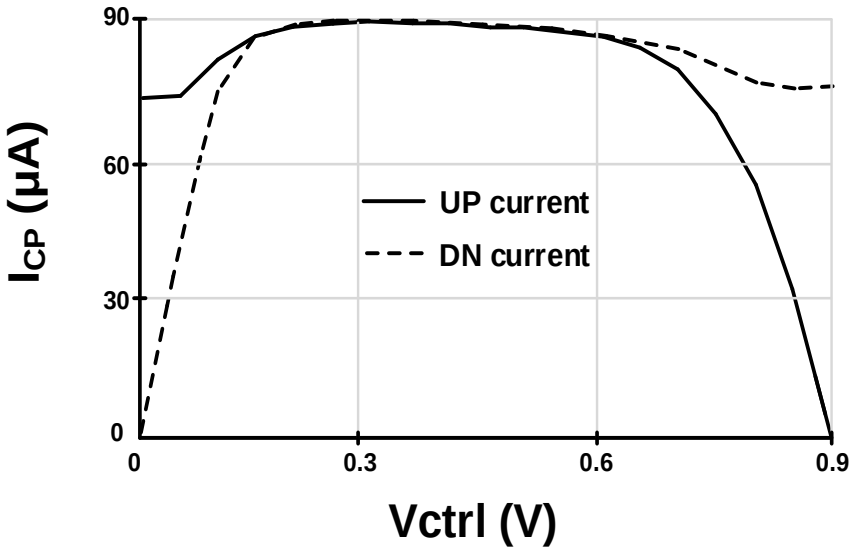


Figure 3.7 Simulation results of UP and DN current of the proposed charge pump.

However, there are additional issues to consider when designing the charge pump. One of them is the charge sharing effect. It is caused by internal nodes' parasitic capacitance at the current path of the charge pump [10]. Due to the charge sharing effect, the leakage current exits even when the current path is deactivated. It also makes the static phase offset after the PLL lock occurs and degrades the reference spur's performance. To mitigate the charge sharing effect of the charge pump, the proposed circuit exploits PMOS at the internal node of the up current path and NMOS at the internal node of the down current path [11], [12]. Each internal node is charged or discharged to the control voltage when the up or down signal is turned off. It helps reduce the charge sharing effect of the circuit by resetting the internal node to control voltage when the current path should be deactivated. It is enough to use only the NMOS or PMOS switch, not the CMOS transmission gate at the internal node, because the output voltage of the charge pump is not adjacent to the ground or VDD due to the proper operation range of the charge pump keeping equal and fixed current. Due to these switches, unintended charges of internal nodes are eliminated, so the reverse leakage current is reduced, and its settling time that takes when the time up or down signal changes from high to low and the current of the charge pump doesn’t flow is faster than the case without the switches. These simulation results are shown in Figure 3.8. It represents that the simulated down current when the down signal changes from high to low.

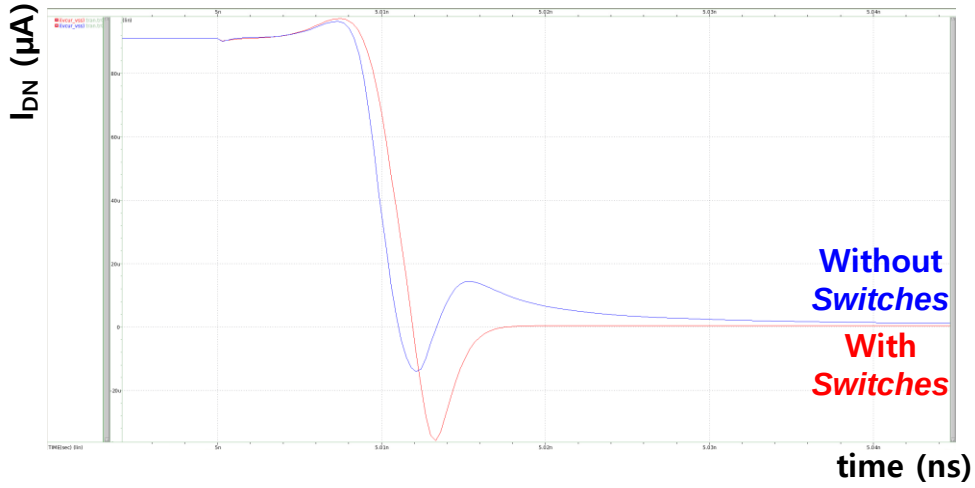


Figure 3.6 Simulated down current when down signal changes from high to low.

3.3.3 Switched Capacitor Loop Filter

The conventional loop filter of the charge pump PLL comprises of a series connection with RC. The resistor plays the role of the proportional path, and the capacitor plays the part of the integral path. The proportional path corrects the instantaneous phase error and the integral path sets the average frequency of the VCO. However, because the thermal noise of the resistor in the loop filter is the primary source of the loop filter [3], the proposed PLL adopts the switched capacitor instead of the resistor.

The schematic of the basic switched capacitor used for the resistor is depicted in Figure 3.9 (a). The equivalent model of the switched capacitor is drawn in Figure 3.9 (b). To operate the switched capacitor, a non-overlapping clock is required to ensure the proper turn on and turn off of the switches. The timing diagram of the non-overlapping clock is drawn in Figure 3.10. The principle of the switched capacitor is described as follows. First, the switch that operates with φ_1 is closed, and the switch that works with φ_2 is open. The charge stored in the capacitor is expressed as

$$Q_1 = CV_1. \tag{3.1}$$

When the switch that operates with φ_1 is open, and the switch that operates with φ_2 is closed, the charge remained in the capacitor is expressed as

$$Q_2 = CV_2. \tag{3.2}$$

The charge transferred from V_1 to V_2 is

$$Q = C(V_1 - V_2). \tag{3.3}$$

An average current that flows from V_1 to V_2 is expressed as

$$I = \frac{Q}{T} = fC(V_1 - V_2). \tag{3.3}$$

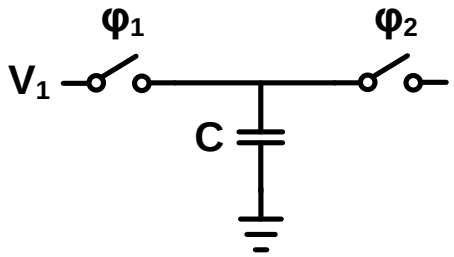
So the corresponding resistance of the switched capacitor can be expressed as

$$R_{eq} = \frac{1}{fC} = \frac{T}{C}. \tag{3.4}$$

The use of the switched capacitor helps to reduce the uncertainty of the precise resistance, so the proposed switched capacitor loop filter adopts the switched capacitor instead of the resistor.

The switched capacitor loop filter is similar to the sample and reset loop filter. And those two loop filters are adopted at the previous PLLs in [13]-[19]. However, the switched capacitor loop filter requires only a single charge pump, and it does not need the reset voltage generation [17]. So the switched capacitor loop filter has advantages

of power consumption and area efficiency compared with the sample and reset loop filter.



(a)

(b)

Figure 3.9 (a) Basic switched capacitor (b) Equivalent model of the switched capacitor.

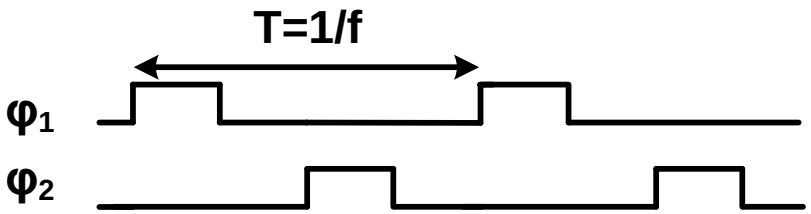


Figure 3.10 Timing diagram of the non-overlapping clock.

The schematic of the proposed switched capacitor loop filter is drawn in Figure 3.11. Its structure is the same as [14], [17], but, unlike the previous design, the proposed switched capacitor loop filter is differentiated in the waveform of the non-

overlapping clock. In [17], an instant reset occurs at the falling edge of the reference clock, but in [14], it emerges at the positive edge of the reference clock. Due to this change, the deterministic jitter and the ripple of the control voltage are reduced [17]. Unlike those structures, to reduce the possibility of overlapping non-overlapping clock and clock feedthrough issue[20], the switching clock of the switched capacitor is generated from the logic output of divided reference clock, and the waveform of the switched capacitor loop filter is shown in Figure 3.12. Also, the non-overlapping clock generation circuit is shown in Figure 3.13. Due to the low speed of the switched clock generation path, its power consumption occupies a minor part of the total power consumption. The effective resistance of the switched capacitor is expressed as

$$R_{eq} = \frac{1}{f_{ref} \cdot (C_{prop1} + C_{prop2})}, \tag{3.5}$$

where f_{ref} is the frequency of the input clock, C_{prop1} and C_{prop2} are the capacitance of proportional capacitance. So on, the PLL loop dynamics are associated with the ratio of the proportional capacitance and integral capacitance, not resistance and capacitance of the conventional RC filter independent of each other [14]. So that comparatively precise resistance can be obtained, and accurate PLL parameters can be achieved. As stated before, through adopting the switched capacitor at the loop filter, the thermal noise of the resistor that is the primary noise source of the loop filter is eliminated, and the precise and equivalent resistance can be applied regardless of the process, voltage, temperature (PVT) variation [3] ,[14].

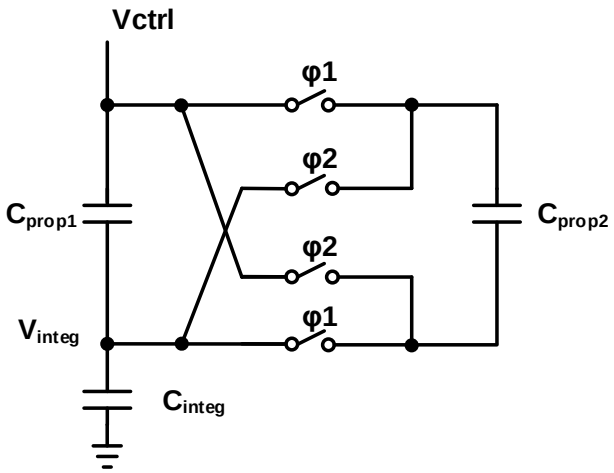


Figure 3.11 Schematic of the proposed switched capacitor loop filter.

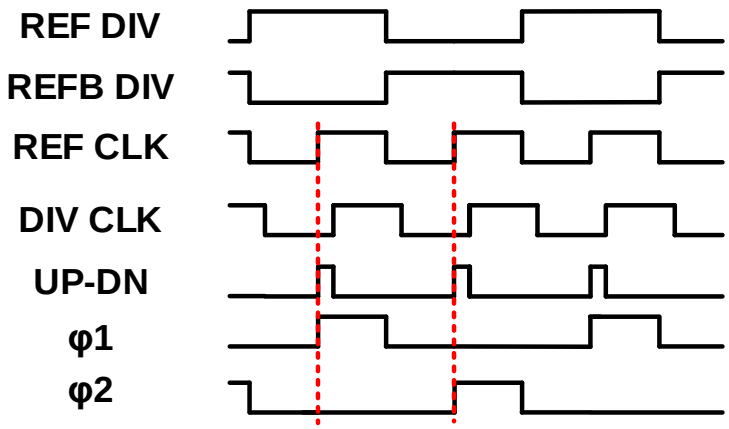


Figure 3.12 Waveform of the proposed switched capacitor loop filter.

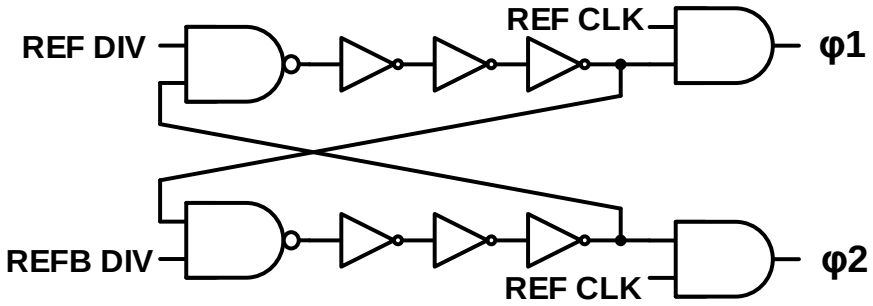


Figure 3.13 Schematic of non-overlapping clock generator.

The operation principle is as follows. When the rising edge between the input clock and the divider output is compared at the PFD, switches operated with φ_1 are closed first. Then V_{integ} and V_{ctrl} are determined according to the polarity of net current. When both switches worked with φ_1 and φ_2 are open, all the capacitors keep their charge. After the quarter of the reference clock period, switches operated with φ_2 are closed. At this time, stacked charges between proportional capacitors are reset by changing the cathode and anode of the C_{prop2}. When the connection of switches is changed, the CP event and reset of the charges simultaneously occur.

3.3.4 Voltage Controlled Oscillator

The VCO is the most crucial block of the PLL in aspects of noise performance and power dissipation. In addition to generating the target frequency of the PLL, the VCO should have appropriate the gain of the VCO, K_{VCO}, the high phase noise performance,

and the high power efficiency. The proposed VCO is shown in Figure 3.14 and implemented with two stages differential ring oscillator with current tuning [2]. To generate quadrature phases for the transmitter, the VCO is designed as above. And to cover a wide range of the VCO, the bias current source of the VCO is controlled by 4bits. Its unit differential inverter is drawn in Figure 3.15. Based on [2], a strong enough cross-coupled latch compared with the main inverter determines the proper initial condition of the oscillation node, and the latch-up effect can be avoided. Besides, the VCO that consists of this unit inverter forces the appropriate phase difference between the quadrature phases. Therefore, when designing the VCO, we should consider the frequency range and its gain. The post-layout phase noise simulation result of the VCO is shown in Figure 3.16, and the post layout transient simulation result that represents the gain of the VCO is shown in Figure 3.17. The gain of the VCO is 4.5 GHz/V (28.3 Grad/s), and the phase noise is -82.5 dBc/Hz, -107.2 dBc/Hz, -128 dBC/Hz at 1 MHz, 10 MHz, and 100 MHz offset, respectively.

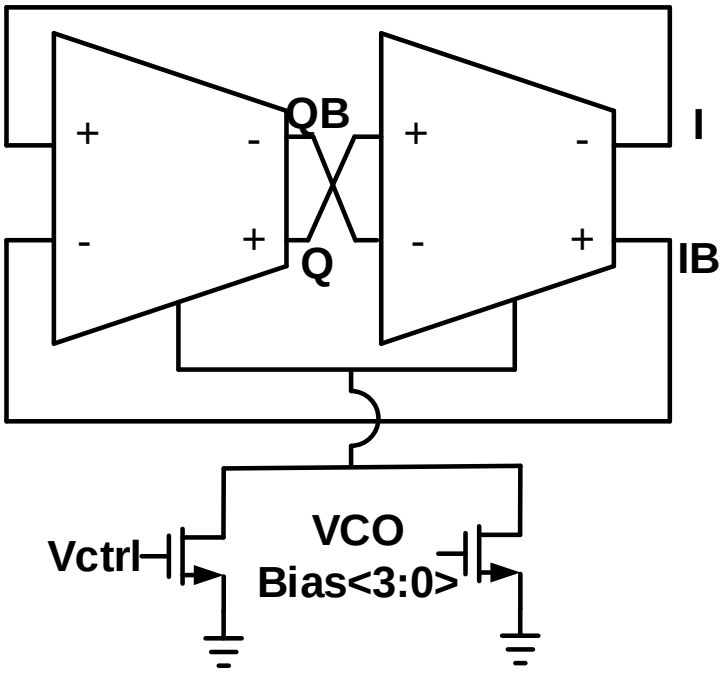


Figure 3.14 Schematic of the VCO.

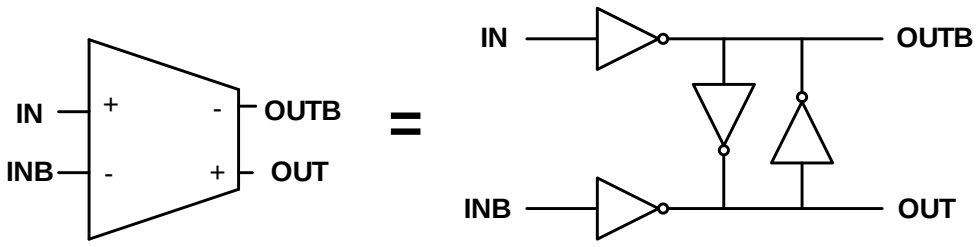


Figure 3.15 Schematic of the unit differential inverter.

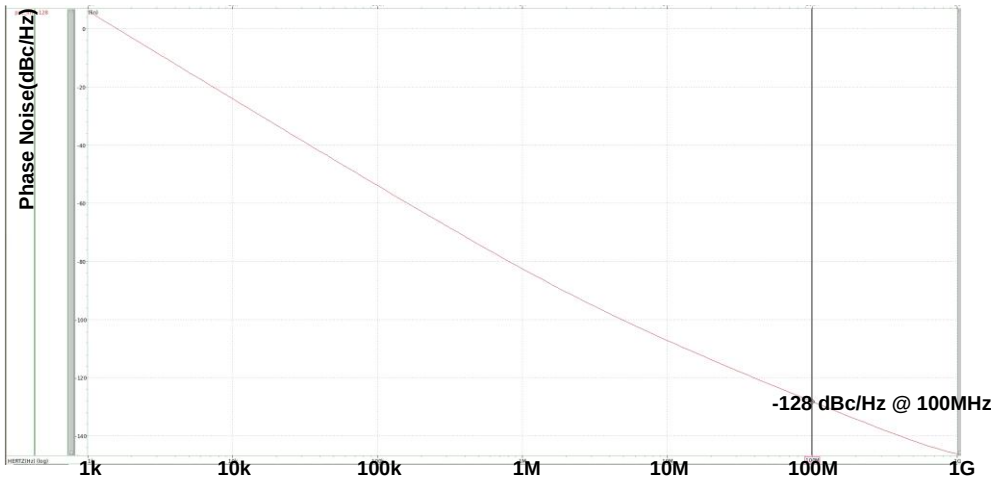


Figure 3.16 Phase noise plot of the VCO.

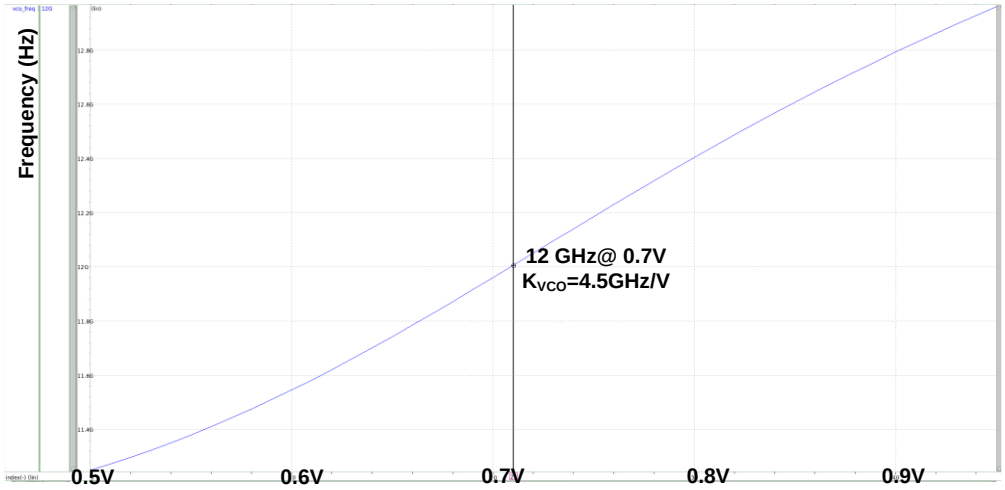


Figure 3.17 Frequency – V_{ctrl} curve of the VCO.

3.3.5 Post VCO Amplifier

Output swing of the VCO is not rail-to-rail (ground to supply voltage swing, equal to full swing), and its common level is not half of the supply voltage due to its current tuning structure. So AC coupled resistive feedback inverter is adopted to make output swing rail-to-rail and plays the role of post VCO amplifier. The schematic of the post VCO amplifier is depicted in Figure 3.18. It corrects the duty cycle of the output and makes limited swing to rail-to-rail by playing the role of a bandpass filter [2]. AC magnitude response of post-layout simulation results is represented in Figure 3.19. The magnitude of Vx, the output of the resistive feedback inverter, and the buffered clock are shown.

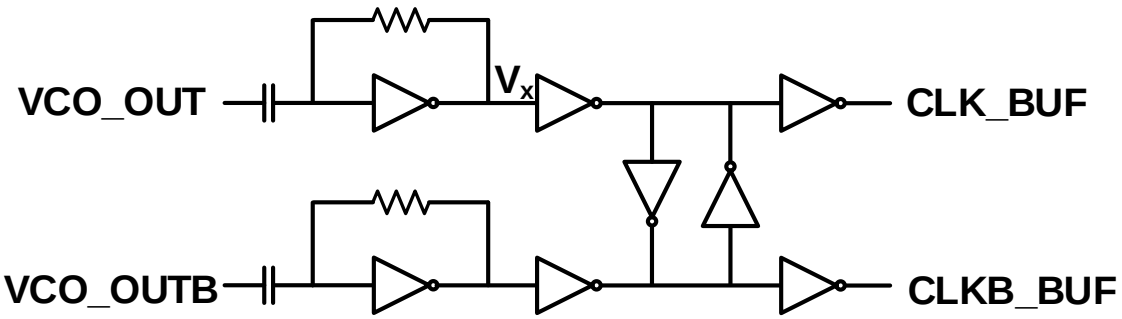


Figure 3.18 Schematic of the post VCO amplifer.

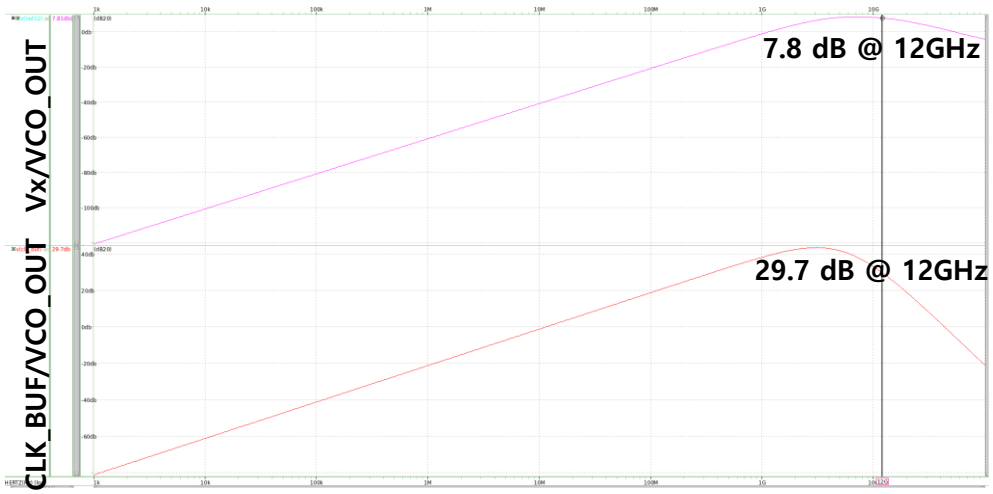
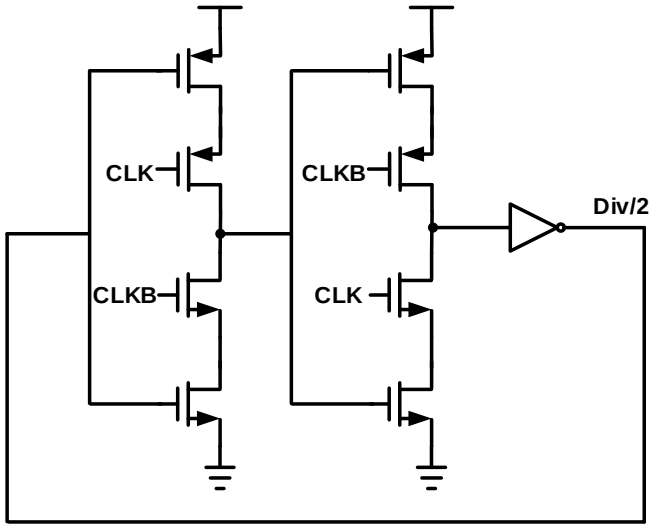


Figure 3.19 Magnitude response of the post VCO amplifier.

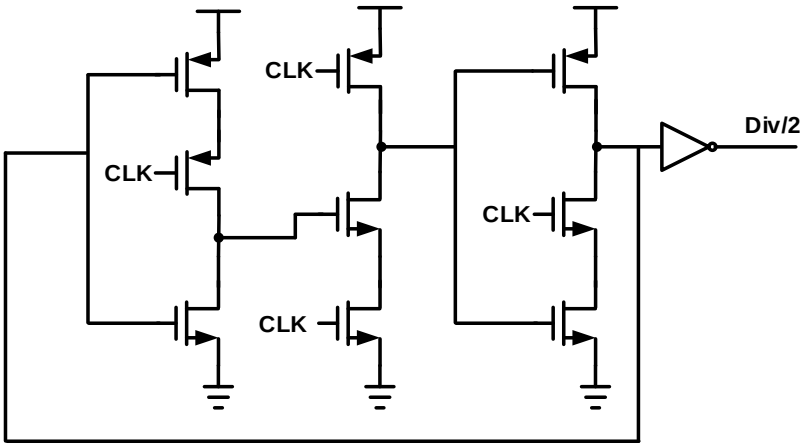
3.3.6 Frequency Divider

The target frequency of the PLL is 12 GHz, and the dividing factor of the frequency divider is 16, so the input clock frequency is determined to be 750 MHz. The frequency divider is composed of 4 stages of divider that divides the frequency of the clock by 2. The first stage of the frequency divider is implemented with a divider based on a tri-state inverter to cover the high frequency of the VCO output [2]. The second, third and fourth stage of the divider are implemented with a TSPC divider. Schematic of the divider based on a tri-state inverter and TSPC divider are shown in Figure 3.20. The divider based on a tri-state inverter works well up to 21 GHz on post layout simulation and its result is represented in Figure 3.21. Note that the frequency divider should cover higher frequency than the target frequency of the PLL because

the VCO can oscillate at a higher frequency than the target frequency of the PLL depending on the initial condition of the control voltage [3].



(a)



(b)

Figure 3.20 Schematic of (a) divider based on a tri-state inverter (b) TSPC divider.

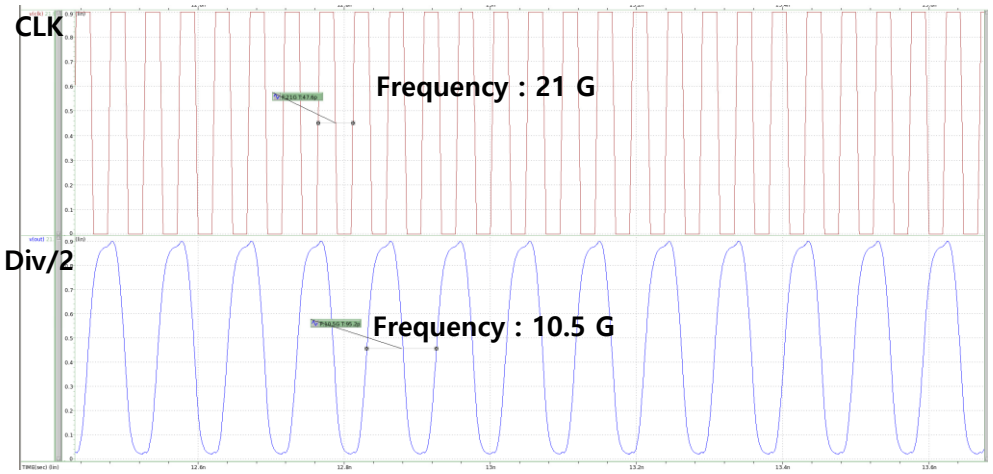


Figure 3.21 Waveform of the divider based on a tri-state inverter.

Chapter 4

Measurement Results

4.1 Chip Photomicrograph

The prototype chip is fabricated in the 40-nm CMOS process and it occupies an active area of 0.008 mm^2 (110 um x 70 um). The chip photomicrograph is depicted in Figure 4.1, and the block description of the chip is represented in Figure 4.2. The PLL consumes 6.35 mW at 12 GHz operation and 0.9 V supply voltage. The power break-down of the PLL is shown in Figure 4.3.

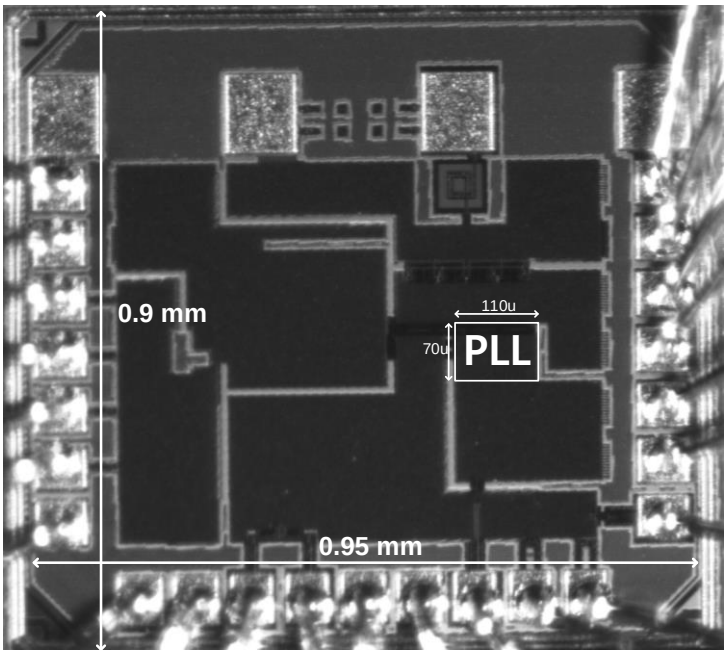
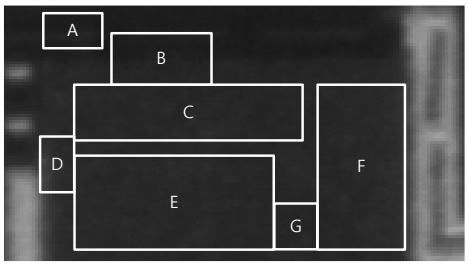


Figure 4.2 Chip photomicrograph.



	Block description
A	Divider
B	Post VCO amplifier
C	VCO
D	PFD
E	Charge pump
F	Switched capacitor loop filter
G	Non-overlapping clock generator

Figure 4.1 Block description of the chip.

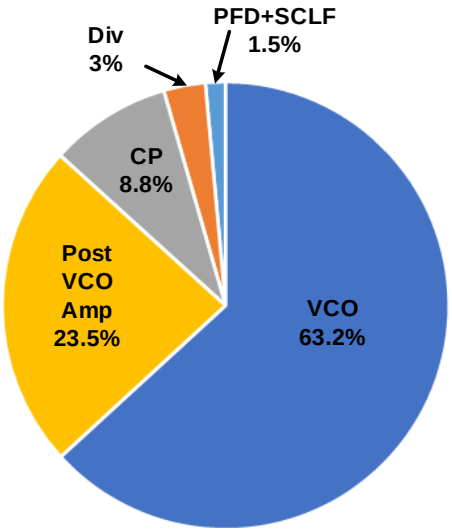


Figure 4.3 Power breakdown of the PLL.

4.2 Measurement Setup

As shown in Figure 4.4 Measurement setup, the vector signal generator (Agilent E8267D) generates a 750 MHz reference clock signal, and after passing the bias tee, a proper reference clock is delivered to the chip. For supplying the stable supply voltage, a power regulation board is used, and the generated clock signal is delivered to the spectrum analyzer (Keysight N9040B) to measure phase noise and reference spur, and the oscilloscope (Tektronix MSO 71604C) to measure peak-to-peak jitter and eye

diagram of the PLL. The PLL output is measured after divided-by-4 and PMOS open drain driver is adopted to drive the pad. The schematic of the open drain driver, pad capacitance, the inductance of wire bonding, and PCB trace capacitance are shown in Figure 4.5.

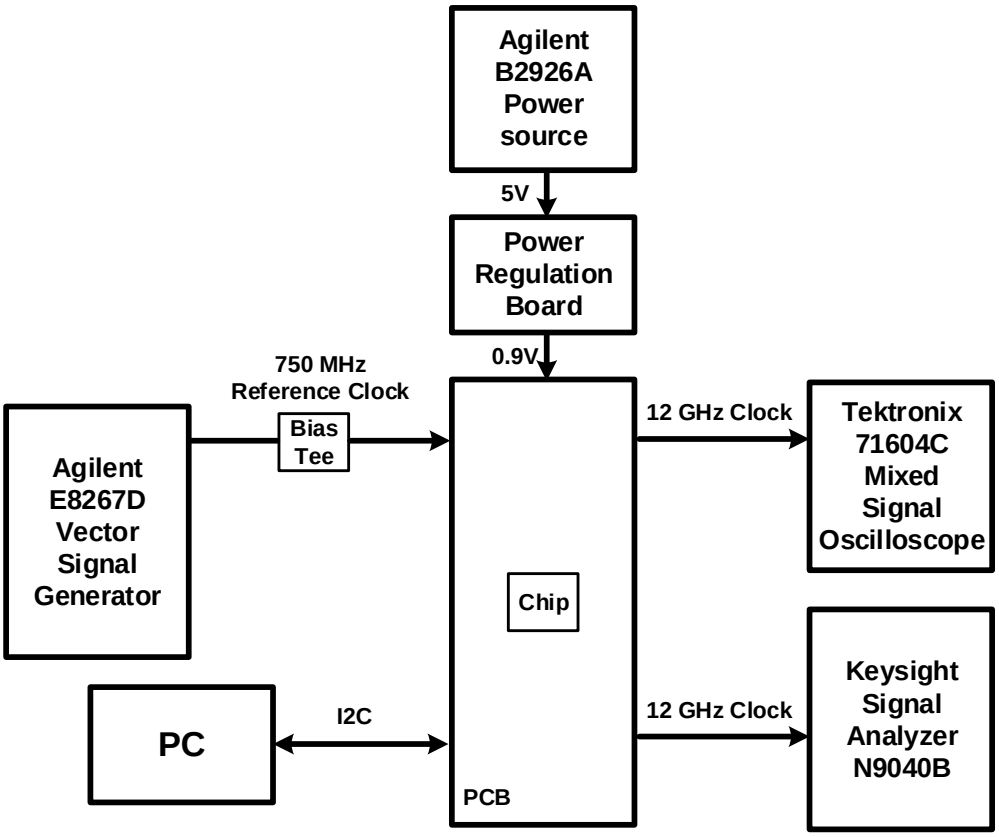


Figure 4.4 Measurement setup.

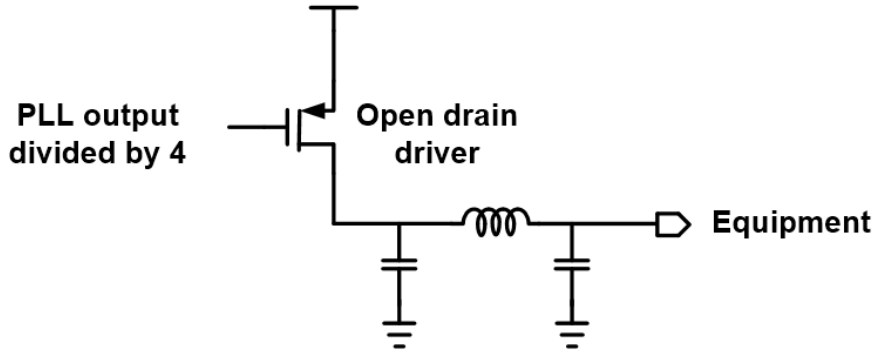


Figure 4.5 Schematic of open drain driver and modeling of pad and wire bonding.

4.3 Measured Phase Noise and Reference Spur

Figure 4.6 represents the measured phase noise of the 12 GHz clock, as mentioned before output clock is divided by 4 for measurement. Integrated RMS jitter (10 k to 100 Meg) is 244.8fs at 12 GHz. Integrated RMS jitter is one of the leading performance indicators in the PLL, and the jitter is obtained by integrating phase noise by at least three decades of range, and it should cover the loop bandwidth of the PLL [1], [21]. So the integration range of the jitter should be wide enough to measure phase noise within a large range. The measured output clock spectrum is represented in Figure 4.7. The measured reference spur level is -60.37 dBc at reference clock frequency

750 MHz. Figure 4.7 shows the jitter analysis with the oscilloscope. The peak to peak jitter is 3.61 ps, and its standard deviation is 464 fs.

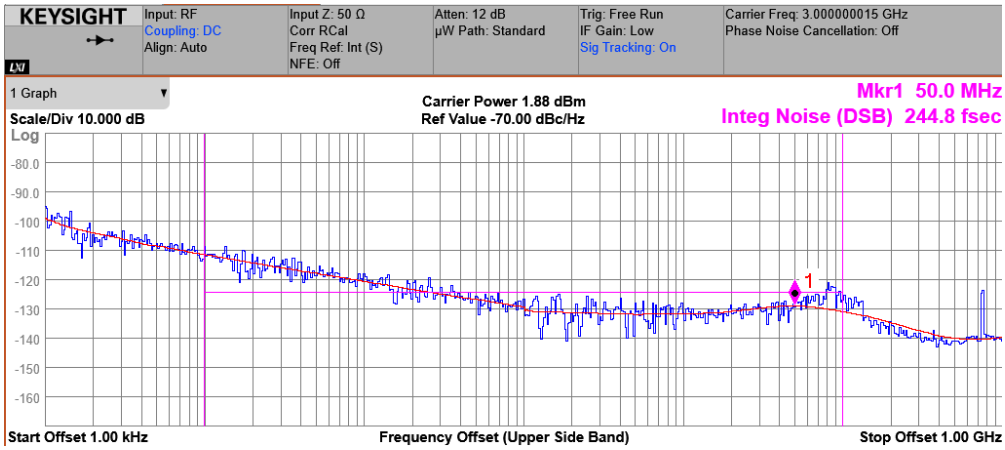


Figure 4.6 Measured phase noise of 12 GHz PLL.

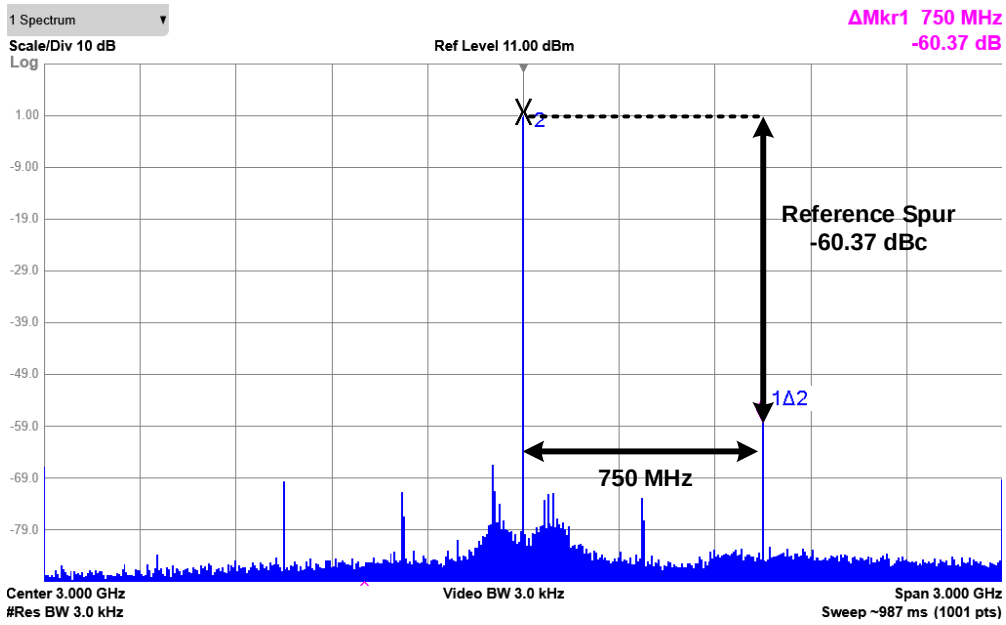


Figure 4.7 Measured output spectrum with reference spur at 750 MHz.

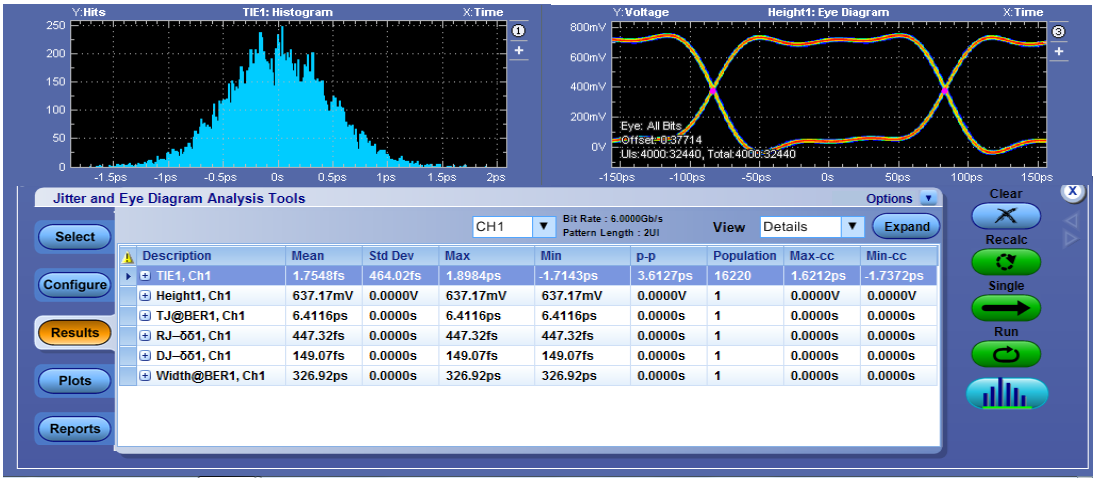


Figure 4.7 Jitter analysis of the PLL with oscilloscope.

4.4 Performance Summary

As stated in Chapter 4.1, the PLL occupies a 0.008 mm2 of active area and consumes 6.35 mW at 12 GHz PLL frequency. Integrated RMS jitter from 10 kHz to 100 MHz is 244.8 fs, so it achieves a figure-of-merit (FoM) of -244.2 dB, where the FoM is defined as

$$\mathbf{FoM}\ \ (\mathbf{dB}) = \mathbf{10} \cdot \mathbf{log}[\left(\frac{Jitter_{integrated,RMS}}{1\ s}\right)^{\mathbf{2}} \cdot \left(\frac{Power}{1\ mW}\right)] \tag{4.1}$$

in [21], and power efficiency of 0.53 (mW/GHz). Table 1 shows the performance summary and comparison of published state-of-the-art ring oscillator based PLLs. It achieves the best power efficiency among the works faster than the frequency of 10 GHz ring oscillator based PLLs and the comparable jitter and reference spur performance.

Table 4.1 PLL performance comparison

	JSSC'16 [2]	ISSCC'14 [23]	CICC'17 [24]	TCAS-II'19 [22]	**This work**
Technology(nm)	65	20	65	28	**40**
Type	CP PLL	Injection Locked CP PLL	Injection Locked Clock Multiplier	Injection Locked DPLL	**Switched Capacitor LF CP PLL**
Ref. Freq.(MHz)	625	1875	2500	468.75	**750**
Out. Freq.(GHz)	10	15	10	15	**12**
Power(mW)	7.6	46.2	59.4	17.81	**6.35**
Power Eff.(mW/GHz)	0.76	3.08	5.94	1.18	**0.53**
Integ jitter(fs) (Range)	414 (10k~100M)	268 (100k~1G)	56.1 (10k~40M)	213 (1k~40M)	**244.8 (10k~100M)**
Ref Spur(dBc)	-58.28	-48	-57.13	-43	**-60.3**
FoM(dB)	-238.8	-234.8	-247.3	-240.9	**-244.2**
Area(mm^2)	0.009	0.044	0.022	0.03	**0.008**

Chapter 5

Conclusion

This thesis proposes the low jitter PLL with switched capacitor loop filter and source switched charge pump. The switched capacitor loop filter replaces the resistor of the loop filter with the switched capacitor for accurate PLL parameters. Source switched charge pump makes the up and down current equal and constant across broad control voltage range and switch transistor is inserted at internal nodes to reduce the charge sharing effect. The prototype chip is fabricated in the 40 nm CMOS technology, and exhibits an integrated RMS jitter of 244.8fs. It consumes 6.35 mW at 12 GHz and occupies a total active area of 0.008mm^2.

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초 록

본 논문에서는 낮은 RMS jitter 와 낮은 레퍼런스 스퍼를 가지며 스위치축전기 루프 필터와 소스 스위치 전하 펌프를 이용한 PLL 을 제안한다. 제안된 PLL 은 레퍼런스 스퍼의 성능을 위해 넓은 컨트롤 전압의 범위 동안 전류의 오차를 줄여주고 전하 공유 효과를 줄여주는 하나의 조절 가능한 전하 펌프를 사용하였다. 저항의 온도, 공급 전압, 공정 변화에 따른 민감도를 낮추기 위해 스위치 축전기 루프 필터가 사용되었다. 다양한 인터페이스 표준을 지원하기 위해 제안하는 PLL 은 넓은 주파수 범위를 지원하고 낮은 RMS jitter 와 낮은 레퍼런스 스퍼를 갖는다. 스위치 축전기 루프 필터와 소스 스위치 전하 펌프의 동작 원리에 대해 분석하였다.

40 nm CMOS 공정으로 제작되었으며, 제안된 회로는 quarter-rate 송신기를 위해 4 개의 phase 를 만들어내며 750 MHz 의 레퍼런스 클락을 이용하여 12 GHz 에서 6.35 mW 의 power 를 소모하고 0.008mm^2 의 유효 면적을 차지하고 10 kHz 부터 100 MHz 까지 적분했을 때의 RMS jitter 값은 244.8fs 이다. 제안하는 PLL 은 -244.2 dB 의 FoM, 0.53 mW/GHz 의 power 효율을 달성했으며 레퍼런스 스퍼는 -60.3 dBc 이다.

주요어 : 위상 동기화 루프 (PLL), 소스 스위치 전하 펌프, 스위치 축전기 루프 필터, 전압으로 조절되는 발진기 (VCO), 위상 잡음, 레퍼런스 스퍼

학 번 : 2020-24729