Master's Thesis

Design of High-Speed Transmitter for Built-Out Self-Test of LPDDR5

LPDDR5 의 외장 자가 테스트를 위한 고속 송신기의 설계

by

Jihee Kim

February, 2022

Department of Electrical and Computer Engineering
College of Engineering
Seoul National University

Design of High-Speed Transmitter for Built-Out Self-Test of LPDDR5

지도 교수 정 덕 균

이 논문을 공학석사 학위논문으로 제출함
2022 년 2 월

서울대학교 대학원
전기·정보공학부
김 지 희

김지희의 석사 학위논문을 인준함
2022 년 2 월

위 원 장 ______________________ (인)

부위원장 ______________________ (인)

위 원 ______________________ (인)

Design of High-Speed Transmitter for Built-Out Self-Test of LPDDR5

by

Jihee Kim

A Thesis Submitted to the Department of
Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for the degree of
Master of Science
at
SEOUL NATIONAL UNIVERSITY

February, 2022

Committee in Charge:

Professor Jaeha Kim, Chairman

Professor Deog-Kyoon Jeong, Vice-Chairman

Professor Woo-Seok Choi

Abstract

To overcome the speed gap between Automatic Test Equipment (ATE) and memory, the concept of Built-out Self-test (BOST) was introduced. This thesis presents the design of a transmitter for BOST of LPDDR5. It transmits high-speed DQS and WCK to DRAM while receiving low-speed clocks from ATE. Since they don't always have clock-toggle, a digital block generates some data patterns. Also, by phase interpolators, phases of the outputs are shifted by desired.

The analog part of the transmitter consists of phase interpolators, serializers, and drivers. Phase interpolators and drivers are designed in a current mode to be resistant to supply noise. The divider of the serializer is newly proposed so that the timings of all outputs are the same. In addition, the time it takes to receive enabling signals from ATE and transmit outputs to DRAM is constant. As a result, the transmitter sends DQS and WCK with data patterns to DRAM at the desired timing.

The proposed transmitter is fabricated in a 40 nm CMOS process. 1 TX lane consumes 31.4 mW and occupies 0.06 mm^2. Measured DQS has a swing of 230 mV and an RMS jitter of 770 fs at 10 Gb/s with 50 Ω termination. And WCK has a swing of 185 mV and an RMS jitter of 894 fs at 10 Gb/s with 40 Ω termination.

Keywords : Automatic test equipment (ATE), built-out self-test (BOST), current mode driver, phase interpolator (PI), SerDes, transmitter.

Student Number : 2020-23016

Contents

ABSTRACT **I**

CONTENTS **II**

LIST OF FIGURES **IV**

LIST OF TABLES **VII**

CHAPTER 1 INTRODUCTION **1**

1.1 MOTIVATION 1

1.2 THESIS ORGANIZATION 3

CHAPTER 2 BACKGROUND ON SERIAL LINK **4**

2.1 OVERVIEW..........4

2.2 BASIS OF MEMORY INTERFACE 7

2.3 BUILDING BLOCKS..........9

2.3.1 PHASE INTERPOLATOR..........9

2.3.2 SERIALIZER..........14

2.3.3 DRIVER 18

CHAPTER 3 DESIGN OF TRANSMITTER FOR BOST **22**

3.1 DESIGN CONSIDERATION 22

3.2 OVERALL ARCHITECTURE 24

3.3 CIRCUIT IMPLEMENTATION 26

3.3.1 CLOCK PATH..........26

3.3.2 PHASE INTERPOLATOR..........29

3.3.3 SERIALIZER..........33

3.3.4 DRIVER..........41

CHAPTER 4 MEASUREMENTS RESULTS 48

4.1 DIE PHOTOMICROGRAPH..........48

4.2 MEASUREMENT SETUP..........49

4.3 MEASUREMENT RESULTS..........51

4.4 PERFORMANCE SUMMARY..........57

CHAPTER 5 CONCLUSION 59

BIBLIOGRAPHY 60

초 록 **63**

List of Figures

FIG. 2.1 (A) PARALLEL COMMUNICATION AND (B) SERIAL COMMUNICATION. 5

FIG. 2.2 ARCHITECTURE OF SERIAL LINK. 5

FIG. 2.3 TIMING DIAGRAM OF (A) FULL-RATE, (B) HALF-RATE, AND (C) QUARTER-RATE SCHEMES. 7

FIG. 2.4 DQ AND DQS. 8

FIG. 2.5 (A) DELAY LINE AND (B) PHASE INTERPOLATOR. 9

FIG. 2.6 PI OF (A) VOLTAGE MODE AND (B) CURRENT MODE. 11

FIG. 2.7 INTERPOLATION OF CLOCKS WITH (A) FAST TRANSITION AND (B) SLOW TRANSITION. 12

FIG. 2.8 (A) BOUNDARY SWITCHING AND (B) SEAMLESS BOUNDARY SWITCHING. 13

FIG. 2.9 16:1 SERIALIZER ARCHITECTURE. 14

FIG. 2.10 (A) 2:1 SERIALIZER ARCHITECTURE AND (B) TIMING DIAGRAM OF (A). 16

FIG. 2.11 FREQUENCY DIVIDER (A) ARCHITECTURE AND (B) TIMING DIAGRAM. 17

FIG. 2.12 (A) VOLTAGE MODE DRIVER AND (B) CURRENT MODE DRIVER. 18

FIG. 2.13 SOURCE-SERIES TERMINATED (SST) DRIVER. 19

FIG. 2.14 CURRENT-MODE LOGIC (CML) DRIVER. 20

FIG. 2.15 SCHEMATIC OF THE DESIGNED MAIN DRIVER. 21

FIG. 3.1 OVERALL BLOCK DIAGRAM OF TX FOR BOST CHIP. 24

FIG. 3.2 IMPLEMENTATION OF CLOCK PATH. 26

FIG. 3.3 (A) CLOCK TIMING OF 8 PHASE PI INPUTS AND (B) DELAY OF 2 ADJACENT CLOCKS. .. 28

FIG. 3.4 (A) CML PI AND AC BUFFER. (B) CML BASED PI. 30

FIG. 3.5 SIMULATION RESULTS OF PI (A) WAVEFORM, (B) PHASE ERROR, AND (C) PHASE SHIFT.

.... 31

FIG. 3.6 DNL OF THE PI (A) AT 2 GHZ AND (B) AT 5 GHZ................................ 32

FIG. 3.7 16:1 SERIALIZER STRUCTURE. 33

FIG. 3.8 2:1 SERIALIZER STRUCTURE. 34

FIG. 3.9 STRUCTURE OF DIVIDER FOR SERIALIZER. 35

FIG. 3.10 (A) PART OF DIVIDER – SHARING NODE AND (B) TIMING DIAGRAM OF (A). 37

FIG. 3.11 (A) PART OF DIVIDER – STACKED AND (B) TIMING DIAGRAM OF (A). 38

FIG. 3.12 (A) RESET SIGNAL GENERATION AND (B) TIMING DIAGRAM OF (A)........................... 39

FIG. 3.13 SERIALIZER TRANSIENT SIMULATION – PRBS-7 PATTERN. 40

FIG. 3.14 SERIALIZER TRANSIENT SIMULATION – 2 DIFFERENT INITIAL CONDITION. 40

FIG. 3.15 SCHEMATIC OF 3:1 MUX. 41

FIG. 3.16 (A) ENABLE PULSE GENERATOR BLOCK, (B) LAST STAGE 2:1 SERIALIZER FOR DATA,

.... 43

FIG. 3.17 DRIVER STRUCTURE................................ 44

FIG. 3.19 SCHEMATIC OF MAIN DRIVER. 45

FIG. 3.18 SCHEMATIC OF PRE-DRIVER. 45

FIG. 3.20 TRANSIENT SIMULATION OF DRIVER. 46

FIG. 3.21 EYE DIAGRAMS OF DRIVER OUTPUTS. (A) I_SEL=5’B11111, R_SEL=6’B111111,.. 47

FIG. 4.1 DIE PHOTOMICROGRAPH. 49

FIG. 4.2 MEASUREMENT SETUP. 50

FIG. 4.3 DQS OUTPUT WHEN DRE2 IS HIGH AT (A) 4 GB/S AND (B) 10 GB/S. 51

FIG. 4.4 DQS OUTPUT CONTROLLED BY DRE2 AT 4 GB/S. 52

FIG. 4.6 EYE-DIAGRAMS OF DQS AT (A) 4 GB/S, (B) 6 GB/S, (C) 8 GB/S, AND (D) 10 GB/S...... 53

FIG. 4.5 DQS AS A PARITY AT 4 GB/S................................ 53

FIG. 4.7 (A) CLK OUTPUT CONTROLLED BY DRE1 AT 4 GB/S AND (B) ENLARGED VIEW OF (A). 54

FIG. 4.8 EYE-DIAGRAMS OF CLK (A) AT 4 GB/S, I_SEL=5'B11111, ... 55

FIG. 4.9 EYE-DIAGRAMS OF CLK AT 10 GB/S 56

FIG. 4.10 POWER BREAKDOWN. 58

List of Tables

TABLE 2.1 COMPARISON OF CMOS STRUCTURE AND CML STRUCTURE. 11

TABLE 3.1 (A) DELAY BETWEEN 2 ADJACENT CLOCKS AND (B) DELAY OF DQS0 CLOCK AND OTHER CLOCKS. 27

TABLE 3.2 DIVIDER STATE. 36

TABLE 4.1 PERFORMANCE SUMMARY OF FIG. 4.6. 54

TABLE 4.2 PERFORMANCE SUMMARY OF FIG. 4.8. 56

TABLE 4.3 PERFORMANCE SUMMARY OF FIG. 4.9. 56

TABLE 4.4 SUPPLY VOLTAGE AND POWER BREAKDOWN OF EACH BLOCK. 57

TABLE 4.5 COMPARISON WITH OTHER TESTING CHIPS... 58

Chapter 1

Introduction

1.1 Motivation

Built-out Self-test (BOST) is a concept first proposed by Credence Systems Corporation in 1999 [1] Recently, as the operating speed of memory chips is getting faster, there is a limit to the speed of the existing Automatic Test Equipment (ATE), which is a device for testing chips. Therefore, it is necessary to remake multiple devices operating at high speed, but it takes too much cost. In addition, the number of I/O channels in ATE is limited [2] mainly target ATE in this thesis has only eight channels for signal. Therefore, it is challenging to test while giving the chip various control signals and hard to check while receiving multiple values. Accordingly, a Built-in Self-test (BIST) has been used to overcome the limitations of ATE by adding a tester circuit into a chip [3] [4] However, once a tester circuit is in a chip, other functions not designed in advance cannot be tested. Moreover, only the tester circuit except the core cannot be corrected when something goes wrong. Therefore, in this thesis, the limitations of ATE are compensated using the BOST instead of BIST.

Low power DRAM (LPDDR), which is mobile DRAM, is targeted. It is specified in JEDEC up to LPDDR5, which operates at 6.4 Gb/s. For testing it up to 10 Gb/s, DQS and WCK of 10 Gb/s are needed, but the tester's I/O can only handle up to 8 Gb/s. Therefore, a proposed BOST chip acts as a bridge that gives high-speed signals to DRAM while receiving low-speed signals from ATE. By phase-locked loop (PLL), the speed of ATE output is doubled, but BOST cannot be implemented with PLL alone because both DQS and WCK are not simple clocks. So, DQS and WCK of several patterns are generated with a digital block. In addition, to give DQS and WCK as freely as ATE, multiple modes are implemented by various control signals.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, background on transmitter in serial link and basis on memory interface are explained. Then, it presents the operation of each building block and also its advantages and disadvantages.

In Chapter 3, the transmitter for BOST of LPDDR5 is implemented. What should be considered when designing and the circuit implementation are explained. Specifically, it presents the implementation and simulation results of clock path, phase interpolator, serializer, and driver.

In Chapter 4, measurement results of the prototype chip are shown. The data patterns and eye-diagram of DQS and WCK are measured. In addition, it describes the performance of the chip like power consumption, area, jitter, and peak-to-peak voltage.

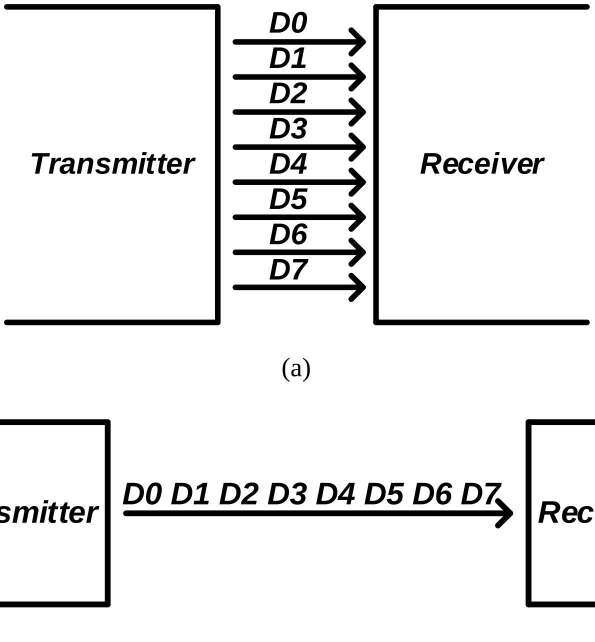
Chapter 5 summarizes the proposed work and concludes this thesis.

Chapter 2

Background on Serial Link

2.1 Overview

As a communication method between chips, there are parallel communication and serial communication (Fig. 2.1). In the case of parallel communication, multiple data is transmitted over multiple channels each, which leads to clock skews between different channels, requires a lot of physical cables, and leads to crosstalk. In addition, since it transmits multiple data, it consumes more power [5] Therefore, serial links are generally used (e.g., Ethernet, HDMI, PCE Express, SONET, and so forth). Here, serializers and deserializers are required for serial links. As shown in Fig. 2.2, when parallel data is received from SOC, it is serialized and transmitted. And the data is deserialized, so parallel data is transmitted to SOC again [6] Similarly, the digital block is used in this chip, which produces data at a slow rate because of not enough timing margin. Thus, slow parallel data is created in a digital block, and fast serialized data is transmitted to DRAM.



(b)

Fig. 2.1 (a) Parallel communication and (b) serial communication.

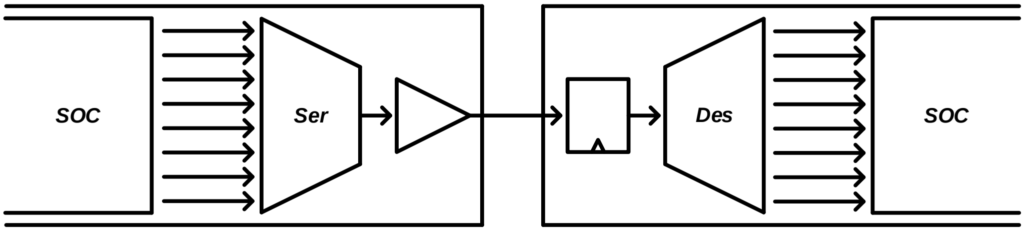
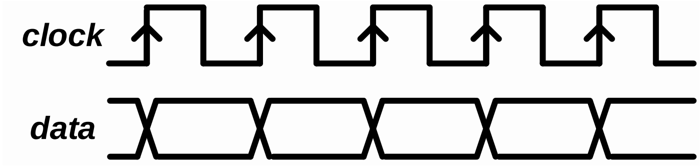
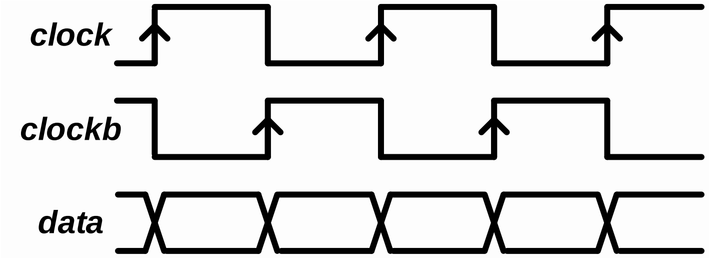


Fig. 2.2 Architecture of serial link.

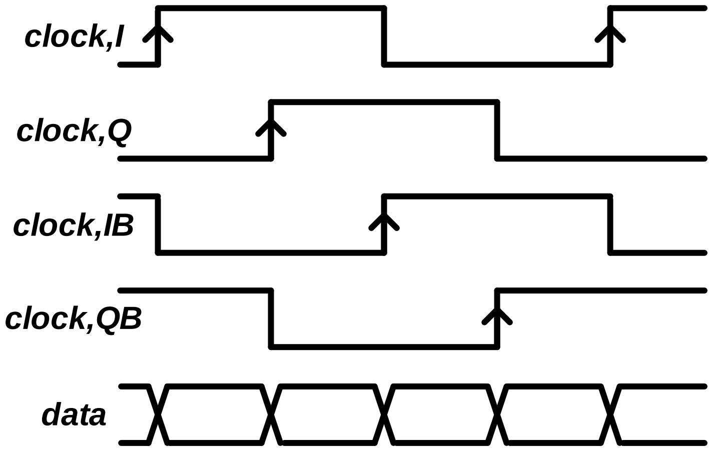
There are three primary clocking schemes; full-rate [7] half-rate [8] and quarter-rate [9] In the case of full-rate, data is aligned at the clock's rising edge, as shown in Fig. 2.3 (a). There is no big problem if the clock's duty is broken because only 1 phase clock is needed, and only the rising edge is used. However, it is difficult to make a fast clock itself, and it is also challenging to buffer and deliver it. In addition, it consumes a lot of power, and the timing margin is tight. Therefore, the half-rate scheme, as shown in Fig. 2.3 (b), is usually used. Compared to full-rate, it is advantageous for power consumption, and the burden of clocking is less. But if the clock's duty is broken, the data will have a horizontal jitter, so it should be noted. As shown in Fig. 2.3 (c), the quarter-rate scheme is used to transmit high-speed data because it uses rising edges of 4 phase low-speed clock. However, it is difficult to maintain a constant phase difference of 90 ° between 4 clocks. In this thesis, since data is not fast enough to use a quarter-rate scheme, the transmitter is implemented by the half-rate clocking scheme.



(a)



(b)



(c)

Fig. 2.3 Timing diagram of (a) full-rate, (b) half-rate, and (c) quarter-rate schemes.

2.2 Basis of Memory Interface

As the data rate of memory gradually increased, a double data rate (DDR) method was introduced instead of a single data rate (SDR). By using the clock’s falling edge as well as rising edge, the data bandwidth is doubled with the same number of I/O pins and the same speed clock. In DDR, data is called DQ, and DQS, a data strobe signal, samples DQ. At the edge of DQS, DQ should have accurate data to avoid errors in the sampled signal. Therefore, usually, DQS has a 90 ° shifted timing in DQ for sufficient set-up and hold time (Fig. 2.4) [10] Other peculiarities are that DQS toggles only when DQ has data, and it has pre-ambles and post-ambles, unlike the general clocks.

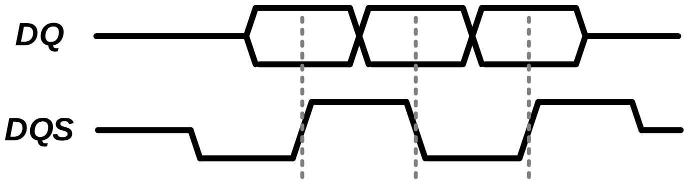


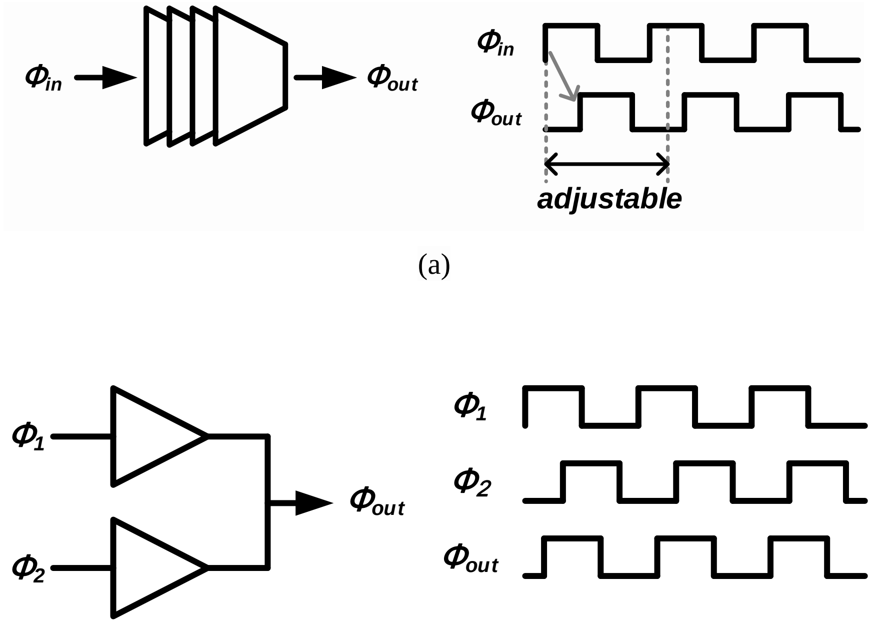
Fig. 2.4 DQ and DQS.

Therefore, these characteristics have to be considered when generating the DQS in this chip. The timing of the DQS can be adjusted fine by using phase interpolator (PI) together without using the PLL clock as it is. In addition, since DQS is not just a toggling clock, a digital block is designed to generate the corresponding pattern.

2.3 Building Blocks

2.3.1 Phase Interpolator

There are two main ways to shift the phase − a method of using a delay line (Fig. 2.5 (a)) and a method of using a phase interpolator (Fig. 2.5 (b)). If the delay line is used to introduce a time delay, the phase cannot be shifted indefinitely, and there is a limit to moving the phase. However, with the phase interpolator, phase-shift is possible with any phase between two input clocks.



(a)

(b)

Fig. 2.5 (a) Delay line and (b) phase interpolator.

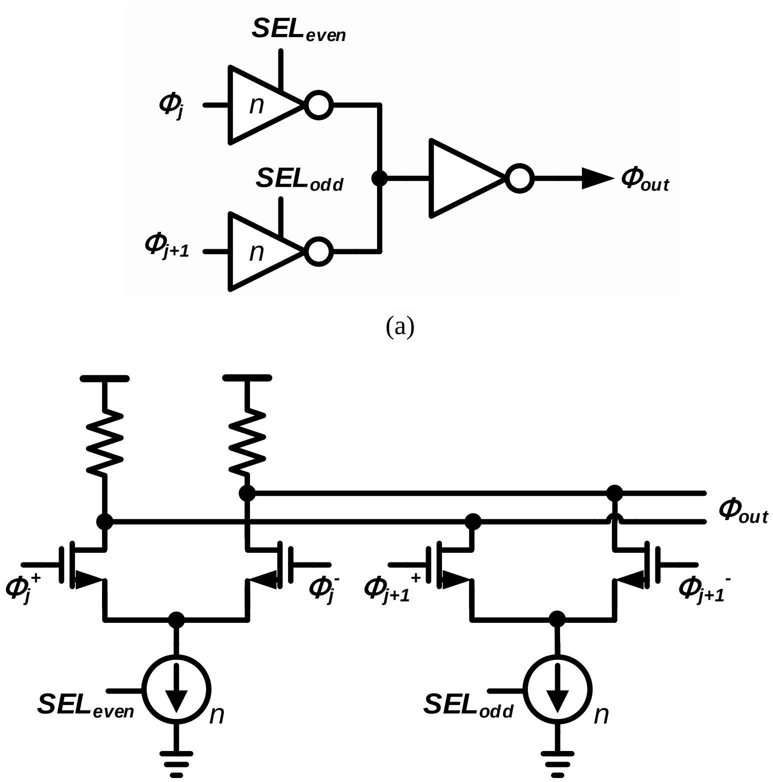
The phase interpolator mixes the phases received as input and creates a phase between them. Let's look at the principle of interpolation of two sine waves with a difference of 90 °. If the amplitude of the two waves is A and frequency is ω, they may be expressed as Equations (2.1) and (2.2). If these two have the same amplitude and frequency and are interpolated into a clock shifted by Φ, it will be expressed as Equation (2.3). If weights are given by cos Φ and sin Φ, respectively, and summed, a clock shifted by Φ can be obtained.

$$\mathrm{V_{in,I} = Asin(\omega t)} \tag{2.1}$$

$$\mathrm{V_{in,Q} = Asin\left(\omega t - \frac{\pi}{2}\right)} \tag{2.2}$$

$$\mathrm{V_{out} = Asin(\omega t - \Phi) = A}\boldsymbol{\cos\Phi} * \mathrm{V_{in,I}} + \mathrm{A}\boldsymbol{\sin\Phi} * \mathrm{V_{in,Q}} \tag{2.3}$$

There are two main structures of PI depending on whether the voltage is added or current is added. As shown in Fig. 2.6 (a), voltage mode PI is a CMOS-based structure, and the weights are controlled by adjusting the number of inverters. On the other hand, current mode PI has a current-mode logic (CML) based structure, and when the number of current sources is adjusted, the weights are controlled by the amount of current flowing (Fig. 2.6 (b)). The results of comparing structures of CMOS and CML are shown in Table 2.1 [11] In this thesis, PI is designed by a CML structure that is advantageous for supply voltage noise.



(a)

(b)

Fig. 2.6 PI of (a) voltage mode and (b) current mode.

Table 2.1 Comparison of CMOS structure and CML structure.

	CMOS	CML
Power	$C_L V_{DD}^2 f$	$V_{DD} I_{BIAS}$
Delay	**Fanout and** V_{DD}	$0.7RC_L$
Swing	V_{DD}	$I_{BIAS}R$
VDD noise	**Sensitive**	**Tolerant**

Better
Worse

The degree of phase shift is adjusted using the digital code, and each time the code is changed, a constant phase shift step is required. If all steps are consistent, it is said to be linear. In the case of interpolating two sharp clocks, there is a section with mid-level voltage, as shown in Fig. 2.7 (a), and thus the linearity decreases. On the other hand, if the rising times of the clocks are long so that all clocks are overlapped during the interpolation without such a section, it will have better linearity, as shown in Fig. 2.7 (b).

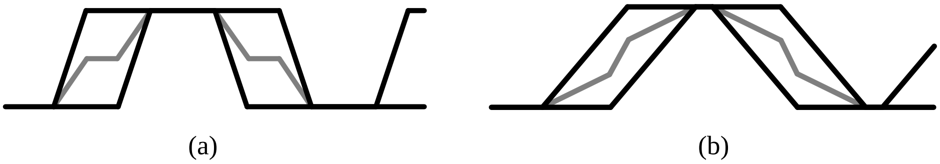


Fig. 2.7 Interpolation of clocks with (a) fast transition and (b) slow transition.

In other words, if the slew rate is intentionally controlled to be slow, the linearity of the PI may be improved. In several papers, various methods of slew rate control have been used. [12] adds a slew buffer that gives an arbitrary delay to input nodes, and [13] adjusts slew by attaching a cap to the output node. In addition, [14] improves the linearity of PI by making the slew slow by allowing input to go through a starved inverter.

Usually, PI does not receive only two clocks but receives multi-phase clocks to cover all degrees of 360. Thus, it is implemented to select two of several clocks and interpolates. When choosing two clocks, seamless boundary switching is also used as a method to improve linearity. If the two inputs are changed, as shown in Fig. 2.8 (a), it will affect the interpolation because the capacitor is not completely discharged even if all the current sources are turned off. However, as shown in Fig. 2.8 (b), seamless switching does not affect interpolation because all current sources are off in the previous code. The effect of using seamless boundary switching is shown in [15]

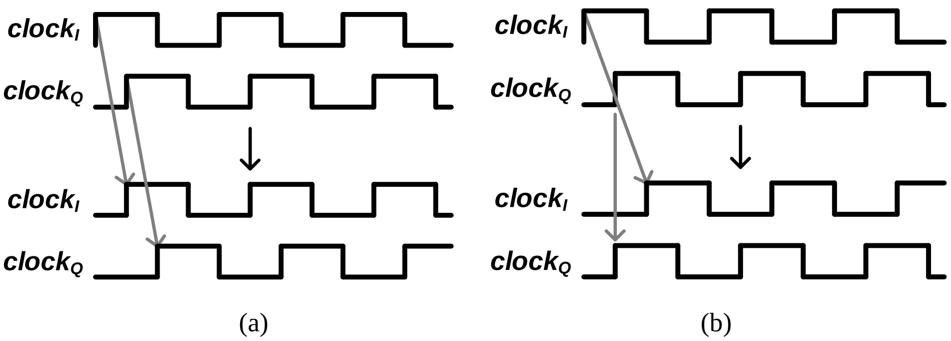


Fig. 2.8 (a) Boundary switching and (b) seamless boundary switching.

The PI of this chip is designed in a CML structure that is robust to supply noise for low jitter, and the seamless boundary switching method is used for linearity. Similarly, to avoid additional noise, the slew rate control is implemented just by lengthening the wire on the layout without adding a circuit or element separately.

2.3.2 Serializer

Serializer allows parallel data, which is multi-bits at a low-speed, to be converted to a high-speed 1-bit data stream. The typical serializer is implemented by stacking 2:1 serializers like a tree. For example, the 16:1 serializer consists of 4-stage 2:1 serializers [16] Since it is a half-rate system, in the 2:1 serializer, the input's data rate and the clock's frequency are the same, and the output has a data rate of twice. That is, as the stage progresses, the number of bits decreases, the data rate becomes faster, and fast clocks are required. Therefore, as shown in Fig. 2.9, the clock used in the last stage is divided, and the divided clocks are used in other stages.

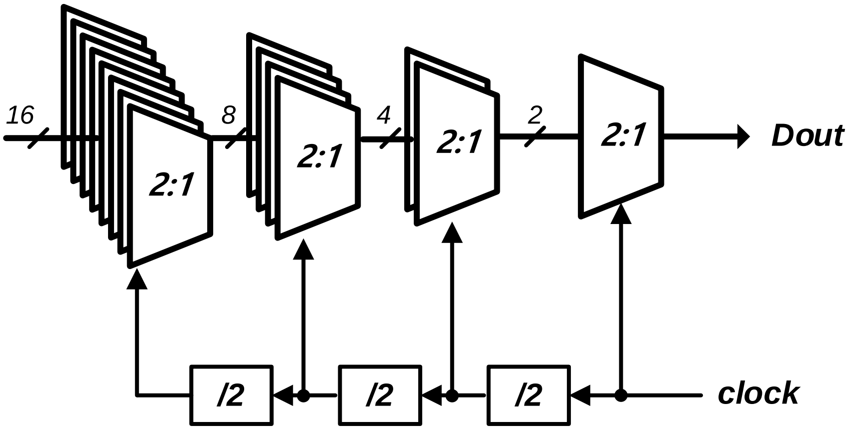
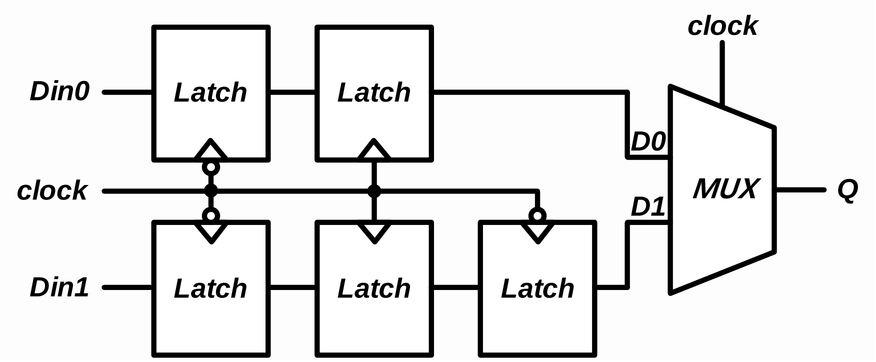
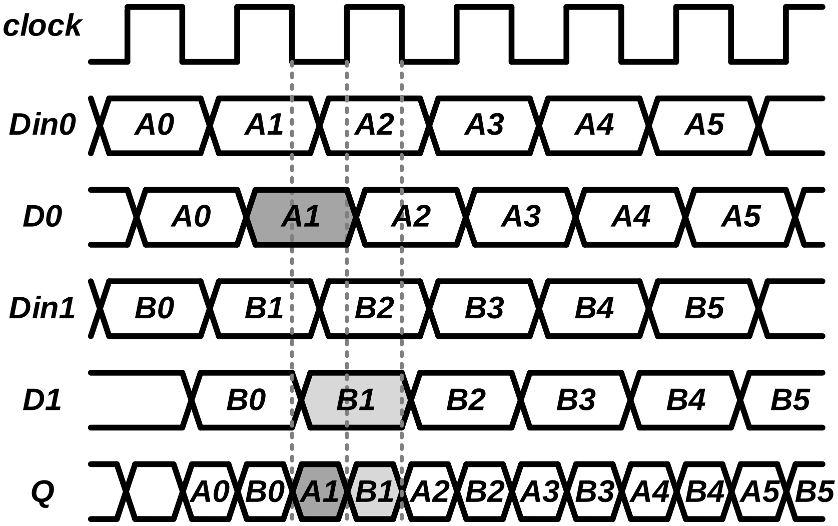


Fig. 2.9 16:1 Serializer architecture.

The structure of the 2:1 serializer is in Fig. 2.10 (a), which consists of 5 latches and a 2:1 MUX. In the last 2:1 MUX, the glitch does not occur only when the timing of D0, D1, and clock is well matched so that the timing margin is enough. For this reason, the timing between clock and D0, D1 is adjusted by five latches. As mentioned earlier, the data rate of Din0 and Din1 and the frequency of the clock are the same. Fig. 2.10 (b) shows the operation process of the 2:1 serializer. The two latches after Din0 operate as a flip-flop, and the third latch after Din1 holds the data sampled by the rising edge until the clock falls. Therefore, D0 and D1 have a phase-shifted by 90 °. After that, D0 goes to Q when the clock is 0, and D1 goes to Q when the clock is 1. At this point, D0 has data after the clock rises and after the clock-to-q delay. Thus, 2:1 MUX has a sufficient set-up time because it exports D0 when the clock falls. Likewise, D1 has data after the falling edge of the clock and after the clock-to-q delay, and the set-up time is sufficient because D1 goes out when the clock rises. Q has a double data rate compared to Din0 and Din1 because D0 and D1 appear as Q one after another when the clock is 0 and 1, respectively. The final output Q is shown in Fig. 2.10 (b).



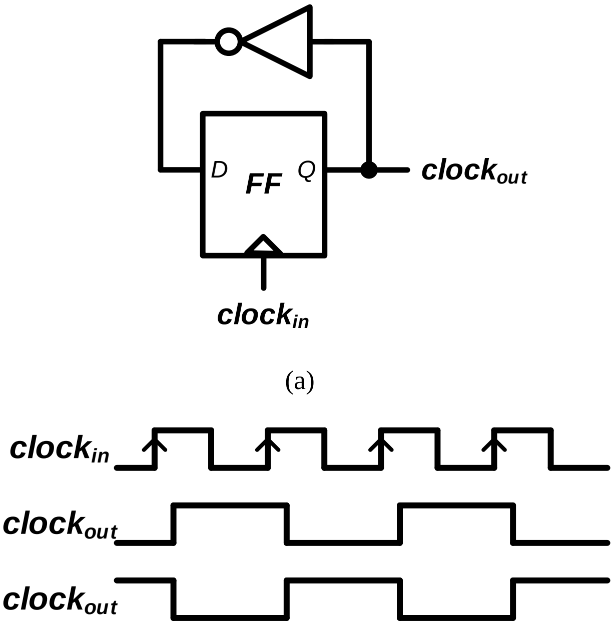
(a)



(b)

Fig. 2.10 (a) 2:1 serializer architecture and (b) timing diagram of (a).

Each stage requires a frequency divider (divide-by-2), easily implemented with a flip-flop and an inverter. The output of the flip-flop is inverted and put back into the input. As a result, the state of clock$_{out}$ turns into inversion of the previous state every time clock$_{in}$ rises (Fig. 2.11 (a)). Whenever clock$_{in}$ rises, the transition of clock$_{out}$ occurs, and as shown in Fig. 2.11(b), the period of clock$_{out}$ is twice the period of clock$_{in}$. In this case, since a feedback loop is formed, the clock$_{out}$'s phase may be changed by 180 ° depending on the initial value. In the case of a 16:1 serializer, clocks of frequency divided-by-8 are required, which can be made by stacking three dividers that divide by 2.



(a)

(b)

Fig. 2.11 Frequency divider (a) architecture and (b) timing diagram.

2.3.3 Driver

At the last stage of the transmitter, a driver drives the transmission line. There are methods of driving with a voltage source and driving with a current source, each of which is called a voltage mode driver and a current mode driver. Here, to transmit a signal through the transmission line without reflection, the source and load impedance must be the same as the characteristic impedance of the transmission line [17] Fig. 2.12 shows the drivers of two modes with impedance matching. In Fig. 2.12 (a), the voltage source has an output impedance of zero, so Z_O is connected in series. Therefore, half of the driver supply voltage is delivered to load, and it is sensitive to supply noise. On the other hand, as shown in Fig. 2.12 (b), because the output impedance of the current source is infinite, Z_O is connected in parallel. In this case, half of the current is consumed in Z_O, so a lot of power is needed to transmit a large voltage.

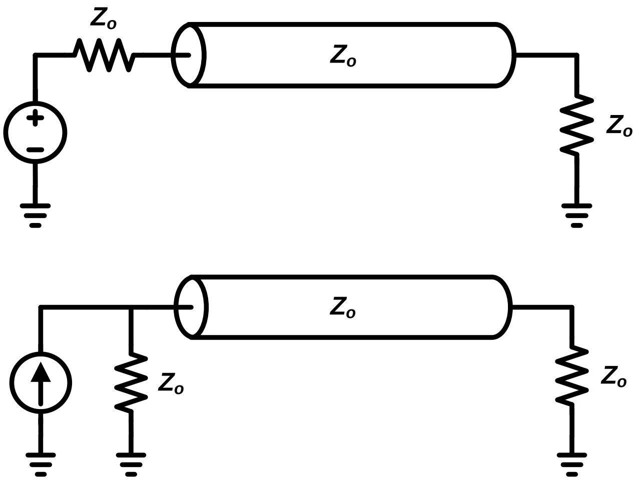


Fig. 2.12 (a) Voltage mode driver and (b) current mode driver.

Voltage mode driver is generally implemented in the source-series terminated (SST) structure of Fig. 2.13 [18] The R_S is connected to the inverter in series, and since NMOS and PMOS are in the linear region when turned on, they have a specific resistance, R_{on}. Thus, impedance matching is achieved only when $R_{on} + R_S = Z_o$. Here, the resistance of MOSFET, R_{on}, is sensitive to process, supply voltage, and temperature (PVT) variation, so reflection is likely to occur if only one SST driver is used. In addition, when a transition occurs, the operating region of the MOSFET changes, so R_{on} changes. Therefore, a way of controlling resistance using several slices or using a regulator is often used. The operation method is as follows. When V_{IN} is low, NMOS is turned on, and thus V_{OUT} goes to zero. When V_{IN} is high, PMOS is turned on, and V_{OUT} becomes $V_{DD}/2$. In other words, it is advantageous when transmitting a large swing of $V_{DD}/2$, but it is sensitive to supply noise because it delivers V_{DD} noise as it is.

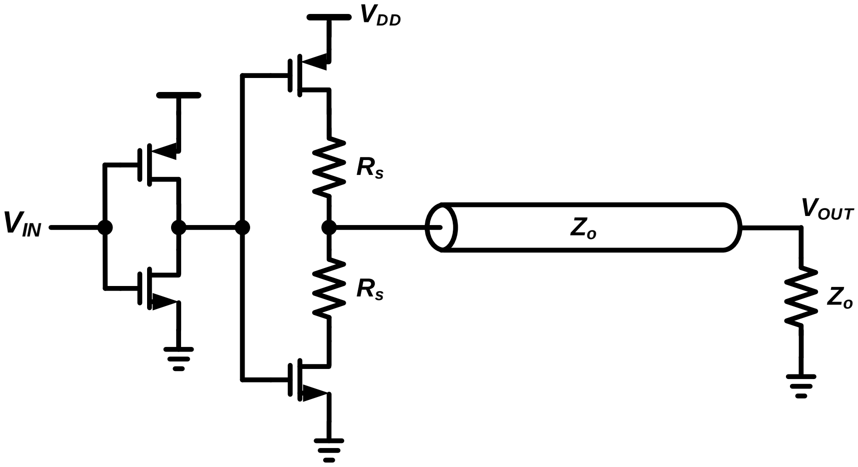


Fig. 2.13 Source-series terminated (SST) driver.

The current mode driver is implemented in a current-mode logic (CML) structure [19] Considering the situation in which the load is terminated to the ground, it can be shown as Fig. 2.14. In this case, the MOSFET acting as the current source or the PMOS for pull-up is in the saturation region, so they have a sufficiently large resistance. Thus, the resistance seen at the driver is approximated by the Z_O connected below. It is advantageous for impedance matching compared to voltage mode because impedance matching is achieved with a passive resistor that is less sensitive to PVT variation. When PMOS is turned off, the resistor connected to the ground pulls-down and V_{OUT} goes to zero, and when PMOS is turned on, pulling-up occurs and V_{OUT} becomes $I_SZ_O/2$. For differential signaling, V_{OUT} has the swing of I_SZ_O. Because it does not require full-swing, it is advantageous when transmitting high-speed signals and is robust to supply noise compared to voltage mode. However, power consumption is significant because current also flows through Z_O connected to CML.

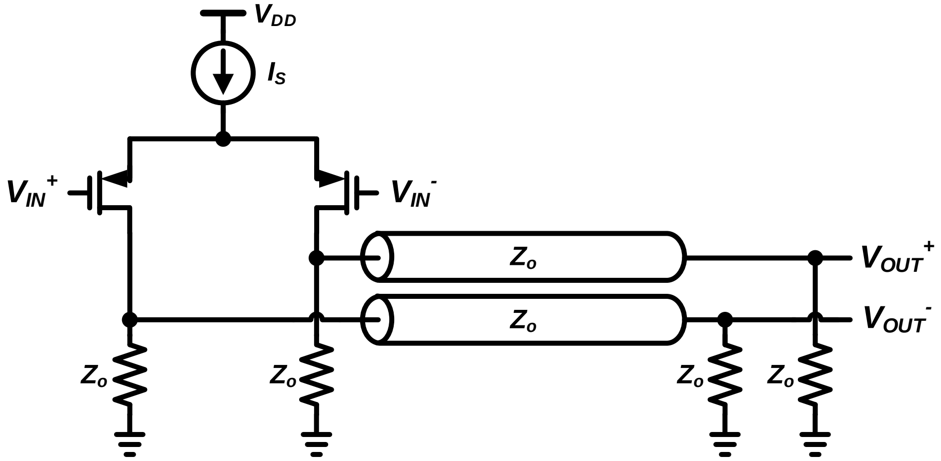


Fig. 2.14 Current-mode logic (CML) driver.

A current mode driver that is less sensitive to supply noise and advantageous for impedance matching is used for the transmitter of this chip. One of the reasons for the selection is that LPDDR has a smaller voltage swing than other DRAMs. However, it does not always transmit differential signals, so the CML driver is not available. Therefore, as shown in Fig. 2.15, a single-ended driver is designed using only one side of the CML driver. Here, the current is adjusted by a current mirror to control the voltage swing.

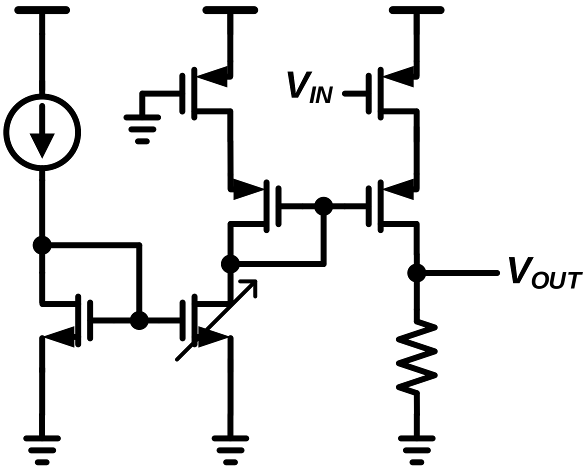


Fig. 2.15 Schematic of the designed main driver.

Chapter 3

Design of Transmitter for BOST

3.1 Design consideration

Since this BOST chip provides DQS and WCK to LPDDR5, the termination, output voltage, and the like are determined by the spec of LPDDR5. In LPDDR, the I/O is terminated to the ground, and the output resistance of the buffer chip’s transmitter should be controlled to 40/ 48/ 60/ 80/ 120 Ω. Therefore, the current mode driver using PMOS is selected, and six 240 Ωs connected in parallel are used as pull-down resistors. JEDEC states that LPDDR5 is operable at a data rate of up to 6.4 Gb/s. But because the chip is for testing, it is designed to transmit outputs at a data rate of up to 10 Gb/s.

The DQS and the WCK should be able to perform operations different from those of the general clocks. Because DQS is sometimes used as a parity, it may be a clock toggling, but it can also be random data. It also has pre-ambles and post-ambles, even if a typical clock is just sent out. Thus, it cannot be implemented with a simple PLL, and complex logic is required. Through digital synthesis, it is possible to transmit the desired DQS signal. Digital block cannot operate at high speed due to timing margin, so 16-bit parallel data is generated in the digital block and serialized by the 16:1 serializer. Although WCK is a toggle clock, it has static data for a while, and pre-amble1 and pre-amble2 that toggle in the quarter and half of the WCK period, respectively. Therefore, like DQS, it is difficult to implement only with PLL, so the digital block generates the pattern. 2 DQS transmitter lanes and 2 WCK transmitter lanes are designed, respectively. For the same timing of 4 TX lanes, the clock path is designed and routed the same.

Digital block makes a signal only when the enable signal is high so that the timing at which DQS and WCK are generated and transmitted can be adjusted. Although not described in this thesis, DQS is also connected to the receiver of this chip. Therefore, the chip should operate as a transmitter when the enable signal is high and as a receiver when it is low. Thus, the driver is designed to be enabled or disabled according to that. In addition, each lane normally transmits a differential signal, but a single-ended driver is used, allowing only one side to send a fix-high or fix-low signal for testing.

3.2 Overall Architecture

The entire block diagram of the proposed transmitter is shown in Fig. 3.1. The enable signals DRE1 and DRE2 are received from ATE. Then WCK and DQS are created according to the timing of the DREs, respectively. And DQS0, DQS1, WCK0, and WCK1 are exported from 4 transmitter lanes.

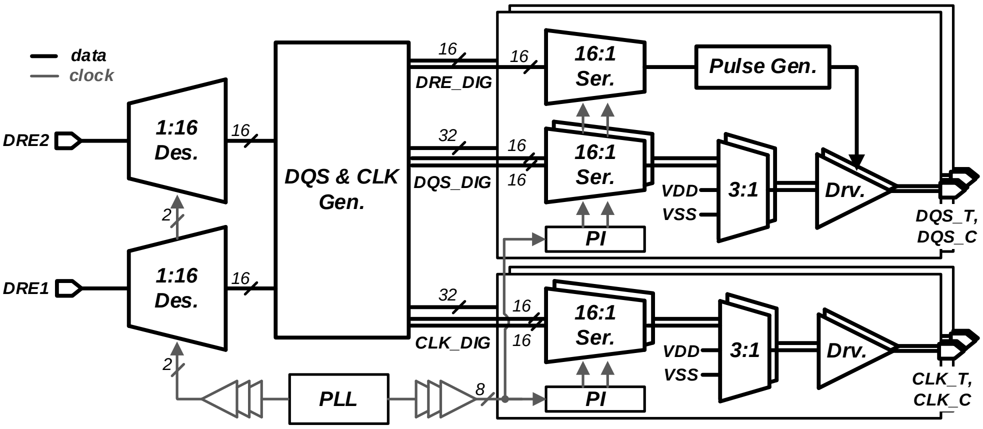


Fig. 3.1 Overall block diagram of TX for BOST chip.

Digital block operates at 1/16 of the TX in/output data rate. Thus, the 1:16 deserializers are placed first so that DRE1 and DRE2, used as digital inputs, also have a 1/16 data rate. The digital block, DQS & WCK generator, receives DRE1_DIG and DRE2_DIG of 16-bit and generates 16-bit differential WCK_DIG and DQS_DIG when DRE1_DIG and DRE2_DIG are high. Also, it converts DRE2_DIG to DRE_DIG that has the same timing as DQS_DIG. Then, DRE_DIG and DQS_DIG are delivered to 2 TX lanes of DQS, and only WCK_DIG is transferred to 2 TX lanes of WCK because it does not need an enable signal of the driver.

In the transmitter of DQS, when DRE is high, the driver is enabled, and DQS0_T, DQS0_C, DQS1_T, and DQS1_C are transmitted to DRAM. The 16-bit differential DQS_DIG signal from the digital block is serialized through 2 serializers, respectively, and goes through 2 single-ended drivers. DRE_DIG, a signal for enabling driver, also goes through a serializer because it is 16-bit parallel data. There is a 3:1 MUX between the serializer and the driver. It is to satisfy not only the normal mode in which DQS data is transmitted but also the mode in which always high or low data is transmitted. The MUX selection signal is determined by an I2C register setting, and one of the DQS, VDD, and VSS is delivered to the driver according to the selection. Driver does not always operate and is enabled only when the enable signal is high. When it is low, the driver is disabled, so only RX is connected to the output pad. The enable signal is generated by modulation of the DRE. If DRE and DQS have precisely the same timing, a glitch will occur because of the time driver turned on. Therefore, DRE is stretched back and forth through the pulse generator. And it is modulated one more time so that the driver may always be enabled regardless of the DRE, in fix-high or fix-low mode. In this way, the DQS is transmitted to the DRAM when DRE2 is high.

The transmitter for WCK always delivers WCK0_T, WCK0_C, WCK1_T, and WCK1_C to DRAM regardless of the DRE. Similarly, 16-bit differential digital output WCK_DIG passes through 2 serializers and 2 drivers. Since WCK also requires fix-high and fix-low mode, 3:1 MUX is placed between a serializer and a driver. The drivers are always turned on without receiving an enable signal, unlike the drivers of DQS.

3.3 Circuit Implementation

3.3.1 Clock Path

This chapter shows how the chip gets a reference clock from ATE and delivers clocks to each block. Since the data rate must be transferred to DRAM twice, the reference clock frequency is doubled through PLL. This PLL clock is delivered to the 4 TX lanes and deserializers for DREs (Fig. 3.2). The clock tree is configured with the same number of buffers and the same clock path length so that all DQS and WCK can be transmitted to the DRAM at the same timing. In front of each TX, there is a phase interpolator that interpolates the 8 phase clocks. The 8 phase clocks are created directly through the differential ring oscillator of PLL, and phase differences of each clock are made as identical as possible.

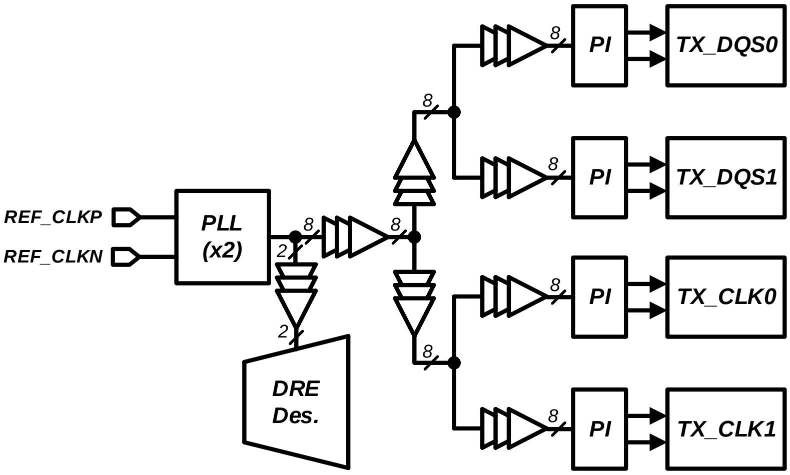


Fig. 3.2 Implementation of clock path.

Fig. 3.3 and Table. 3.1 show the simulation results of whether the phase difference of the 8 phase clocks is constant and whether the timing of clocks delivered to each TX is identical at a maximum frequency of 5 GHz. In Fig. 3.3 (a), Clock[0] to Clock[7] represent 8 phase clocks delivered to TX of DQS0, respectively. The delay between each clock is shown in Fig. 3.3 (b) and Table 3.1 (a). It can be seen that it has almost a constant value without much difference from the ideal delay indicated by the dotted line. The last waveform of Fig. 3.3 (a) combines all four clocks delivered to each TX. Clock timings are almost the same, so four waveforms are practically overlapped. And Table 3.1 (b) shows that the differences in clocks are very minute within 0.5 ps.

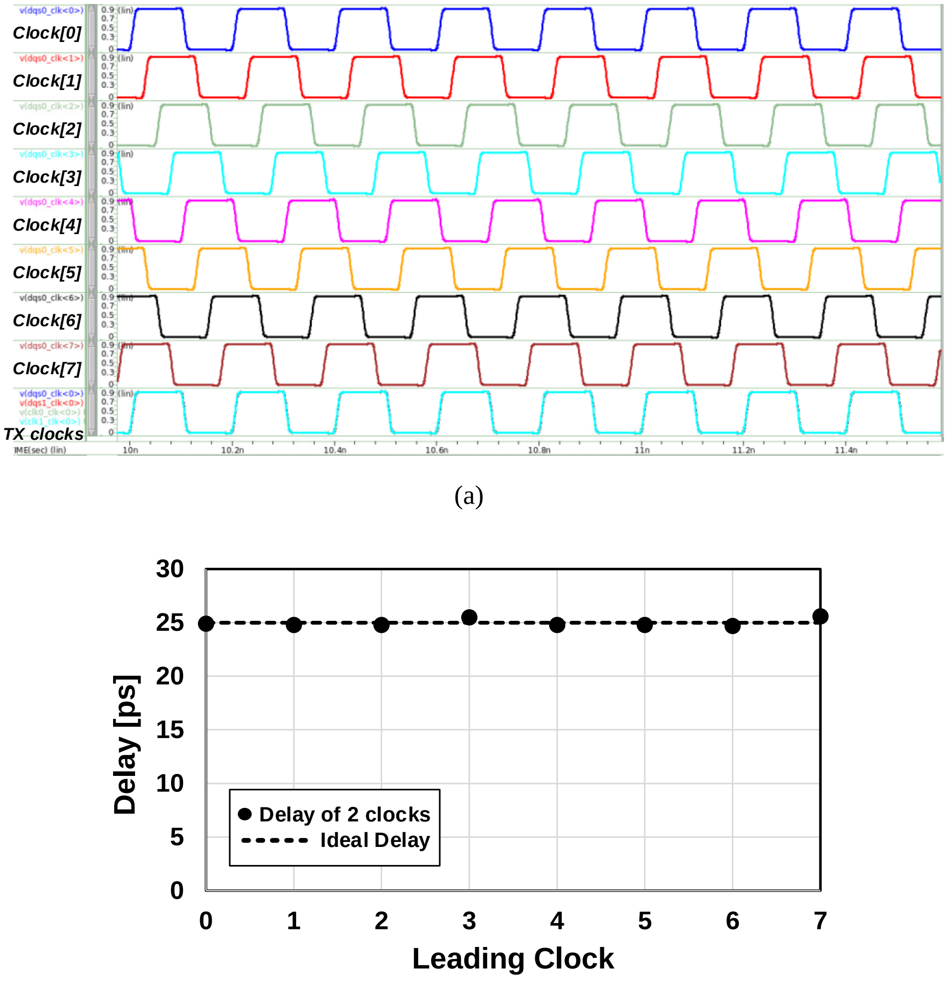
Table 3.1 (a) Delay between 2 adjacent clocks and (b) delay of DQS0 clock and other clocks.

Leading clock	**[0]**	**[1]**	**[2]**	**[3]**	**[4]**	**[5]**	**[6]**	**[7]**
Delay [ps]	24.9	24.8	24.8	25.5	24.8	24.8	24.7	25.6

(a)

Clocks for	**DQS0**	**DQS1**	**WCK0**	**WCK1**
Delay [fs]	0	71.2	44	513

(b)



(a)

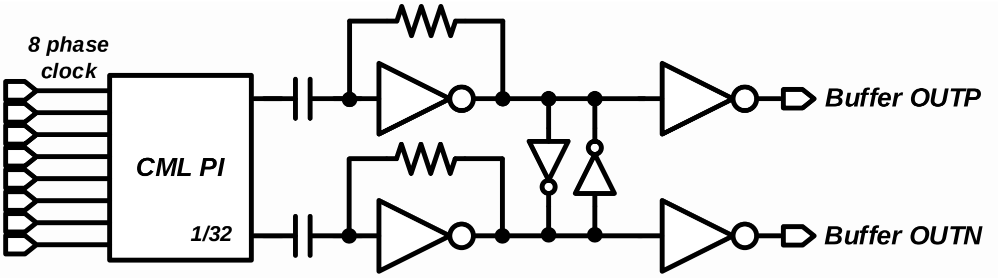
(b)

Fig. 3.3 (a) Clock timing of 8 phase PI inputs and (b) delay of 2 adjacent clocks.

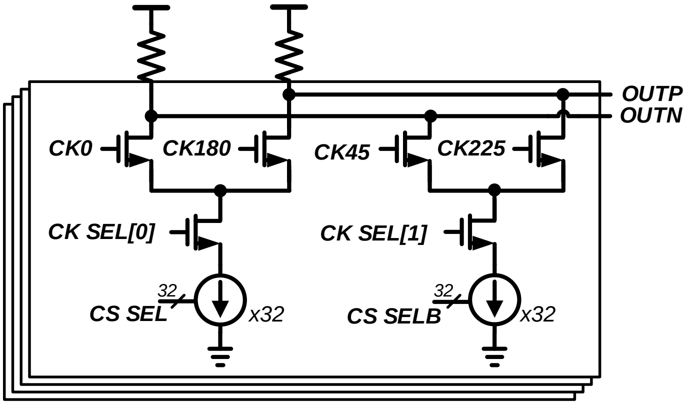
3.3.2 Phase Interpolator

The 8 phase clock delivered from the PLL is interpolated into a differential clock with a specific phase through the phase interpolator (PI). By adjusting the phase of the clock used in the serializer, the phase of DQS and WCK output can be changed. For a resolution of 1 ps or less, PI with a resolution of 78.125 fs is designed with 8-bit control, based on a 5 GHz clock.

The structure of the PI used in this chip is shown in Fig. 3.4. It receives 8 phase clocks, generates 2 phase differential clock through CML PI, and AC buffer sharpens the created clock and corrects duty. A CML structure is selected instead of a CMOS structure that is sensitive to supply noise. The phase is interpolated by the amount of current flowing by adjusting the number of current sources.



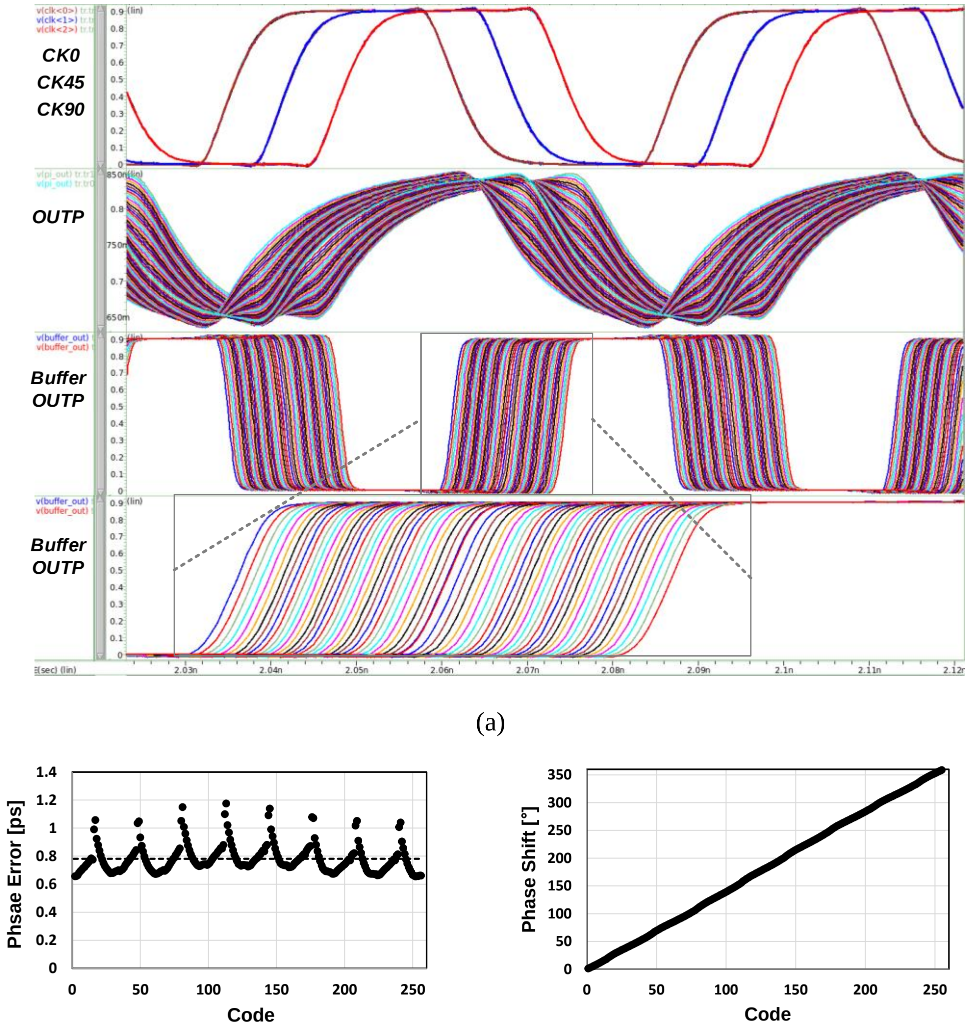
(a)



(b)

Fig. 3.4 (a) CML PI and AC buffer. (b) CML based PI.

First, two adjacent clocks to be interpolated are selected by a signal of CK SEL[0:7]. After that, the CS SEL, 32-bit thermometer code, selects how many current sources will operate in each CML. The number of current sources determines the amount of current flowing through each CML. And the clock is interpolated according to this ratio. The obtained OUTP and OUTN do not have a full swing and have a bad slew. Therefore, an AC buffer and several inverters are placed to make it a sharp clock with full swing. Fig. 3.5 shows the result of simulating PI by giving 8 phase clocks input and sweeping the selection code. Fig. 3.5 (a) shows waveforms when CK0 with a phase of 0 ° and CK45 with 45 ° are selected, and CK45 and CK90 are selected. CS SEL code is fully adjusted in each case. After CML PI, the OUTP signal swings from 650 mV to 850 mV but is converted to full swing through the buffer (Buffer OUTP). The last waveform is the final output of PI. It can be seen that each phase difference is relatively constant. The degree of phase error and phase shift by code are shown in graphs in Fig. 3.5 (b) and (c). Fig. 3.5 (b) shows that each phase error does not differ much with 78.125 fs, an ideal error, with a maximum of 39.4 fs. And Fig. 3.5 (c) shows the phase is linearly shifted in 360 ° of the whole code.



(a)

(b)

(c)

Fig. 3.5 Simulation results of PI (a) waveform, (b) phase error, and (c) phase shift.

How linear the PI is can be expressed numerically. If the difference in each phase is H, differential non-linearity (DNL) can be defined as a difference between ideal H and current H as in Equation (3.1) [20] The DNL calculated using Equation (3.1) is plotted in Fig. 3.6. This PI consumes an average of 1.43 mW of power and operates with a maximum of 0.57 LSB DNL at 2 GHz and 0.5 LSB at 5 GHz.

$$DNL = (H(i) - H_{ideal})/H_{ideal} \quad (3.1)$$

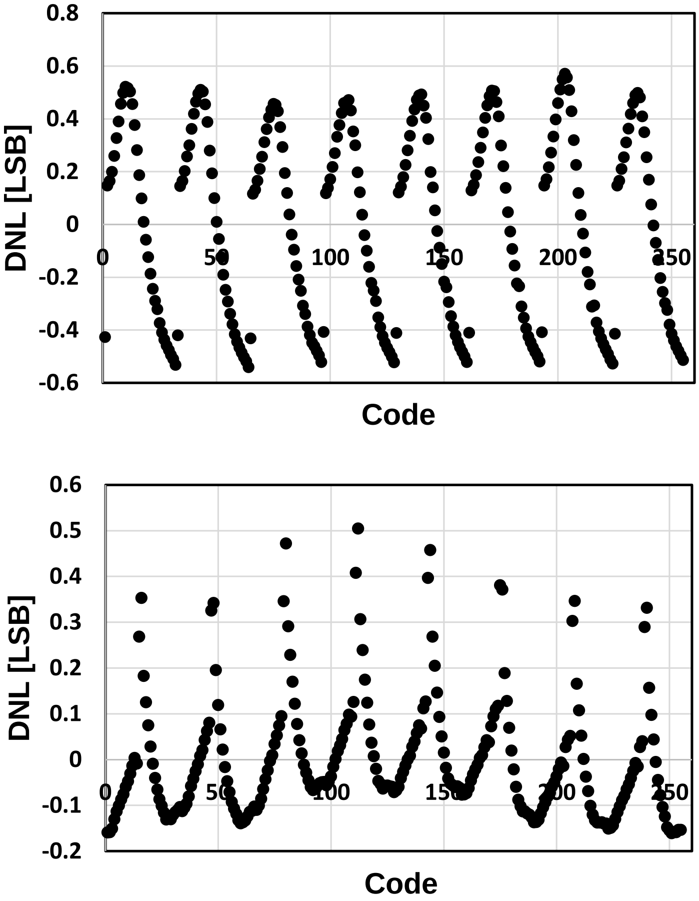


Fig. 3.6 DNL of the PI (a) at 2 GHz and (b) at 5 GHz.

3.3.3 Serializer

The parallel digital output signal of 16-bit is combined into a 1-bit 10 Gb/s signal by a 16:1 serializer. The serializer is designed by stacking a 2:1 serializer that is a conventional structure. The sequence of inputs is configured as Fig. 3.7 so that the order of Dout, which is a serialized output, is generated sequentially from D[0] to D[15]. Each 2:1 serializer consists of latches and a 2:1 MUX, as mentioned in Chapter 2.3.2.

The latch is implemented by a clocked CMOS structure of [21] advantageous for power consumption, and 2:1 MUX was similarly implemented by connecting two tri-state inverters (Fig. 3.8).

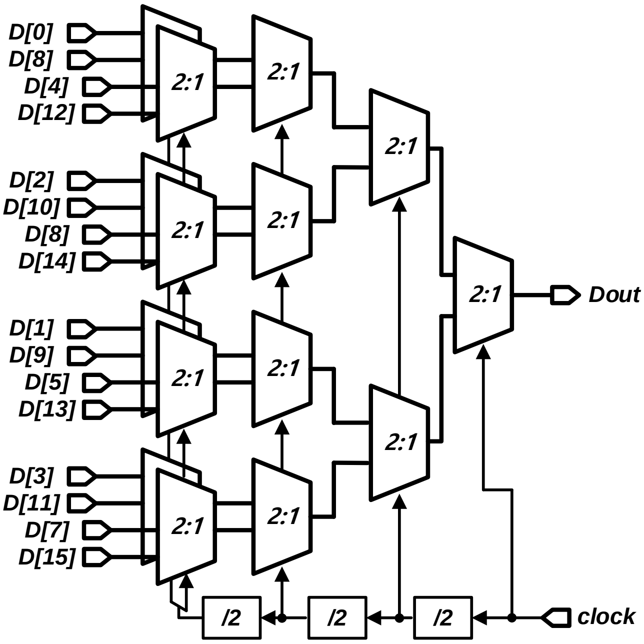


Fig. 3.7 16:1 serializer structure.

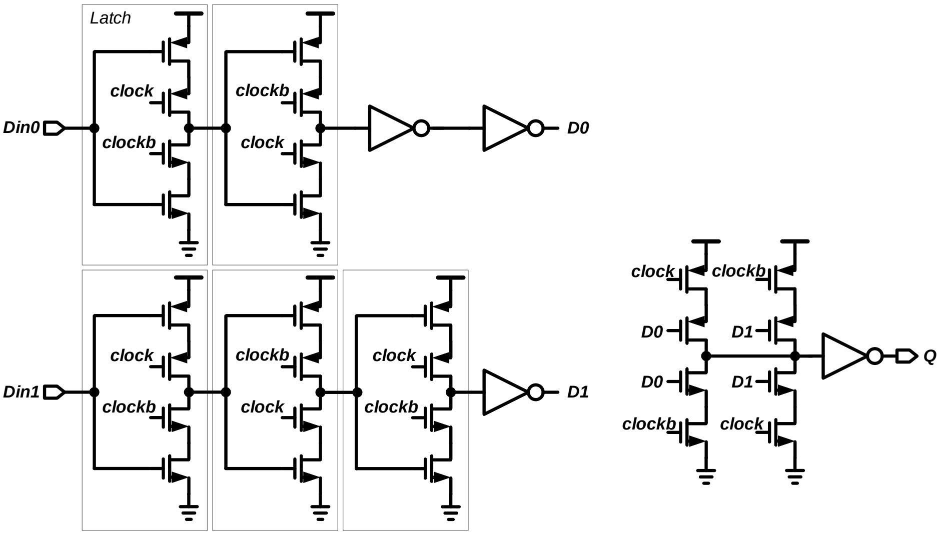


Fig. 3.8 2:1 serializer structure.

The timing at which DQS and WCK are transmitted is an essential condition to be considered when it comes to this chip. All eight DQS and WCK outputs should be exported at the same timing. In addition, the delay in which WCK is output after DRE1 goes high and the delay in which DQS is output after DRE2 goes high should be the same and always have a constant value. The same drivers are used for all TX, and the driver operates independently with the clock. So the above conditions can be satisfied only when the clocks used for the serializers of all TXs are the same. Clocks of the same timing are delivered to the serializer by making all clock paths the same, but a problem occurs in the divided clock. In general, a divider consists of an inverter and a flip-flop (FF) and is implemented by inverting the output of FF and giving it again to FF input. In this situation, since a loop is formed, the clock phase may vary by 180 °, depending on the initial value. That is, the phase of each divided clock may be changed every time the power is reset, and the divided clocks used for each serializer may have different phases. Therefore, to prevent this, the divider was designed, as shown in Fig. 3.9. Two schemes have been added; (1) The output of one FF is shared as the input of all FFs so that all outputs, divided clocks, have the same phase. (2) The RST signal is used to make the delay between DRE1 and WCK (also DRE2 and DQS) constant. For the deserializers of DRE inputs, the divider is implemented in the same way and gets the same RST signal. So, the clocks for the DRE1 (DRE2) deserializer and the WCK (DQS) serializer have the same phases. As a result, if the digital delay is constant, the DRE1 to WCK (DRE2 to DQS) delay will also be constant.

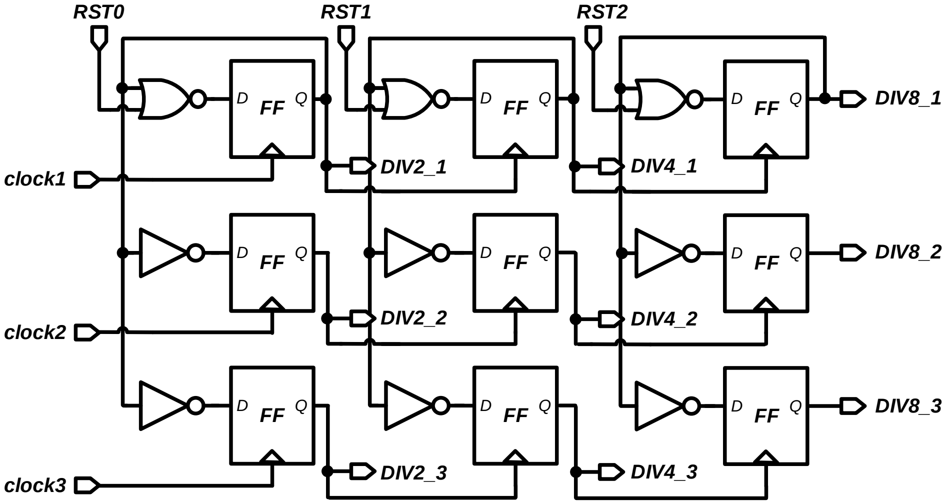
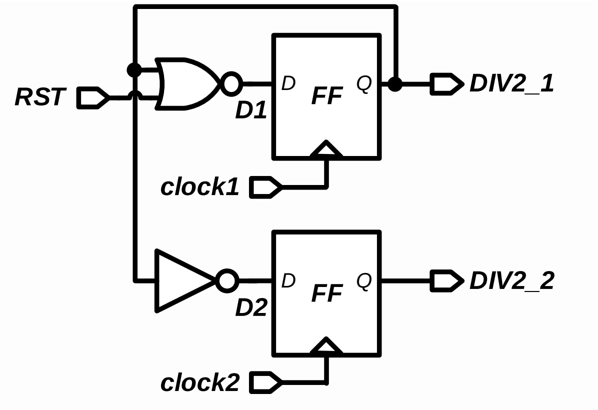


Fig. 3.9 Structure of divider for serializer.

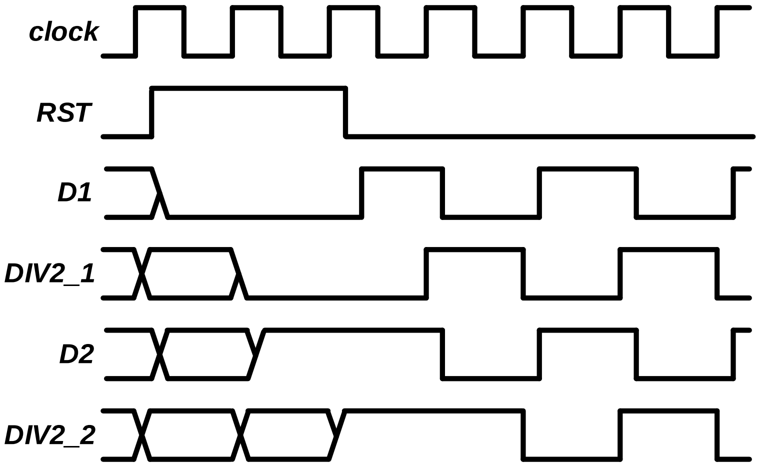
Fig. 3.10 shows how the divider operates when sharing the output node of one FF as the inputs of 2 FFs. As shown in Table 3.2, if RST is 0, the NOR gate acts as an inverter, so D1 and D2 have the inversion of DIV2_1. Therefore, if the timing of clock1 and 2 is the same, DIV2_1 and DIV2_2 will have the same value. When RST is 1, whatever DIV2_1 is, D1 becomes 0. That means by raising the RST to 1, the initial state of D1 may become 0. If RST continues to be 1, D1 continues to be 0. So a pulse having a sequence of 0, 1, 0 should be used as RST. In the case of D2, since it always has the inversion of DIV2_1, D1 and D2 have different values while RST is 1. But when RST becomes 0 again, D1 and D2 have the same value. Thus DIV2_1 and DIV2_2 have the same state after the reset.

Table 3.2 Divider state.

RST	DIV2_1	D1	D2
0	0	1	1
0	1	0	0
1	0	0	1
1	1	0	0



(a)

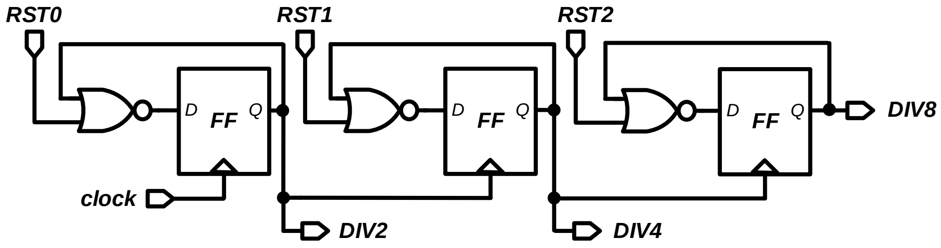


(b)

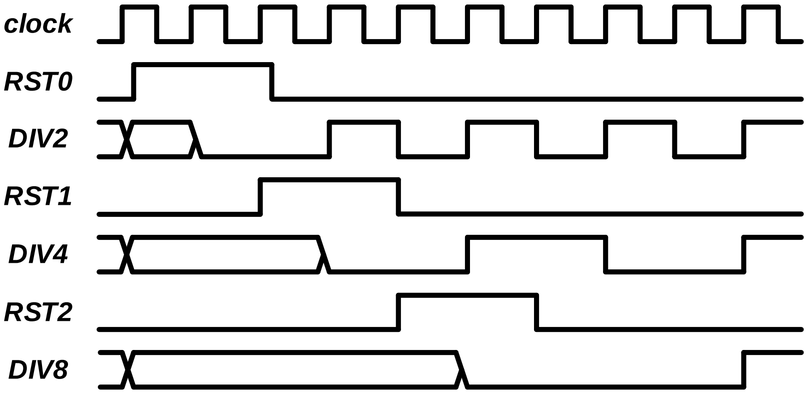
Fig. 3.10 (a) Part of divider – sharing node and (b) timing diagram of (a).

The PLL clock, divided by 2, 4, and 8 clocks are required for the 16:1 serializer. The divider proposed in this thesis also consists of stacked /2 dividers like a conventional divider. Let's see if the RST signal causes no problem. Fig. 3.11 shows the situation in which three /2 dividers are stacked to create a clock divided by 8. If RST is 1, the FF output goes 0; the clock for the next FF is 0. Therefore, after the previous RST pulse is over, and then the latter RST pulse comes in. In particular, the RST pulse safely lasts at 1 during 2 PLL clocks. When RST0 is 1 in the first stage, DIV2 goes 0. And when RST0 becomes 0 again, DIV2 goes 1 and then continues to toggle. This DIV2 is used as a clock for the next stage. Similarly, if RST1 is 1, DIV4 goes 0, and when DIV2 rises after RST1 becomes 0, DIV4 also rises. The last stage also operates on the same principle, with the initial state of DIV8 being zero and DIV8 rising after the DIV4 rises. In the case of RST signals, RST0 is first created by FF, inverter, and

AND gate, as shown in Fig. 3.12. And RST1 and RST2 are created by delaying it by 2 and 4 PLL clocks each through FF.

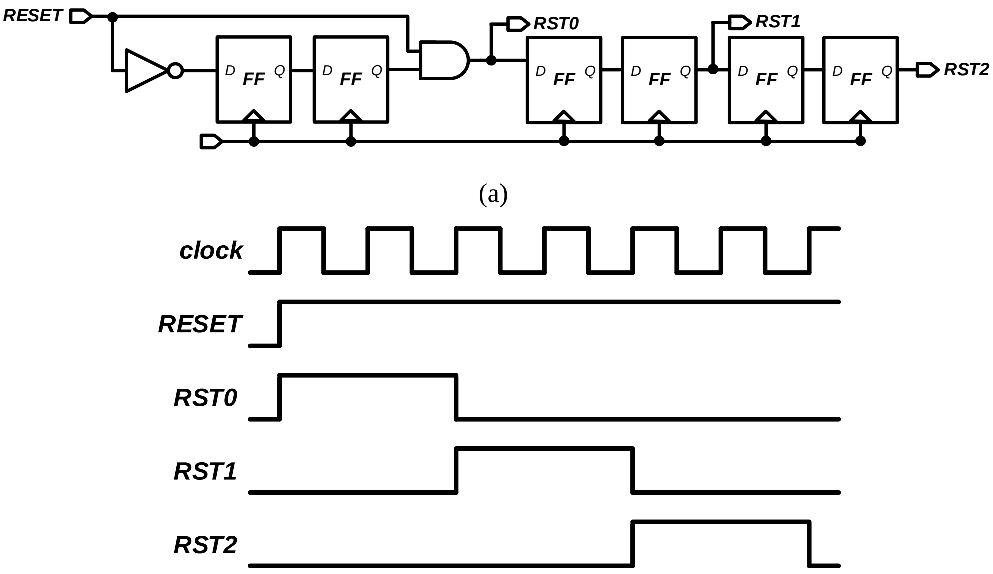


(a)



(b)

Fig. 3.11 (a) Part of divider – stacked and (b) timing diagram of (a).



(b)

Fig. 3.12 (a) Reset signal generation and (b) timing diagram of (a).

Transient simulation is used to check whether the proposed serializer works correctly. First, to confirm serializer itself performs well with 16 to 1 operation, 16 PRBS-7 patterns with different seeds are put in an appropriate order as inputs, and a PRBS-7 pattern is checked as output (Fig. 3.13). 16-bit 625 Mb/s signals are well serialized to a 1-bit 10 Gb/s signal, Dout, and it is matched with an ideal PRBS-7 pattern. Fig. 3.14 shows that the timing of serializer output is constant after receiving the reset signal. In two cases of different initial conditions, DIV2, DIV4, and DIV8 initially have different states. But after reset, each of them has the same value, and so does Dout. This data is also consistent with the ideal PRBS-7 pattern. Since it is a differential signal, two serializers are required per 1 TX lane, but only one divider is used because they operate in the same clock. Running one divider and two serializers consumes an average of 4.9 mW of power.

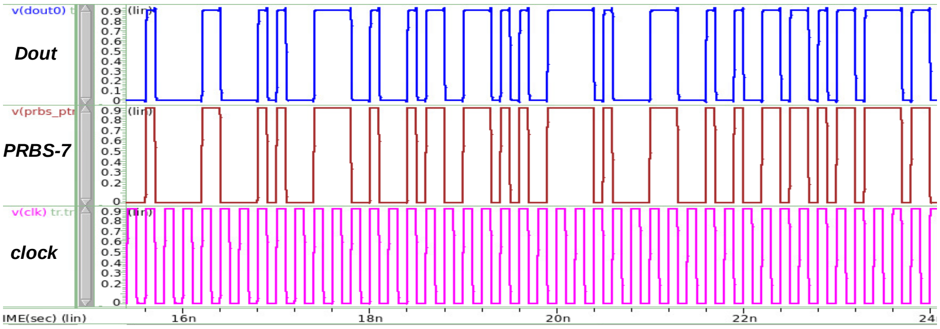


Fig. 3.13 Serializer transient simulation – PRBS-7 pattern.

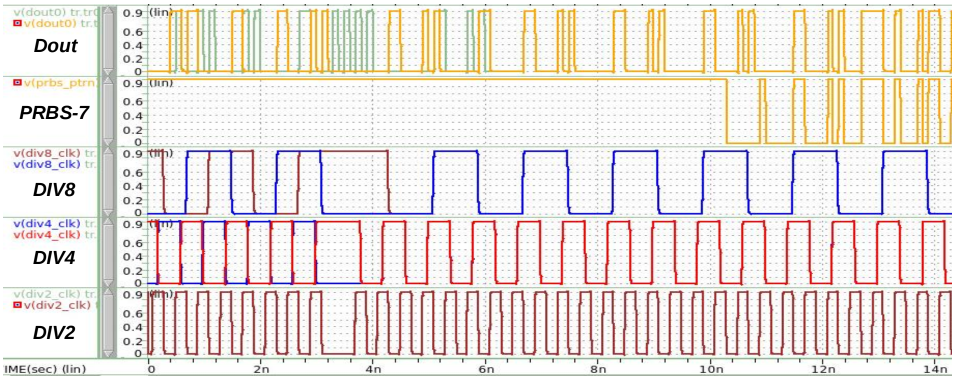


Fig. 3.14 Serializer transient simulation – 2 different initial condition.

3.3.4 Driver

The TX of this chip has differences from other typical TXs. The output from the serializer is not directly transmitted to the driver but goes through MUX. Moreover, in the case of TX for DQS, the driver's activation is adjusted in real-time (Fig. 3.1). As mentioned earlier, this chip does not always transmit DQS and WCK, but there is a mode in which it transmits high or low signals for testing (fix-high, fix-low). Therefore, 3:1 MUX (Fig. 3.15) receiving serializer output, VDD, and VSS as input is placed in front of the driver. In addition, since the enable signal of the driver should be longer back and forth than input data, a pulse generator block is required to make a longer enable signal. It is extended by giving delay and using OR gate. Here, it can be delayed through the inverter chain, but FF is used instead to provide enough margin (Fig. 3.16).

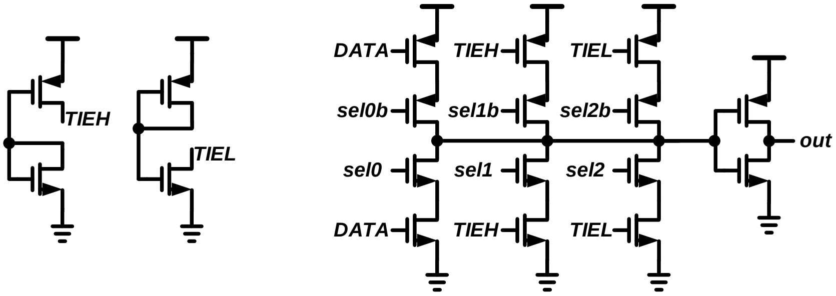
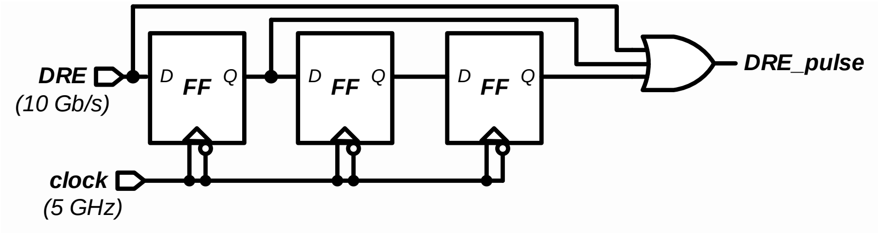


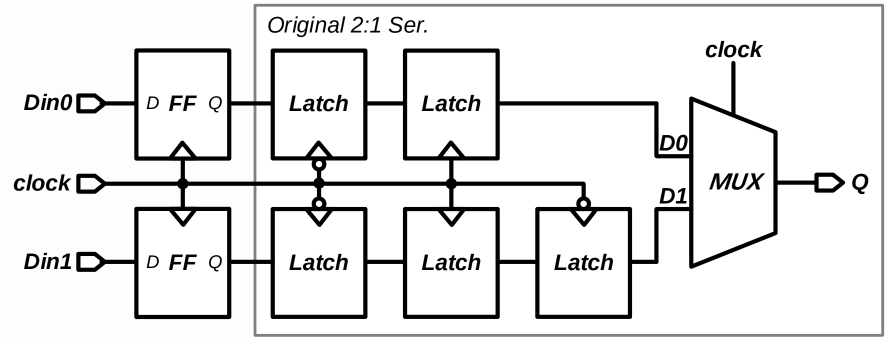
Fig. 3.15 Schematic of 3:1 MUX.

DRE and data (DQS and WCK) operate at a maximum data rate of 10 Gb/s, but since the PLL clock operates at 5 GHz, data should not be aligned by the clock's rising edge. Thus, in the case of DRE, it is delayed using a double-edge triggered FF that operates at both the rising and falling edges. The structure of the FF used is in Fig.

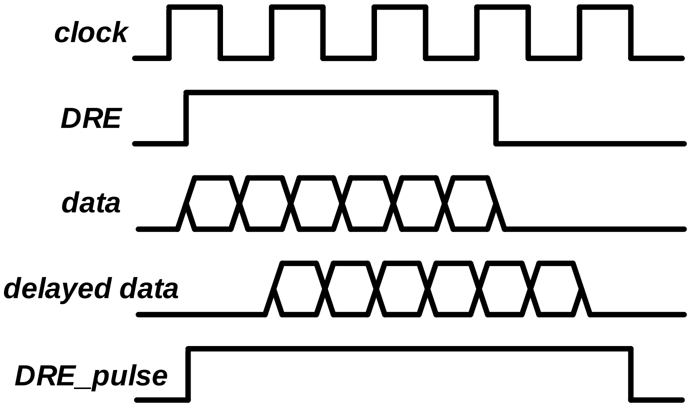
3.16 (d), as shown in [22] In the FF, MUX comes immediately after the latch, so many jitters occur in the output. In the case of DRE, there is no big problem because it is not data but just an enable signal. But the case of DQS and WCK, this FF is not used because many jitters should not occur. Instead, as shown in Fig. 3.16 (b), FF was added to the front end of the last 2:1 serializer in the 16:1 serializer so that all of them can be delayed by one cycle without skip data. Fig. 3.16 (c) shows that the DRE_pulse is longer back and forth than the data. For fix-high and fix-low mode, a high or low signal must be output regardless of DRE, so the mode selection signal and the DRE_pulse signal are appropriately combined to make an enable signal of the driver.



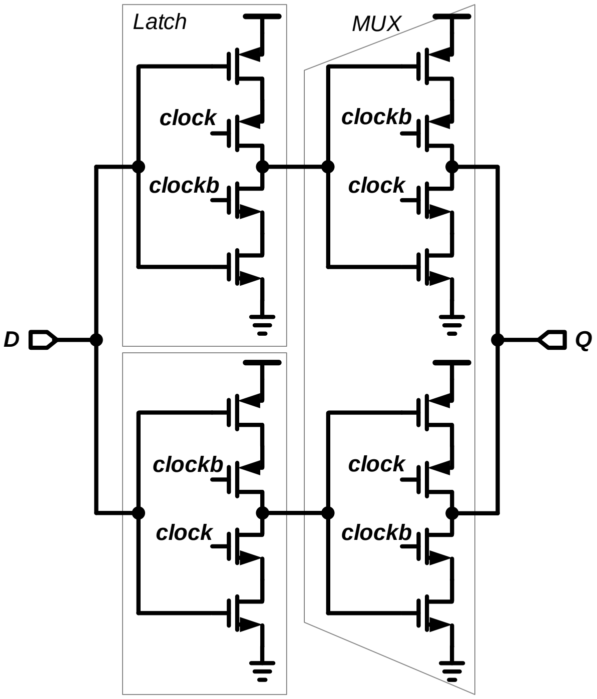
(a)



(b)



(c)



(d)

Fig. 3.16 (a) Enable pulse generator block, (b) last stage 2:1 serializer for data,

(c) timing diagram of DRE and data, and (d) double-edge triggered FF.

This chip typically transmits the differential signal, but there are cases where only one of the two drivers sends a high or low signal. Therefore, 1 TX lane has two single-ended drivers other than a differential driver. As shown in Fig. 3.17, each driver consists of a pre-driver and a main driver. 1.2 V is used as the supply voltage for the main driver, but 0.9 V is used for the previous TX stages, so a pre-driver is needed for level shifting.

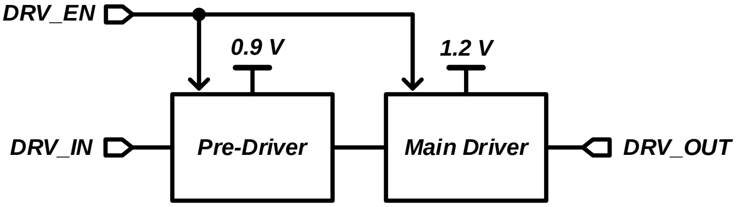


Fig. 3.17 Driver structure.

The level shifter exists to shift the supply voltage in the pre-driver (Fig. 3.18). The level shifter’s input requires a differential signal, so the DRV_IN is converted to PRE_INP and PRE_INN. In addition, according to the enable signal of the driver, the pre-driver also receives the PRE_EN to adjust on/off. Finally, the width of the last stage inverter is increased to 32 µm (PMOS), 16 µm (NMOS) through buffer due to the large MOSFET width of the main driver.

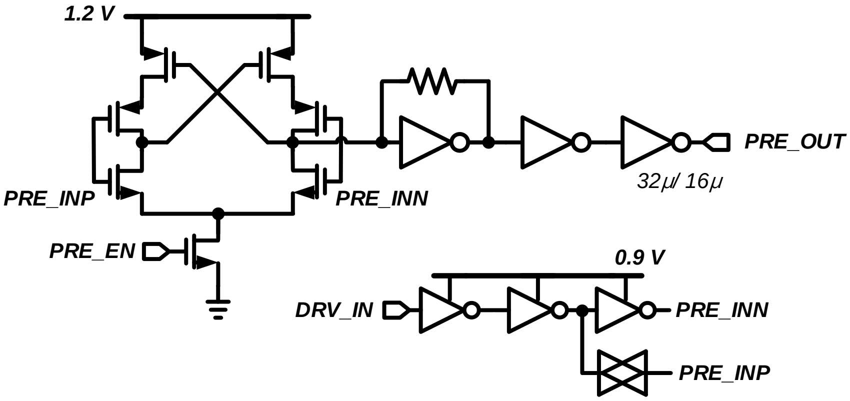


Fig. 3.19 Schematic of pre-driver.

The main driver is designed in a current mode that is robust for supply noise. And in the case of LPDDR5, ground termination is required, so the main driver consists of PMOS and resistor (Fig. 3.19). The resistor comprises six slices of 240 Ω to be controlled to 40/ 48/ 60/ 80/ 120 Ω. Since PMOS is in the saturation region, the resistor slices determine the total resistance. In addition, binary-weighted current DAC and current mirror is used to adjust the amount of current, as shown on the left side of Fig. 3.19. Therefore, the voltage swing may be changed.

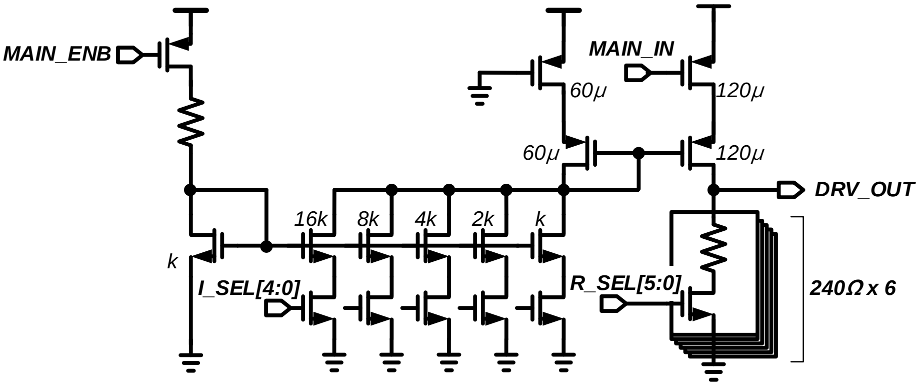


Fig. 3.18 Schematic of main driver.

Considering the termination of LPDDR5 and capacitance of pad and ESD, the driver is simulated with 40/ 80 Ω resistor and 300 fF capacitor. For Fig. 3.20, 40 Ω is selected as the resistance, all current source switches are turned on, and a PRBS-7 pattern of 10 Gb/s is given as driver input. When a signal with 0.9 V swing is given as input, the pre-driver output is level shifted to have a 1.2 V swing, and the final driver output has a swing of 0.6 V. Fig 3.21 shows the eye-diagrams of the driver outputs in various current and resistor control signals. When the maximum current flows, 30 mA, an average of 33.3 mA flows throughout the whole driver.

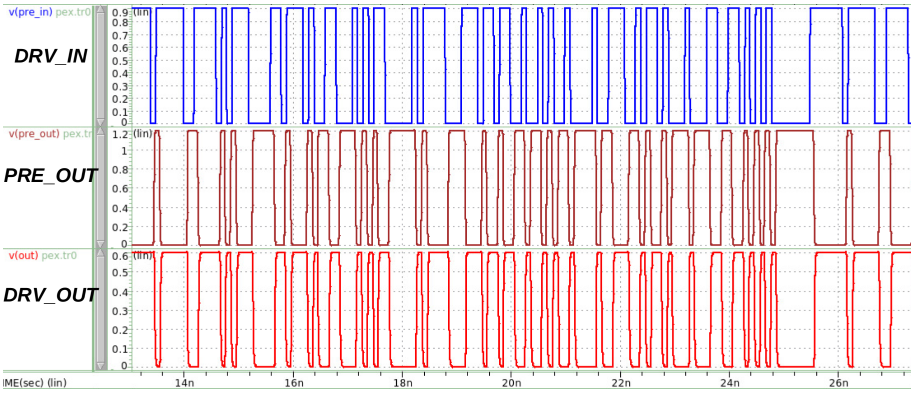


Fig. 3.20 Transient simulation of driver.

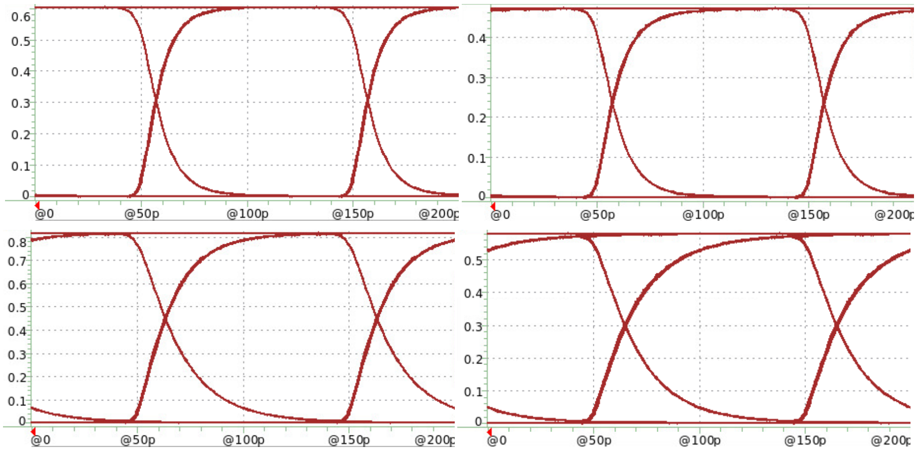


Fig. 3.21 Eye diagrams of driver outputs. (a) I_SEL=5’b11111, R_SEL=6’b111111, (b) 5’b10000, 6’b11111, (c) 5’b10000, 6’b111000, and (d) 5’b01000, 6’b111000.

Chapter 4

Measurements Results

4.1 Die Photomicrograph

The prototype chip is fabricated in a 40 nm GP CMOS process. Die photomicrograph of the chip is shown in Fig. 4.1. The total chip area, including pads, is 1.96-mm^2, and the TX 1-lane from PI to driver is 400 μm wide and 150 μm long, with an area of 0.06 mm^2. RX 2-lane and PLL are also included in this chip, and there is also an I2C block for giving control signals. The total chip power consumed is 271.2 mW at a 10 Gb/s data rate, and the 1 TX lane consumes 31.4 mW of power, except for the digital block.

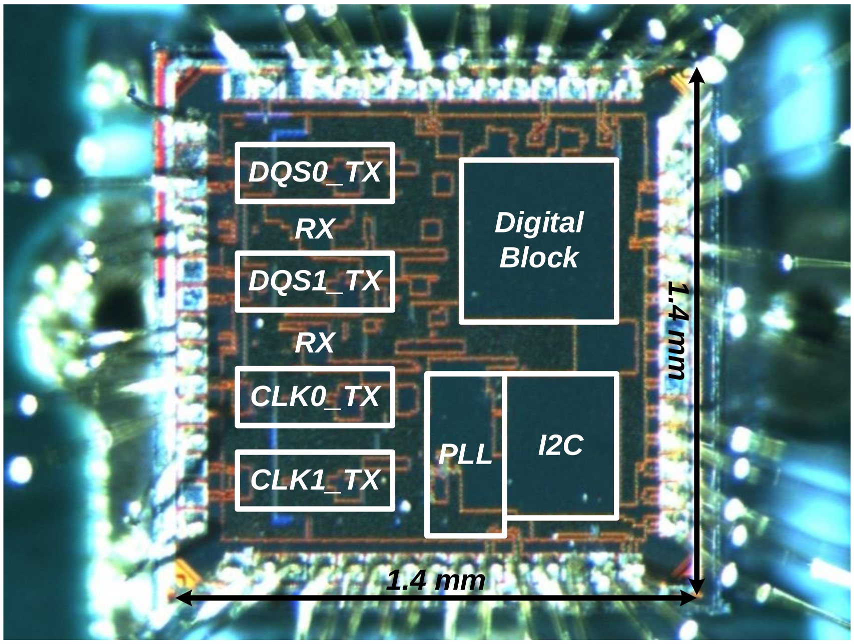


Fig. 4.1 Die photomicrograph.

4.2 Measurement Setup

Inputs required for measurement include supply voltage, write signals of I2C, differential clock, and DREs (Fig. 4.2). A power regulation board receives a supply of 5 V and ground from Agilent E3631A DC power supply, regulates power to reduce supply noise, and supplies the voltage suitable for each domain to the chip. Various control signals for analog and digital blocks are provided through the I2C block. For example, the I2C block offers the pattern for the parity mode of DQS and the PI and driver's selection codes. The PC and this chip communicate through Aardvark, and signals are written to the I2C block using python. Anritsu MP1800A equipment provides differential clock and DRE signals. Not all TX lines were measured simultaneously while giving DRE1 and DRE2 at the same time, but only 1 TX line was measured by connecting to Tektronix MSO71604C Oscilloscope while giving only one DRE signal at a time.

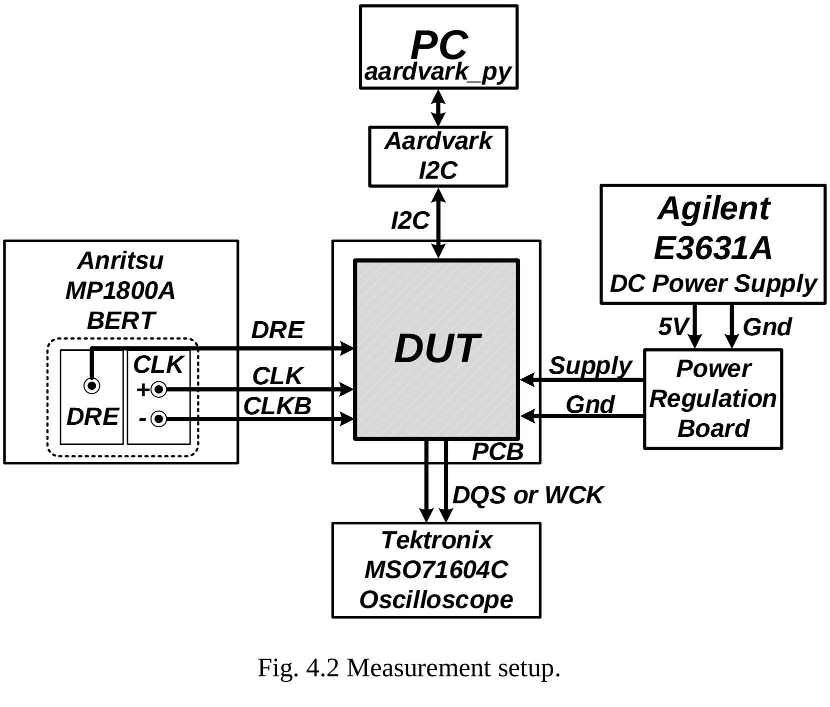
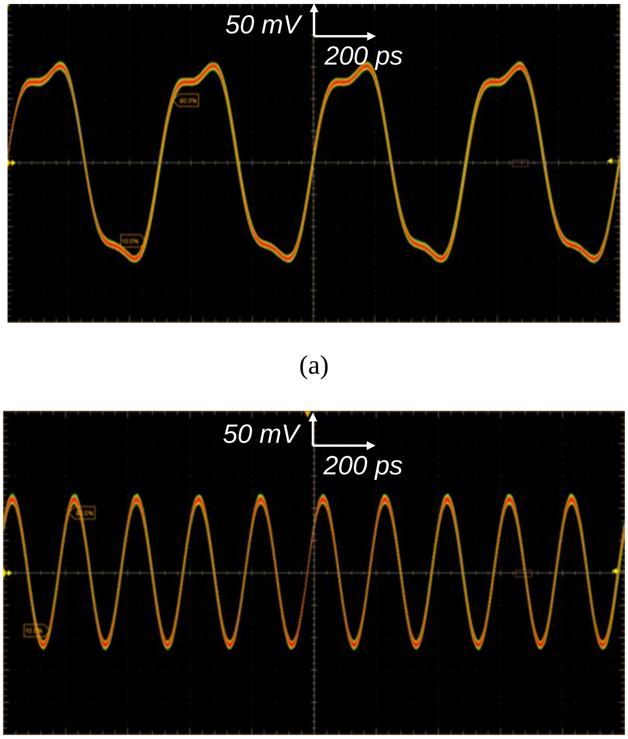


Fig. 4.2 Measurement setup.

4.3 Measurement Results

Pattern and eye-diagrams of DQS and WCK were measured using the Oscilloscope. Fig. 4.3 shows the DQS output result when DRE2 is high. The termination resistance is 50 Ω, and the current flows in maximum. Fig. 4.3 (a) and (b) show the 4 Gb/s and 10 Gb/s output, respectively, and since DRE2 is high, it shows a toggle like a typical clock.



(a)

(b)

Fig. 4.3 DQS output when DRE2 is high at (a) 4 Gb/s and (b) 10 Gb/s.

When DRE2 is controlled, the result of the DQS output is shown in Fig. 4.4. The above is a waveform of DQS, and the following is a waveform of DRE2. When DRE2 is low, the pattern is not output, but when DRE2 goes high, after a certain delay, the pattern is output. Here, pre-ambles and post-ambles are also exported so that the first and last patterns have some data rather than a clock toggle.

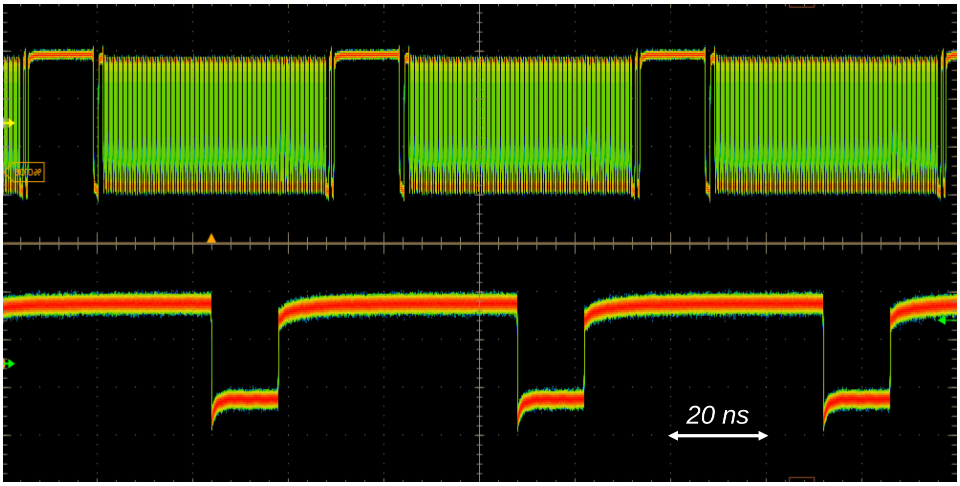


Fig. 4.4 DQS output controlled by DRE2 at 4 Gb/s.

In the case of DQS, it may be used as a parity. In this case, the pattern input to the register is repeatedly output as it is. The DQS output is shown in Fig. 4.5 when input has repeated 64-bit data, which is half the pattern corresponding to PRBS7. It can be seen that 64’h91C2_F95C_D13C_50C1 is well output when DRE2 is high for 128-bits.

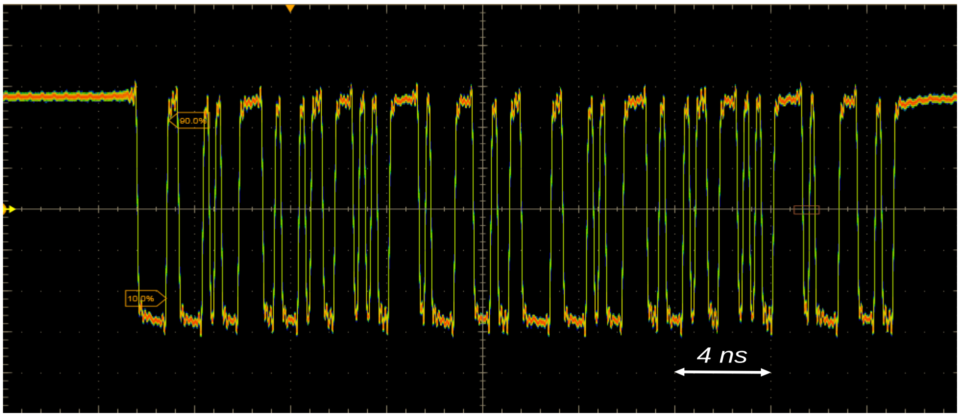
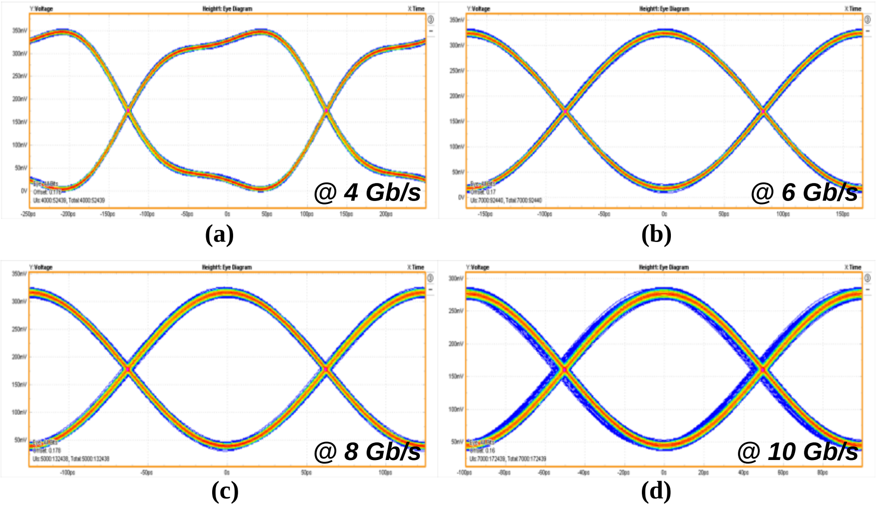


Fig. 4.6 DQS as a parity at 4 Gb/s.

As shown in Fig. 4.6, eye-diagrams are obtained to find out the characteristics of DQS, a clock pattern when DRE2 is high. Similarly, it has 50 Ω-termination and maximum current, and eye diagrams are drawn at 4 Gb/s, 6 Gb/s, 8 Gb/s, and 10 Gb/s. The characteristics of the output at each data rate are summarized in Table 4.1. All have an RMS-jitter of about 1 ps, and the faster the data rate, the lower the amplitude.



(a) (b)

(c) (d)

Fig. 4.5 Eye-diagrams of DQS at (a) 4 Gb/s, (b) 6 Gb/s, (c) 8 Gb/s, and (d) 10 Gb/s.

Table 4.1 Performance summary of Fig. 4.6.

	Data rate	**Frequency**	**RMS jitter**	**Peak to Peak Voltage**
(a)	4 Gb/s	2.000 GHz	962.97 fs	340.8 mV
(b)	6 Gb/s	3.000 GHz	872.21 fs	303.45 mV
(c)	8 Gb/s	4.001 GHz	1.0532 ps	272.55 mV
(d)	10 Gb/s	5.001 GHz	770.09 fs	229.01 mV

Fig. 4.7 shows the output result of WCK when DRE1 is high. 40 Ω is selected as the termination resistance, and the current flows in maximum. Fig. 4.7 (a) shows the WCK output result when DRE1 is controlled. When DRE1 is low, the pattern does not appear, and then DRE1 goes high, the pattern is output. Its enlarged view is shown in Fig. 4.7 (b). It can be seen that there are pre-ambles in which the rate of toggle increases gradually after having a static value with a specific length.

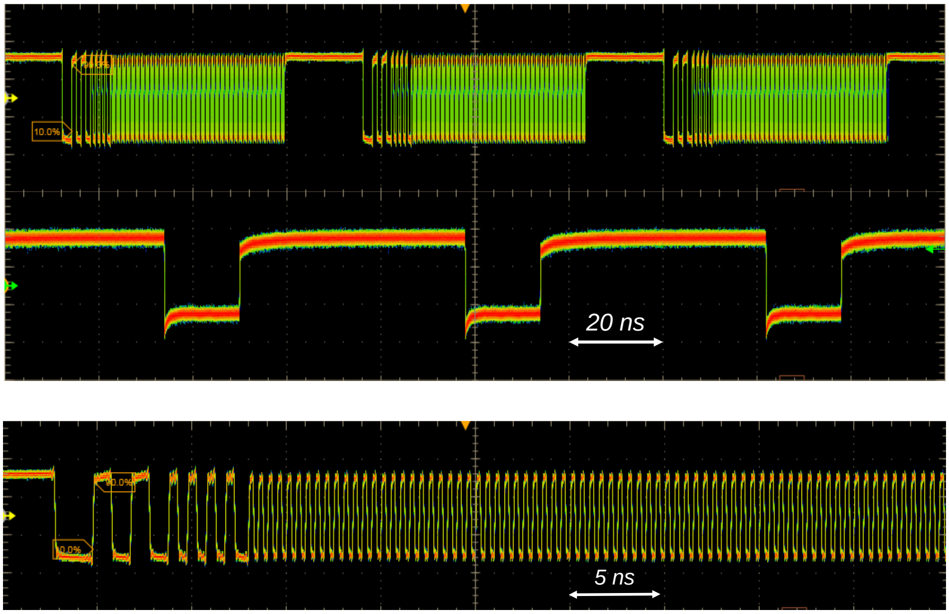


Fig. 4.7 (a) CLK output controlled by DRE1 at 4 Gb/s and (b) enlarged view of (a).

The eye-diagrams of WCK are also drawn to find out the characteristics of the clock pattern (Fig. 4.8). They are the result of 4 Gb/s and 10 Gb/s data rate when 40 Ω termination is selected. As shown in Table 4.2, like DQS, WCK has an RMS-jitter less than 1 ps, and the faster the data rate, the lower the amplitude. In addition, in Fig. 4.8 (c), the amount of current flowing is reduced, and as a result, the voltage swing decreases. Even when the termination resistance is changed, eye-diagrams are obtained at a data rate of 10 Gb/s (Fig. 4.9). It can be seen that the larger the resistance, the larger the voltage swing.

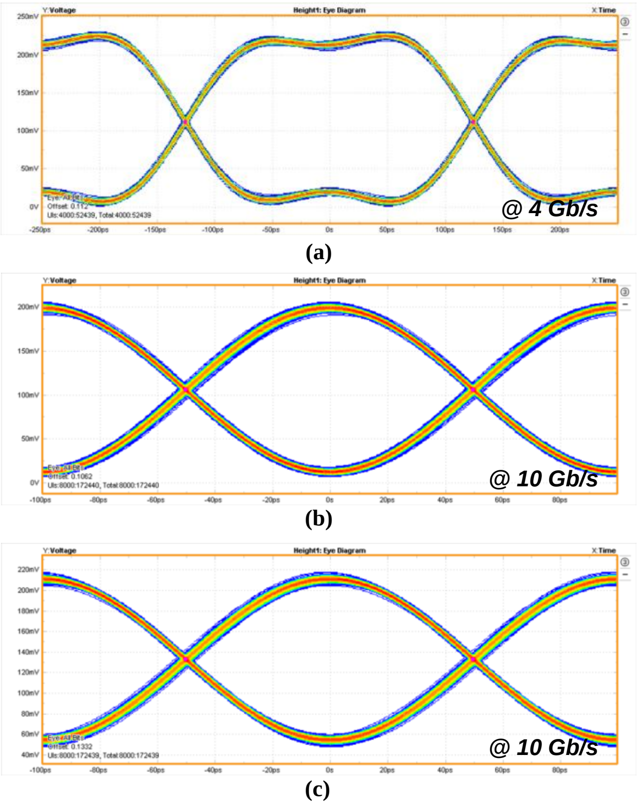
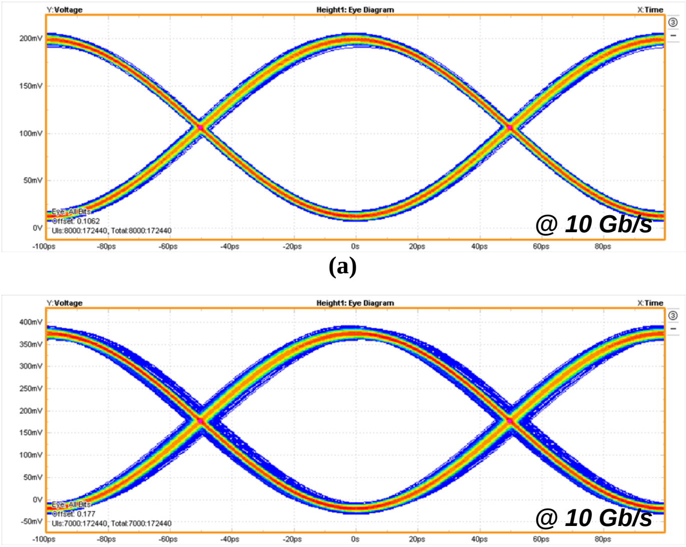


Fig. 4.8 Eye-diagrams of CLK (a) at 4 Gb/s, I_SEL=5’b11111,

(b) at 10 Gb/s, I_SEL=5’b11111, and (c) at 10 Gb/s, I_SEL=5’b10000.

Table 4.2 Performance summary of Fig. 4.8.

	Data rate	**Frequency**	**RMS jitter**	**Peak to Peak Voltage**
(a)	4 Gb/s	2.000 GHz	910.47 fs	216.44 mV
(b)	10 Gb/s	5.001 GHz	894.21 fs	184.07 mV
(c)	10 Gb/s	5.001 GHz	866.32 fs	153.69 mV



(a)

(b)

Fig. 4.9 Eye-diagrams of CLK at 10 Gb/s

(a) R_SEL=6’b111111 and (b) R_SEL=6’b000000.

	Data rate	**Frequency**	**RMS jitter**	**Peak to Peak Voltage**
(a)	10 Gb/s	5.001 GHz	894.21 fs	184.07 mV
(b)	10 Gb/s	5.001 GHz	1.0445 ps	385.34 mV

Table 4.3 Performance summary of Fig. 4.9.

4.4 Performance Summary

The total area of the proposed BOST chip is 1.96 mm^2, of which the total area of 4 TX lanes excluding digital block is 0.24 mm^2. When transmitting data of 10 Gb/s, a total of 271.2 mW of power is consumed, of which 1 TX lane consumes 31.4 mW of power. Table 4.4 shows the supply voltage and power consumption for each block of the entire chip. Power breakdown was calculated based on post-layout simulation results because TX shares the supply voltage with other analog blocks such as RX and PLL. The driver alone uses 1.2 V of supply voltage, and other analog and digital blocks, except for the I2C block, use 0.9 V of voltage. A lot of power is consumed in the current mode driver, and a lot of power is also consumed in delivering the clocks (Fig. 4.10). As a result, 10101010 patterns of 10 Gb/s DQS having a 230 mV swing and 770 fs RMS jitter are measured with the termination of 50 Ω. Also, with the termination of 40 Ω, 10 Gb/s WCK having a 185 mV swing and 894 fs RMS jitter is measured.

Table 4.4 Supply voltage and power breakdown of each block.

	Supply voltage	**Power breakdown**
Driver 4-lane	1.2 V	84 mW
TX 4-lane	0.9 V	41.5 mW
RX 2-lane		38.8 mW
PLL & Clock path		79.9 mW
Digital Block		27 mW

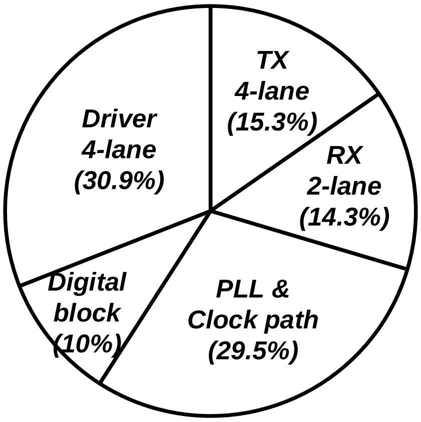


Fig. 4.10 Power breakdown.

Table 4.5 presents a comparison with other works that speed up the ATE signals. Most of the works use PLL for frequency multiplication and [23] multiplexes parallel signals from ATE. This work has no feedback like calibration or compensation, so it can transmit fast signals. The measured data rate is up to 5 Gb/s in other works, but up to 10 Gb/s outputs are measured in this work.

Table 4.5 Comparison with other testing chips.

	[2]	[4]	[23]	[24]	This work
Tech.	**130nm CMOS**	**x**	**PCB**	**20nm DRAM CMOS**	**40nm CMOS**
Built-in/out	**Built-out**	**Built-in**	**Built-out**	**Built-out**	**Built-out**
Frequency multiplication	**By PLL**	**PLL or DLL**	**MUX**	**PLL**	**PLL**
Other functions	**Skew compensation**	**Fail map generation**	**x**	**Self timing/voltage calibration**	**Phase control, DQS check**
Data rate	**440 Mb/s**	**800 Mb/s**	**5 Gb/s**	**3.2 Gb/s**	**10 Gb/s**

Chapter 5

Conclusion

In this thesis, the high-speed transmitter of BOST for LPDDR5 is proposed. The BOST chip receives low-speed signals from ATE and transmits high-speed signals to DRAM using PLL, doubling the frequency. Since DQS and WCK are not general clock patterns, the digital block and transmitter with serializers are required. Moreover, their phase should be finely adjusted, so a phase interpolator is also needed. The phase interpolator and driver are designed in the current mode to endure supply noise.

The proposed BOST is fabricated in the 40nm CMOS process. It consumes a total of 271.2 mW of power and occupies 1.96 mm^2. Among them, 1 TX lane consumes 31.4 mW and occupies 0.06 mm^2. When DRE is high, clock pattern, pre-ambles, post-ambles, and parity pattern are measured as desired. It transmits up to 10 Gb/s DQS with a swing of 230 mV and an RMS jitter of 770 fs and WCK with a swing of 185 mV and an RMS jitter of 894 fs to DRAM.

Bibliography

[1] S. Sunter and A. Roy, “A self-testing BOST for high-frequency PLLs, DLLs, and SerDes,” 2007 IEEE International Test Conference, 2007, pp. 1-8.

[2] J. Park et al., “At-Speed Test of High-Speed DUT Using Built-Off Test Interface,” 2010 19th IEEE Asian Test Symposium, 2010, pp. 269-274.

[3] J. Dreibelbis, J. Barth, R. Kho and Kalter, “An ASIC library granular DRAM macro with buit-in self test,” 1998 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, 1998, pp. 74-75.

[4] M. Nelms, K. Gorman and D. Anand, “Generating At-Speed Array Fail Maps with Low-Speed ATE,” Proc, 22nd IEEE VLSI TEST Symposium, 2004, pp. 87-92.

[5] Wikipedia, serial communication. [Online] [Accessed on 2nd Nov. 2021] http://en.wikipedia.org/wiki/serial_communication.

[6] Texas Instruments. (2016). KeyStone II Architecture Serializer/Deserializer (SerDes): User Guide. Texas, MA: Author.

[7] M. Meghelli, “A 43-Gb/s full-rate clock transmitter in 0.18-μm SiGe BiCMOS technology,” in IEEE Journal of Solid-State Circuits, vol. 40, no. 10, pp. 2046-2050, Oct. 2005.

[8] B. Raghavan et al., “A sub-2W 39.8-to-44.6Gb/s transmitter and receiver chipset with SFI-5.2 interface in 40nm CMOS,” 2013 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, 2013, pp. 32-33.

[9] X. Zheng et al., “A 40-Gb/s Quarter-Rate SerDes Transmitter and Receiver Chipset in 65-nm CMOS,” in IEEE Journal of Solid-state Circuits, vol. 52, no. 11, pp. 2963-2978, Nov. 2017.

[10] Intel.com, DQS I/O Definition. [Online] [Accessed on 16th Nov. 2021] https://www.intel.com/content/www/us/en/programmable/quartushelp/17.0/reference/glossary/def_dqs_io.htm.

[11] W. Bae, “Supply-Scalable High-Speed I/O Interfaces,” Electronics, vol. 9, no. 8, p. 1315, Aug. 2020.

[12] J. F. Bulzacchelli et al., “A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology,” in IEEE Journal of Solid-State Circuits, vol. 41, no. 12, pp. 2885-2900, Dec. 2006.

[13] S. Joshi et al., “A 12-Gb/s transceiver in 32-nm bulk CMOS,” 2009 Symposium on VLSI Circuits, 2009, pp. 52-53.

[14] S. Chen et al., “A 4-to-16GHz inverter based infection-locked quadrature clock generator with phase interpolators for multi-standard I/Os in 7nm FinFET,” 2018 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, 2018, pp. 390-392.

[15] S. Sidiropoulos and M. A. Horowitz, “A semidigital dual delay-locked loop,” in IEEE Journal of Solid-State Circuits, vol. 32, no. 11, pp. 1683-1692, Nov. 1997.

[16] D. Gong et al., “Development of A 16:1 serializer for data transmission at 5 Gbps,” in Topical workshop on electronics in particle physics, pp. 21-25, Sep. 2009.

[17] B. Nauta and M. B. Dijkstra, “Analog line driver with adaptive impedance matching,” in IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 1992-1998, Dec. 1998.

[18] C. Menolfi et al., “A 16Gb/s Source-Series Terminated Transmitter in 65nm CMOS SOI,” 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, 2007, pp. 446-614.

[19] P. Heydari, “Design and analysis of low-voltage current-mode logic buffers,” Proc, Fourth International Symposium on Quality Electronic Design, 2003, pp. 293-298.

[20] A. AbdelHadi, M. Allam and S. Ibrahim, “A high-linearity 6-GHz phase interpolator in 28-nm CMOS technology,” 2017 Japan-Africa Conference on Electronics, Communications and Computers, 2017, pp. 41-44.

[21] Y. Suzuki, K. Odagawa and T. Abe, “Clocked CMOS calculator circuitry,” in IEEE Journal of Solid-State Circuits, vol. 8, no. 6, pp. 462-469, Dec. 1973.

[22] D. Guerrero, et al. “Automatic logic synthesis for parallel alternating latches clocking schemes.” VLSI Circuits and Systems III. Vol. 6590. International Society for Optics and Photonics, 2007.

[23] D. C. Keezer, D. Minier, M. Paradis and L. Binette, “Modular extension of ATE to 5 Gbps,” 2004 International Conference on Test, 2004, pp. 748-757.

[24] J. –W. Moon et al., “An Enhanced Built-Off-Test Transceiver with Wide-range, Self-calibration Engine for 3.1 Gb/s/pin DDR4 SDRAM,” 2018 IEEE Asian Solid-State Circuits Conference, 2018, pp. 139-142.

초 록

자동 테스트 장비 (ATE)와 메모리 간의 속도 차이를 극복하기 위해 외장 자가 테스트 (BOST) 개념이 도입되었다. 본 논문은 LPDDR5 의 BOST 를 위한 송신기 설계를 제시한다. 송신기는 ATE 에서 저속 클럭을 받아서 고속 DQS 와 WCK 를 DRAM 에 전송한다. 출력에 항상 클럭 토글만 있는 것은 아니므로 데이터 패턴이 디지털 블록에서 생성된다. 또한 위상 보간기로 출력의 위상을 원하는 대로 움직인다.

송신기의 아날로그 부분은 위상 보간기, 시리얼라이저, 드라이버로 구성된다. 위상 보간기와 드라이버는 공급 노이즈에 견고하도록 전류 모드로 설계되었다. 시리얼라이저의 디바이더가 새롭게 제안되어서 모든 출력의 타이밍이 같다. 또한 ATE 에서 활성화 신호를 받아서 DRAM 으로 출력을 전송하는데 걸리는 시간도 일정하다. 그 결과 송신기는 데이터 패턴이 있는 DQS 와 WCK 를 원하는 타이밍에 DRAM 으로 전송한다.

제안된 송신기는 40 nm CMOS 공정으로 제작되었다. 송신기의 하나의 레인은 31.4 mW 를 소비하고 0.06mm^2 를 차지한다. 측정된 DQS 는 50 Ω 터미네이션일 때 10 Gb/s 에서 230 mV 의 스윙과 770 fs 의 RMS 지터를 가진다. 그리고 WCK 는 40 Ω 터미네이션일 때 10 Gb/s 에서 185 mV 의 스윙과 894 fs 의 RMS 지터를 갖는다.

주요어 : 자동 테스트 장비 (ATE), 외장 자가 테스트 (BOST), 전류 모드 드라이버, 위상 보간기 (PI), SerDes, 송신기.

학 번 : 2020-23016