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공학박사학위논문

Design and Electrical Reliability of Co Alloy Self-Forming Barrier for Advanced Interconnects

차세대 반도체 배선을 위한 코발트 합금 자가형성 확산방지막 재료 설계 및 전기적 신뢰성에 대한 연구

2022년 2월

서울대학교 대학원

재료공학부

김 철

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DESIGN AND ELECTRICAL RELIABILITY OF CO ALLOY SELF-FORMING BARRIER FOR ADVANCED INTERCONNECTS

지도교수: 주영창

이 논문을 공학박사 학위논문으로 제출함

2022년 2월

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ABSTRACT

Design and Electrical Reliability of Co Alloy Self-Forming Barrier for Advanced Interconnects

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Recently, the resistance-capacitance (*RC*) delay of the Cu interconnects in metal 1 (M1) level has been increased rapidly due to the reduction of the interconnect linewidth along with the transistor scaling down, and the interconnect reliability becomes a severe issue again. In order to overcome interconnect performance problems and move forward to the next-generation interconnects system, study on low resistivity (ρ_o) and low electron mean free path (λ) metals was conducted. Generally, metals such as Cobalt (Co), Ruthenium (Ru), and Molybdenum (Mo) are mentioned as candidates for next-generation interconnect materials, and since they have a low $\rho_o \times \lambda$ value, it is expected that the influence of interface scatterings and surface scattering can be minimized. However, harsh operating environments such as high electric fields, critical Joule heating, and reduction of the pitch size are severely deteriorating the performance of electronic devices as well as device reliability. For example, since time dependent dielectric breakdown (TDDB) problems for next-generation interconnect system have been reported recently, it is necessary to study alternative barrier materials and processes to improve the interconnect reliability. Specifically, extrinsic dielectric breakdown due

to penetration of Co metal ions in high electric fields has been reported as a reliability problem to be solved in Co interconnect systems. Therefore, there is a need for new material system design and research on a robust diffusion barrier that prevents metal ions from penetrating into the dielectric, thereby improving the reliability of Co interconnects. Moreover, in order to lower the resistance of the interconnect, it is necessary to develop an ultra-thin barrier. This is because even a barrier with good reliability characteristics will degrade chip performance if it takes up a lot of volume in the interconnect. The recommended thickness for a single diffusion barrier layer is currently reported to be less than 2.5 nm. As a result, it is essential to develop materials that comprehensively consider performance and reliability.

In this study, we designed a Co alloy self-forming barrier (SFB) material that can make sure of low resistance and high reliability for Co interconnects, which is attracting attention as a next-generation interconnect system. The self-forming barrier methodology induces diffusion of an alloy dopant at the interface between the metal and the dielectric during the annealing process. And the diffused dopant reacts with the dielectric to form an ultra-thin diffusion barrier. Through this methodology, it is possible to improve reliability by preventing the movement of metal ions. First of all, material design rules were established to screen the appropriate alloy dopants and all CMOS-compatible metals were investigated. Dopant resistivity, intermetallic compound formation, solubility in Co, activity coefficient in Co, and oxidation tendency is considered as the criteria for the dopant to escape from the Co matrix and react at the Co/SiO_2 interface. In addition, thermodynamic calculations were performed to predict which phases would be formed after the annealing process. Based on thermodynamic calculations, 5 dopant metals were selected, prioritized for self-forming behavior. And the self-forming material was finally selected through thin film and device analysis. We confirmed that Cr, Zn, and Mn out-diffused to the surface of the thin film structure using X-ray photoelectron spectroscopy (XPS) depth profile and investigated the chemical state of out-diffused dopants through the analysis of a binding energy. Cr shows the most ideal self-forming behavior with the SiO_2 dielectric and reacted with oxygen to form a Cr_2O_3 barrier. In metal-insulator-semiconductor (MIS) structure, out-diffused Cr reacts with SiO_2 at the interface and forms a self-formed single layer. It was confirmed that the thickness of the diffusion barrier layer is about 1.2 nm, which is an ultra-thin layer capable of minimizing the total effective resistance. Through voltage-ramping dielectric breakdown (VRDB) tests, Co-Cr alloy showed highest breakdown voltage (V_{BD}) up to 200 % than pure Co. The effect of Cr doping concentration and heat treatment condition applicable to the interconnect process was confirmed. When Cr was doped less than 1 at%, the robust electrical reliability was exhibited. Also, it was found that a Cr_2O_3 interfacial layer was formed when annealing process was performed at 250 °C or higher for 30 minutes or longer. In other words, Co-Cr alloy is well suited for the interconnect process because current interconnect process temperature is below 400 °C. And when the film thickness was lowered from 150 nm to 20 nm, excellent V_{BD} values were confirmed even at high Cr doping concentration (~7.5 at%). It seems that the amount of Cr present at the Co/SiO_2 interface plays a very important role in improving the Cr oxide SFB quality. Physical modeling is necessary to understand the amount of Cr at the interface according to the interconnect volumes and the reliability of the Cr oxide self-forming barrier. TDDB lifetime test also performed and Co-Cr alloy interconnect shows a highly reliable diffusion barrier property of self-formed interfacial layer. The DFT analysis also confirmed that Cr_2O_3 is a very promising barrier material because it showed a higher energy barrier value than the TiN diffusion barrier currently being studied.

A Co-based self-forming barrier was designed through thermodynamic calculations

that take performance and reliability into account in interconnect material system. A Co interconnect system with an ultra-thin Cr_2O_3 diffusion barrier with excellent reliability is proposed. Through this design, it is expected that high-performance interconnects based on robust reliability in the advanced interconnect can be implemented in the near future.

Keywords: back end of line (BEOL), RC delay, reliability, self-forming barrier (SFB), diffusion barrier, cobalt, Co-Cr alloy, Cr_2O_3, voltage ramp dielectric breakdown (VRDB), time dependent dielectric breakdown (TDDB)

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Table of Contents

Abstract……………...……………………………………………… i

Table of Contents…………………………………………………… v

List of Tables…………………………………………………….... ix

List of Figures……………………………………………………. xii

Chapter 1. Introduction

1.1. Scaling down of VLSI systems 1
1.2. Driving force of interconnect system evolution 7
1.3. Driving force of beyond Cu interconnects 11
1.4. Objective of the thesis 18
1.5. Organization of the thesis 21

Chapter 2. Theoretical Background

2.1. Evolution of interconnect systems 22
  2.1.1. Cu/barrier/low-k interconnect system 22
  2.1.2. Process developments for interconnect reliability 27
  2.1.3. 3rd generation of interconnect system 31
2.2 Thermodynamic tools for Co self-forming barrier 42
  2.2.1 Binary phase diagram 42

2.2.2 Ellingham diagram 42
2.2.3 Activity coefficient 43
2.3. Reliability of Interconnects 45
2.3.1. Current conduction mechanisms in dielectrics 45
2.3.2. Reliability test vehicles 50
2.3.3. Dielectric breakdown assessment 52
2.3.4. Dielectric breakdown mechanisms 55
2.3.5. Reliability test: VRDB and TDDB 56
2.3.6. Lifetime models 57

Chapter 3. Experimental Procedures

3.1. Thin film deposition 60
3.1.1. Substrate preparation 60
3.1.2. Oxidation 61
3.1.3. Co alloy deposition using DC magnetron sputtering 61
3.1.4. Annealing process 65
3.2. Thin film characterization 67
3.2.1. Sheet resistance 67
3.2.2. X-ray photoelectron spectroscopy (XPS) 68
3.3. Metal-Insulator-Semiconductor (MIS) device fabrication 70
3.3.1. Patterning using lift-off process 70
3.3.2. TDDB packaging 72
3.4. Reliability analysis 74
3.4.1. Electrical reliability analysis 74
3.4.2. Transmission electron microscopy (TEM) analysis 75

3.5. Computation 76

3.5.1 Factsage^{TM} calculation 76

3.5.2. Density Functional Theory (DFT) calculation 77

Chapter 4. Co Alloy Design for Advanced Interconnects

4.1. Material design of Co alloy self-forming barrier 78

4.1.1. Rule of thumb of Co-X alloy 78

4.1.2. Co alloy phase 80

4.1.3. Out-diffusion stage 81

4.1.4. Reaction step with SiO_2 dielectric 89

4.1.5. Comparison criteria 94

4.2. Comparison of Co alloy candidates 97

4.2.1. Thin film resistivity evaluation 97

4.2.2. Self-forming behavior using XPS depth profile analysis 102

4.2.3. MIS device reliability test 110

4.3 Summary 115

Chapter 5. Co-Cr Alloy Interconnect with Robust Self-Forming Barrier

5.1. Compatibility of Co-Cr alloy SFB process 117

5.1.1. Effect of Cr doping concentration 117

5.1.2. Annealing process condition optimization 119

5.2. Reliability of Co-Cr interconnects 122

5.2.1. VRDB quality test with Co-Cr alloys 122

5.2.2. Lifetime evaluation using TDDB method 141

5.2.3. Barrier mechanism using DFT 142
5.3. Summary 145

Chapter 6. Conclusion

6.1. Summary of results 148
6.2. Research perspectives 150

References 151

Abstract (In Korean) 166

Curriculum Vitae 169

LIST OF TABLES

Table 1.1 Scaling down of transistor and interconnect: In addition to the fact that transistors were continuously decreasing, the linewidth of the interconnects continued to decrease as well.

Table 2.1 Bulk resistivity (ρ_0) and the electron mean free path (λ) of alternative metal candidates.

Table 2.2 Comparison of current conduction mechanisms in dielectrics: electrode-limited conduction mechanism depends on the electrical properties (barrier height) at interface between electrode and dielectric and bulk-limited conduction mechanism depends only on the properties of dielectric itself. (i.e. trap level, spacing, density)

Table 2.3 Reliability test vehicles: damascene structure (MIM), metal-insulator-silicon planar capacitor structure (MIS), low-k planar capacitor (p-cap).

Table 2.4 Voltage acceleration models**.**

Table 3.1 Sputtering process parameters

Table 3.2 Process recipe of photolithography using AZ4330 photoresist.

Table 4.1 Modified rule of thumb for Co-X alloy self-forming barrier: resistivity, intermetallic compound formation, solubility, activity coefficient, diffusivity, oxide formation enthalpy, and reaction phase were used as the selection criteria for Co self-forming barrier.

Table 4.2 Solubility and intermetallic compound (IMC) information for 39 elements. Values were calculated using Factsage^{TM} software.

Table 4.3 Activity coefficient of each dopant in the Co matrix at 450 °C: dopants in the Co matrix are less stable when the activity coefficient is greater than 1. Activity coefficients were calculated using Factsage^{TM} software.

Table 4.4 Calculation of interfacial stable phase at annealing temperature (450 °C) using Factsage^{TM}: The thermodynamic stable phase of each element was calculated in binary system (M-SiO_2) and ternary system (M-SiO_2-Co).

Table 4.5 Comparison of Co alloy self-forming barrier (SFB) criteria: Comparison of SFB suitability of 9 dopant with 7 criteria.

Table 4.6 Interfacial stability phase after annealing (450 °C) using thermodynamic calculations for each alloy: Co-Cr, Co-Mn, Co-Zn.

Table 4.7 Comparison of Co alloy test results and self-forming barrier design rule (rule of thumb of Co-X alloy).

LIST OF FIGURES

Figure 1.1 (a) Schematic diagram of changes in users' electronic devices: in the 1990s, access to computers was very limited, but in the 2020s, semiconductor chips are being used not only for humans but also for things, (b) As the demand for semiconductors is rapidly increasing, the issue of chip shortage has continued from 2020 to the present.

Figure 1.2 History of transistor node technology: through continuous scaling down (Moore's law) of transistors, the gate delay speed of devices has been reduced.

Figure 1.3 Correlation between the number of transistors per chip and clock speed: Chip speed does not increase linearly even if transistors are continuously scaled down. Clock frequency is limited because issues such as thermal management and resistance-capacitance (RC) delay remain unresolved.

Figure 1.4 Very large system integration (VLSI) development diagram (1974 – 2020): Transistors are developed smaller in the following order: planar field-effect transistor (FET), FinFET, Gate All Around (GAA) FET, and Multi-Bridge Channel (MBC) FET. On the other hand, interconnect has been developed in the direction of increasing stacking layers from narrow interconnects to wide interconnects in consideration of transistor connection and system resistance.

Figure 1.5 Changes in chip architecture with technology nodes (2007 ~ 2016): when looking at the cross-section of a chip, the transistor occupies a very narrow area, while the interconnect area is growing in line with the development of node technology. It shows that the importance of interconnect technology is becoming more important day by day in chip architecture as well.

Figure 1.6 Driving force of interconnect system evolution, "*Performance*": (a) It is very important to lower the RC delay of the interconnect in order to improve "chip performance". In order to secure low RC delay, it is necessary to develop a low resistivity metal and a low dielectric constant dielectric constant. In other words, material development is very important because RC delay is highly dependent on material.

Figure 1.7 The change from Al/SiO_2 system to Cu interconnect is an important material change to reduce RC delay.

Figure 1.8 Driving force of interconnect system evolution, "*Reliability*": (a) current density with technology node development, the operating environment is getting harsher as chip scaling down continues, (b) there are various reliability issues in interconnect systems, but dielectric breakdown is the biggest problem as the mechanical properties of dielectrics continue to weaken in recent years.

Figure 1.9 Driving force of interconnect system evolution: the interconnect material system has changed the Cu/barrier/low-k system from Al/SiO_2, and research on the beyond Cu interconnect system is in progress worldwide. It is self-evident that research on materials required in the upcoming era of non-Cu interconnects is a low resistance and dielectric constant materials that can reduce RC delay and robust barrier materials that can ensure high reliability even in harsh operating environments.

Figure 1.10 Driving force of beyond Cu interconnect, "*Size effect*": the electron mean free path of Cu is 39 nm, and the resistivity increases significantly when the linewidth becomes thinner than 39 nm. When the electron moves in the damascene structure, the effect of side wall and grain boundary scattering increases and the effective resistivity increases significantly.

Figure 1.11 Driving force of beyond Cu interconnect, “*Metal and barrier system”*: (a) although Cu interconnect has high effective resistivity, pure Cu is still effective for interconnect because the resistance of pure Cu is very low, (b) when the resistivity of the barrier layer of the interconnect is taken into consideration, the resistivity of the Cu/TaN system greatly increases as the linewidth becomes smaller.

Figure 1.12 Driving force of beyond Cu interconnect, “*Barrier thickness effect*”: A barrier is absolutely necessary to secure reliability, but it is necessary to minimize the thickness of the barrier in order to minimize the RC delay. It is known that robust reliability can be secured only when the TaN barrier is at least 2.5 nm thick.

Figure 1.13 Driving force of beyond Cu interconnect, “Extrinsic failure behavior of Co": the extrinsic failure behavior of pure Co was first reported in 2017. This is the same phenomenon as the extrinsic failure caused by Cu ion diffusion/drift in Cu interconnects, and a diffusion barrier to prevent metal ions is essential for reliable interconnects.

Figure 1.14 Requirements of diffusion barrier: (a) Considering the interconnect reliability aspect, a diffusion barrier that can prevent the movement of metal ions under E-field is absolutely necessary. (b) it has been reported that the area fraction of barriers in Cu M1 interconnects at 24 nm pitch is greater than 40%. Barrier requires that the diffusion barrier be thin and highly reliable.

Figure 1.15 When the self-forming barrier methodology is used, a very thin diffusion barrier can be formed, and high reliability can be secured. In early 2010, the $MnSi_xO_y$ self-forming barrier was suggested using Cu-Mn alloy, securing both performance and reliability.

Figure 2.1 Changes in the interconnect material system: Since 1998, as the Cu interconnect system has changed, barrier and capping layer materials have been added. These new materials have resulted in high TDDB and EM reliability. Changes in interconnect materials indicate the need to develop a corresponding material system.

Figure 2.2 Key milestones in Cu BEOL manufacturing: important technologies for Cu interconnect development include the introduction of low-k materials that can improve performance and diffusion barrier and capping layer materials that can significantly improve reliability.

Figure 2.3 In the case of dielectric films, researchers have continued to develop materials that control porosity based on SiO_2 in order to reduce the dielectric constant.

Figure 2.4 Ta/TaN barrier is proposed to prevent Cu ion diffusion (bulk dielectric diffusion) in Cu interconnects.

Figure 2.5 In order to improve Cu electromigration (EM) characteristics and to enhance the interficial adhesion energy between dielectric and capping layers, capping layer materials are continuously being developed.

Figure 2.6 Comparison of interconnect reliability technologies: alloy, ALD, self-forming barrier (SFB), and a-BN methodologies have been used to improve reliability. It is predicted that ALD and SFB, which can form very thin barriers, are most suitable as the linewidth becomes narrower.

Figure 2.7 Self-forming barrier (SFB) technology: a Mn silicate self-forming barrier has been reported in the annealing using Cu-Mn alloy. It showed low resistance rise and excellent e-field resistance.

Figure 2.8 Process comparison of conventional barrier and self-forming barrier: (a) two-step PVD process, (b) one-step SFB process.

Figure 2.9 Rule of thumb for Cu-Mn alloys proposed by J. Koike of the University of Tokyo.

Figure 2.10 A history of interconnect system innovation: 1st generation Al/SiO_2, 2nd generation Cu/low-k, 3rd generation beyond Cu systems.

Figure 2.11 Limitation of Cu damascene interconnects: as sidewall scattering and grain boundary scattering increased, resistivity higher than bulk resistivity appeared.

Figure 2.12 Surface scattering and grain boundary scattering: As the linewidth decreases, materials with a long mean free path have a greater scattering effect.

Figure 2.13 The lower the product of the bulk resistivity (ρ_0) and the electron mean free path (λ), the less the scattering effect.

Figure 2.14 Technology roadmap of logic devices (2020 - 2034) published by International Roadmap for Devices and Systems (IRDS).

Figure 2.15 Non-Cu Interconnects: effective resistivity of Co and Ru.

Figure 2.16 Advantages and disadvantages of alternative metals, Co and Ru.

Figure 2.17 Ru interconnect research results of integrated device manufacturers (IDM): imec's 10nm Ru evaluation and GlobalFoundries and IBM's 24nm Ru evaluation.

Figure 2.18 Co interconnect research by IDMs: intel’s 10nm Co integration, Samsung’s 10nm Co demonstration, and AMAT’s 17nm Co interconnect test.

Figure 2.19 Co/TiN metal/barrier system proposed by Applied Materials: Resistance crossover between Co/TiN and Cu/Ta/TaN systems: advantages of Co and ALD diffusion barriers.

Figure 2.20 Co/ALD TiN system proposed by AMATs shows better TDDB properties than Cu/Ta/TaN.

Figure 2.21 Ellingham diagram for Co alloy self-forming barrier (left), Ellingham diagram published by MIT. (right)

Figure 2.22 Activity coefficient calculation in alloy.

Figure 2.23 Conduction mechanisms in dielectric films.

Figure 2.24 Electrode-limited conduction mechanisms: Schottky emission, Fowler-Nordheim tunneling, thermionic-field emission.

Figure 2.25 Bulk-limited conduction mechanisms: Poole-Frenkel emission, hopping conduction, Ohmic conduction.

Figure 2.26 Current conduction mechanism in dielectric and identification of current conduction in damascene Cu interconnects.

Figure 2.27 Test vehicles: MIS vs. MIM.

Figure 2.28 Dielectric breakdown assessment: constant voltage stress (CVS), ramped voltage stress (RVS), constant current stress (CCS), ramped current stress (RCS), bipolar applied field stress (BAFS).

Figure 2.29 Dielectric breakdown mechanisms: extrinsic breakdown; percolation paths are formed extrinsically due to Cu ions, intrinsic breakdown; broken bonds by dipole-dipole interaction or injected electrons from cathode can form conductive paths.

Figure 2.30 Dielectric breakdown mechanisms: the gradual increase in leakage current was observed in Cu/SiO$_2$ sample under BTS, while sample of Al/SiO$_2$ was not.

Figure 2.31 Reliability test methods: Ramp voltage stress (VRDB) and time dependent dielectric breakdown (TDDB)

Figure 2.32 TDDB modeling: The dielectric breakdown lifetime has dependence on electric field, temperature, and area.

Figure 2.33 TDDB Lifetime assessment: VRDB (Step 1), TDDB (Step 2), Weibull plotting (Step 3), voltage acceleration modeling (Step 4).

Figure 2.34 TDDB E-field acceleration models: accurate lifetime prediction of devices using various acceleration models is still controversial.

Figure 3.1 Oxide thickness measurement using an ellipsometer: (a) dry oxidation process; 100 nm SiO_2 was deposited using a SELTRON (SHF-150). (b) CVD TEOS was deposited using Applied Material Korea (P-5000 IV).

Figure 3.2 Chip on target deposition: Co alloy thin films and MIS samples were deposited by placing a dopant chip on the Co target.

Figure 3.3 Target deposition rate of pure Co: confirmation of deposition rate with deposition uniformity (center to edge) and plasma powers (50W, 100W, 150W).

Figure 3.4 Co-Cr alloy deposition rate change: the deposition rate was investigated according to the number of Cr chips. (1 ea ~ 4 ea)

Figure 3.5 Co alloy deposition rate investigation: thickness check of 8 different dopant metals. (100 W, 4 mTorr, 10 minutes)

Figure 3.6 Vacuum furnace: thin film samples were subjected to vacuum annealed (< 0.0013 Pa) for surface diffusion.

Figure 3.7 Wafer-level heat treatment furnace: MIS samples were subjected to annealed under N_2 atmosphere for barrier self-forming.

Figure 3.8 Sheet resistance measurement using 4-point probe method.

Figure 3.9 Sheet resistance measurement in bilayer: (a) in case of alloy, the sheet resistance increases due to more scattering sites, but it is assumed that it is a single layer. (b) in the case of a self-forming barrier, it should be calculated considering that it is a bilayer. However, the data should be compared considering whether the dopant is present in the mother phase and whether the doping concentration is the same.

Figure 3.10 XPS analysis area and pattern sample size problem: It is difficult to get accurate quantitative analysis results from pattern MIS structure.

Figure 3.11 Fabrication flow of MIS device: all MIS devices are fabricated using a lift-off lithography process.

Figure 3.12 Process flow of lift-off photolithography.

Figure 3.13 TDDB packaging: after attaching the die to the ceramic package using silver paste, Au wiring was performed.

Figure 3.14 VRDB and TDDB measured under constant voltage stress are measured under voltage ramping stress.

Figure 3.15 TEM sampling with focused ion beam (FIB).

Figure 3.16 Analytical TEM with EDS analysis.

Figure 3.17 Factsage^{TM}: phase diagram, reaction, and equilibrium calculation were used to get thermodynamic properties of Co alloy systems.

Figure 4.1 Self-forming barrier behaviors (3-step): the rule of thumb for Co-X alloy was designed by dividing the self-forming barrier behavior into three steps.

Figure 4.2 Bulk resistivity of CMOS compatible metals: among materials with resistivity lower than 20 μΩ·cm, materials with a melting point higher than Co are marked in blue.

Figure 4.3 Change in resistivity with alloying element concentration.

Figure 4.4 Binary phase diagram of Co-Cr: calculate the solubility limit of Cr with annealing temperature (450 °C) and proceed the same for all other dopants.

Figure 4.5 Confirmation of solubility of Co-X alloy dopant at 450 °C and intermetallic compound (IMC) formation: There are 4 cases regarding solubility and intermetallic compound. low solubility and Cr not forming IMC, Mn having high solubility but not forming IMC, low solubility and forming IMC Al, high solubility and Sn from which IMC is formed.

Figure 4.6 Solid solubility limit graph with bulk resistivity: when intermetallic compound (IMC) is formed, it is indicated in red, and when it is not formed, it is indicated in blue. The limit of solubility in Co at 450 °C is used.

Figure 4.7 Solute diffusivity graph with Solid solubility limit: It shows diffusivity values of solute in FCC Co matrix at 1500K. Co self-diffusivity is 6.6 × 10^{-16} m^2/s.

Figure 4.8 Stage of self-forming diffusion barrier: process of dopants reacting with SiO$_2$ dielectric after out-diffusion.

Figure 4.9 Ellingham diagram: Self-forming barrier materials should have descent oxidation tendency. Reaction with oxygen on SiO_2 should occur at an appropriate level.

Figure 4.10 Changes in resistivity of pure Co with annealing temperature (150 °C – 450 °C) and time (30 minutes – 10 hours): data before annealing were used as room temperature data.

Figure 4.11 Resistivity change with annealing temperature (150 °C – 450 °C) and time (30 minutes – 10 hours): Based on the design rule, the three most suitable Co alloys (Co-Cr, Co-Fe, Co-Zn) were investigated.

Figure 4.12 Resistivity change with annealing temperature (150 °C – 450 °C) and time (30 minutes – 10 hours): Co alloys (Co-Mn, Co-Ni, Co-Sn) were investigated.

Figure 4.13 Resistivity change with annealing temperature (150°C – 450°C) and time (30 minutes – 10 hours): Co alloys (Co-Al, Co-Cu, Co-Mg) were investigated.

Figure 4.14 Observation of change in resistivity of Co alloy thin films before and after annealing: In the case of pure Co thin film, it drops to the level of bulk resistivity after heat treatment.

Figure 4.15 XPS depth profiles of the as-deposited and annealed Co alloy thin films: Co-Cr, Co-Zn, Co-Mn.

Figure 4.16 XPS depth profiles of Co-Ni, Co-Fe and energy dispersive X-ray spectroscopy (EDS) mapping of Co-Fe alloy.

Figure 4.17 XPS depth profile of annealed Co alloy thin film: y-axis enlarged to confirm the top surface and SiO_2 interface composition.

Figure 4.18 Behavior of Co alloying elements at SiO_2 interface after annealing: Zn and Mn exist inside SiO_2 after heat treatment, but Cr exists only at the interface, not inside SiO_2.

Figure 4.19 Schematic diagram of barrier formation when self-forming barrier is applied to low dielectric material (SiCO:H, airgap, etc.): Since the driving force of the forming barrier is diffusion and oxide formation, conformal barrier formation will be possible than PVD barrier process.

Figure 4.20 Binding energy analysis of Co-Cr alloy before and after annealing: In the case of as-deposited samples, comparison of binding energy in the top surface region (① ~ ③), and comparison of binding energy in the surface diffused region (① ~ ③) for annealing samples.

Figure 4.21 Diffusion barrier effect: The leakage current shape is different in pure Co and Co sample to which the barrier is applied, meaning that the dielectric current conduction is different, and the breakdown voltage is also greatly improved.

Figure 4.22 VRDB analysis by pure Co and Co alloy: Electrical failure (breakdown voltage) was defined when leakage current increased over 10^{-8} A, and I-V analysis was performed on a 125 °C stage chuck.

Figure 4.23 Comparison of breakdown voltage of pure Co and Co alloy: 12 times per sample were measured, and the median value was used among them.

Figure 4.24 Cumulative distribution function (CDF) plot of breakdown voltage of pure Co and Co alloys.

Figure 4.25 TEM-EDS mapping image of Co-1.6 at% Cr alloy thin film: When comparing the electrical analysis result and EDS image, it was confirmed that Cr oxide barrier was formed after surface diffusion of Cr at the SiO_2 interface.

Figure 4.26 Material design of Co alloy self-forming barrier: Co-Cr alloy shows excellent barrier (Cr oxide) quality and superior reliability compared to pure Co.

Figure 5.1 Process temperature for integrated chips (IC) manufacturing processes: lowering the thermal budget of interconnects from 450 °C to under 400 °C.

Figure 5.2 Resistivity evaluation of Co-Cr thin films: Doping concentrations up to 2 at% Cr are appropriate because low resistivity can be obtained.

Figure 5.3 Change in resistivity of Co-Cr alloy thin film according to annealing conditions (temperature and time) and Cr doping concentration: temperature range (150 °C – 450 °C, 100 °C/step), annealing time range (0.5 hours, 2 hours, 10 hours), Cr doping concentration range (~ 7.5 at%).

Figure 5.4 Annealing effect of Co-Cr alloy thin films: The effect of annealing temperature, time, and Cr doping concentration was confirmed.

Figure 5.5 Co-Cr alloy resistivity change in low doping concentration region: 0.4 at% Cr, 0.9 at% Cr, 1.6 at% Cr.

Figure 5.6 Change in breakdown voltage of as-deposited pure Co and Co-Cr alloy MIS structures using cumulative distribution function.

Figure 5.7 I-V characteristics of as deposited samples: pure Co and Co-Cr alloy (0.4 at% - 7.5 at%).

Figure 5.8 I-V characteristics of pure Co and Co alloys after annealing (450 °C): Electrical failure (breakdown voltage) was defined when leakage current increased over 10^{-8} A, and I-V analysis was performed on a 125 °C stage chuck.

Figure 5.9 Comparison of breakdown voltage between pure Co and Co-Cr alloys using the median value for each MIS sample.

Figure 5.10 Comparison of the average breakdown voltage of pure Co and Co-Cr alloys: The average value and standard deviation are calculated using the values measured 9 times for each sample.

Figure 5.11 Cumulative distribution function (CDF) plot of breakdown voltage of pure Co and Co alloys after annealing.

Figure 5.12 I-V characteristic change with Cr doping concentration (0.4 at% - 7.5 at%): observed from 1st breakdown to 3rd breakdown.

Figure 5.13 EDS line scan profile across the 0.4 at% Cr sample interface.

Figure 5.14 EDS line scan profile across the 7.5 at% Cr sample interface.

Figure 5.15 High-resolution transmission electron microscopy (HR-TEM) images: (a) 0.4 at% Cr and (b) 7.5 at% Cr samples.

Figure 5.16 EDS mapping images with FE-TEM: Co, Cr, O, and Si elements were analyzed at each interface: (a) 0.4 at% Cr and (b) 7.5 at% Cr samples.

Figure 5.17 Changes in I-V characteristics in the low Cr doping region (0.4 at%, 0.9 at%, 1.6 at%) with annealing temperature (250 °C, 350 °C, 450 °C).

Figure 5.18 Breakdown voltage change with annealing temperatures (250 °C, 350 °C, 450 °C) and Cr doping concentration (0.4 at%, 0.9 at%, 1.6 at%).

Figure 5.19 CDF plot of breakdown voltage change with annealing temperatures (250 °C, 350 °C, 450 °C) and Cr doping concentration (0.4 at%, 0.9 at%, 1.6 at%).

Figure 5.20 Difference between damascene and MIS structure.

Figure 5.21 Size (metal thickness) effect of Co-Cr alloys with MIS structure.

Figure 5.22 CDF plots of 20 nm thick pure Co and Co alloy samples

Figure 5.23 Co-Cr layer thickness effect: CDF plot shows breakdown voltage changes when metal linewidth is 150 nm and 20 nm.

Figure 5.24 EDS mapping images for each 20 nm Co-Cr alloy (0.4 at% Cr - 7.5 at% Cr) using high resolution EDS.

Figure 5.25 HR-TEM images for 20 nm Co-Cr alloys (0.4 at% Cr - 7.5 at% Cr).

Figure 5.26 TOF-SIMS depth profile of Co-0.4at% Cr alloy after annealing at 450 °C for 2 hours.

Figure 5.27 TOF-SIMS depth profile of Co-7.5at% Cr alloy after annealing at 450 °C for 2 hours.

Figure 5.28 Selective Cr oxidation behaviors in CoCr alloy: arrows indicate the driving force direction of each element in the oxidation process, and the figure on the right indicates the displacement of each atom after MD and geometry relaxation.

Figure 5.29 TDDB Weibull plot with doping concentration: Analysis was performed at 200 °C and E-field variations (6, 7, 8 MV/cm) with 150 nm thick Co-Cr alloys.

Figure 5.30 TDDB Weibull plot with E-field: Analysis was performed at 200 °C.

Figure 5.31 Co diffusion in TiN lattices (upper) and Cr_2O_3 lattices (lower).

Figure 5.32 Co diffusion barrier difference in TiN (interstitial-to-interstitial) and Cr_2O_3 (vacancy-to-interstitial).

Figure 6.1 The era of hyper-scaling in electronics: materials are one of the keys to moving forward beyond current VLSI systems.

CHAPTER 1

Introduction

1.1. Scaling down of VLSI systems

At the point of living in the present, it can be said that we are living with semiconductors. As such, semiconductors have become very important in our lives. As shown in **Fig. 1.1 (a)**, personal computers (PCs), which were available in large groups such as schools in the 1990s, became widespread enough to be easily found in homes in the 2000s. Around the 2010s, mobile devices capable of exchanging large amounts of information such as e-mail, Internet surfing, and music became easily accessible to individuals. Currently, in 2021, not only individual electronic devices but also electronic devices are being combined with objects. We live in a world where we can feel the world becoming digital like virtual reality (VR), augmented reality (AR), and Internet of Things (IoT). [1-3] As shown in **Fig. 1.1 (b)**, from 2020, the non-contact era has suddenly arrived due to COVID-19, resulting in a sharp increase in demand for semiconductors. As a result, the chip shortage issue has not been resolved to this day.

[4-6] This aspect alone shows that the importance of semiconductor technology and industry has become more and more important.

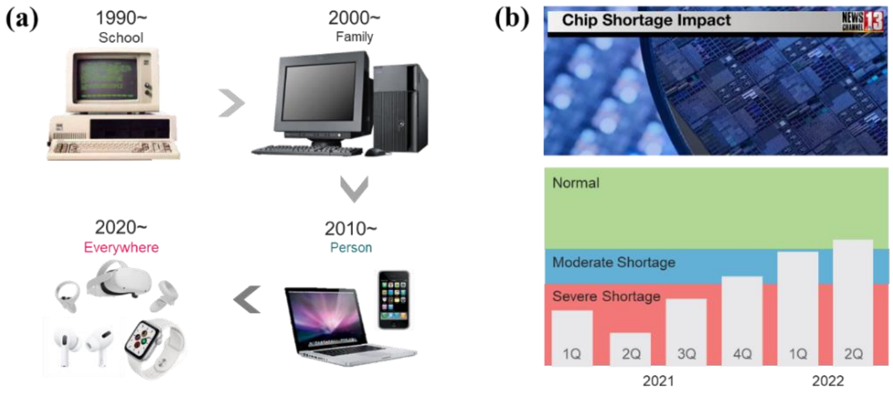

(a)
1990~
School
2000~
Family
2010~
Person
2020~
Everywhere
(b)
Chip Shortage Impact
Normal
Moderate Shortage
Severe Shortage
1Q
2Q
3Q
4Q
1Q
2Q
2021
2022

Figure 1.1 (a) Schematic diagram of changes in users' electronic devices: in the 1990s, access to computers was very limited, but in the 2020s, semiconductor chips are being used not only for humans but also for things[1-3], (b) As the demand for semiconductors is rapidly increasing, the issue of chip shortage has continued from 2020 to the present.[4-6]

If you look at **Fig. 1.2**, you can see the history of transistor node technology at a glance. [7-10] Through continuous scaling down of transistors, commonly known as Moore's law, it was possible to achieve device performance improvement, form factor, and cost reduction. In 1987, after 30 years of 3 μm node technology, transistors have continued to shrink below the 5 nm node. It has been reduced by more than 600 times! In other words, the development of very large system integration (VLSI) system technology has played a pivotal role in the transition to the digital world.

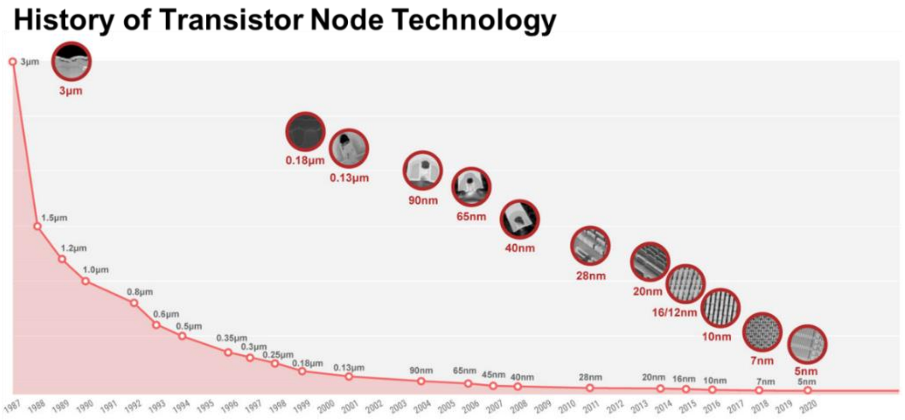


Figure 1.2 History of transistor node technology: through continuous scaling down (Moore's law) of transistors, the gate delay speed of devices has been reduced.[7-10]

However, the transistor scaling down in the VLSI system did not have a continuous linear relationship with the clock speed improvement, which is a performance indicator of the device. As can be seen in **Fig. 1.3**, chip transistors have increased in log scale, but clock speed has not improved significantly since around 2005. [10-12] Paradoxically, thermal budget, *RC* delay, and memory latency significantly increased as transistor density and clock speed were improved. As power consumption has increased significantly, heat caused by joule heating due to increase in power density has become so important for thermal management that device performance is limited. And the operating speed of the chip is affected by the resistance and capacitance of the interconnects that transmits signals and power. As the size of the chip decreases, the interconnects become thinner, and the resistance increases. Also, when the metal line gets closer each other, the electric capacity also increases significantly. In other words, as the RC product increases, the interconnect delay also increases. Lastly, in the Von Neumann architecture, as the speed difference between the central processing unit (CPU) and memory increases, the total speed is inevitably limited, so a systematic approach is required for continuous VLSI system scaling down.

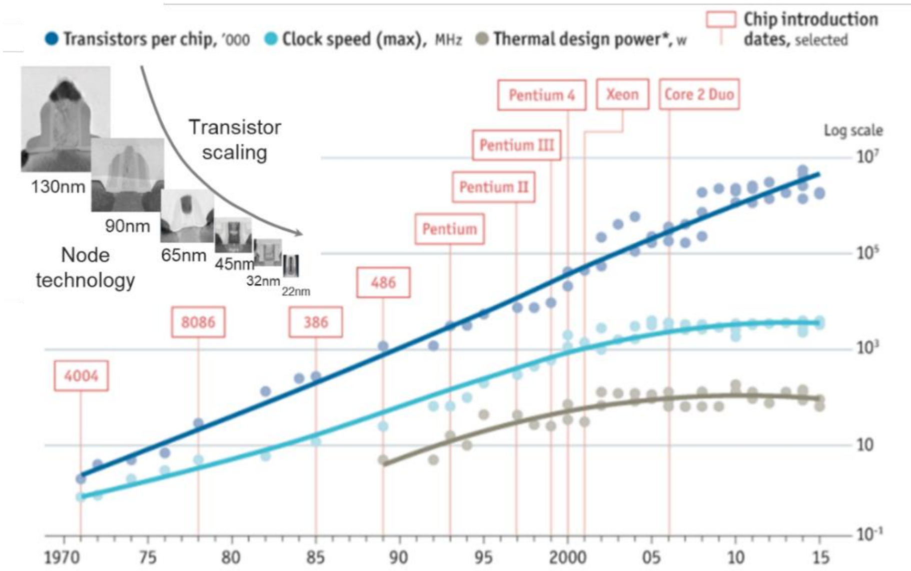


Figure 1.3 Correlation between the number of transistors per chip and clock speed: Chip speed does not increase linearly even if transistors are continuously scaled down. Clock frequency is limited because issues such as thermal management and resistance-capacitance (RC) delay remain unresolved.[10-12]

Let us take a look at how the VLSI system has evolved once again. As shown in **Fig. 1.4** and **Fig. 1.5**, transistors are being developed smaller in the order of planar Field-effect transistor (FET), FinFET, Gate All Around (GAA) FET, and Multi-Bridge Channel (MBC) FET. [8-9, 13-14] On the other hand, interconnect has been developed in a direction in which stacking layers are gradually increasing in order to connect more transistors and lower system resistance. In particular, considering that the currently applied interconnect structure consists of 10 to 16 stacking layers, it can be noticed that interconnect has as much influence on chip performance as the large area it occupies on the chip. [15-17] In **Table 1.1**, not only the fact that the transistor is continuously decreasing, but also the linewidth of the interconnect continues to decrease. It has decreased to 48 nm pitch based on 5 nm node technology. [8-9, 13-14, 18] The fact that the linewidth of the interconnects continues to narrow is not an important fact in a wide pitch area. However, as the interconnect RC delay crossovers with the RC delay of the transistor, it began to be highlighted. Consequently, breakthroughs in interconnect technology as well as transistor scaling down are needed to improve chip performance.

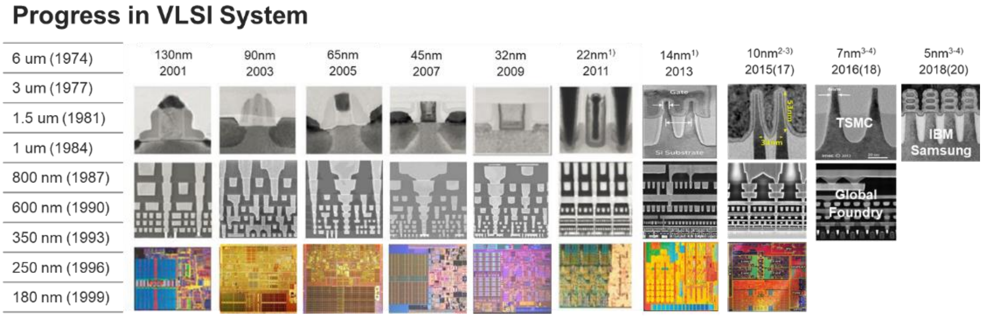

Progress in VLSI System
6 um (1974)
3 um (1977)
1.5 um (1981)
1 um (1984)
800 nm (1987)
600 nm (1990)
350 nm (1993)
250 nm (1996)
180 nm (1999)
130nm 2001
90nm 2003
65nm 2005
45nm 2007
32nm 2009
22nm1) 2011
14nm1) 2013
10nm2-3) 2015(17)
7nm3-4) 2016(18)
5nm3-4) 2018(20)
TSMC
IBM Samsung
Global Foundry

Figure 1.4 Very large system integration (VLSI) development diagram (1974 – 2020): Transistors are developed smaller in the following order: planar field-effect transistor (FET), FinFET, Gate All Around (GAA) FET, and Multi-Bridge Channel (MBC) FET. On the other hand, interconnect has been developed in the direction of increasing stacking layers from narrow interconnects to wide interconnects in consideration of transistor connection and system resistance.[8-9, 13-14]

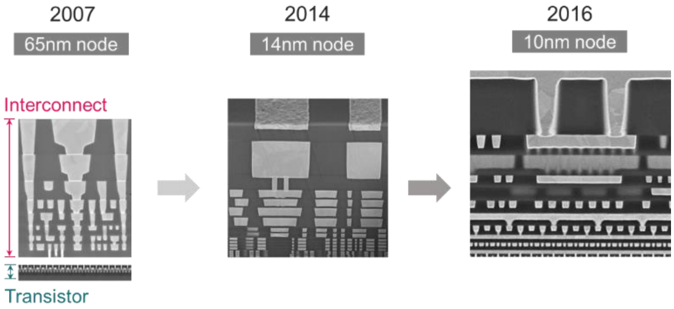


Figure 1.5 Changes in chip architecture with technology nodes (2007 ~ 2016): when looking at the cross-section of a chip, the transistor occupies a very narrow area, while the interconnect area is growing in line with the development of node technology. It shows that the importance of interconnect technology is becoming more important day by day in chip architecture as well.[15-17]

Table 1.1 Scaling down of transistor and interconnect: In addition to the fact that transistors were continuously decreasing, the linewidth of the interconnects continued to decrease as well.[8-9,13-14,18]

Technology node (nm)	130	90	65	45	32
Transistor density (MTr/mm^2)	-	-	-	-	-
Transistor Fin Pitch (nm)	319	220	210	160	112.5
Interconnect Pitch (nm)	345	260	220	180	112.5

Technology node (nm)	22	14	10	7	5
Transistor density (MTr/mm^2)	-	37.5	100.76	96.5	173
Transistor Fin Pitch (nm)	60	42	34	40	30
Interconnect Pitch (nm)	90	52	54	-	48

1.2 Driving force of interconnect system development

Interconnects has been continuously developed with transistor scaling down for decades. The driving force of interconnect research and development has been largely conducted from two perspectives: "*performance*" and "*reliability*". For example, by changing from Al to Cu interconnect, performance was achieved, and materials and processes that ensure reliability were developed. [19-20]

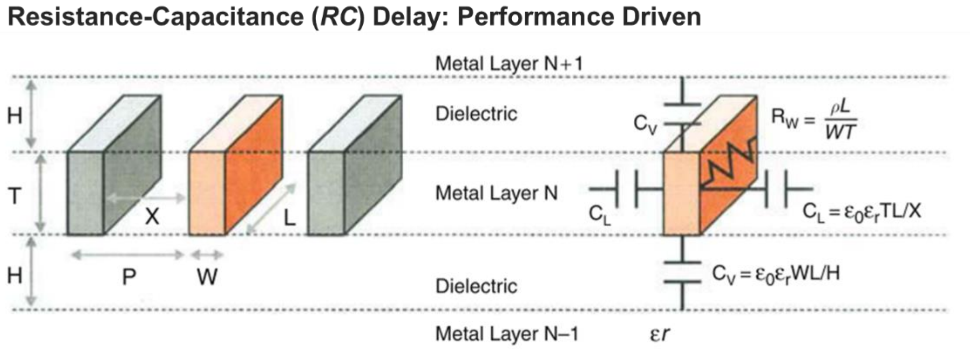

Resistance-Capacitance (*RC*) Delay: Performance Driven
Metal Layer N+1
Dielectric
Metal Layer N
Dielectric
Metal Layer N–1
H
T
H
X
L
P
W
C_V
$R_W = \frac{\rho L}{WT}$
C_L
$C_L = \varepsilon_0 \varepsilon_r TL/X$
$C_V = \varepsilon_0 \varepsilon_r WL/H$
εr

Figure 1.6 Driving force of interconnect system evolution, "***Performance***": (a) It is very important to lower the RC delay of the interconnect to improve "chip performance". To secure low RC delay, it is necessary to develop a low resistivity metal and a low dielectric constant dielectric constant. In other words, material development is very important because RC delay is highly dependent on material.[19-20]

As shown in **Fig. 1.6** and **Eq. 1.1**, resistance-capacitance (*RC*) in general interconnect can be calculated as follows. Each term is defined as follows. [19]

$$\begin{aligned} \boldsymbol{RC} &= \mathbf{2R}(\boldsymbol{C_V} + \boldsymbol{C_L}) \\ &= \left[\frac{2\rho L}{WT}\right]\left[\left\{\frac{\varepsilon_0\varepsilon_r WL}{H}\right\} + \left\{\frac{\varepsilon_0\varepsilon_r TL}{X}\right\}\right] \\ &= \left[\left\{\frac{2\rho\varepsilon_0\varepsilon_r L}{WT}\right\}\left\{\frac{WL}{H} + \frac{TL}{X}\right\}\right] \\ &= 2\rho\varepsilon_0\varepsilon_r\left(\frac{L^2}{TH} + \frac{L^2}{WX}\right) \end{aligned} \tag{1.1}$$

Where,

R = Resistance of the interconnect

C_V= Interlayer capacitance, C_L = Intra-layer capacitance

ρ = Resistivity of the interconnect metal

L= Length of the interconnect, W=Width of the interconnect

T = Thickness of the metal layer = H_{int}

ε_0 = The permittivity of space

ε_r = The relative permittivity of the dielectric

H= Height of the dielectric layer = H_d

X= Spacing between adjacent interconnects

P = Pitch of the line

$$RC\ delay\ [s] = 2\rho\varepsilon_0\varepsilon_r\left(\frac{L^2}{TH} + \frac{L^2}{WX}\right) \tag{1.2}$$

As in **Eq. 1.2**, *RC* is defined as a time constant and is determined with the resistivity of the metal, the permittivity of the dielectric, and the geometric term. Considering that the geometric term is a constant determined at the design stage, the only way to reduce the *RC* delay of an interconnects is to improve a material using a low resistivity metal and a low dielectric constant dielectric. As shown in **Fig. 1.7**, the gate delay continues to decrease as node technology shrinks, but in the case of Al/SiO_2 interconnects, the *RC* delay increases dramatically. [21] In order to solve this problem, Cu interconnect technology has been proposed.

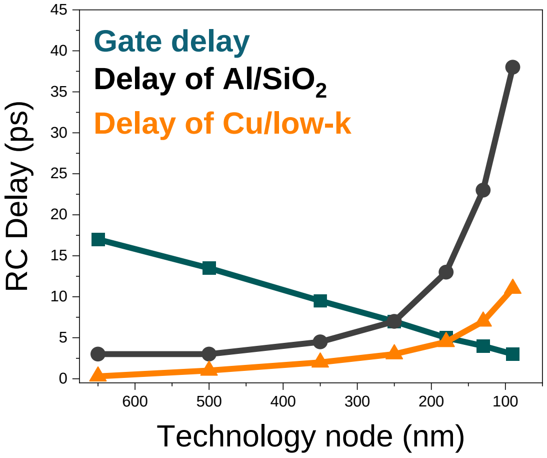


Figure 1.7 The change from Al/SiO_2 system to Cu interconnect is an important material change to reduce RC delay.[21]

As shown in **Fig. 1.8 (a)** and **(b)**, the narrower the interconnect linewidth, the more severe the operating environment is, so numerous reliability issues appear. For example, electromigration (EM), poor etch selectivity, and poor adhesion strength with surface were observed using metal Cu. As a result, new processes such as capping layers (Si based and metal based) and liners have been developed. In addition, problems such as time dependent dielectric breakdown (TDDB), poor thermal stability, tensile stress, poor cohesive strength, and low Young’s modulus and hardness have been reported while using low-k materials. TDDB, which is an interaction problem between Cu showing high diffusivity and low-k dielectric having weak mechanical properties, is recently reported as the biggest reliability issue. [22-23] In other words, the future direction of interconnect development requires a comprehensive material design considering not only metal but also dielectric.

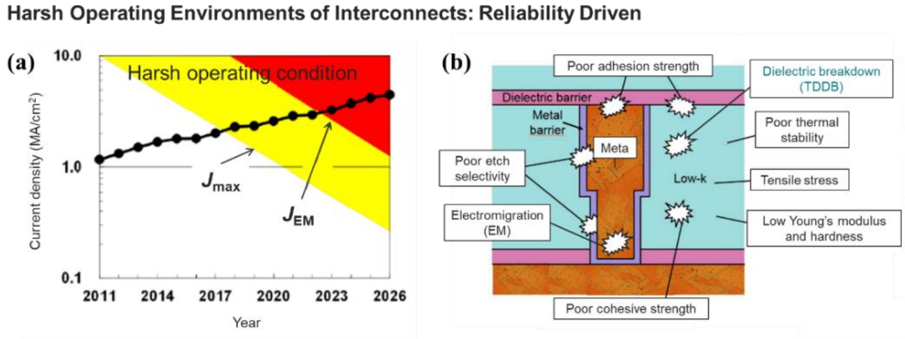


Figure 1.8 Driving force of interconnect system evolution, "***Reliability***": (a) current density with technology node development, the operating environment is getting harsher as chip scaling down continues, (b) there are various reliability issues in interconnect systems, but dielectric breakdown is the biggest problem as the mechanical properties of dielectrics continue to weaken in recent years.[22-23]

1.3 Driving force of beyond Cu interconnects

Let us look at what the driving force will be in the development of next-generation interconnects that goes beyond Cu interconnects. **Fig. 1.9** shows the change of interconnect materials system with node technology. First, the change from Al to Cu interconnects was the reason for higher performance and electromigration (EM) problems. As Cu interconnects was applied, *RC* delay could be greatly improved, and Cu diffusion induced reliability could be solved through Ta/TaN barrier and capping layer (dielectric barrier) processes. [23-28]

Then, let us think about what kind of research is needed to apply Co and Ru, which are spotlighted as beyond Cu (non-Copper) materials, to the next interconnects. It was necessary to approach it from the point of view of the material systems. The driving force for the development of next-generation interconnect systems has been summarized into four major categories (*size effect*, *metal/barrier system*, *barrier thickness effect*, and *extrinsic failure behavior*).

First, the *size effect* appears as the line width narrows. For more information on effective resistivity, please refer to 2.1 evolution of interconnect system, chapter 2. As shown in **Fig. 1.10**, the electron mean free path of Cu is 39 nm, and the effective resistivity increases significantly in Cu interconnects thinner than 39 nm. In the dual damascene structure, the effect of side wall and grain boundary scattering increases, resulting in higher effective resistivity than bulk resistivity. [16, 29-32] Generally, the resistivity of a material is known as a constant!

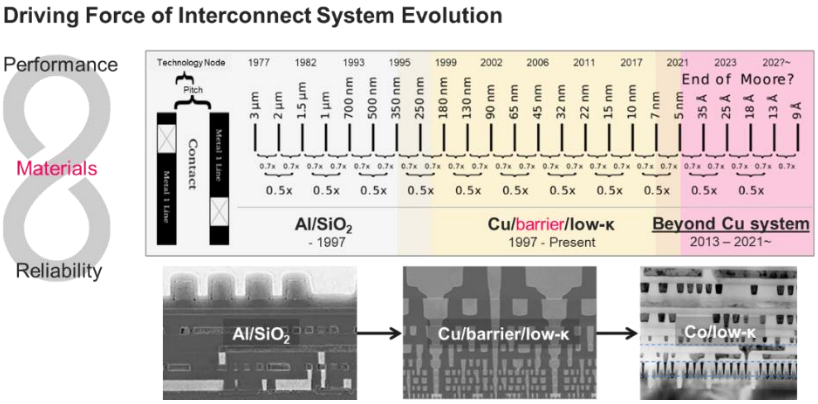

Driving Force of Interconnect System Evolution
Performance
Materials
Reliability
Technology Node
Pitch
Metal 1 Line
Contact
Metal 1 Line
1977
1982
1993
1995
1999
2002
2006
2011
2017
2021
2023
2027~
End of Moore?
3 µm
2 µm
1.5 µm
1 µm
700 nm
500 nm
350 nm
250 nm
180 nm
130 nm
90 nm
65 nm
45 nm
32 nm
22 nm
15 nm
10 nm
7 nm
5 nm
35 Å
25 Å
18 Å
13 Å
9 Å
0.7x
0.5x
Al/SiO$_2$
- 1997
Cu/barrier/low-κ
1997 - Present
Beyond Cu system
2013 – 2021~
Al/SiO$_2$
Cu/barrier/low-κ
Co/low-κ

Figure 1.9 Driving force of interconnect system evolution: the interconnect material system has changed the Cu/barrier/low-k system from Al/SiO$_2$, and research on the beyond Cu interconnect system is in progress worldwide. It is self-evident that research on materials required in the upcoming era of non-Cu interconnects is a low resistance and dielectric constant materials that can reduce RC delay and robust barrier materials that can ensure high reliability even in harsh operating environments.[23-28]

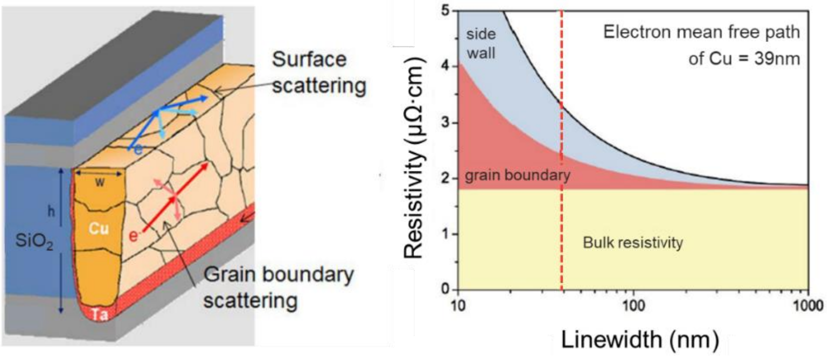


Figure 1.10 Driving force of beyond Cu interconnect, ***"Size effect"***: the electron mean free path of Cu is 39 nm, and the resistivity increases significantly when the linewidth becomes thinner than 39 nm. When the electron moves in the damascene structure, the effect of side wall and grain boundary scattering increases and the effective resistivity increases significantly.[16,29-32]

Nevertheless, as shown in **Fig. 1.11 (a)**, since the bulk resistivity of Cu is very low, even if the linewidth is narrowed, it is lower than the resistivity of platinum metal group (PGM) materials, which are known as next-generation interconnect materials. [33-34] Of course, since it is the result of the size effect of the epitaxial metal layer, the influence on the damascene structure will be greater. Referring to **Fig. 1.11 (b)**, the resistivity change of the next-generation interconnect metal material is smaller compared to the TaN/Cu/TaN system. As mentioned above, it is important to consider the resistance of the *metal/barrier system* because the use of Cu and diffusion barriers can ensure reliability. In the case of using a diffusion barrier in future interconnect metal materials, research design is required in consideration of the *metal/barrier system* as in the Cu interconnect systems.

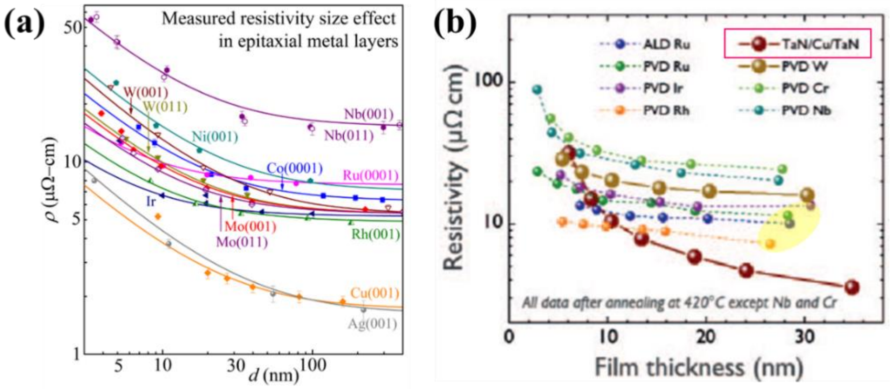


Figure 1.11 Driving force of beyond Cu interconnect, ***“Metal and barrier system”***: (a) although Cu interconnect has high effective resistivity, pure Cu is still effective for interconnect because the resistance of pure Cu is very low, (b) when the resistivity of the barrier layer of the interconnect is taken into consideration, the resistivity of the Cu/TaN system greatly increases as the linewidth becomes smaller.[33-34]

When using a diffusion barrier, there are three major considerations: *barrier thickness*, liner formation, and reliability. As shown in **Fig. 1.12**, as the node size decreased, the metal linewidth narrowed. If the thickness of the diffusion barrier is too thick, the proportion of the interconnect metal is less than 50%. [35] Barrier-less or very thin (< 2 nm) barrier process is absolutely required. In Cu interconnects, TaN is used as a diffusion barrier (> 2.5 nm thick) and Ta is used as a wetting layer (liner, ~2 nm thick). However, since it occupies a large volume, it is necessary to study barrier materials without a liner. And despite being a very thin film, high reliability must be ensured. Extrinsic failure behavior due to metal ions in Cu interconnects has been reported. Therefore, it must effectively block metal ion penetration while being thin enough.

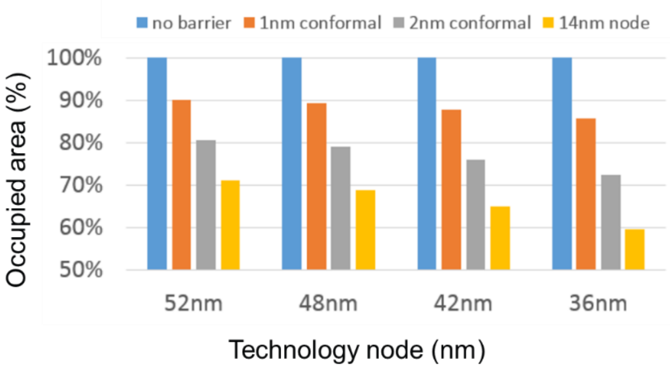


Figure 1.12 Driving force of beyond Cu interconnect, "***Barrier thickness effect***": A barrier is absolutely necessary to secure reliability, but it is necessary to minimize the thickness of the barrier in order to minimize the RC delay. It is known that robust reliability can be secured only when the TaN barrier is at least 2.5 nm thick.[35]

As shown in **Fig 1.13**, when pure Co was applied to the interconnect metal, *extrinsic failure behavior* due to Co ions was reported by imec in 2017 and 2019. [34, 36] This is a failure behavior that has also been reported for Cu interconnects. Extrinsic breakdown refers to the behavior of dielectric breakdown by metal ions compared to intrinsic breakdown in which the dielectric film is broken in a high electric field. [37-38] When Cu ions penetrate the dielectric to make nano-scale filaments, short circuit failure behavior is shown. In other words, to apply Co interconnects, a barrier material capable of blocking Co ions is absolutely necessary.

In summary, as shown in **Fig. 1.14,** the area occupied by diffusion barriers should be minimized and the development of a wiring system with high reliability characteristics should be pursued. [39-40] If it is possible to lower the *RC* delay reduction and realize high reliability in next-generation interconnect materials such as Co and Ru, beyond Cu interconnects will be able to successfully settle in the non-Cu era to come, just as the wiring system has changed from Al to Cu.

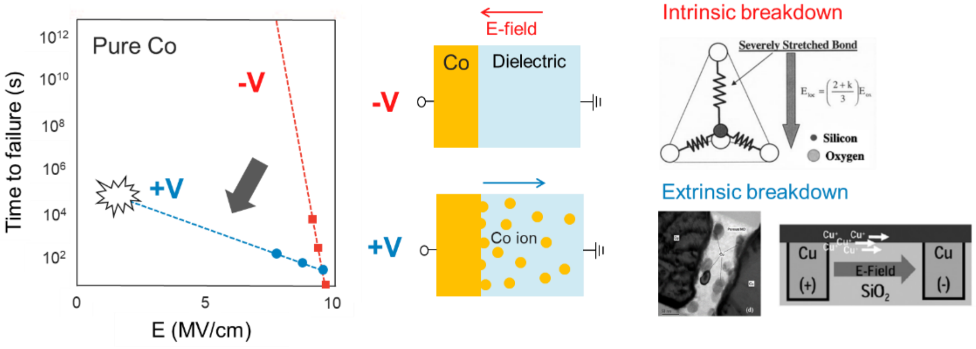

Pure Co
Time to failure (s)
10¹²
10¹⁰
10⁸
10⁶
10⁴
10²
0
5
10
E (MV/cm)
-V
+V
E-field
Co
Dielectric
-V
+V
Co ion
Intrinsic breakdown
Severely Stretched Bond
E_loc = ((2+k)/3) E_ox
Silicon
Oxygen
Extrinsic breakdown
(d)
Cu⁺
Cu
(+)
E-Field
SiO₂
Cu
(-)

Figure 1.13 Driving force of beyond Cu interconnect, “Extrinsic failure behavior of Co": the extrinsic failure behavior of pure Co was first reported in 2017.[34-36] This is the same phenomenon as the extrinsic failure caused by Cu ion diffusion/drift in Cu interconnects, and a diffusion barrier to prevent metal ions is essential for reliable interconnects.[37-38]

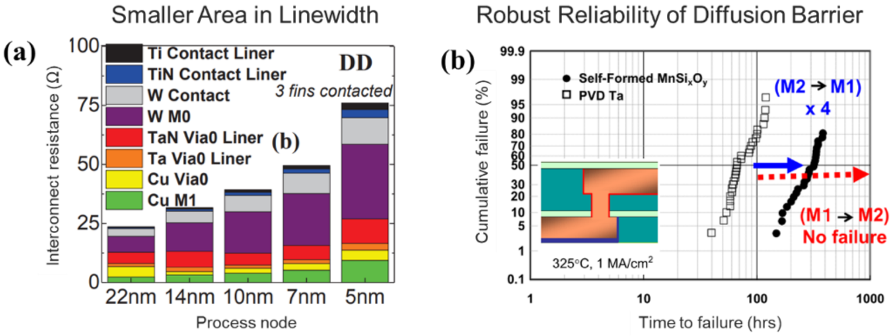


Figure 1.14 Requirements of diffusion barrier: (a) Considering the interconnect reliability aspect, a diffusion barrier that can prevent the movement of metal ions under E-field is absolutely necessary. (b) it has been reported that the area fraction of barriers in Cu M1 interconnects at 24 nm pitch is greater than 40%. Barrier requires that the diffusion barrier be thin and highly reliable.[39-40]

How the interconnect research has been conducted so far and the future direction of interconnect research has been considered. In the past interconnect R&D, metal and dielectric research has been conducted focusing on *performance* and *reliability*. However, future interconnect research should be conducted from a *comprehensive perspective of material systems* such as metal, barrier, dielectric, and capping layer in consideration of size scaling, performance, and reliability. Considering these aspects, this study selected the self-forming barrier (SFB) methodology as a systematic material design for next-generation interconnects. As a next-generation interconnect metal, Co is the promising and dielectric is continuously conducting research to increase porosity. However, it seems that the reliability part in the Co interconnect system has not been considered until now. In this respect, ultimately, the *development* of a *ultra-thin* and *highly reliable diffusion barrier* is an important study to complete the 3rd generation interconnect system. The details of barrier technologies and SFB methodology are mentioned in 2.1 Evolution of interconnect systems, Chapter 2. As shown in **Fig. 1.15**, in early 2010, a $MnSi_xO_y$ self-forming barrier was successfully developed using Cu-Mn alloy. A thin barrier with a thickness of 2 nm to 8 nm can be formed, and reliability is greatly improved, and it is still used in M1 and above lines. Using the research methodology used in Cu interconnect more than a decade ago, we intend to study a barrier design with ultra-thin and excellent reliability that can control the extrinsic failure behavior in next-generation Co interconnects.

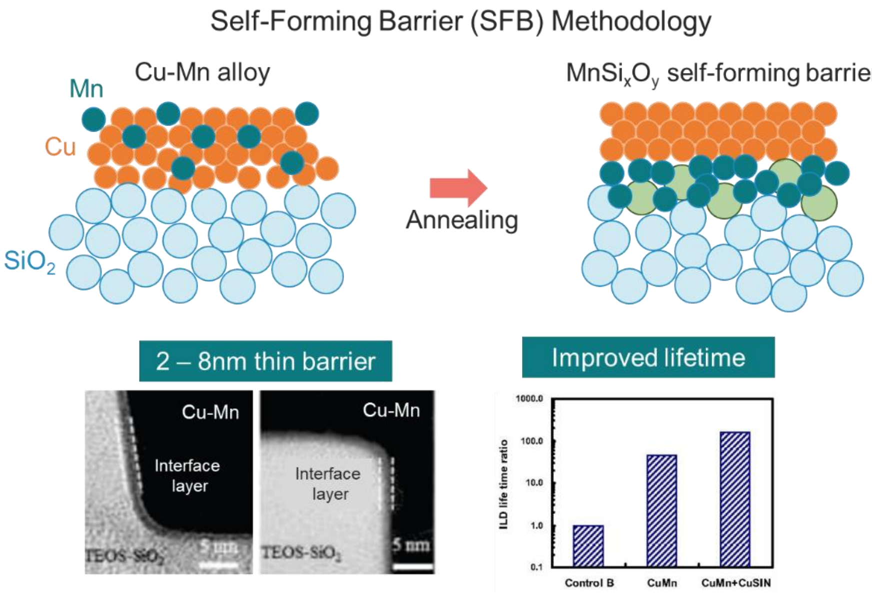

Self-Forming Barrier (SFB) Methodology
Cu-Mn alloy
Mn
Cu
SiO2
Annealing
MnSixOy self-forming barrier
2 – 8nm thin barrier
Cu-Mn
Interface layer
TEOS-SiO2
5 nm
Cu-Mn
Interface layer
TEOS-SiO2
5 nm
Improved lifetime
ILD life time ratio
1000.0
100.0
10.0
1.0
0.1
Control B
CuMn
CuMn+CuSIN

Figure 1.15 When the self-forming barrier methodology is used, a very thin diffusion barrier can be formed, and high reliability can be secured. In early 2010, the $MnSi_xO_y$ self-forming barrier was suggested using Cu-Mn alloy, securing both performance and reliability.[41-44]

1.4 Objective of the thesis

As semiconductor devices get smaller and transistors become more integrated, the importance of the technology that connects them is becoming very important. Looking back on the history of semiconductor interconnects, efforts have been made to reduce RC delay and improve reliability. The transition from first-generation Al/SiO_2 interconnects to second-generation Cu/barrier/low-k material systems began in 1998 and has been in use for over 20 years. To evolve from Cu interconnects to third generation interconnects, Co/low-k system, diffusion barrier research with robust reliability must be solved. To this end, it is necessary to design a barrier material that has a thin thickness and can effectively prevent Co ion diffusion/drift.

The objective of this thesis is to develop robust diffusion barrier material and analysis of electrical property of Co-Cr alloy interconnect using self-forming barrier methodology for Co interconnect in the near future.

The first research focus is to design a Co alloy material that forms a self-forming barrier and evaluate whether it exhibits excellent barrier properties. The self-forming barrier methodology is the behavior of dopant diffusion to the surface during the heat treatment of a thin film deposited in the form of alloy. The surface-diffused dopant reacts with SiO_2 to form oxide or silicate, and the layer formed (oxide or silicate) acts as a barrier to prevent Co ion diffusion. In this study, thermodynamic material design was carried out by dividing the behavior of self-forming barrier into three categories: Co alloy phase, out-diffusion, and reaction with dielectric. First, in the Co alloy phase, materials having a low resistivity and a higher melting point than Co were selected among CMOS-compatible materials. Since the barrier occupies the area of the interconnects, a material with a low resistivity was considered to be the most suitable.

Next, four major criteria were established for out-diffusion behavior. Materials in which intermetallic compound (IMC) was not formed and solubility was not high were selected. Since the IMC phase is thermodynamically stable, surface diffusion does not occur during the heat treatment process. Also, if the solubility is too high, it may remain in the matrix even if out-diffusion behavior occurs. In addition, the out-diffusion behavior was predicted by calculating the activity coefficient to know the dopant stability measure in the Co matrix. And, using the diffusivity literature value of dopant, metals with higher diffusivity than Co self-diffusivity were classified. The oxide formation enthalpy was calculated to check whether the surface-diffused dopant reacts with the SiO_2 dielectric. Oxidation tendency was set as the most suitable when it exists between Co and SiO_2. Finally, the stable phase existing at the Co/SiO_2 interface with the annealing temperature was predicted using Factsage^{TM} software. Nine metals were selected through this material design, and a Co self-forming barrier material with high electrical reliability was selected through thin film analysis.

The last focus confirmed the process compatibility of the Co-Cr alloy self-forming barrier. Considering that the heat treatment process temperature of the interconnects is below 450°C, the annealing process temperature at which the Cr_2O_3 diffusion barrier is formed was confirmed**.** In addition, an applicable process window was proposed by confirming the electrical characteristics with the process temperature. And the effect of resistance was confirmed by controlling the Cr doping concentration. An optimal concentration range was proposed by confirming the electrical characteristics with the Cr doping concentration. Barrier quality analysis with interconnect width (150 nm, 20 nm) was also performed. In order to reflect the structure of the metal linewidth under 5 nm node (< 24 nm), an experiment was conducted by reducing the thickness of the thin film to 20 nm. Electrical lifetime evaluation (TDDB) was conducted to propose the possibility of a Co-Cr alloy interconnect according to the process parameters. Lastly, whether the Cr_2O_3 diffusion barrier shows higher characteristics than the existing barrier (TiN), density function theory (DFT) was calculated to compare the diffusion barrier difference.

In this thesis, it was shown that when Co-Cr alloy is applied to interconnects, Cr_2O_3 diffusion barrier is formed between Co and SiO_2 interface. Through systematic Co alloy design, the research results of the $Co/Cr_2O_3/SiO_2$ interconnect system with very good reliability were proposed. The Co alloy self-forming barrier material design was able to produce an appropriate self-forming barrier based on seven criteria. In fact, Co-Cr alloy showed improved breakdown voltage characteristics of 200% or more compared to pure Co sample. Even at a low annealing temperature (> 250 °C) and a low doping concentration (< 1 at% Cr), a Cr_2O_3 self-forming barrier was formed, effectively preventing co ion movement. As a result of DFT calculation, the Cr_2O_3 barrier formed during the annealing process showed a higher diffusion barrier height than the TiN barrier. This result could potentially pave the way for third-generation interconnects consisting of high-performance Co interconnects and diffusion barriers with robust reliability under 5 nm node technology.

1.5 Organization of the thesis

In **Chapter 2**, changes in semiconductor interconnect material systems are explained as research trends for 1st generation Al/SiO_2 interconnects, 2nd generation Cu/low-k interconnects, and 3rd generation interconnects. And thermodynamic calculation methods for designing self-forming diffusion barriers are introduced. Finally, background theory necessary to evaluate the reliability of interconnects is included. **Chapter 3** describes the experimental procedures for material design, thin film fabrication, device fabrication, and electrical property measurements. **Chapter 4** describes the research method for designing Co alloy self-forming barrier materials. And through electrical reliability evaluation, we present the results of which Co alloy is appropriate. **Chapter 5** reports the influence of Co-Cr process parameters to determine the applicable process suitability in industry. And to confirm the effectiveness of the Cr_2O_3 diffusion barrier, TDDB lifetime evaluation and DFT analysis results are described. **Chapter 6** summarizes the results of this study and suggests research perspectives on interconnects.

CHAPTER 2

Theoretical background

2.1. Evolution of interconnect systems

2.1.1 Cu/barrier/low-k interconnect systems

As shown in **Fig. 2.1 (a)**, from 1970 to mid-1990, Al metal and SiO_2 dielectric were used for interconnect materials. In addition, TiN and TiW performed the functions of barrier, glue layer, anti-reflection coating, and short local interconnects (shunt layer). The reason Al interconnects was widely used is because of its low resistivity, low process difficulty, dry etching, no interdiffusion with Si, ohmic contact with Si (shallow junction issue), and very high adhesion energy with dielectrics. However, as the metal linewidth of Al became smaller, the problem of electromigration had a significant effect on the lifetime of the Al interconnects. And electrical short failure due to hillock formation is also raised as a big problem. Under these circumstances, Cu interconnects have been proposed because of the increased demand for lower *RC* delay and high reliability interconnection material systems. It was started to be applied to interconnects by IBM in 1998 and has been in the spotlight for its low resistivity and high EM resistance of Cu. [45-46] However, as shown in **Fig. 2.1 (b)**, dry etching was difficult, so a chemical-mechanical polishing (CMP) process was added. Most importantly, the diffusion barrier process was applied because the reliability problem of Cu contamination into Si was very serious. [46-49]

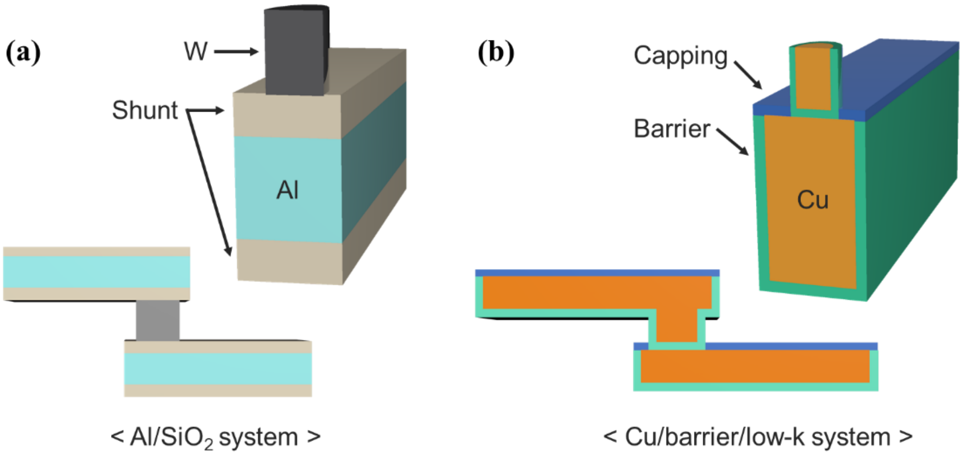


Figure 2.1 Changes in the interconnect material system: Since 1998, as the Cu interconnect system has changed, barrier and capping layer materials have been added. These new materials have resulted in high TDDB and EM reliability. Changes in interconnect materials indicate the need to develop a corresponding material system.[45-49]

Fig. 2.2 lists important technologies of back-end-of-line (BEOL) Cu interconnects over time. In 1985, the damascene structure was developed, and it became possible to fabricate EP-Cu interconnects using the electroplating method. And as Ta-based diffusion barriers were continuously developed, a barrier process called Ta/TaN (liner/barrier) was optimized. As low-k dielectrics continue to be improved, the *RC* delay is minimized, and the Cu/Ta/TaN/low-k material system continues to be used today. [47,51] What is noteworthy here is that a generation of interconnect technology has been developed over a long period of 10 to 15 years. In the case of Cu interconnects, the development of materials such as metal line, diffusion barrier, and low-k dielectric played an important role so that Cu could be applied to interconnects.

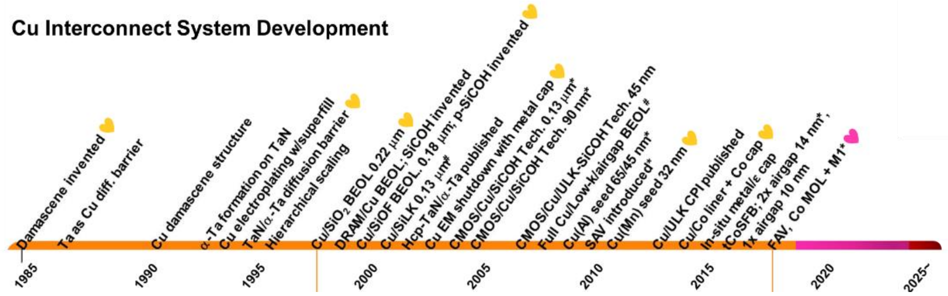
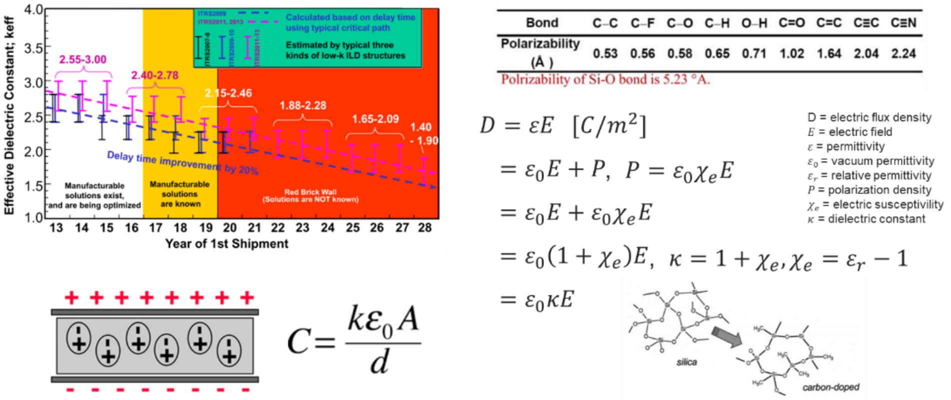

Cu Interconnect System Development
Damascene invented
Ta as Cu diff. barrier
Cu damascene structure
α-Ta formation on TaN
Cu electroplating w/superfill
TaN/α-Ta diffusion barrier
Hierarchical scaling
Cu/SiO$_2$ BEOL 0.22 μm
DRAM/Cu BEOL; SiCOH invented
Cu/SiOF BEOL. 0.18 μm; p-SiCOH invented
Cu/SiLK 0.13 μm#
Hcp-TaN/α-Ta published
Cu EM shutdown with metal cap
CMOS/Cu/SiCOH Tech. 0.13 μm*
CMOS/Cu/SiCOH Tech. 90 nm*
CMOS/Cu/ULK-SiCOH Tech. 45 nm
Full Cu/Low-k/airgap BEOL#
Cu(Al) seed 65/45 nm*
SAV introduced*
Cu(Mn) seed 32 nm
Cu/ULK CPI published
Cu/Co liner + Co cap
In-situ metal/ε cap
tCoSFB; 2x airgap 14 nm*,
1x airgap 10 nm
FAV, Co MOL + M1*
1985
1990
1995
2000
2005
2010
2015
2020
2025~

Figure 2.2 Key milestones in Cu BEOL manufacturing: important technologies for Cu interconnect development include the introduction of low-k materials that can improve performance and diffusion barrier and capping layer materials that can significantly improve reliability.[51]

Fig. 2.3 is a low-k dielectric scaling roadmap published by the international technology roadmap for semiconductors (ITRS). The capacitance of the dielectric is proportional to the dielectric constant and the area and inversely proportional to the distance. As the linewidth continues to decrease, the capacitance increases. Therefore, it is necessary to reduce the dielectric constant or make the area smaller. However, since the area is determined at the design stage in the same way as the linewidth, a material with a substantially low dielectric constant must be used. SiO_2 was first used as a dielectric, and development into fluorine doped SiO_2 and carbon doped SiO_2 continues. [20, 52]



Bond	C–C	C–F	C–O	C–H	O–H	C=O	C=C	C≡C	C≡N
Polarizability (Å)	0.53	0.56	0.58	0.65	0.71	1.02	1.64	2.04	2.24

Polrizability of Si-O bond is 5.23 °A.

$$
\begin{aligned}
D &= \varepsilon E \quad [C/m^2] \\
&= \varepsilon_0 E + P,\ \ P = \varepsilon_0 \chi_e E \\
&= \varepsilon_0 E + \varepsilon_0 \chi_e E \\
&= \varepsilon_0 (1 + \chi_e) E,\ \ \kappa = 1 + \chi_e, \chi_e = \varepsilon_r - 1 \\
&= \varepsilon_0 \kappa E
\end{aligned}
$$

D = electric flux density
E = electric field
ε = permittivity
ε_0 = vacuum permittivity
ε_r = relative permittivity
P = polarization density
χ_e = electric susceptivility
κ = dielectric constant

$$C = \frac{k\varepsilon_0 A}{d}$$

Figure 2.3 In the case of dielectric films, researchers have continued to develop materials that control porosity based on SiO_2 in order to reduce the dielectric constant.[20,52]

As shown in **Fig. 2.4**, the diffusion barrier was developed to block Cu, which has a high diffusion coefficient. Tantalum (Ta) with a melting point of 3,017 °C was first used as a Cu diffusion barrier. As a refractory metal, PVD Ta diffusion barrier prevents Cu ion diffusion and plays a good role as a wetting layer. However, since the α-Ta phase and the α-Ta phase (metastable) coexist, an issue of Cu diffusion along the grain boundary has been reported. [53] Therefore, the diffusion barrier properties were improved by adding a Ta nitride film. According to the amount of nitrogen, tetragonal β-Ta is converted to bcc TaN and fcc TaN, showing nano-crystalinity. [54] The TaN layer has excellent thermal properties and diffusion barrier properties, but since the interfacial adhesion energy with Cu is low, a Ta liner is used together. So far, the Ta/TaN bilayer has played an important role in improving the reliability of Cu interconnects. However, as the linewidth becomes very narrow, there is a situation in which the Ta/TaN diffusion barrier must also be thin. However, in the case of TaN, when the thickness is lower than 2.5 nm, the diffusion barrier property deteriorates rapidly, so the scaling down limit is reached. For the capping layer, Si-based materials have been developed to increase the electromigration resistance of Cu. The interfacial adhesion energy between Cu and the capping layer was improved to increase the EM resistance. However, as the dielectric was changed from SiO_2 to low-k and ULK, as shown in **Fig. 2.5**, the interface adhesion energy between the dielectric and the capping layer became weak, and the behavior of interface diffusion induced failure was observed. For dielectric and capping layer interface modulation, a Co-based metal capping layer has been recently developed and is attracting attention as a self-aligned interface barrier as well as interface diffusion. [53, 55-56]

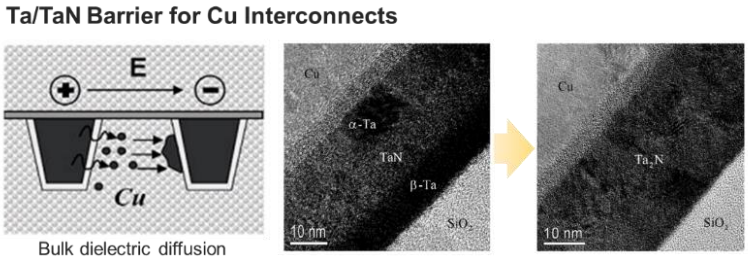

Ta/TaN Barrier for Cu Interconnects
E
Cu
Bulk dielectric diffusion
Cu
α-Ta
TaN
β-Ta
SiO2
10 nm
Cu
Ta2N
SiO2
10 nm

Figure 2.4 Ta/TaN barrier is proposed to prevent Cu ion diffusion (bulk dielectric diffusion) in Cu interconnects.[52-54]

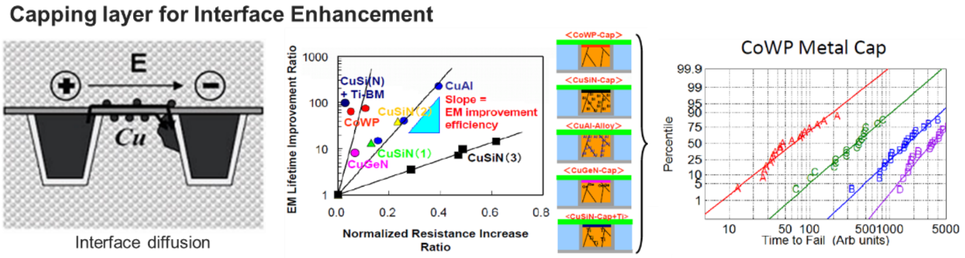


Figure 2.5 In order to improve Cu electromigration (EM) characteristics and to enhance the interfacial adhesion energy between dielectric and capping layers, capping layer materials are continuously being developed.[53,55-56]

2.1.2 Process developments for interconnect reliability

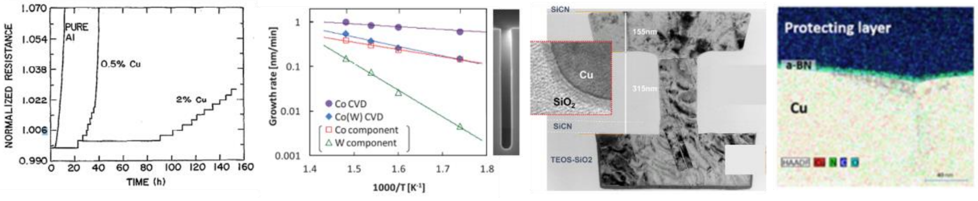
Let us take a closer look at the process developed to improve interconnect reliability. There are several processes, but if divided with the material manufacturing methods, they can be classified as alloy, atomic layer deposition (ALD), self-forming barrier, and amorphous boron nitride (a-BN). As shown in **Fig. 2.6**, alloy was first applied to Al interconnects. An Al-Cu alloy is a representative example, and it was able to significantly improve the electromigration and hillock reliability issues. However, as an alloy form, there is a problem in that the resistivity increases. [57-58]

Next is a barrier process using atomic layer deposition (ALD) deposition. Since it is possible to form a thin film of several nanoscales by using a gas precursor, there is a great advantage that it can be applied even with a thin linewidth. TiN and TaN, which are used as barriers, are deposited by ALD and are known to have good reliability characteristics. [59] However, since it is a chemical vapor deposition using a gas phase, residues remain and thus the sheet resistance is generally higher than that of PVD thin film. And to increase productivity in a large-scale process, more technology development will be required.

Self-forming barrier (SFB) is a well-known barrier formation methodology when Professor J. Koike proposed Cu-Mn alloy SFB to the university of Tokyo around 2010. [60] When Cu-X alloy is annealed, the dopant diffuses to the surface and reacts with the dielectric to form a barrier. Because the diffusion principle is used, the increase in resistivity of metals can be minimized and the resistance to electromigration and TDDB is very high. In addition, since it reacts with SiO_2 to form oxide or silicate, it is a process with high low-k process compatibility. In the case of Cu-Mn proposed by Professor J. Koike, it is still used for interconnect integration because it conformally forms a $MnSi_xO_y$ self-forming barrier with a thickness of 2 nm – 8 nm.

Finally, a paper has been reported that an amorphous boron nitride dielectric material can be applied as a dielectric and diffusion barrier. a-BN showed very low dielectric constant (~1.16) properties at 1 MHz and effectively blocked Co ion diffusion. [61] Of course, to be applied to the semiconductor process, there remains a task to develop the hydrogen free process and large-scale process. Nevertheless, the research direction of a-BN having a hybrid function (robust barrier property with low dielectric constant) is a very important implication for future interconnect materials R&D.

Technology	Alloy	ALD	Self-forming barrier (SFB)	a-boron nitride
Materials	Al-0.5wt% Cu alloy	TiN, TaN	Cu-Mn	a-BN
Resistivity	△	△	O	- (dielectric)
EM/TDDB resistance	O	O	O	O
Low-κ compatibility	-	O	O	O
Process suitability (productivity and cost)	O	△	O	△



Hitachi, *Thin Solid Films*, 437 (2003) TNSC and IBM, *ECS JSSST*, 2 (2013) Coutesy of J. Koike Samsung, *Nature*, 582 (2020)

Figure 2.6 Comparison of interconnect reliability technologies: alloy, ALD, self-forming barrier (SFB), and a-BN methodologies have been used to improve reliability. It is predicted that ALD

and SFB, which can form very thin barriers, are most suitable as the linewidth becomes narrower.[57-61]

Let us understand more about SFB methodology. In the 5 nm node technology, the thickness of the barrier is most important because the metal linewidth is narrowed down to 20 nm. As shown in **Fig. 2.7**, the Cu-Mn seed layer is stacked, and self-aligned barrier formation occurs during the annealing process. The thickness of the self-forming barrier can be controlled with the Mn (dopant) doping concentration, annealing temperature, and annealing time. [44,62] In general, since the annealing process is carried out at 400 °C for 1 hour, the time and formation energy for Mn to react with SiO_2 are not large. Therefore, thin silicate can be formed. It has been reported that the diffusion barrier film can be formed with a thickness in the range of 2 nm to 8 nm with annealing temperatures (350 °C – 450 °C) of Cu-Mn alloy. [55, 62-65] As a result, Cu-Mn alloy has a smaller resistance rise than other Cu alloys and has greatly improved reliability, so it can be said that it is a methodology that can be sufficiently applied to interconnects with a narrow linewidth.

As shown in **Fig. 2.8**, it shows the difference between the traditional barrier process and the SFB process. The traditional barrier process is a two-step process that deposits a TiN or Ta/TaN barrier and proceeds with PVD Cu seed layer/electroplating Cu. On the other hand, the SFB process is a one-step process and has great advantages in terms of process time and cost because it forms a barrier during the annealing process by depositing the alloy phase.

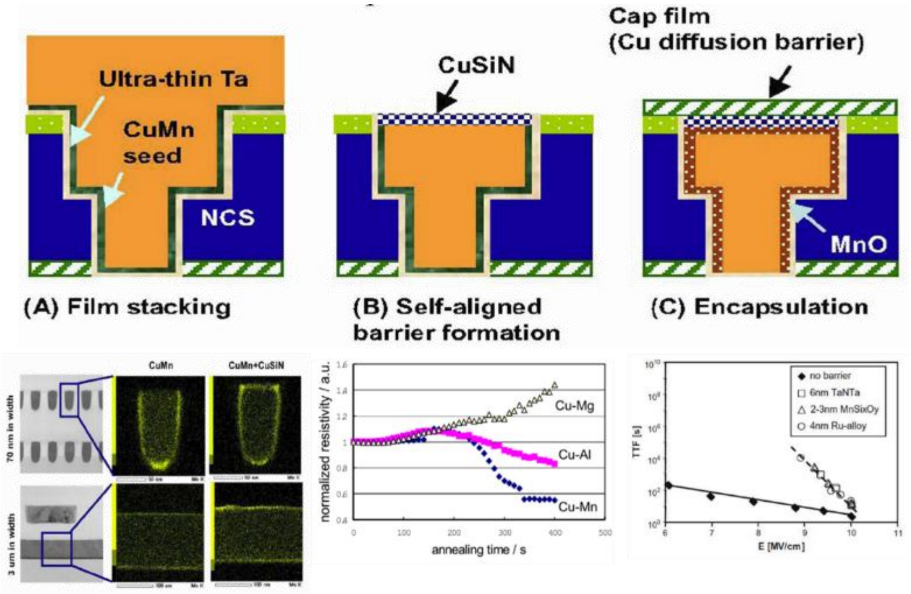

Cap film
(Cu diffusion barrier)
CuSiN
Ultra-thin Ta
CuMn
seed
NCS
MnO
(A) Film stacking
(B) Self-aligned barrier formation
(C) Encapsulation
CuMn
CuMn+CuSiN
70 nm in width
3 um in width
normalized resistivity / a.u.
annealing time / s
Cu-Mg
Cu-Al
Cu-Mn
0
100
200
300
400
500
0.4
0.6
0.8
1
1.2
1.4
1.6
TTF [s]
E [MV/cm]
no barrier
6nm TaNTa
2-3nm MnSixOy
4nm Ru-alloy
10^0
10^2
10^4
10^6
10^8
10^{10}
6
7
8
9
10
11

Figure 2.7 Self-forming barrier (SFB) technology: a Mn silicate self-forming barrier has been reported in the annealing using Cu-Mn alloy. It showed low resistance rise and excellent e-field resistance.[44,52,62-65]

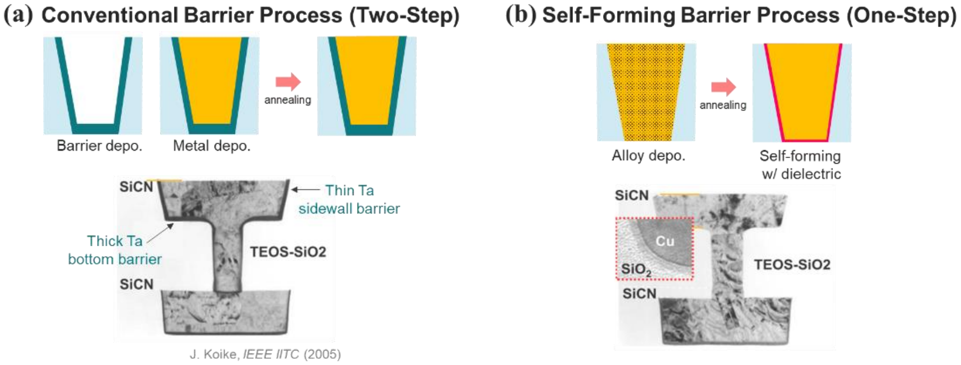
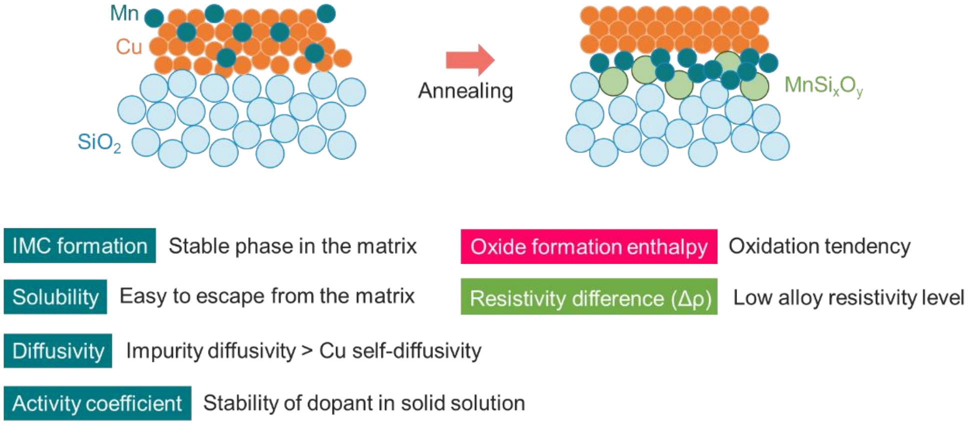

(a) Conventional Barrier Process (Two-Step)
(b) Self-Forming Barrier Process (One-Step)
annealing
Barrier depo.
Metal depo.
annealing
Alloy depo.
Self-forming
w/ dielectric
SiCN
Thin Ta
sidewall barrier
Thick Ta
bottom barrier
TEOS-SiO2
SiCN
SiCN
Cu
SiO_2
SiCN
TEOS-SiO2
J. Koike, IEEE IITC (2005)

Figure 2.8 Process comparison of conventional barrier and self-forming barrier: (a) two-step PVD process, (b) one-step SFB process.[60]

As shown in **Fig. 2.9**, several criteria were established to design the Cu-Mn self-forming barrier material. First, the Cu dopant should form a simple solid solution and not form an intermetallic compound. Second, for the dopant to preferentially move to the interface rather than the Cu element, the diffusion coefficient of the dopant must be faster than Cu self-diffusivity. Third, the active coefficient (γ) of the dopant in the Cu solid solution state should be close to or greater than 1. Finally, it should have a lower degree of oxidation (higher standard free energy) than SiO_2. [42, 60, 62]



IMC formation	Stable phase in the matrix	Oxide formation enthalpy	Oxidation tendency
Solubility	Easy to escape from the matrix	Resistivity difference (Δρ)	Low alloy resistivity level
Diffusivity	Impurity diffusivity > Cu self-diffusivity		
Activity coefficient	Stability of dopant in solid solution		

Figure 2.9 The rule of thumb for Cu-Mn alloys proposed by J. Koike of the University of Tokyo.[42,60,62]

2.1.3 3^{rd} generation of interconnect systems

Previously, Al/SiO_2, Cu/barrier/low-k, and reliability driven process development were investigated. Let's find out why the upcoming 3rd generation interconnect is being mentioned. As shown in **Fig. 2.10**, research on the beyond Cu system is being actively conducted for semiconductor interconnects following Al/SiO_2 and Cu/barrier/low-k interconnects. [45,67-68] The biggest reason for looking for beyond Cu interconnect materials is that the limit of Cu damascene interconnects is coming. As the metal linewidth continues to decrease, the resistivity of Cu rapidly increases. As shown in **Fig. 2.11**, Cu has an electron mean free path of 39 nm, so the bulk resistivity is very low. However, in the damascene structure, since it is a trench structure, there is a scattering term due to the sidewall. Electroplating Cu mostly has poly-crystallinity, so the scattering term due to the grain boundary should also be considered. In other words, if the linewidth continues to decrease, the influence of side wall and grain boundary scattering increases when electrons move. [29-30] As a result, the Cu resistivity in damascene structure rises much higher than the bulk resistivity.

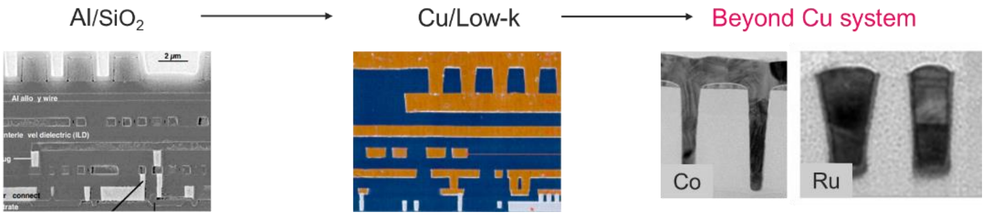
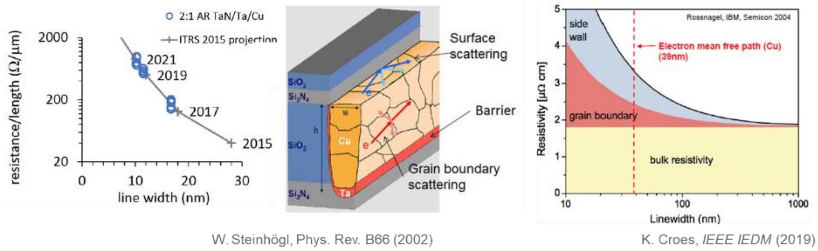


Figure 2.10 A history of interconnect system innovation: 1st generation Al/SiO_2, 2nd generation Cu/low-k, 3rd generation beyond Cu systems.[45,67-68]



Surface Scattering

: Fuchs-Sondheimer model

$\rho_{surf} = \rho\,(h, w, p, \lambda)$

Grain Boundary Scattering

: Mayadas-Shatzkes model

$\rho_{GB} = \rho\,(d, R, \lambda)$

h, w : conductor height and width
p : specularity parameter (Fraction of electrons scattered elastically from the interface)
λ : electron mean free path
d : avr. grain boundary distance
R : Reflection coefficient at GB

Figure 2.11 Limitation of Cu damascene interconnects: as sidewall scattering and grain boundary scattering increased, resistivity higher than bulk resistivity appeared.$^{29\text{-}30}$

Referring to **Fig. 2.12**, the diffusion barrier (dielectric) and grain boundary are electron scattering sites. [69-72] If only bulk resistivity is considered when linewidth is wide enough, metals with low electron mean free path are more appropriate for narrow linewidth. Surface scattering and grain boundary scattering can be understood with the Fuchs-Sondheimer model and the Mayadas-Shatzkes model, respectively. In summary, both bulk resistivity (ρ_0) and electron mean free path (λ) must be considered for narrow linewidths. Recently, considering the value of $\rho_0 \times \lambda$, a metal material to replace Cu has been proposed. When the Fermi surface area is calculated using the linear Boltzmann transport equation, the $\rho_0 \times \lambda$ value can be obtained as shown in **Fig. 2.13**. [73-75] Representative materials with low $\rho_0 \times \lambda$ values can be found in **Table 2.1**. [34, 73-78]

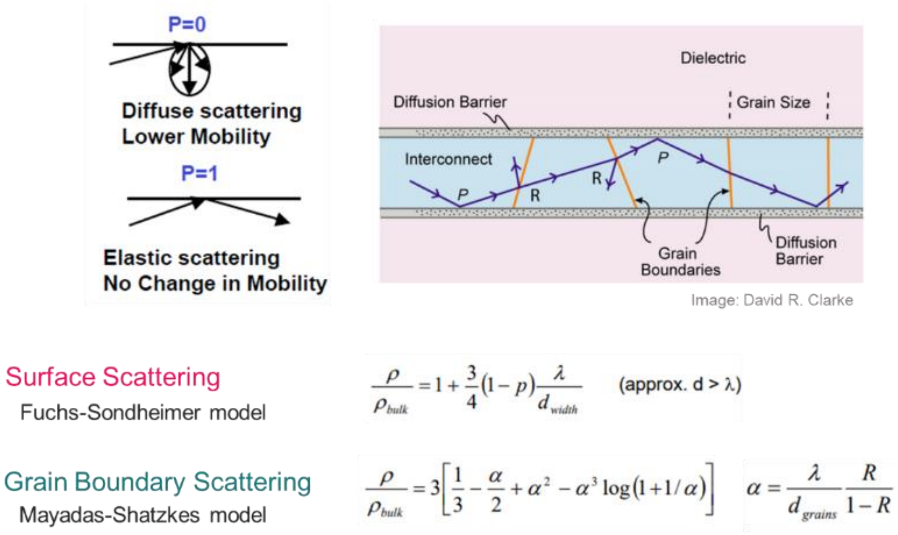

P=0
Diffuse scattering
Lower Mobility
P=1
Elastic scattering
No Change in Mobility
Dielectric
Diffusion Barrier
Grain Size
Interconnect
P
R
R
P
Grain Boundaries
Diffusion Barrier
Image: David R. Clarke
Surface Scattering
Fuchs-Sondheimer model
$\frac{\rho}{\rho_{bulk}} = 1 + \frac{3}{4}(1-p)\frac{\lambda}{d_{width}}$ (approx. d > λ)
Grain Boundary Scattering
Mayadas-Shatzkes model
$\frac{\rho}{\rho_{bulk}} = 3\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \log(1+1/\alpha)\right]$
$\alpha = \frac{\lambda}{d_{grains}}\frac{R}{1-R}$

Figure 2.12 Surface scattering and grain boundary scattering: As the linewidth decreases, materials with a long mean free path have a greater scattering effect.[69-72]

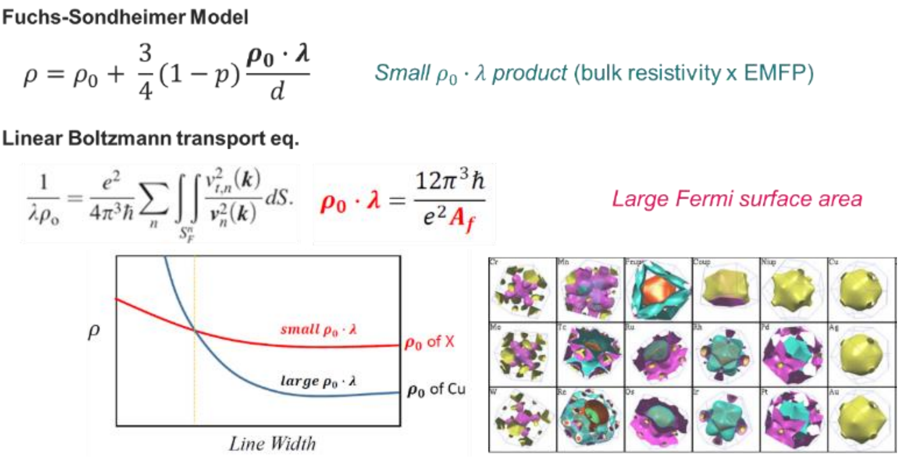

Fuchs-Sondheimer Model
$\rho = \rho_0 + \frac{3}{4}(1-p)\frac{\rho_0 \cdot \lambda}{d}$
Small $\rho_0 \cdot \lambda$ product (bulk resistivity x EMFP)
Linear Boltzmann transport eq.
$\frac{1}{\lambda\rho_0} = \frac{e^2}{4\pi^3\hbar}\sum_n \iint_{S_F^n} \frac{v_{t,n}^2(\boldsymbol{k})}{v_n^2(\boldsymbol{k})} dS.$
$\rho_0 \cdot \lambda = \frac{12\pi^3\hbar}{e^2 A_f}$
Large Fermi surface area
ρ
small $\rho_0 \cdot \lambda$
large $\rho_0 \cdot \lambda$
ρ_0 of X
ρ_0 of Cu
Line Width

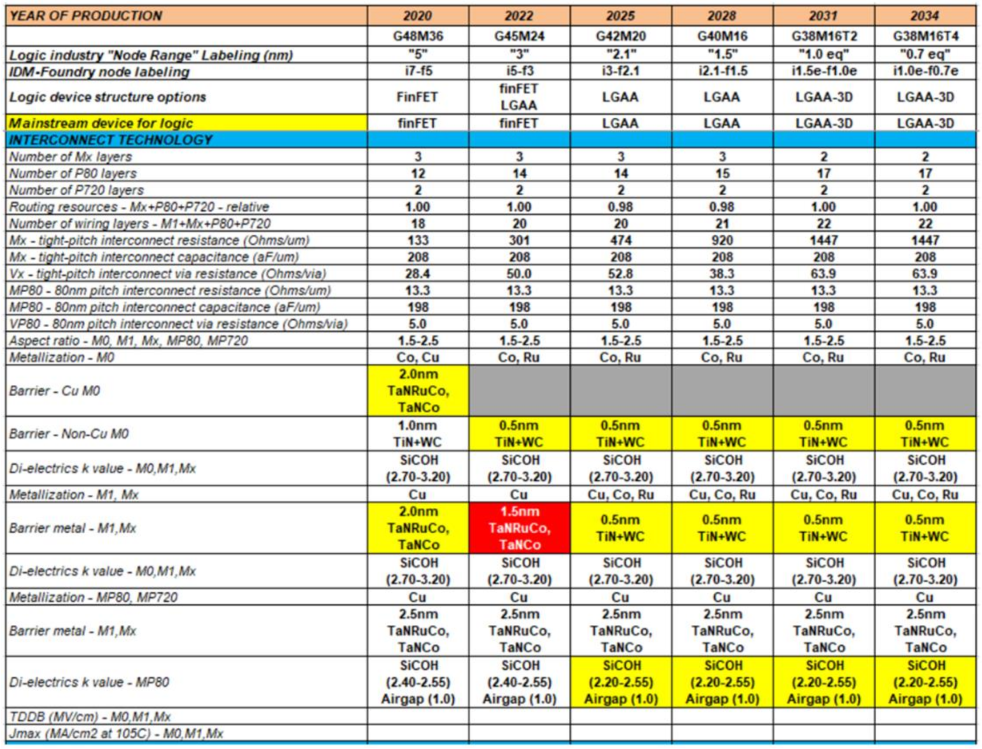
Figure 2.13 The lower the product of the bulk resistivity (ρ_0) and the electron mean free path (λ), the less the scattering effect.[73-75]

Table 2.1 Bulk resistivity (ρ_0) and the electron mean free path (λ) of alternative metal candidates.[34,73-78]

Element	$\rho_{o,rt}$ (μm·cm)	λrt (nm)	$\rho \times \lambda$ ($10^{-16} \times m^2$)	T_m (°C)
Cu	1.678	39.9	6.7	1,085
Ag	1.587	53.3	8.46	962
Au	2.214	37.7	8.35	1,064
Al	2.65	18.9	5.01	660
Ca	3.36	35.4	11.9	842
Be	3.56	48.0/68.2*	17.1/24.3	1,287
Mg	4.39	22.3/20.0*	9.81/8.8	1,091
Rh	4.7	6.88	3.23	1,964
Ir	5.2	7.09	3.69	2,466
W	5.28	15.5	8.2	3,422
Mo	5.34	11.2	5.99	2,623
Zn	5.9	17.4/13.7*	10.3/8.1	419
Co	6.2	11.8/7.77*	7.31/4.82	1,495
Ni	6.93	5.87	4.07	1,455
Cd	7.5	16.8/15.1*	12.6/11.3	321
Ru	7.8	6.59/4.88*	5.14/3.81	2,334
In	8.8	8.65/8.16*	7.62/7.18	156
Os	8.9	7.20/4.87*	6.41/4.33	3,033

*For hexagonal and tetragonal crystal structures (hcp and bct), the two listed values are for transport perpendicular and parallel to the hexagonal/tetragonal axis.

Fig. 2.14 is a roadmap for interconnect technology for logical devices through 2034 published by the International Roadmap for Devices and Systems (IRDS). [79] M0 and M1 pitch scaling will be reduced to 20 nm in 2025. In terms of metal linewidth, it should be reduced by 10 nm, which is close to single nanowire. And for the M1 interconnect material, Co and Ru are being considered as well as Cu as of 2025. The important part here is that the metal material will change, but the TiN + WC barrier system remains the same. In other words, studies on metal, dielectric, and barrier, which are important for future wiring development, need to be conducted more systematically from a material point of view.



YEAR OF PRODUCTION	2020	2022	2025	2028	2031	2034
	G48M36	G45M24	G42M20	G40M16	G38M16T2	G38M16T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Mainstream device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
INTERCONNECT TECHNOLOGY						
Number of Mx layers	3	3	3	3	2	2
Number of P80 layers	12	14	14	15	17	17
Number of P720 layers	2	2	2	2	2	2
Routing resources - Mx+P80+P720 - relative	1.00	1.00	0.98	0.98	1.00	1.00
Number of wiring layers - M1+Mx+P80+P720	18	20	20	21	22	22
Mx - tight-pitch interconnect resistance (Ohms/um)	133	301	474	920	1447	1447
Mx - tight-pitch interconnect capacitance (aF/um)	208	208	208	208	208	208
Vx - tight-pitch interconnect via resistance (Ohms/via)	28.4	50.0	52.8	38.3	63.9	63.9
MP80 - 80nm pitch interconnect resistance (Ohms/um)	13.3	13.3	13.3	13.3	13.3	13.3
MP80 - 80nm pitch interconnect capacitance (aF/um)	198	198	198	198	198	198
VP80 - 80nm pitch interconnect via resistance (Ohms/via)	5.0	5.0	5.0	5.0	5.0	5.0
Aspect ratio - M0, M1, Mx, MP80, MP720	1.5-2.5	1.5-2.5	1.5-2.5	1.5-2.5	1.5-2.5	1.5-2.5
Metallization - M0	Co, Cu	Co, Ru	Co, Ru	Co, Ru	Co, Ru	Co, Ru
Barrier - Cu M0	2.0nm TaNRuCo, TaNCo					
Barrier - Non-Cu M0	1.0nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC
Di-electrics k value - M0,M1,Mx	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)
Metallization - M1, Mx	Cu	Cu	Cu, Co, Ru	Cu, Co, Ru	Cu, Co, Ru	Cu, Co, Ru
Barrier metal - M1,Mx	2.0nm TaNRuCo, TaNCo	1.5nm TaNRuCo, TaNCo	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC	0.5nm TiN+WC
Di-electrics k value - M0,M1,Mx	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)	SiCOH (2.70-3.20)
Metallization - MP80, MP720	Cu	Cu	Cu	Cu	Cu	Cu
Barrier metal - M1,Mx	2.5nm TaNRuCo, TaNCo	2.5nm TaNRuCo, TaNCo	2.5nm TaNRuCo, TaNCo	2.5nm TaNRuCo, TaNCo	2.5nm TaNRuCo, TaNCo	2.5nm TaNRuCo, TaNCo
Di-electrics k value - MP80	SiCOH (2.40-2.55) Airgap (1.0)	SiCOH (2.40-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)	SiCOH (2.20-2.55) Airgap (1.0)
TDDB (MV/cm) - M0,M1,Mx						
Jmax (MA/cm2 at 105C) - M0,M1,Mx						

Figure 2.14 Technology roadmap of logic devices (2020 - 2034) published by International Roadmap for Devices and Systems (IRDS).[79]

As shown in **Fig. 2.15**, it is the result of comparing the bulk resistivity and effective resistivity of Co and Ru, which are mentioned as non-copper materials. If only the bulk resistivity is considered, Co and Ru are 3 to 4 times higher than Cu. On the other hand, if the effective resistivity is compared considering the electron mean free path, the opposite result can be obtained. [33-34, 71, 73-74, 80] In addition, the range of change in resistivity of the TaN/Cu/TaN system is much higher than that of Ru and Co. It seems worthy of discussion that Ru and Co are beyond Cu metals.

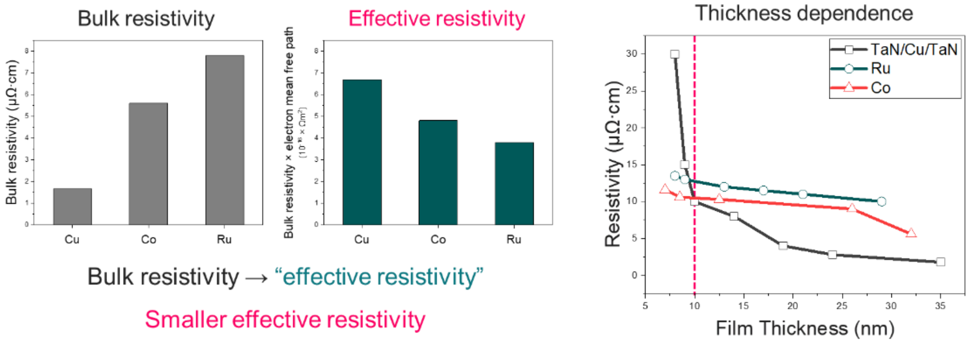


Figure 2.15 Non-Cu Interconnects: effective resistivity of Co and Ru.[73-74,77]

So, which material, Co or Ru, is best for interconnects? In **Fig. 2.16**, Co has a lower resistivity than Ru. And because of its good wetting properties, it is used as an adhesion layer (liner) for Cu. Above all, in the Cu damascene structure to which the CoWP capping layer is applied, Co seems to be the most suitable for forming a homogeneous material system. However, as will be mentioned again later, extrinsic breakdown behavior due to Co ion diffusion/drift has been reported, so a reliability solution is needed. Ru has no solubility with Cu and no intermetallic compound is formed, so it is also used as an adhesion layer. It shows higher bulk resistivity than Co, but has excellent reflow and gap-fill properties, so there is a process advantage. Since it has a very high melting point of 2,334 °C, it is known that EM and TDDB resistance are very high. However, the problem of interdiffusion with CoWP, which is used as an interface barrier, has been recently reported, and it is necessary to solve this problem. In the end, which material can be applied to the interconnects will be decided depending on the material and process technology required for each material is developed. [81-86]

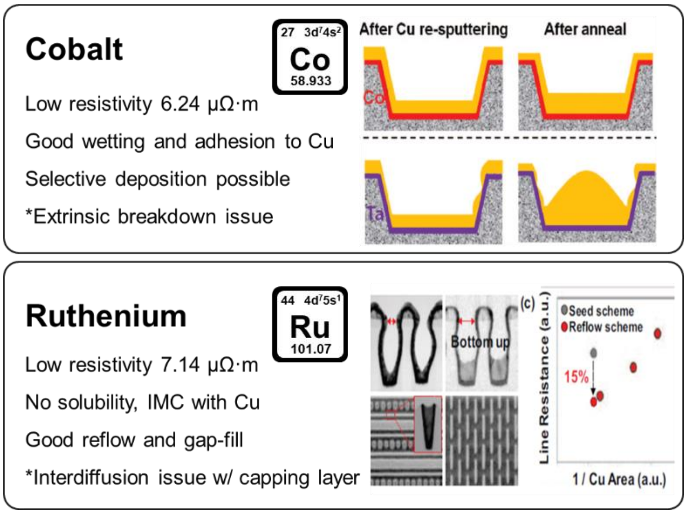

Cobalt
27 3d⁷4s²
Co
58.933
Low resistivity 6.24 μΩ·m
Good wetting and adhesion to Cu
Selective deposition possible
*Extrinsic breakdown issue
After Cu re-sputtering
After anneal
Co
Ta
Ruthenium
44 4d⁷5s¹
Ru
101.07
Low resistivity 7.14 μΩ·m
No solubility, IMC with Cu
Good reflow and gap-fill
*Interdiffusion issue w/ capping layer
Bottom up
(c)
Line Resistance (a.u.)
Seed scheme
Reflow scheme
15%
1 / Cu Area (a.u.)

Figure 2.16 Advantages and disadvantages of alternative metals, Co and Ru.[81-86]

As shown in **Fig. 2.17**, imec, GlobalFoundries, and IBM consistently report research results on Ru interconnect. As mentioned above, the TDDB and EM properties of Ru are known to be very good. [68,87] **Fig. 2.18** shows the results of Co interconnect research. Representative IDMs include Intel, Samsung, and Applied Materials. [67,89] It shows superior reliability characteristics in Co interconnect than Cu alloy. As Intel and Samsung, which produce logic devices, consistently report Co interconnects research, Co seems to be a bit more powerful for beyond Cu interconnects.

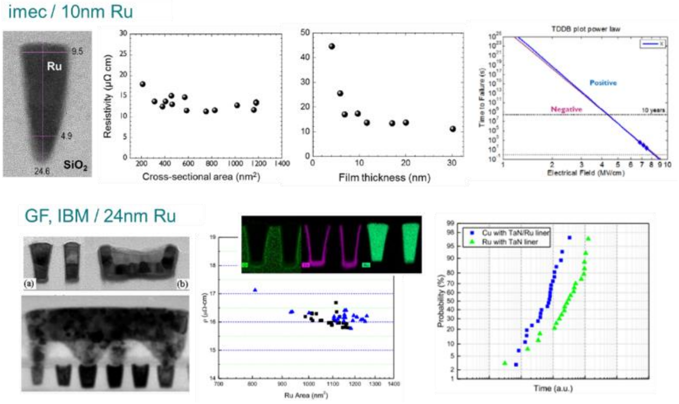


Figure 2.17 Ru interconnect research results of integrated device manufacturers (IDM): imec's 10nm Ru evaluation and GlobalFoundries and IBM's 24nm Ru evaluation.[68,88]

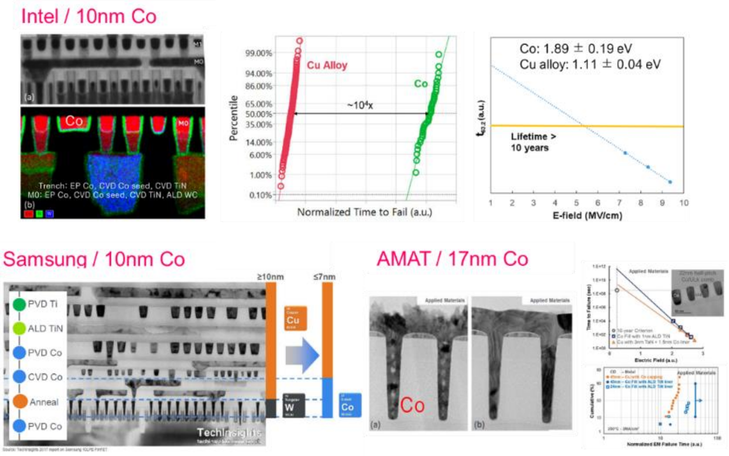
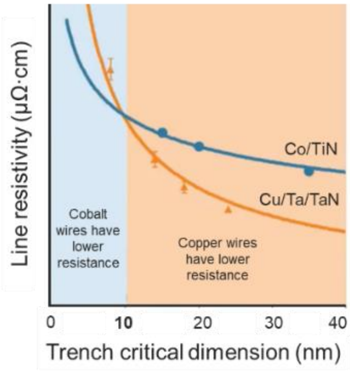
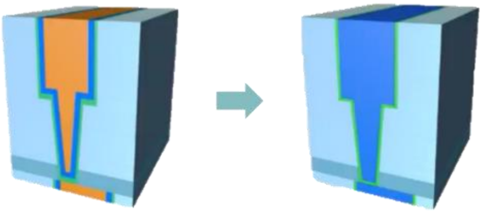


Figure 2.18 Co interconnect research by IDMs: intel’s 10nm Co integration, Samsung’s 10nm Co demonstration, and AMAT’s 17nm Co interconnect test.[67,89]

Fig. 2.19 shows the advantages of the Co/TiN interconnect system proposed by Applied Materials. It is reported that when Co/TiN interconnect is used, lower resistivity can be obtained than Cu/Ta/TaN system when the critical dimension is below 10 nm. Since the TiN barrier does not require a liner and can be made very thin through the ALD process, the metal fill ratio can be increased to 87%. [89] This is very important data for barrier thickness effect in terms of maximizing the performance of the interconnects discussed earlier. And as shown in **Fig. 2.20**, a 1 nm ALD TiN barrier process was proposed by Applied Materials in 2017. [89-90] It showed excellent TDDB resistance even with a 1 nm ALD TiN barrier. However, considering that there have been no additional reports since 2017, it can be considered that the ALD TiN barrier process issue or reliability has not yet reached the manufacturing level.





5nm node	Cu + liner + barrier	Co + ALD super thin barrier
Liner	27%	0%
Barrier	40%	13%
Metal fill	33%	87%

Figure 2.19 Co/TiN metal/barrier system proposed by Applied Materials: Resistance crossover between Co/TiN and Cu/Ta/TaN systems: advantages of Co and ALD diffusion barriers.[89-90]

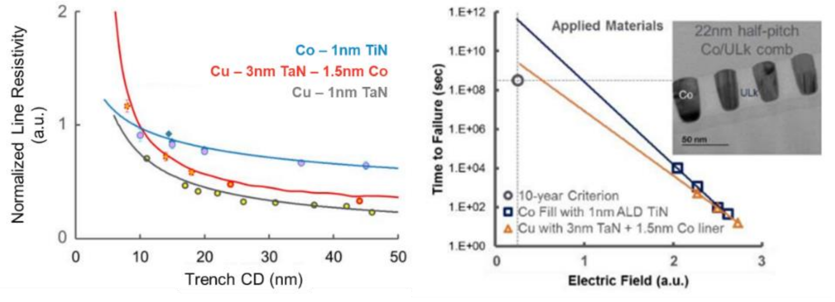


Figure 2.20 Co/ALD TiN system proposed by AMATs shows better TDDB properties than Cu/Ta/TaN.[89-90]

2.2. Thermodynamic tools for self-forming barrier methodology

2.2.1 Binary phase diagram

Phase diagram is a material engineering approach to know the equilibrium phase under specific conditions such as temperature and pressure. So, phase diagram can contribute to predict process parameters and material composition. In this study, a binary phase diagram was used to design the barrier metallurgy predicting the composition of Co alloy materials with the annealing temperature.

2.2.2 Ellingham diagram

Ellingham diagram defines the standard Gibbs free energy ($\boldsymbol{\Delta G}°$) of metal compound formation with the temperatures and partial pressure of gaseous components such as carbon monoxide (CO), hydrogen (H_2), and oxygen (O_2). [91-93] In **Fig. 2.21**, left y-axis represents the standard Gibbs free energy of compound formation ($\boldsymbol{\Delta G}°$) and right y-axis represents the oxygen partial pressure (pO_2). For example, if you need to know the specific oxygen partial pressure (pO_2), you can see the intersection point by connecting an extension line at a specific temperature on the x-axis. The relationship between Gibbs free energy and oxygen partial press is defined as follows.

$$\boldsymbol{\Delta G}° = \mathbf{RTlnpO_2} \qquad (2.1)$$

where R is gas constant, and T is temperature of the system. By comparing the $\boldsymbol{\Delta G°}$ values of compounds, the degree of oxidation/reduction between elements can be determined from the Ellingham diagram.

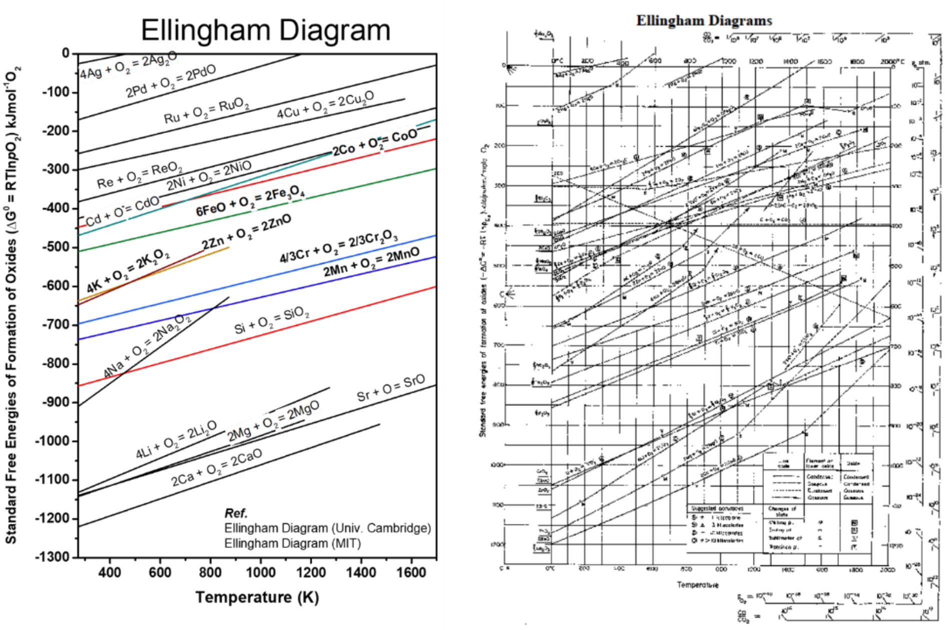


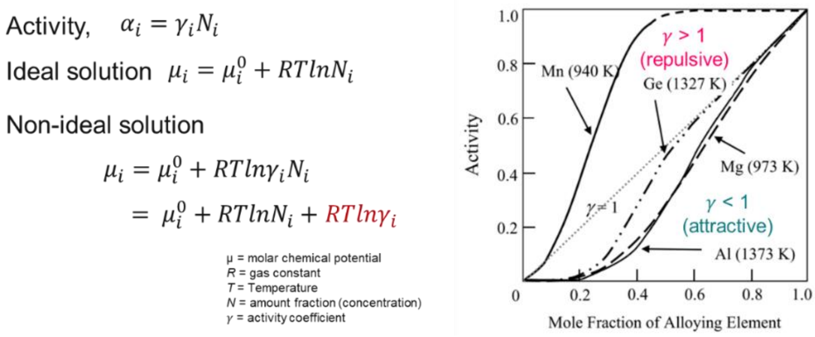
Figure 2.21 Ellingham diagram for Co alloy self-forming barrier (left), Ellingham diagram published by MIT. (right) [92-93]

2.2.3 Activity coefficient

As shown in **Fig. 2.22**, activity indicates how much a given component is active in a single phase. The activity of a component in a mixture is proportional to the amount of that component, but also varies depending on which components it is present with. Activity is a concept for indicating the tendency of a substance to depart together with fugacity. The activity of a certain component has a correlation with the mole fraction, which is defined as the activity coefficient. The activity coefficient is a proportional constant for the relationship between the activity of one component and the mole fraction. If the activity coefficient is 1, the activity of one component is equal to the mole fraction of the original component. [40,62] In case of Co alloy, the stability of elements in Co solid solution can be expressed as an activity coefficient.

When activity coefficient $\gamma > 1$, the metal dopant in the Co matrix is less stable.

When activity coefficient $\gamma < 1$, the metal dopant is more stable in the Co matrix.



Activity, $\alpha_i = \gamma_i N_i$

Ideal solution $\mu_i = \mu_i^0 + RTlnN_i$

Non-ideal solution

$$\begin{aligned}\mu_i &= \mu_i^0 + RTln\gamma_i N_i \\ &= \mu_i^0 + RTlnN_i + RTln\gamma_i\end{aligned}$$

μ = molar chemical potential

R = gas constant

T = Temperature

N = amount fraction (concentration)

γ = activity coefficient

Figure 2.22 activity coefficient calculation in alloy.[40,62]

2.3. Reliability of interconnects

2.3.1 Current conduction mechanisms in dielectrics

As shown in **Fig. 2.23**, the conduction mechanism in dielectric is divided into two types; An electrode-limited conduction mechanism that depends on the electrical properties (barrier height) at the electrode and dielectric interface and a bulk-limited conduction mechanism that depends only on the properties of the dielectric. [94-95]

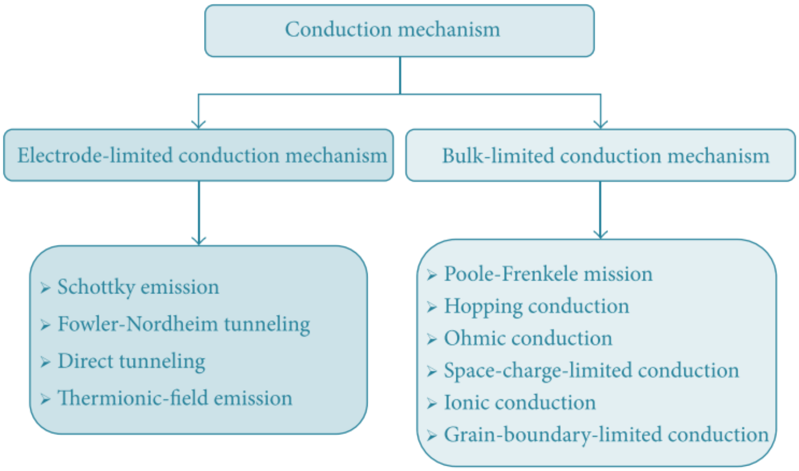

Conduction mechanism
Electrode-limited conduction mechanism
Bulk-limited conduction mechanism
➢ Schottky emission
➢ Fowler-Nordheim tunneling
➢ Direct tunneling
➢ Thermionic-field emission
➢ Poole-Frenkele mission
➢ Hopping conduction
➢ Ohmic conduction
➢ Space-charge-limited conduction
➢ Ionic conduction
➢ Grain-boundary-limited conduction

Figure 2.23 Conduction mechanisms in dielectric films.[94-95]

First, the electrode-limited conduction mechanism, which depends on the electrical characteristics of the interface, is divided into four major categories. As shown in **Fig. 2.24**, the conduction mechanism called Schottky, or thermionic emission is a mechanism in which electrons are emitted from metal to dielectric conduction band. When the carrier gains sufficient energy by thermal activation, it conducts beyond the built-in potential (barrier height) of the metal/dielectric interface. Next, Fowler-Nordheim tunneling is a mechanism in which electron tunneling occurs and conduction from the metal Fermi level to the dielectric conduction band. Even in the presence of built-in potential, in a sufficiently thin (< 10 nm) dielectric, penetration occurs when electrons can penetrate, or the E-field is large enough. Therefore, it is independent of temperature, and if the E-field is small and the dielectric thickness is small enough, direct tunneling occurs. (Tunneling current can be confirmed at low temperature) Finally, thermionic-field emission refers to a case in which the tunneling electrons conduct thermal activation with energy between the Fermi level of the metal and the conduction band of the dielectric. [94,96]

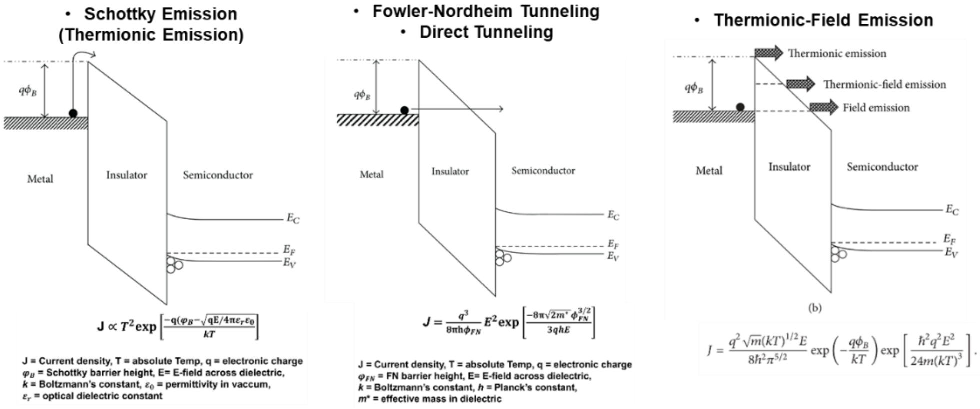

• Schottky Emission
(Thermionic Emission)
$q\phi_B$
Metal
Insulator
Semiconductor
E_C
E_F
E_V
$J \propto T^2 \exp\left[\frac{-q(\varphi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0})}{kT}\right]$
J = Current density, T = absolute Temp, q = electronic charge
φ_B = Schottky barrier height, E= E-field across dielectric,
k = Boltzmann's constant, ε_0 = permittivity in vaccum,
ε_r = optical dielectric constant
• Fowler-Nordheim Tunneling
• Direct Tunneling
$q\phi_B$
Metal
Insulator
Semiconductor
E_C
E_F
E_V
$J = \frac{q^3}{8\pi h \phi_{FN}} E^2 \exp\left[\frac{-8\pi\sqrt{2m^*}\,\phi_{FN}^{3/2}}{3qhE}\right]$
J = Current density, T = absolute Temp, q = electronic charge
φ_{FN} = FN barrier height, E= E-field across dielectric,
k = Boltzmann's constant, h = Planck's constant,
m^* = effective mass in dielectric
• Thermionic-Field Emission
Thermionic emission
Thermionic-field emission
Field emission
$q\phi_B$
Metal
Insulator
Semiconductor
E_C
E_F
E_V
(b)
$J = \frac{q^2\sqrt{m}(kT)^{1/2}E}{8\hbar^2\pi^{5/2}} \exp\left(-\frac{q\phi_B}{kT}\right) \exp\left[\frac{\hbar^2 q^2 E^2}{24m(kT)^3}\right].$

Figure 2.24 Electrode-limited conduction mechanisms: Schottky emission, Fowler-Nordheim tunneling, thermionic-field emission.[94,96]

As shown in **Fig. 2.25**, The bulk-limited conduction mechanism is based on the dielectric properties, especially the trap level, spacing, and density of the dielectric film. (the trap energy level of the dielectric film, trap spacing, trap density, electronic drift mobility, dielectric relaxation time, and density of states are important) First, Poole-Frenkel emission is a mechanism in which electrons trapped in the dielectric are thermally activated and excited. It is also called internal Schottky emssion because it is similar to the Schottky emission mechanism. Since P-F emission is a mechanism for thermal activation in the E-field, it is reported that it appears at high temperature (300K – 400K) and high E-field. (Appears only in damaged insulators) Next, hopping conduction is a model in which trapped electrons are hopped to trap by tunneling effect and conduction occurs at a high E-field and thickness below 1 nm. Ohmic conduction is conduction due to movement of mobile electrons in the conduction band or mobile holes in the valence band and has a linear relationship with the E-field. In dielectric, it is observed only in very low voltage range. In addition, space-charge-limited conduction is a mechanism in which a space charge is generated in the dielectric by electrons injected from the electrode at a very high E-field and conduction. SCLC depends only on carrier mobility, and I-V characteristics show I-V^2. If the ohmic conduction is conduction by the mobile carrier, it can be regarded as conduction by the space charge generated by the injected electrons. Ionic conduction is appeared due to the movement of ions in the E-field (the presence of a lattice defect in the dielectric), which is generally insignificant in dielectrics because the ion mass is too large. And grain-boundary-limited conduction in poly-dielectric, since the resistivity of the grain boundary is much larger than that of grain, there is a grain boundary energy barrier. This has a relationship that increases as the dielectric constant is lowered. [94,96-102] As described above, factors that can affect the conduction mechanism in the dielectric include temperature, E-field, stress condition, device structure, material (dielectric, electrode), film thickness, and deposition method. Therefore, the current conduction analysis in the dielectric suitable for the device environment should be carried out. A summary of the current conduction mechanism described above is summarized in **Table 2.2**. And as shown in **Fig. 2.26**, SC emission, P-F emission, and F-N tunneling conduction phenomena can be analyzed in the damascene Cu/low-k interconnect system. [48,94,96]

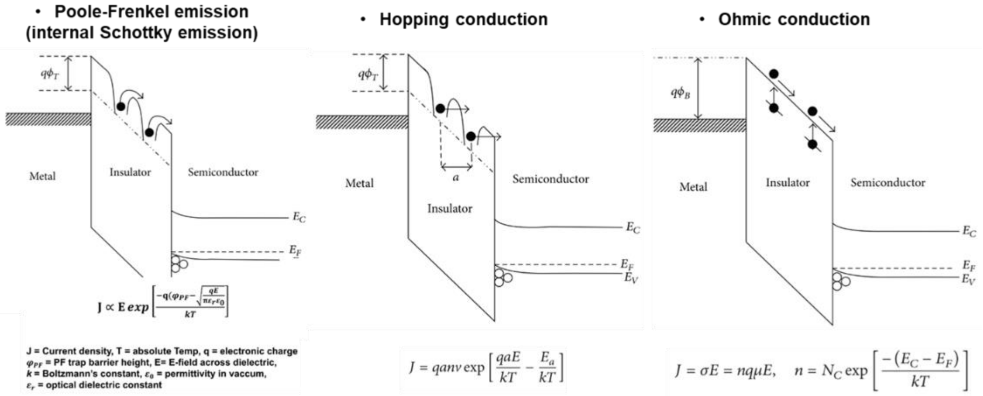

• Poole-Frenkel emission (internal Schottky emission)
• Hopping conduction
• Ohmic conduction
$q\phi_T$
Metal
Insulator
Semiconductor
E_C
E_F
$J \propto E\, exp\left[\frac{-q(\varphi_{PF}-\sqrt{\frac{qE}{\pi\varepsilon_r\varepsilon_0}})}{kT}\right]$
J = Current density, T = absolute Temp, q = electronic charge
φ_{PF} = PF trap barrier height, E= E-field across dielectric,
k = Boltzmann's constant, ε_0 = permittivity in vaccum,
ε_r = optical dielectric constant
$q\phi_T$
a
Metal
Insulator
Semiconductor
E_C
E_F
E_V
$J = qanv \exp\left[\frac{qaE}{kT} - \frac{E_a}{kT}\right]$
$q\phi_B$
Metal
Insulator
Semiconductor
E_C
E_F
E_V
$J = \sigma E = nq\mu E, \quad n = N_C \exp\left[\frac{-(E_C - E_F)}{kT}\right]$

Figure 2.25 Bulk-limited conduction mechanisms: Poole-Frenkel emission, hopping conduction, Ohmic conduction.[94,96-102]

Table 2.2 Comparison of current conduction mechanisms in dielectrics: electrode-limited conduction mechanism depends on the electrical properties (barrier height) at interface between electrode and dielectric and bulk-limited conduction mechanism depends only on the properties of dielectric itself. (i.e., trap level, spacing, density)[48,94-102]

Category of conduction	Space-charge-limited conduction (SCLC)	Schottky emission	Poole-Frenkel emission	Fowler-Nordheim Tunneling
Current conduction	Transport-limited conduction	Injection-limited conduction	Transport-limited conduction	Injection-limited conduction
Assumption	If free-carrier density in oxide < accumulated electron density, electron injection from oxide is initiated and forms space charge.	Field-assisted thermionic emission of an electron over a surface barrier	Field-assisted thermal de-trapping of carrier from bulk oxide to conduction band	When electrons are able to tunnel through a triangular barrier into conduction band of an oxide
Characteristic	@Very low voltage range, Ohm's law, Trap-filled-limit (TFL) emission, Child's law	Highly depends on T	High T & E-field	Non-dependent of T High E-field induced
Linear plot	Log J vs. Log V	$\mathrm{Ln}(J/T^2)$ vs. $E^{1/2}$	$\mathrm{Ln}(J/E)$ vs. $E^{1/2}$	$\mathrm{Ln}(J/E^2)$ vs. $1/E$

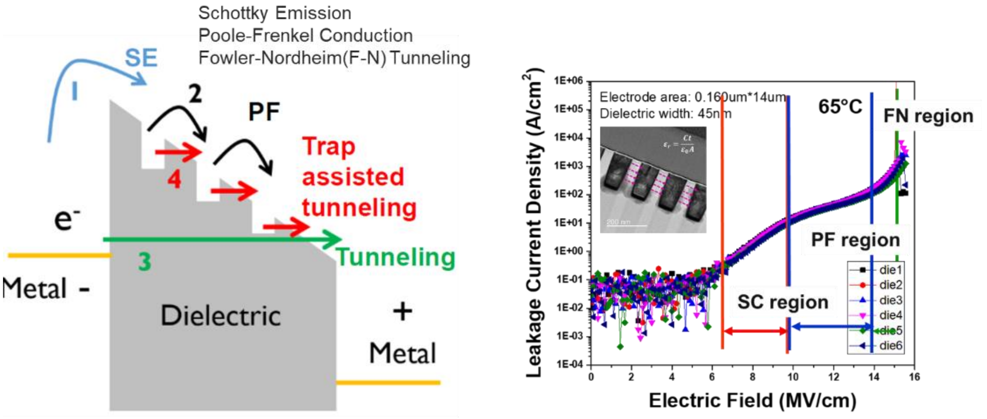
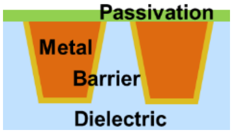
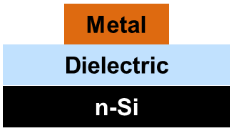
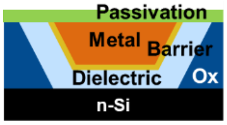


Figure 2.26 Current conduction mechanism in dielectric and identification of current conduction in damascene Cu interconnects.[103]

2.3.2 Reliability test vehicles

Table 2.3 and **Fig. 2.27** is information about reliability test vehicles. Film level MIS capacitor is a structure mainly used to check the stability of metal/low-k interface, and since C-V analysis is possible, properties such as thickness and impurity concentration of dielectric film can be measured. While time to failure test is difficult in MIS structure, it is possible in interconnect test chip (MIM) structure, and the effect of line edge roughness (LER) and dielectric damage can be confirmed. In case of low-k planar capacitor and p-cap, it is a failure test structure that reflects the interconnect structure, and moisture absorption effect, barrier effect, and plasma characteristics can be obtained through the capping layer.

Table 2.3 Reliability test vehicles: damascene structure (MIM), metal-insulator-silicon planar capacitor structure (MIS), low-k planar capacitor (p-cap). [104-107]

Test vehicles	Damascene (MIM) Interconnect test chips	MIS Metal-Insulator-Silicon planar capacitor	P-cap Low-k planar capacitor
Structure	 Passivation Metal Barrier Dielectric	 Metal Dielectric n-Si	 Passivation Metal Barrier Dielectric Ox n-Si
Fabrication	High	Low	High
Analysis Level	Device failure, bulk dielectric breakdown	Metal/dielectric interface, bulk dielectric breakdown	Metal/Low-k interface, bulk dielectric breakdown
Advantage	Device level reliability test	Motion of impurities, quality of dielectric film (E=V/thickness of dielectric)	Undamaged low-k/barrier (damage free), No moisture uptake
Disadvantage	Process variability (LER, plasma exposure, CMP residue, misalignment, interface leakage)	Moisture uptake, inadequate to device failure dynamics w/ process variability	Included CMP process, inadequate to device failure dynamics w/ process variability

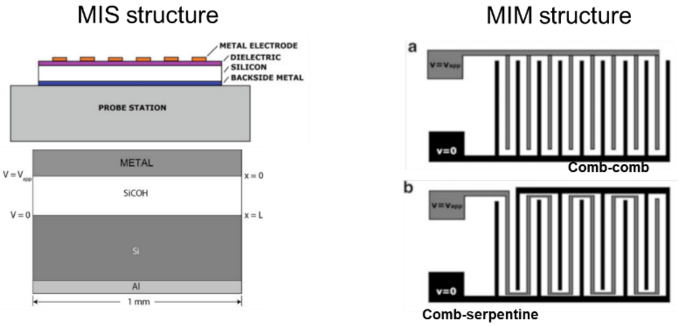
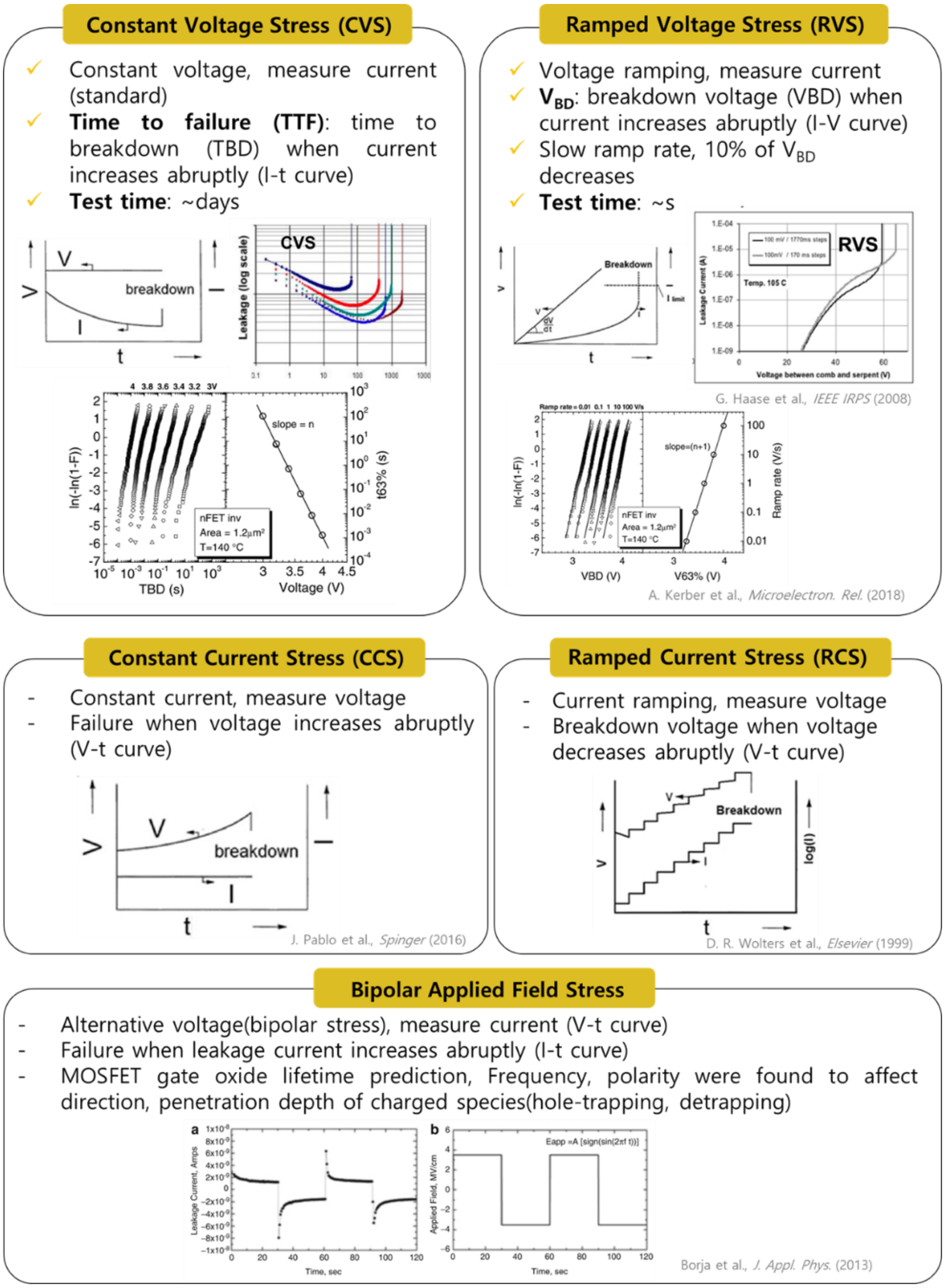

MIS structure
METAL ELECTRODE
DIELECTRIC
SILICON
BACKSIDE METAL
PROBE STATION
METAL
$V = V_{app}$
$x = 0$
SiCOH
$V = 0$
$x = L$
Si
Al
1 mm
MIM structure
a
$V = V_{app}$
v=0
Comb-comb
b
$V = V_{app}$
v=0
Comb-serpentine

Figure 2.27 Test vehicles: MIS vs. MIM.[104,108-109]

2.3.3 Dielectric breakdown assessment

The dielectric breakdown assessments are summarized as in **Fig. 2.28**. The constant voltage stress (CVS) method is the most used and measures the leakage current after applying a constant voltage. The section in which the current rapidly increases in the I-t curve is defined as time to failure, TTF. This is a method that takes several days or more depending on the sample. The voltage ramping stress (RVS) method, which can be confirmed relatively quickly, measures the leakage current while increasing the voltage linearly. Here, the breakdown voltage, V_{BD}, is defined as a sudden increase in current in the I-V curve. It has been experimentally reported that breakdown voltage can be reduced by about 10% depending on the ramping rate. Next is the constant current stress (CCS) method, which measures the voltage by applying a constant current. Here, the breakdown voltage is defined as a rnage in which the voltage rapidly decreases in the V-t curve. In a similar way, the method of measuring the voltage while increasing the current linearly is called ramped current stress (RCS). The section in which the voltage rapidly decreases is defined as breakdown voltage. Finally, there is the bipolar applied field stress (BAFS) method. If the previous method checks the failure behavior when the direct current flows, it is a method to measure the leakage current when AC bias is applied. When the current suddenly increases in the I-t curve, the failure region is defined and used to predict the lifespan of the MOSFET gate oxide. Failure is affected by frequency and polarity. [104,110-114]



Constant Voltage Stress (CVS)

- ✓ Constant voltage, measure current (standard)
- ✓ **Time to failure (TTF)**: time to breakdown (TBD) when current increases abruptly (I-t curve)
- ✓ **Test time**: ~days

V
I
breakdown
t
CVS
Leakage (log scale)
4 3.8 3.6 3.4 3.2 3V
ln(-ln(1-F))
TBD (s)
slope = n
nFET inv
Area = 1.2μm²
T=140 °C
t63% (s)
Voltage (V)

Ramped Voltage Stress (RVS)

- ✓ Voltage ramping, measure current
- ✓ $\mathbf{V_{BD}}$: breakdown voltage (VBD) when current increases abruptly (I-V curve)
- ✓ Slow ramp rate, 10% of V_{BD} decreases
- ✓ **Test time**: ~s

Breakdown
V
I
I limit
dV/dt
t
RVS
Temp. 105 C
Leakage Current (A)
Voltage between comb and serpent (V)
Ramp rate = 0.01 0.1 1 10 100 V/s
ln(-ln(1-F))
slope=(n+1)
nFET inv
Area = 1.2μm²
T=140 °C
VBD (V)
V63% (V)
Ramp rate (V/s)

G. Haase et al., *IEEE IRPS* (2008)

A. Kerber et al., *Microelectron. Rel.* (2018)

Constant Current Stress (CCS)

- Constant current, measure voltage
- Failure when voltage increases abruptly (V-t curve)

V
I
breakdown
t

J. Pablo et al., *Spinger* (2016)

Ramped Current Stress (RCS)

- Current ramping, measure voltage
- Breakdown voltage when voltage decreases abruptly (V-t curve)

V
I
Breakdown
log(I)
t

D. R. Wolters et al., *Elsevier* (1999)

Bipolar Applied Field Stress

- Alternative voltage(bipolar stress), measure current (V-t curve)
- Failure when leakage current increases abruptly (I-t curve)
- MOSFET gate oxide lifetime prediction, Frequency, polarity were found to affect direction, penetration depth of charged species(hole-trapping, detrapping)

a
Leakage Current, Amps
Time, sec
b
Applied Field, MV/cm
Eapp =A [sign(sin(2πf t))]
Time, sec

Borja et al., *J. Appl. Phys.* (2013)

Figure 2.28 Dielectric breakdown assessment: constant voltage stress (CVS), ramped voltage stress (RVS), constant current stress (CCS), ramped current stress (RCS), bipolar applied field stress (BAFS).[104,110-114]

2.3.4 Dielectric breakdown mechanisms

Looking at **Fig. 2.29**, dielectric breakdown behavior is classified into an extrinsic breakdown behavior and an intrinsic breakdown behavior. Extrinsic breakdown refers to a phenomenon in which metal ions such as Cu ion diffuse and drift into the dielectric by temperature and electric field to form Cu filaments and breakdown. Conversely, in the case of Al interconnects, since Al does not move into Si, extrinsic failure is not observed. The dielectric breakdown behavior in the Al interconnects is an intrinsic failure, which is a result of Si-O bond breakage due to thermal chemical stress. In **Fig. 2.30**, in the Cu/SiO_2 system, the current gradually increases and then suddenly increases. On the other hand, Al/SiO_2 shows an intrinsic failure behavior that increases suddenly after no current flows. [115-116]

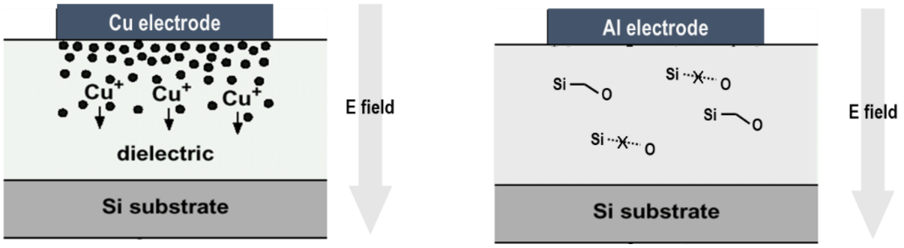


Figure 2.29 Dielectric breakdown mechanisms: extrinsic breakdown; percolation paths are formed extrinsically due to Cu ions, intrinsic breakdown; broken bonds by dipole-dipole interaction or injected electrons from cathode can form conductive paths.[115]

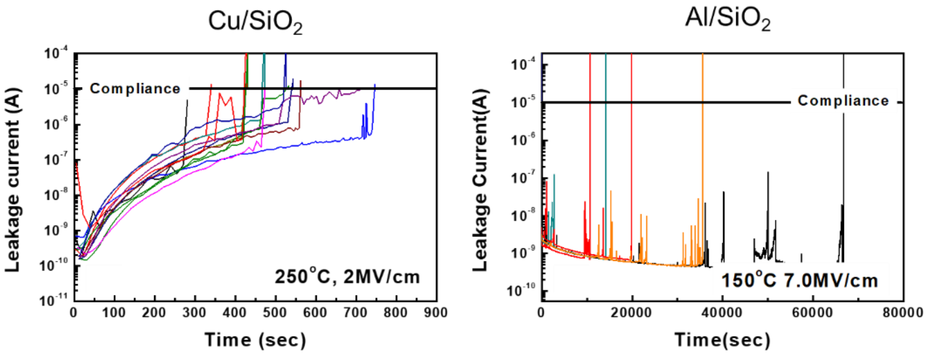


Figure 2.30 Dielectric breakdown mechanisms: the gradual increase in leakage current was observed in Cu/SiO_2 sample under BTS, while sample of Al/SiO_2 was not.[116]

2.3.5 Reliability test: VRDB and TDDB

As shown in **Fig. 2.31**, reliability test methods are divided into wafer-level reliability (WLR) test and package-level reliability (PLR) test. [55, 111] A typical WLR method is voltage ramped dielectric breakdown (VRDB) and checks the current change while sweeping the voltage. The measurement time itself is very fast and it is generally used to check the quality of the material. The PLR method, time dependent dielectric breakdown (TDDB), is a method of measuring current until breakdown by applying a constant voltage and temperature. In general, it is used to predict the lifetime of a device. TDDB is a useful tool to identify intrinsic and extrinsic wear failure mechanisms. Integrated circuit (IC) performance can be evaluated for semiconductor wear mechanisms by evaluating TDDB under given operating conditions. The breakdown model can be used to predict the failure time of a component due to TDDB.

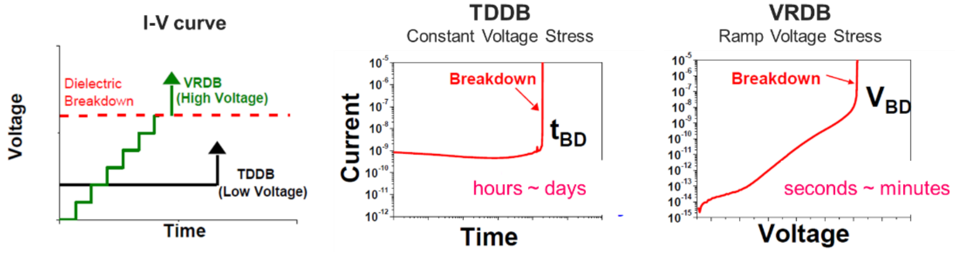
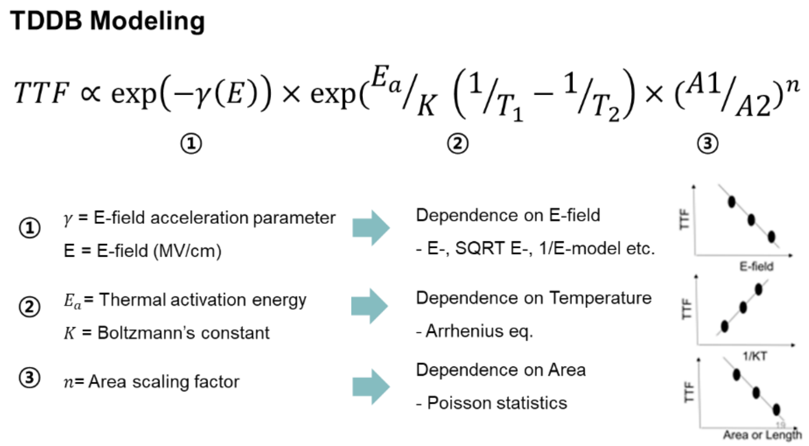


Figure 2.31 Reliability test methods: Ramp voltage stress (VRDB) and time dependent dielectric breakdown (TDDB).[55,111]

2.3.6 Lifetime models

Using the TDDB analysis result, the lifetime of the device can be predicted. As shown in **Fig. 2.32**, the factors of TDDB modeling include electric field, temperature, and device area. According to the influence of each factor, voltage accelerating models have been proposed. In general, the lifetime evaluation process calculates the device failure time through VRDB and TDDB analysis as shown in **Fig. 2.33**. The process in which failure occurs due to the formation of metal filaments in the dielectric is represented by probability distribution. Therefore, semi-empirical lifetime statistics are processed using the Weibull distribution function. And the 10-year lifetime is evaluated using the voltage acceleration models. [52] Numerous voltage acceleration models have been proposed, but they are still controversial research areas. It is summarized in **Table 2.4** and **Fig. 2.34**. [117-123]



TDDB Modeling

$$TTF \propto \exp(-\gamma(E)) \times \exp({}^{E_a}/_{K}\ ({}^{1}/_{T_1} - {}^{1}/_{T_2})) \times ({}^{A1}/_{A2})^n$$

① ② ③

① γ = E-field acceleration parameter
E = E-field (MV/cm)
→ Dependence on E-field
- E-, SQRT E-, 1/E-model etc.

② E_a = Thermal activation energy
K = Boltzmann's constant
→ Dependence on Temperature
- Arrhenius eq.

③ n = Area scaling factor
→ Dependence on Area
- Poisson statistics

Figure 2.32 TDDB modeling: The dielectric breakdown lifetime has dependence on electric field, temperature, and area.[52]

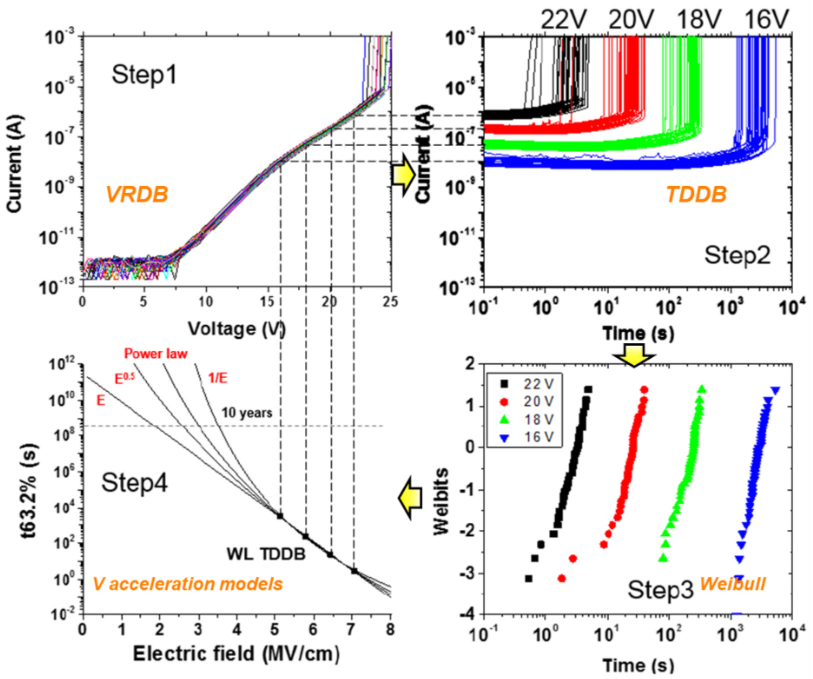


Figure 2.33 TDDB Lifetime assessment: VRDB (Step 1), TDDB (Step 2), Weibull plotting (Step 3), voltage acceleration modeling (Step 4).[52]

Table 2.4 Voltage acceleration models.[117-124]

Voltage acceleration models	TTF dependence	Breakdown physics
E (= Thermochemical model)	$A\exp(-\boldsymbol{\Upsilon} E)$	Thermal energy breaks the Si-O bond (Thermo-chemical)
√E (SQRT E)	$A_{RE}\exp(-\boldsymbol{\Upsilon}_{RE}\sqrt{E})$	Cu diffusion PF conduction, Schottky conduction
Power Law (PL)	$A_{PL}E^{-\gamma}$	Hydrogen induced defects The interaction of release H with weak
Impact Damage (ID) (= Lucky electron model)	$A_{ID}\exp(\frac{\boldsymbol{\beta}}{\boldsymbol{E}}-\boldsymbol{\Upsilon}_{ID}\sqrt{E})$	PF conduction (Lucky electron) + (momentum transfer
E^2 (E square)	$A\exp(\boldsymbol{E_a}-\frac{\boldsymbol{\Upsilon E^2}}{\boldsymbol{KT}})$	Lucky electron with Cu Cu ion polarization effect
1/E (= Anode hole injection)	$A\exp(\frac{\boldsymbol{\alpha}}{\boldsymbol{E}})$	FN tunneling, high energy hole-induced damage

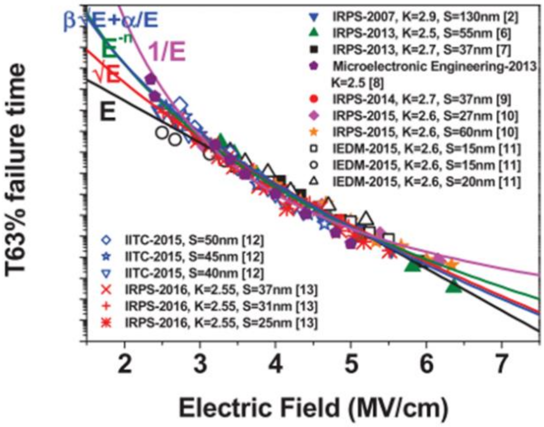


Figure 2.34 TDDB E-field acceleration models: accurate lifetime prediction of devices using various acceleration models is still controversial.[124]

CHAPTER 3

Experimental procedures

3.1. Thin film deposition

3.1.1. Substrate preparation

A *p*-type silicon (100) wafer (resistivity: 1 – 10 Ω·cm) was used to fabricate the thin film sample and MIS device. In order to remove the intrinsic oxide from the Si wafer, sulfuric acid peroxide mixture (SPM) cleaning and dilute hydrofluoric acid (DHF) cleaning were performed. The cleaned substrates were thoroughly rinsed with deionized water (DIW) and dried using wafer spin dryer. The conditions for each process are as follows.

SPM cleaning	H_2SO_4:H_2O_2 = 4:1, 130 °C, 10 min
DIW cleaning	deionized water, 5 min
DHF cleaning	DIW:HF = 10:1, 2 min
DIW cleaning	deionized water, 5 min

3.1.2. Oxidation

Then, as shown in **Fig. 3.1,** the SiO_2 films were thermally grown to a thickness of 100 nm on Si wafer using dry oxidation method (SELTRON, SHF-150). In the case of the MIS device sample, 30 nm thick TEOS dielectric (tetraethoxy silane, Soulbrain Co. Ltd.) was deposited using the CVD method.

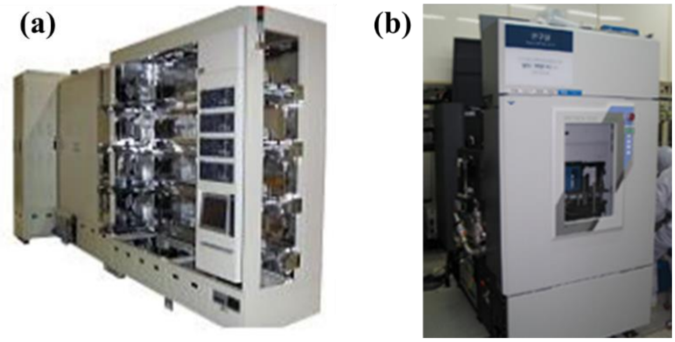


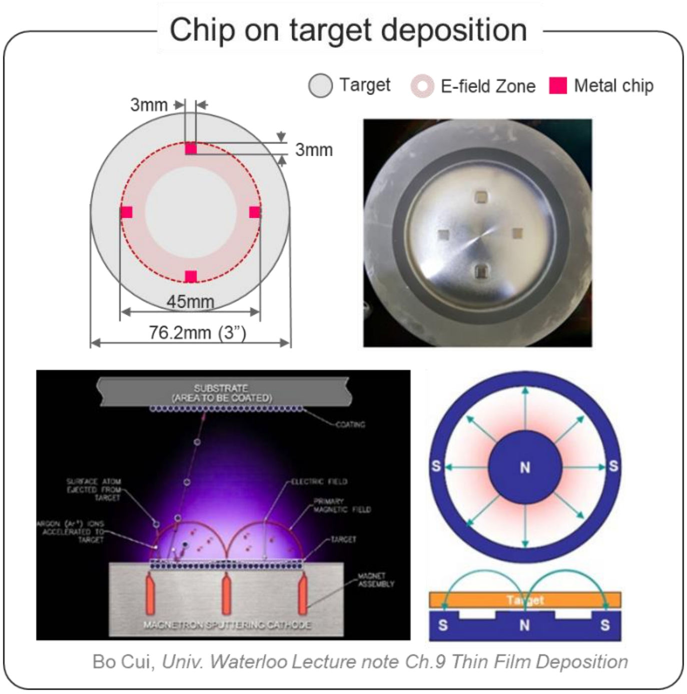
Figure 3.1 Oxide thickness measurement using an ellipsometer: (a) dry oxidation process; 100 nm SiO_2 was deposited using a SELTRON (SHF-150). (b) CVD TEOS was deposited using Applied Material Korea (P-5000 IV).

3.1.3. Co alloy deposition using DC magnetron sputtering

In this experiment, Co alloy thin film and MIS structure were fabricated using DC magnetron sputtering deposition system (ULTECH Co.,). The detailed conditions for sputtering are described in **Table 3.1**. The 3-inch targets used in this experiment are Co, Co (5 at% Cr), and Co (10 at% Cr), and a chip on target deposition method was used to make a Co alloy thin film. As shown in **Fig. 3.2**, a dopant chip is placed on a Co target and deposited to obtain a doped Co alloy thin film. There are 9 types of dopant metal chips (Cr, Fe, Zn, Mg, Al, Ni, Sn, Cu, and Mn) used, and the doping concentration was increased by increasing the number of chips from 1 to 4. The reason for using the chip on target method is that it is possible to quickly verify the material of various alloy materials without the need to manufacture a target for each composition. Also, in the case of alloy with high doping concentration, it has a great effect on resistivity, so it is a very easy deposition method to control a small amount of doping concentration.

Table 3.1 Sputtering process parameters.

Method	DC Sputter
Thin film/substrate	100 nm SiO_2/*p*-Si (10 mm × 10 mm × 525±25 μm)
MIS die size/substrate	30 nm TEOS/*p*-Si (5 mm × 5 mm × 525±25 μm)
Target material	Co (6N)
Dopant	Cr, Zn and 7 other chips (3 mm × 3 mm)
Initial pressure	~ 2.5×10^{-6} Torr (0.0003 Pa)
Working pressure	4 mTorr
Substrate temperature	RT
Power	100 W_{DC}
Dep. rate	29.44 ~ 36.63 nm/s
Film thickness	~ 150 nm
Post annealing	150 ℃, 250 ℃, 350 ℃, 450 ℃


Chip on target deposition
Target
E-field Zone
Metal chip
3mm
3mm
45mm
76.2mm (3")
SUBSTRATE
(AREA TO BE COATED)
COATING
SURFACE ATOM EJECTED FROM TARGET
ARGON (Ar⁺) IONS ACCELERATED TO TARGET
ELECTRIC FIELD
PRIMARY MAGNETIC FIELD
TARGET
MAGNET ASSEMBLY
MAGNETRON SPUTTERING CATHODE
S
N
S
Target
S
N
S

Bo Cui, *Univ. Waterloo Lecture note Ch.9 Thin Film Deposition*

Figure 3.2 Chip on target deposition: Co alloy thin films and MIS samples were deposited by placing a dopant chip on the Co target.

As shown in **Fig. 3.3**, the deposition rate of the pure Co target was investigated with plasma power (50 W, 100 W, 150 W) and wafer position (center and edge). In the case of the thin film sample, since the active layer was deposited with a thickness of 150 nm, the 100 W condition was most suitable, and the sample was placed on the edge with better uniformity. The deposition rate of Co-Cr alloy was investigated as shown in **Fig. 3.4** according to the number of chips. The deposition rates of the remaining Co alloy samples were also performed as shown in **Fig. 3.5**.

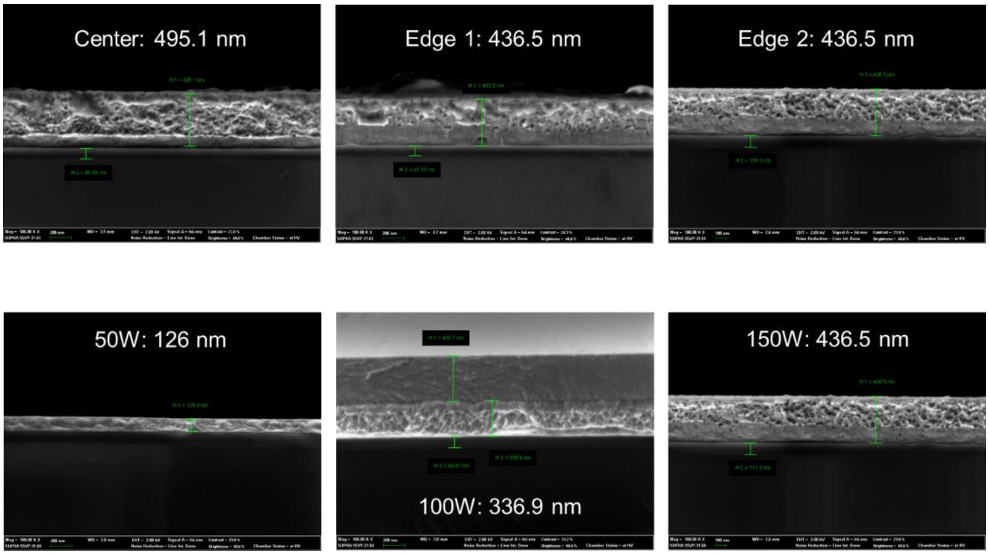

Center: 495.1 nm
Edge 1: 436.5 nm
Edge 2: 436.5 nm
50W: 126 nm
100W: 336.9 nm
150W: 436.5 nm

Figure 3.3 Target deposition rate of pure Co: confirmation of deposition rate with deposition uniformity (center to edge) and plasma powers (50 W, 100 W, 150 W).

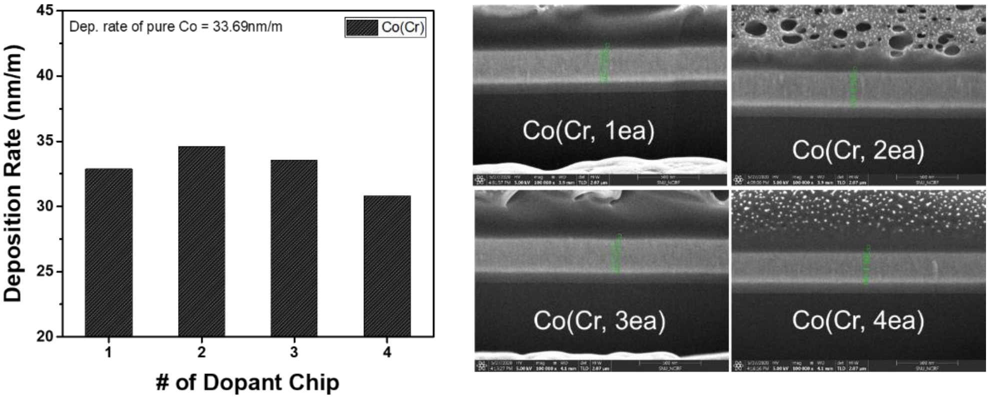


Figure 3.4 Co-Cr alloy deposition rate change: the deposition rate was investigated according to the number of Cr chips (1 ea ~ 4 ea).

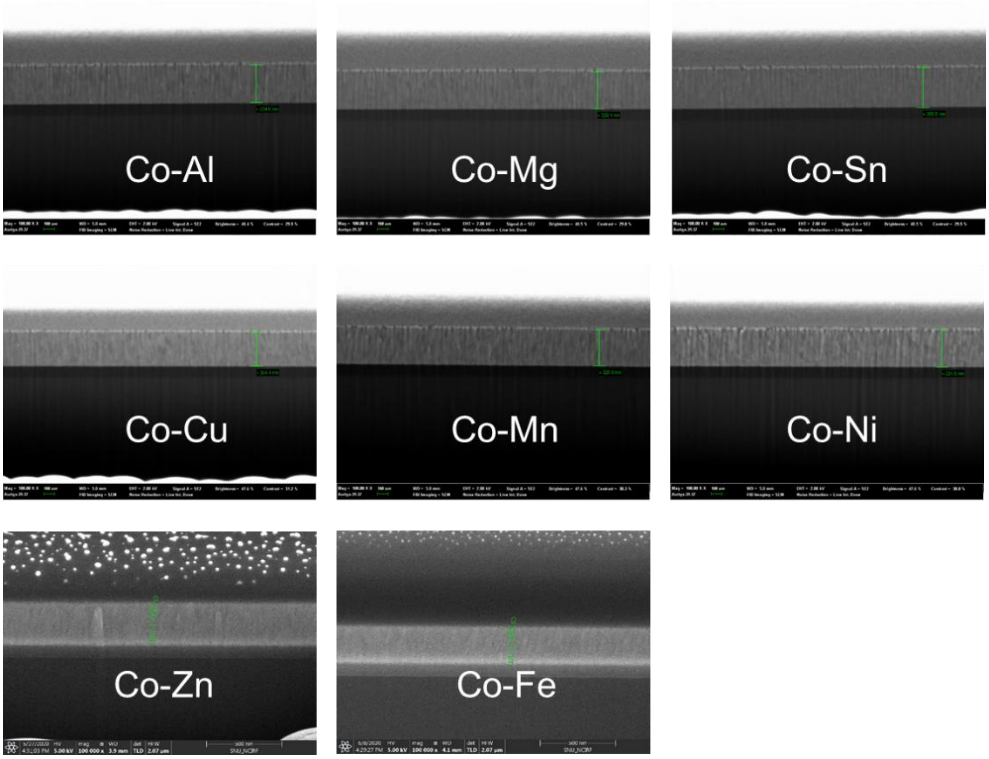


Figure 3.5 Co alloy deposition rate investigation: thickness check of 8 different dopant metals. (100 W, 4 mTorr, 10 minutes)

3.1.4. Annealing process

As shown in **Fig. 3.6** and **Fig. 3.7**, the sample annealing process was performed. In the case of thin film samples, heat treatment was performed in a vacuum chamber to induce surface diffusion behavior. When designing this experiment, it was determined that bi-layer resistivity analysis would be possible if self-forming barrier behavior was observed. However, since it is difficult to accurately control the dopant concentration when the chip-on target deposition method is used, even after the self-forming barrier is formed, the dopant is still present on the Co matrix, making it difficult to accurately analyze the resistivity. Next, the MIS device was subjected to wafer-level annealing in an N_2 atmosphere. Wafer-level annealing was performed to control the self-forming barrier uniformity on the wafer, and as a result, it was confirmed that the barrier formation uniformity was well formed throughout the wafer.

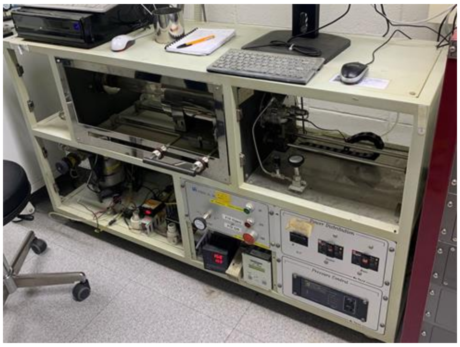
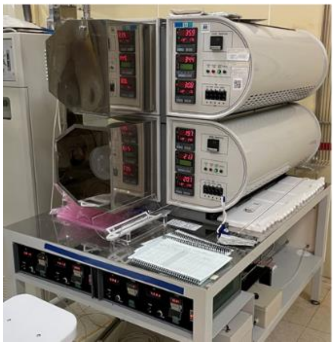


Figure 3.6 Vacuum furnace: thin film samples were subjected to vacuum annealed (< 0.0013 Pa) for surface diffusion.



Seoul Electronics Co. (SMF-800)	
Annealing temperature range	450 °C – 1000 °C
Temperature uniformity	± 2 °C
Gas	N_2 4 SLPM

Figure 3.7 Wafer-level heat treatment furnace: MIS samples were subjected to annealed under N_2 atmosphere for barrier self-forming.

3.2. Thin film characterization

3.2.1. Sheet resistance

To obtain the resistivity of the thin film, the sheet resistance was measured as shown in **Fig. 3.8**. Since sheet resistance generally considers the thin film itself as one layer, when measuring a bi-layer sample, it is necessary to calculate the resistivity of each thin film. Through **Fig. 3.9** and **Eq. 3.1**, the resistivity in the bilayer can be calculated, and when one thin film is very small, it can be expressed as the resistivity of the other thin film. [125]

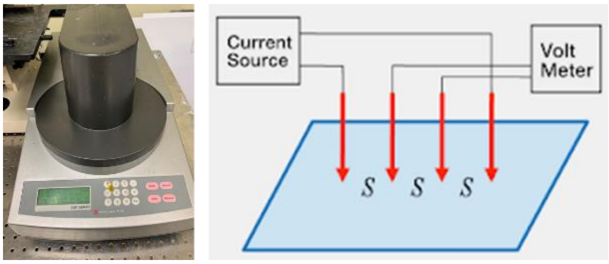


Figure 3.8 Sheet resistance measurement using 4-point probe method.[125]

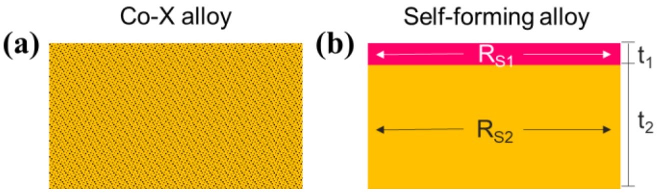


Figure 3.9 Sheet resistance measurement in bi-layer: (a) in case of alloy, the sheet resistance increases due to more scattering sites, but it is assumed that it is a single layer. (b) in the case of a self-forming barrier, it should be calculated considering that it is a bilayer. However, the data

should be compared considering whether the dopant is present in the mother phase and whether the doping concentration is the same.

$$\text{Sheet resistance}, R_S = 4.53\frac{\Delta V}{I} \tag{3.1}$$

$$\text{Resistivity}, \rho = \mathrm{R}_S \times thickness$$

$$\mathrm{Rs} = \frac{R_{S1} \times R_{S2}}{R_{S1} + R_{S2}}, \qquad R_{S1} = \frac{\rho_1}{t_1}, R_{S2} - \frac{\rho_2}{t_2}$$

$$\text{If } t_1 \ll t_2,\ R_S \cong R_{S2}$$

3.2.2. X-ray photoelectron spectroscopy (XPS)

The basic principle of photoelectron spectroscopy is that when X-rays (Al Kα 1486.6 eV) with constant energy are irradiated onto the target surface (1 – 10 nm thick), photoelectrons are emitted. By measuring the kinetic energy of these photoelectrons, the binding energy required to emit the photoelectrons from the sample can be calculated. In **Eq. 3.2**, KE is kinetic energy, *h* is Planck constant (6.62×10^{-34} m^2kgs^{-1}), ν is photon's frequency, BE is binding energy, ϕ_s is spectral work function (spectrometer work function). The element composition ratio, chemical bond state between elements, and depth profile of the thin film were measured using a photoelectron spectrometer (NEXSA, Thermo Fisher Scientific) located at the Jinju Center of the Korea Institute of Ceramic Engineering and Technology (KICET). At the time of measurement, the 30s etching process was first performed in order to remove the native oxide on the surface of the thin film. The measured data was corrected for 284.6eV C1s peak to remove hydrocarbon noise. As shown in **Fig. 3.10**, in the case of the MIS sample, the patterned dot diameter was 100 μm, which was smaller than the XPS analysis area of 400 μm, so there were problems with poor resolution or difficult quantitative analysis.

$$KE = h\nu - BE - \emptyset_s \tag{3.2}$$

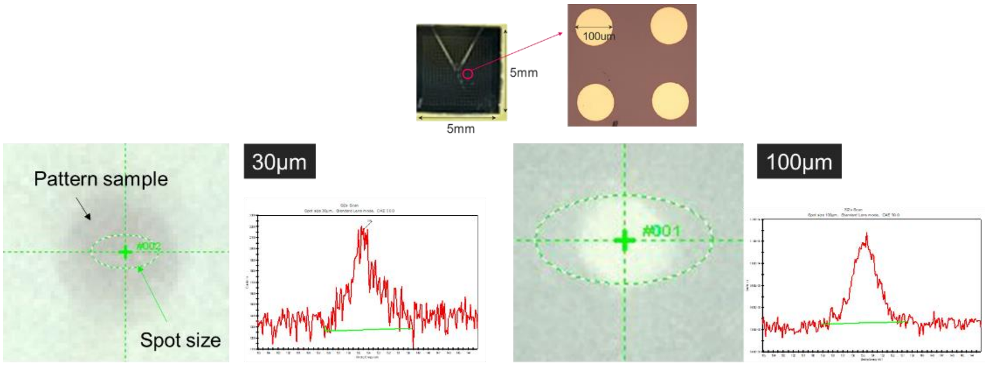


Figure 3.10 XPS analysis area and pattern sample size problem: It is difficult to get accurate quantitative analysis results from pattern MIS structure.

3.3. Metal-Insulator-Semiconductor (MIS) device fabrication

3.3.1. Patterning using lift-off process

Fig. 3.11 is a process schematic diagram of a Metal-Insulator-Semiconductor (MIS) device. 300Å TEOS was deposited on the p-Si wafer after SPM and BOE cleaning. And patterning was carried out using AZ4330 photoresist (positive PR) and lift-off photolithography process. The liftoff process is detailed in **Fig. 3.12** and **Table 3.2**. After the lift-off process, the PR thickness was measured using a 3D profiler (DEKTAK XT-A), and as a result, it was confirmed to be 2.2 μm to 2.6 μm. Using sputtering equipment, pure Co, Co/TiN, Co/TiN/Ti, Co-Cr alloy, and Co alloy thin films were deposited as active layers. After that, it was passivated using Ta. This is to induce the dopant to react with TEOS (SiO_2) during the annealing process. Ta passivation was used as a metal capping layer to increase the driving force reacting with oxygen. [42] Next, the bottom and top electrodes were deposited using an e-beam evaporator (MAESTEK, ZZS550-2/D). The Al bottom electrode was deposited to a thickness of 500 nm at a deposition rate of 5 Å/s. An 80 nm Au top electrode (3 Å/s) and a 20 nm Ti adhesion layer (1 Å/s) were performed after the Ta process. As shown in **Fig. 3.7**, annealing was performed in wafer level. The annealing temperature and time were 250 °C/350 °C/450 °C and 2 hours, respectively. The fabricated sample was dicing 5 mm × 5 mm through a dicing saw (DAD525, DISCO) process.

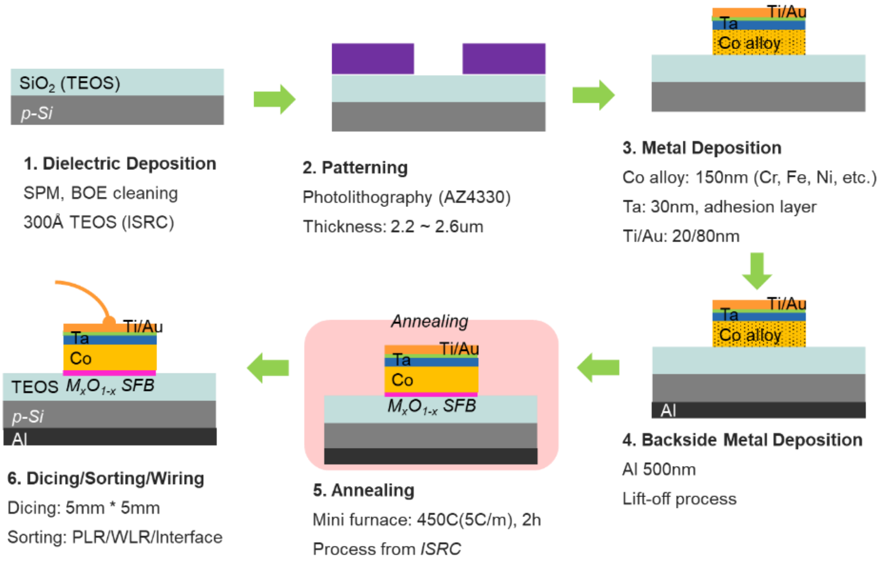

SiO$_2$ (TEOS)
p-Si
1. Dielectric Deposition
SPM, BOE cleaning
300Å TEOS (ISRC)
2. Patterning
Photolithography (AZ4330)
Thickness: 2.2 ~ 2.6um
Ti/Au
Ta
Co alloy
3. Metal Deposition
Co alloy: 150nm (Cr, Fe, Ni, etc.)
Ta: 30nm, adhesion layer
Ti/Au: 20/80nm
Ti/Au
Ta
Co alloy
Al
4. Backside Metal Deposition
Al 500nm
Lift-off process
Annealing
Ti/Au
Ta
Co
M_xO_{1-x} SFB
5. Annealing
Mini furnace: 450C(5C/m), 2h
Process from ISRC
Ti/Au
Ta
Co
TEOS M_xO_{1-x} SFB
p-Si
Al
6. Dicing/Sorting/Wiring
Dicing: 5mm * 5mm
Sorting: PLR/WLR/Interface

Figure 3.11 Fabrication flow of MIS device: all MIS devices are fabricated using a lift-off lithography process.

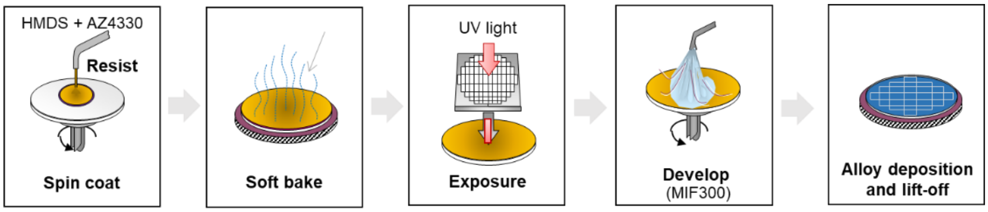

HMDS + AZ4330
Resist
Spin coat
Soft bake
UV light
Exposure
Develop
(MIF300)
Alloy deposition
and lift-off

Figure 3.12 Process flow of lift-off photolithography.

Table 3.2 Process recipe of photolithography using AZ4330 photoresist.

Photolithography	Condition (AZ4330 PR)
HMDS coating 1	1000 rpm / 10 s
HMDS coating 2	1500 rpm / 30 s
PR apply	0 rpm / 10 s
PR coating 1	1500 rpm / 15 s
PR coating 2	4000 rpm / 35 s
Soft bake	95 ℃ / 90 s
Release	RT / 60 s
Exposure	20 s
Develop	10 m – 15 m

3.3.3. TDDB packaging

As shown in **Fig. 3.13**, packaging for TDDB analysis was performed using the die samples. A 28-lead side brazed package manufactured by Kyocera Co. was used and the die was fixed using Ag paste. After that, wiring bonding was performed on the upper and lower electrodes of the two devices to perform TDDB analysis.

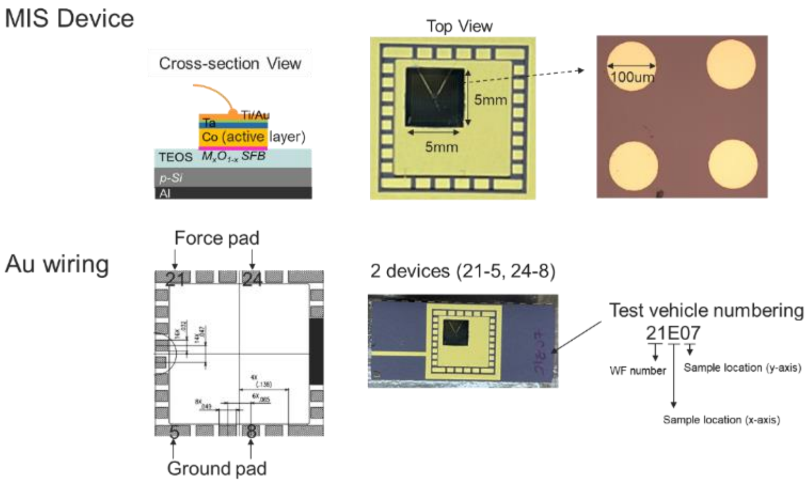

MIS Device
Cross-section View
Ti/Au
Ta
Co (active layer)
TEOS M_xO_{1-x} SFB
p-Si
Al
Top View
5mm
5mm
100um
Au wiring
Force pad
21
24
5
8
Ground pad
2 devices (21-5, 24-8)
Test vehicle numbering
21E07
WF number
Sample location (y-axis)
Sample location (x-axis)

Figure 3.13 TDDB packaging: after attaching the die to the ceramic package using silver paste, Au wiring was performed.

3.4. Reliability analysis

3.4.1. Electrical reliability analysis

The I-V characteristics (VRDB) of the fabricated devices were measured using a probe station (Modusystems, Inc. and MSTECH) and a semiconductor parameter analyzer (Keithley 4200A-SCS and Keysight B1500A). In the I-V curve, the voltage was swept from 0 to -80 V in steps of -100 mV. TDDB samples were prepared as Co-Cr interconnects in the form of MIS structures. The TEOS material was used as the dielectric layer and the Ta layer was used as the capping layer. Package-level TDDB experiments were performed under accelerated conditions from 150 °C to 200 °C. The range of current density was DC 6 ~ 10 MV/cm. The compliance current was 0.01 A to determine the time-to-failure (TTF). All TDDB analysis was performed by Samsung Electronics' reliability evaluation team. [52, 126-129]

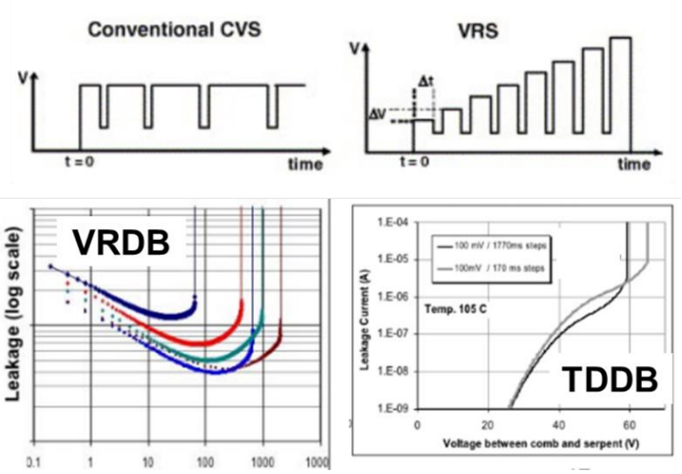


Figure 3.14 VRDB and TDDB measured under constant voltage stress are measured under voltage ramping stress.[52,126-129]

3.4.2. Transmission electron microscopy (TEM) analysis

TEM is a powerful analytical tool that can obtain accurate information about the interface, thickness, microstructure, and chemical composition of materials at the nanoscale. After annealing, TEM and EDS analysis were performed to confirm the formation of the Cr_2O_3 interface. Sampling for TEM analysis were conducted using focused ion beam (FIB) equipment as shown in **Fig. 3.15**. As shown in **Fig. 3.16**, analytical TEM (Talos F200X, JEM-F200(TFEG), 2100F, and Tecnai F20) and energy dispersive X-ray spectrometer (super-X EDS and Oxford EDS) were used to obtain the HRTEM image, line EDS, and EDS mapping.

Helios G4
Thermo Fisher Scientific, USA
NCIRF SNU

Helios 650
FEI USA
NCIRF SNU

NX5000
Hitachi Japan
KIST AAC

Figure 3.15 TEM sampling with focused ion beam (FIB).

Talos F200X
Super-X EDS
FEI, USA
KIST AAC

JEM-F200(TFEG)
JEOL EDS
JEOL Ltd. Japan
NCIRF SNU

2100F
Oxford EDS
JEOL Ltd. Japan
RIAM SNU

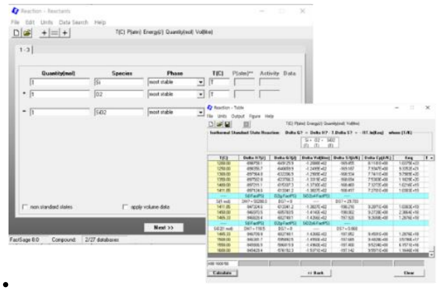
Figure 3.16 Analytical TEM with EDS analysis.

3.5. Computation

3.5.1. Factsage^{TM} calculation

A binary phase diagram calculated by a thermochemical database program (Factsage^{TM} 7.3 software) was used to derive the solubility, intermetallic compound (IMC) formation, and activity coefficients of the Co-X system. [40, 130] The database in this calculation was composed of the Copper alloy database (FScopp), general alloy database (SGTE), FACT light metal (FTlite), steel alloy database (FTstel), Spencer group carbide-nitride-boride-silicide systems (spMCBN), and noble metal alloy database (SGnobl). When calculations could not be performed due to the absence of a material library, binary phase diagrams published by ASM (1986), nishizawa (1984), and elliott were also used. Binary phase diagram calculations of 48 Co-X alloys were performed with temperature variables of 150 °C – 450 °C under atmospheric pressure. The stable phase at the Co-X and SiO_2 interface was calculated at 450 °C and atmospheric pressure, and a binary phase system (out-diffused metal (X) – SiO_2) and a ternary phase system (Co – X – SiO_2) were considered. The concentration before the appearance of a phase other than Cr_2O_3 was defined as the theoretical optimal Cr doping concentration with the annealing temperature.

< Reaction calculation >



< Equilibrium calculation >

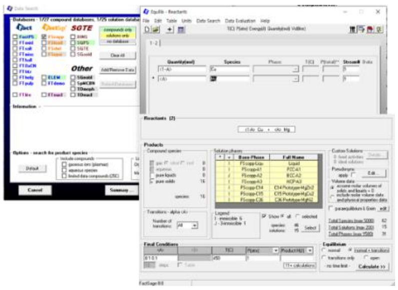


Figure 3.17 Factsage^{TM}: phase diagram, reaction, and equilibrium calculation were used to get thermodynamic properties of Co alloy systems.[130]

3.5.2. Density Functional Theory (DFT) calculation

All DFT calculations were performed within the generalized gradient approximation (GGA) of the Perdew–Burke–Ernzerhof (PBE) functional [131] using the Vienna ab initio simulation package (VASP). [132-133] The plane-wave basis had an energy cut-off of 450 eV. The Brillouin zone was sampled using a 3 × 3 × 1 Monkhorst-Pack mesh. Structural optimization was performed until the force on each atom was less than 0.01 eV/Å. A 2 × 2 supercell of α-Cr_2O_3 slab with thickness of 1.3 nm and a 2 × 2 supercell of TiN slab with thickness of 1.3 nm were modelled. And the vacuum space was set to 20 Å to avoid interactions with periodic images. Energy barriers of Co ion diffusion were calculated with nudged elastic band (NEB) method.

CHAPTER 4

4.1. Material design of Co alloy self-forming barrier

4.1.1. Rule of thumb of Co-X alloy

As shown in **Fig. 4.1**, this study attempted to explore Co alloy self-forming barrier materials using the self-forming barrier methodology. The thermodynamic material design was conducted by dividing the behavior of the self-forming barrier into three major steps (Phase I, II, III). The Cu-Mn alloy selection rules proposed by Professor J. Koike were changed with Co material, and the specific goals were modified in consideration of the roadmap values suggested by ITRS and IRDS. **Table 4.1** sets out specific goals for the modified rule of thumb for Co-X alloy self-forming barrier. As detailed criteria, CMOS compatibility, resistivity, melting temperature, intermetallic compound formation, solubility limit, activity coefficient, diffusivity, oxide formation enthalpy, and reaction phase were used as the criteria for Co self-forming barrier. The criteria to be considered for each behavior will be described in detail below. Phase I is the criteria to be considered in the type of Co alloy. Phase II explained the parts to be considered in the situation where the dopant is outdiffused during the annealing process.

Phase III investigated the factors to be considered when reacting the surface-diffused dopant with the SiO_2 dielectric.

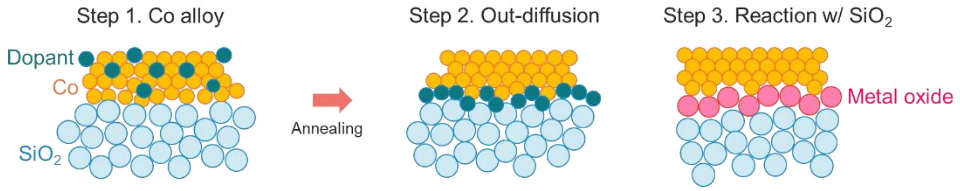


Figure 4.1 Self-forming barrier behaviors (3-step): the rule of thumb for Co-X alloy was designed by dividing the self-forming barrier behavior into three steps.

Table 4.1 Modified rule of thumb for Co-X alloy self-forming barrier: resistivity, intermetallic compound formation, solubility, activity coefficient, diffusivity, oxide formation enthalpy, and reaction phase were used as the selection criteria for Co self-forming barrier.

Criteria	Phase I	Phase II				Phase III	
	Resistivity ($\mu\Omega\cdot cm$)	IMC formation (O / X)	Solubility (at%) @450 °C	Activity coefficient (γ)	Diffusivity (m^2/s)	Oxide formation enthalpy ($-\Delta G^{293}$, kJ/mol of O_2)	Reaction phase w/ SiO_2 @450°C
M in Co	< 20	X	< 5	> 1	$D_{Co} < D_M$	$\Delta G_{Si} < \Delta G_M < \Delta G_{Co}$	oxide or silicate

4.1.2. Co alloy phase

Phase I confirmed what criteria should be considered when designing a Co alloy. In this study, CMOS compatibility, resistivity, and melting point were considered. First, since it is a Co alloy to be applied to semiconductor interconnects, it is necessary to consider whether it is suitable for CMOS process. Therefore, 20 metal materials mainly used in the VLSI process were selected. Among the 20 metals, materials with bulk resistivity higher than 20 μΩ·cm were not suitable as Co alloy materials. As can be seen in **Fig. 1.11**, the bulk resistivity of Co is considered when the metal linewidth is reduced to 10 nm (~ 20 nm pitch). In addition, since the *RC* delay needs to be minimized, if the bulk resistivity is high, the effective resistivity will eventually increase, which inevitably leads to performance degradation. The next thing to consider is the melting temperature. In general, the higher the melting point, the higher the electromigration resistance, so the criterion was set that it should have a melting point at the level of Co, which is the parent phase. Of course, if the melting point is too high, out-diffusion behavior may be difficult to occur. Since the diffusion behavior is temperature dependent, the surface diffusion will not occur sufficiently when the melting point is high. It can also be understood through the homologous temperature (T/T_m). When the interconnect annealing temperature is T, the homologous temperature is low for a high T_m material. It is known that when the homologous temperature is low, the steady-state creep characteristic, which is one of diffusion dependent formation, is generally high. As mentioned earlier, the interesting thing about interconnect research is that you have to catch two rabbits at the same time: performance and reliability, but there is a trade-off relationship between the two! Considering the three criteria, 12 metals (Cr, Fe, Mo, Ni, Ir, Pd, Pt, Rh, Ru, Ta, V, W) could be selected as suitable candidates for Co alloy. Of course, metals with low resistivity but low melting point can be considered as alternative candidates, and 7 metals (Ag, Au, Cu, In, Mg, Zn) were identified.

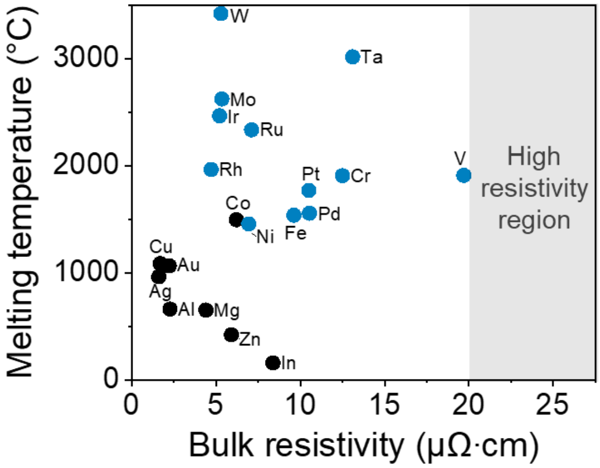


Figure 4.2 Bulk resistivity of CMOS compatible metals: among materials with resistivity lower than 20 µΩ·cm, materials with a melting point higher than Co are marked in blue.

4.1.3. Out-diffusion stage

In Phase II, criteria for diffusion of dopant metal from the Co matrix to the surface during the annealing process were considered. The annealing temperature was carried out at 250 °C, 350 °C, and 450 °C in the experiment, but in the case of material design, it will be explained with values calculated by fixing it at 450 °C. First, the solubility limit and the presence or absence of intermetallic compound (IMC) formation were confirmed. IMC formation and solubility limits in binary Co alloys were calculated using Factsage™ software. Since a solid solution is unstable in a matrix, it can be seen as a phase with a driving force to escape to a stable place. Therefore, we considered a binary alloy with solubility. In addition, as shown in **Fig. 4.3**, if the solubility is too high, resistivity of thin films increases rapidly. 5 at% solubility was set as the limit because it may exist in the Co matrix even after surface diffusion. When IMC is formed, it is known that the driving force for out-diffusion behavior is very low because it is a thermodynamically very stable phase.

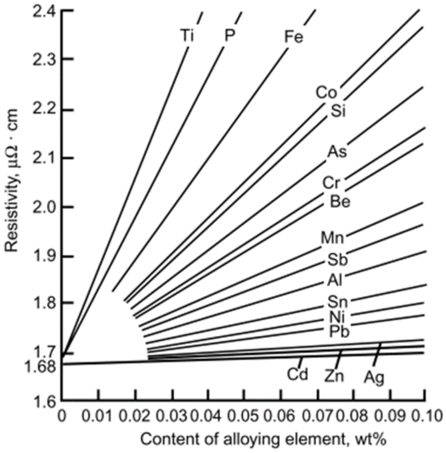


Figure 4.3 Change in resistivity with alloying element concentration.[134]

As shown in **Fig. 4.4**, the solubility limit of Co dopant was defined as dopant solubility at 450 °C. For details, refer to section 3.5 Computation. **Fig. 4.5** shows a representative Co alloy phase diagram considering IMC and solubility. According to the solubility limit of Co-X alloy dopant and intermetallic compound formation, it can be classified into 4 groups: Co-Cr alloy with low solubility and no IMC formation, Co-Mn alloy with high solubility but not forming IMC, Co-Al alloy with low solubility and IMC formation, Co-Sn alloy with high solubility and IMC formation. These are examples of four representative groups. In this study, it is most important that a suitable group as a

Co alloy self-forming barrier criterion has a low solubility limit, and that IMC is not formed.

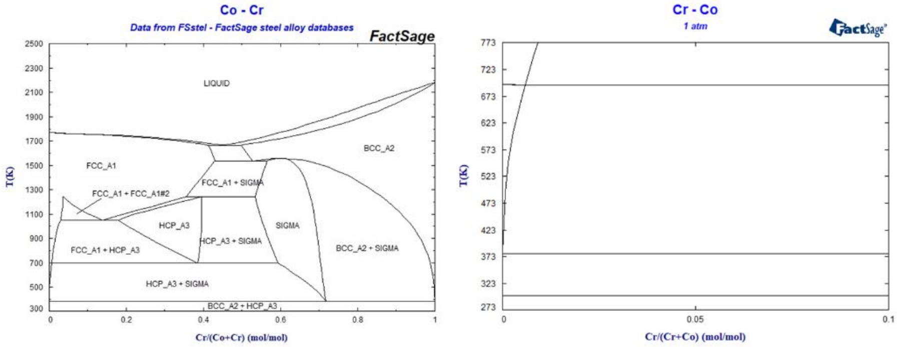


Figure 4.4 Binary phase diagram of Co-Cr: calculate the solubility limit of Cr with annealing temperature (450 °C) and proceed the same for all other dopants.

In **Table 4.2**, the solubility limit with Co and the presence or absence of IMC formation for 39 metals were reported in detail. The comparison results, including CMOS-compatible elements and resistivity criteria, are shown in **Fig. 4.6**. It can be divided into two groups: 6 metals that form IMC (Al, In, Mg, Mo, Ta, W) and 9 metals that do not form IMC (Ag, Au, Cr, Cu, Pd, Ru, Sn, V, Zn). Furthermore, groups with solubility below 1 at% can be considered advantageous in terms of performance, and five metals (Ag, Au, Cr, Cu, Ru) meet this standard.

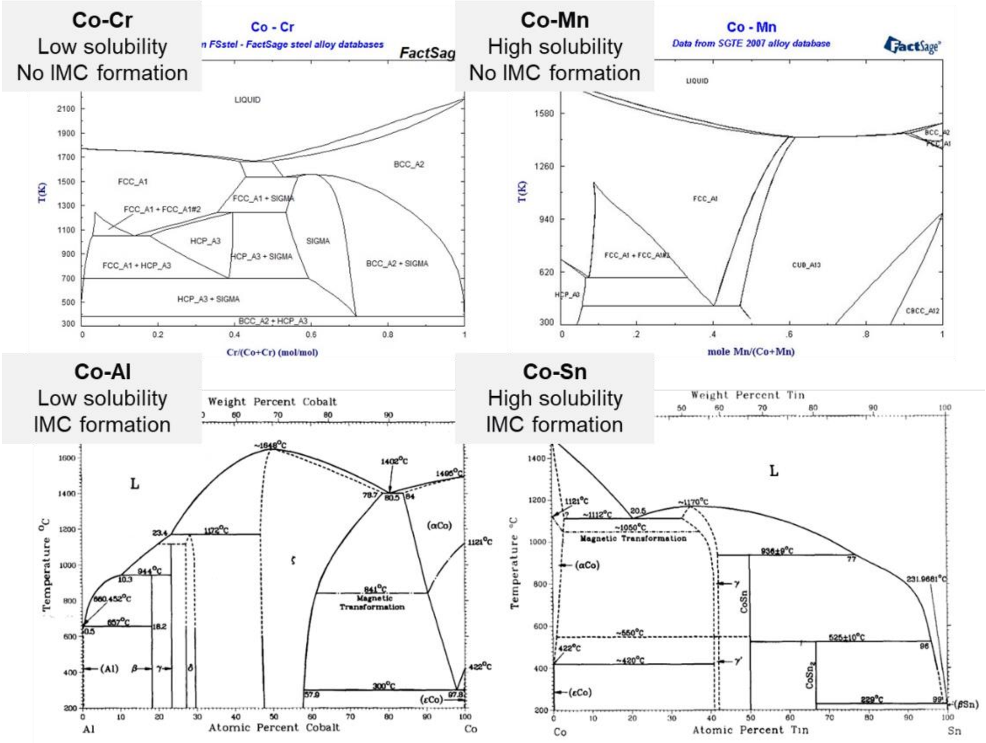


Figure 4.5 Confirmation of solubility of Co-X alloy dopant at 450 °C and intermetallic compound (IMC) formation: There are 4 cases regarding solubility and intermetallic compound. low solubility and Cr not forming IMC, Mn having high solubility but not forming IMC, low solubility and forming IMC Al, high solubility and Sn from which IMC is formed.

Table 4.2 Solubility and intermetallic compound (IMC) information for 39 elements. Values were calculated using Factsage^{TM} software.

Element	Solubility (at% @450°C)	Intermetallic compound formation (Y/N)	Element	Solubility (at% @450°C)	Intermetallic compound formation (Y/N)
Ag$^{1)}$	No	N	Mo$^{4)}$	0.04	Y
Al$^{1)}$	1.58	Y	Na$^{3)}$	4.96E-07	liquid
As$^{1)}$	3.11	N	Nb$^{1)}$	0.108	Y
Au$^{2)}$	0.14	N	Ni$^{1)}$	100	N
B$^{3)}$	No	Y	Pd$^{1)}$	4.02	N
Be$^{1)}$	0.19	N	Pt$^{1)}$	100	N
Bi$^{1)}$	No	liquid	Re$^{5)}$	0.417	N
Ca$^{1)}$	No	N	Rh$^{4)}$	3.427	N
Cd$^{1)}$	6.79E-04	liquid	Ru$^{6)}$	~0.3	N
Cr$^{1)}$	0.305	N	Sb$^{2)}$	No	Y
Cu$^{1)}$	0.07	N	Sc$^{5)}$	0.2	Y
Fe$^{1)}$	10.11	N	Sn$^{1)}$	2.12	Y
Ga$^{2)}$	10.834	Y	Ta$^{4)}$	1.24	Y
Ge$^{1)}$	1.17	N	Ti$^{1)}$	0.635	Y
Hf$^{3)}$	No	Y	V$^{2)}$	1.7	Y
In$^{1)}$	No	Y	W$^{1)}$	No	Y
K$^{4)}$	X	liquid	Y$^{2)}$	No	Y
Li$^{4)}$	No	liquid	Zn$^{1)}$	4.88	N
Mg$^{1)}$	No	Y	Zr$^{1)}$	No	Y
Mn$^{1)}$	8.11	N			

Material database: 1) FScopp, 2) SGTE, 3) FTlite, 4) FTstel, 5) spMCBN, 6) SGnobl

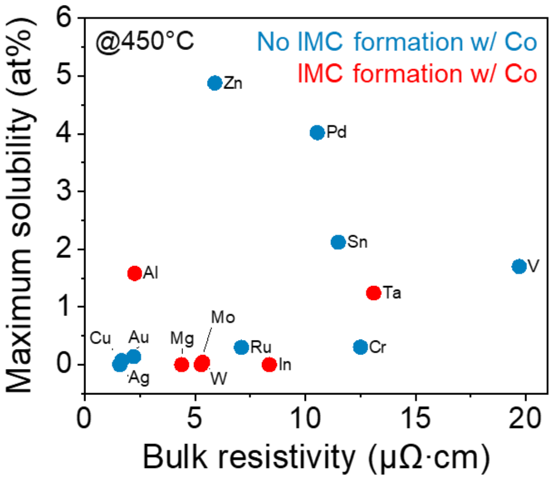


Figure 4.6 Solid solubility limit graph with bulk resistivity: when intermetallic compound (IMC) is formed, it is indicated in red, and when it is not formed, it is indicated in blue. The limit of solubility in Co at 450 °C is used.

Next, as shown in **Fig. 4.7**, solute diffusivity in Co was considered. In Phase II, out-diffusion stage, dopants dissolved in the Co matrix should diffuse to the surface during the annealing process. For this, the diffusivity of the solute is very important, and compared to the Co self-diffusivity, a material with higher diffusivity was considered as an effective self-forming barrier candidate. We compared values using literature values and compared solubility diffusivity and Co self-diffusivity values in FCC Co matrix at 1500 K rather than annealing temperature (723 K) in this study. The self-diffusivity of Co on the FCC Co matrix is 6.6×10^{-16} m^2/s. Therefore, rather than comparing absolute values, it was centered on whether it has a relatively high diffusivity. Among the materials with solubility below 5 at%, a total of 11 metals (Al, Au, Cr, Cu, Mo, Pd, Rh, Ru, Ta, V, Zn) were considered applicable.

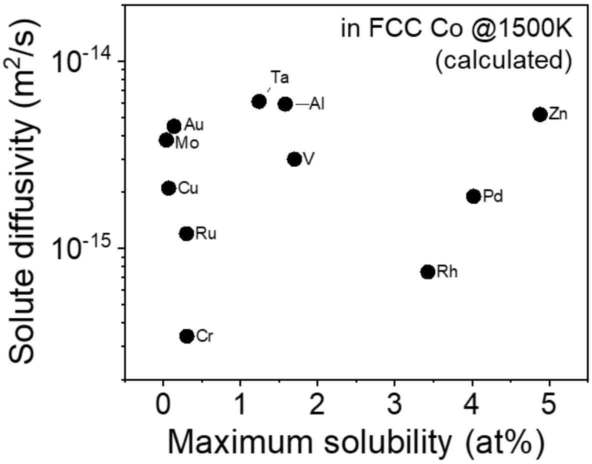


Figure 4.7 Solute diffusivity graph with Solid solubility limit: It shows diffusivity values of solute in FCC Co matrix at 1500K. Co self-diffusivity is 6.6×10^{-16} m^2/s.

The activity coefficient of dopant in Co alloy is an important indicator to confirm out-diffusion behavior. For the first time in Cu-Mn alloy, the activity coefficient criterion was applied to the self-forming barrier methodology. Co alloy was also used as an indicator of stability of alloying element in solid solution. When the activity coefficient is higher than 1, the dopant is less stable in the Co matrix and tends to out-diffusion. Conversely, when an activity coefficient lower than 1 is shown, diffusion to the surface is difficult because it is thermodynamically stable inside the Co matrix. **Table 4.3** shows the activity coefficient values of alloying elements that can be calculated in the Factsage^{TM} 7.3 library. Elements showing an activity coefficient greater than 1 are 11 metals (As, Be, Cd, Cr, Cu, Ge, Mo, Ni, Pt, Sn, Zn). And seven metals (Cr, Cu, Mo, Ni, Pt, Sn, Zn) satisfied at least one of the aforementioned criteria. These elements are marked with *.

Table 4.3 Activity coefficient of each dopant in the Co matrix at 450 °C: dopants in the Co matrix are less stable when the activity coefficient is greater than 1. Activity coefficients were calculated using Factsage™ software.

Element	Activity coefficient (γ)
Al$^{1)}$	3.330E-06
As$^{1)}$	3.023
Be$^{1)}$	3.217
Cd$^{1)}$	1.094E+05
Cr$^{*,1)}$	68.572
Cu$^{*,1)}$	1.428E+03
Fe$^{1)}$	0.263
Ga$^{2)}$	8.150E-04
Ge$^{1)}$	3.137
Mn$^{1)}$	0.463
Mo$^{*,3)}$	2.075
Ni$^{*,1)}$	0.999
Pd$^{1)}$	1.29E-08
Pt$^{*,1)}$	0.999
Sn$^{*,1)}$	2.653
Ta$^{3)}$	3.89E-07
Ti$^{1)}$	3.75E-06
V$^{2)}$	4.898E-03
Zn$^{*,1)}$	0.997

Material database: 1) FScopp, 2) SGTE, 3) FTlite, 4) FTstel, 5) spMCBN, 6) SGnobl

4.1.4. Reaction step with SiO_2 dielectric

Lastly, it is the Phase III stage considering the reaction between the SiO_2 dielectric and the surface-diffused dopant. As shown in the schematic diagram of out-diffusion and self-forming barrier in **Fig. 4.8**, the degree of oxygen reaction with the alloying element diffused to the surface was considered. It was considered good to have a moderate oxidation tendency between Co and Si. This is because, when it has a lower oxidation tendency than Co, Co oxide is expected to form because the driving force that Co reacts with oxygen is higher than that of the alloying element. And if it has a higher oxidation degree than Si, a diffusion barrier will be formed, but free Si may be formed by reaction with too much oxygen. Since free Si might serve as an electrical path within the SiO_2 dielectric, it is not expected to be good in terms of electrical reliability. As an example, the Cu-Mg alloy exhibited excellent self-forming barrier behavior but did not show high reliability due to the high oxidation tendency of Mg. Above all, it was considered that a material having an appropriate oxidation tendency could form an oxide film with a thin thickness because the resistance of the interconnect system increases as the thickness of the self-forming barrier increases. **Fig. 4.9** is an Ellingham diagram showing the standard free energy of oxidation formation of each element with the temperature. The details of the Ellingham diagram are described in section 2.2. Through the Ellingham diagram, a total of 6 metals (Cr, Fe, K, Mn, Sn, Zn) located between the oxidation degrees of Co and Si were identified. Among them, potassium (K) belongs to the alkali metal group and is known as a very reactive material. Since CMOS compatibility is a very important criterion, Cr, Fe, Mn, Sn, and Zn, except for potassium, were classified as metals with appropriate oxidation tendency.

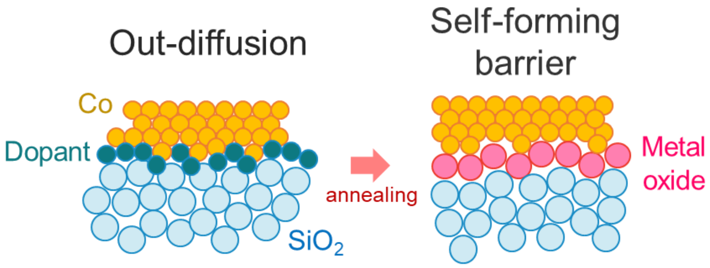

Out-diffusion
Self-forming barrier
Co
Dopant
SiO$_2$
annealing
Metal oxide

Figure 4.8 Stage of self-forming diffusion barrier: process of dopants reacting with SiO$_2$ dielectric after out-diffusion.

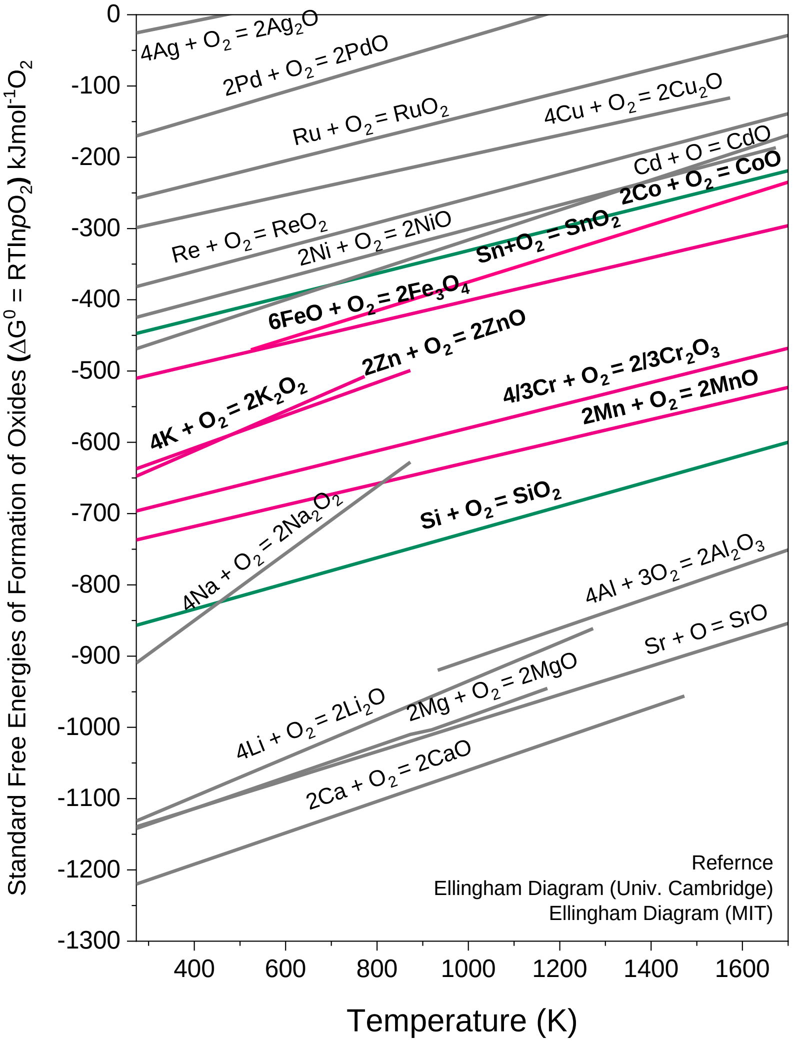


Figure 4.9 Ellingham diagram: Self-forming barrier materials should have descent oxidation tendency. Reaction with oxygen on SiO_2 should occur at an appropriate level.

Finally, the thermodynamic stability phase that may exist at the Co and SiO2 interface after annealing was calculated using Factsage^{TM} software. In the previous Ellingham diagram, the reaction with Si was not expected because only the standard free energy of oxide formation was considered. If the interconnect system (metal, diffusion barrier, dielectric) material design can be more accurate, the time required for trial and error is expected to be greatly reduced. In this study, the method of calculating the thermodynamic stability phase was applied for the first time, and it will be a very powerful material design tool because it can predict the thermodynamic stability phase in Co, diffusion barrier, and SiO_2 dielectric material systems. In the existing Cu-Mn alloy, it was experimentally proven that Mn silicate ($MnSi_xO_y$) is formed at the interface. Since there has been some controversy over which stable phase forms in Cu-Mn alloy, the thermodynamic stable phase calculation will serve as a more valid indicator.

Since the reaction phase with the dielectric is important, it was calculated considering the M-SiO_2 binary system and the Co-M-SiO_2 ternary system. For materials without a Factsage database, the calculation of thermodynamic stability was limited. **Table 4.4** shows the thermodynamic stability of each element. Metals that make compound phases in binary and ternary systems were identified as Cr, Fe, Mn, Ni, and Zn. Four elements except Cr were confirmed to form silicate in the binary system (M-SiO_2), and this was classified as a silicate former. Among the silicate formers, Fe and Mn cooperated with Co in the ternary system, and Fe-Co-Si and CoSiO3 other stable phases respectively appeared. In the case of Zn silicate former, since the same Zn_2SiO_4 phase was formed in binary and ternary systems, Zn seems to be suitable for use as a diffusion barrier layer for Co interconnects. On the other hand, in Cr, the same Cr_2O_3 phase in binary and ternary systems is calculated as a thermodynamically stable phase, so it is likely to be formed as a stable diffusion barrier in Co interconnects.

Table 4.4 Calculation of interfacial stable phase at annealing temperature (450 °C) using Factsage^{TM}: The thermodynamic stable phase of each element was calculated in binary system (M-SiO_2) and ternary system (M-SiO_2-Co).

Element	Activity coefficient (γ)	Binary system @450 °C (M-SiO_2)	Ternary system @450 °C (M-SiO_2-Co)
Ag	0	X	-
Au	0.140	X	-
Cr	68.570	Cr_2O_3	Cr_2O_3
Cu	1,428	X	-
Fe	0.263	Fe_2SiO_4	Fe-Co-Si compound
Ge	3.137	X	-
Mn	0.463	$MnSiO_3$	$CoSiO_3$ compound
Ni	100	Ni_2SiO_4	X
Pd	4.02	X	-
Pt	100	X	-
Ru	-	X	-
Zn	0.997	Zn_2SiO_4	Zn_2SiO_4

4.1.5. Comparison criteria

Table 4.5 is a table summarizing the results of 7 indicators for each material to select the most suitable self-forming barrier (SFB) material. A total of 9 materials (Al, Cr, Cu, Fe, Mg, Mn, Ni, Sn, Zn) were primarily selected as SFB materials. Let's look at the specific criteria for each indicator. First, in the case of resistivity, it was classified as “low” if it showed a resistivity lower than Co, “intermediate” if it was higher than Co but lower than 20 μm·Ω, and “high” if it was higher than 20 μm·Ω. Next, in the case of melting temperature, it was classified as “high” when it was higher than Co, “intermediate” when it showed the melting point between Cu and Co, and “low” when it was lower than Cu. Again, if the melting point is too high, the out-diffusion tendency may not be high. And the reason for using the melting point of Cu is because it is expected that the electromigration issue will be larger if it has a lower melting point than Cu. Solubility was divided into “low” when it was lower than 1 at%, “intermediate” when it was 1 at% to 5 at%, and “high” when it was higher than 5 at%. Intermetallic compound (IMC) formation was classified as “not formed” or “formed” depending on the presence or absence of IMC. Activity coefficient was divided into cases higher or lower than 1 and expressed. Oxidation tendency was divided into strong, moderate, and weak according to the degree of oxide formation. Finally, the thermodynamic stable phase after annealing was classified according to whether a stable phase was created in the binary system. Alloying elements that showed excellent properties for each index were classified as “highly applicable”, if they showed satisfactory properties, they were classified as “applicable”, and if they were not appropriate, they were classified as “inapplicable”.

As can be seen intuitively from Table 4.5, SFB material priorities can be determined in the order of Cr > Fe > Zn > Mn. Among them, Cr has relatively high bulk resistivity, but it can be said that it is the most promising SFB candidate material as it satisfies all other criteria. In section 4.2, we will experimentally confirm how effective the SFB criteria are and which indicators play a major role in the selection of SFB substances.

Table 4.5 Comparison of Co alloy self-forming barrier (SFB) criteria: Comparison of SFB suitability of 9 dopant with 7 criteria.

🟥 Highly applicable 🟦 Applicable ⬜ Inapplicable

Criteria		Cr	Fe	Zn	Mn	Ni	Sn	Al	Mg	Cu
Resistivity (μΩ·cm) 🟥 low (≤ 5.6), 🟦 intermediate (5.6 < X < 20), ⬜ high (≥ 20)	measured (reference)	🟦 14.40 (12.50)	🟦 8.48 (9.61)	🟦 10.6 (5.90)	⬜ 38.7 (144)	🟦 8.76 (6.93)	🟦 22.8 (11.50)	🟥 15.2 (2.26)	🟥 19.5 (4.39)	🟥 9.32 (1.68)
Melting temperature (℃) 🟥 high (≥ 1,495), 🟦 intermediate (1,495 < X < 1,083), ⬜ low (≤ 1,083)	reference	🟥 1,907	🟥 1,538	⬜ 420	🟦 1,246	🟦 1,455	⬜ 232	⬜ 660	⬜ 650	🟦 1,085
Solubility (at% @450℃) 🟥 low (≤ 1), 🟦 intermediate (1 ≤ X ≤ 5), ⬜ low (≥ 5)	measured value	🟥 0.31	⬜ 10.11	🟦 4.88	⬜ 8.11	⬜ 100	🟦 2.12	🟥 1.58	🟥 0	🟥 0.07
IMC formation @450℃ 🟥 not formed, ⬜ formed	No / Yes	🟥 N	🟥 N	🟥 N	🟥 N	🟥 N	⬜ Y	⬜ Y	⬜ Y	🟥 N
Activity coefficient of dopant 🟥 less stable in Co (γ > 1), ⬜ more stable in Co (γ < 1)	calculated value	🟥 68.572	⬜ 0.263	⬜ 0.997	⬜ 0.463	⬜ 0.999	🟥 2.653	⬜ 3.33E-6	⬜ -	🟥 1427.771
Oxidation tendency 🟥 moderate(SiO_2 < T < Co), 🟦 strong (≤ SiO_2), ⬜ weak (≥ Co)	M/ S/ W	🟥 M	🟥 M	🟥 M	🟥 M	⬜ W	🟥 M	🟦 S	🟦 S	⬜ W
Reaction in binary system @450℃ 🟥 formed(silicate/oxide), ⬜ not formed (or unknown)	stable phase	🟥 Cr_2O_3	🟥 Fe_2SiO_4	🟥 Zn_2SiO_4	🟥 $MnSiO_3$	🟥 Ni_2SiO_4	⬜ unknown	⬜ unknown	⬜ unknown	⬜ X

4.2. Comparison of Co alloy candidates

4.2.1. Thin film resistivity evaluation

Fig. 4.10 shows the change in resistivity of pure Co with annealing temperature (150 °C – 450 °C) and time (0.5 h – 10 hrs). For room temperature resistivity, the resistivity of the as-deposited sample was used. When annealing at 350 °C or higher, it was confirmed that the resistivity dropped to the level of bulk resistivity. The change in resistivity with the annealing time did not have a significant effect at 350 °C.

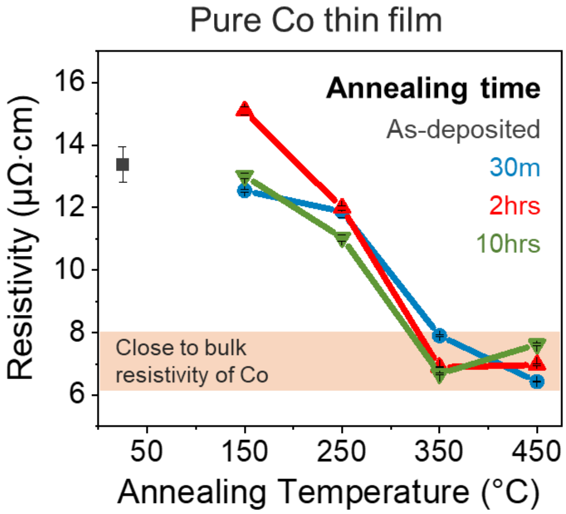


Figure 4.10 Changes in resistivity of pure Co with annealing temperature (150 °C – 450 °C) and time (30 minutes – 10 hours): data before annealing were used as room temperature data.

To compare the resistivity data, the annealing conditions should be the same, so an annealing condition experiment was conducted with 9 Co alloy thin films. **Fig. 4.11** –

4.13 shows the change in resistivity for each alloy according to the heat treatment conditions. As mentioned above, it was expected that the resistivity of the self-forming barrier and the Co film could be separated through resistivity analysis. In other words, when the resistivity was taken by inducing surface diffusion, it was expected that the resistivity of the diffused metal would appear close to that of the metal. As a result, accurate quantitative comparison itself was difficult because the change in resistivity was large depending on the dopant and doping concentration remaining in the Co matrix.

Co-Cr, Co-Fe, Co-Zn, Co-Mn, Co-Cu, and Co-Mn alloys showed the lowest resistivity when heat treated at 450 °C for more than 30 minutes. Co-Ni, Co-Sn, and Co-Al alloys showed a continuous decrease in resistivity when annealed at 450 °C for 2 hours or more. The experimental results to be used from now on are based on samples annealed at 450 °C for 2 hours to compare Co alloys, and if not, they will be marked separately.

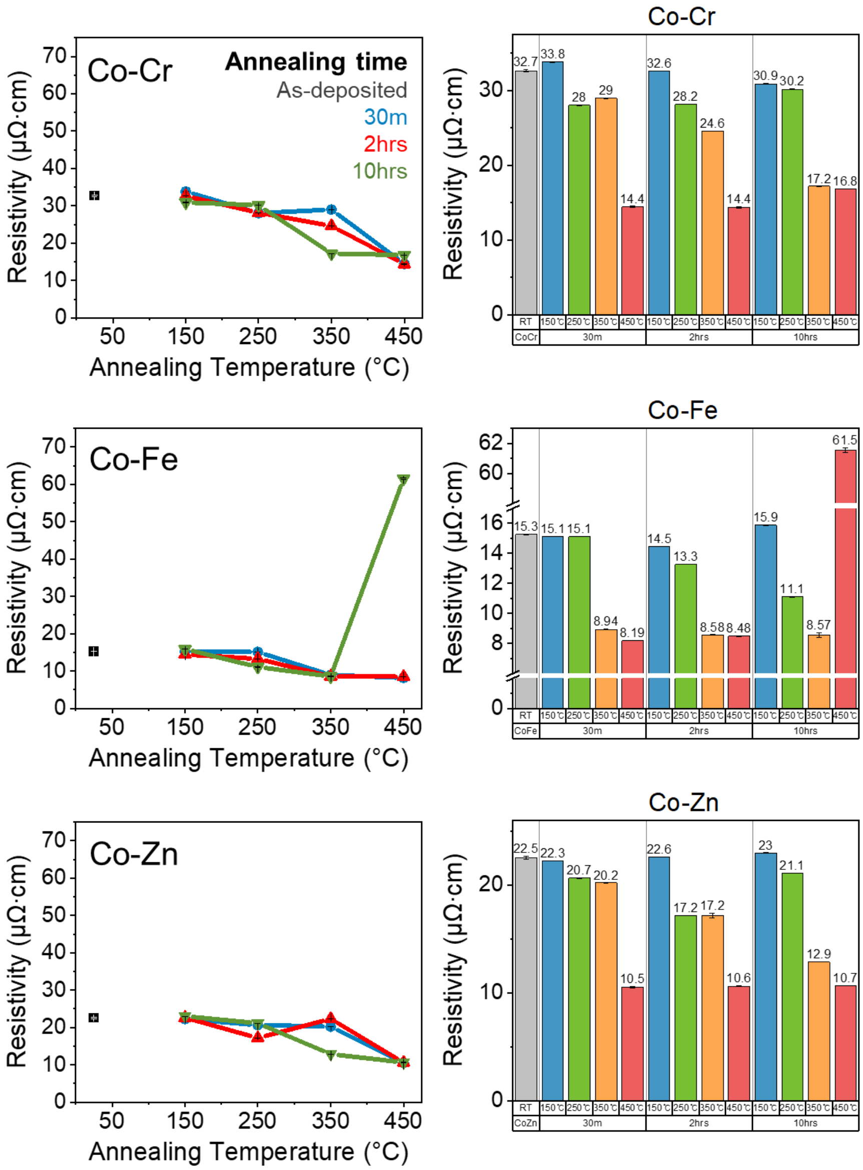


Figure 4.11 Resistivity change with annealing temperature (150 °C – 450 °C) and time (30 minutes – 10 hours): Based on the design rule, the three most suitable Co alloys (Co-Cr, Co-Fe, Co-Zn) were investigated.

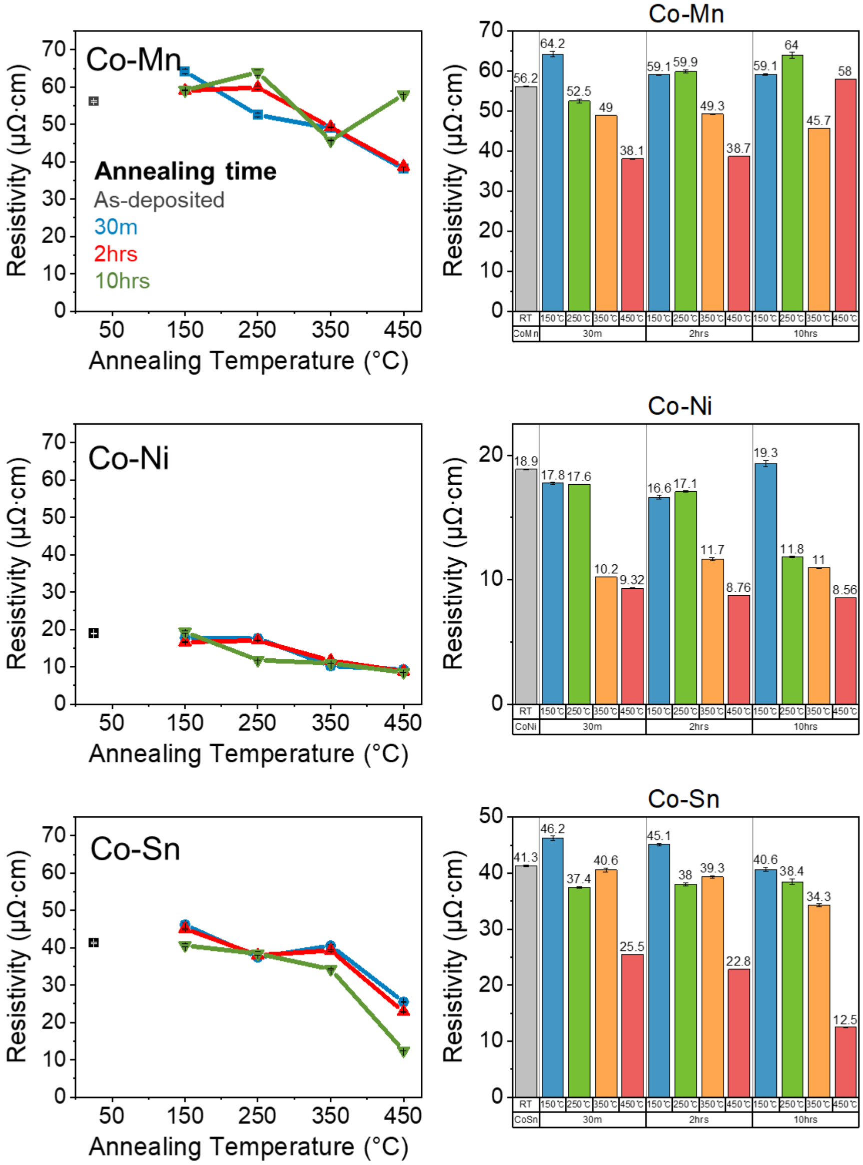


Figure 4.12 Resistivity change with annealing temperature (150 °C – 450 °C) and time (30 minutes – 10 hours): Co alloys (Co-Mn, Co-Ni, Co-Sn) were investigated.

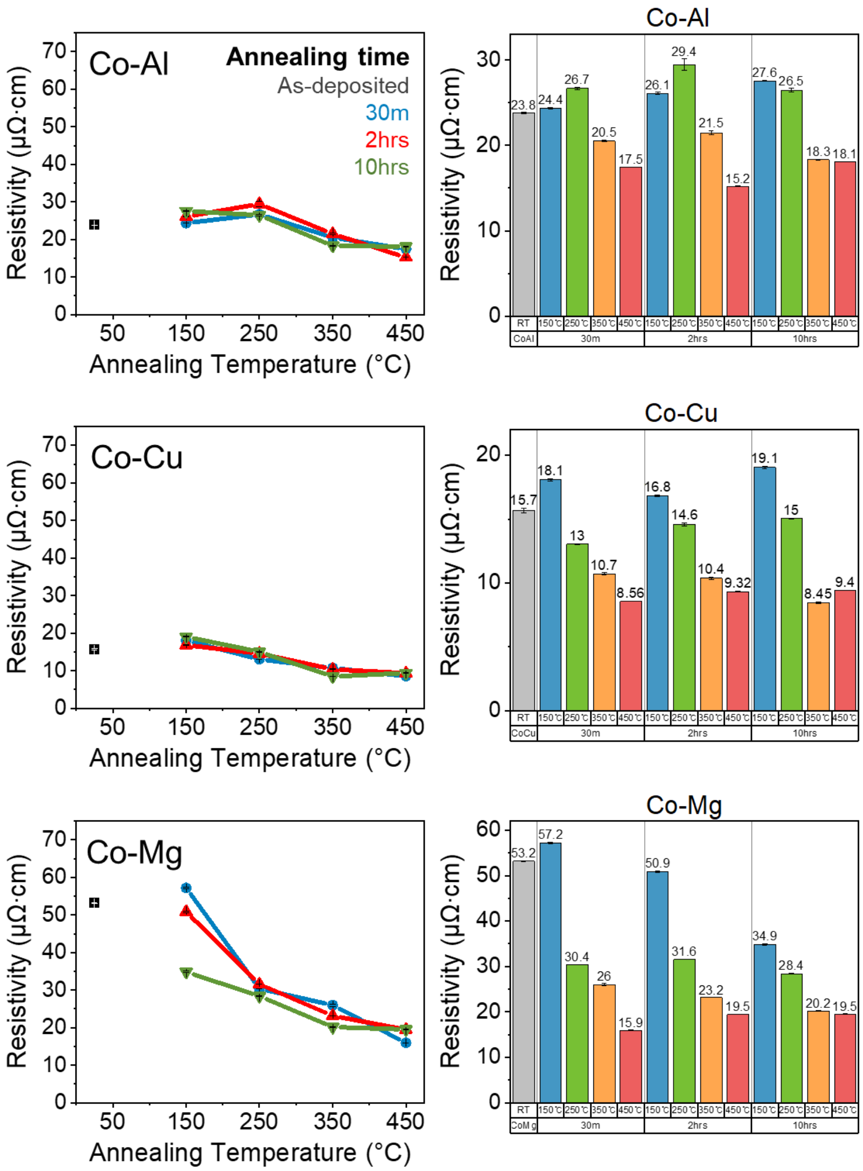


Figure 4.13 Resistivity change with annealing temperature (150°C – 450°C) and time (30 minutes – 10 hours): Co alloys (Co-Al, Co-Cu, Co-Mg) were investigated.

Fig. 4.14 shows the change in resistivity of pure Co and Co alloy before and after annealing (450 °C, 2 hours). Except for the Mn element, Fe, Ni, Zn, and Cr alloying elements showed low resistivity, which complies with the design rule criteria.

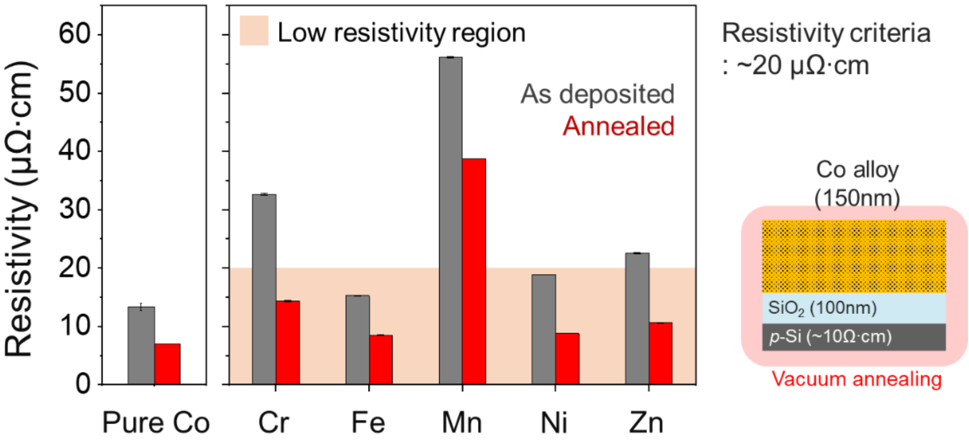


Figure 4.14 Observation of change in resistivity of Co alloy thin films before and after annealing: In the case of pure Co thin film, it drops to the level of bulk resistivity after heat treatment.

4.2.2. Self-forming behavior using XPS depth profile analysis

XPS depth profile analysis was performed on Co-Cr, Co-Fe, Co-Mn, Co-Ni, and Co-Zn alloys before and after annealing, and the results for Co-Cr, Co-Zn, and Co-Mn are shown in **Fig. 4.15**. The doping concentrations of Cr, Zn, and Mn were confirmed to be 1.6 at%, 5.5 at%, and 2.7 at% Mn through the results of the As-deposited sample, respectively. After annealing, it was confirmed that all three alloys moved to the top surface. In other words, the out-diffusion behavior of the alloying element from the Co matrix to the surface during the annealing process was observed. On the other hand, as shown in **Fig. 4.16**, the Co-Ni alloy did not diffuse to the surface even after heat treatment. In the case of the Co-Fe alloy, it was difficult to distinguish the two elements by XPS analysis because the binding energies of Co and Fe overlap. Therefore, energy dispersive X-ray spectroscopy (EDS) mapping analysis was additionally performed, and as a result of the analysis, it was still present on the Co matrix after annealing. The reason Co-Ni and Co-Fe alloys do not diffuse on the surface is because Co, Ni, and Fe are representative ferromagnetic materials and tend to mix well with each other. It is also the reason for using Co, Ni, and Fe in fields such as batteries. [135]

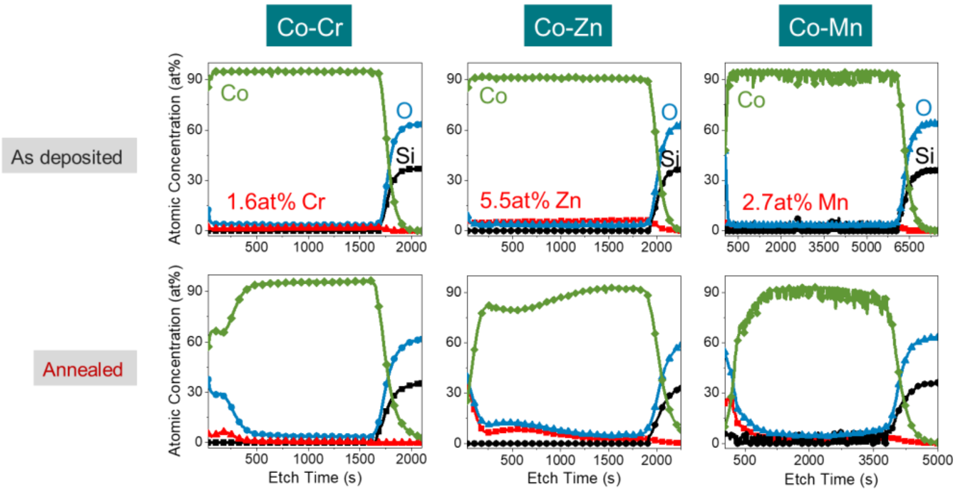


Figure 4.15 XPS depth profiles of the as-deposited and annealed Co alloy thin films: Co-Cr, Co-Zn, Co-Mn.

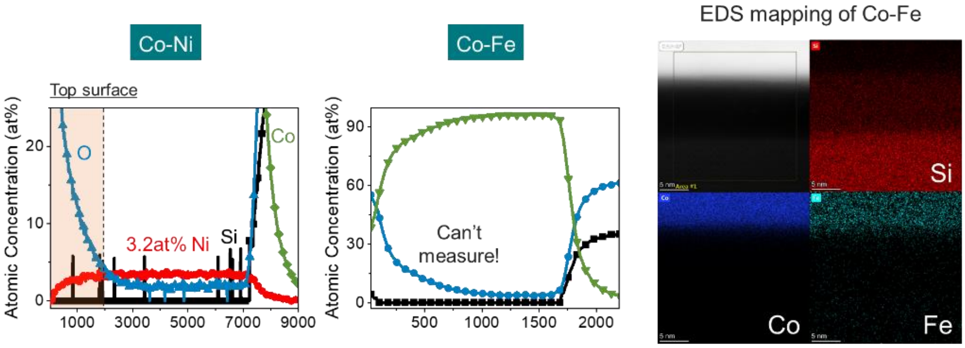


Figure 4.16 XPS depth profiles of Co-Ni, Co-Fe and energy dispersive X-ray spectroscopy (EDS) mapping of Co-Fe alloy.

Fig. 4.17 is the XPS result of expanding the area diffused to the top surface. If you look closely, Cr, Zn, and Mn all show surface diffusion behavior, but the type of diffusion is slightly different. Looking at **Table 4.3**, the activity coefficients of Zn and Mn are 0.997 and 0.463, respectively. On the other hand, Cr shows a very high activity coefficient value of 68.572. From this point of view, it seems that the out-diffusion behavior of Co-Cr alloy actively occurred during the annealing process. This needs to be elucidated through a more accurate analysis. Next, it is necessary to pay attention to the SiO$_2$ interface, which was enlarged as shown in **Fig. 4.18**. The profiles of alloying elements were different before and after annealing. In the case of Mn and Zn, they are still present in the SiO$_2$ region even after annealing. Since it is deposited in the PVD method, metal penetration may occur into the dielectric. On the other hand, Cr does not remain in SiO$_2$ after heat treatment and exists only at the interface. This behavior is also consistent with the previous thermodynamic calculations. In **Table 4.6**, when the interfacial stability phases of Cr, Mn, and Zn were calculated after annealing, Cr$_2$O$_3$, MnSiO$_3$, and Zn$_2$SiO$_4$ were thermodynamically stable phases, respectively. Comparing with the XPS results, Mn and Zn can exist in the SiO_2 region because they also react with Si as silicate formers. On the other hand, Cr, as an oxide former, appears to form a clean interface with SiO_2 because of its high reaction drive with oxygen rather than reaction with Si. Although additional interfacial analysis is required, it is expected that Cr migrated to the top surface, which is the free oxygen zone, except for reacting with defects (dangling bonds) existing at the SiO_2 interface.

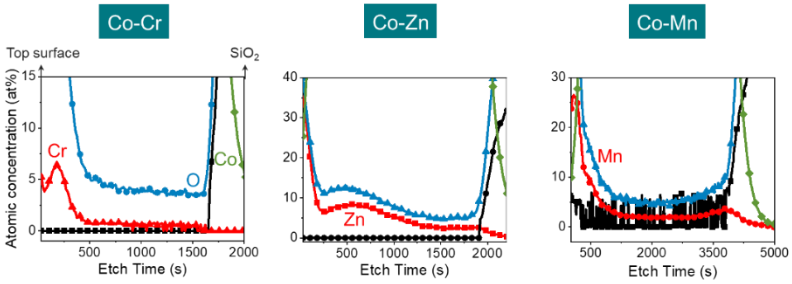


Figure 4.17 XPS depth profile of annealed Co alloy thin films: y-axis enlarged to confirm the top surface and SiO_2 interface composition.

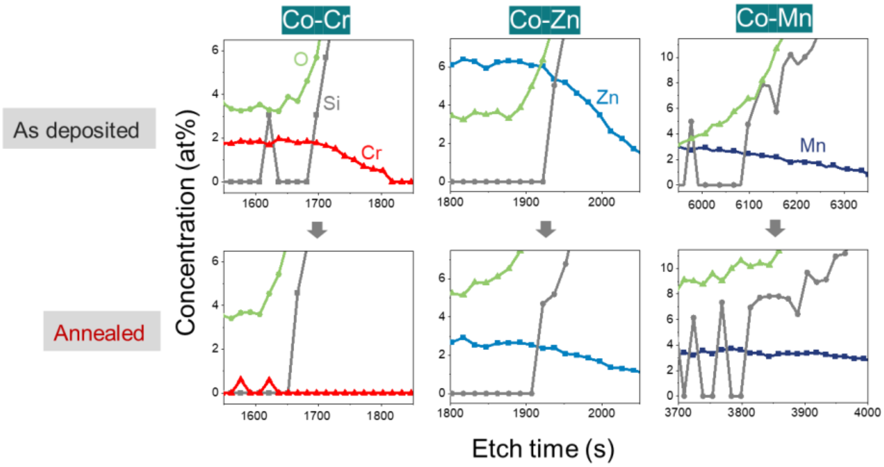


Figure 4.18 Behavior of Co alloying elements at SiO_2 interface after annealing: Zn and Mn exist inside SiO_2 after heat treatment, but Cr exists only at the interface, not inside SiO_2.

Table 4.6 Interfacial stability phase after annealing (450 °C) using thermodynamic calculations for each alloy: Co-Cr, Co-Mn, Co-Zn.

Interfacial stable phase (calculated) @450 °C	
Cr	Cr_2O_3
Mn	$MnSiO_3$
Zn	Zn_2SiO_4

Additionally, the self-forming barrier methodology, in which the driving force of barrier formation is diffusion, is expected to form a conformal and excellent diffusion barrier in low-k, ULK, and airgap dielectrics in the near future. **Fig. 4.19** is a schematic diagram of the expected barrier when a Co self-forming barrier is formed for each dielectric. As can be expected from the figure, when a porous low-k (ULK) dielectric is used, nm-scale pores exist. When processing these pores with the existing PVD barrier, it is very difficult to form a conformal barrier. On the other hand, since the Co-Cr alloy self-forming barrier forms a Cr_2O_3 barrier by reacting with oxygen through diffusion mechanism, it is expected to move to the nm-scale pore and react. The same result can be expected in the airgap structure. The current airgap structure makes an airgap by using the process conditions, in which case SiO_2 dielectric is present on the sidewall. The oxygen source needed for Cr_2O3 formation is on the sidewall! In the future, we expect that the Co-Cr self-forming barrier will still be effective even when the airgap structure is formed only with pure air. Because 21% of the air is made up of oxygen!

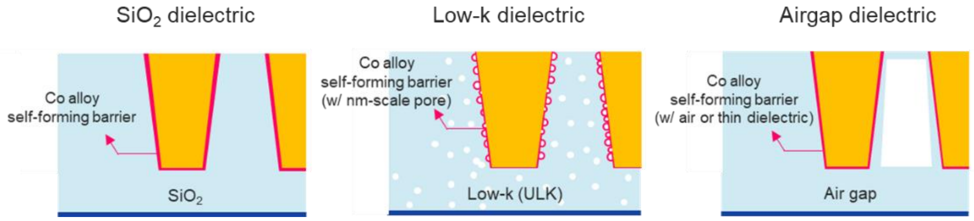
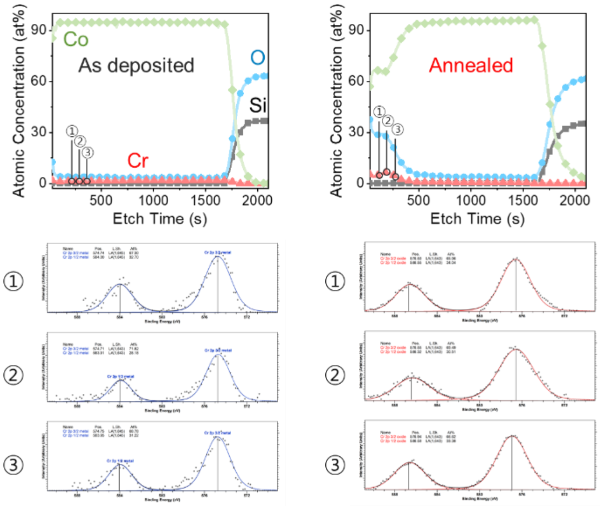

SiO$_2$ dielectric
Low-k dielectric
Airgap dielectric
Co alloy
self-forming barrier
Co alloy
self-forming barrier
(w/ nm-scale pore)
Co alloy
self-forming barrier
(w/ air or thin dielectric)
SiO$_2$
Low-k (ULK)
Air gap

Figure 4.19 Schematic diagram of barrier formation when self-forming barrier is applied to low dielectric material (SiCO:H, airgap, etc.): Since the driving force of the forming barrier is diffusion and oxide formation, conformal barrier formation will be possible than PVD barrier process.

Fig. 4.20 is the binding energy analysis result of Co-Cr alloy before and after annealing. Binding energy of metallic Cr and oxide Cr^{3+} was obtained using literature values. [136-140] In the case of the as-deposited sample, the binding energy of the top surface area (① ~ ③) and the annealing sample were compared with the binding energy of the diffused area (① ~ ③). In the case of Co-Cr alloy, it existed as a metallic Cr phase, and after annealing, it reacted with oxygen to generate a peak shift with Cr^{3+} binding energy, confirming that it was formed into a Cr_2O_3 phase. **Table 4.7** summarizes the Co alloy self-forming barrier design and experimental results. According to the design rule, it was expected to show the behavior of the self-forming barrier well in the order of Cr > Fe > Zn > Mn > Ni. As a result of the experiment, the self-forming barrier behavior of Cr, Zn, and Mn was confirmed, whereas Fe and Ni did not. Considering that Fe and Ni show unique magnetic properties along with Co, the design rule itself can be said to be a very valid model. In particular, it shows that the Co alloy self-forming barrier material design rule is very effective because the thermodynamic calculation results and the experimental results agree well.



As deposited	Metallic Cr 2*p*	Peak gap
Reference	574.1 – 574.4	9.3
Measured	574.71 – 574.75	9.2 – 0.26

Annealed	Oxide Cr(+3) 2*p*	Peak gap
Reference	576.5 – 576.9	9.7 – 9.9
Measured	576.55 – 576.94	9.65 – 9.96

Figure 4.20 Binding energy analysis of Co-Cr alloy before and after annealing: In the case of as-deposited samples, comparison of binding energy in the top surface region (① ~ ③), and comparison of binding energy in the surface diffused region (① ~ ③) for annealing samples.[136-140]

Table 4.7 Comparison of Co alloy test results and self-forming barrier design rule (rule of thumb of Co-X alloy).

🟥 Highly applicable 🟦 Applicable ⬜ Inapplicable

Criteria		Cr	Fe	Zn	Mn	Ni
Resistivity (μΩ·cm)	Measured (bulk value)	14.40 (12.50)	8.48 (9.61)	10.6 (5.90)	38.7 (144)	8.76 (6.93)
Solubility @450℃ (at%)	calculated value	0.31	10.11	4.88	8.11	100
IMC formation @450℃	No / Yes	N	N	N	N	N
Activity coefficient of dopant	Calculated value	68.572	0.263	0.997	0.463	0.999
Oxidation tendency	M/ S/ W	M	M	M	M	W
Reaction in binary system @450℃	stable phase	Cr_2O_3	Fe_2SiO_4	Zn_2SiO_4	$MnSiO_3$	Ni_2SiO_4
Self-forming barrier formation	O / X	O	X	O	O	X

4.2.3. MIS device reliability test

In order to confirm the barrier quality of the self-forming barrier, a sample of the MIS structure was prepared, and a voltage-ramp dielectric breakdown (VRDB) analysis was performed. The ramped voltage stress (RVS) test is an efficient and alternative method instead of constant voltage stress (CVS) test to characterize the dielectric breakdown and to confirm the quality of diffusion barrier. [141-142] In general, VRDB is a way to quickly confirm the reliability and quality of interconnects before TDDB lifetime evaluation. Please refer to section 2.3 for details. **Fig. 4.21** shows the measurement result of breakdown voltage of pure Co and Co/3 nm barrier. Breakdown voltage (V_{BD}) is defined when leakage current abruptly increases, and V_{BD} is defined as voltage when leakage current exceeds 10^{-8} A in this study. In the case of pure Co, dielectric breakdown occurred before 15 V, whereas in the case of Co/3 nm barrier, dielectric breakdown occurred around 23 V. In general, the higher the V_{BD}, the better the metal/barrier material. The problem of early extrinsic breakdown by Co ion has been reported since 2017, and the early breakdown of pure Co could be confirmed through this experiment. [34, 37] In general, in Cu/Ta/TaN systems, the current conduction mechanisms of Schottky emission, Poole-Frenkel emission, and F-N tunneling are mainly reported. In the case of Cr_2O_3, Poole-Frenkel emission and F-N tunneling appeared as current conduction mechanisms. Research for accurate conduction mechanism analysis is in progress. In summary, if Co alloy forms a barrier after surface diffusion and reaction with SiO_2 during annealing, leakage current change with the barrier effect can be confirmed as shown in **Fig. 4.21**.

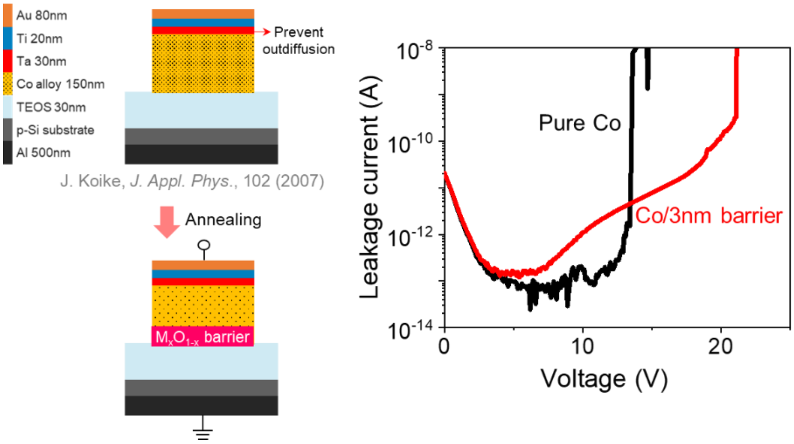


Figure 4.21 Diffusion barrier effect: The leakage current shape is different in pure Co and Co sample to which the barrier is applied, meaning that the dielectric current conduction is different, and the breakdown voltage is also greatly improved.

Fig. 4.22 schematically shows the VRDB analysis results for each pure Co and Co alloys. All samples were analyzed 12 times, and I-V results for 9 samples except for the maximum value, minimum value, and outliner were shown. Compared to the pure Co sample, the breakdown voltage of Co-Cr, Co-Fe, Co-Ni, and Co-Zn was improved. In the case of Co-Mn, it can be said that there is no self-forming barrier effect because the leakage current increases from the 6 V region. Co-Ni and Co-Fe showed higher V_{BD} characteristics than pure Co but did not confirm the leakage current shape change due to the barrier effect. Previously, Ni and Fe were well mixed with Co, so it can be understood as V_{BD} improvement by Co alloy phase. In the case of Co-Cr and Co-Zn, changes in current conduction due to the barrier effect were observed, and Co-Cr showed very good V_{BD} characteristics. In the case of Co-Zn, it is expected that a conformal barrier was not formed at the interface because there was a result that the barrier effect did not appear. In the case of Co-Cr, a breakdown voltage of up to 31.2 V was observed, and it seems that a Cr_2O_3 self-forming barrier with very good diffusion barrier properties was formed. **Fig. 4.23** is a schematic diagram of the median breakdown voltage of pure Co and Co alloy. Excellent breakdown voltage characteristics were shown in the order of Cr > Zn > Fe > Ni > Mn. And only Zn and Cr showed the barrier effect.

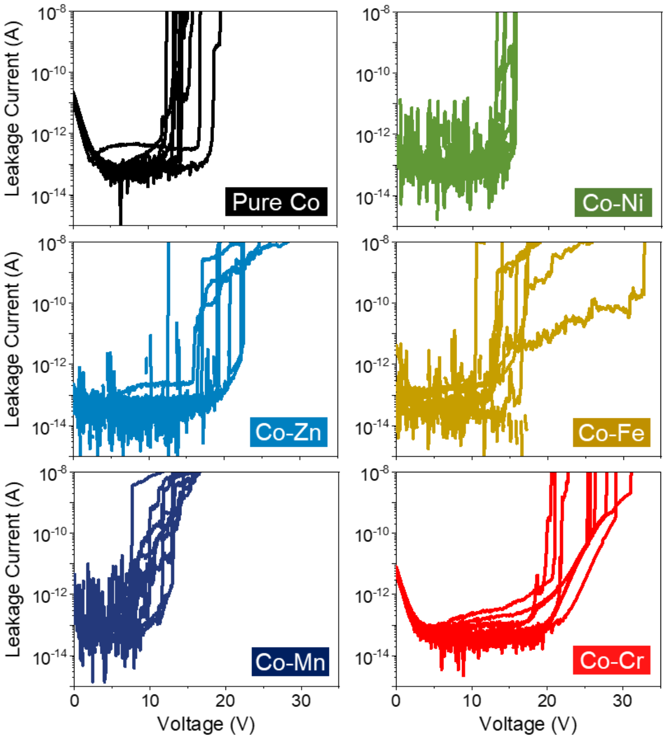


Figure 4.22 VRDB analysis by pure Co and Co alloy: Electrical failure (breakdown voltage) was defined when leakage current increased over 10^{-8} A, and I-V analysis was performed on a 125 °C stage chuck.

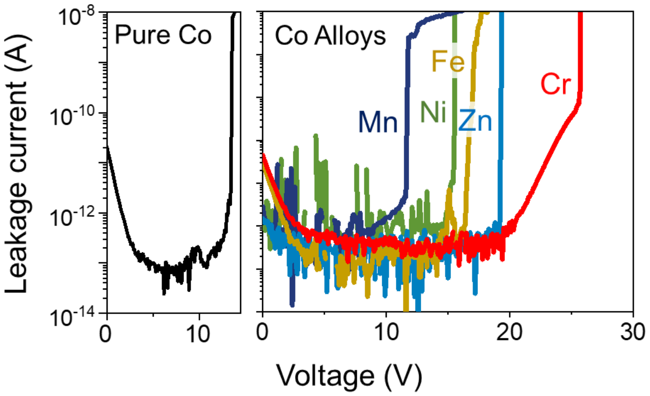


Figure 4.23 Comparison of breakdown voltage of pure Co and Co alloy: 12 times per sample were measured, and the median value was used among them.

Fig. 4.24 shows the breakdown voltage of pure Co and Co alloys as a cumulative distribution function (CDF) plot. The breakdown voltage of the Co-Cr alloy itself was also measured high, showing that the breakdown voltage variation is very small. Next, Zn, which showed excellent properties, has a large V_{BD} variation, so material improvement seems to be necessary to apply it to interconnects. Since VRDB analysis is a method to confirm the quality of materials, we will confirm the device reliability through lifetime analysis. We will refer to this in Chapter 5. **Fig. 4.25** is a TEM-EDS mapping image of the Co-Cr alloy and SiO_2 interface showing high V_{BD} characteristics. After annealing, it can be seen that Cr outdiffused from the Co matrix to the SiO_2 interface. Although it is not known whether Cr and oxygen react through EDS mapping analysis, it can be said that Cr is present at the SiO_2 interface as Cr_2O_3 phase if we look at the results of the previous thermodynamic calculations and electrical analysis. Based on the EDS results, the thickness of Cr_2O_3 was calculated to be 1.2 nm, indicating that an ultra-thin barrier was formed. As mentioned in the previous research goal, the Cr_2O_3

self-forming barrier meets the barrier criteria for high reliability of an ultra-thin film. The detailed interpretation of the interface through HR-TEM analysis will be explained in Chapter 5.

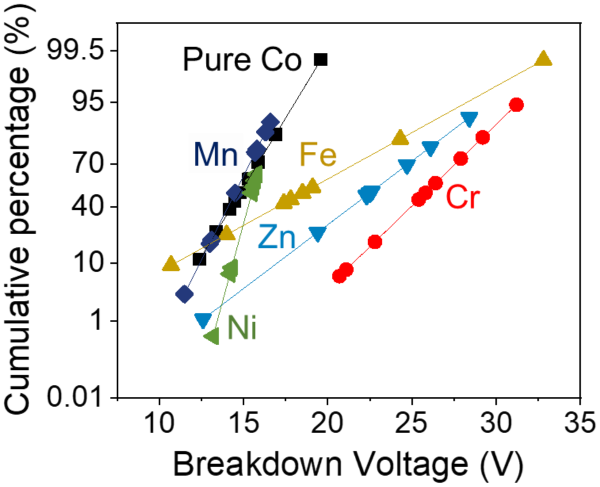


Figure 4.24 Cumulative distribution function (CDF) plot of breakdown voltage of pure Co and Co alloys.

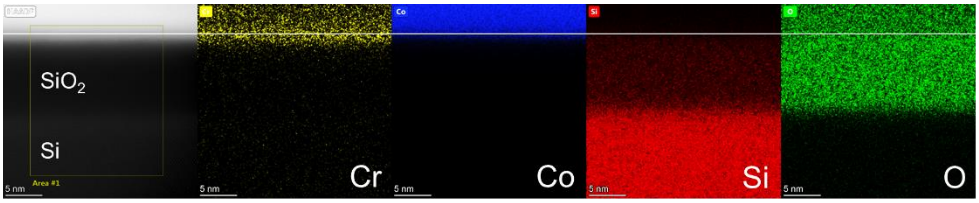


Figure 4.25 TEM-EDS mapping image of Co-1.6at% Cr alloy thin film: When comparing the electrical analysis result and EDS image, it was confirmed that Cr oxide barrier was formed after surface diffusion of Cr at the SiO_2 interface.

4.3. Summary

In Chapter 4, we designed a Co-ally self-forming barrier material to improve the reliability of the Co interconnects. As shown in **Fig. 4.26**, we prioritized Cr > Fe > Zn > Mn > Ni by considering thermodynamic parameters such as bulk resistivity, solubility limit, intermetallic compound formation, activity coefficient, oxidation formation energy, and interfacial stable phase. Through resistivity comparison, microstructural analysis, and electrical reliability evaluation, it was confirmed that Co-Cr alloy exhibited the best self-forming barrier behavior. The experimental results and the thermodynamic material design rule were in good agreement, indicating that the Co alloy self-forming barrier design is an effective methodology. It was verified through thermodynamic calculations and experiments that the Co-Cr alloy was formed into a very thin Cr_2O_3 self-forming barrier with a thickness of 1.2 nm during annealing. The Cr_2O_3 diffusion barrier formed at the SiO_2 interface has a very clean interface profile, and the breakdown voltage characteristics are improved by up to 203 % compared to pure Co. In this study, a novel interconnect material system composed of $Co/Cr_2O_3/SiO_2$ was proposed. This will solve the problem of extrinsic failure behavior in Co, which is referred to as a next-generation interconnects.

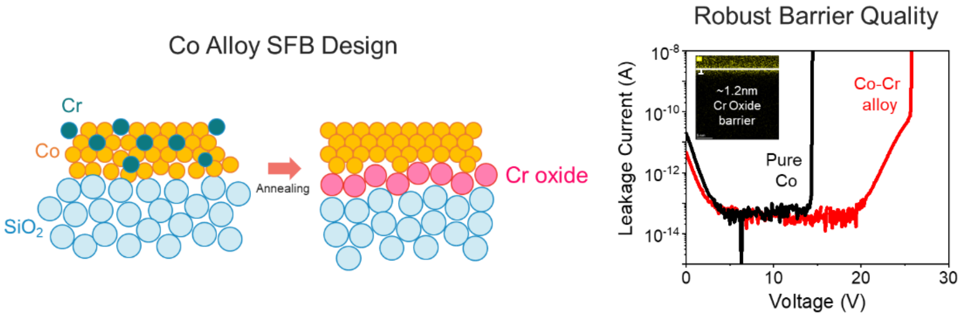


Figure 4.26 Material design of Co alloy self-forming barrier: Co-Cr alloy shows excellent barrier (Cr oxide) quality and superior reliability compared to pure Co.

CHAPTER 5

5.1. Compatibility of Co-Cr alloy SFB process

In Chapter 5, it was confirmed whether the Co-Cr alloy self-forming barrier methodology could be applied to the semiconductor interconnect process. There is various process variability in the BEOL (back-end-of-line) process. For example, line edge roughness (LER), via-to-line misalignment, chemical-mechanical polishing (CMP), interface leakage, interfacial adhesion energy, alloy doping concentration, and annealing issues exist. Since this study is limited in the use of patterned structures (dual damascene), process compatibility was confirmed by focusing on material effects.

5.1.1. Effect of Cr doping concentration

Fig. 5.1 shows the thermal budget for each stage of FEOL (front-end-of-line), BEOL (back-end-of-line), MEOL (middle-end-of-line), and assembly to make a semiconductor chip. Using the Czochralski method, a Si wafer is made around 1400 °C, and NMOS and PMOS are formed at 1100 °C using implantation. After that, interconnects are formed to connect the transistors, and from this point on, the thermal budget is very limited. Because the device was made using expensive processes before, it is important to ensure device reliability above all else. Therefore, the process temperature of interconnects has been limited to 450 ºC and has recently been lowered to 400 ºC and is expected to continue to decrease in the future. [143] Furthermore, with the use of low-k dielectrics, the thermal budget becomes very important. In addition, the annealing time is performed for 1 hour. In order for Co-Cr alloy to be applied to interconnect system, the temperature at which the Cr_2O_3 self-forming barrier is formed must be below 450 °C, and if the process is lowered, there is a great advantage in the process.

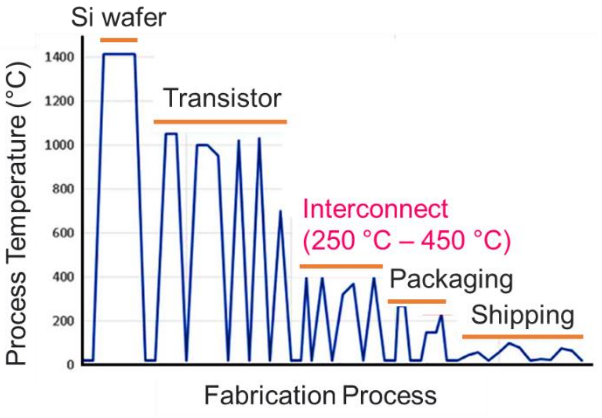


Figure 5.1 Process temperature for integrated chips (IC) manufacturing processes: lowering the thermal budget of interconnects from 450 °C to under 400 °C.[143]

Fig. 5.2 shows the change in resistivity before and after annealing (450 °C, 30 minutes) with the Cr doping concentration. As defined as a low resistivity area when it is less than 20 μΩ·cm in the previous study, the area where the low resistivity area appears was around 2 at%. Although the behavior of the self-forming barrier was confirmed even when the Cr doping concentration was high, doping below 2 at% seems to be the best because the *RC* delay can be greatly increased.

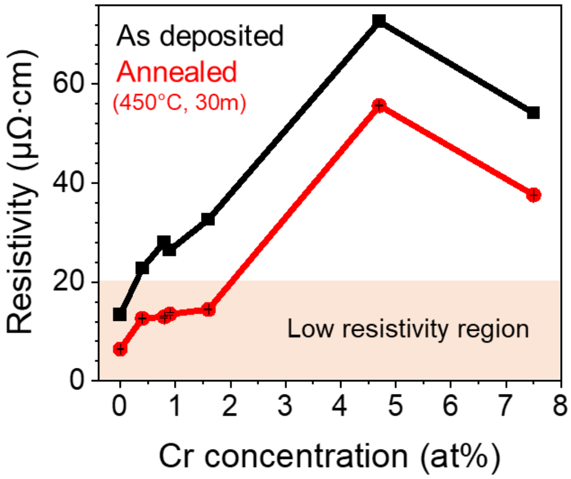


Figure 5.2 Resistivity evaluation of Co-Cr thin films: Doping concentrations up to 2 at% Cr are appropriate because low resistivity can be obtained.

5.1.2. Annealing process condition optimization

Fig. 5.3 and **Fig. 5.4** show the change in resistivity of Co-Cr alloy thin film with annealing conditions (temperature and time) and Cr doping concentration. It was confirmed that the resistivity decreased as the annealing temperature and time increased. In the case of doping concentration, the resistivity increased up to 4.7 at%, but decreased at 7.5 at%. **Fig. 5.5** shows the decrease in resistivity at low doping concentrations. The lowest resistivity (11 μΩ·cm) was shown in the 0.4 at% Cr sample that was heat treated at 350 °C for 2 hours.

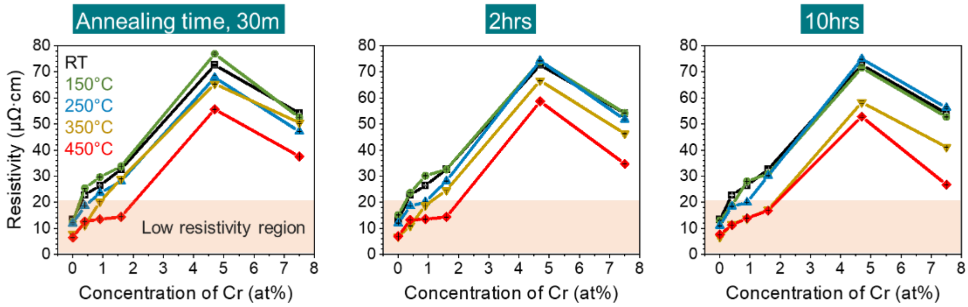
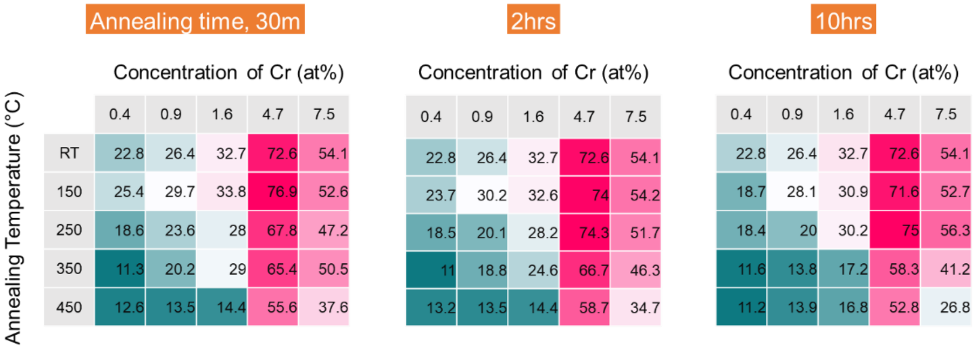


Figure 5.3 Change in resistivity of Co-Cr alloy thin film according to annealing conditions (temperature and time) and Cr doping concentration: temperature range (150 °C – 450 °C, 100 °C/step), annealing time range (0.5 hours, 2 hours, 10 hours), Cr doping concentration range (~ 7.5 at%).


Annealing Temperature (°C)
Concentration of Cr (at%)

Annealing time, 30m

	0.4	0.9	1.6	4.7	7.5
RT	22.8	26.4	32.7	72.6	54.1
150	25.4	29.7	33.8	76.9	52.6
250	18.6	23.6	28	67.8	47.2
350	11.3	20.2	29	65.4	50.5
450	12.6	13.5	14.4	55.6	37.6

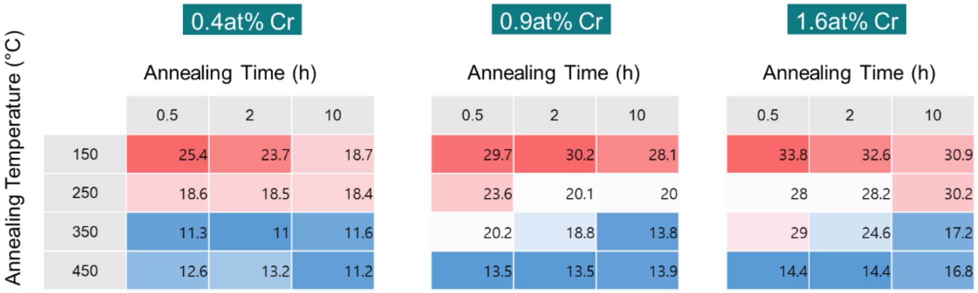
2hrs

	0.4	0.9	1.6	4.7	7.5
RT	22.8	26.4	32.7	72.6	54.1
150	23.7	30.2	32.6	74	54.2
250	18.5	20.1	28.2	74.3	51.7
350	11	18.8	24.6	66.7	46.3
450	13.2	13.5	14.4	58.7	34.7

10hrs

	0.4	0.9	1.6	4.7	7.5
RT	22.8	26.4	32.7	72.6	54.1
150	18.7	28.1	30.9	71.6	52.7
250	18.4	20	30.2	75	56.3
350	11.6	13.8	17.2	58.3	41.2
450	11.2	13.9	16.8	52.8	26.8

Figure 5.4 Annealing effect of Co-Cr alloy thin films: The effect of annealing temperature, time, and Cr doping concentration was confirmed.



Annealing Temperature (°C)	0.4at% Cr			0.9at% Cr			1.6at% Cr		
	Annealing Time (h)			Annealing Time (h)			Annealing Time (h)		
	0.5	2	10	0.5	2	10	0.5	2	10
150	25.4	23.7	18.7	29.7	30.2	28.1	33.8	32.6	30.9
250	18.6	18.5	18.4	23.6	20.1	20	28	28.2	30.2
350	11.3	11	11.6	20.2	18.8	13.8	29	24.6	17.2
450	12.6	13.2	11.2	13.5	13.5	13.9	14.4	14.4	16.8

Figure 5.5 Co-Cr alloy resistivity change in low doping concentration region: 0.4 at% Cr, 0.9 at% Cr, 1.6 at% Cr.

In order to obtain a low resistivity, Cr doping below 1.6 at% doping concentration seems to be the appropriate direction. It also showed a low resistivity at 250 °C annealing temperature, which is expected to exhibit sufficient self-forming barrier behavior at 250 °C. Therefore, the process temperature of the Co-Cr alloy self-forming barrier can be performed at a minimum of 250 °C, and the low resistivity can be obtained even with an annealing time of 30 minutes. In summary, Co-Cr alloy is a process that has high applicability to semiconductor interconnect process and can sufficiently respond to the continuously decreasing annealing temperature.

5.2. Reliability of Co-Cr interconnects

In section 5.2, electrical reliability was evaluated with three variables using voltage ramped dielectric breakdown (VRDB) analysis; Cr doping concentration, annealing temperature, Co-Cr alloy thickness. Structural analysis was additionally performed according to each variable to understand the electrical reliability characteristics.

5.2.1. VRDB quality test with Co-Cr alloys

Fig. 5.6 is a plot measuring breakdown voltage before annealing pure Co and Co alloy MIS devices. Electrical failure (breakdown voltage) was defined when leakage current increased over 10^{-8} A, and I-V analysis was performed on a 125 °C stage chuck. The breakdown voltage is concentrated in the 20 V – 25 V region. No improvement in V_{BD} was observed due to the barrier effect discussed above, and there was no change in V_{BD} with the Cr doping concentration. Since Co-Cr alloy exists in a solid solution phase, it can be understood that it cannot prevent Co ion depending on the applied voltage. For the I-V characteristics of each sample, you can see the diagram in **Fig. 5.7**. **Fig. 5.8** shows the I-V characteristics of the samples annealed at 450 °C for 2 hours. A clear I-V change can be seen not only in pure Co but also in Co-Cr alloy.

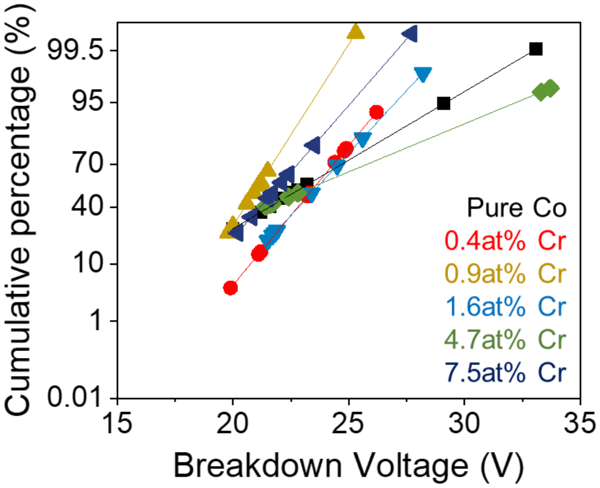


Figure 5.6 Change in breakdown voltage of as-deposited pure Co and Co-Cr alloy MIS structures using cumulative distribution function.

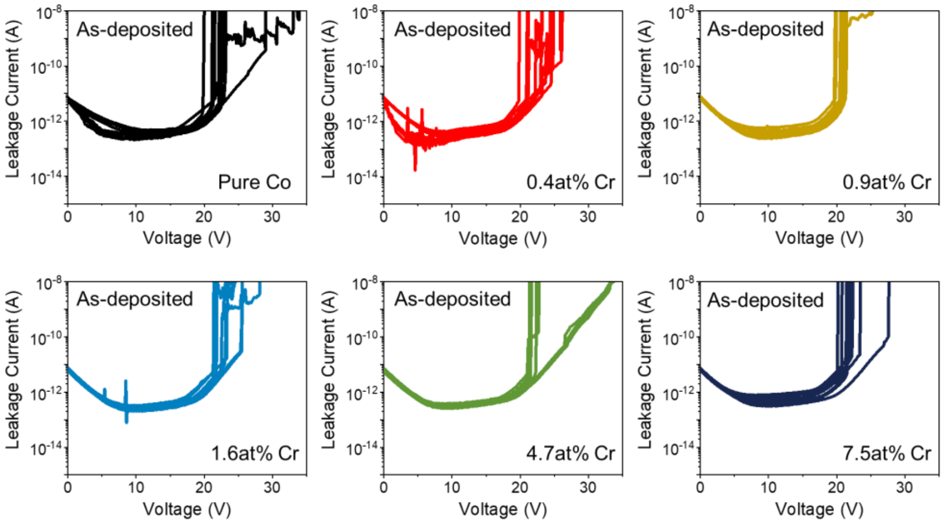


Figure 5.7 I-V characteristics of as deposited samples: pure Co and Co-Cr alloy (0.4 at% - 7.5 at%).

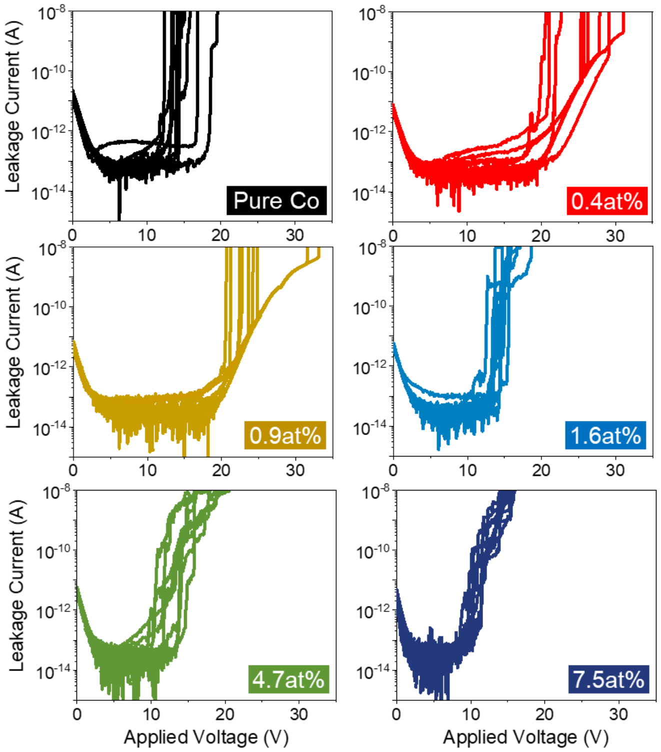


Figure 5.8 I-V characteristics of pure Co and Co alloys after annealing (450 °C): Electrical failure (breakdown voltage) was defined when leakage current increased over 10^{-8} A, and I-V analysis was performed on a 125 °C stage chuck.

In **Fig. 5.9**, the V_{BD} change according to the Cr doping concentration compared to pure Co can be confirmed by using the median value for each sample. Pure Co showed 14.8 V V_{BD}, whereas 0.4 at% Cr and 0.9 at% Cr samples showed high barrier quality of 25.8 V V_{BD} and 24.4 V V_{BD}, respectively. On the other hand, when the Cr doping concentration was 1.6 at% or more, the results were similar to or inferior to those of pure Co. **Fig. 5.10** is a chart showing the average V_{BD} value and standard deviation for each sample. At a Cr doping concentration below 1 at%, V_{BD} of 25 V or higher was measured, while the remaining Co-Cr alloy samples did not show a significant difference from pure Co. **Fig. 5.11** shows the breakdown voltage in the form of a cumulative distribution function. In the CDF plot, the 0.9 at% Cr sample shows the highest V_{BD}, but in terms of V_{BD} distribution, the 0.4 at% Cr sample has a narrower good distribution.

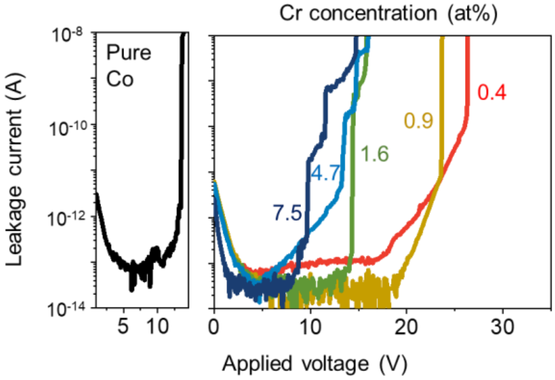


Figure 5.9 Comparison of breakdown voltage between pure Co and Co-Cr alloys using the median value for each MIS sample.

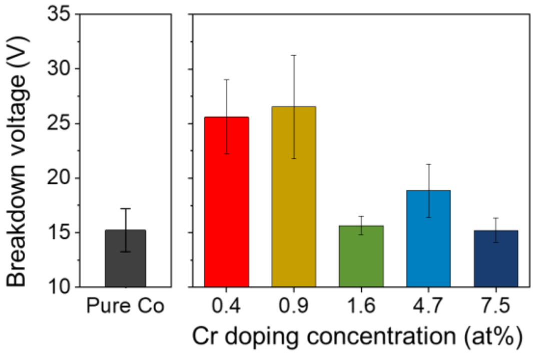


Figure 5.10 Comparison of the average breakdown voltage of pure Co and Co-Cr alloys: The average value and standard deviation are calculated using the values measured 9 times for each sample.

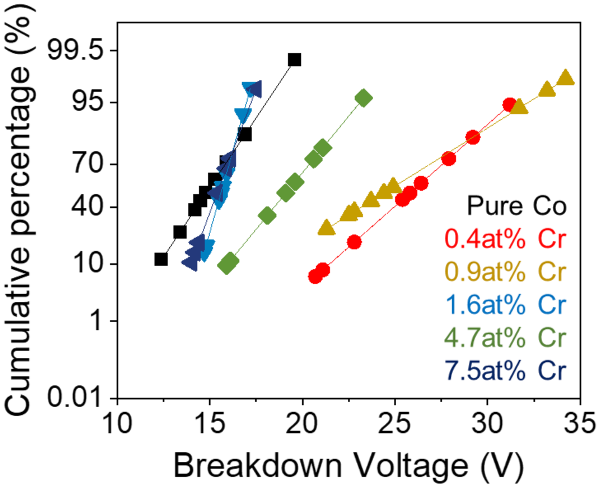


Figure 5.11 Cumulative distribution function (CDF) plot of breakdown voltage of pure Co and Co alloys after annealing.

The high doped Co-Cr alloy can be expected to affect the Cr_2O_3 diffusion barrier properties because the resistivity of Co-Cr is also increased when Cr doping at 2 at% or more is increased. Through VRDB analysis, we predicted that the Cr_2O_3 barrier quality would not be good because the amount of Cr diffused to the surface was too large when Cr doping more than 1 at% was performed, and eventually the I-V characteristics deteriorated rapidly. **Fig. 5.12** shows the effect of Cr doping concentration in voltage sweep up to 80 V. Interestingly, the 2nd or 3rd breakdown behavior was observed when doping more than 1.6 at%. All samples showing the 2nd breakdown behavior showed 1st breakdown around 15 V, which is close to the Pure Co VBD average value. In other words, it can be understood that breakdown due to pure co ion drift has occurred. After that, unlike pure Co, the current gradually increases, and a plateau region (19.1 V – 42.2 V) in which the current does not increase appears in the 7.5 at% Cr sample. Additional analysis is required, but when the Cr doping concentration is high, a lot of metallic Cr reacts with oxygen, and it is expected that it is an early breakdown due to free Si or metallic Cr residues.

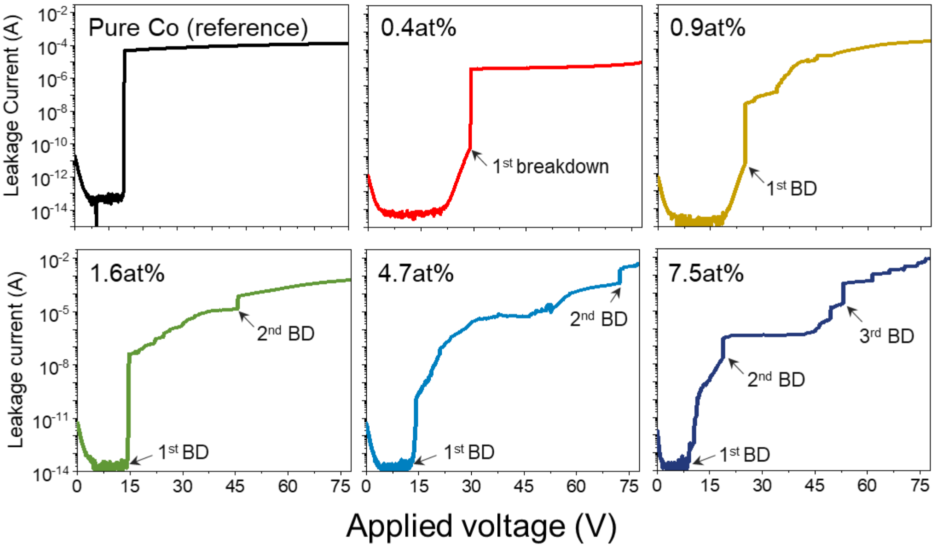


Figure 5.12 I-V characteristic change with Cr doping concentration (0.4 at% - 7.5 at%): observed from 1st breakdown to 3_{rd} breakdown.

Fig. 5.13 and **Fig. 5.14** are the results of analyzing the SiO_2 interfacial EDS line profile of 0.4 at% Cr and 7.5 at% Cr samples, respectively. First, looking at **Fig. 5.13**, the intensity of Cr Kα1 peak clearly increases at the SiO_2 interface. On the other hand, in **Fig. 5.14**, although the Cr Kα1 peak exists at the SiO_2 interface, Si Kα1 appears conspicuously. These results show that the interface state changes according to the Cr doping concentration, and thus the barrier quality can be greatly affected. In the case of a high doping concentration, it is expected that a large amount of metallic Cr exists at the interface, reacts with oxygen of SiO_2, and as a result free Si is generated, resulting in deterioration of the interface properties.

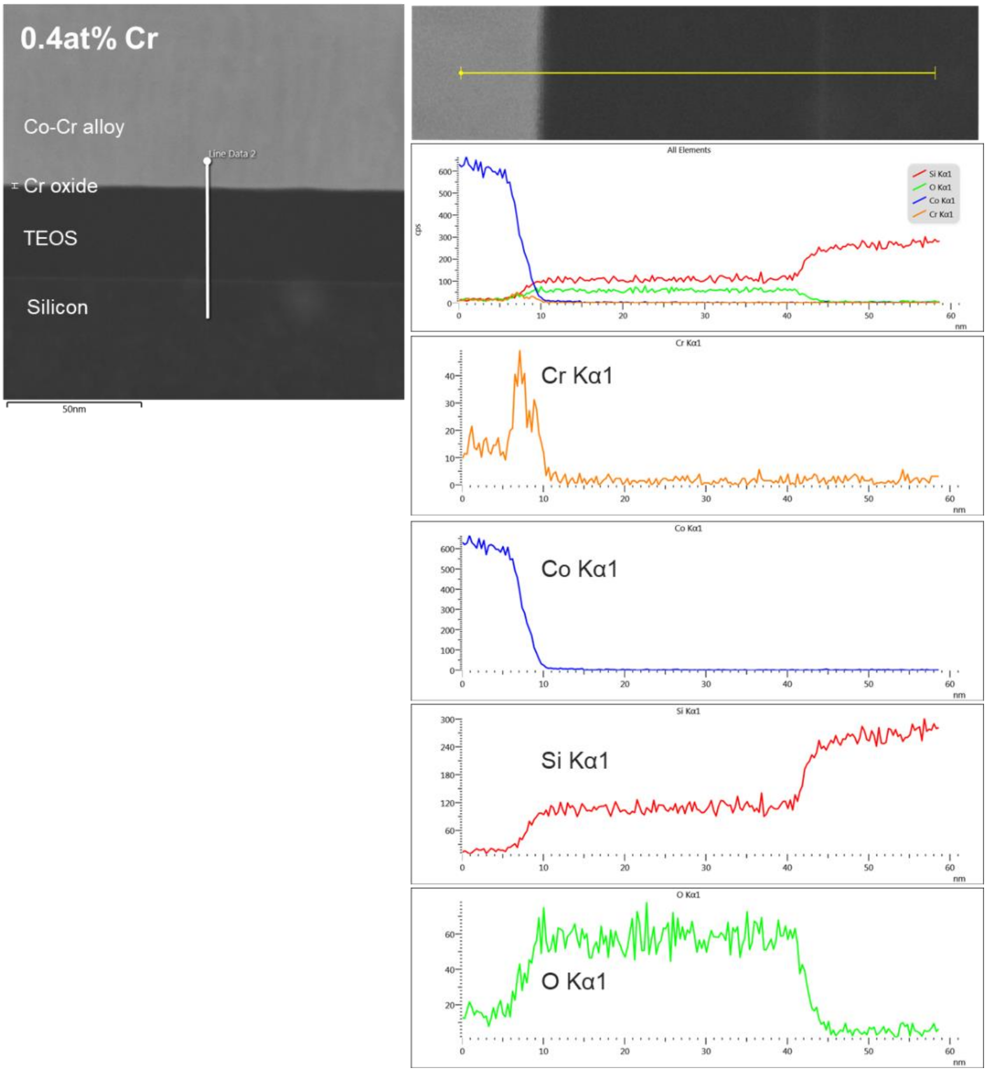


Figure 5.13 EDS line scan profile across the 0.4 at% Cr sample interface.

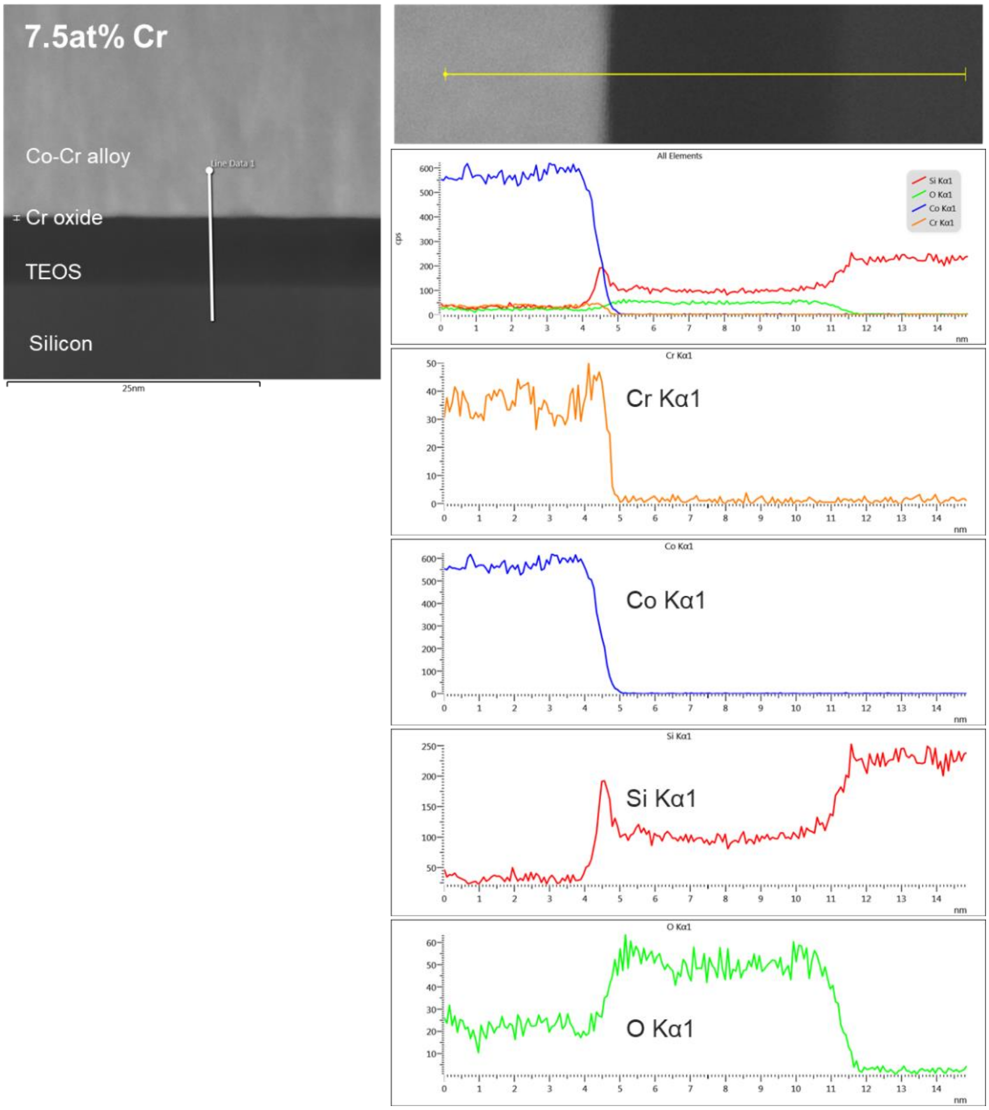


Figure 5.14 EDS line scan profile across the 7.5 at% Cr sample interface.

Fig. 5.15 (a) and **(b)** are interfacial HR-TEM images of each sample. In **Fig. 5.15** (a), a Cr_2O_3 layer with a thickness of ~1.2 nm was seen, whereas in **Fig. 5.15 (b)**, the interface was not clearly distinguished. Due to the very thin thickness, it was difficult to confirm the exact phase by selected area electron diffraction (SAED) analysis and diffraction peak analysis, but it can be said that the interface quality changed according to the Cr doping concentration. **Fig. 5.16** is an interfacial EDS mapping image according to doping concentration (0.4 at% and 7.5 at%). It was confirmed that Cr was present in both samples at the SiO_2 interface. However, information on Si Kα1 that could be confirmed in the EDS line profile could not be obtained. EDS mapping is difficult to confirm the change in the amount of Si at the interface because the analysis area is taken up to the Si substrate. In the 20 nm Co-Cr analysis, which will be discussed later, the change in Si Kα1 could be confirmed through the high-resolution super-X EDS instrument.

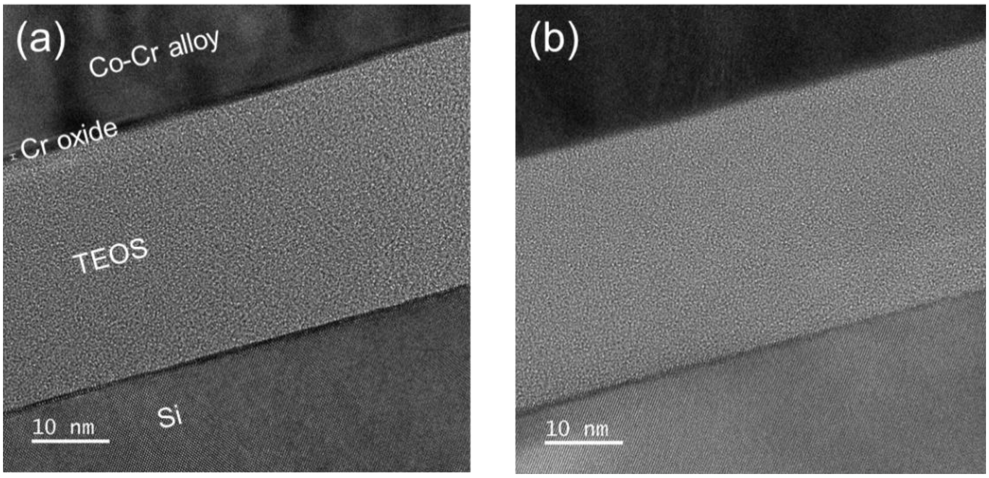


Figure 5.15 High-resolution transmission electron microscopy (HR-TEM) images: (a) 0.4 at% Cr and (b) 7.5 at% Cr samples.

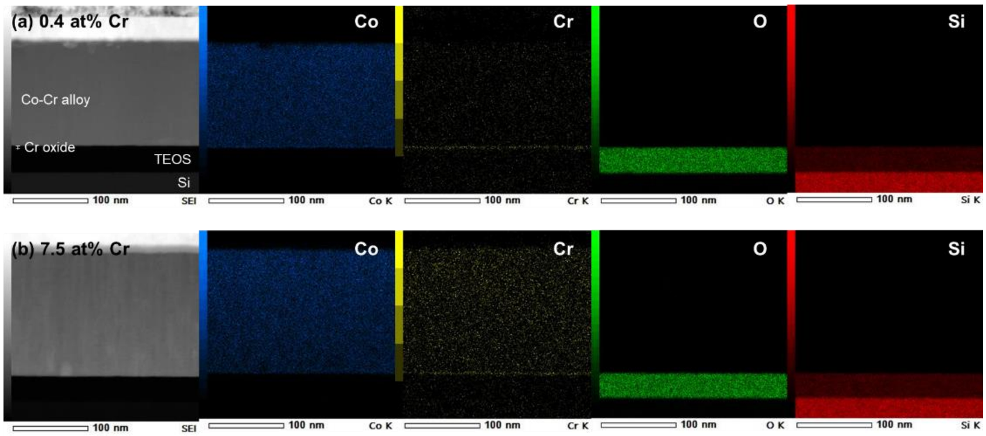


Figure 5.16 EDS mapping images with FE-TEM: Co, Cr, O, and Si elements were analyzed at each interface: (a) 0.4 at% Cr and (b) 7.5 at% Cr samples.

Next, the I-V characteristics with the annealing temperatures can be confirmed in **Fig. 5.17**. The 350 °C and 250 °C annealed samples showed better barrier quality than the 450 °C annealed samples. Note that, in the previous analysis, if leakage current of 10^{-8} A was defined as the failure criterion, in the low-temperature process samples, a sudden increase in current was observed as the electrical failure criterion. This is because the area where the leakage current linearly increases due to excellent barrier properties is very wide. Even at a low process temperature of 250 °C – 350 °C, the process compatibility is very high because it shows the same high barrier properties as the result with low resistivity. **Fig. 5.18** shows the average value and standard deviation of breakdown voltage according to the annealing temperature. A much higher V_{BD} and narrow standard deviation were found for the low temperature process compared to 450 °C. As shown in **Fig. 5.19**, robust barrier properties were confirmed even at 1.6 at% Cr when the low-temperature process was performed. In the low-temperature process, it can be considered that metallic Cr exhibits good barrier properties even at high doping concentration because the driving force that makes the oxide at the interface is lower than 450 °C. It is expected that these results were obtained because the interconnect resistance does not significantly affect the VRDB reliability analysis. Ultimately, since Co-Cr alloy with low resistivity is applied, it is difficult to say that the lower the process temperature, the better only with the barrier quality results in the low-temperature process. After that, the optimal annealing process should be considered by considering the TDDB lifetime evaluation.

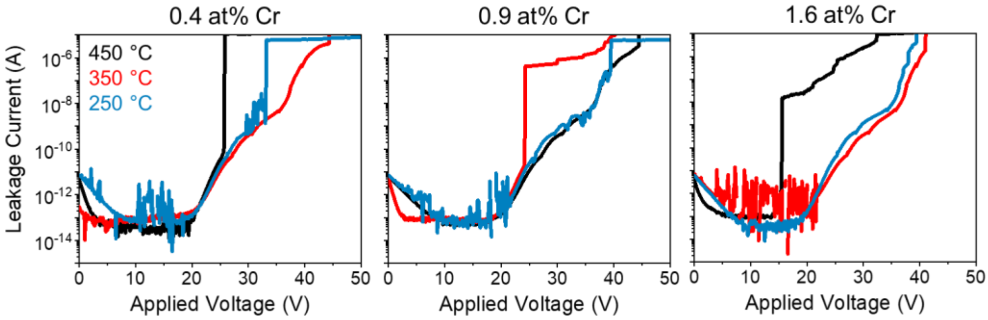


Figure 5.17 Changes in I-V characteristics in the low Cr doping region (0.4 at%, 0.9 at%, 1.6 at%) with annealing temperature (250 °C, 350 °C, 450 °C).

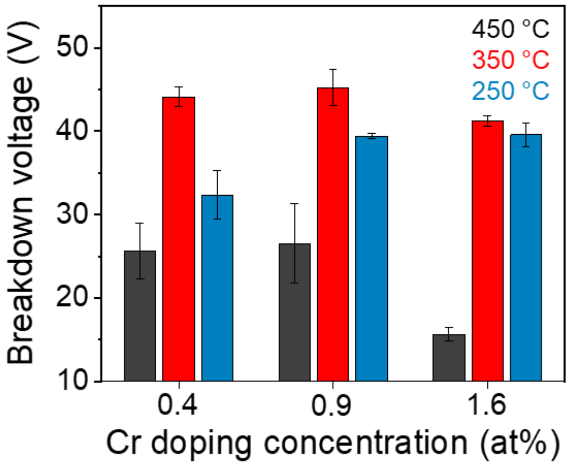


Figure 5.18 Breakdown voltage change with annealing temperatures (250 °C, 350 °C, 450 °C) and Cr doping concentration (0.4 at%, 0.9 at%, 1.6 at%).

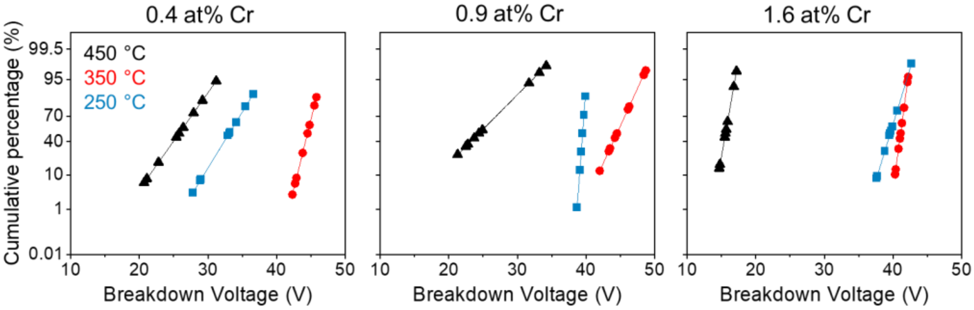


Figure 5.19 CDF plot of breakdown voltage change with annealing temperatures (250 °C, 350 °C, 450 °C) and Cr doping concentration (0.4 at%, 0.9 at%, 1.6 at%).

Next, the barrier properties of Co-Cr alloy according to the metal linewidth size effect were confirmed. **Fig. 5.20** shows the difference between the MIS structure and the interconnect structure used in this study. Reliability evaluation using the Damascene structure requires a patterning technique that can make the metal linewidth small. At the moment when the process below the 3 nm node is being developed, only IDM companies can realize very thin metal linewidth. Therefore, like MIS, we tried to reflect the structure of the metal linewidth of several tens of nanometers by controlling the thickness of the thin film. In this study, a 150 nm thick metal linewidth was considered, but the Cr_2O_3 self-forming barrier behavior was confirmed by reducing it to 20 nm in consideration of a 24 nm metal linewidth in the future.

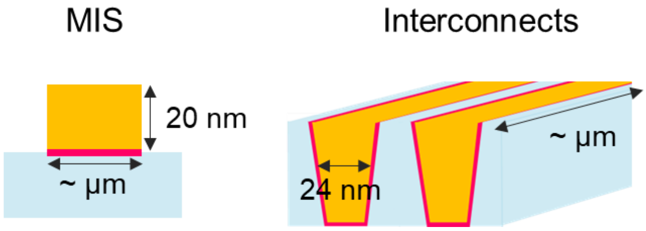


Figure 5.20 Difference between damascene and MIS structure.

Fig. 5.21 shows the leakage current change for each pure Co and Co-Cr alloy when the thickness of the Co-Cr alloy is reduced to 20 nm. There are a few things to note before proceeding with the analysis. First, a Keithley 4200A-SCS instrument was used, but due to equipment failure, the Keysight B1500A was used for this analysis. The difference between the two instruments is that the areas where leakage current can be measured are fA (~ 10^{-15}) and pA (~ 10^{-12}), respectively. Therefore, we could not confirm the section where leakage current temporarily decreased due to the initial electron trapping. In addition, in the process of making a thin device with a thickness of 20 nm, the initial current level increased significantly from ~ 10^{-11} to ~ 10^{-9}. This is expected to be a patterning issue during the photo process. Compared to pure Co, the V_{BD} of Co-Cr alloys increased due to the barrier effect. This result is consistent with the previous 150 nm thick sample. It seems that the size effect of the metal linewidth does not have a significant effect in the part where Cr diffuses on the surface or forms a diffusion barrier.

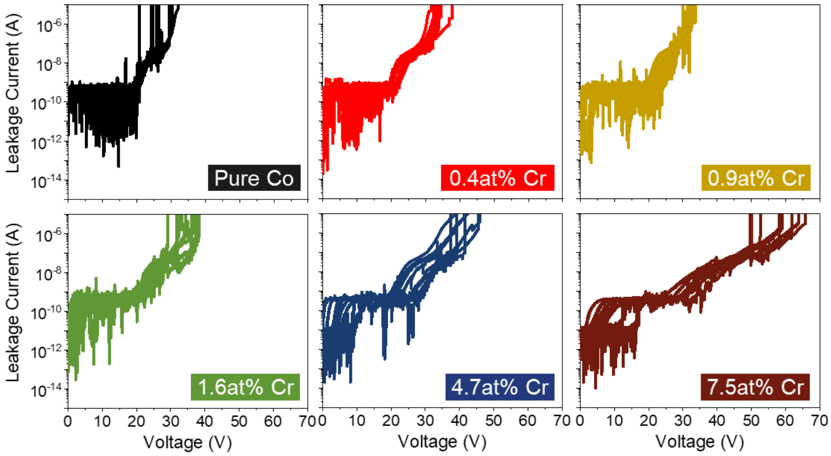


Figure 5.21 Size (metal thickness) effect of Co-Cr alloys with MIS structure.

However, the difference from the 150 nm Co-Cr alloy is that it shows higher V_{BD} characteristics as the Cr doping concentration increases. **Fig. 5.22** shows the V_{BD} changes of 20 nm Co-Cr alloys. Compared to pure Co, Co-Cr alloy shows good V_{BD} properties, and especially the 7.5 at% Cr sample shows very good barrier quality. **Fig. 5.23** is a CDF plot of V_{BD} changes according to Co-Cr alloy thickness. The doping effect of 150 nm thick Co-Cr alloy and 20 nm thick Co-Cr alloy showed opposite V_{BD} behavior. 20 nm Co-Cr showed higher V_{BD} characteristics, and the higher the doping concentration, the better the V_{BD} characteristics. This behavior can be understood in two ways: *Co-Cr thickness effect* and *Cr_2O_3 quality effect*. First, it can be understood in the same context as the V_{BD} improvement according to the annealing temperature mentioned above. It was considered that the lower the annealing temperature, the lower the degree of surface diffusion of Cr and the lower the driving force to create a Cr_2O_3 diffusion barrier by reacting with oxygen. On the other hand, in Co-Cr alloy, the amount of Cr will be less than 150 nm because the film thickness is reduced to 20 nm. For this reason, even if Cr diffuses to the surface during the annealing process, there is not much Cr itself present at the interface. In other words, it was expected that the absolute amount of Cr required to form Cr_2O_3 in the Co-Cr alloy would affect the V_{BD} characteristics when the interconnect linewidth was narrowed. Of course, further analysis is needed to confirm this hypothesis. The next thing to consider is the thickness of the Cr_2O_3 produced.

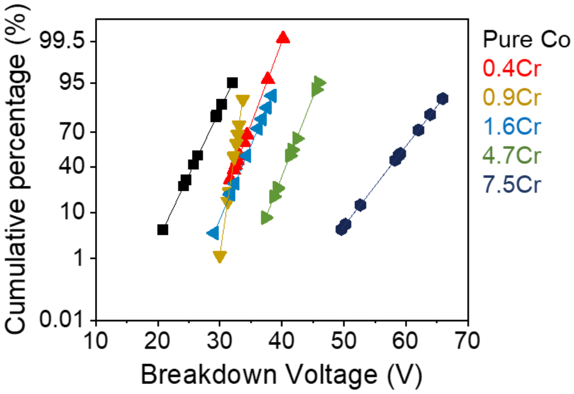


Figure 5.22 CDF plots of 20 nm thick pure Co and Co alloy samples.

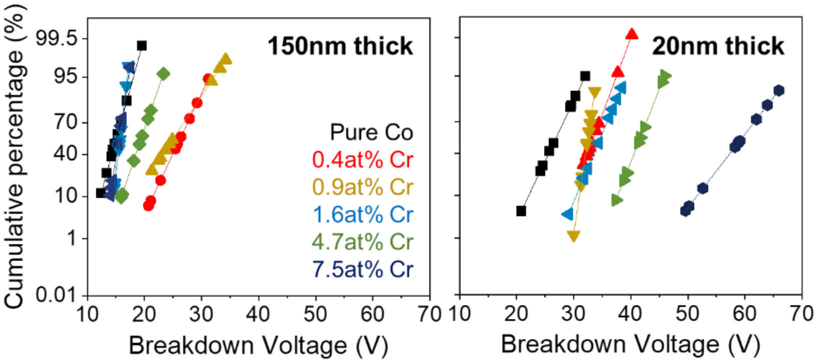


Figure 5.23 Co-Cr layer thickness effect: CDF plot shows breakdown voltage changes when metal linewidth is 150 nm and 20 nm.

As shown in **Fig. 5.24**, Cr is clearly present at the SiO_2 interface after annealing. As the doping concentration increases, Cr_2O_3 becomes thicker, and it is observed that the intensity of Si in SiO_2 increases. Previously, it was predicted that too much Cr reacts with oxygen at the interface to form free Si when the Cr doping concentration of 150 nm Co-Cr is 7.5 at%. The same behavior was also observed in 20 nm Co-Cr, so why is the barrier quality greatly improved? Although a detailed analysis of this part should be carried out, it can be understood that the most suitable conditions for forming the Cr_2O_3 self-forming barrier are provided as the absolute amount of Cr itself decreases while reducing the thickness of Co-Cr. This is because the Cr_2O_3 barrier can be formed thick enough at the interface if an appropriate amount of Cr compared to the volume of the interconnect has a sufficient reaction temperature and time. Since Cu-Mn alloy was also applied as a PVD seed layer, it seems advantageous to use a Co-Cr alloy with a high Cr doping concentration when using a PVD seed layer. In summary, the V_{BD} properties improved as the doping concentration increased in the 20 nm Co-Cr alloy sample. The reason can be explained by the *Co-Cr thickness effect* and the *Cr_2O_3 quality effect*. If a certain amount of Cr diffuses on the surface to form a Cr_2O_3 self-forming barrier with low impurity at a sufficient temperature, it seems that Co ions can be effectively blocked even at high doping concentrations.

However, in the HR-TEM image of **Fig. 5.25**, it was difficult to confirm the thickness change or interface difference of the Cr_2O_3 self-forming barrier according to the doping concentration. It was difficult to confirm even in STEM because it forms a very thin barrier. However, as the doping concentration increased, it was confirmed that the interface with SiO_2 became unclear. In this study, as the cause of this behavior, free Si was formed at the interface like Cr_2O_3, so it was expected that the degree of amorphization would increase, and the interface would become unclear.

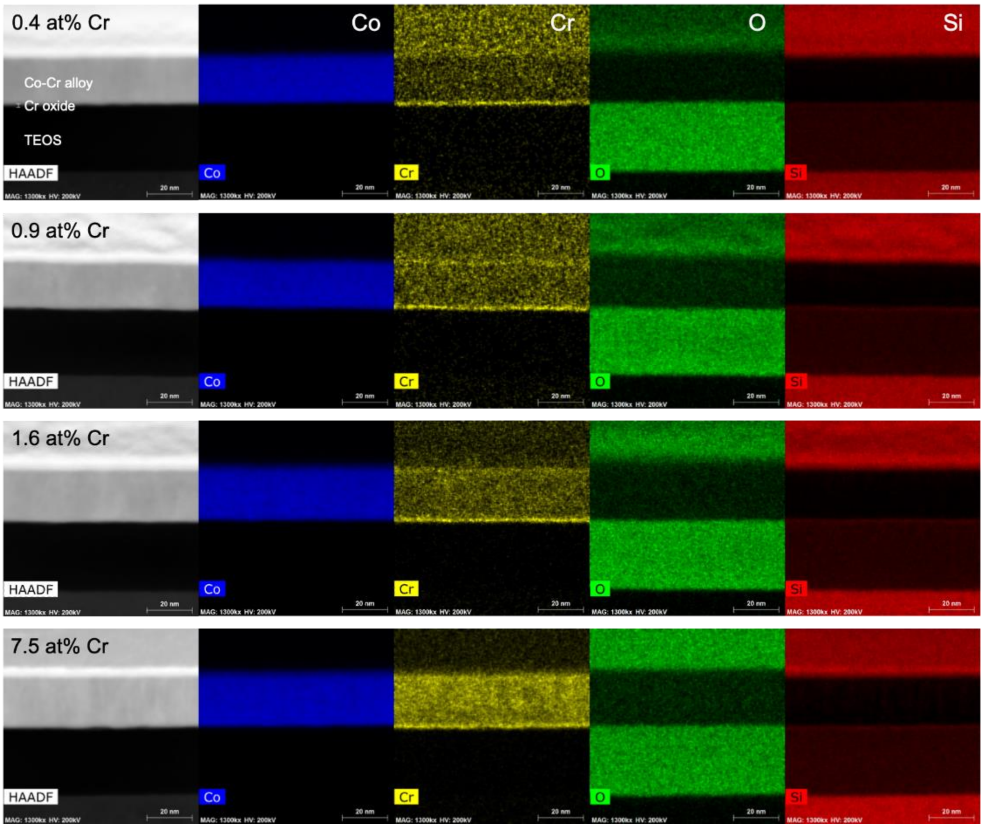


Figure 5.24 EDS mapping images for each 20 nm Co-Cr alloy (0.4 at% Cr - 7.5 at% Cr) using high resolution EDS.

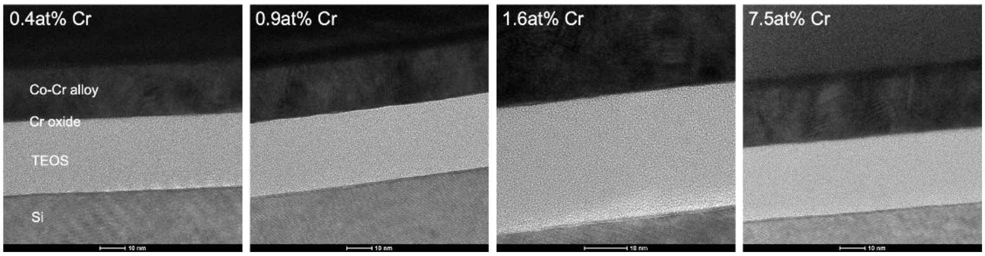
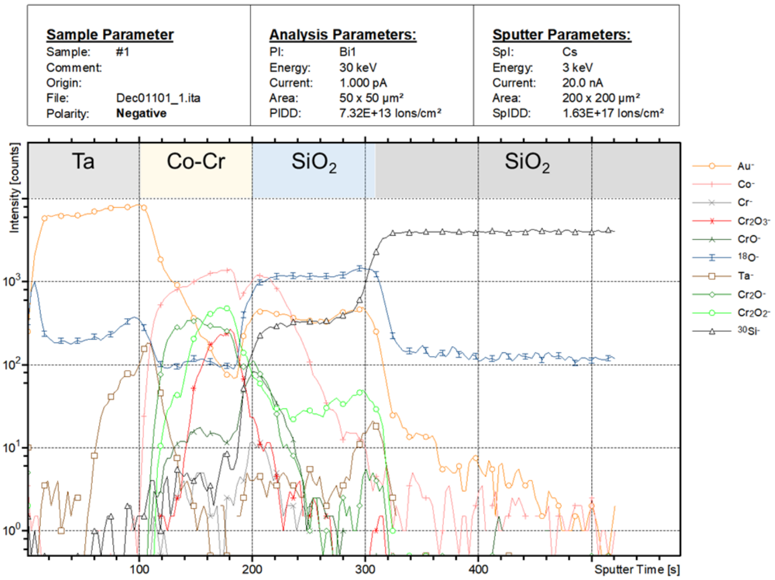

0.4at% Cr
Co-Cr alloy
Cr oxide
TEOS
Si
0.9at% Cr
1.6at% Cr
7.5at% Cr
10 nm

Figure 5.25 HR-TEM images for 20 nm Co-Cr alloys (0.4 at% Cr - 7.5 at% Cr).

Fig. 5.26 shows the result of ToF-SIMS (Time-of-Flight Secondary Ion Mass Spectrometry) depth profile after annealing the 0.4 at% Cr-doped sample. It can be confirmed that Cr_2O_3 exists at the interface between Co-Cr and SiO_2. Since SIMS analysis has different ionization rates for each element, it was difficult to compare quantitative analysis. **Fig. 5.27** is a 7.5 at% Cr sample and shows the same trend. In other words, it is formed as a Cr_2O_3 self-forming barrier during the annealing process to prevent the movement of Co ions. Cr^- exists next to $Cr_2O_3^-$, and since the ionization rates in the SiO_2 matrix and the Co-Cr matrix are different, it can be interpreted as a Cr_2O_3 phase rather than the presence of Cr. In this regard, it is necessary to accurately identify the depth profile by additionally performing other depth profile analysis such as XPS. Since ToF-SIMS analysis measures the mass of elements that are ionized by about 5%, it will be necessary to obtain a standard sample for quantitative analysis.

Fig. 5.28 shows the results to confirm the selective oxidation behavior of Cr in Co-Cr alloy through modeling. [144] As a result of the experiment, Cr has a higher oxygen affinity than Co, but an amorphous oxide network is mainly formed in Co. This oxide network acts as a driving force for Cr to move in the lattice as seen in the 2nd layer. At this time, O atoms diffuse further down due to Cr and Co vacancies. It has been reported that selective oxidation occurs when Cr diffuses. Looking at the literature results, it will be possible to understand the V-shape distribution at the interface of Co^- in ToF-SIMS. In addition, Cr is a major element forming the oxide layer in the Co-Cr alloy.

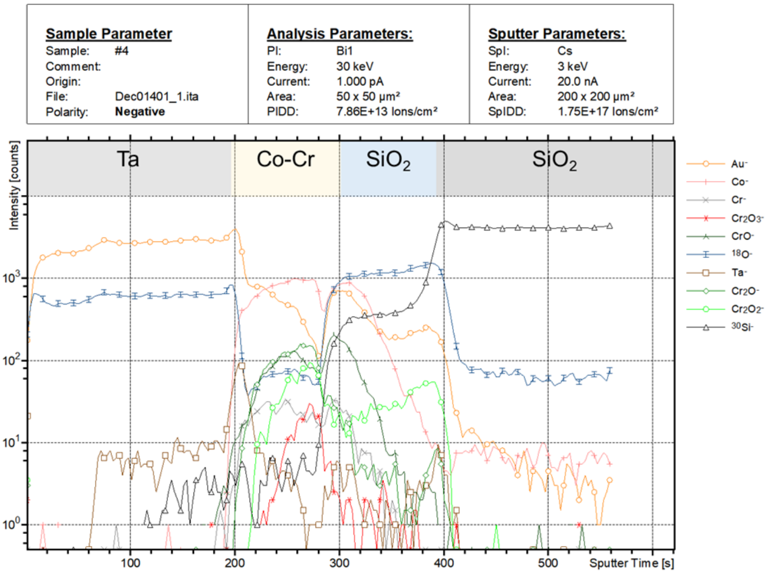


Sample Parameter
Sample: #1
Comment:
Origin:
File: Dec01101_1.ita
Polarity: **Negative**

Analysis Parameters:
PI: Bi1
Energy: 30 keV
Current: 1.000 pA
Area: 50 x 50 µm²
PIDD: 7.32E+13 Ions/cm²

Sputter Parameters:
SpI: Cs
Energy: 3 keV
Current: 20.0 nA
Area: 200 x 200 µm²
SpIDD: 1.63E+17 Ions/cm²

Figure 5.26 TOF-SIMS depth profile of Co-0.4at% Cr alloy after annealing at 450 °C for 2 hours.



Sample Parameter
Sample: #4
Comment:
Origin:
File: Dec01401_1.ita
Polarity: **Negative**

Analysis Parameters:
PI: Bi1
Energy: 30 keV
Current: 1.000 pA
Area: 50 x 50 µm²
PIDD: 7.86E+13 Ions/cm²

Sputter Parameters:
SpI: Cs
Energy: 3 keV
Current: 20.0 nA
Area: 200 x 200 µm²
SpIDD: 1.75E+17 Ions/cm²

Figure 5.27 TOF-SIMS depth profile of Co-7.5at% Cr alloy after annealing at 450 °C for 2 hours.

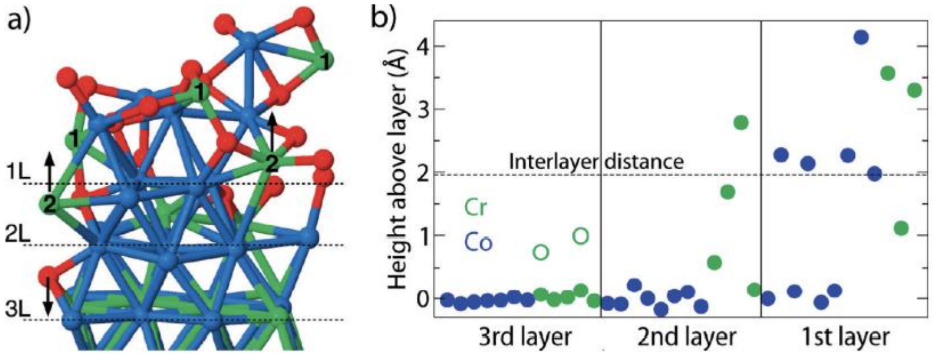


Figure 5.28 Selective Cr oxidation behaviors in CoCr alloy: arrows indicate the driving force direction of each element in the oxidation process, and the figure on the right indicates the displacement of each atom after MD and geometry relaxation.[144]

5.2.2. Lifetime evaluation using TDDB method

The TDDB lifetime evaluation is in progress with Samsung Electronics' reliability team, and only the results that have been produced so far will be mentioned. As soon as additional analysis results are released, it is expected that the influence of pure Co, TiN barrier, and Cr doping concentration will be confirmed. **Fig. 5.29** is the result of analyzing the TDDB lifetime according to the electric field and Cr doping concentration. The best lifetime was seen in the 0.9 at% Cr sample. It is difficult to say that the lifetime of the Co-Cr alloy has improved because the results for pure Co and high Cr doped samples have not been obtained yet. However, when it was below 1 at%, it showed a similar trend to the VRDB data showing high barrier quality. **Fig. 5.30** shows the lifetime with the e-fields. The dependence on the E-field is not as large as the lifetime characteristic variation with the Cr doping concentration. In the future, we plan to obtain more data to compare VRDB and TDDB results and to verify the effectiveness of the Cr_2O_3 self-forming barrier.

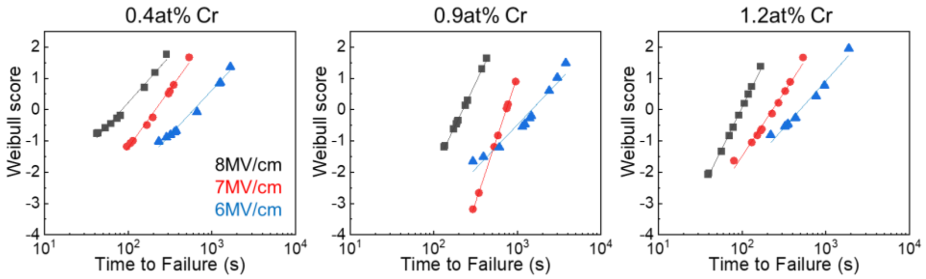


Figure 5.29 TDDB Weibull plot with doping concentration: Analysis was performed at 200 °C and E-field variations (6, 7, 8 MV/cm) with 150 nm thick Co-Cr alloys.

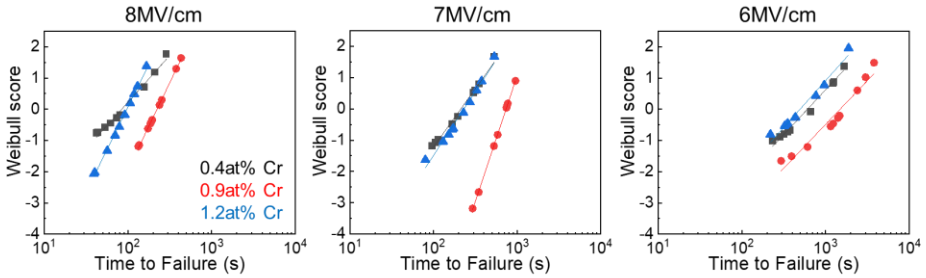


Figure 5.30 TDDB Weibull plot with E-field: Analysis was performed at 200 °C.

5.2.3. Barrier mechanism using DFT

Through the previous electrical reliability evaluation, it was confirmed that Co-Cr alloy has superior reliability than pure Co because it forms a robust Cr_2O_3 self-forming barrier. It was found that the barrier quality was significantly different according to Cr doping concentration, annealing temperature, and Co-Cr alloy thickness (metal linewidth). Although it was confirmed through HRTEM and EDS analysis that Cr was present at the SiO_2 interface, it was difficult to accurately analyze the interface such as SAED and DP because the diffusion barrier was very thin. Cr_2O_3 passivation layer is also used as a passivation film in stainless steel, and it is known that it is very difficult to observe the passivation film in related studies. In this study, it was confirmed that Cr_2O_3 existed as a stable phase at the interface through thermodynamic calculations and ToF-SIMS analysis. Also, Density functional theory (DFT) calculations were performed to confirm that the Cr_2O_3 diffusion barrier exhibits higher reliability than the TiN diffusion barrier, which is currently being studied in the industry. In recent DFT studies, it has been calculated that Cr_2O_3 exhibits anisotropic diffusion behaviors between in-plane and out-of-plane. [145] The fact that it is not easy for metal ions to move in the out-of-plane direction in Cr_2O_3 is also expected to show the same trend for the movement of Co ions. For more information on DFT calculation, refer to section 3.5. In general, electrical extrinsic failure in interconnects requires metal ions to penetrate the diffusion barrier and form metal filaments in the dielectric. If it is assumed that metal ions move in the vacancy-to-vacancy, vacancy-to-interstitial, and interstitial-to-interstitial paths within the barrier, the region with the highest barrier height among each path will determine the diffusion barrier properties of the material. and the calculation of the diffusion barrier for the vacancy-to-interstitial for Cr_2O_3 and the interstitial-to-interstitial path for TiN has been completed so far. The calculation priority was determined by referring to the literature for each material. [146-147] **Fig. 5.31** schematically illustrates the path that Co diffusion moves through the interstitial in TiN and Cr_2O_3. The diffusion barrier height when Co moves along this path was calculated through DFT.

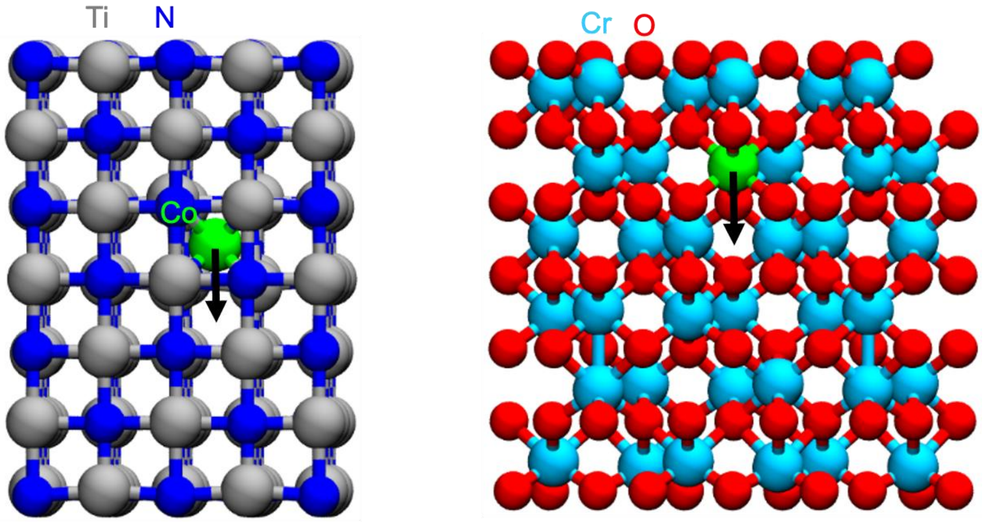


Figure 5.31 Co diffusion in TiN lattices (upper) and Cr_2O_3 lattices (lower).

As can be seen in **Fig. 5.32**, the barrier energy of TiN was 1.08 eV, whereas that of Cr_2O_3 was 1.34 eV, which was higher than TiN. In other words, it is more difficult for Co ions to migrate to the Cr_2O_3 self-forming barrier than the TiN barrier. Calculations were carried out with a crystal structure, and vacancy-to-interstitial diffusion in Cr_2O_3 and interstitial-to-interstitial diffusion in TiN were calculated. Based on the results so far, the movement of Co ions is difficult in Cr_2O_3 compared to TiN. Of course, since the diffusion path is different, it is necessary to perform additional calculations considering the same path and multiple paths. This is because, in TiN or Cr_2O_3, the movement of Co ions is determined depending on the low diffusion barrier path, respectively. It is important to compare the paths with the lowest energy barrier height for each material. In this study, it was expected that the reliability of Co interconnects could be improved by using a Cr_2O_3 self-forming barrier with a thickness of 1.2 nm, and the DFT calculation results agree well with this. Since the TiN crystal structure has a cubic structure, whereas Cr_2O_3 has a corundum structure, the interstitial-to-interstitial path of Cr_2O_3 may have a high barrier height. Therefore, to determine which path is the lowest diffusion path and which barrier is more suitable for the Co interconnect, it is necessary to obtain the DFT calculation results for future vacancy-to-vacancy, vacancy-to-interstitial, and interstitial-to-interstitial.

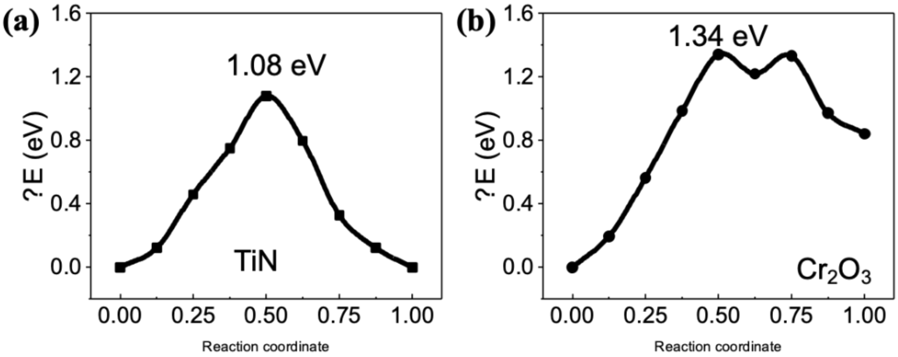


Figure 5.32 Co diffusion barrier difference in TiN (interstitial-to-interstitial) and Cr_2O_3 (vacancy-to-interstitial).

5.3. Summary

In **Chapter 5**, the process compatibility and reliability of Co-Cr alloys were evaluated. First, the resistivity analysis of the Co-Cr alloy thin film according to Cr doping concentration, annealing temperature, and annealing time was performed. In order to realize a low resistivity interconnects, it is necessary to manufacture a Co-Cr alloy with a doping concentration of 1.6 at% or less. In the case of annealing temperature, it has been confirmed that the Cr_2O_3 self-forming barrier is formed up to 250 °C, so it is likely to be sufficiently applicable to the interconnect process. Next, it was confirmed whether the Co-Cr alloy could form a diffusion barrier with high reliability through VRDB and TDDB reliability evaluation of the Co-Cr alloy.

Cr_2O_3 self-forming barrier quality was evaluated according to Cr doping concentration, annealing temperature, and Co-Cr alloy thickness using the VRDB method. The Cr doping concentration (~ 0.9 at%) of 150 nm Co-Cr showed excellent Cr_2O_3 self-forming barrier properties with an ultra-thin film thickness of ~1.2 nm. When the doping concentration is too high, it was confirmed that Cr consumes a lot of oxygen in the SiO_2 dielectric, and the diffusion barrier property deteriorates due to the mixture of free Si and metallic Cr. Next, the annealing temperature showed the best diffusion barrier quality at 350 °C. Even when Cr was doped with a high concentration, it showed excellent properties. In the low-temperature process, it was expected that a high-quality Cr_2O_3 film could be obtained because the driving force for forming the Cr_2O_3 self-forming barrier was lower than 450 °C. On the other hand, since Cr may still exist in Co, it is necessary to consider the optimal annealing process by considering line resistance and lifetime evaluation as well. Finally, when the thickness of the Co-Cr alloy was as thin as 20 nm, excellent barrier quality properties were exhibited even at high doping concentrations due to the Co-Cr thickness effect and the Cr_2O_3 thickness effect. When the wiring line width is narrowed, the amount of Cr is reduced in consideration of the volume in order for the Co-Cr alloy to form Cr_2O_3. It seems that only an appropriate amount of Cr reacts on the surface to form Cr_2O_3 of good quality. It was confirmed once again that free Si was formed at high doping concentration. Nevertheless, it is expected that the reason for the improved reliability is that the thickness of the good quality Cr_2O_3 barrier increases as Cr and oxygen continuously react. If a certain amount of Cr is diffused on the surface to form a Cr_2O_3 self-forming barrier with few impurities (free Si and metallic Cr) at a sufficient temperature, it seems that Co ions can be effectively blocked even at a high doping concentration.

Because the TDDB analysis results were not all out, it could not be said that Co-Cr alloy showed higher lifetime characteristics than pure Co. However, a trend like the VRDB data showing high barrier quality below 1 at% was confirmed. After obtaining lifetime data, we will compare VRDB and TDDB results and verify the effectiveness of the Cr_2O_3 self-forming barrier. Finally, the difference in barrier energy between the traditional TiN barrier and the Cr_2O_3 self-forming barrier was confirmed through DFT calculation. It was confirmed that the barrier energy of TiN was 1.08 eV, whereas that of Cr_2O_3 was 1.34 eV. Accordingly, when a Cr_2O_3 self-forming barrier having a thickness of 1.2 nm is used, the reliability of the Co interconnects can be enhanced. This study showed the applicability of a new material system called $Co/Cr_2O_3/SiO_2$ to the interconnect process. As a result, it was possible to confirm the promising Cr_2O_3 self-forming barrier properties that can replace the existing TiN barrier with high process compatibility and high reliability.

CHAPTER 6

Conclusion

6.1. Summary of results

In this study, a robust diffusion barrier material with an ultra-thin thickness, which is essential to evolve into a 3G interconnect (Co/low-k) systems beyond the Cu interconnection was studied. Co/Cr_2O_3/SiO_2 material system has been proposed considering low *RC* delay (*performance*) and excellent barrier properties (*reliability*) as interconnects continue to get smaller. Co alloy material design and verification, and the compatibility of Cr_2O_3 self-forming barrier were confirmed. Considering thermodynamic parameters such as bulk resistivity, solubility limit, intermetallic compound formation, activity coefficient, oxidation formation energy, and interfacial stable phase, it was confirmed that Co-Cr alloy exhibited the best self-forming barrier behavior. Since the experimental results and the thermodynamic material design rule agree well, it can be said that the Co alloy self-forming barrier design is an effective methodology. It was shown that a Cr_2O_3 self-forming barrier with a very thin thickness of 1.2 nm was formed and had a clean interface profile with the SiO_2 interface.

Next, the process compatibility of Co-Cr alloy was confirmed. In the case of annealing temperature, the Cr_2O_3 self-forming barrier is formed up to 250 °C, so it is likely to be sufficiently applicable to the interconnect process. Cr_2O_3 self-forming barrier quality was evaluated according to Cr doping concentration, annealing temperature, and Co-Cr alloy thickness. Through this, if a certain amount of Cr is diffused on the surface to form a Cr_2O_3 self-forming barrier with few impurities at a sufficient temperature, it seems that Co ions can be effectively blocked. Through TDDB lifetime analysis, it was confirmed that it was in good agreement with the VRDB results. Finally, through the DFT calculation, it was confirmed that the Cr_2O_3 self-forming barrier has a high diffusion barrier height over the traditional TiN barrier.

In this study, a novel interconnection material system called $Co/Cr_2O_3/SiO_2$ was proposed. For next-generation interconnects to be used, *performance* and *reliability* must be accomplished, and the $Co/Cr_2O_3/SiO_2$ system was able to satisfy both standards. It was confirmed that an excellent Cr_2O_3 self-forming barrier was formed when the Co self-forming barrier design rule was used. As the metal linewidth continues to decrease, the Co-Cr alloy self-forming barrier can solve the problem of extrinsic failure behavior of Co metal, which is referred to as a next-generation interconnect material.

6.2. Research perspectives

As shown in **Fig. 6.1**, the VLSI system has been continuously scaled down from the 1970s to the present. The reason why the transistor could be continuously scaled down was not only the innovative change in architecture but also the change in material played a very big role. Especially, for semiconductor interconnects, the era of 3rd generation interconnects beyond Al and Cu interconnects is fast approaching. As the saying goes that there is opportunity in crisis, new interconnects will necessarily require a new material system. In this aspect, it is hoped that the results of this study ("Design and Electrical Reliability of Co Alloy Self-Forming Barrier for Advanced Interconnects") provide a good direction for research beyond the current Cu interconnects where the entire world is digitizing.

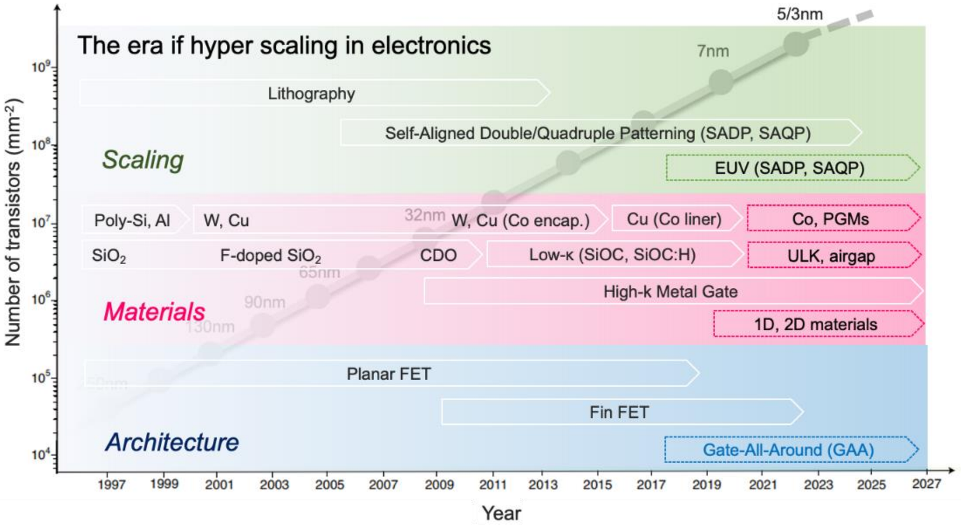


Figure 6.1 The era of hyper-scaling in electronics: materials are one of the keys to moving forward beyond current VLSI systems.

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요약(국문초록)

최근 반도체 소자 스케일링에 따른 배선 선폭 감소로 M0, M1 영역에서의 metal 비저항이 급격히 증가하여 배선에서의 *RC* delay 가 다시 한번 크게 문제가 되고 있다. 이를 해결하기 위해서 차세대 배선 시스템에서는 낮은 비저항과 electron mean free path (EMFP)을 가지는 물질 연구가 진행되었다. 대표적으로 Co, Ru, Mo 와 같은 금속들이 차세대 배선 재료 후보로 언급되고 있으며 낮은 $\rho_0 \times \lambda$ 값을 갖기 때문에 interface (surface) scattering 과 grain boundary scattering 영향을 최소화할 수 있을 것으로 보고 있다. 하지만 가혹한 electrical field 와 높은 *Joule* heating 이 발생하는 동작 환경으로 인해 performance 뿐만 아니라 소자 신뢰성이 더 열악한 상황에 놓여있다. 예를 들어 차세대 금속에 대한 time dependent dielectric breakdown (TDDB) 신뢰성 문제가 보고되고 있기 때문에 이를 보안할 확산방지막 물질 및 공정연구가 필요하다. 특히 높은 전기장에서 Co ion 이 유전체로 침투하여 extrinsic dielectric breakdown 신뢰성 문제가 최근 보고되고 있다. 따라서 금속 이온이 유전체 내부로 침투하는 것을 방지하여, Co 배선의 신뢰성을 향상시킬 수 견고한 확산방지막 개발 및 새로운 배선 시스템 설계가 필요한 시점이다. 또한, 배선 저항을 낮추기 위해서는 매우 얇은 확산방지막 개발이 필요하다. 신뢰성이 좋은 확산방지막이라도 배선에서 많은 영역을 차지할 경우 전체 성능이 저하되기 때문이다. Cu 확산방지막으로 사용되고 있는 TaN 층은 2.5 nm 보다 얇을 경우 신뢰성이 급격히 나빠지므로 2.5 nm 보다 얇은 두께의 견고한 확산방지막 개발이 필요하다.

본 연구는 차세대 반도체 배선 물질로 주목받고 있는 Co 금속에 대하여 저저항 · 고신뢰성을 확보할 수 있는 Co alloy 자가형성 확산방지막 (Co alloy self-forming barrier, SFB) 소재 디자인하였다. 자가형성 확산방지막 방법론은 열처리 과정에서 금속과 유전체 계면에서 도펀트가 확산하게 된다. 그리고 확산되니 도펀트는 얇은 확산방지막을 형성하는 방법론이다. 이 방법론을 통해 금속 이온의 이동을 방지하여 Co 배선 신뢰성을 향상시킬 수 있을 것으로 예상하였다. 우선, Co 합금상에서 적절한 도펀트를 찾기 위해서 CMOS 공정에 적용 가능한 금속들을 선별하였다. 도펀트 저항, 금속간 화합물 형성 여부, Co 내 고용도, Co alloy 에서의 활성계수, 산화도, Co/SiO$_2$ 계면에서의 안정상을 열역학적 계산을 통해서 물질 선정 기준으로 세웠다. 열역학적 계산을 기반으로 9 개의 도펀트 금속이 선택되었으며, Co 합금 자가형성 확산방지막 기준에 따라서 우선 순위를 지정하였다. 그리고 최종적으로 박막과 소자 신뢰성 평가를 통해서 가장 적합한 자가형성 확산방지막 물질을 선정하였다. X-ray photoelectron spectroscopy (XPS) 분석을 이용하여 Cr, Zn, Mn 이 박막 구조의 표면으로 외부 확산 여부를 확인하고 결합 에너지 분석을 통해 외부로 확산된 도펀트의 화학적 상태를 조사하였다. 분석 결과 Cr, Zn, Mn 이 유전체 계면으로 확산되어 산소와 반응하여 oxide/silicate 확산 방지막 (e.g. Cr_2O_3, Zn_2SiO_4, $MnSiO_3$)을 형성한 것을 확인하였다. 그 중 Cr 은 SiO$_2$ 유전체와 함께 가장 이상적인 자기 형성 거동을 나타내며 산소와 반응하여 Cr_2O_3 층을 형성하는 것을 확인하였다. MIS (Metal-Insulator-Semiconductor) 구조에서도 외부로 확산된 Cr 은 계면에서 SiO$_2$ 와 반응하여 Cr_2O_3 자가형성 확산방지막이 형성되었다. 확산방지층의 두께는 약 1.2nm 로 전체 유효저항을 최소화할 수 있는 충분히 얇은 두께를 확보하였다. VRDB (Voltage-Ramping Dielectric Breakdown) 테스트를 통해 Co-Cr 합금은 순수 Co 보다 최대 200% 높은 항복 전압 (breakdown voltage)을 보였다.

반도체 배선 공정에 적용할 수 있는 Cr 도핑 농도와 열처리 조건의 영향을 확인하였다. Cr 이 1at% 미만으로 도핑되었을 때 우수한 전기적 신뢰성을

나타내었다. 또한, 250℃ 이상에서 30 분 이상 열처리를 하였을 때 Cr_2O_3 계면층이 형성됨을 알 수 있었다. 즉, 현재 배선 공정 온도가 400° C 미만이기 때문에 Co-Cr 합금이 배선 공정에 적용 가능함을 확인하였다. TDDB 수명 테스트도 수행되었으며 Co-Cr 합금 배선은 자체 형성된 계면층의 매우 안정적인 확산 장벽 특성을 보여주었다. DFT 분석은 Cr_2O_3 자가형성 확산방지막이 현재 연구되고 있는 TiN 확산 장벽보다 더 높은 에너지 장벽 값을 보여주기 때문에 매우 유망한 확산방지막임을 보여주었다.

본 연구는 반도체 배선 물질 시스템에서 성능과 신뢰성을 고려한 열역학적 계산을 통해 Co 기반 자가형성 확산방지막을 설계하였다. 실험 결과 신뢰성이 우수하고 아주 얇은 Cr_2O_3 확산방지막이 있는 Co-Cr 합금이 제안하였다. 물질 설계와 전기적 신뢰성 검증을 $Co/Cr_2O_3/SiO_2$ 물질 시스템을 제안하였고 앞으로의 다가올 차세대 배선에서 구현될 수 있을 것으로 기대된다.

표제어: 차세대 배선 시스템, 코발트, 유효 비저항, 배선 신뢰성, 자가형성 확산방지막, 확산방지막, 코발트 크롬 합금, 크롬 산화물

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RESEARCH EXPERIENCES

Material design and electrical reliability of Co-Cr alloy interconnects using self-forming barrier (SFB) for advanced Co interconnect system

- Designing Co alloy self-forming barrier using thermodynamics for robust reliability and high-performance interconnect system.

- Identifying TDDB reliability of Co interconnects based on Cr_2O_3 barrier and TiN barrier under 5 nm VLSI technology
- Measurement and analysis with wafer-level reliability test (VRDB) and package-level reliability test (TDDB)
- Investigation of percolation path for conduction mechanism in dielectrics
- Theoretical study to correlate diffusion barrier transport mechanism and dielectric breakdown

Theoretical study of dielectric reliability in Cu interconnects

- Identifying interfacial adhesion effect between capping layer and dielectric in Cu interconnects
- Failure analysis (FA) of Cu interconnect using microstructural method; TEM, EDS, ASTAR
- Correlation interfacial adhesion of capping materials and electromigration characteristic of Cu interconnects
- Measurement and analysis of 4-point bending (4-PB) test and double-cantilever beam (DCB) test

Design of planar-radial structured thermoelectric cooler (TEC) for local hot spot cooling in mobile electronics

- Designing planar-radial structure thermo-electronics with mobile form factor for dynamic thermal management (DTM)
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Analysis on p-type tin oxide thin films using various Sn-SnO composite target by RF reactive magnetron sputtering

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- Improving the electrical property of p-type SnO thin film with respect to a sputtering condition; oxygen pressure, plasma power, tin concentration
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PRESENTATIONS IN INTERNATIONAL CONFERENCE

Oral Presentations

- Analysis of Interfacial Adhesion Energy between Dielectric/Capping Layers of Interconnects", *KMEPS fall*, Seoul (online), Korea (Feb. 2020)
- Planar-Radial Structured Thermoelectric Cooler for Local Hot Spot Cooling in Mobile Electronics", *IEEE ECTC*, Florida (online), US (June. 2020) (*Future Packaging Vision Contest Award*)

Poster Presentations

- Thickness effect of horizontal thermoelectric cooling device on different substrates, *KMEPS spring*, Gyeonggi-do, Korea (Apr. 2019)
- The study of two-dimensional horizontal thermoelectric Peltier cooling device, *ISMP fall*, Gangwon-do, Korea (Dec. 2018)

- The study of 2D horizontal thermoelectric Peltier cooling for hot spot control of on-chip mobile electronics, *Korean Conference on Semiconductors*, Seoul, Korea (Feb. 2018) (*Best Poster Award*)
- The effect of annealing on the structural and electrical properties of sputter-deposited SnOx thin films by a composite target, *Korean Conference on Semiconductors*, Seoul, Korea (Feb. 2017)

R&D PROJECTS

- "Gas-solid reaction induced defect control, polymorphic transition and their applications in TMD materials", funded by Ministry of Science and ICT, 2021. 3. ~ present.
- "Research on Microstructure and Bump and RDL Reliability of Nano-Twin Cu", Cooperative System Project funded by SK Hynix Co., Ltd., 2020. 5. ~ present.
- "A Study on Robust Reliability Interconnects for Next-Generation Logic Devices", Cooperative System Project funded by Samsung Electronics Co., Ltd., 2018. 3. ~ 2021. 5.
- "Development of Energy Reduction Technology through Planar-Radial Structured Cooler of Mobile Ddevices", The MOTIE (Ministry of Trade, Industry and Energy) and KSRC (Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device, 2017. 08. ~ 2019. 07.
- "Internal Electrode Material Improvement and Stress Analysis for High-Capacity MLCC Development", Cooperative System Project funded by Samsung Electro-Mechanics Co., Ltd., 2017. 08. ~ 2018. 07.