**Ph. D. DISSERTATION**

# Self-Heating and Electrothermal Properties of Sub-5-nm 3-D Transistors

## 5nm 이하 3D Transistors 의 Self-Heating 및 전열특성 분석 연구

**BY**

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# Self-Heating and Electrothermal Properties of Sub-5-nm 3-D Transistors

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In this thesis, Self-Heating Effect (SHE) is investigated using TCAD simulations in various Sub-10-nm node Field Effect Transistor (FET). As the node decreases, logic devices have evolved into 3D MOSFET structures from Fin-FET to Nanosheet-FET. In the case of 3D MOSFET, there are thermal reliability issues due to the following rea sons: i) The power density of the channel is high, ii) The channel structure surrou nded by $SiO_2$, iii) The overall low thermal conductivity characteristics due to scaling down. Many papers introduce the analysis and prediction of temperature rise by SHE in the device, but there are no papers presenting the content of mitigation of temperature rise. Therefore, we have studied the methods of decreasing the maximum lattice temperature ($T_{L,max}$) such as shallow trench isolation (STI) composition engineering in Fin-FET, thermal analysis according to DC/AC/duty cycle in nanowire-FET, and active region

( e.g., gate metal thickness, channel width, channel number etc..) optimization in nanosheet-FET. In addition, lifetime affected by hot carrier injection (HCI) / bias-temperature instability (BTI) is also analyzed according to various thermal relaxation methods presented.

**Keywords:** Self-Heating Effect (SHE), Nanoplate-FET, Nanowire-FET, FinFET, Vertical-FET, Thermal resistance, Temperature, Time delay, Bias Temperature Instability (BTI), Hot Carrier Injection (HCI).

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# Chapter 1

# Introduction

## 1.1 Development of semiconductor structure

As CMOS technology scales down to a sub-20-nm node, the device experiences severe short-channel effects (SCEs) [1], [2]. To mitigate SCE and have good electrostatic gate control, good subthreshold slope, low-leakage current, and higher transistor density, as shown in Fig. 1.1 device structures have changed from planar structures to multi-gate structures (FinFET). However, as the technology node scaled down from 7 to 5 nm, the FinFET device did not have sufficient electrostatic gate controllability [3]–[5] and thus could not provide further improvement. The gate-all-around (GAA) structure, on the other hand, was a strong candidate for scaling down on sub-5-nm nodes [3]. Furthermore, a nanosheet (NS) structure for better performance has been introduced in [4]. However, even with advanced channel structures of GAA devices, contact gate pitch (CGP) scaling of conventional lateral devices is severely limited by gate length, spacer thickness, and source/drain contact size [5]. Accordingly, vertical nanowire FETs (VFETs) have been proposed to solve the CGP problem and improve scalability. In the conventional device,

the channel is oriented horizontally, while the VFET is oriented vertically. Also, source and drain are at the bottom and top, respectively, with the gate at the center [6]–[9]. Through this vertically oriented structure, the gate length and spacer thickness relaxed CGP and then the SCE can be further mitigated as a result [6]–[9]. VFETs are also more power efficient and have smaller foot prints than lateral field effect transistors of the same node. However, there is no solution for how to induce stress in the channel during VFET fabrication yet and thus cannot increase channel mobility, leading to a lower $I_{ON}$ compared to the lateral nanowire FET. Taking this situation into consideration, we have introduced an NS-VFET that makes the width of the channel wide in the nanowire structure to compensate for the weakness of $I_{ON}$ of VFETs.

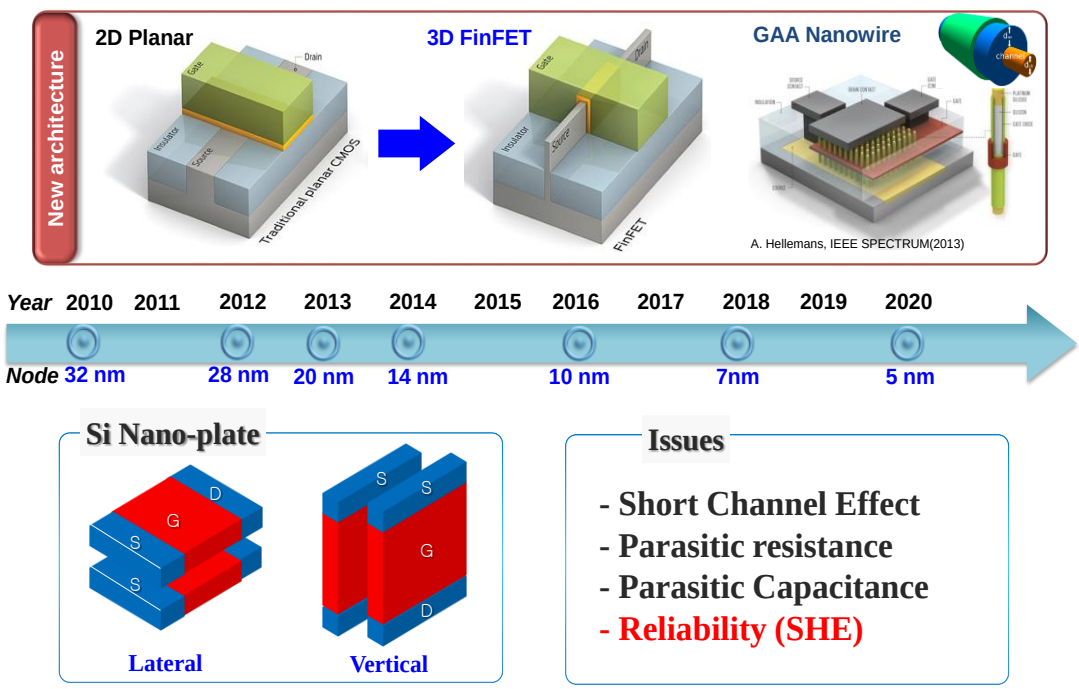


**Fig. 1.1.** Device structure change according to node and various emerged issues.

## 1.2 Self-Heating Effect issues in Semiconductor devices

On the other hand, self-heating effect (SHE) is the accumulation of heat in the channel at high-power levels. This is caused by the high current density, material with low thermal conductivity such as SiO2, and a reduced dimension of devices due to downscaling. In the case of Bulk and silicon on insulator (SOI) FinFETs, SiO2 with low thermal conductivity (gate dielectrics; 1.1–1.4 $W \cdot m^{-1} \cdot K^{-1}$) surrounds the three sides of the channel [10], [11]. Especially for SOI FinFETs, substrate is also blocked by SiO2 buried oxide (buried oxide (BOX); 1.4 $\cdot m^{-1} \cdot K^{-1}$). Therefore, it is impossible to efficiently dissipate heat generated at the channel. In the case of the VFET, the channel is entirely surrounded by SiO2, which makes it difficult to efficiently dissipate the heat generated from the channel. Also, although VFET is not the SOI structure, the drain is located at the bottom as mentioned earlier, and heavily doped drain has low thermal conductivity due to the phonon impurity scattering [12]. For these reasons, the heat dissipation characteristics to the substrate of VFET are also poor. Furthermore, as the device downscaled, the dimensions of the devices (Bulk/SOI FinFET and VFET) became smaller than that of the phonon mean-free-path (100–300 nm). As a result, the thermal conductivity of the Si lattice is influenced by phonon boundary scattering [12], which is lower than that of bulk Si (150 $W \cdot m^{-1} \cdot K^{-1}$) and deteriorates SHE. The lattice temperature ($T_{Lattice}$) elevated by SHE further aggravates the vibrations of the lattice, thereby reducing the mobility of the carriers and thus causing performance degradation. In addition, the elevated $T_L$ further aggravates the hot carrier injection (HCI) and bias temperature instability (BTI), causing problems with reliability [13].

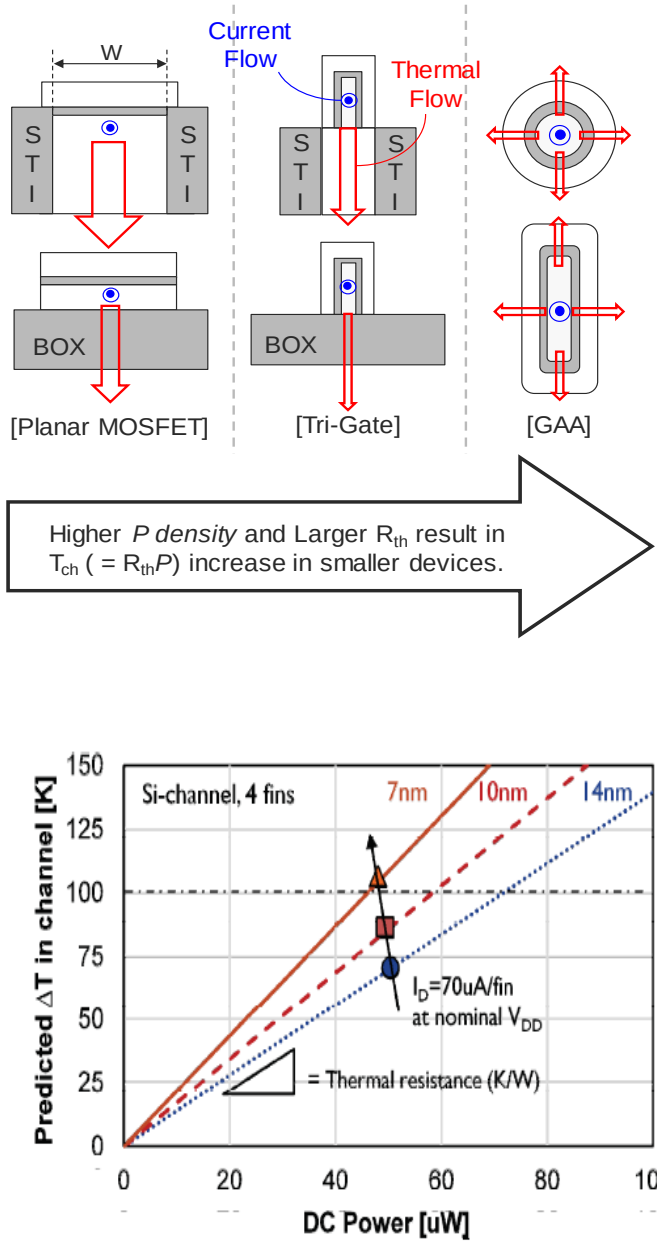


**Fig. 1.2. (a)** Current path and thermal flow according to each structure, **(b)** Predicted channel temperature rise of Si bulk FinFETs (4 fins) at given drive current. An increase in temperature of about 70℃ is expected for 14nm node and over 100℃ for 7nm node.

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# Chapter 2

# Thermal-Aware Shallow Trench Isolation Design Optimization for Minimizing $I_{off}$ in Various Sub-10-nm 3-D Transistor

## 2.1 Introduction

In this chapter, based on ITRS 2015, Bulk/SOI FinFETs that can be used up to 7-nm node and VFETs that appeared as new candidates in/under 5-nm node are made through Sentaurus, a TCAD simulator. we have studied the method of decreasing the maximum lattice temperature ($T_{L,max}$) through shallow trench isolation (STI) engineering considering $I_{OFF}$ in each structure and also the improvement of HCI/BTI lifetime based on temperature reduction by STI engineering solution in each structure.

## 2.2 Device Structure and Simulation Conditions

The Bulk/SOI FinFET and VFET structures used in this paper were made using Synopsys Sentaurus [14], a TCAD simulator. Detailed specifications of structures refer to

the values of 5-/7-nm node presented in ITRS [15]. Fig. 2.1 shows the entire structure and cross-sectional views of the FinFET. As shown in Fig. 2.1 (a), there is a heavily doped local doping area under source (S)/drain (D) region to improve the $I_{OFF}$ characteristic in the bulk FinFET. The shape of S/D bulk is made considering that the growth rate varies depending on the lattice direction when growing epitaxially. Fig. 2.1 (b) shows the structure of the SOI FinFET. SOI FinFET is all the same except that the STI-all-around region of the Bulk FinFET is replaced with an insulator. The following is an introduction to the structure of a VFET. Fig. 2.2 shows the entire structure and cross-sectional views of the VFET. Fig. 2.2 (a) shows the entire structure of a VFET and includes back end of line (BEOL) and large substrate, just like the entire structure of a FinFET. As mentioned in Section introduction, the channel is vertically oriented and the S/D is made up and down the channel. The shape of the S/D is made into a rectangular shape different from that of the FinFET by referring to the papers [6]–[9] dealing with the fabrication of the VFET. In addition, to improve the performance ($I_{ON}$) of the nanowire channel VFET, a VFET with a sheet-shaped channel can be seen in the cross section. The structure specification such as channel thickness ($T_{fin}$/$T_{ch}$), effective oxide thickness, STI/BOX thickness (Tsti/Tbox), doping concentration, and thermal conductivity of each region is shown in Table 2.1. TCAD tool has a function to tune the thermal conductivity and dielectric constant value of material inside. The thermal conductivity and dielectric constant value are added to the parameter part to account for the difference of the STI material. Values for each substance are obtained through various documents [10]–[12].

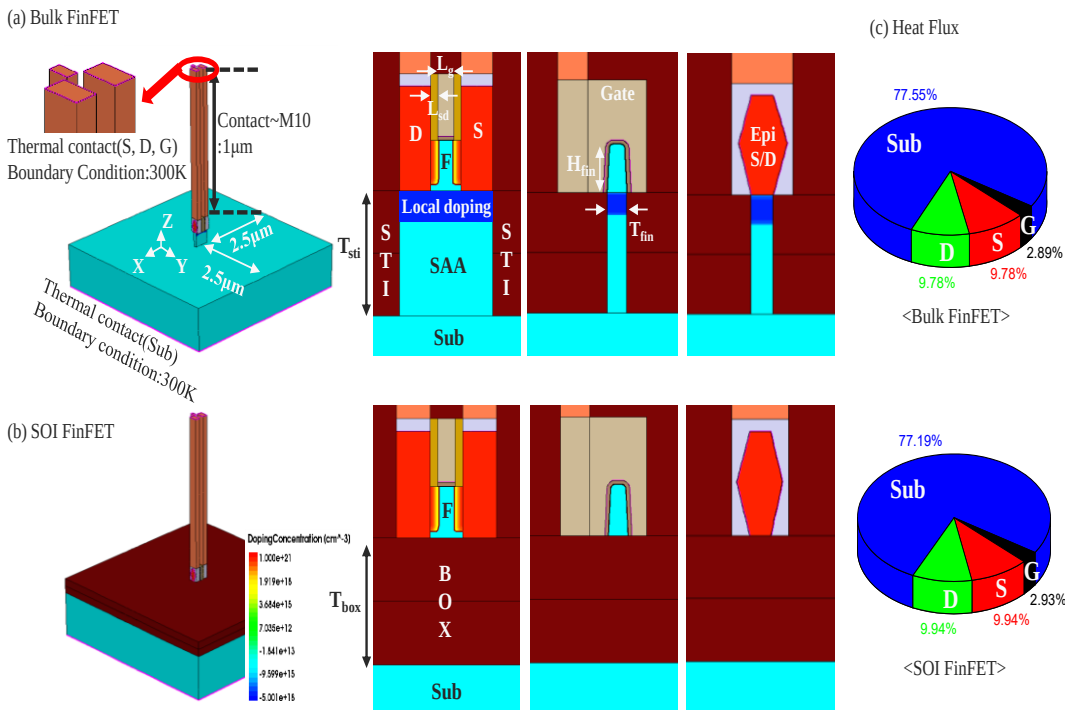



**Fig. 2.1** Entire structure and cross sectional views (a)Bulk and (b)SOI FinFETs. In the Bulk FinFETs, there is a heavily doped local doping area in order to improve characteristics of Ioff. Thermal contacts are set on the Source, Drain, Gate, and Substrate, and thermal boundary conditions (temperature: 300K) are set for each contact. In case of Back End of Line (BEOL), it is made up to 1 m (M10 layer height) refer to specification of Table 2.2. (c) For Bulk/SOI FinFET, the heat dissipation from hot spot to thermal contacts is shown by heat flux.

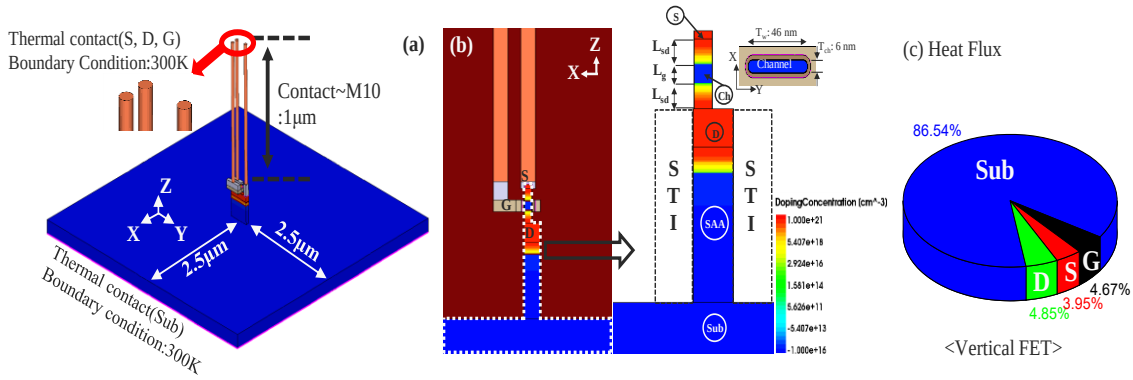



**Fig. 2.2** (a) Entire structure of VFET and (b) cross sectional views of VFET. In the Vertical FETs, the channel is a vertically oriented structure. Thermal contacts, thermal boundary conditions and BEOL specification is set the same as those of the FinFET. (c) For VFET, the heat dissipation from hot spot to thermal contacts is shown by heat flux.

Table 2.1 Thermal and structural specifications.

| Category | | FinFET |
|---|---|---|
| $V_{DD}$ (V) | | 0.7 |
| EOT (nm) | | 0.7 |
| S/D Doping ($cm^{-3}$) | | 1 x $10^{21}$ |
| Channel Doping ($cm^{-3}$) | | 1 x $10^{16}$ |
| Local doping($cm^{-3}$) | | 5 x $10^{18}$ |
| $T_{fin}/L_g$ (nm) | | 7/14 |
| $H_{fin}/L_{sd}$ (nm) | | 40/6 |
| $T_{sti}/T_{box}$(nm) | | 100 |
| **Thermal Conductivity[Ref] (W/m/K)** | | |
| Si | Source/Drain [S, D] | 16 |
| | Fin [F] | 19 |
| | STI-all-around [SAA] | 18 |
| | Substrate [Sub] | 148 |

| Category | | VFET |
|---|---|---|
| $V_{DD}$ (V) | | 0.65 |
| EOT (nm) | | 0.7 |
| S/D Doping ($cm^{-3}$) | | 1 x $10^{21}$ |
| Channel Doping ($cm^{-3}$) | | 1 x $10^{16}$ |
| $T_{ch}$ (nm) | | 6 |
| $W_{fin}$ (nm) | | 46 |
| $L_g$ (nm) | | 12.2 |
| $L_{sd}$ (nm) | | 11.9 |
| **Thermal Conductivity [Ref] (W/m/K)** | | |
| Si | Source [S] | 3.8 |
| | Channel [Ch] | 8.9 |
| | Drain [D] | 5.6 |
| | STI-all-around [SAA] | 18 |
| | Substrate [Sub] | 148 |

It is underestimated to verify $T_{Lattice}$ by SHE of single device except BEOL structure. The reason for this is that in the case of modern devices, the BEOL forms up to the maximum M10 layer, which not only lengthens the path of heat dissipation to the BEOL but also the dielectric surrounding the metal line has a low thermal conductivity. In order to consider contributing the increase of $T_{Lattice}$ of BE-OL, the BEOL height is briefly calculated by referring to the announcements of companies and several papers [16], [17]. Table 2.2 shows the thickness of Via/Metal for each layer. It becomes approximately 1 μm when it is raised up to M10 layer. This height can also be seen in the entire structures of Fig.2.1 and 2.2.

Table 2.2 BEOL specifications.

| Category | Metal Thickness(nm) |
|---|---|
| W Contact/M0 | 27/38 |
| M1~M3 (1xPitch)<br>V0~V3 (1xPitch) | 20 |
| M4(1.4xPitch)<br>V4(1.4xPitch) | 28 |
| M5(2xPitch)<br>V5(2xPitch) | 40 |
| M6(3xPitch)<br>V6(3xPitch) | 60 |
| M7~M8(4xPitch)<br>V7~V8(4xPitch) | 80 |
| M9~M10(4xPitch)<br>V9~V10(4xPitch) | 80 |

Several factors have been taken into account for thermal analysis of the device. The thermal contact is set in the area where the heat is dissipated. In [18] and [19] dealing with SHE, source, drain, gate, and substrate are set to thermal contact. In addition, a boundary condition is required when calculating the temperature in the device, and accordingly, we have specified room temperature (300 K) for the thermal contacts. We include equantumPotential and emobility (thinlayer) in the physics to account for the quantum effect. In order to improve the electrical accuracy, the calibration was carried out in the same way as in [23]. Finally, in the case of the hydrodynamic model, the change of device temperature is directly taken into account in the current and can also improve the accuracy of the simulation. For this reason, the hydrodynamic model is used for the overall SHE analysis.

## 2.3 Results and Discussion

Depending on the material filling the STI, the interface trap density ($D_{it}$) of the Si/oxide interface is different. In the case of STI filled with a commonly used $SiO_2$, $D_{it}$ has a $2 \times 10^{11}$ [$cm^{-2} \cdot eV^{-1}$], whereas in the case of STI filled with Al2O3, Dit increases to $3 \times 10^{13}$ [$cm^{-2} \cdot eV^{-1}$] referring to the paper [20]. Fig. 2.3 shows the $I_d$–$V_g$ curves that reflect $D_{it}$ according to STI materials in sub-10-nm devices. Depending on the material constituting the STI, it can be seen that the off regions are different. There is little difference in the on regions, which can be explained by the fact that the capacitance according to the material in Fig. 2.4 has almost the same. The SHE analysis of this paper proceeded at the current level in Fig. 2.3.

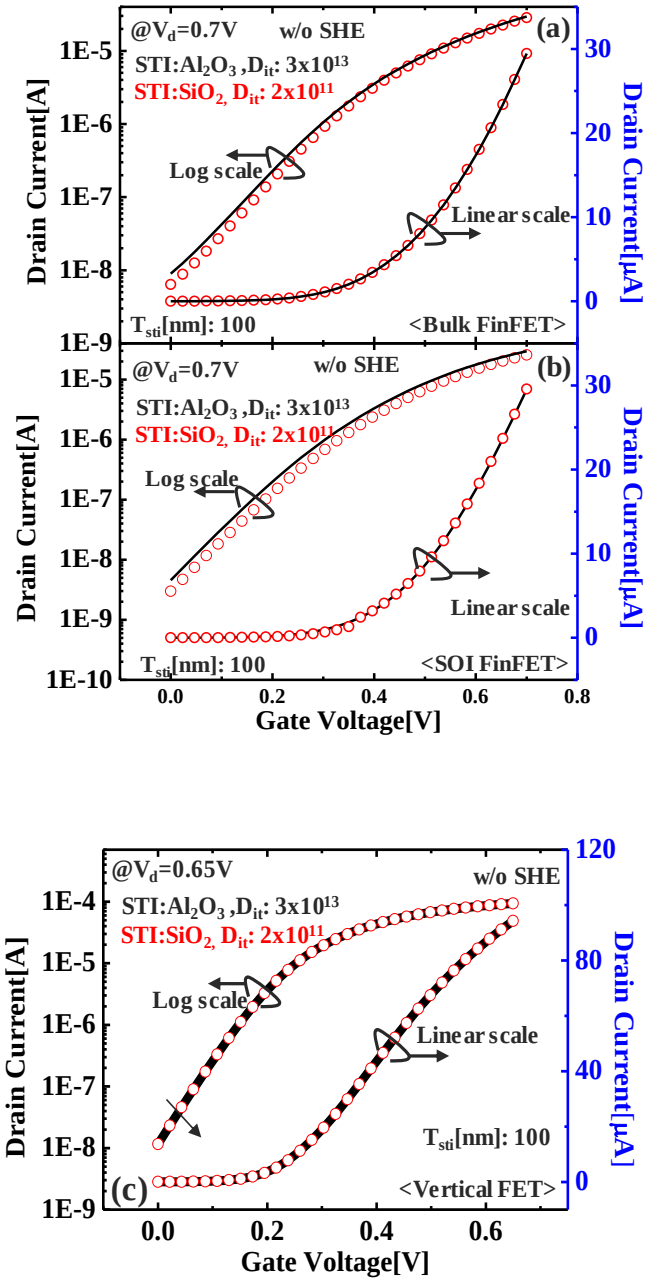



Fig. 2.3 (a) Fig. 3. $I_d$-$V_g$ curves according to STI materials ($SiO_2$/$Al_2O_3$). (a) Bulk FinFET (b) SOI FinFET (c) VFET.

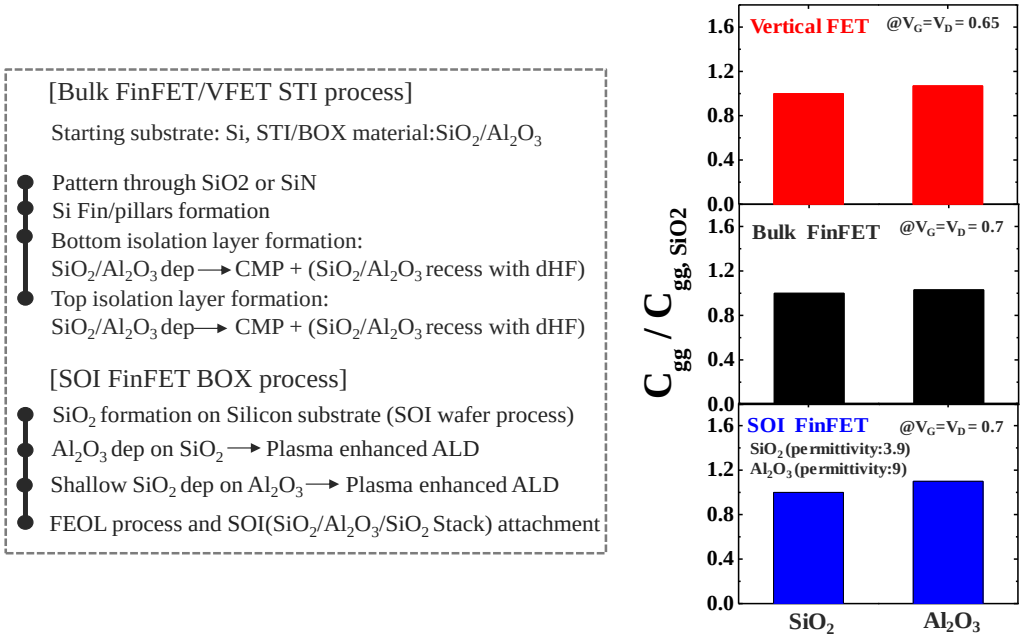



Fig. 2.4 (a) Schematics of the STI process flow in sub -10nm devices and comparison of capacitance according to STI material.

Fig. 2.5 shows a detailed analysis of the OFF current ($I_{OFF}$, condition, $V_g$ = 0 V, $V_d$ = $V_{DD}$) characteristics reflecting the difference in $D_{it}$ according to the STI material. As shown in Fig. 2.5 (a), in the Bulk FinFET, not only $I_{OFF}$ changes according to the STI thickness but also the STI made of $Al_2O_3$ having a higher $D_{it}$ than $SiO_2$ has a larger $I_{OFF}$ value. In addition, the $I_{OFF}$ tends to increase sharply as the thickness of the STI becomes less than 40 nm. As shown in Fig. 2.5 (b), there is no $I_{OFF}$ tendency depending on the STI thickness because the bottom leakage path is blocked by the BOX and only the $I_{OFF}$ difference due to $D_{it}$ changes according to BOX material. As in the case of Bulk FinFET, STI made of $Al_2O_3$ has a larger $I_{OFF}$ value. Finally, in the case of VFETs, it can be confirmed that there is no $I_{OFF}$ tendency depending on the STI material and thickness. As mentioned in [12],

the current direction of the VFET is different from that of the Lateral FET, and therefore, the $I_{OFF}$ characteristics are not affected by the STI specification and properties in the VFET.

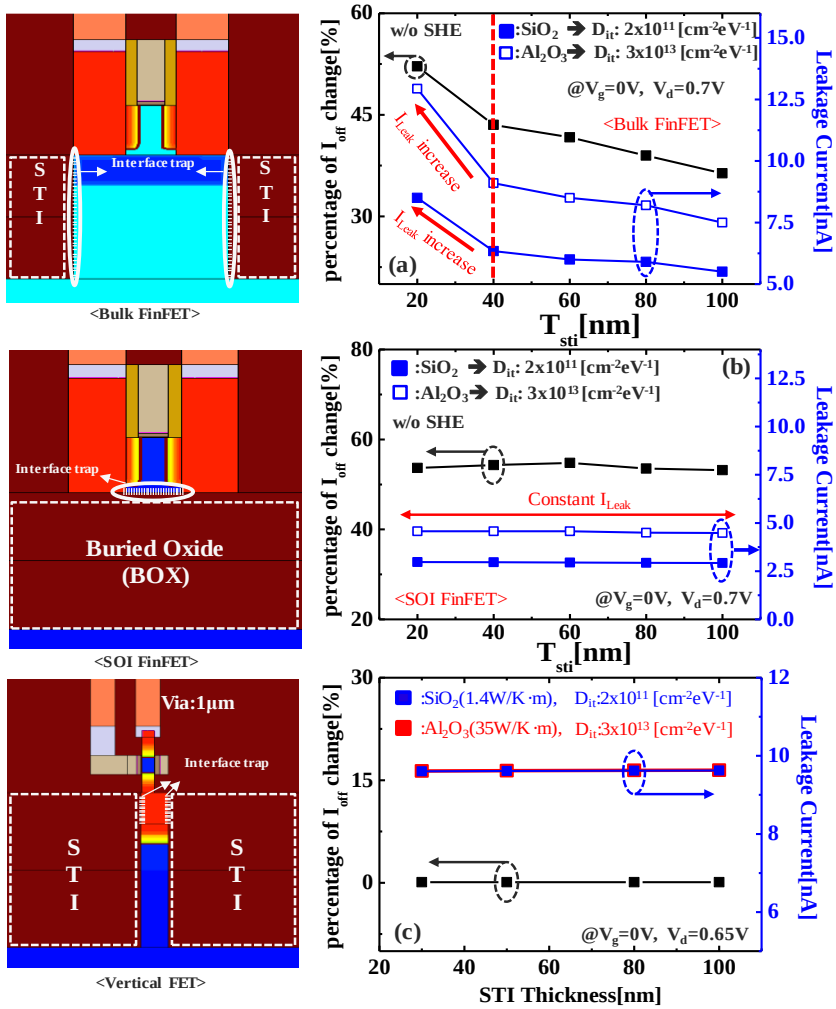



Fig. 2.5 $I_{off}$ characteristics according to STI specification and properties. (a)Bulk FinFET, (b)SOI FinFET and (c)VFET. The Bulk FinFET is all affected by specification and properties of the STI and the SOI FinFET is only affected by the properties of the STI. VFET is not affected by STI.

In this section, we analyzed the thermal characteristics according to the difference in thermal conductivity (k) between $Al_2O_3$ (k: 35 W $\cdot m^{-1} \cdot K^{-1}$) and $SiO_2$(k: 1. 4 W$\cdot m^{-1} \cdot K^{-1}$) used in STI, and then analyzed the SHE relaxation in each device through STI composition considering $I_{OFF}$. $SiO_2/Al_2O_3$ stack are widely used in the semiconductor industry from the gate-stack of logic device to the oxide–nitride–oxide layer of NAND Flash [24]–[26]. Nevertheless, our group has again analyzed whether the $SiO_2/Al_2O_3$ interfacial characteristics ($D_{it}$: 1e13–1e14 [24]) are causing device performance problems. As shown in the bottom left of Fig. 2.6 (b), there was no performance ($I_{OFF}$) change. Fig. 2.6 also shows the thermal characteristics, which show the max lattice temperature ($T_{L,max}$) according to the STI composition [21]. Bulk/SOI FinFET and VFET both show the same temperature tendency according to the STI composition. In the case of #3, $T_{L,max}$ is decreased much compared to #1, because the $Al_2O_3$ with high thermal conductivity efficiently dissipates heat to the substrate. In addition, the difference between #2 and #4 is that the material order in the composition is changed. The reason why the $T_{L,max}$ of #4 is lower than that of #2 is that the heat flux to the STI region becomes larger as the material having a higher thermal conductivity is located near the hotspot as shown in the top left of Fig. 2.6 (b).

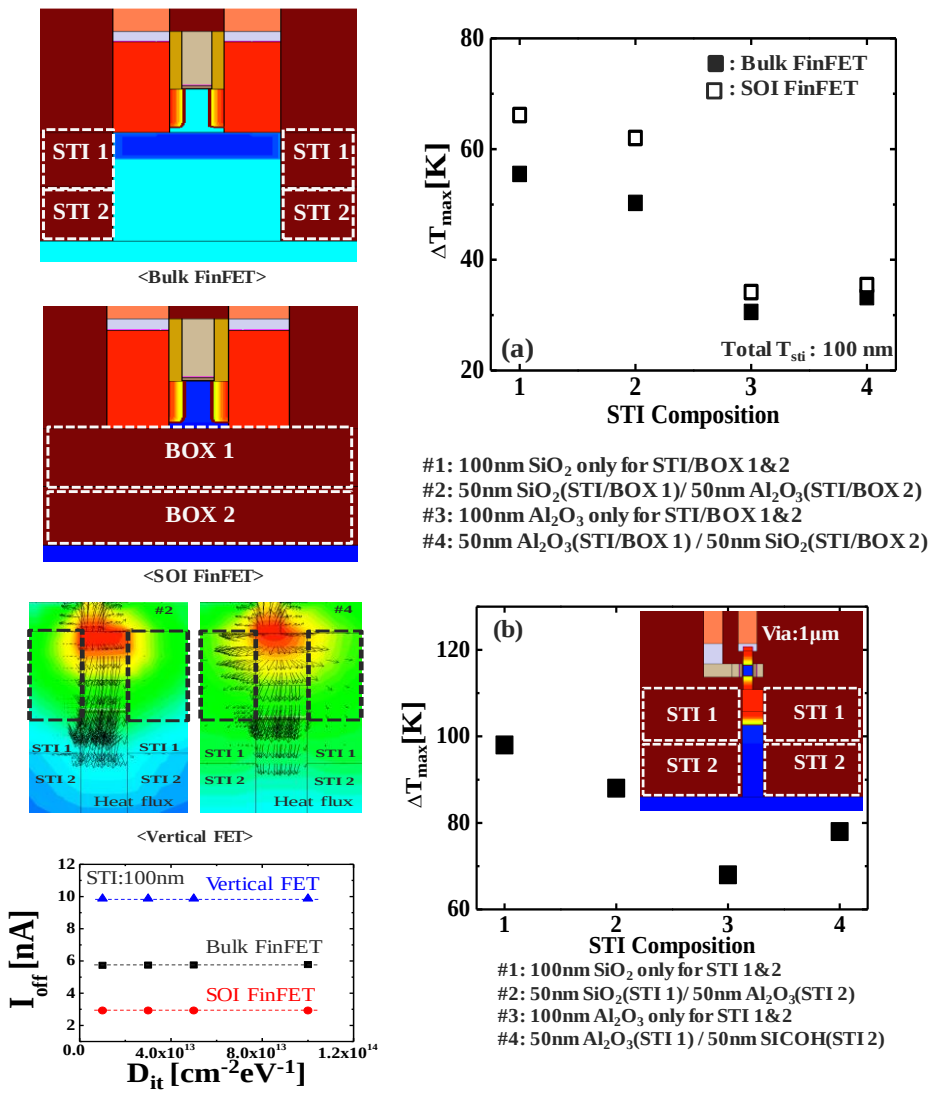



Fig. 2.6 $T_{L,max}$ change according to STI composition. (a) Bulk/SOI FinFET and (b) VFET. As the material with high thermal conductivity properties is located near the hot spot, $T_{L,max}$ decreases.

Now, mitigation of SHE through the STI composition considering $I_{OFF}$ in each device is discussed. As shown in Fig. 2.7 (a), comparing the $T_{L,max}$ for the three cases in a Bulk FinFET. The first is the case where the STI is made only with $SiO_2$. The second is the case where the upper part (20 nm) of the STI is made of $SiO_2$ and the lower part (80 nm) is made of $Al_2O_3$ based on the $I_{OFF}$ analysis of the Bulk FinFET in the front part. The third case is that the entire STI is made of $Al_2O_3$. When the STI thickness is 100 nm, TL,max is reduced by 13 K in $SiO_2/Al_2O_3$ composition compared to using only $SiO_2$. When STI is made entirely of $Al_2O_3$, $T_{L,max}$ decrease to 25 K. Fig. 2.7 (b) shows that $R_{th}$ is reduced by 20% in the case of $SiO_2/Al_2O_3$ composition and about 42% in the case of only $Al_2O_3$. Comprehensively, $I_{OFF}$ and $I_{ON}$ degradation rate according to $T_{L,max}$ for $SiO_2/Al_2O_3$ composition and only $Al_2O_3$ are compared with ordinary case. As can be seen in Fig. 2.7(c), when STI only made of $Al_2O_3$ with interfacial properties, $I_{OFF}$ is increased by 36%, but the $I_{ON}$ degradation rate is reduced from 7.8% to 3% compared to ordinary case. In the case of $SiO_2/Al_2O_3$ composition considering $I_{OFF}$ characteristic, the $I_{OFF}$ is slightly increased to 2.4%, and the $I_{ON}$ degradation rate is reduced from 7.8% to about 5% compared to ordinary case. Therefore, in the case of a high-performance (HP) device which focuses on the $I_{ON}$ characteristics rather than $I_{OFF}$, it is expected that using only $Al_2O_3$ will minimize the $I_{ON}$ degradation due to the SHE. Next, in the case of a low-power (LP) device in which the $I_{OFF}$ characteristics is important, it is expected that the $SiO_2/Al_2O_3$ composition can be used to maintain $I_{OFF}$ while improving the $I_{ON}$ characteristic.

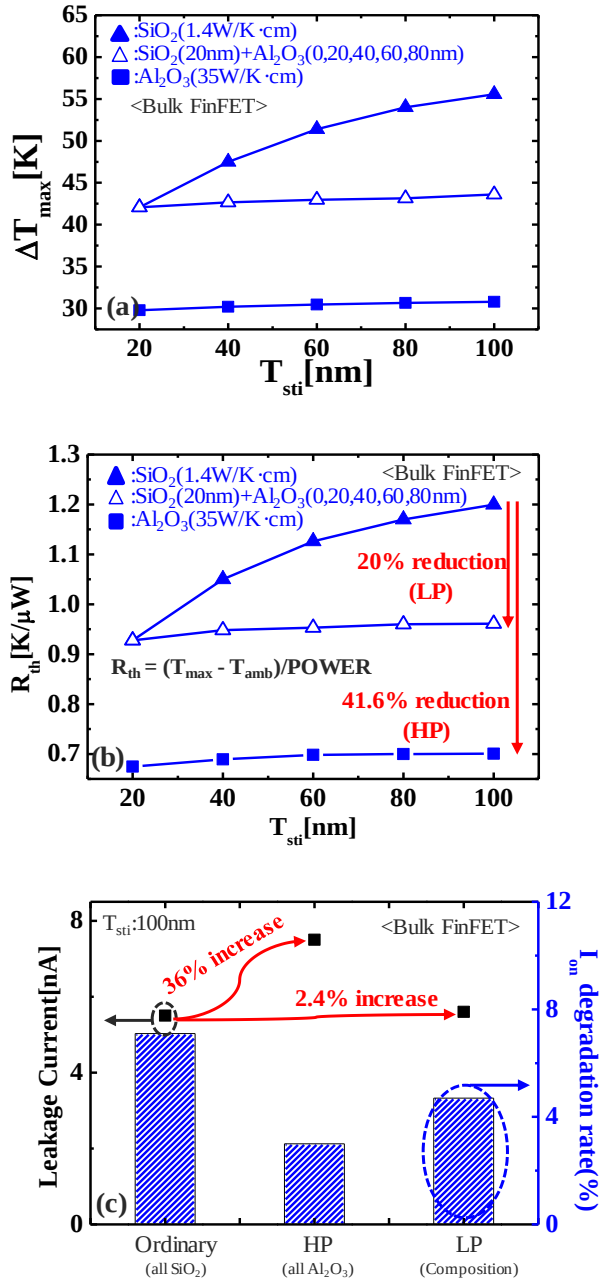
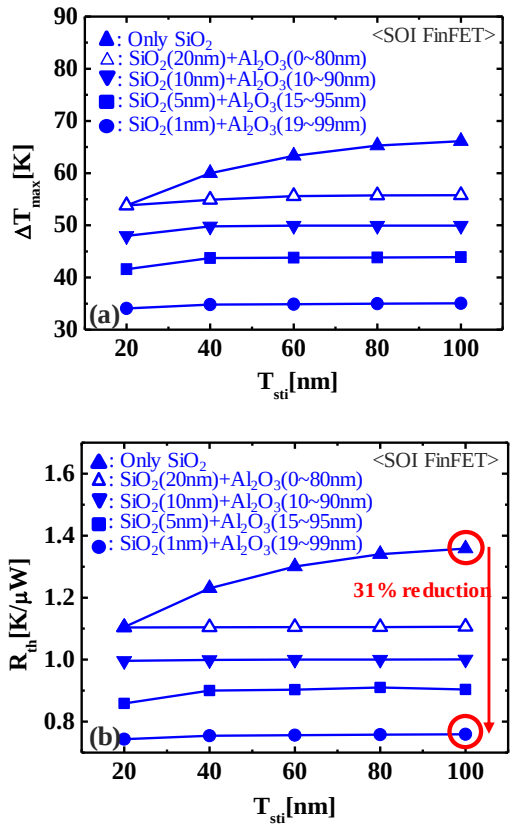



Fig. 2.7 SHE analysis and mitigation through detailed STI composition considering $I_{off}$ in Bulk FinFET. (a) $T_{L,max}$ change, (b) $R_{th}$ change and (c) $I_{on}$ degradation rate due to $T_{L,max}$ change and leakage current ($I_{off}$) change according to STI composition.

In the case of SOI FinFET, $I_{OFF}$ changed only by the number of $D_{it}$ at the BOX/Si interface. Therefore, the analysis is carried out by making the upper part of the BOX with $SiO_2$ and the lower part with $Al_2O_3$. As can be seen in Fig. 2.8 (a), when 1 nm of thin $SiO_2$ is laid on the interface and the rest (99 nm) is made of $Al_2O_3$, $T_{L,max}$ is reduced by about 32 K compared to all $SiO_2$. Similarly, Fig. 2.8 (b) shows that $R_{th}$ is reduced by 31%. Fig. 2.8 (c) shows that the BOX made of all $Al_2O_3$ improves the temperature characteristics and hence the $I_{ON}$ degradation rate is decreased, but $I_{OFF}$ is increased by 53.5% compared to all $SiO_2$. On the other hand, when the BOX is composed of 1 nm (at interface) $SiO_2$ and 99 nm (rest) $Al_2O_3$, $I_{OFF}$ can be kept at almost the same as that of all $SiO_2$ while keeping $I_{ON}$ as good as all $Al_2O_3$.



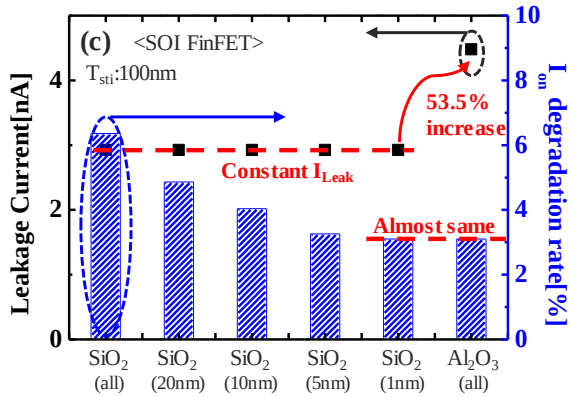



Fig. 2.8 SHE analysis and mitigation through detailed STI composition considering $I_{off}$ in SOI FinFET. (a) $T_{L,max}$ change, (b) $R_{th}$ change and (c) $I_{on}$ degradation rate due to $T_{L,max}$ change and leakage current ($I_{off}$) change according to STI composition.

In the case of VFET, there is no $I_{OFF}$ change depending on the thickness and kind of material of STI due to the nature of the structure. Fig. 2.9(a) shows $T_{L,max}$ depending on the STI thickness and the material constituting the STI. In VFET, it can be seen that $T_{L,max}$ is reduced by 30 K compared to all $SiO_2$ (100 nm) when STI is made with all $Al_2O_3$ (100 nm). In addition, since the thickness of STI does not affect $I_{OFF}$, if STI is made of $Al_2O_3$ with a thickness of 30 nm which can isolate drain region (20 nm) of VFET, it is possible to reduce $T_{L,max}$ by 42 K compared to all $SiO_2$(100 nm). Fig. 2.9(b) shows the change in $R_{th}$. When the STI is made of all $Al_2O_3$ (30 nm), it can be seen that $R_{th}$ is reduced up to 19% compared to all $SiO_2$(100 nm). As shown in Fig. 2.9(c), there is no change in $I_{OFF}$ depending on the material and thickness of STI. Therefore, when STI is made of all $Al_2O_3$(30nm), the $I_{ON}$ degradation rate is changed from 8% to 5%, while $I_{OFF}$ is kept equal to all $SiO_2$(100 nm).

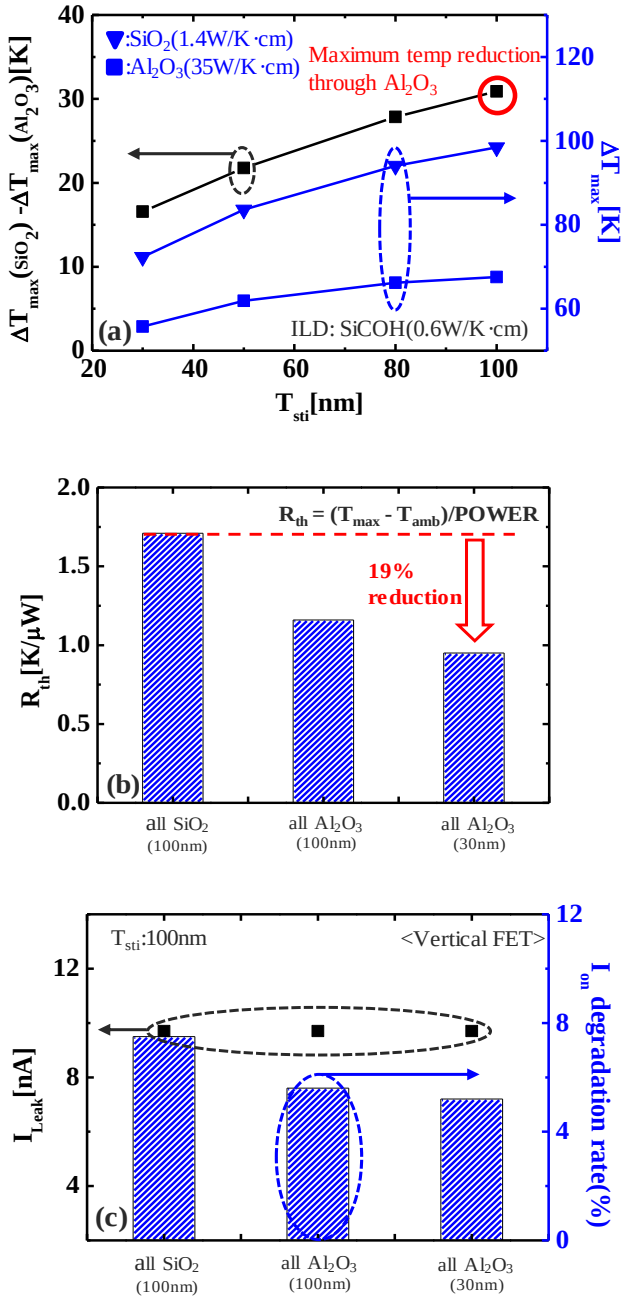



Fig. 2.9 SHE analysis and mitigation through detailed STI composition considering $I_{off}$ in VFET. (a) $T_{L,max}$ change, (b) $R_{th}$ change and (c) $I_{on}$ degradation rate due to $T_{L,max}$ change and leakage current ($I_{off}$) change according to STI composition.

Finally, to organize at a glance, we compiled the best case of Bulk/SOI FinFET and VFET by comparing standby power dissipation (SPD = $V_{dd} \cdot I_{OFF}$) and $T_{L,max}$ change according to STI composition. As can be seen in Fig. 2.10, in the case of Bulk FinFET, there are two best cases: HP can minimize $T_{L,max}$ while increasing SPD, and LP can lower $T_{L,max}$ a little while keeping the SPD almost the same. In the case of SOI FinFET and VFET, all devices have the best case to minimize $T_{L,max}$ while maintaining the same SPD, respectively

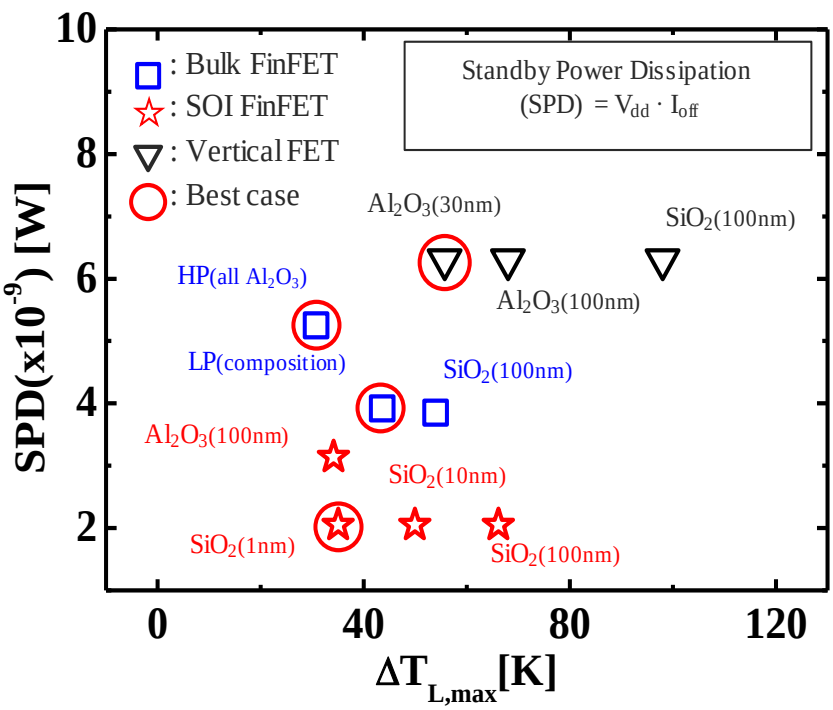
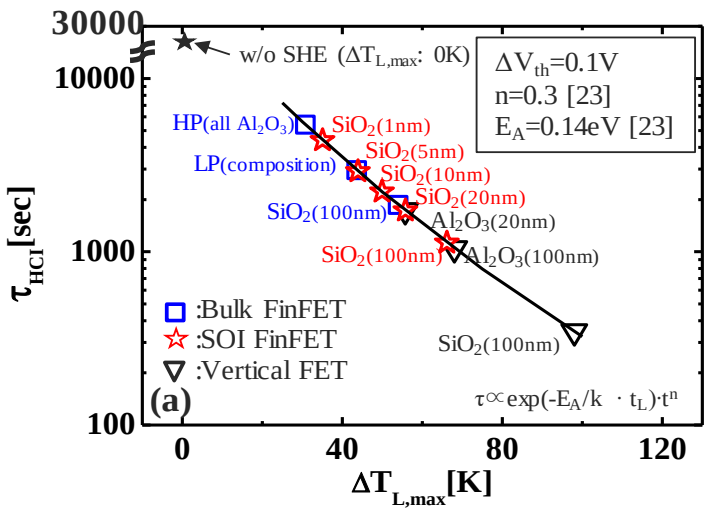



Fig. 2.10 Comparison of standby power dissipation and $T_{L,max}$ according to STI composition in Bulk/SOI FinFET and VFET.

As mentioned in Section 2.3, when optimization of STI composition is performed considering $I_{OFF}$ in Bulk/SOI FinFET and VFET, respectively, $T_{L,max}$ decreases compared to ordinary STI (only $SiO_2$). Therefore, in this section, we study the change of HCI/BTI lifetime of devices according to $T_{L,max}$ change. The HCI/BTI lifetime of devices can be predicted through (1) with $E_a$ and $n$ [22]. Lifetime is defined as the time to reach $\Delta V_{th} \sim 0.1$ V. We compare three lifetimes: $\tau_0$, assuming no temperature rise due to SHE, i.e., T = 300 K; $\tau_{ordinary}$, for STI made only of $SiO_2$; and $\tau$, for STI made with composition in each device

$$\Delta Vth \sim \exp(-E_A/k \cdot T_{L,max}) \times t^n. \quad (1)$$

Fig. 2. 11 (a) and (b) shows a comparison of HCI and BTI lifetime according to $T_{L,max}$ using (1). The black star point represents the HCI/BTI lifetime when $\Delta T_{L,max}$ is 0 K (i.e., without SHE). In addition, it is also confirmed that the lifetime is improved due to $\Delta T_{L,max}$ relaxation through STI engineering compared to the case of ordinary STI in Bulk/SOI FinFET and VFET.



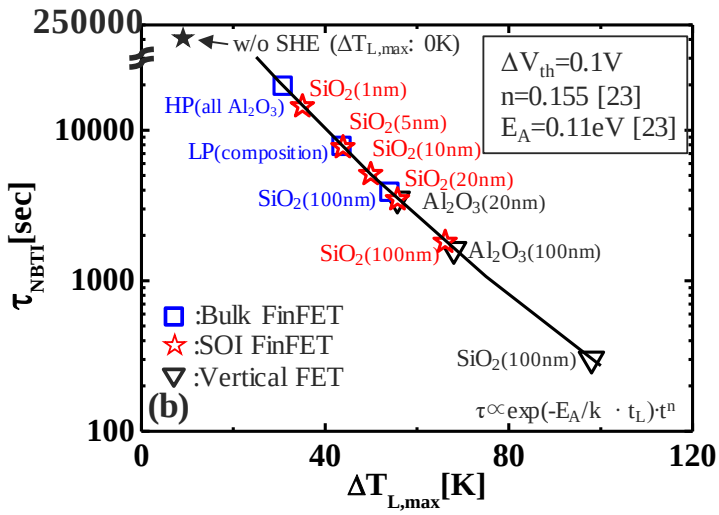



Fig. 2. 11. A comparison of (a) HCI, and (b) BTI, lifetime as a function of $\Delta T_{L,max}$. The $T_{L,max}$ is determined by SHE with various STI composition.

Fig. 2.12 shows the quantitative improvement of the HCI/BTI lifetime when STI engineering is applied compared to ordinary STI in each device. As shown in Fig. 2.12(a), in the case of Bulk FinFET, the HCI lifetime increases up to 3× and the BTI lifetime increases up to 5×. As shown in Fig. 2.12(b), when BOX is composed of $SiO_2$(1 nm) and $Al_2O_3$(99 nm), the HCI lifetime increases up to 4× and the BTI lifetime increase up to 12×. Finally, as shown in Fig. 2.12(c), when the STI is made only with $Al_2O_3$(30 nm), the HCI lifetime increases about 5× and the BTI lifetime increases about 11×. For all structures, the HCI/BTI lifetime can be significantly enhanced through STI engineering to improve thermal properties of devices and minimize $I_{OFF}$ degradation.

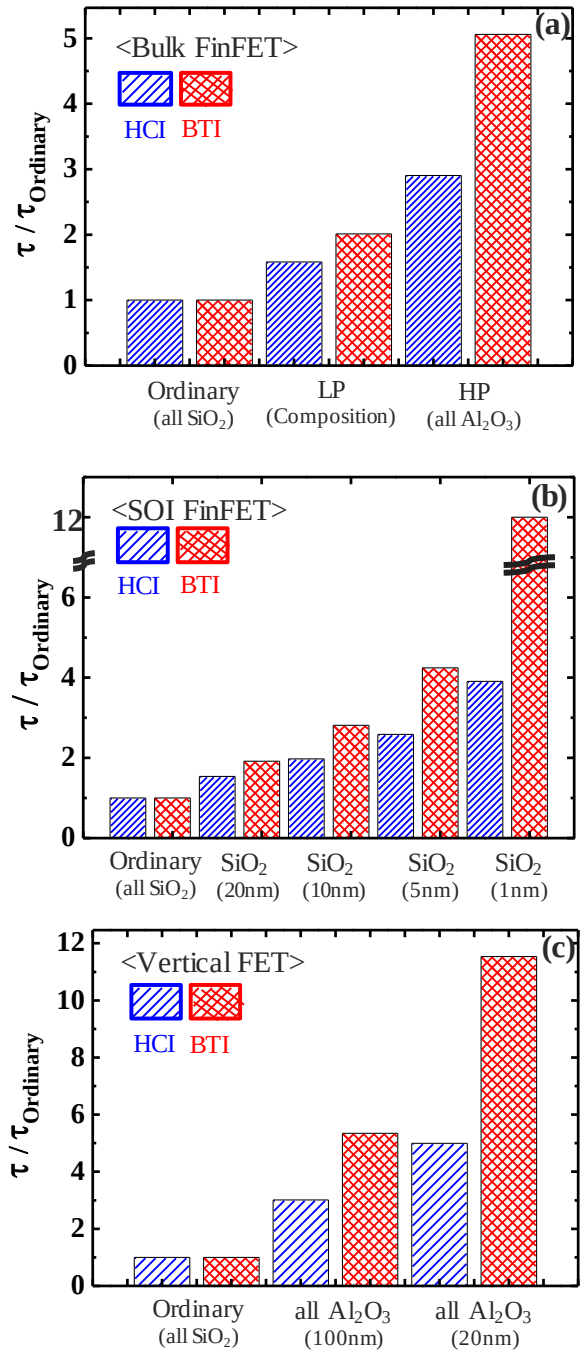



Fig. 2.12 Comparison of life time improvement in STI engineering case compared to Ordinary STI case. (a)Bulk FinFET, (b)SOI FinFET and (c) VFET.

## 2.4 Summary

In this chapter, we have analyzed SHEs in both FinFET (Bulk/SOI) and VFET, which are presented as potential candidates in 7- and 5-nm node, respectively. More specifically, we have studied the lattice temperature relaxation using high thermal conductivity STI materials while considering the $I_{OFF}$ characteristic due to the difference in $D_{it}$ according to STI materials. In the case of Bulk FinFET, using all $Al_2O_3$ compared to using all $SiO_2$, reduces $I_{ON}$ degradation rate from 7.8% to 3%, while $I_{OFF}$ increases by 36%. Therefore, using all $Al_2O_3$ for the STI material could be presented as an HP solution for Bulk FinFET. In the case of using $SiO_2$ for upper 20 nm and $Al_2O_3$ for lower 80 nm, $I_{ON}$ degradation rate reduces from 7.8% to 5%, while $I_{OFF}$ negligibly increases by 2.4%. Therefore, using $SiO_2$ for upper 20 nm and $Al_2O_3$ for lower 80 nm could be presented as LP solution for Bulk FinFET. In the case of SOI FinFET, when using all $Al_2O_3$ instead of all $SiO_2$, $I_{ON}$ degradation rate reduces from 7% to 3% but $I_{OFF}$ increases by 53.5%. However, when using our STI design of $SiO_2$ for upper 1 nm and $Al_2O_3$ for lower 99 nm, $I_{ON}$ characteristic is kept similar to that of all $Al_2O_3$, while keeping the same $I_{OFF}$ value as that of $SiO_2$. Finally, in the case of VFET, our investigation shows that using all 30-nm $Al_2O_3$ is optimal solution, compared to using 100 nm all $Al_2O_3$ or all $SiO_2$ for STI composition, because while $I_{OFF}$ is independent of STI material and thickness for VFET, $I_{ON}$ degradation reduces from 8% to 5% when using 30 nm all $Al_2O_3$ compared to others. We also estimated the improvement of HCI/BTI lifetime due to $T_{L,max}$ relaxation through STI engineering of each device. Depending on the device, the HCI lifetime can be increased from 1.5× to 5×, and BTI can be increased from 2× to 12×.

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# Chapter 3

# Analysis of Self Heating Effect in DC/AC Mode in Multi-channel GAA-Field Effect Transistor

## 3.1 Introduction

Continuous downscaling of semiconductor devices required the contacted gate pitch (CGP) to be reduced as well. This resulted in reducing the gate length. However, when the gate length decreases, it is difficult for transistors to scale down while maintaining the electrostatic characteristics. As a solution to this problem, 3-D devices such as a fin field effect transistors (FETs) or gate-all-around (GAA) nanowire-FETs have been introduced, which improve the controllability of a gate significantly [1]–[3]. By using such multi-gate FETs (MGFETs), downscaling of devices became feasible. However, in MGFETs, especially in nanowire-FETs, a gate dielectric with low thermal conductivity surrounds the channel [4], making it difficult to dissipate heat from the hot spot in the channel. In addition, due to the ultra-scale dimension, thermal conductivity is reduced, and then the

heat transfer efficiency of the nanowire-FET is also decreased [5]. As a result, the ON-current ($I_{on}$) decreases and causes reliability problems due to the increased temperature caused by self-heating effect (SHE). Therefore, thermal issues in nanowire device structures are expected to be continuously addressed in the future. In this chapter, analysis of SHE in a nanowire-FET is conducted in the dc/ac mode.

## 3.2 Multi-Channel Nanowire FET and Back End Of line

The multi-channel nanowire-FET structures used in this chapter were simulated using a Synopsys Sentaurus [6], a TCAD simulator. For detailed specifications of structures, refer to the values of the 5-/7-nm node presented in the International Technology Road Map for Semiconductor (ITRS) [7]. Fig. 3.1 shows the entire structures and cross-sectional views of a multi-channel nanowire-FET created by Synopsys simulation tools for the self-heating study. Fig. 3.1(a) shows a 3-D nanowire-FET structure. Fig. 3.1(b) and (c) shows the XZ plane of the 3-D nanowire-FET and the YZ plane of the channel region, respectively. Table 3.1 shows the device specifications with referenced to ITRS 2015. The supply voltage to the device is 0.75 V and the effective oxide thickness (EOT) is 1 nm. The source/drain doping concentration is $1 \times 10^{21}$ $cm^{-3}$, the channel doping is $10^{15}$ $cm^{-3}$, and the local doping for reducing the leakage current is $5 \times 10^{18}$ $cm^{-3}$. The channel thickness ($T_{ch}$) is 6 nm and the STI thickness for isolation is 100 nm. The lengths of the gate ($L_g$) and channel extensions ($L_{SD}$) are 10 and 5 nm, respectively. Fig. 3.1(a) also includes a back end of line (BEOL) metal; the height of the M8 layer is 680 nm and the height is calculated from [18, Table II] based on the short course data on IEDM (2016)

and various articles [10]–[13].

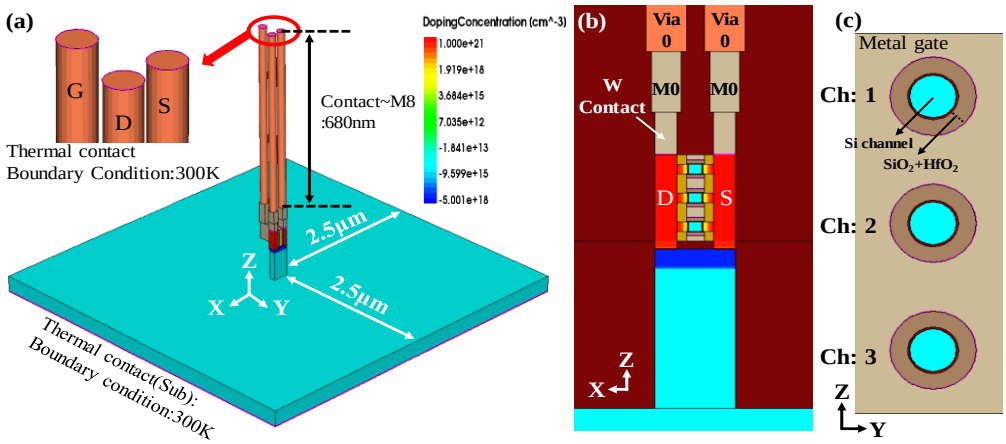



Fig. 3.1 (a) Three-dimensional nanowire FET structure with thermal contact, boundary condition and BEOL. (b) X-Z plane of three-dimensional nanowire FET. (c) Y-Z plane of mulita-channel region.

Table 3.1

Electrical / Thermal specification of Nanowire-FET

| Category | NWFET | Thermal Conductivity (W/m/K) | | |
|---|---|---|---|---|
| $V_{DD}$ (V) | 0.75 | | | |
| EOT (nm) | 1 | Si | ① Source/Drain | 7.9 |
| S/D Doping ($cm^{-3}$) | 1 x $10^{21}$ | | ② Channel | 8.9 |
| Channel Doping ($cm^{-3}$) | 1 x $10^{15}$ | | ③Local doping | 24.6 |
| Local Doping($cm^{-3}$) | 5 x $10^{18}$ | | ④STI-all-around | 25 |
| $T_{ch}$ (nm) | 6 | | ⑤ Substrate | 148 |
| $T_{STI}$ (nm) | 100 | | | |
| $L_g$ (nm) | 10 | | | |
| $L_{SD}$ (nm) | 5 | | | |

## 3.3 Work Flow and Calibration Process

Fig. 3.2(a) shows the total work flow in the study. The calibration of the nanoplate-FET is performed and then the channel width is reduced to convert to the nanowire structure. Finally, SHE analysis is performed on the nanowire-FET. Quantum corrections are conducted for I–V calibration under 3-D TCAD simulation provided by Synopsys [6]. We use the density gradient quantization model (quantumPotential) to consider the quantum effect and use the mobility model (thin layer/phumob/Enormal(lombardi)) to account for Coulomb scattering and interfacial surface calibration roughness scattering for accuracy. First, I–V simulations are performed with the quantum model and the gate work function (WF) and the saturation velocity are carefully adjusted to match the I–V characteristics with the measured data [24]. Second, the thermal conductivity, heat conduction paths, and thermal boundary condition (300 K) to each heat path are considered to reflect the thermal characteristics of the nanoplate-FET. Fig. 3.2(b) shows that our simulation result is well fit with the measured data of the three-channel nanoplate-FETs [24]. The calibrated TCAD models are used to predict the electro-thermal characteristics of the 5-nm node nanowire-FET.

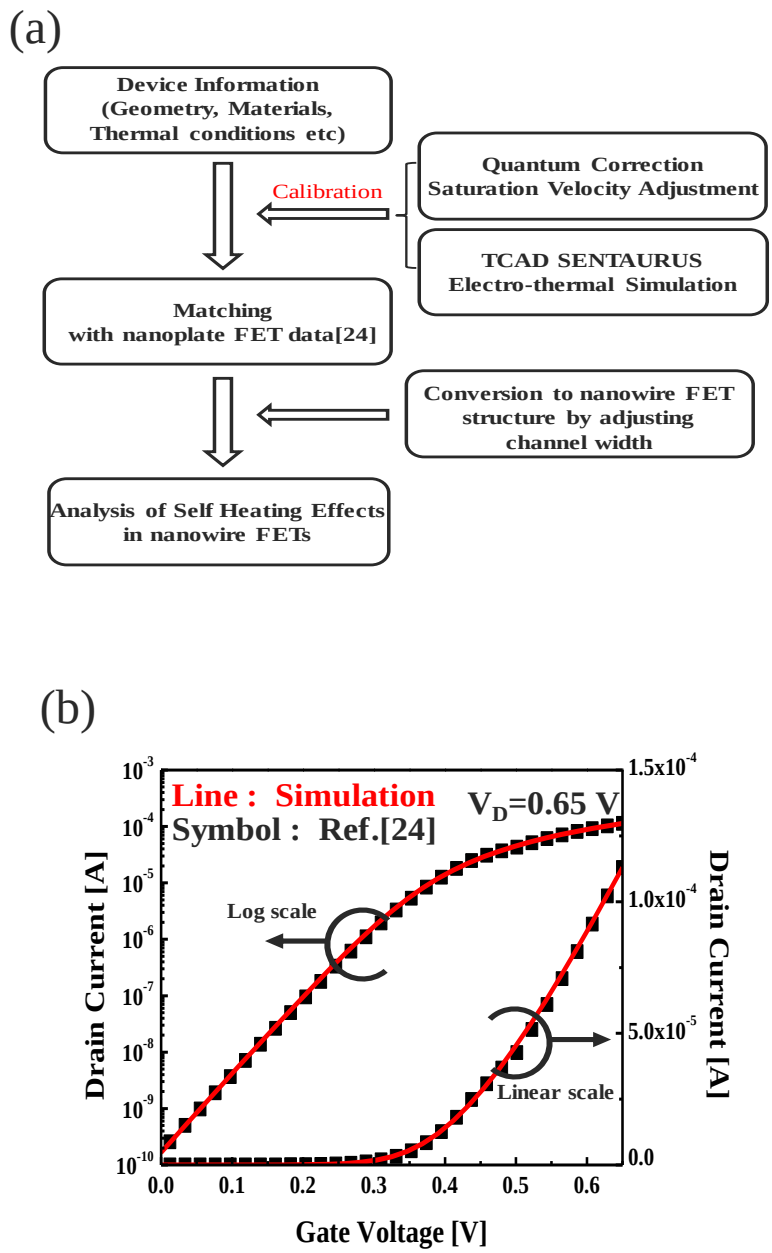



Fig. 3.2 (a) Overall work flow for analysis of SHE in nanowire-FET structures, (b) $I_D$-$V_G$ calibration results based on the nanosheet FET structure.

## 3.4 More Detailed Thermal Simulation of Nanowire-FET

Fig. 3.3(a) shows the device divided into five regions; Fig. 3.3(b) shows the thermal conductivity graph, which is calculated by considering the doping type, doping concentration, and region thickness from the previous articles [8], [14], [15] about modeling the thermal conductivity of silicon by phonon Boltzmann transport equations. Using this graph, we set the thermal conductivity value of the regions. Table 3.1 shows the thermal conductivity of each region. The thermal contact is set in the area where the heat is dissipated. With reference to the articles [9], [16]–[18] dealing with SHE, the source, drain, gate, and substrate are set to thermal contact. In addition, a boundary condition is required when calculating the temperature of the device, and accordingly, we have specified room temperature (300 K) for the thermal contacts. Finally, the thermodynamic model is used for the overall SHE analysis because in the case of thermodynamic model, the change in the device temperature is directly taken into account in the current [17].

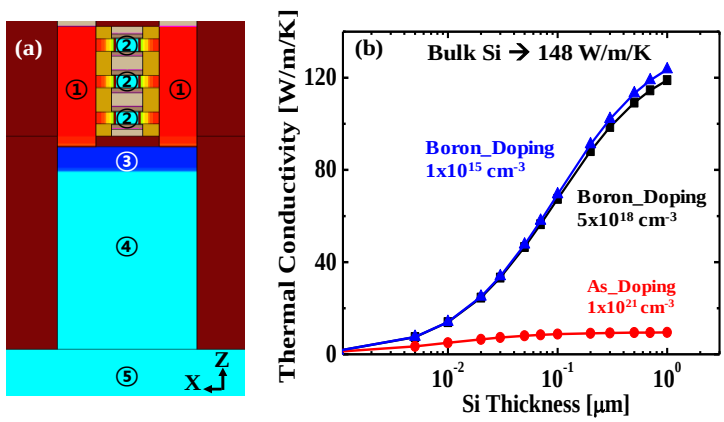



Fig. 3.3 (a) The five region for setting of thermal conductivity, (b) Thermal conductivity according to doping type, doping concentration, region thickness.

## 3.5 Performance Analysis by Number of Channels

First, we explain why the study is conducted using three-channel nanowire-FETs instead of a single-channel nanowire-FET. Nanowire-FETs with multiple channels (three channels) are very attractive compared to single-channel nanowire-FETs, because they exhibit a better performance [20]. Fig. 3.4(a) shows the structure created by simulation (Synopsys) for single-, two-, and three-channel nanowire-FETs. Fig. 3.4(b) shows a comparison of the Ion and $I_{on}$ degradation rate for each channel number. As the number of channels increases from one to three, the Ion increases almost three times for the same CGP. The reason why the current does not increase linearly according to the number of channels is because the source and drain sheet resistances increase with the number of channels. Also, as the channel number increases, the $I_{on}$ degradation rate due to SHE increases. In other words, as the number of channels increases, the degradation due to SHE becomes worse. For this reason, SHE studies are conducted on three-channel nanowire-FETs rather than single-channel nanowire-FETs.

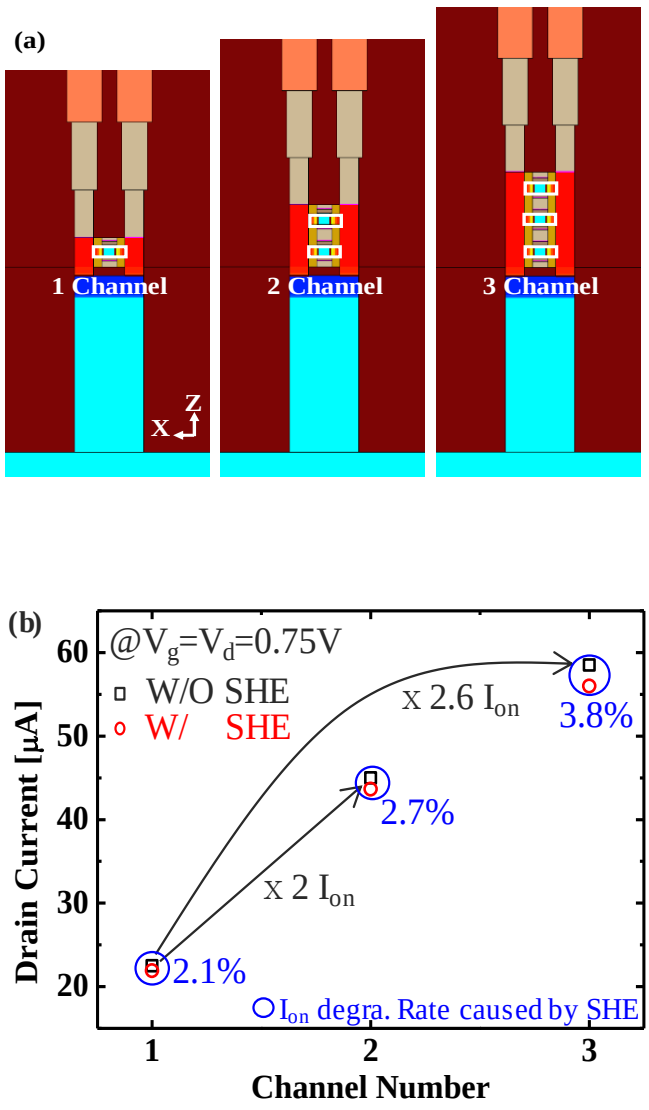



Fig. 3.4 (a) Nanowire-FET structures from one channel to three channels. (b) The comparison of $I_{on}$ according to channel number.

## 3.6 DC Characteristic of SHE in Three Channel Nanowire-FETs

Next, the analysis of dc characteristics of SHE in a three-channel nanowire-FET is conducted. Fig. 3.5(a) shows the $I_d$ –$V_g$ curve when $V_d$ is 0.75 V, the $I_{on}$ degradation rate by SHE, and the percentage of heat flux to the heat paths at $V_d$ = $V_g$ = 0.75 V. The $I_{on}$ reduces by approximately 3.8% caused by the decrease in electron mobility. Fig. 3.5(b) shows the maximum lattice temperature ($T_{max}$) of the three-channel nanowire-FET with the BEOL (M8 layer height :680 nm). $\Delta T_{max}$, which represents the $T_{max}$ −300 K (the boundary temperature), is approximately 65 K. Fig. 3.5(c) shows the $\Delta T_{max}$ curve according to the dc power. We can extract the thermal resistance ($R_{th}$) from the slope of the straight line. As shown in Fig. 3.5(c), it can be analyzed that how much the thermal properties of a three-channel nanowire-FET are worse compared to a single-channel nanowire-FET. $R_{th}$ is 3.34 K/μW for the single- channel and $R_{th}$ is 4.875 K/μW for three-channels. That is, the thermal characteristics are worsened when a three-channel nanowire-FET is used.

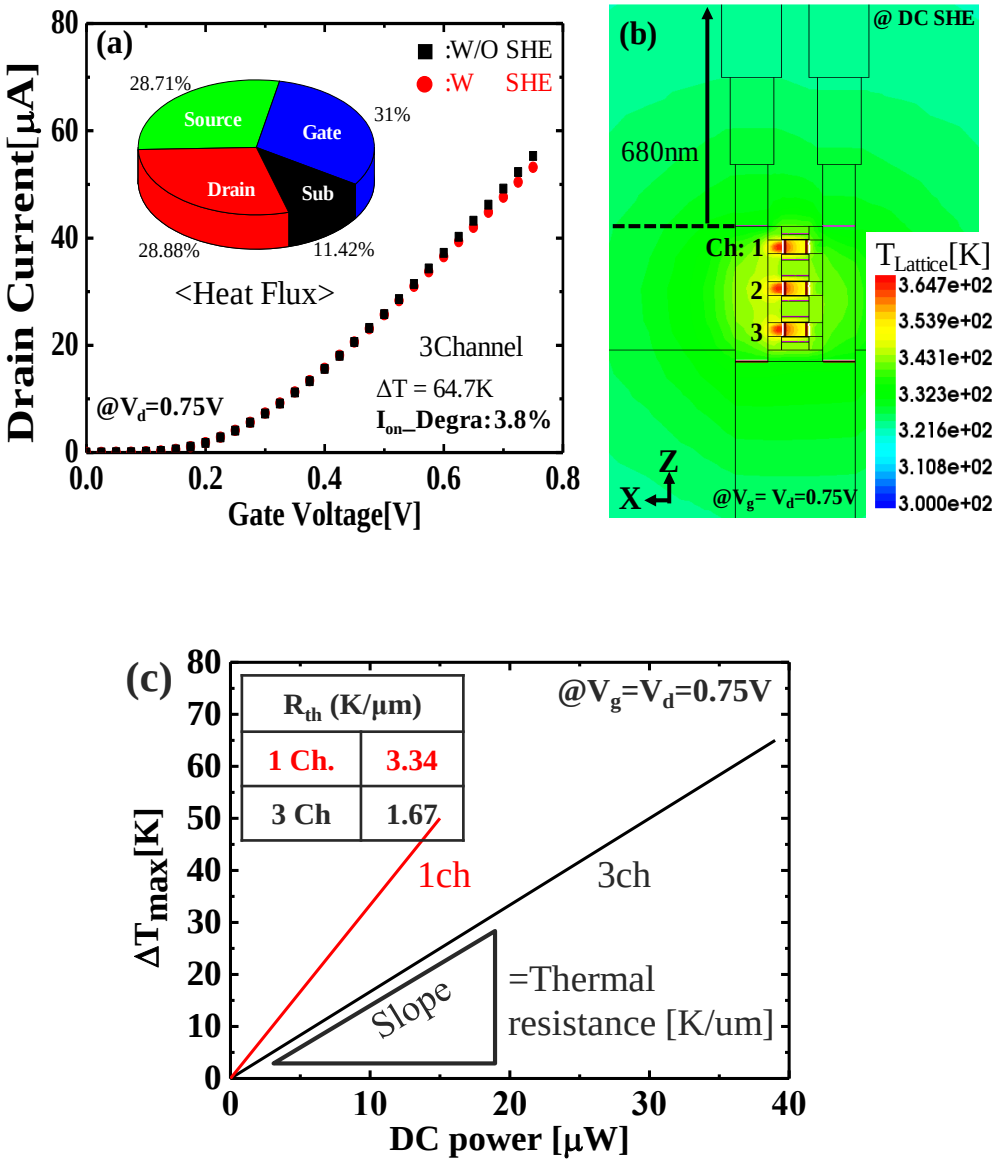
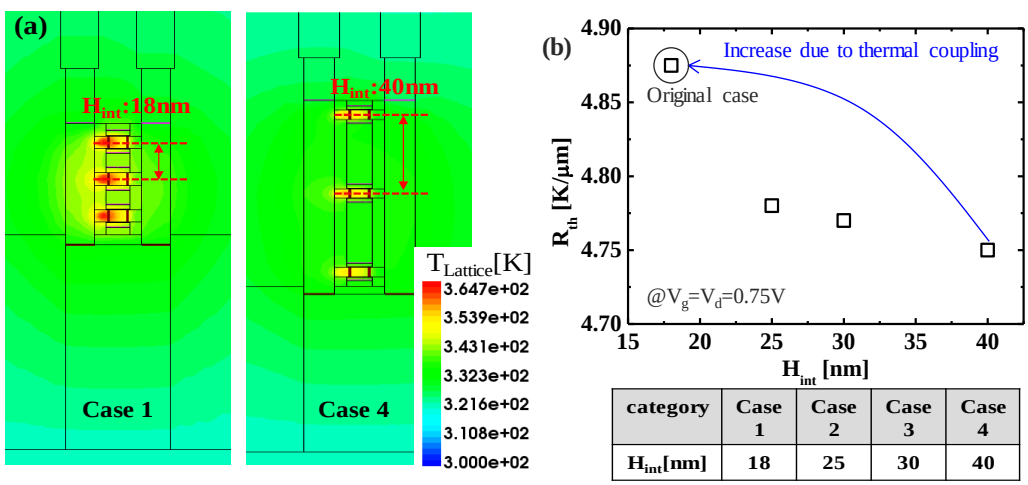



Fig. 3.5 (a) $I_d$-$V_g$ curve with heat flux to heat path and $I_{on}$ degradation rate by SHE, (b) Thermal distribution and max lattice temperature, (c) Normalized $R_{th}$ for single-channel and three-channel nanowire-FET.

Fig. 3.6 shows the reason why the thermal characteristics of a three-channel nanowire-FET are worse than that of a single channel nanowire-FET a. Fig. 3.6(a) shows the structures when the channel-to-channel distance ($H_{int}$) is 18 nm and $H_{int}$ is 40 nm, respectively. When $H_{int}$ is extended to 40 nm, $T_{max}$ decreases. As shown in Fig. 3.6(b), the effect of $H_{int}$ variation on the thermal properties of the three-channel nanowire-FET is analyzed through $R_{th}$. As the Hint becomes narrower, the heat generated per channel is further coupled with each other, adversely affecting heat dissipation, resulting in an increase of $R_{th}$. On the other hand, if $H_{int}$ is high, the thermal coupling between the heat generated in each channel is weakened, resulting in a decrease in $R_{th}$. Therefore, in a three-channel nanowire-FET, the thermal properties are degraded by the large $I_{on}$ and thermal coupling between channels.




| category | Case 1 | Case 2 | Case 3 | Case 4 |
|---|---|---|---|---|
| $H_{int}$[nm] | 18 | 25 | 30 | 40 |

Fig. 3.6 (a) The structures when *$H_{int}$* is 18 nm and 40 nm, (b) $R_{th}$ when *$H_{int}$* is from 8 nm to 40 nm.

## 3.7 AC Characteristic of SHE in Three Channel Nanowire-FETs

Finally, we analyze the SHE characteristics in the ac mode. Fig. 3.7(a) shows the method of setting the gate voltage to the ac mode. The pulse voltage consists of the rising time (RT), pulse time (PT), and off time (OT). One cycle consists of one PT and OT. The definition of the duty cycle is PT/OT. Fig. 3.7(b) shows the drain voltage. For pulse signals, the drain voltage must be in the dc mode to prevent any overshoot [21]. Therefore, the drain voltage was in the dc mode through ultrashort RT. In the ac mode, we can obtain various frequencies by adjusting the PT and the OT of the gate voltage. Before studying SHE according to the operating frequency, we proceeded to the study of $T_{Lattice}$ according to pulse heating time and cooling time. Cooling time is related to heat dissipation capacity ($1/R_{th}$) and thermal capacitance ($C_{th}$). $C_{th}$ is proportional to the total heat generated by the device [22].

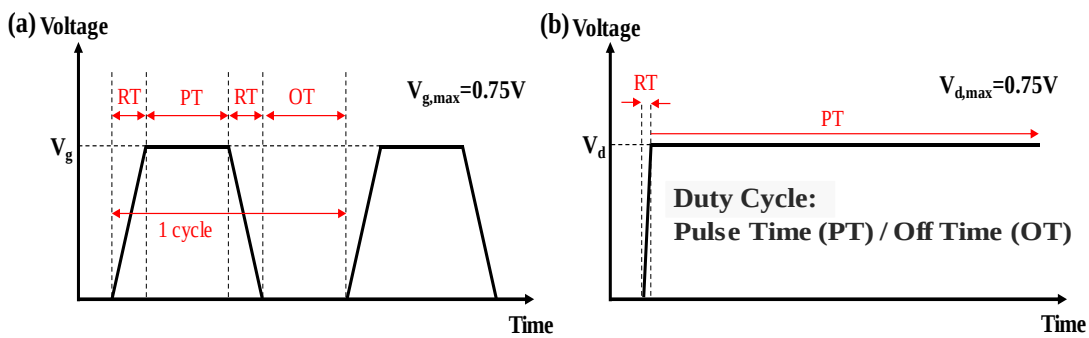



Fig. 3.7 (a) Gate voltage for AC mode including *RT* (Rising Time), *PT* (Pulse Time) and *OT* (Off Time), (b) DC Drain voltage using ultra-short *RT*.

Changing the heating time at the transient input (pulse voltage) makes the difference in total heat in the same device. Fig. 3.8(a) shows the temperature contour of the three-channel nanowire-FET for different heating times. Fig. 3.8(b) shows the difference in $T_{max}$ according to the heating time and shows each required cooling time accordingly. Here, the heating time is the same as the PT, which means the gate voltage is ON and the cooling time is the time required for $T_{Lattice}$ to return to 300 K after the gate pulse is off. In conclusion, the longer heating time result in a greater $T_{max}$ and accordingly, a longer cooling time, as shown in Fig. 3.8(b).

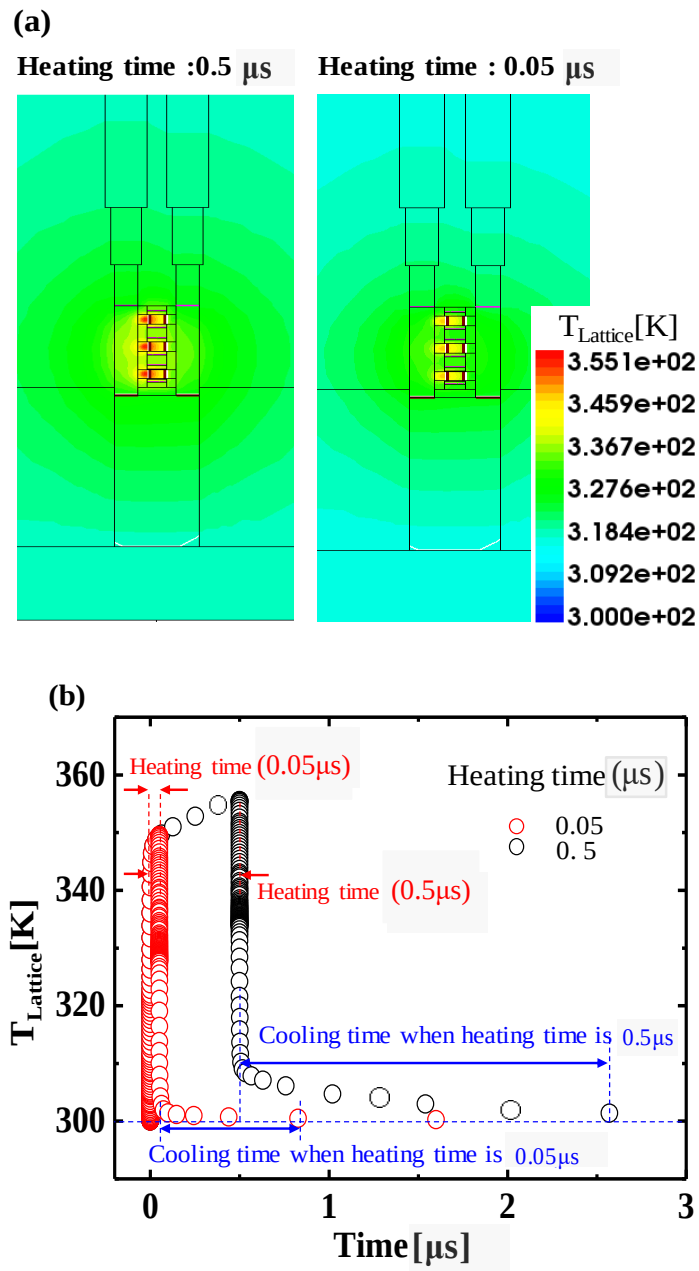



Fig. 3.8 (a) Temperature contour of the three-channel nanowire-FET for different heating times, (b) the transient data of device $T_{Lattice}$ and cooling time.

Fig. 3.9 shows the SHE of the device when the gate voltage is set to the ac mode. Fig. 3.9(a) shows the temperature characteristics of the lattice when the gate voltage is 50% duty cycle (that is, PT = OT) and the frequency is 100 kHz (that is, PT and OT are 5 μs each, and RT is set to about 5 ns, which is about 1/1000 times that of PT and OT). At 100 KHz, the temperature rises almost up to 365 K, which is the temperature rise in the dc operation. Fig. 3.9(b) shows the temperature characteristics of the lattice when the operating frequency is 4 GHz (that is, PT and OT are 0.25 ns each and RT is set to $0.25\times10^{-12}$ s) and the duty cycle is set to 50%. At 4 GHz, it is observed that $T_{max}$ saturates to 340 K, which is 25 K less than the temperature in the dc mode or at a low operating frequency. The reason why $T_{max}$ saturates at a low value when the frequency is high can be explained by the heating time and the cooling time illustrated above [Fig. 3.8(b)]. As the frequency increases, the heating time becomes shorter and the temperature rise becomes less. Also, since the cooling time is short, the temperature of the lattice cannot be reduced to 300 K and the residual temperature is generated. For this reason, at high operating frequencies, the temperature characteristic is as shown in Fig. 3.9(b). Fig. 3.9(c) shows the $\Delta T_{max}$ value according to various frequencies. As the operating frequency rises, it is observed that $\Delta T_{max}$ decreases and saturates to approximately 40 K. As the device becomes smaller, the operating frequency increases in an inverse proportion to $L_g$. When the device operates in the circuit level, it is driven in the ac mode, and the temperature increasing due to SHE is expected to be reduced compared to the dc mode.

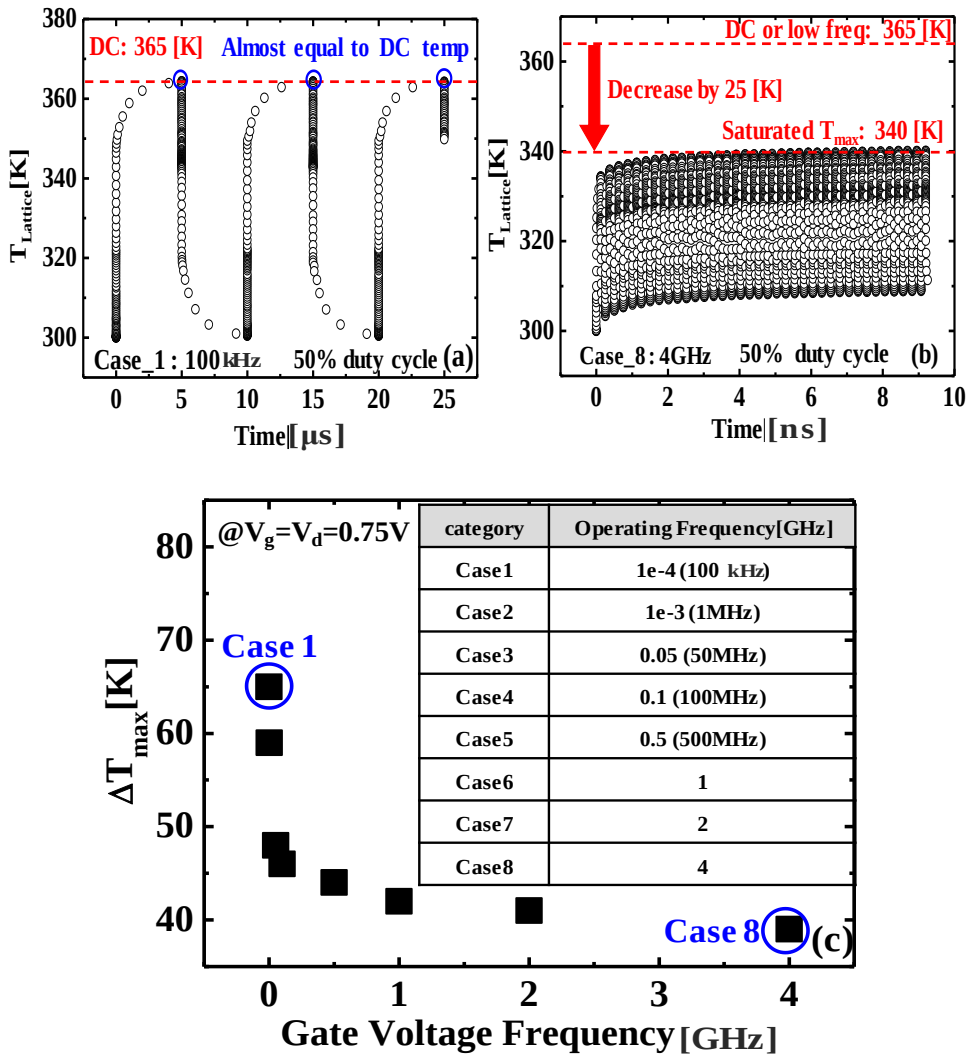



Fig. 3.9 (a) $T_{Lattice}$ at operating frequency of 100KHz, (b) $T_{Lattice}$ at operating frequency of 4GHz, (c) $\Delta T_{max}$ according to operating frequency.

Fig. 3.10(a) shows $I_{on}$ when the frequency is fixed at 1 GHz and the duty cycle is different. To analyze the effect of only the duty cycle on $I_{on}$, the results of Fig. 3.10(a) are carried out with the exception of SHE. It is confirmed that $I_{on}$ is constant according to the duty cycle and has the same $I_{on}$ as the dc condition illustrated above [Fig. 3.5(a)]. Fig. 3.10(b) shows $T_{Lattice}$ according to the duty cycle. When the duty cycle is 50%, it is the same as 1 GHz in Fig. 3.9(c). As shown in Fig. 3.10(b), as the duty cycle increases, the $T_{Lattice}$ increases. This is because as the duty cycle increases, the heating time increases and the cooling time decreases. Fig. 3.10(c) shows $\Delta T_{max}$ according to the duty cycle of the gate voltage. Similar to the results of Fig. 3.10(b), $\Delta T_{max}$ increases as the duty cycle increases. Therefore, if the duty cycle is reduced at the same operating frequency, the $\Delta T_{max}$ decreases without affecting the $I_{on}$ characteristics, so the SHE-induced temperature rise will be alleviated if the duty cycle of the gate voltage is reduced. As a result, it is expected that the Ion degradation rate will be reduced and the reliability problem due to heat will be reduced.

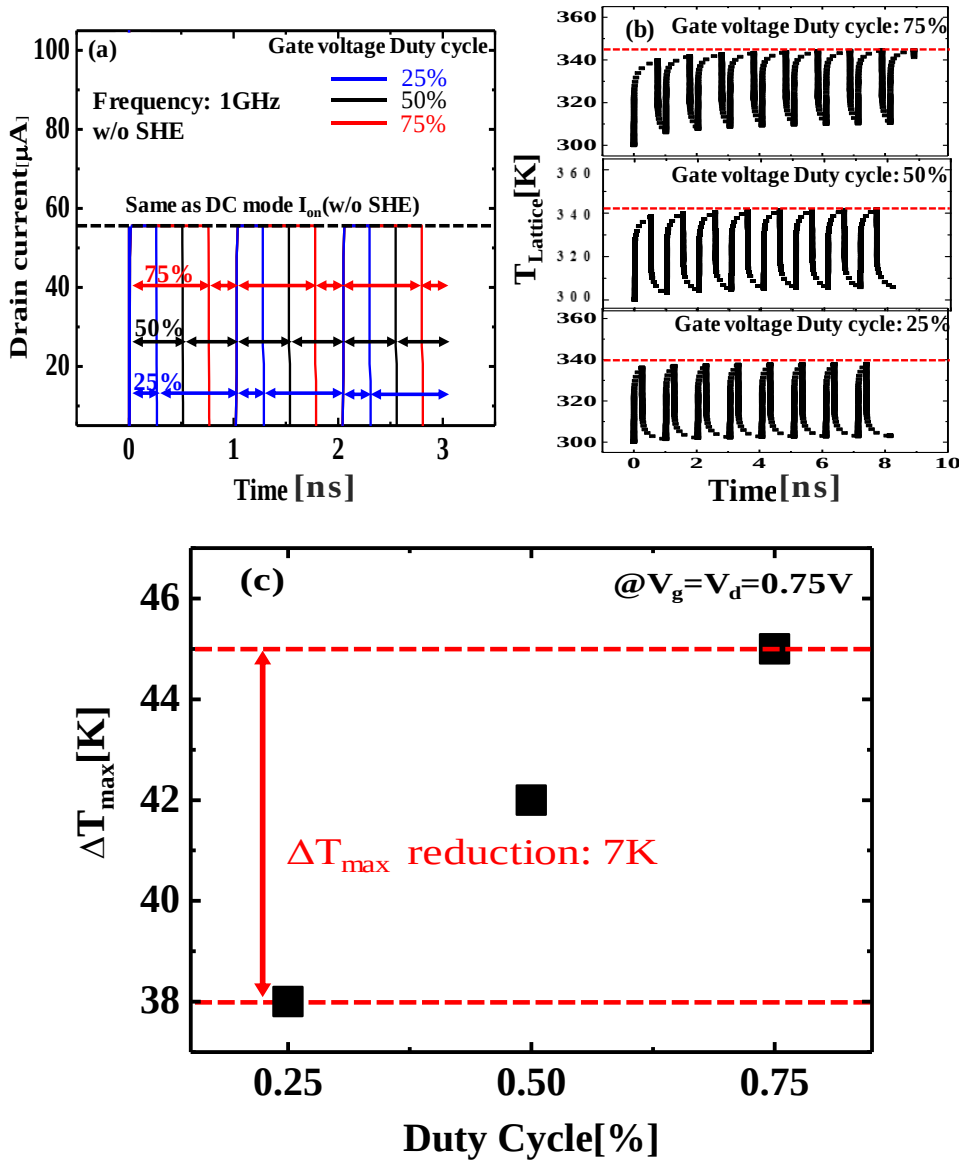



Fig. 3.10 (a) $I_{on}$ comparison according to duty cycle when SHE is not considered, (b) Comparison of $T_{Lattice}$ according to duty cycle, (c) $\Delta T_{max}$ Comparison according to Duty Cycle.

A comparison of the HCI/BTI lifetime is shown in Fig. 3.11, where τ is normalized with the HCI/BTI lifetime at 300 K ($\tau_{300K}$). The $E_a$ and the *n* of the nanowire-FET were assumed to be the same as [18], [19], and [23]. The $\tau/\tau_{300K}$ ratio was significantly changed, from $1\times10^{-1}$ to $7\times10^{-3}$, according to the operation mode and the duty cycle of the ac mode. Therefore, in the ac mode, the SHE can be mitigated, as compared with the dc mode. In the ac mode, the performance can be maintained according to the duty cycle, while HCI and BTI lifetime can be increased up to two times and three times, respectively.

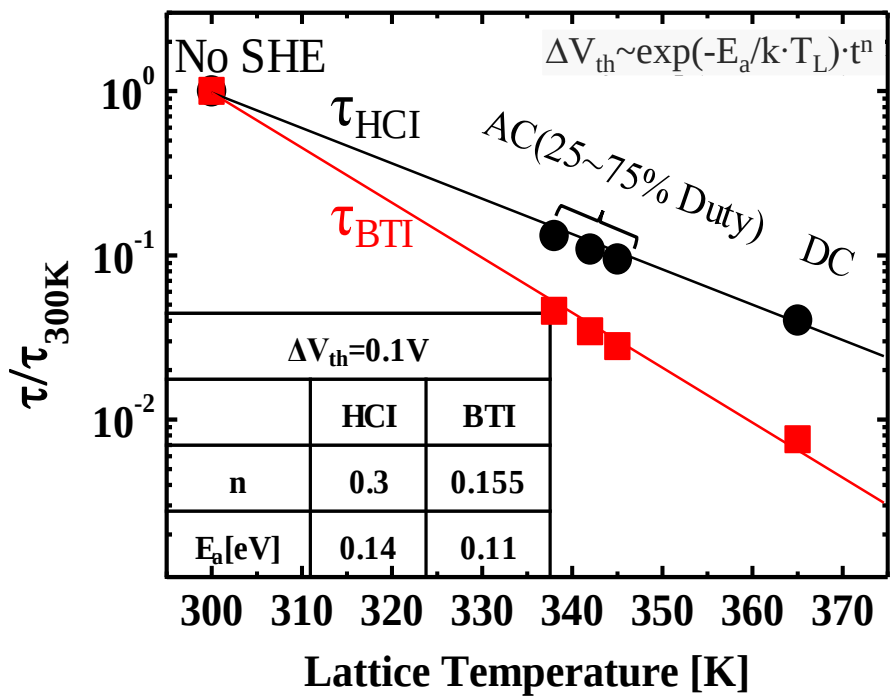



Fig. 3.11 A comparison of HCI (black) and BTI (red) lifetime as a function of $T_{L,max}$. The $T_{L,max}$ is determined by SHE with operation mode and various duty cycle

## 3.8 Summary

In this chapter, we analyzed the SHE of dc and ac for a three-channel nanowire-FET. When using a three-channel nanowire-FET over a single-channel nanowire-FET to increase the performance ($I_{on}$), $\Delta T_{max}$ in the dc mode increases from 50 to 65 K, resulting in an $I_{on}$ degradation rate of 3.8%. Also, the $R_{th}$ increases from 3.34 to 4.875 K/μW compared to the single channel. In the ac mode, when the heating time (PT) becomes longer, the total heat amount increases and the maximum temperature increases. Thus, a longer time is required for cooling to 300 K in the same device. Next, it was confirmed that $\Delta T_{max}$ decreases as the device operating frequency increases with the duty cycle set to 50% and $\Delta T_{max}$ saturates to about 40 K at 4 GHz. Finally, when the operating frequency is at 1 GHz, the temperature characteristics are analyzed while changing the duty cycle. As a result, $\Delta T_{max}$ is reduced when the duty cycle is short. In the ac mode, the performance can be maintained according to the duty cycle, while HCI and BTI lifetime can be increased up to two times and three times, respectively.

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# Chapter 4

# Self-Heating and Electrothermal Properties of Advanced Sub-5-nm node Nanoplate FET

## 4.1 Introduction

Reliability of modern field effect transistors (FET) emerged as one of the most important factors in the semiconductor industry to satisfy the increasing demand of stable computing performance. At the same time, industry continuously targeted to downscale devices by a few nano-meter range to improve integrated circuit performance. Race to downsize transistor introduced new innovative device structures such as Fin-shaped transistor (FinFET) [1-3], nanowire transistor and stacked nanoplate GAA transistor [4]. However, as a result of aggressive downscaling, current FinFET showed high thermal resistance and lattice temperature due to SHE, putting thermal reliability at stake [5,6]. SHE ultimately leads to performance and other reliability issues including, but not limited to, on-current degradation, hot carrier injection (HCI), Bias-temperature instability (BTI) and reduction of device's lifetime [7-9]. Being considered as a successor of FinFET,

GAA nanoplate-FET has growing concerns for self-heating effect as well [10]. Many suggests that especially for nanoplate-FET, SHE could be worse than FinFET due to confined geometry, where gate dielectric with low thermal conductivity fully surrounds the channels [11,12]. In this paper, based on ITRS 2015, nanoplate-FET that appeared as a new candidate in/under 5-nm node [4] is modelled through Sentaurus, a Technology Computer-Aided Design (TCAD) simulator. We have analyzed the temperature characteristics by manipulating several architecture parameters such as number of channels, channel width, and inter-layer metal thickness. And lastly, HCI / BTI lifetime according to maximum lattice temperature (TL,max) fluctuations by varying gate metal thickness is analyzed.

## 4.2 Device Structure and Simulation Condition

The multi-channel nanoplate-FET structure used in this paper is simulated using a Synopsys Sentaurus [13], a TCAD simulator. Detailed specifications of structure are referred from the values of the 5-nm node in the International Technology Road Map for Semiconductor (ITRS) [14], listed in Table 4.1. Fig. 4.1 shows the entire structures and cross-sectional views of a multi-channel nanoplate-FET for the self-heating study [8-10]. Source (S) and drain (D) structures are modelled as cuboid [4], and the size of S/D bulk is changed according to channel width ($T_W$) and metal thickness ($T_M$) [21]. S/D is doped with phosphorus (P) as other materials such as arsenic (As) can easily damage the silicon Epi. A metal contact is contacted over the S/D bulk, where S/D bulk is composed of Silicon.

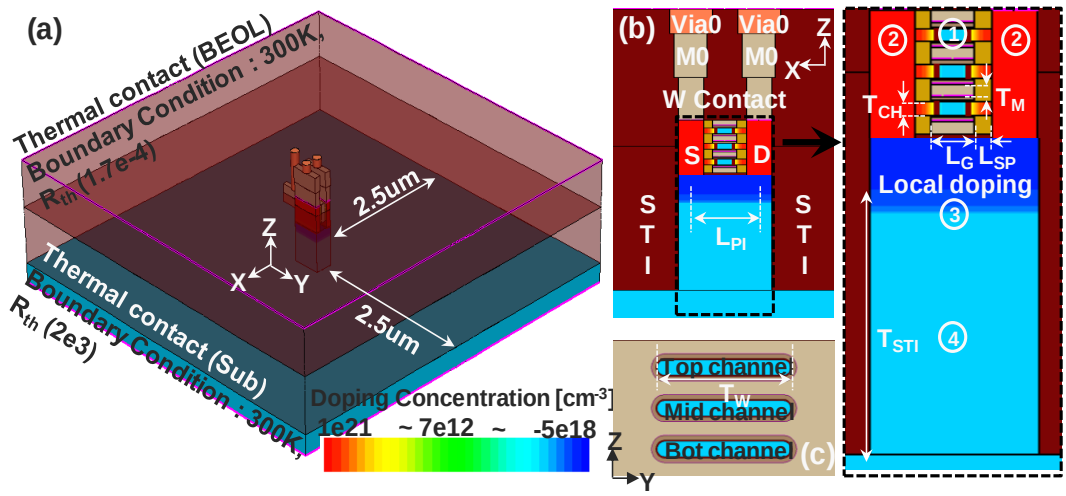


Fig. 4.1 (a) 3-D nanoplate-FET structure with the thermal contact, boundary condition, (b) XZ plane of a 3-D nanoplate-FETs, (c) YZ plane of a multi-channel region.

Table 4.1

Structural / Thermal specification of a nanosheet-FET

| **Structural Parameters** | **Value** (Unit: nm) | **Thermal Conductivity** | **Value** (Unit: W/K·m) |
|---|---|---|---|
| Gate Length ($L_G$) | 12 | ① Channel | 7.5 |
| Spacer Length ($L_{SP}$) | 5 | ② Source/Drain (Phosphorus) | 9.4 |
| Gate Pitch ($L_{PI}$) | 48 | ③ Local doping | 45.4 |
| Channel Thickness ($T_{CH}$) | 5 | ④ STI-all-around | 46 |
| STI Thickness ($T_{STI}$) | 100 | ⑤ Substrate (Bulk silicon) | 148 |
| Channel Width ($T_W$) | 25 | Oxide ($SiO_2$) | 1.4 |
| Effective Oxide Thickness (EOT) | 1 | Interconnect (Cu / W) | 400 / 175 |
| Gate metal thickness ($T_M$) | 4.45 | Metal gate (W) | 175 |
| Substrate Width | 5000 | **Thermal Contact Resistance** | **Value** (Unit: $cm^2$·K/W) |
| **Doping Concentration** | **Value** (Unit: $cm^{-3}$) | $Si/SiO_2$ interface | $2\times10^{-4}$ |
| | | Back End Of Line (BEOL) | $1.7\times10^{-4}$ |
| Source/Drain Doping | $1\times10^{21}$ | Thermal Contact Resistance (Sub) | $2\times10^{3}$ |
| Local Doping | $5\times10^{18}$ | Thermal Boundary condition (BEOL, Sub) | 300K |

Fig. 4.2 (a) shows the active area divided into five regions. Fig. 4.2 (b) shows calculated thermal conductivity curve based on doped impurity type, doping concentration, and region thickness with reference to the previous research [19] on modelling thermal conductivity of silicon using the Phonon Boltzmann transport equation. We used this curve to determine thermal conductivity of each region in the parameter section.

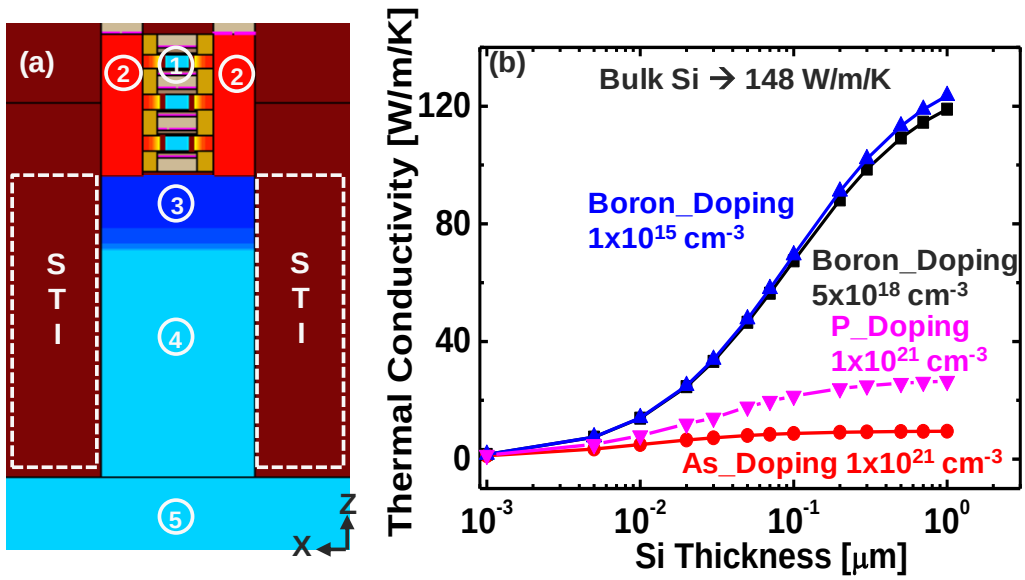


Fig. 4.2 (a) Five regions for setting thermal conductivity. (b) Thermal conductivity according to the doping type and concentration versus Si thickness.

Fig. 4. 3 (a) shows the overall experiment process. Firstly, calibration of the nanoplate-FET is performed to match the published on-current data [4]. Next, optimization of thermal characteristics is done by adjusting the channel width, which is then illustrated in respect to the number of stacked channels [15]. Finally, optimization by varying gate metal thickness, is performed considering the fabrication limitations, to analyze SHE under more realistic circumstances [15-17,20]. For I–V calibration to reflect true performance measurement of the data, adjustments in both quantum model using gate work function (WF) and saturation velocity are made [18]. And for realistic reflection of thermal and electrical properties, density gradient quantization model (quantumPotential) [13] and mobility model (thin layer / phumob / Enormal(lombardi)) [13] are utilized to consider the quantum effect, Coulomb scattering and interfacial surface roughness scattering. Thermal conductivity of each region, contact resistance, and boundary condition (300 K) to each heat path are also considered as shown in Fig 4. 1 (a), and Table 4. 1.

Fig. 4. 3 (b) shows that our simulation result is well calibrated with the measured data in [4]. This calibrated TCAD model is ultimately utilized to analyze the electro-thermal characteristics of the sub-5-nm node nanoplate-FET.

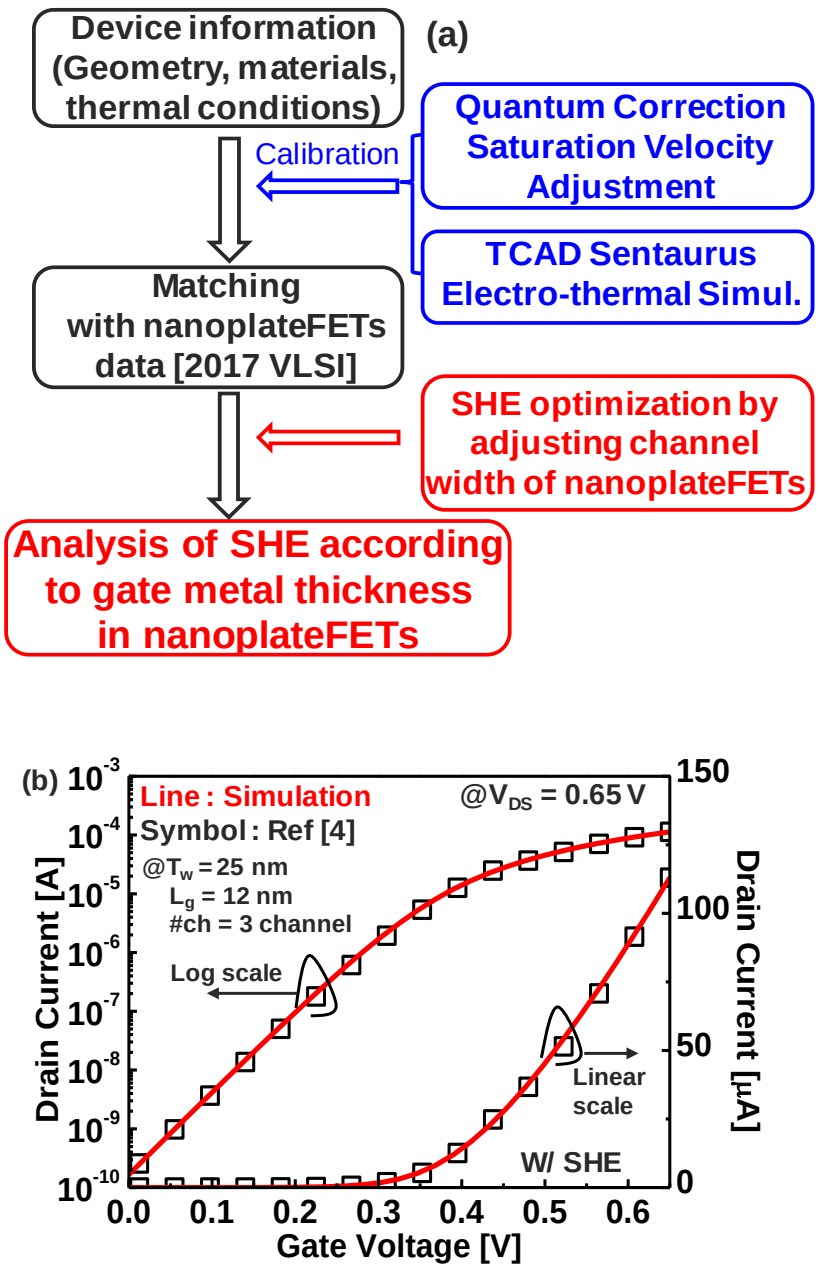


Fig. 4.3 (a) Overall work flow for the analysis of SHE in nanosheet-FET. (b) $I_D$-$V_G$ calibration results based on the nanosheet-FET.

## 4.3 Thermal characteristics by channel number and width

As shown in Fig. 4.4 (a) and inset of Fig. 4.4 (b), when using a stacked three-channel nanoplate-FET over a single-channel nanoplate-FET to increase the performance ($I_{on}$), $\Delta T_{max}$ increases from 61 to 78 K for channel width ($T_w$) of 20 nm due to heat coupling between channels. Also, when channel width ($T_w$) is increased from 20nm to 45nm in the three-channel nanoplate-FET to obtain better performance (higher on-current), $\Delta T_{max}$ increases from 78K to 103K as Joule heat increases with high performance. However, only examining lattice temperature does not show meaningful analysis of thermal characteristics on nanoplate-FET and should further examine thermal resistance ($R_{th}$), which is a parameter that shows the correlation between DC power and temperature as shown in Fig. 4.4 (c). From a macroscopic point of view, if rise of temperature is lower than the improvement of performance, overall it could be considered as a good device. Therefore, further analysis on $R_{th}$ is conducted for nanoplate-FETs with varying number of channels where $R_{th}$ is not normalized against the number of channels. As shown in Fig. 4.4 (d), as Tw widens, $R_{th}$ decreases since the heat generated in the channel is easier to dissipate through the source and drain bulk. Following this $R_{th}$ trendline, stacked three-channel nanoplate-FET with $T_w$ of 45nm has the lowest $R_{th}$ characteristics. Due to this $R_{th}$ characteristics, as shown in Fig. 4.4 (b), the $I_{on}$ degradation rate is also the lowest in the three-channel nanoplate-FET with $T_w$ of 45nm. Therefore, further analysis of SHE is simulated with variations of inter-layer metal thickness ($T_M$) in the nanoplate-FET while having $T_w$ of 45nm constant, which had the most reliable thermal characteristics out of all options explored for channel width above.

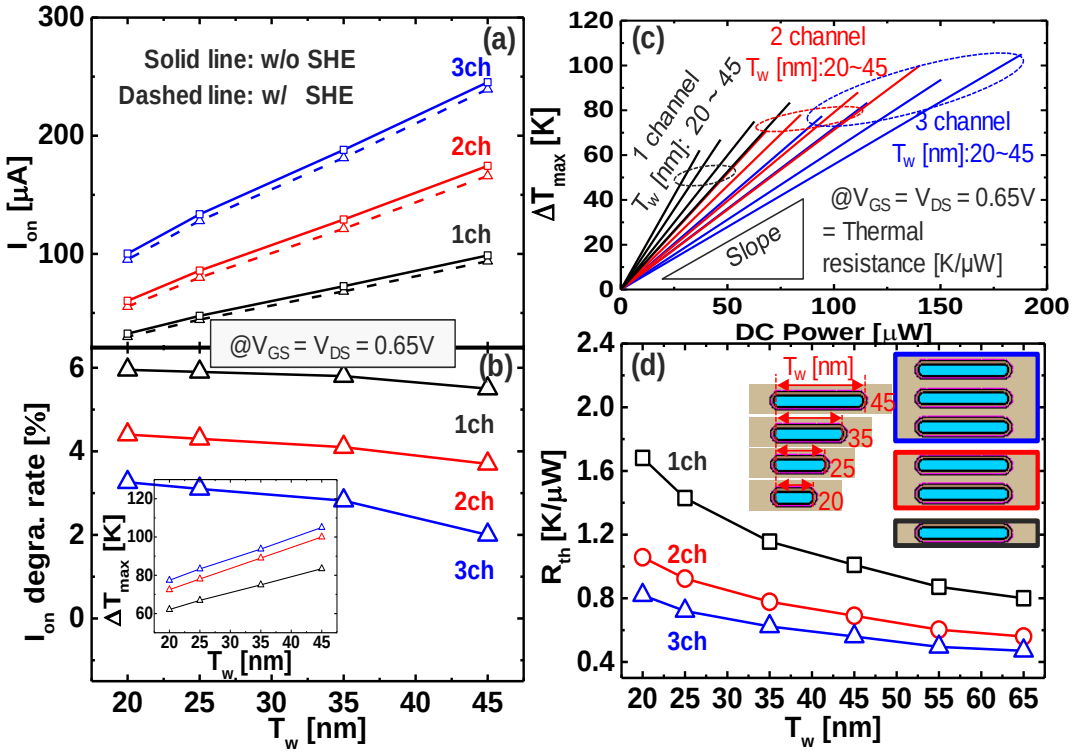


Fig. 4.4 Thermal characterization by channel width ($T_w$) in nanosheet FETs. (a) $I_{on}$ according to w/ and w/o SHE, (b) $I_{on}$ degradation rate and $\Delta T_{max}$ by SHE, (c) DC power-$\Delta T_{max}$ curve, (d) Thermal resistance ($R_{th}$).

## 4.4 Thermal characteristics by inter layer-metal thickness ($T_M$)

Many studies indicate that various $T_M$ is used when presenting nanoplate-FET structure [15-17,20]. For the analysis on impact of inter-layer metal thickness ($T_M$) on SHE, TM is reduced from 25nm to 4.45nm. As TM increases, as shown in Fig. 4.5 (a), total capacitance ($C_{total}$) and resistance ($R_{total}$) also increase. This is due to the increased area of the metal and source/drain on both sides of the inner spacer and increased source/drain vertical resistance. Depending on the structure of the device, various resistance components such as vertical resistance, sheet resistance, and contact resistance are responsible for the increase with different contributions. Vertical resistance mainly accounts for the increase of total resistance. Because sheet resistance and contact resistance are the components that make the total resistance smaller as the S/D epi size increases. As shown in Fig. 4.5 (b), RC time delay, a performance indicator, increases with increasing $T_M$. On the other hand, as $T_M$ increases, thermal indicator of $\Delta T_{max}$ and $R_{th}$ decrease as shown in Fig. 4.5 (b) and (c). This illustrates that performance measurement of RC time delay is compensated in return of a better thermal reliability when increasing $T_M$. Therefore, we defined Figure of Merit (FoM) factor to evaluate the technology trend of both performance and thermal characteristics.

$$\text{FoM} = 1/ (R_{th} \text{ x RC time delay}). \quad (1)$$

As shown in Fig. 4.5 (d), as the $T_M$ decreases, the overall performance improved in the three channel nanoplate-FET. Where FoM is for each $T_M$ condition and $FoM_{25}$ is when TM is 25 nm.

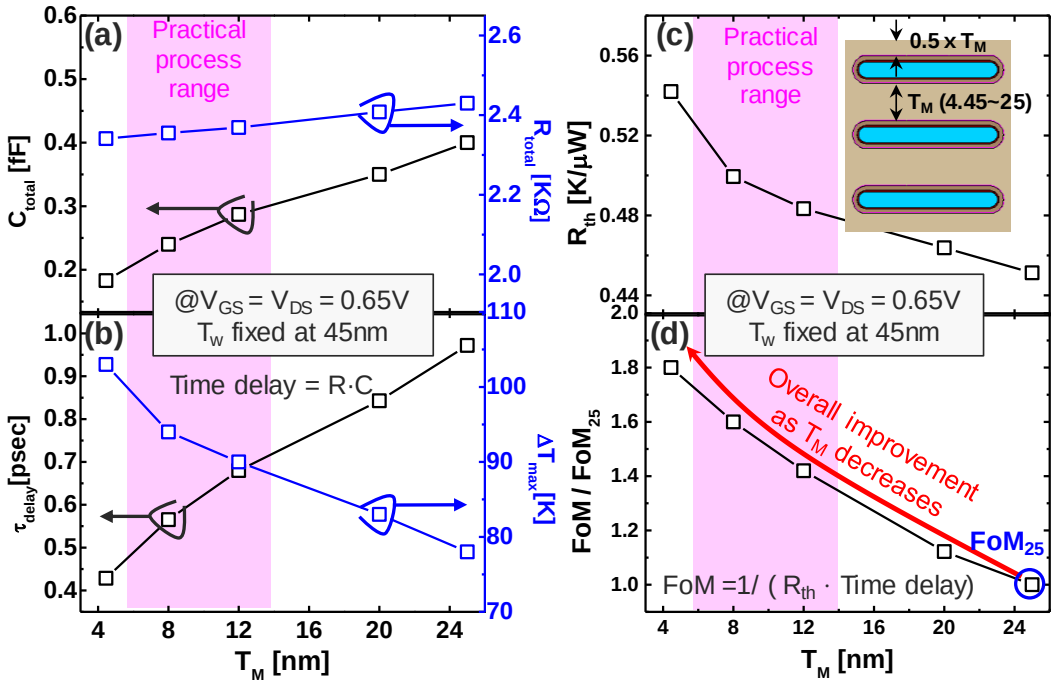


Fig. 4.5 Thermal characterization by $T_M$ in multi-channel nano-plate FETs. (a) Total capacitance and resistance, (b) Time delay and $\Delta T_{max}$, (c) $R_{th}$, (d) Figure of Merit (FoM) to determine overall performance.

## 4.5 Life Time Prediction

The HCI / BTI lifetime of nanoplate-FET can be predicted through $\Delta V_{th} \sim \exp(-E_a / k \cdot T_{L,max}) \times t^n$ with $E_a$ and n. Lifetime is defined as the time to reach $\Delta V_{th} = 0.1V$. As shown in the inset table in Fig. 4.5, the $E_a$ and n of the nanoplate-FET are assumed to be the same as [7, 18]. The $\tau/\tau_{300K}$ ratio is changed per gate metal thickness, where $\tau_{300K}$ means lifetime when no temperature rises due to SHE, i.e., T = 300K and $\tau$ is the lifetime for each of the $T_M$ when the temperature rises due to SHE. As can be seen in Fig. 4.6, for

HCI, as the interlayer metal thickness is increased based on $T_M$: 4.45nm, the life time increases up to 2.33 times due to the decreasing device temperature. BTI life time also increases the life time by 3.63 times compared to 4.45 nm for the same reason. Therefore, it is advantageous to increase the $T_M$ to increase the life time and prevent thermal degradation of the device (i.e. temperature increase).

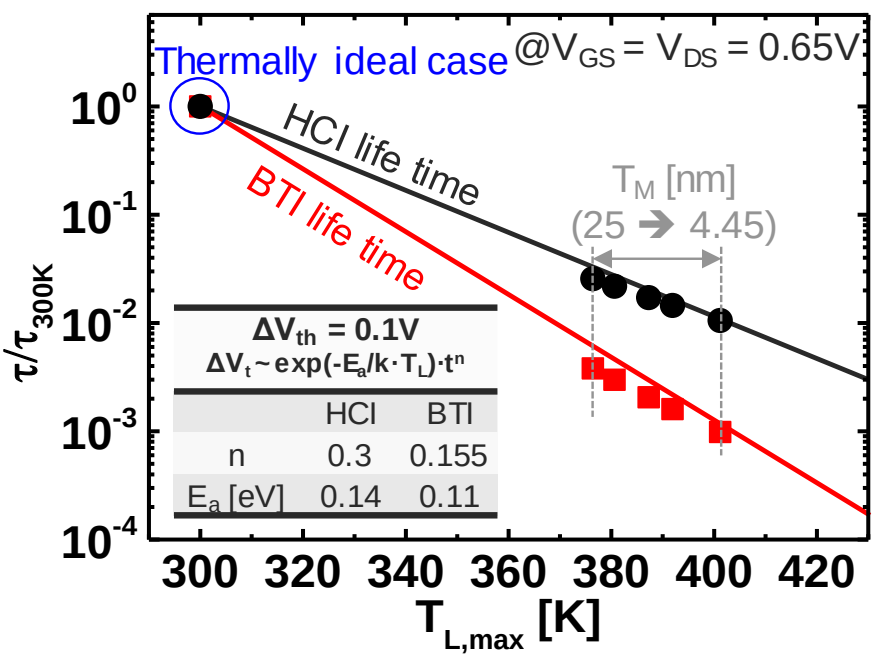


Fig. 4.5 A comparison of HCI / BTI lifetime as a function of $T_{L,max}$ according to $T_M$.

## 4.6 Summary

In this chapter, we analyzed SHE of nanoplate-FET according to active area specifications used at the sub-5nm node including number of channels, channel width $T_w$ and metal thickness $T_M$. When stacked three-channel with $T_w$ of 25nm is chosen over a single-channel nanoplate-FET with same $T_w$ to increase the performance ($I_{on}$), $\Delta T_{max}$ increases from 61 to 78 K due to heat coupling between channels. Extending the performance measurement by increasing Tw from 20nm to 45nm in the three-channel nanoplate-FET, $\Delta T_{max}$ increases further from 78K to 103K as Joule heat increases with high performance. However, when investigating thermal resistance $R_{th}$, which is more comprehensive measurement to understand thermal reliability of a device, three-channel nanoplate-FET with $T_w$ of 45nm has the lowest $R_{th}$. Both $I_{on}$ and $R_{th}$ characteristics are improved with increased $T_W$, and $R_{th}$ tends to be saturated when $T_W$ is 45nm or higher. Then, SHE is analyzed with variations of $T_M$ from 25nm to 4.45nm, and constant $T_w$ of 45nm. As $T_M$ increases, performance parameter of RC delay increases but thermal parameter of $R_{th}$ decreases. Therefore, this is judged comprehensively using FoM factor and suggests that overall, the device improves as $T_M$ decreases. However, designing a multi-channel nanoplate-FET with a lower $T_M$ should be carefully adjusted because HCI / BTI life time, which is affected by temperature, can be reduced significantly due to increased lattice temperature.

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# Chapter 5

# Study on Self Heating Effect and life time in Vertical-channel Field Effect Transistor

## 5.1 Introduction

In this chapter, self-heating effect in newly introduced Vertical-channel Field Effect Transistors (VFETs) is investigated and discussed, and several architecture parameters such as channel width, number of channels affecting thermal reliability of VFET are studied through simulations. In addition, a study on the change of thermal properties is conducted when air gap/spacer is used to reduce the influence of the parasitic capacitance. It is illustrated that VFET shows high lattice temperature and thermal resistance increase from changes in such architecture parameters, air gap in BEOL (Back End of Line), and air spacers. Additionally, the lattice temperature imbalance between channels can be mitigated by adjusting the inter-channel spacing of a multi-channel VFET.

## 5.2 Device Structure and Simulation

Following device specification of ITRS Roadmap for 5nm node technology [14], a three-dimensional structure of single channel VFET is constructed using TCAD

SENTAURUS as shown in Fig. 5.1. The height of the BEOL (Back End of Line) is calculated as suggested in the preceding paper [8]. Thermal and electrical specifications of this device are shown in Table 5.1. The details of the thermal conductivity setting for each region are described later. To verify the accuracy of the predicted temperature through SENTAURUS simulator, First, using SENTAURUS, the SOI MOSFET structure [9] in the inset of Fig. 5.2 was made in the same way. Second, the basic model (thermodynamics [13]) was specified for the electro-thermal simulation and compared with the measurement data [9] of the planar SOI MOSFET. We confirmed that the simulation predicts the gate temperature well according to the power, as shown in Fig. 5.2. Then, to accurately reflect the change in thermal properties as the device shrinks, thermal conductivity of each region is calculated with taking account of phonon boundary and phonon impurity scattering [7].

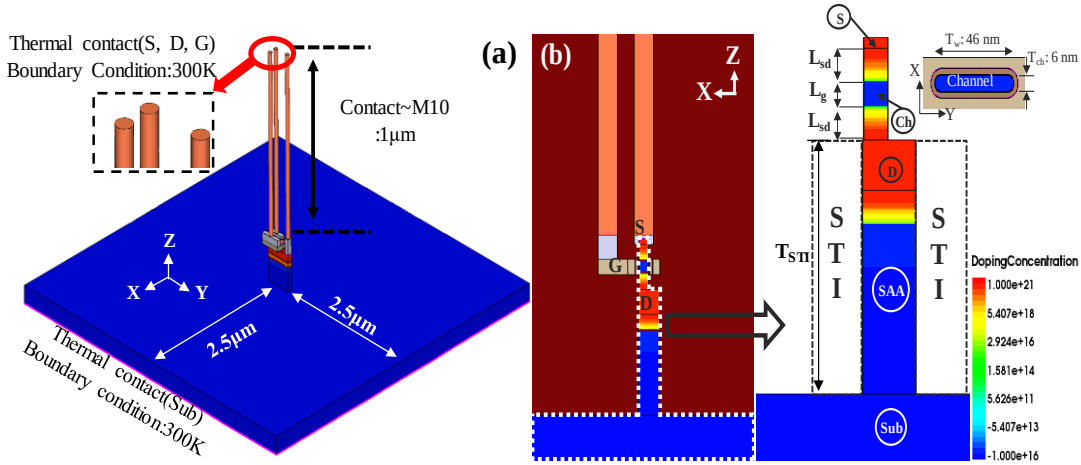



Fig. 5.1 (a) Entire structure of VFET, (b) Cross sectional views of VFET, (C) An enlarged view of a region highlighted by a dotted line in (b).

Table. 5.1

Thermal / electrical specifications of single-channel Vertical Field Effect Transistor (VFET) following ITRS roadmap for 5nm node.

| **Structural Parameters** | **Value** (Unit: nm) | **Thermal Conductivity** | **Value** (Unit: W/K·m) |
|---|---|---|---|
| Gate Length ($L_g$) | 12.2 | ① Source | 3.8 |
| Spacer Length ($L_{sd}$) | 11.9 | ② Channel | 8.9 |
| Channel Thickness ($T_{ch}$) | 6 | ③ Drain | 5.6 |
| STI Thickness ($T_{STI}$) | 100 | ④ STI-all-around | 18 |
| Channel Width ($T_w$) | 46 | ⑤ Substrate (Bulk silicon) | 148 |
| Effective Oxide Thickness (EOT) | 0.7 | Oxide ($SiO_2$) / SiCOH / Vacuum | 1.4 / 0.6 / 0 |
| BEOL Height | 1000 | Interconnect (Cu / W) | 400 / 175 |
| Substrate Width | 5000 | **Thermal Contact Resistance** | **Value** (Unit: $cm^2$·K/W) |
| $V_{DD}$ ($V_{GS}$,$V_{DS}$) | 0.65V | | |
| **Doping Concentration** | **Value** (Unit: $cm^{-3}$) | $Si/SiO_2$ interface [2,3] | $2\times10^{-4}$ |
| Source/Drain Doping (As) | $1\times10^{21}$ | Thermal Contact Resistance (Sub) | $2\times10^{3}$ |
| Channel Doping (Boron) | $1\times10^{16}$ | Thermal Boundary condition (S, D, G, Sub) | 300K |

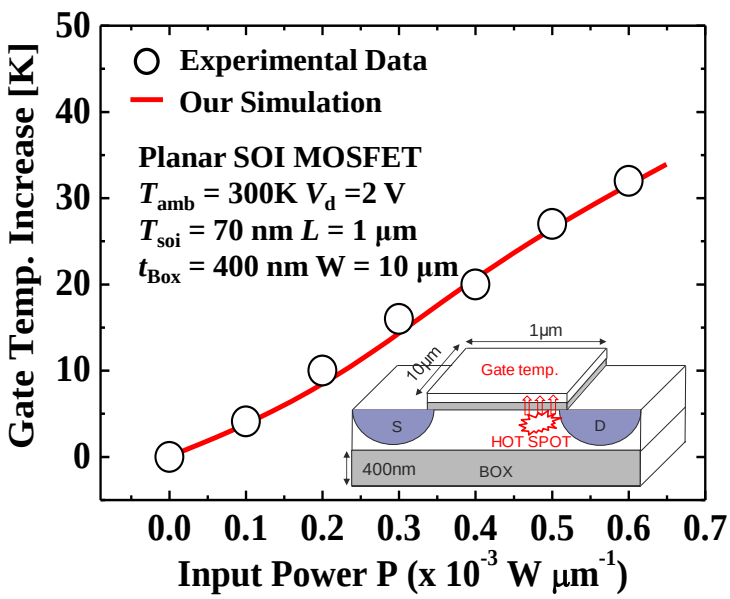



Fig. 5.2 Comparison of simulation and measured data to clarify the accuracy of the thermal analysis of the simulation.

Thermal conductivity of VFET, separated into five section is shown in Fig. 5.3 (a). Area 1 to 4 are small and thin so they are mainly affected by phonon boundary scattering, and area 5 is less affected by phonon boundary scattering because it is bulk silicon. In addition, since area 1 and 3 have a high doping concentration of $10^{21}$, they are greatly affected by phonon impurity scattering. The thermal conductivity according to the phonon impurity scattering and phonon boundary scattering for each area was calculated with reference to [10] and is shown in Fig. 5.3 (b). Based on fig. 5.3 (b), the thermal conductivity of five active regions is determined. It is also stated in Table.5.1. In TCAD SENTAURUS, hydrodynamic model [13] is utilized to analyze SH [8,11,12]. And density gradient quantization model (quantumPotential) [13] and mobility model (thin layer / phumob / Enormal(lombardi)) [13] are utilized to consider the quantum effect, Coulomb scattering and interfacial surface roughness scattering. Contact resistance and boundary condition (300 K) to each heat path are also considered as shown in Fig 5.1 (a), and Table 5.1.

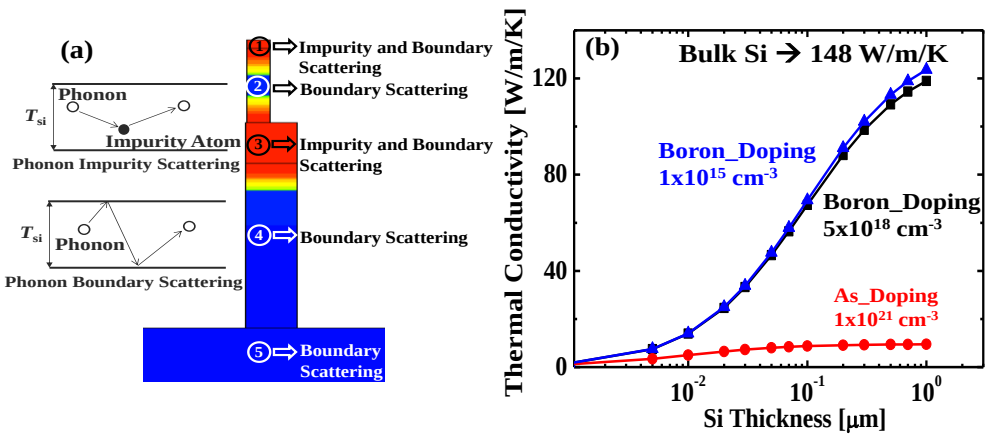



Fig. 5.3 Thermal conductivity of this device is calculated with taking account of phonon boundary and phonon impurity scattering. Thermal conductivity of each region, separated into five section according to doping concentration and dimension.

## 5.3. Temperature and $R_{TH}$ according to channel width($T_W$)

To evaluate the extent to which temperature adversely affect the single channel Vertical FET performance, on-current ($I_{on}$) is calculated without SH and with SH. Then, these data are plotted into Fig. 5.4, which clearly illustrates that due to SH, the device cannot fully perform at its maximum as there is on-current degradation of 5.5% when $V_{DD}$ =0.65V. Also, through the heat flux of each heat path, the main heat path is the substrate [5,6,8].

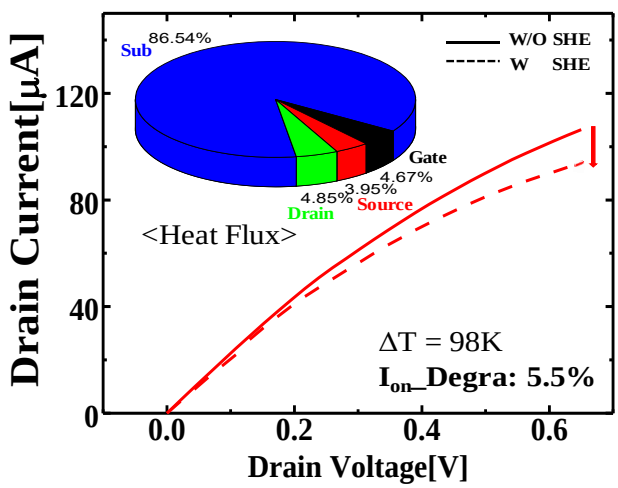



Fig. 5.4 On-current ($I_{on}$) degradation rate and heat flux in each heat path in VFET. Max Lattice temperature rises to 98K in single-channel VFET. And $I_{on}$ degradation rate is 5.5%.

Fig. 5.5 (a) shows the YZ cross section view of VFET. Fig. 5.5 (b) shows $P_{DC}$-$\Delta T_{L,max}$ curve according to channel width ($T_w$). $R_{th}$ is obtained from slope of this curve. As a

result, as shown in inset of fig. 5.5 (b), $R_{th}$ decreases according to cases from 1 to 5. The reason why the $R_{th}$ decreases as the $T_w$ increases is that the main heat path of the VFET is the substrate and the efficiency of the heat dissipation to substrate increases as the $T_w$ increases. Thus, even if the performance ($I_{on}$) is improved by increasing the $T_w$ in the VFET, the thermal characteristic is not deteriorated. Therefore, in the later analysis, $T_W$ is carried out in a fixed at 46nm.

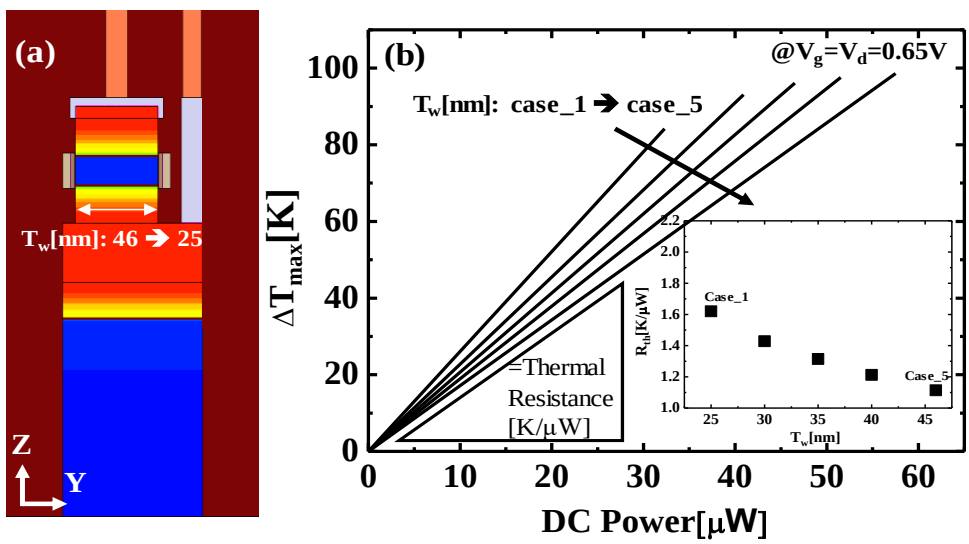



Fig. 5.5 (a)Y-Z cross sectional views of VFET, (b) DC Power ($P_{DC}$) – $\Delta T_{L,max}$ curve for $R_{th}$ according to $T_w$.

## 5.4. Thermal properties according to air spacers and air gap

As the length of the channel becomes shorter, the influence of drain and source on the channel increases, and thus parasitic capacitance is an issue. Therefore, to reduce parasitic capacitance between source/drain and channel, vacuum with low dielectric constant is

used as spacer. Meanwhile, in the case of vacuum, the thermal conductivity is close to zero. Therefore, analysis of current and temperature according to the use of vacuum spacer is conducted.

Fig. 5.6 (a) and (b) show the structure and temperature contours when SiCOH spacer and vacuum spacer are used. In the case of the vacuum spacer, the temperature rises about 5K higher than that of the SiCOH spacer due to the very low thermal conductivity characteristics. In addition, as shown in Fig. 5.6 (c), the $I_{on}$ degradation rate increases from 5.5% to 7% due to the increased temperature when vacuum with a very low thermal conductivity is used as spacer. Thus, when the vacuum spacer is used, the subthreshold slope characteristics of the device may improve by reducing the parasitic capacitance, but the temperature and $I_{on}$ degradation rate characteristics are deteriorated. Therefore, the use of vacuum spacers, which can affect the reduction of $I_{on}$ and deterioration of temperature characteristics, should be handled carefully depending on the desired performance condition.

In 7 nm node BEOL and beyond, the Cu interconnect faces a sharp increase in line R. The reasons are, first, the line width is smaller than that of Cu electron MFP. Second, it has a limited Cu volume fraction due to the presence of a barrier/wetting layer with limited scaling [15]. Therefore, in the sub 7nm node device, the BEOL time delay increases due to the increased R of BEOL. Accordingly, SiCOH having a lower dielectric constant is recently used in Inter Layer Dielectrics (ILD) [15]. In addition, a method of reducing parasitic capacitance in a layer where metal is densely processed has been proposed by using air gap [16]. Based on these facts, the thermal characteristics of device

are analyzed according to the use of SiCOH and air gap in BEOL.

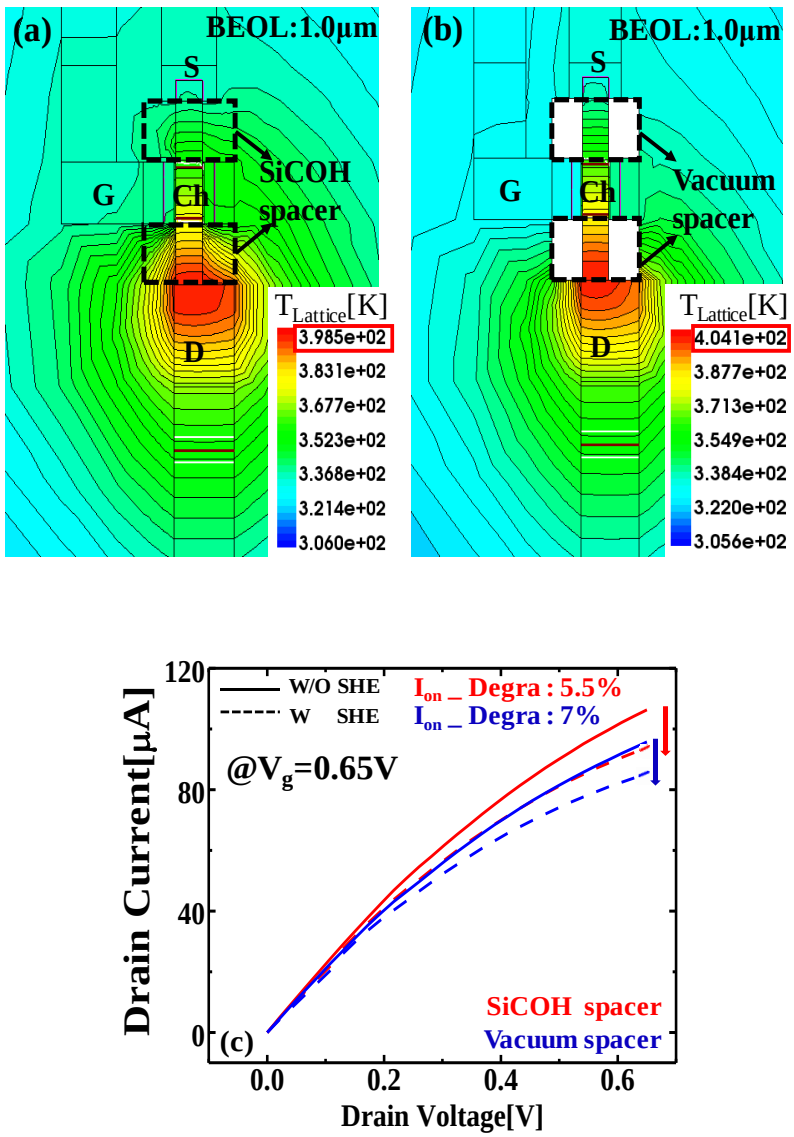
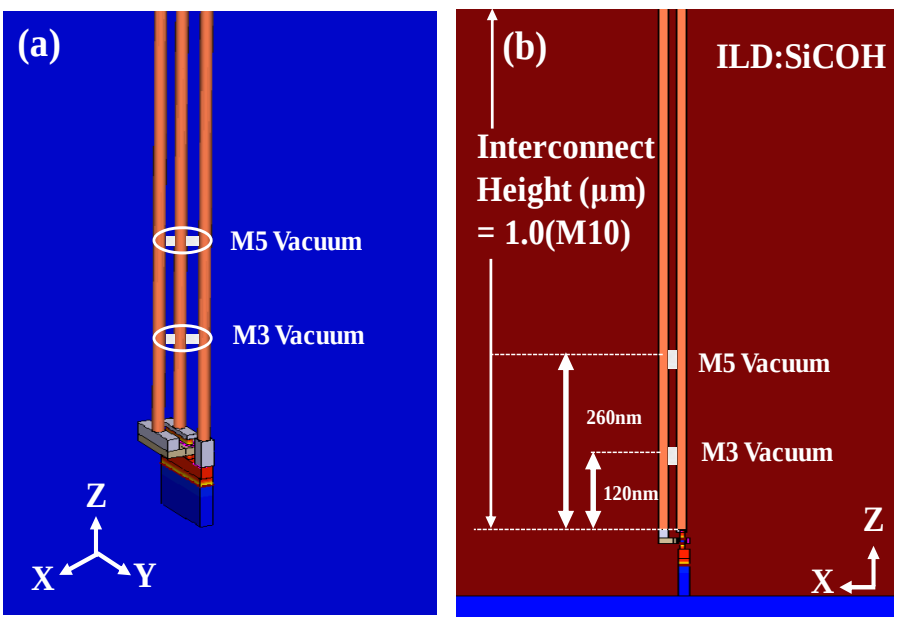



Fig. 5.6 Temperature contour and $T_{max}$ when using (a) SiCOH spacer and (b) vacuum spacer, (c) Each $I_D$-$V_D$ curve and $I_{on}$ degradation rate.

Fig. 5.7 (a) and (b) show 3D and XZ planes, respectively. SiCOH is used as ILD with reference to [15], and the properties of the materials are also reflected. In addition, layers with air gaps are determined by referring to [16], and the heights of the layers are calculated by referring to [8]. Fig. 5.7 (c) shows the $\Delta T_{max}$ of the hot spot according to the thermal conductivity of the ILD material, where 1.4W/K·cm corresponds to the general $SiO_2$ and shows a temperature rise of about 89K. And when SiCOH with 0.6W/K·cm is used, it can be seen that the temperature rises about 10K higher than that of $SiO_2$. In addition, when air gaps are used in the M3 and M5 layers, the temperature increases by 1~2K additionally. Therefore, when using SiCOH and air gaps to reduce the time delay of BEOL, it is necessary to recognize that the temperature characteristics are degraded, and SiCOH is the main case.



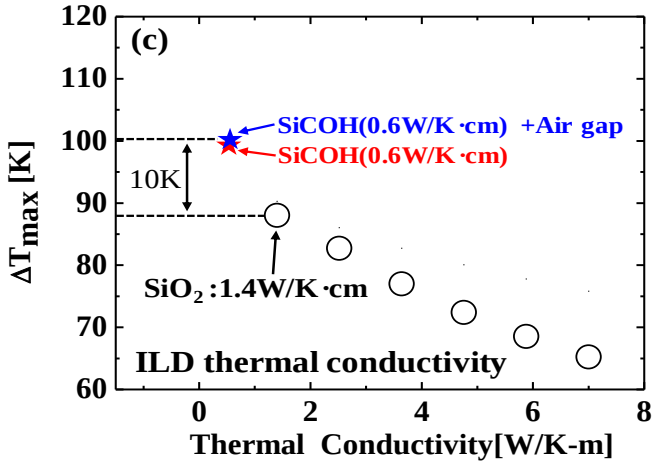



Fig. 5.7 Structure when using air gap in M3 and M5 layers (a) 3D, (b) XZ plane. (c) $\Delta T_{max}$ of hot spot according to thermal conductivity of inter layer dielectric.

## 5.5. $I_{on}$ boosting according to Channel numbers

To improve $I_{on}$ characteristics, this single-channel VFET is modified into three and five channels by arranging the channel horizontally. Five channel VFET is shown in Fig. 5.8.

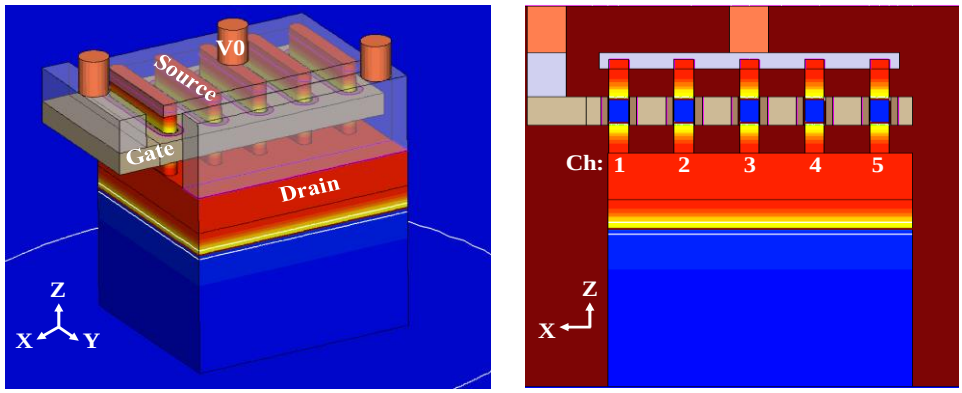



Fig. 5.8 (a) Entire structure of multi-channel VFETs, (b) XZ plane of multi-channel VFETs.

As shown in Fig. 5.9, the structure can be confirmed when increasing from 1 channel to 3 or 5 channels, As the channel increases, $I_{on}$ also increases logarithmically. This is better than LFETs (for example, multi-channel NWFETs, NanoplateFETs [11,12]). In the case of Lateral FET, as the channel is stacked, S/D bulk sheet resistance ($R_{ext}$) increases, and $I_{on}$ boosting tends to saturation. However, in the case of VFETs, the drain metal can affect the multi-channel equally, so that the $I_{on}$ can be logarithmically increased.

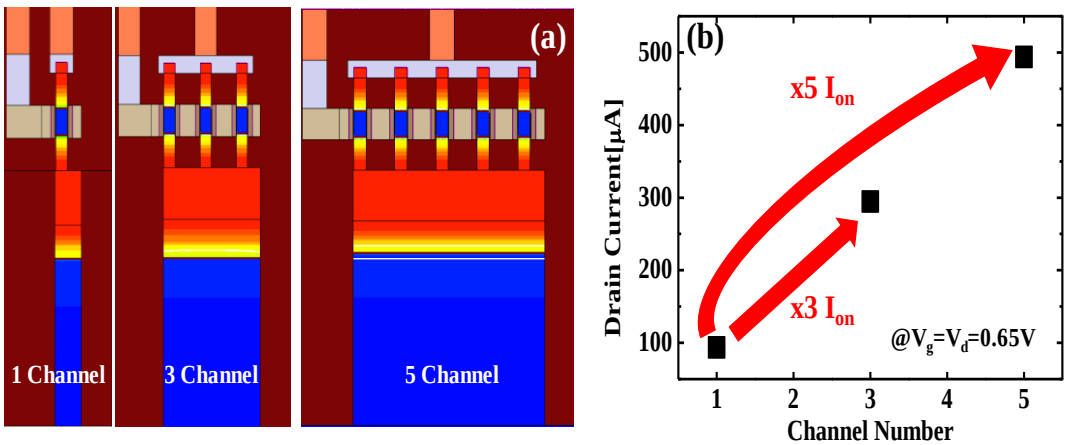



Fig. 5.9 (a) Structure of VFETs according to channel number (1,3,5) and (b) $I_{on}$ change according to channel number.

## 5.6. Temperature imbalance of multi-channel VFETs

Fig. 5.10. (b) shows the temperature of channels when using five-channel VFET for performance ($I_{on}$) improvement. When using five channels compared to single-channel VFET ($\Delta T_{max}$: 98K), it can be seen that the temperature increases up to 135K by thermal coupling. Also, as shown in Fig. 5.10 (a), the STI is extended to the right to reduce the fringing capacitance between the gate via and the drain bulk. As a result, effective area below the first channel is reduced, which reduces the heat path to the substrate (refer to

the heat flux vector in Fig.5.11 (a)). For this reason, the temperature decreases from first to fifth channel as shown in Fig. 5.10 (b).

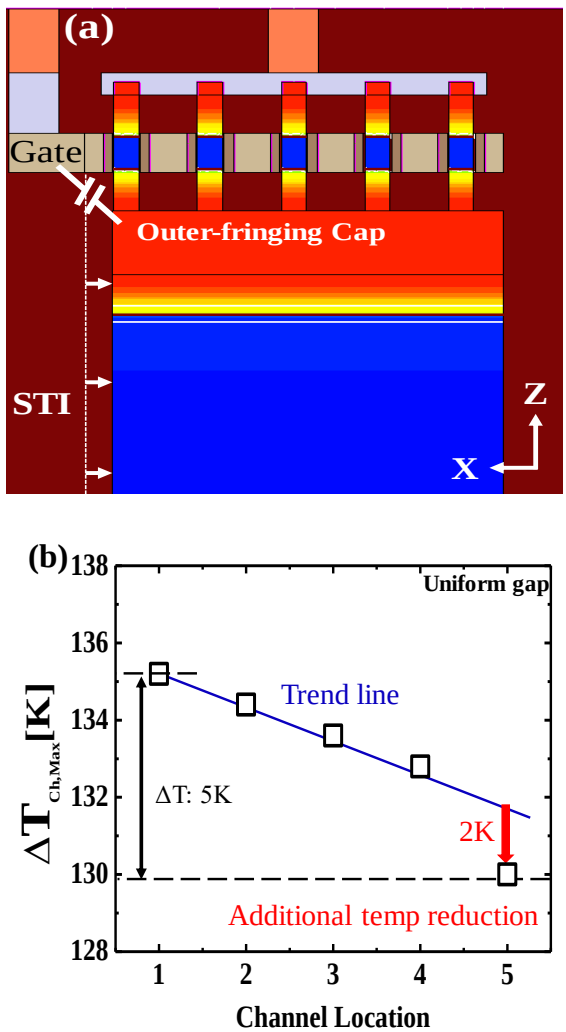



Fig. 5.10 (a) Cross sectional view of five channel VFETs. the STI is extended to the right to reduce the fringing capacitance between the gate via and the drain bulk, (b) Temperature of channels when using five-channel VFET for performance ($I_{on}$) improvement.

In addition, the temperature in the fifth channel is further reduced, which can be explained in Fig.5.11 (b). Fig. 5.11 (b) shows the top view of the VFET. Due to the nature of the structure, the drain metal is located beyond the right side of the fifth channel and there is an un-coupled heat flux to the side, which results in an additional temperature decrease of 2K in fifth channel. To further confirm above claim for the additional temperature reduction of 2K in fifth channel, we have created 3-channel, 5-channel, 6-channel VFETs and analyzed the temperature profile as shown in Fig. 5.11 (c). Additional temperature reduction occurs in the third and sixth channels in the 3-channel and 6-channel VFETs. When multi-channel is used to increase the performance ($I_{on}$) of a VFET, thermal coupling between channels causes the temperature increase of the channels more than that in the single channel, as well as the temperature variation between the channels. Therefore, when the device is used for a long time, SH may cause performance difference or life time difference between channels. we proposed a method to mitigate the temperature imbalance between channels.

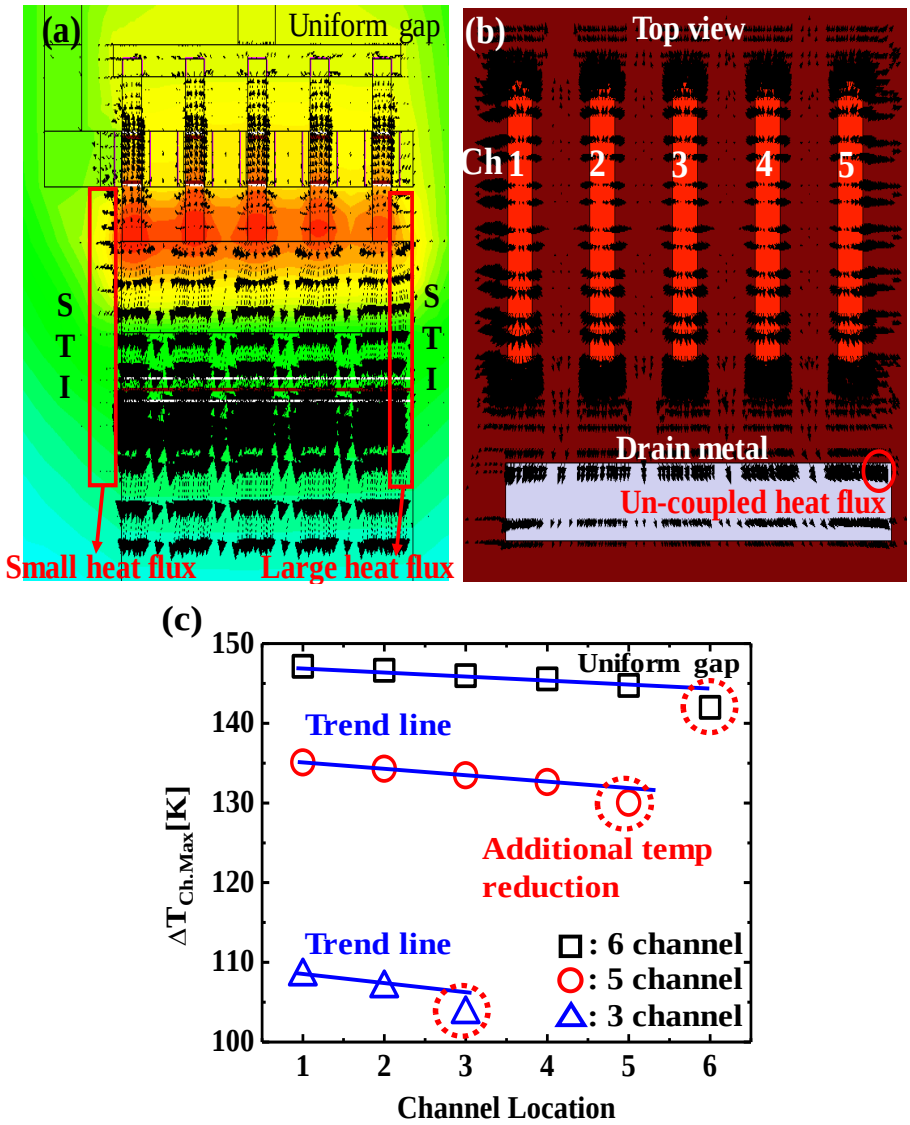
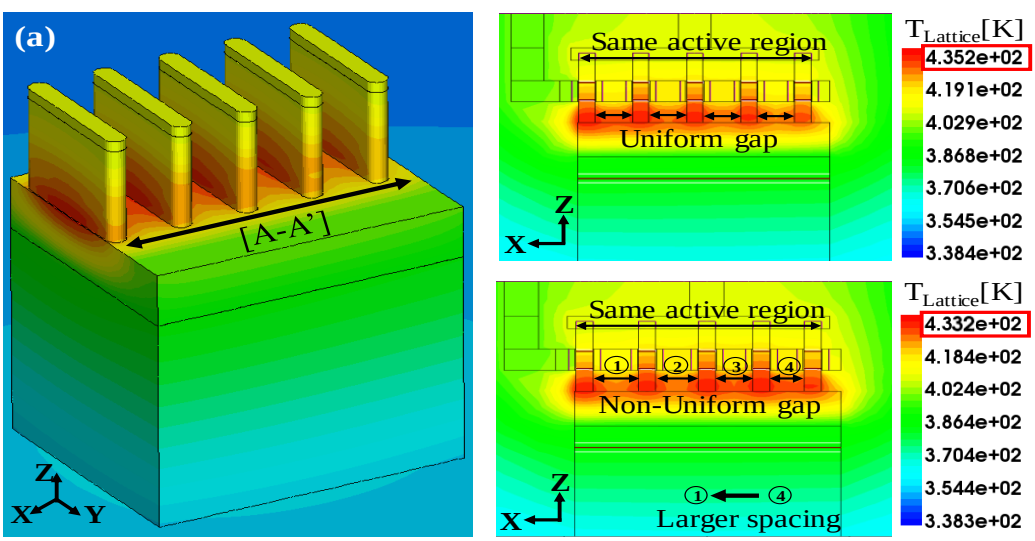



Fig. 5.11 heat flux in VFETs (a)XZ plane, (b) the top view of the VFET. (c) Additional temperature reduction occurs in the third and sixth channels in the 3-/ 6-channel VFETs.

## 5.7. Mitigation of the channel temperature imbalance

Fig. 5.12 (a) shows the adjustment of channel gap to mitigate temperature imbalance between channels. In the XZ plane, we compared the structures where the gap between the channels is uniform and non-uniform. In the case of the non-uniform gap, the gap between the channels is made larger toward the first channel having the highest temperature in order to reduce the thermal coupling. The size of the active region from the first channel to the fifth channel is same. Fig. 5.12 (b) shows that performance ($I_{on}$ / $I_{off}$) is not adversely affected when a device is fabricated with a non-uniform gap because the active region has the same size. Fig. 5.12 (c) is a comparison of $R_{th}$, which shows that $R_{th}$ in the non-uniform gap is slightly smaller than the uniform gap.



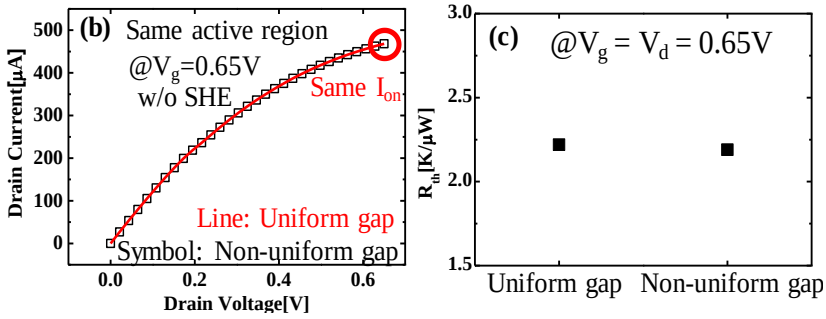



Fig. 5.12 (a) Simulation structure for 5 vertical channel arrangement for VFETs and XZ plane for uniform/non-uniform gap in channels. (b) performance ($I_{on}/I_{off}$) for uniform/non-uniform gap. (c) $R_{TH}$ for uniform/non-uniform gap.

The maximum temperature is reduced by 2K as shown in Fig 5.13 (a). Finally, Fig. 5.13 (b) shows the temperature imbalance mitigation between channels when the thermal coupling is controlled by using a non-uniform gap. In a uniform gap VFET, the temperature difference between the channels is up to 5K, but the VFET with non-uniform gap has a constant value of about 0.8K. Therefore, it is possible to prevent differences in performance or reliability between channels when non-uniform gap is used.

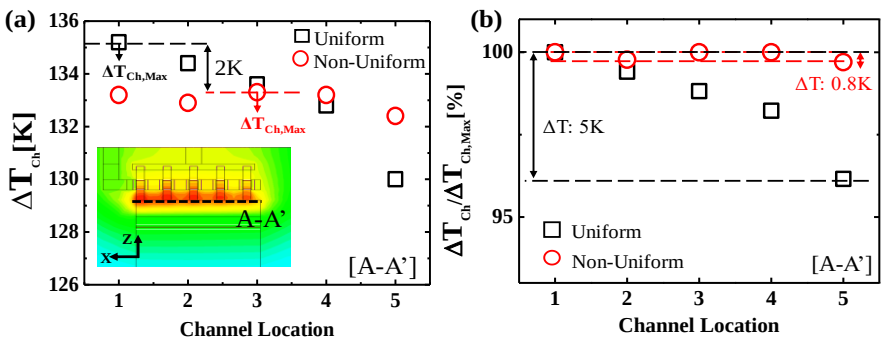



Fig. 13 (a) Temperature profiles of uniform/non-uniform gap. (b) Temperature uniformity of uniform/non-uniform gap.

## 5.8. Life time depending on various analysis conditions

The HCI/BTI lifetime of VFET can be predicted through $V_{TH} \sim \exp(-E_a/kT_{L,max}) \times t^n$. Lifetime is defined as the time to reach $V_{TH}$ = 0.1V. The $E_a$ and n of the VFET are assumed to be the same as [4], [8], [11,12]. $\tau_{300K}$ means lifetime when no temperature rises due to SH, i.e., T = 300K and $\tau$ is the lifetime for each analysis condition when the temperature rises due to SH. HCI/BTI lifetime according to various analysis conditions is confirmed. As shown in Fig. 5.14, it can be seen that the HCI/BTI life time continues to decrease due to the increase in temperature as SiCOH ILD is used and the air gap is added to SiCOH ILD than when $SiO_2$ ILD is used. In addition, it can be seen that the life time is reduced when the air spacer is used. Therefore, the conditions used for performance improvement may shorten the life time, so it would be good to consider it according to the design goal. And, as shown in the circles of the inset in Fig. 5.14, in case of uniform gap, the lifetime of each channel is different. But, if the device is made with a non-uniform gap, it can be seen that the channels have almost the same lifetime as the star symbol of the inset.

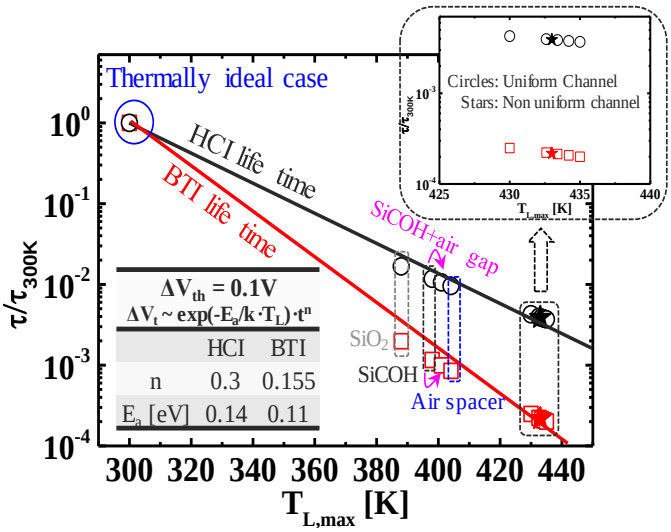



Fig. 5.14. A comparison of HCI / BTI lifetime as a function of $T_{L,max}$ according to analysis conditions.

## 5.9. Summary

Our work has analyzed the lattice temperature and $I_{on}$ degradation rate by SH in VFET. The lattice temperature (hot spot) is increased by 98K and the $I_{on}$ degradation rate is 5.5%. When using materials with low dielectric constant used to reduce parasitic capacitance in the active and BEOL area, the thermal characteristics of the device may deteriorate and the life time affected by HCI/BTI may be shortened by about 1/2 times. Therefore, it would be used carefully according to design requirements. Furthermore, in case of using multi-channel to increase $I_{on}$, temperature imbalance occurs between channels due to its structural feature. Non-uniform gap process can lower $T_{L,\ max}$ by 2K and lower the temperature imbalance between channels from 5K to 0.8K. Accordingly, the HCI/BTI lifetime of channels can be made similar.

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# Conclusions

In this dissertation, first, we have devised on shallow trench isolation (STI) design considering leakage current ($I_{OFF}$) in Bulk/silicon on insulator (SOI) FinFET and vertical FET (VFET). The $I_{OFF}$ tendency is considered in terms of the interface trap density ($D_{it}$) difference depending on the STI material type and STI thickness. In the case of Bulk FinFET, the STI design for each of high performance (HP) and low power (LP) is presented. On the other hand, in the case of SOI FinFET and VFET, STI designs which do not distinguish HP/LP are presented. Max lattice temperature ($T_{L,max}$)/thermal resistance ($R_{th}$)/on current ($I_{ON}$) degradation rate according to STI design in each structure are also analyzed. We compare the hot carrier injection (HCI)/bias temperature instability (BTI) lifetime as a function of the device temperature which is varied depending on STI design. Second, the (SHE of both dc and ac for a three-channel nanowire-field effect transistor (FET) is investigated and analyzed. In the dc mode, as $\Delta T_{max}$ (definition: $T_{max}$ −300K) increases to 65 K, the transistor suffers from an $I_{on}$ degradation of 3.8% along with a $R_{th}$ of 4.875 [K/μW]. In the ac mode, as the heating time (same as the pulse time) increases, the heat is accumulated more and the cooling time increases accordingly. It is confirmed that $\Delta T_{max}$ decreases as the device operating frequency increases and $\Delta T_{max}$ saturates to about 40 K at 4 GHz. The thermal characteristics and the lifetime are analyzed while changing the duty cycle to 25%, 50%, and 75%. It shows that $\Delta T_{max}$ increases to 38, 42, and 45 K, respectively, and HCI and BTI lifetime can be increased up

to two times and three times, respectively. Third, SHE of Gate-All-Around (GAA) nanoplate field effect transistor (FET) with variations of active area specifications including number of vertically stacked channels,metal gate thickness, and channel width, is investigated using TCAD simulations. Our research suggests that varying these architecture parameters not only affect overall performance of sub-5-nm node GAA nanoplate FET such as on-current degradation and time-delay, but also greatly impact thermal reliability such as lattice temperature and thermal resistance, which are comprehensively analyzed using the Figure of Merit (FoM). Furthermore, thermal reliability of GAA nanoplate-FET is analyzed from perspective of Hot Carrier Injection (HCI) / Bias Temperature Instability (BTI) lifetime variation using maximum lattice temperature ($T_{L,max}$) and metal gate thickness ($T_M$). Finally, SHE in newly introduced Vertical channel Field Effect Transistors (VFETs) is investigated and discussed, and several architecture parameters such as channel width, number of channels affecting thermal reliability of VFET are studied through simulations. In addition, a study on the change of thermal properties is conducted when air gap/spacer is used to reduce the influence of the parasitic capacitance. It is illustrated that VFET shows high lattice temperature and thermal resistance increase from changes in such architecture parameters, air gap in BEOL (Back End of Line), and air spacers. Additionally, the lattice temperature imbalance between channels can be mitigated by adjusting the inter-channel spacing of a multi-channel VFET.

# Appendix A. A Simple and Accurate Modeling Method of Channel Thermal Noise using BSIM4 Noise Models

## A.1 Introduction

The continuous scaling of complementary meta-oxide semiconductor (CMOS) devices has resulted in major performance improvements, and CMOS has become a viable candidate for radio frequency (RF) applications [1-3]. Thus, the accurate modeling of the channel thermal noise characteristics of CMOS RF devices is important for predicting RF circuit and system performance. This is because the thermal noise of the transistor is the largest source of noise at high frequencies [4-6], which fundamentally limits the achievable signal-to-noise ratio. The channel thermal noises of advanced devices in sub-200-nm nodes increases compared to the theoretical predictions made by the conventional models [7-8] for long channel devices, since the long channel model does not account for short channel effects, carrier heating effects [9], and velocity saturation [10-12]. Several analytical models have been proposed to predict the channel thermal noise [6, 13-15]. However, given the complexity of the equations that require voltage information on the internal nodes and externally inaccessible parameters, it is difficult for circuit designers to use these models simply in Simulation Program with Integrated Circuit Emphasis (SPICE) simulation. On the other hand, in the thermal noise model

implemented in Berkeley Short-channel IGFET Model 4 (*BSIM4*) models [16] of a process design kits (PDK), the default parameter of *NTNOI* (noise enhancement factor) [16] does not match the experimental bias dependency or the measured noise parameters in short channel devices, which can compromise simulation accuracy. In this chapter, we propose a modeling method that can be applied simply by designers and that can achieve high accuracy under various operation conditions. The primary focus is to develop and implement a model based on the measured noise parameters of a transistor. The contents of this paper are organized as follows. In Section II, the SPICE modeling process is briefly introduced in terms of the DC (*I*-*V*) and AC (*S*-/*Y*-parameters) measurements of 130-nm MOSFETs as well as their noise parameters. In Section III, we extract the *valid* noise spectral density ($S_{id}$) from the noise parameters ($NF_{min}$, $G_{opt}$, $B_{opt}$, and $R_n$) [4, 5] measured under various voltage and frequency conditions as well as different numbers of fingers for the charge-based model (when the noise model select parameter, *TNOIMOD is set 0*) in *BSIM4*. A bias-dependent empirical formula is proposed for modeling the excess noise. Then, the noise parameters are compared with the measurements obtained under various conditions to verify the accuracy of the proposed model. In addition, a modeling technique for the holistic model (*TNOIMOD = 1*) is discussed.

# A.2 Overall Schematic of the RF MOSFET Model

Throughout this paper, HSPICE (circuit simulator) [22] and a *BSIM4* (version 4.5) model were used for simulation. The device-under-test (DUT) of an n-type MOSFET with a channel length ($L_g$) of 0.13 μm and a channel width ($W_g$) of 4.5 μm was connected in a common-source configuration. All values of the model elements (capacitance, resistance, diode, etc.) in the transistor model were obtained from HSPICE simulation using BSIM4 models.

The equivalent model of a MOSFET is shown in Fig.A.1. It consists of an intrinsic MOSFET ($m_0$), intrinsic *R*'s and *C*'s, and a body *R*-*C* network ($R_{sb}$, $R_{db}$, $C_{sb}$, $C_{db}$, $R_{sub}$, $C_{sub}$). Here, $C_{gs\_fr}$ and $C_{gd\_fr}$ represent the capacitances of the sidewall spacer, and they are bias-independent elements. $R_g$, $R_s$, and $R_d$ each represent a terminal resistance. Using the body network model is necessary to achieve an accurate simulation of the output characteristics and RF noise of a MOSFET. All components of the MOSFET model were set to vary according to device specifications such as $W_g$, $L_g$, and the number of fingers (*nr*). The accuracy of the MOSFET model was verified by comparing the simulation results with the measured DC $I_{DS}$ versus $V_{GS}$ characteristics and *Y*-parameters.

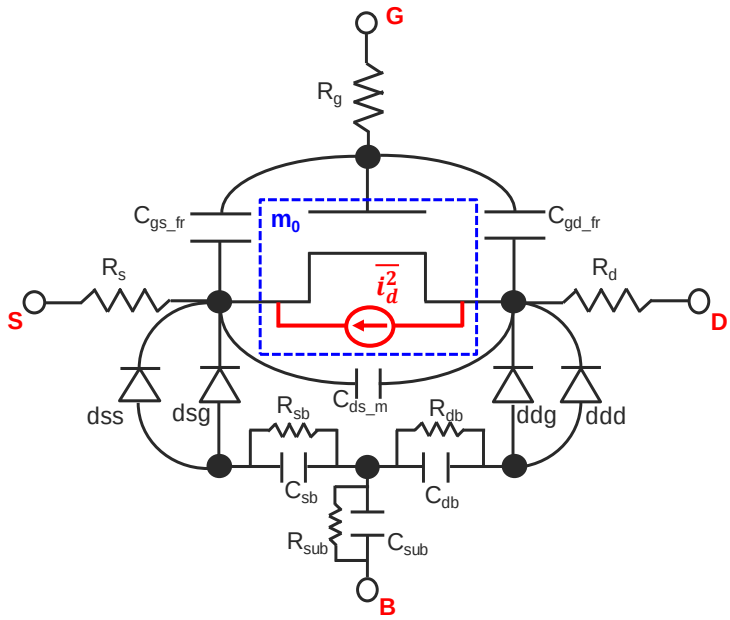


Fig. A.1 The full MOSFET model including an intrinsic MOSFET (blue box), intrinsic parasitic components, and a body *R*-*C* network.

# A.3 Verification of the DC Characteristics of the RF MOSFET Model

First, the *I*-*V* measurements were carried out with $V_{DS}$ = 1.2 V and *nr* ranging from 16 to 64. Fig.A.2 shows the measured and simulated (using the HSPICE *BSIM4* model) $I_{DS}$ versus $V_{GS}$ characteristics. Several DC parameters were used, such as low field bulk mobility (*U0*) and mobility degradation factors (*UA*, *UB*, *UC*, *etc*.). Other parameters were also used, including saturation velocity (*VSAT*), *ETA* for the threshold voltage, *NFACTOR* for subthreshold swing, *PCLM* for the length modulation equation, and both

*RDSW* and *PRWG* for the $R_{ds}$ [16], a gate bias dependent resistor in the lightly doped drain (LDD) region. The remaining DC model parameters were set to default values provided by the foundry. As shown in Fig. A.2, the MOSFET model fits well with the measured $I_{DS}$ versus $V_{GS}$ for different *nr*.

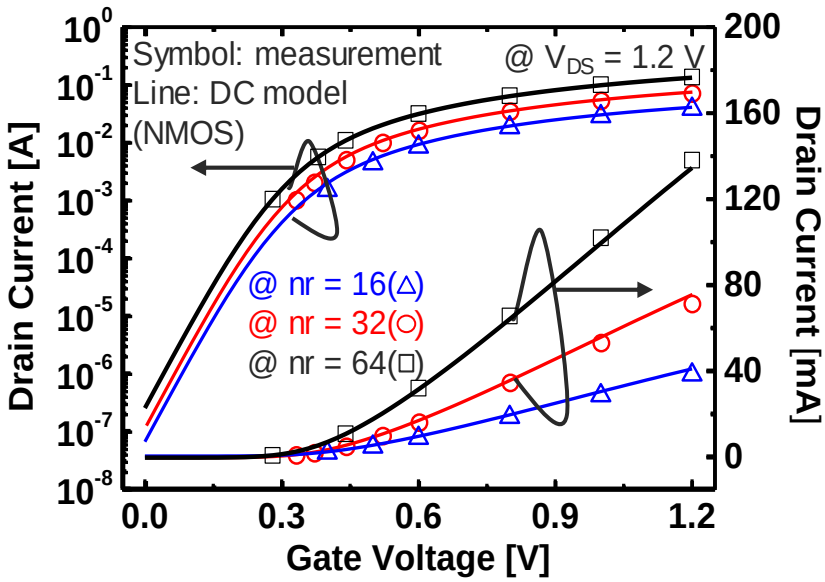


Fig. A.2 Measured and simulated $I_{DS}$ versus $V_{GS}$ characteristics of 4.5 μm/0.13 μm n-type MOSFETs biased in strong inversion region under $V_{DS}$ = 1.2 V with the number of fingers (*nr*) of 16, 32, or 64.

# A.4 Verification of the MOSFET Model with Measured Y-parameters

Secondly, *S*-parameters were measured for various bias conditions, frequencies, and *nr* ranging from 16 to 64. Then, the *S*-parameters were mathematically converted to *Y*-parameters using conversion equations (1) ~ (4) [17]. The simulated *Y*-parameters of the MOSFET from HSPICE are shown in Fig. A.3. The figure shows the characteristics of the measured and simulated *Y*-parameters when $nr$ = 64 and $I_{DS}$ = 2 mA. The results indicate that the simulated and measured *Y*-parameters accurately match under all bias conditions.

$$y_{11} = \frac{(1 - s_{11})(1 + s_{22}) + s_{12}s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \tag{1}$$

$$y_{12} = \frac{-2s_{12}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \tag{2}$$

$$y_{21} = \frac{-2s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \tag{3}$$

$$y_{22} = \frac{(1 + s_{11})(1 - s_{22}) + s_{12}s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \tag{4}$$

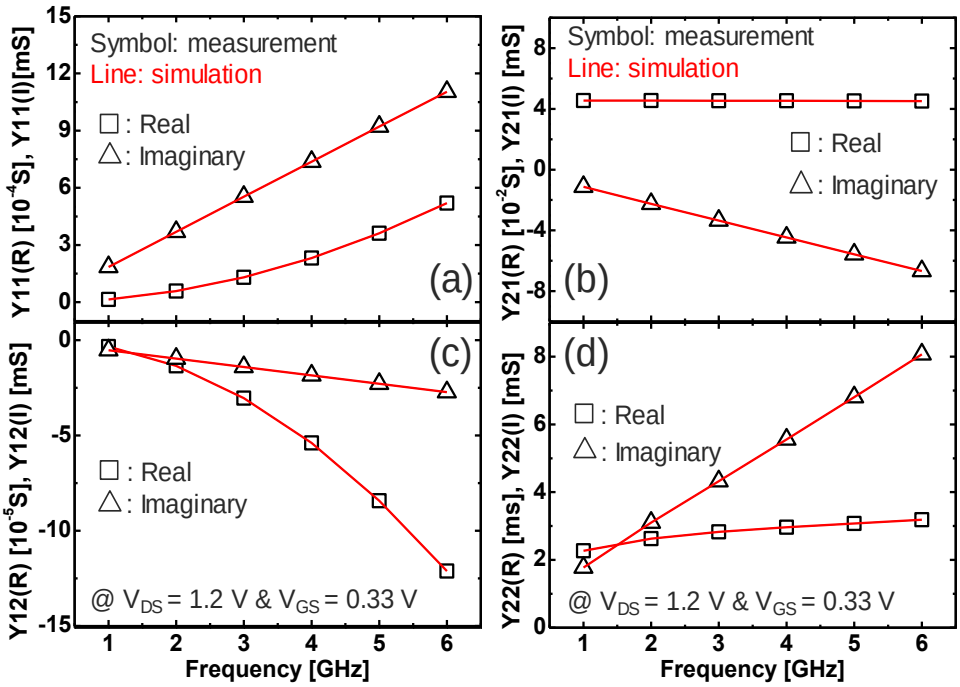


Fig. A.3. Converted *Y*-parameters (symbol) from the measured *S*-parameters and simulated (line) *Y*-parameters of the MOSFET biased at $I_{DS}$ = 2.0mA. ($V_{DS}$ = 1.2 V and $V_{GS}$ = 0.33 V and *nr* = 64). Real and imaginary of (a) *Y*11 (b) *Y*21 (c) *Y*12 (d) *Y*22 are shown.

# A.5 Verification of the MOSFET Model with Measured Noise Parameters

In the previous sections, we confirmed that the MOSFET model fits well to both *I-V* and *Y*-parameters. In this section, the results of the noise parameter simulation using the

charge-based channel thermal noise model (*TNOIMOD = 0*) implemented in *BSIM4* [16] are discussed. This model (*TNOIMOD = 0*) is given by (5) and (6) [16], and *NTNOI*, a noise enhancement factor, which is equivalent to γ, has the default value of 1. The other parameters of *W*, *L*, $C_{ox}$ and $R_{ds}$ are the same as they were in previous settings.

$$S_{id} = \frac{4 \cdot k_B \cdot T \cdot \Delta f}{\left( R_{ds} + \frac{L^2_{eff}}{\mu_{eff} \cdot |Q_{inv}|} \right)} \cdot NTNOI = 4kT \cdot G_{do} \cdot \gamma \tag{5}$$

$$Q_{inv} = W_{active} \cdot L_{active} \cdot C_{oxeff} \cdot NF \cdot \left( V_{gsteff} - \frac{A_{bulk} \cdot V_{dseff}}{2} + \frac{A^2_{bulk} \cdot V^2_{dseff}}{12 \cdot (V_{gsteff} - \frac{A_{bulk} \cdot V_{dseff}}{2})} \right) \tag{6}$$

Fig. A.4 shows the measured and simulated noise figure parameter data. While the accuracies of the *I-V* and *Y*-parameters were respectively verified in Section II B and C, the default *NTNOI* is not suitable for fitting the measured noise parameters. The *NTNOI* value of about 1.52 is required to match the measured data when *nr* =64 and $V_{GS}$ =0.33 V. In addition, different *NTNOI* values are required for different bias conditions. Many previous studies [3, 5-7, 14, 15, 21] have modeled *γ*, a thermal noise enhancement factor, as bias dependent, implying that *NTNOI*, which is the same as *γ*, should be dependent on bias. Therefore, the next chapter introduces a series of procedures that are used to model the bias-dependent *NTNOI*, and also verifies with measured noise data

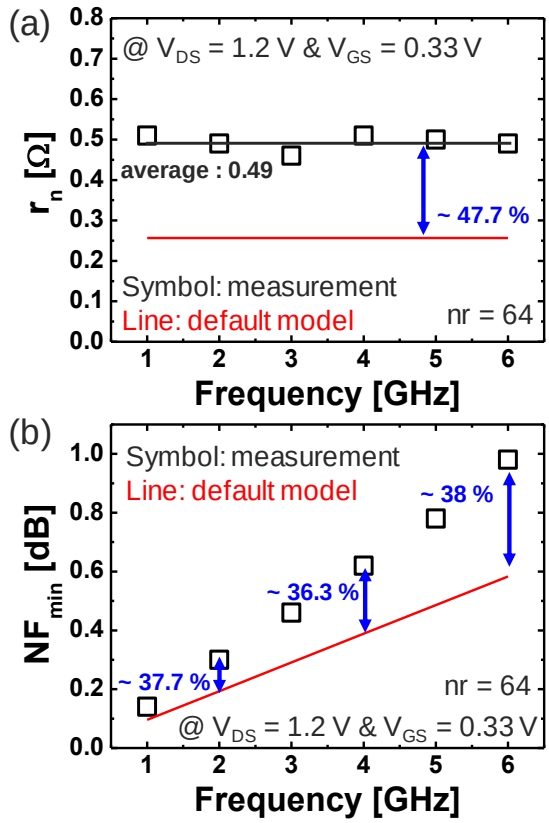


Fig. A.4. Comparison of the measured (symbols) and *BSIM4*-simulated (lines) (a) $r_n$ and (b) $NF_{min}$ both at *V*DS = 1.2 V and *V*GS = 0.33 V. For simulation, the default model (*TNOIMOD* = 0 using *NTNOI* = 1) was used.

# A.6 Thermal Noise Extraction and Modeling (TNOIMOD = 0)

The modeling sequence that consists of five steps is described in detail in Fig. A.5. For RF noise modeling, it is imperative that the measured data be accurately

de-embedded parasitics associated with interconnection lines, vias, and pad structures. Accordingly, the de-embedding process must be conducted in Step 1. Then, in Step 2, the SPICE model parameters (e.g. *BSIM*) is fitted to the measured *S*-parameters. In this work, the open-short method was used for de-embedding [18-20], and it shows a good match between the de-embedded measured and the PDK-simulated Y-parameters (see Fig. A.3).

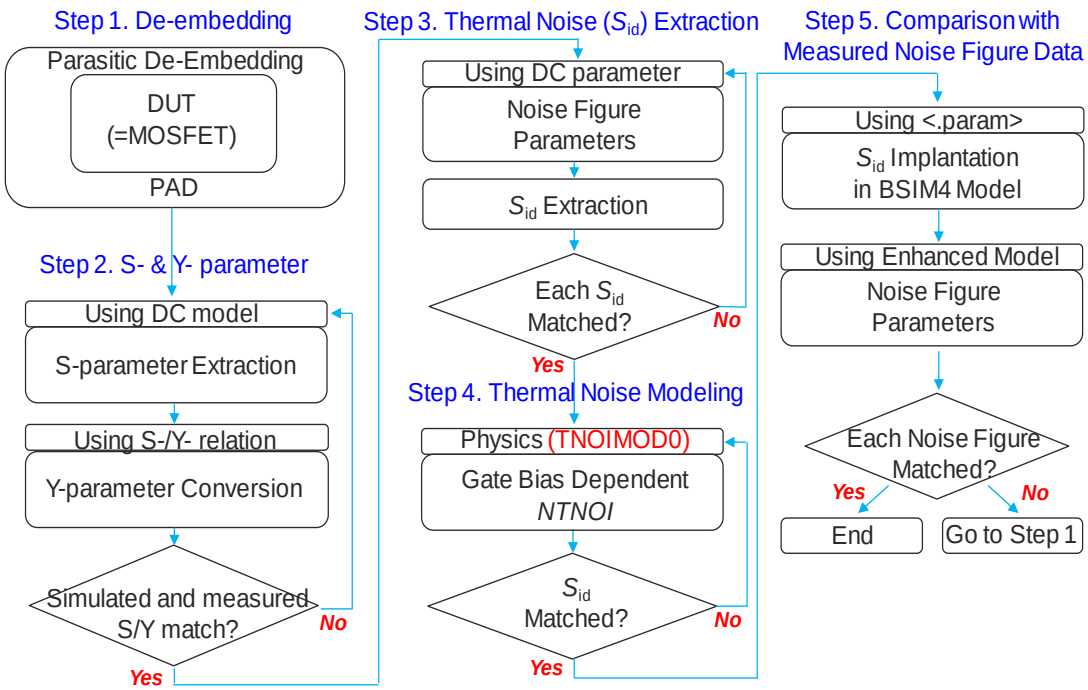


Fig. A.5. Procedure diagram of thermal noise and noise parameter modeling.

We extracted the $S_{id}$ from the noise figure data, using (7) ~ (10) [5]. Each analytical equation consists of *Y*-parameters, $R_g$, and DC parameters. In (7) ~ (10), $\chi$ represents [$G_{do}$ x *NTNOI*]. Therefore, since the measured noise figure, *Y*-parameter, and $R_g$ are all given,

$\chi$ can be extracted from each equation. Then, multiplying $\chi$ by $4kT$ [5] yields $S_{id}$, where $kT$ is the thermal energy.

$$R_n (= r_n \times 50) = R_g + \frac{\chi}{|Y_{21}|^2} \tag{7}$$

$$\mathrm{Re}\{Y_{opt}\} = G_{opt} = \frac{|Y_{11}||Y_{21}|\sqrt{\chi \cdot R_g}}{R_g \cdot |Y_{21}|^2 + \chi} \tag{8}$$

$$\mathrm{Im}\{Y_{opt}\} = B_{opt} = \frac{-\chi \cdot \mathrm{Im}[Y_{11}]}{R_g \cdot |Y_{21}|^2 + \chi} \tag{9}$$

$$NF_{\min} = 1 + \frac{2}{|Y_{21}|^2}\left\{|Y_{11}||Y_{21}|\sqrt{\chi \cdot R_g} + \mathrm{Re}[Y_{11}] \cdot \chi\right\} \tag{10}$$

Often, high-frequency noise-figure data show fluctuations that are attributable to the influence of the varied measurement environment. Therefore, it is important to assess the reliability of the $\chi$ value extracted from each noise parameter. Fig. A.6 (a) - (d) shows equations (7) - (10) expressed in terms of $Y$-parameter values and $R_g$ values when $nr$ = 32, frequency = 1GHz, $V_{GS}$ = 0.33 V, and $V_{DS}$ = 1.2 V. The general solution of $\chi$, which is always real and positive, can be expressed in terms of $Y$-parameters and $R_g$ (as represented by blue letters and lines in Fig. A. 6. In addition, the gray box in the Fig. A.6 shows the variation in the measured data.

Fig. A.6 (a) shows the $G_{opt}$ expression. In the ase of $G_{opt} > |Y_{11}|/2$, the ideal value of $G_{opt}$, the $\chi$ solution cannot be obtained from the measured $G_{opt}$ value. If $G_{opt} < |Y_{11}|/2$, two $\chi$ solutions are obtained from the measured $G_{opt}$ value. Fig. A.6 (b) shows the $B_{opt}$ expression. Most of the measured $B_{opt}$ values are greater than $-\mathrm{Im}\{Y_{11}\}$. In this case, one $\chi$ solution can be obtained from the measured $G_{opt}$ value. However, since the slope of the function is near zero, even if $B_{opt}$ is measured to be slightly different from the ideal value, the $\chi$ solution will be more than 10 times greater than the correct solution. In addition, some $B_{opt}$ have a value under $-\mathrm{Im}\{Y_{11}\}$, resulting in negative $\chi$, which is physically contradictory. On the other hand, Fig. A.6 (c) shows the $R_n$ expression. It should be noted that $R_n$ is a linear function, and the measured data set is always greater than $R_g$. Hence, even if $R_n$ has some variation, $\chi$ does not change substantially. Therefore, a $\chi$ solution that is reliable can always be obtained from the measured $R_n$. Lastly, Fig. A.6 (d) shows the $NF_{min}$ expression. Similar to the $R_n$ function, one reliable $\chi$ can be extracted from the measured $NF_{min}$. Table A.1 presents a description of the reliability of $\chi$ extracted from four noise-figure parameters.

The values of $S_{id}$ extracted from $R_n$ and $NF_{min}$ are almost similar within a 1 % error. In the subsequent modeling steps, the average value of $S_{id}$ was used. As will be discussed later, both $G_{opt}$ and $B_{opt}$ can be accurately calculated from $S_{id}$ extracted from two other reliable noise-figure parameter ($R_n$ and $NF_{min}$).

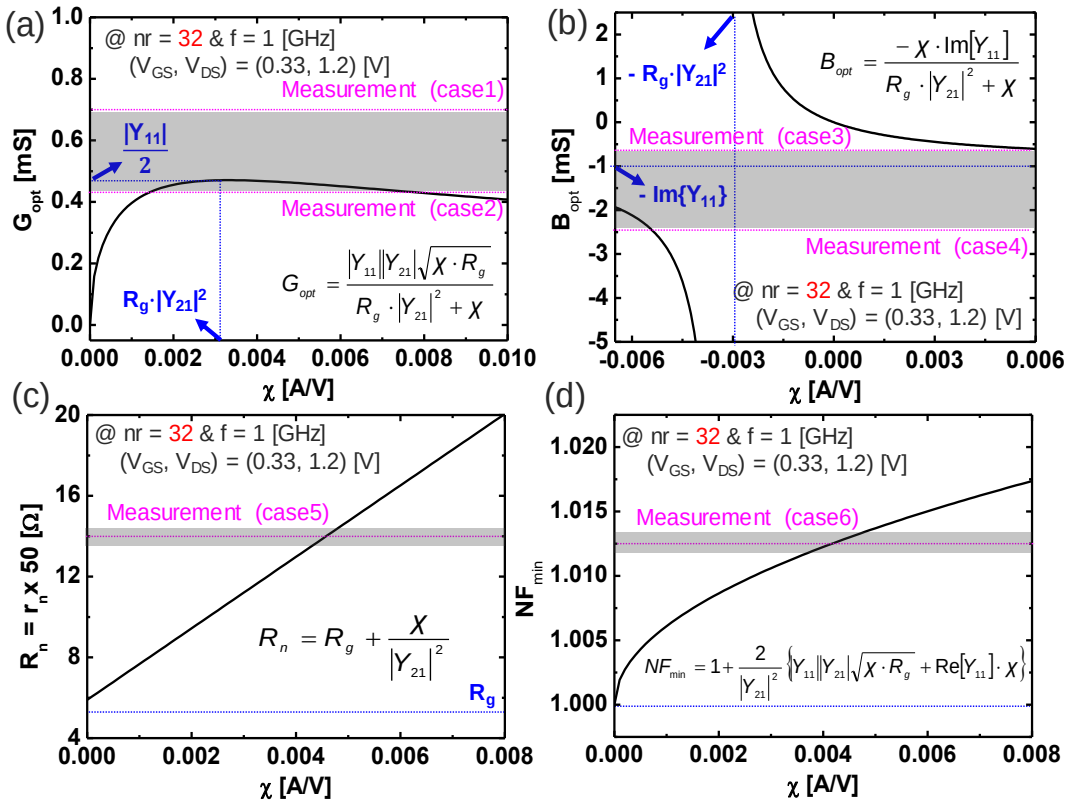


Fig. A.6. Plots for describing the reliability of $\chi$ solutions extracted from the measured noise parameters (a) $G_{opt}$ (b) $B_{opt}$ (c) $R_n$ (d) $NF_{min}$. The gray box in the figures shows the variation of the measured data.

Table A.1

Reliability of Extracted $\chi$ from Noise Figure Parameters

| Noise Figure Parameters | Case | Measured Data Range | $\chi$ Solution | Reliability |
|---|---|---|---|---|
| $G_{opt}$ | 1 | $G_{opt} > \|Y_{11}\|/2$ | No solution | Very low |
| | 2 | $G_{opt} < \|Y_{11}\|/2$ | Two solution (surjective) | Very low |
| $B_{opt}$ | 3 | $B_{opt} > -\mathrm{Im}\{Y_{11}\}$ | Highly variable solution | low |
| | 4 | $B_{opt} < -\mathrm{Im}\{Y_{11}\}$ | Negative solution (physical contradiction) | Extremely low |
| $R_n$ | 5 | $R_n > R_g$ | One to one mapping (bijective) | Very high |
| $NF_{min}$ | 6 | $NF_{min} > 1$ | One to one mapping (bijective) | High |

Fig. A.7 shows the $S_{id}$ extracted using the method described earlier. The symbol represents the average value of $S_{id}$ extracted from the measured data, red box for $nr$ = 64, and black box for $nr$ = 32. The lines show the value obtained from the MOSFET model using *TNOIMOD = 0*, the charge-based thermal noise model, with *NTNOI* set at a default value of 1. As shown in Fig. A.7, the value of $S_{id}$ reproduced by the model is insufficient compared to $S_{id}$ from the measured noise parameter data under different drain current, $I_{DS}$ (or the gate voltage, $V_{GS}$). As expected, the *NTNOI* values for fitting the measured $S_{id}$ are bias-dependent.

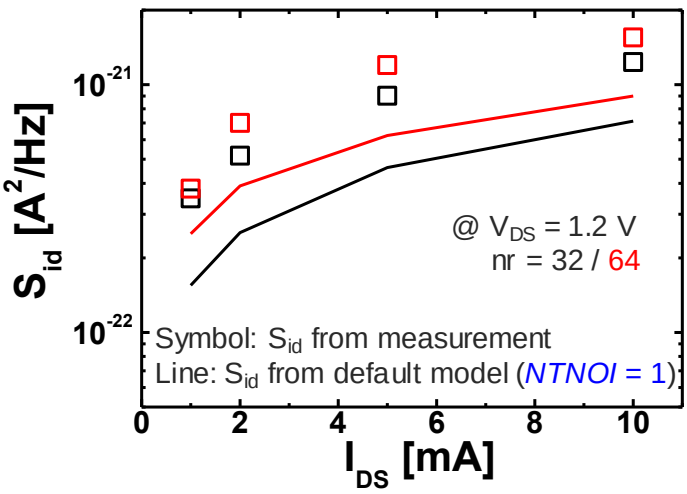


Fig. A.7 Channel thermal noise versus $V_{GS}$ (= $I_{DS}$) of MOSFETs with different finger number, *nr* = 32 / 64. Symbols and lines represent the $S_{id}$ extracted from the measured $r_n$ & $NF_{min}$ data and $S_{id}$ of the default model, respectively.

As shown in Fig. A.8, the black box symbol represents the *NTNOI* value for fitting the measured $S_{id}$ from low to high biases. In addition, the circle symbols are taken from [21] and reproduced here for comparison. This shows the required noise enhancement factor for all bias conditions from 200 nm to 40 nm nodes. Compared with the data in [21], the extracted *NTNOI* value is confirmed to be reasonable for the given node. The black line represents the model to fit the required *NTNOI* values for the overall bias conditions. The enhanced *NTNOI* model equation and parameters for the 130 nm node MOSFET are summarized in Table A.2.

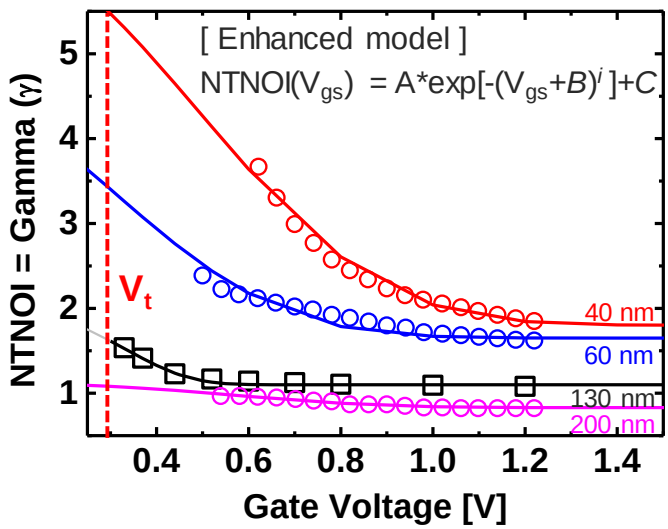


Fig. A.8 Extracted (black box symbol) and modeled (lines) *NTNOI* value versus $V_{GS}$ in saturation region under $V_{DS}$ = 1.2 V. The various circle symbols are shown, after [21]. It is shown that extracted *NTNOI* value is reasonable considering the γ values in [21].

The enhanced *NTNOI* model is expressed as a function of gate voltage. Those parameters are not derived from device physics, thereby presenting no correlation with physical meaning. However, the proposed formula has a simple functional form, which can cover the required NTNOI not only for different gate voltages, but also for various technology nodes. For a given tech node, the role of parameters *A* and *C* is to determine the maximum and the minimum range of NTNOI, while *i* adjusts the sensitivity of NTNOI at low gate bias and *B* reflects the changes in $V_t$. Thus, by adjusting the parameter set, designers can easily reproduce NTNOI values for each bias and node. The solid lines in Fig. A.8 illustrate the proposed model's flexibility and reproducibility. The gate-bias-dependent enhanced *NTNOI* model can be implanted into *TNOIMOD = 0* by

using *Verilog-A*. Typically, however, modifying the model through *Verilog-A* involves a complicated process and often slows down the simulation. Therefore, in our implementation, the model equation and parameters were declared through <.*param*>, a command in HSPICE, and the simulation was performed quickly.

Table A.2

Modified *BSIM*4 Thermal Noise Model Parameters for 130 nm MOSFETs

| **Charge-based model (TNOIMOD0) parameter set [ $S_{id}$ error rate: 1 % ]** | | | | | | | |
|---|---|---|---|---|---|---|---|
| $NTNOI(V_{gs}) = A \cdot \exp[-(V_{gs}+B)^i]+C$ | | | | | | | |
| ***A*** | **1.0** | ***B*** | **0.65** | ***i*** | **8** | **C** | **1.0** |
| **Holistic model (TNOIMOD1) parameter set [ $S_{id}$ error rate: 1.5 % ]** | | | | | | | |
| $\beta_{tnoi}$ | **Default** | **Modified** | $\theta_{tnoi}$ | **Default** | **Modified** | | |
| **RNOIA** | **0.577** | **0.8** | **RNOIB** | **0.37** | **0.37** | | |
| **TNOIA** | **1.5e6** | **2.7e7** | **TNOIB** | **3.5e6** | **3.5e6** | | |

Fig. A.9 shows the accuracy of the enhanced *NTNOI* model for both *nr* = 32 and 64. The figure shows that the measured and simulated $S_{id}$ are well fitted. Note that the enhanced *NTNOI* model can reproduce $S_{id}$ of all *nr* using the same parameter values.

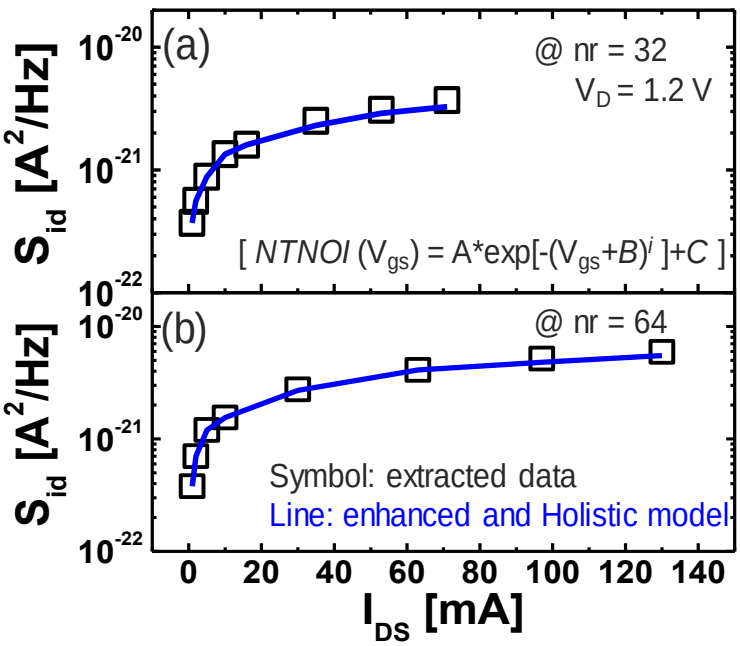


Fig. A.9 Channel thermal noise versus $V_{GS}$ (= $I_{DS}$) of MOSFETs with different finger number, (a) *nr* = 32 (b) *nr* = 64. Symbol and line represent the $S_{id}$ extracted from the measured $r_n$ & $NF_{min}$ data and $S_{id}$ of the enhanced models respectively.

# A.7 Verification of the Enhanced Model with Noise Parameters

We simulated the noise figure parameters using the enhanced *NTNOI* model. Since there are multiple measurement data sets, we have constructed them in Fig. A.10 to compactly show that the enhanced model fits well for all cases. Fig. A.10 (a) shows $r_n$ in all *nr* cases when the frequency is 4GHz. While the error rate varies slightly depending on *nr*, for $R_n$, the maximum error rate is reduced from 41 % down to only about 4 % when

the enhanced model is used. Fig. A.10 (b) shows $NF_{min}$ at $nr$ = 64 when the frequency is 4 GHz, and it can also be seen that the accuracy is improved by the enhanced model. Fig. A. 10 (c) and (d) show both $G_{opt}$ and $B_{opt}$ versus frequency, and they show low and high bias conditions, respectively. Therefore, the reproducibility for all noise parameters is greatly improved by the enhanced model for different *nr*, frequency, and bias.

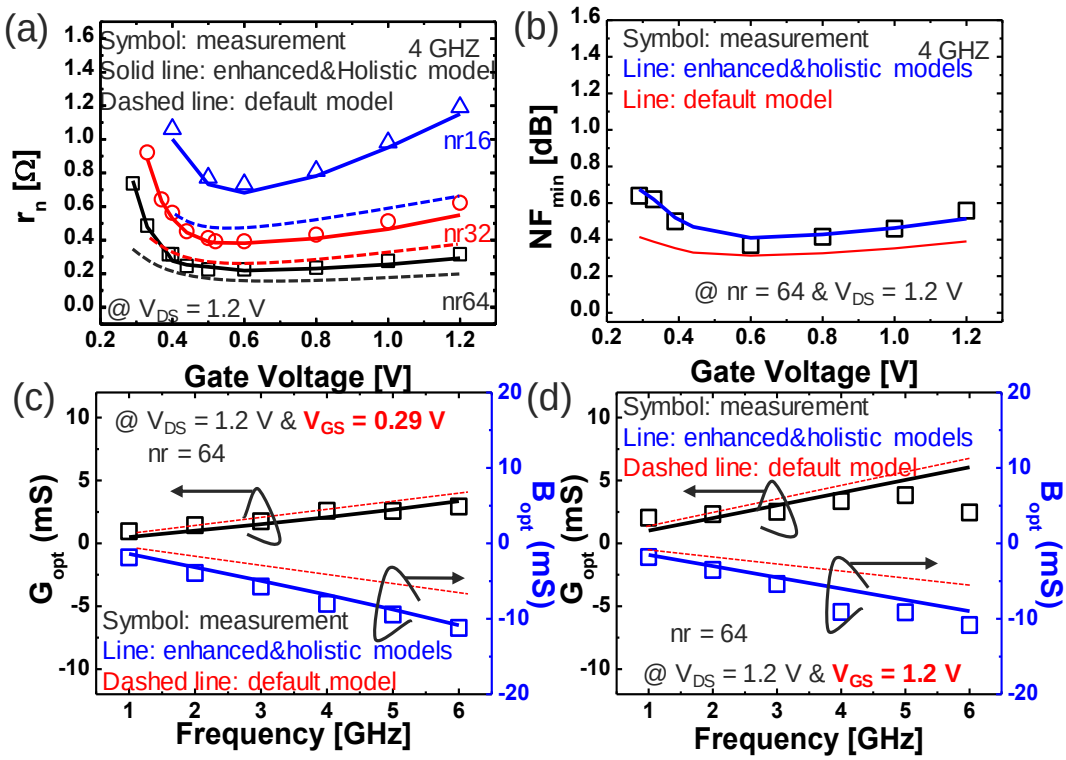


Fig. A.10 Comparison of measured noise parameters (symbol) and *BSIM*4 simulation using default (dash lines) and modified (solid lines) thermal noise models. (a) $r_n$ according to finger number (b) $NF_{min}$ according to $V_{GS}$ (c) $G_{opt}$ & $B_{opt}$ according to frequency at low $V_{GS}$ and (d) $G_{opt}$ & $B_{opt}$ according to frequency at high $V_{GS}$.

# A.8 Holistic Model (TNOIMOD = 1)

In this section, a modeling technique using *TNOIMOD = 1* is discussed. The holistic model is given as (11) ~ (13) [16], and four fitting parameters are used: *RNOIA*, *TNOIA*, *RNOIB* and *TNOIB*.

$$S_{id} = \frac{4 \cdot k_B \cdot T \cdot \Delta f}{I_{ds}} \cdot \left[ (G_{ds} + \beta_{tnoi}(G_m + G_{mbs}))^2 - \theta_{tnoi}{}^2 (G_m + G_{mbs} + G_{ds})^2 \right] \tag{11}$$

$$\beta_{tnoi} = RNOIA \cdot \left[ 1 + TNOIA \cdot L_{eff} \left( \frac{V_{gsteff}}{E_{SAT} \cdot L_{eff}} \right)^2 \right] \tag{12}$$

$$\theta_{tnoi} = RNOIB \cdot \left[ 1 + TNOIB \cdot L_{eff} \left( \frac{V_{gsteff}}{E_{SAT} \cdot L_{eff}} \right)^2 \right] \tag{13}$$

Here, *RNOIA* and *TNOIA*, which are factors for channel thermal noise, are mainly optimized, while *RNOIB* and *TNOIB*, which are induced gate noise correlation factors, make little contribution to the overall $S_{id}$ change. Some versions of the *BSIM* manual have default values of 1.5 and 3.5 for *TNOIA* and *TNOIB*, respectively, while other versions have $1.5 \times 10^6$ and $3.5 \times 10^6$ by default. The set of constants multiplied after *TNOIA* and *TNOIB* in (12) and (13), respectively, are about $1 \times 10^{-7}$. Therefore, the latter is suggested to be correct. Based on these investigations, we optimized the *RNOIA* and *TNOIA* to match $S_{id}$ first. As shown in Fig. A.9, the accuracy for the $S_{id}$ is found to be similar to that

of the enhanced *NTNOI* model. In addition, as shown in Fig. A.10, the model accuracy for the noise figure parameters is also very close to the enhanced model. The holistic model parameter values are summarized in Table A.2. If holistic model is required to use, adjusting both *RNOIA* and *TNOIA* to appropriate values will result in an accurate thermal noise component.

# A.9 Evaluation the validity of the model

we evaluate the validity of the model for drain bias. The effect of channel length modulation is applied in *I-V* model and $L_{eff}$ in eq. (5). Eq. (A.1) is the *I-V* model of *BSIM4* [16], and the $C_{clm}$ term in eq. (A.1) represents channel length modulation (CLM). Eq. (A.2) represents the $C_{clm}$ of *BSIM4* [16]. Many of the parameters are described in the *BSIM4* manual, so there are only two important expressions:

$$I_{ds} = \frac{I_{ds0} \cdot NF}{1 + \frac{R_{ds} \cdot I_{ds0}}{V_{dseff}}} \cdot \left[ 1 + \frac{1}{C_{dm}} \cdot \ln\left( \frac{V_A}{V_{Asat}} \right) \right] \times \left( 1 + \frac{\Delta V_{ds}}{V_{ADIBL}} \right) \cdot \left( 1 + \frac{\Delta V_{ds}}{V_{ADITS}} \right) \cdot \left( 1 + \frac{\Delta V_{ds}}{V_{ASCBE}} \right) \tag{A.1}$$

$$C_{dm} = \frac{1}{PCLM} \cdot F \cdot F_{PVAG} \cdot \left( 1 + \frac{R_{ds} \cdot I_{ds0}}{V_{dseff}} \right) \cdot \left( L_{eff} + \frac{V_{dsat}}{E_{sat}} \right) \cdot \frac{1}{l_{itl}} \tag{A.2}$$

$$\Delta L_{dm} = l_{itl} \cdot \ln\left(\frac{V_{ds} - V_{dsat} / l_{itl}}{E_{SAT}}\right) \qquad \text{(A.3)}$$

Fig. A.11 shows the measured and simulated (using the HSPICE *BSIM4* model) $I_{DS}$ versus $V_{GS}$ characteristics. It can be seen that the model reproduces well for measured data that showing increasing trends by CLM. Eq. (A.3) is the *BSIM* equation [16], which represents the channel length variation due to channel length modulation, and is reflected in $L_{eff}$ of eq. (5). Fig. A. 12 shows the $S_{id}$ of the model according to the drain bias, and it can be seen that model is reasonable compared with data in [5].

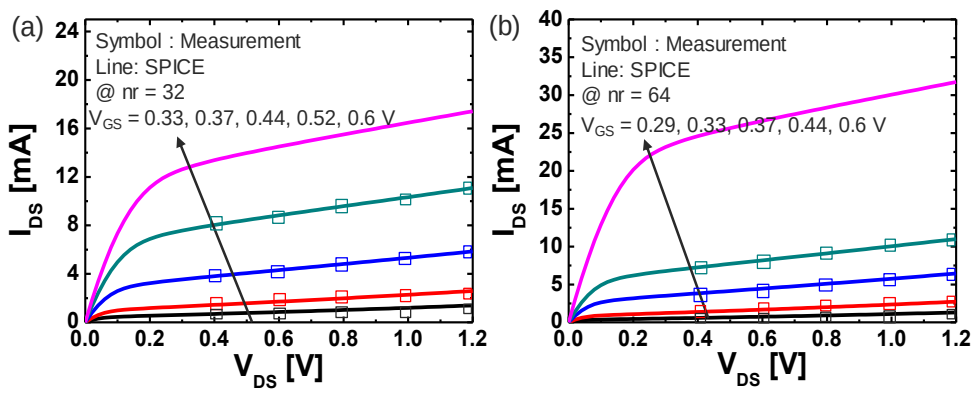


Fig. A.11 Measured and simulated $I_{DS}$ versus $V_{DS}$ characteristics of 4.5 μm/0.13 μm n-type MOSFETs with the number of fingers of (a) 32, or (b) 64.

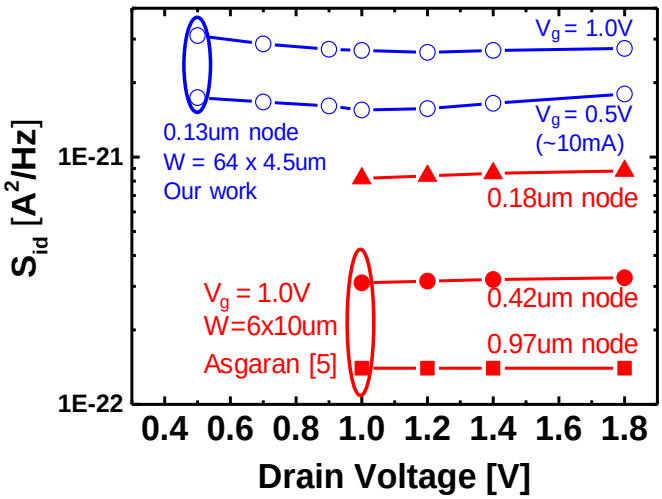


Fig. A.12 Channel thermal noise versus $V_{DS}$ of MOSFETs with *nr* = 64. Blue represents the $S_{id}$ from the enhanced model and red represent the $S_{id}$ from [5].

# A.10 Conclusion

In this chapter, a simple and effective method for the SPICE compact modeling of thermal noise is presented. Analytical expressions for MOSFETs' noise parameters such as $R_n$ and $NF_{min}$ were used to extract the spectral density of thermal noise. In order to match the noise spectral density obtained from measurement and SPICE simulation, we modeled the excess noise factor '*NTNOI*' in the charge-based model. Gate-bias-dependent *NTNOI* is implanted in the SPICE model, and it was shown to be consistent with the measured noise parameters. We also matched noise spectral density using the holistic model, and then the noise parameters were well-matched. Both the charge-based model and the holistic model were found to be suitable for matching noise

spectral density and noise parameters. This method can also be applied to other node devices by adjusting the coefficients of the *NTNOI* equation (*A*, *B*, C, and *i*) in the former or the fitting parameters (*RNOIA*, *RNOIB*, *TNOIA*, and *TNOIB*) in the latter. It is expected that modeling time and effort can be significantly reduced while keeping the high accuracy of the compact model for sub-micron MOSFETs through the use of these simple modeling steps.

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# 초 록

이 논문에서는 다양한 Sub-10nm 노드 전계 효과 트랜지스터 (FET)에서 TCAD 시뮬레이션을 사용하여 자체 발열 효과 (SHE)를 조사합니다. 노드가 감소함에 따라 논리 장치는 Fin-FET 에서 Nanosheet-FET 로 3D MOSFET 구조로 진화했습니다. 3D MOSFET 의 경우 ⅰ) 채널의 전력 밀도가 높음, ⅱ) SiO2 로 둘러싸인 채널 구조, ⅲ) 축소로 인해 전체적으로 낮은 열전도 특성 등 다음과 같은 이유로 열 신뢰성 문제가 있습니다. 한편, 많은 논문이 device 에서 SHE 에 의한 온도 상승의 분석 및 예측을 소개하지만 온도 상승 완화의 내용을 제시하는 논문은 거의 없습니다. 따라서 Fin-FET 의 STI (Shallow Trench Isolation) 구성 공학, nanowire-FET 의 DC / AC / 듀티 사이클에 따른 열 분석, nanosheet-FET 에서 소자의 중요영역(예: 게이트 금속 두께, 채널 폭, 채널 번호 등)의 최적화를 통해서 최대 격자 온도 ($T_{L,max}$)를 낮추는 방법등을 연구했습니다. 또한 더 나아가서 HCI (Hot Carrier Injection) / BTI (Bias-Temperature Instability)의 영향을 받는 수명도 제시된 다양한 열 완화 방법에 따라 분석하여 소자의 제작에 있어 열적 특성과 수명을 좋게 만드는 지표를 제시합니다 .

**주요어** : 자기 열 발생 효과, 열 저항, 온도, 시간지연, 전압-온도 불안정성 (BTI), 열 전자 효과 (HCI).

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