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Nanostructures for Local Electric Field Enhancement in Electronic Devices

전자 장치 내 국부적 전계 향상을 위한
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Abstract

The goal of this dissertation is to investigate effect of nanostructures for local electric field enhancement in electronic devices and to provide experimental and theoretical bases for their practical use. Resistive random access memory (RRAM) is a data storage device that can be modulated its resistance states by external electrical stimuli. The electric field generated by the applied potential difference between the two electrodes acts as the driving force to switch the resistance states, so controlling the electric field within the device can lead to improved operational performance and reliability of the device. Even though considerable progress has been made through significant efforts to control the electric field within the device, selectively enhancing the electric field in the intended position for stable and uniform resistive switching behavior is still challenging.

Engineered metal structures in the RRAM can efficiently manipulate the electric field. As the radius of the metal structures decreases, the charge density increases, generating electric field enhancements in confined region. To minimize the radius of the metal structure and thus to greatly increase the electric field in a local area, we introduced a nanoscale metal structure into the RRAM.

First, pyramid-structured metal electrode with a sharp tip was used to achieve a tip-enhanced electric field, and the effect of the enhanced electric field on the resistive switching behaviors of the device was investigated. Based on numerical simulation and experimental results, we confirmed that pyramidal electrode with a tip radius of tens of nanometers can selectively enhance the electric field at the tip. The tip-enhanced electric field can facilitate the thermochemical reaction in transition metal oxide-based RRAMs and efficiency of charge injection and transport in organic-based RRAMs, as well as provide position selectivity during formation of conductive filament. The resulting RRAM exhibited reliable resistive switching behavior and highly improved device performance compared with conventional RRAM with planar electrode.

As another approach to enhance the electric field within the resistive switching layer, we prepared spherical nanostructures via self-assembled block copolymer (BCP)/metal compound micelles. BCP and metal precursors were dissolved in aqueous media for use as BCP/metal compound micelles. These micelles were used as complementary resistive switch (CRS) layers of the memory device and the mechanism of CRS behavior was investigated. The spherical metal nanostructures can improve the electric fields, promoting a resistive switching mechanism based on electrochemical metallization. The

resulting CRS memory exhibited reliable resistive switching behavior with four distinct threshold voltages in both cycle-to-cycle and cell-to-cell tests. Also, the conduction and resistive switching mechanism are experimentally demonstrated through the the analysis of the current–voltage data plot and detemination of the temperature coefficient of resistance.

Overall, we pursued efficient engineering of metal nanostructures capable of manipulating electric fields for improving the operational performance and reliability of memory devices. There is no doubt that the commercialized RRAM will become popular in the near future after overcoming all the challenges of RRAM through continuous interest and research. We believe that these results will not only contribute to the significant advancement of all electronic devices, including RRAM, but will also help promote research activities in the electronic device field.

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Abbreviation and Nomenclature

AFM   atomic force microscopy

BCP   block copolymer

BE   bottom electrode

BPDA-PPD   poly(3,3′,4,4′-biphenyltetracarboxylic   dianhydride-*co*-1,4-phenylenediamine)

C-AFM   conductive atomic force microscopy

CF   conductive filament

CRS   complementary resistive switch

CuCl$_2$ copper(II) chloride

DC   direct current

ECM   electrochemical metallization

EDS   energy dispersive X-ray spectroscopy

FIB   focused ion beam

HRS   high resistance state

I–V   current-voltage

KOH   potassium hydroxide

LRS   low resistance state

NMP   N-methyl-2-pyrrolidone

P-F	Poole-Frenkel
PI	polyimide
PR	photoresist
PS-*b*-P2VP	polystyrene-*b*-poly(2-vinylpyridine)
RIE	reactive-ion etching
RRAM	random access memory
SCLC	space-charge limited current
SEM	scanning electron microscopy
STEM	scanning transmission electron microscopy
TCM	thermochemical mechanism
TCR	temperature coefficient of resistance
TE	top electrode
TEM	transmission electron microscopy
XPS	X-ray photoelectron spectroscopy

Chapter 1. Introduction

1.1. Background

1.1.1. Necessity of new memory devices

Information and communication technology (ICT) is an essential science technology for realizing and leading fourth industrial revolution [1]. ICT has been advanced significantly based on emerging technologies such as artificial intelligence (AI), big data, Internet of Things (IoT), and cloud computing. The innovation of the technologies for a fully realized industrial revolution can be achieved through digital transformation in which offline information is digitized, and successful digital transformation requires high-performance media capable of processing and storing enormous volumes of data [2]. Digital transformation has presented new possibilities of computing technology, but it has also brought limitations to conventional semiconductors and computing. One of the limitations is the von-Neumann bottleneck (a phenomenon that computer system throughput is limited due to the relative ability of processors compared to top rates of data transfer) caused by the current computer architecture, the von-Neumann architecture (Figure 1.1.) [3]. The serial processing between multiple memory devices causes the serious bottleneck when executing high-speed parallel operation that are recently required.

To solve this problem, an innovative memory/storage hierarchy that adds an acceleration processor specialized for specific data operations to existing hierarchy has been proposed [4]. For this, the need for research and

development of new memory devices has emerged [5]. The new memory devices must meet all three functional elements of the memory: density, non-volatility, and speed (Figure 1.2.). Furthermore, characteristics of low power consumption, excellent durability, and compatibility with existing semiconductor manufacturing process systems are also required. Considering the characteristics required for the functional elements, the new memory devices are used as a storage class memory (SCM) or persistence memory to improve the volatile characteristics of dynamic random-access memory (DRAM) and the inefficiency of the data storage system caused by the performance difference between DRAM and NAND flash (Figure 1.3.) [6,7]. As representative candidates for the new memory devices, phase-change random access memory (PRAM), spin-transfer torque magnetoresistive random access memory (STT-MRAM), and resistive random access memory (RRAM) have been developed and commercialized, thereby being utilized to improve the efficiency of the memory/storage system (Figure 1.4.).

1.1.2. Resistive random access memory

RRAM is a data storage device that works by switching the resistance across dielectric materials [8]. RRAM has a great potential as next-generation non-volatile memory device, owing to its simple structure, high density, fast operating speed, and low power consumption [8-13]. Furthermore, resistive switching behaviors can be applied to the future memory devices such as the memristors for neuromorphic computing [14].

In general, a RRAM cell is composed of a metal/insulator (dielectric

material)/metal (MIM) structure (Figure 1.5.). The cell can be modulated with a high resistance state (HRS) or low resistance state (LRS) by external electrical stimulation [15]. Figure 1.6. shows the switching principles with corresponding current–voltage (I–V) characteristics. The transition from HRS to LRS and the corresponding voltage are called SET operation and V_{set}, respectively. The reverse operation and corresponding voltage are denoted RESET and V_{reset}, respectively. In the HRS, the negligible current flows throughout the cell due to the intermediate insulator. When V_{set} is applied, a conductive filament (CF) with high conductance is formed inside the insulator material so that a high current flows throughout the cell, switching to the LRS. When V_{reset} is applied, the CF is ruptured and the cell changes back to the HRS.

Based on the resistive switching operation, RRAM has been exhibited excellent miniaturization down to 10 nm [9], fast operation speed (<100 ps) [10], good retention (>10 years at 85 °C, extrapolated) [11], high endurance cycle (>10^{12} switching cycles) [12], and low power consumption (<10 fJ) [13]. Therefore, RRAM is a potential alternative to improve the efficiency of current memory systems.

1.2. Motivation

Thanks to the efforts of researchers all around the world over the past decades, the performance of RRAMs has improved considerably. However, it must be admitted that there are still some challenges to be studied for the practical application of RRAM.

The first is the ability to control CF in RRAM. In the conventional planar cell structure, the electric field within dielectric materials is uniformly distributed over the entire cell, which leads to competitive growth of multiple CFs [16,17]. The multiple CFs can be fused during successive switching cycles, causing large fluctuations in operating performance [18]. Many techniques have been developed to control the formation of CFs in RRAM. For example, resistance switching in the controlled region has been pursued by introducing metal nanoparticles [19], doping materials [20], and interfacial layers into the switching layer [21]. Despite significant progress being achieved through these methods, CF formation at a controlled location has remained elusive, and an effective approach to further improve the RRAM performance is still required.

Another challenge is a thorough investigation of the resistive switching mechanism, which can serve as a guide for optimizing the architecture and performance of RRAM. For example, different switching mechanisms have been proposed even in the same cell structure, which can cause confusion in understanding the resistive switching behavior of RRAM [22-24]. Therefore, a systematic study is needed to get a complete understanding of the switching mechanism.

The last is to solve the sneak-path problem. Ultra-high density can be

achieved by setting the unit cell size to $4F^2$ (F is the feature dimension) through the passive crossbar array architecture [25]. However, the sneak-current, which reduces the read-out sense margin, increases the power consumption, and limits the array size, is a significant hurdle to realizing the practical use of RRAMs [26]. To suppress the undesired leakage current, many approaches have been attempted to make the nonlinear RRAM cells in a LRS. For example, nonlinear circuit elements such as diode, transistor, and selector were characterized, connecting in series with each RRAM cell [27-29]. Even though the integration of the elements and cells can mitigate the leakage currents, the applicable element type is different according to the RRAM type, so appropriate one should be adopted [25]. Therefore, a distinct method achieving $I–V$ nonlinearity is required.

After overcoming all the above challenges through continued interest in RRAM applications, there is no doubt that commercialized RRAM will become popular in the near future. We believe that this dissertation will not only contribute to the significant advancement of all electronic devices, including RRAM, but will also help promote research activities in the electronic device field.

1.3. Dissertation Overview

This dissertation offers experimental and theoretical bases for practical use of RRAM particularly, focused on the effects on (i) the charge trapping/de-trapping mechanism in organic material-based RRAM, (ii) the thermochemical mechanism in transition metal oxide-based RRAM, and (iii) the electrochemical metallization (ECM) type complementary resistive switch (CRS) memory via the local enhancement of electric fields through metal nanostructures. Accordingly, the remaining chapters are organized as follows.

In Chapter 2, the influences of the enhanced electric fields achieved by the structured electrode on the resistive switching of the organic RRAM are investigated. This chapter has been published as Han-Hyeong Choi, Minsung Kim, Jingon Jang, Keun Hyung Lee, Jae Young Jho, and Jong Hyuk Park, "Tip-Enhanced Electric Field-Driven Efficient Charge Injection and Transport in Organic Material-Based Resistive Memories," *Applied Materials Today* 20 (2020) 100746 (DOI: 10.1016/j.apmt.2020.100746). In this work, we describe the introduction of a pyramid-structured electrode to organic RRAM, to achieve tip-enhanced electric fields, and our investigation of the influence of the generated electric field on the resistive switching characteristics of the device. The electric field in the pyramid-structured RRAM can be significantly enhanced only at the tip, thereby facilitating charge injection at the electrode/polyimide (PI) interface and charge transport through the PI switching layer. The charge transport mechanism follows the space-charge limited current model modified by the Poole–Frenkel effect. These results provide an effective strategy to control the charge concentration, injection, and

transport in organic RRAM.

In Chapter 3, the effect of the introduction of structured electrodes into thermochemical mechanism (TCM)-based RRAM on CF formation and device performance is investigated. This chapter has been published as Han-Hyeong Choi, Sung Hoon Paik, Youngjin Kim, Minsung Kim, Yong Soo Kang, Sang-Soo Lee, Jae Young Jho, Jong Hyuk Park, "Facilitation of the thermochemical mechanism in NiO-based resistive switching memories via tip-enhanced electric fields," *Journal of Industrial and Engineering Chemistry* 94 (2021) 233–293 (DOI: 10.1016/j.jiec.2020.10.041). In this work, we demonstrate that Platinum pyramid-structured electrodes can promote the TCM in nickel oxide-based RRAM by improving the electric field within the switching material and controlling Joule heat generation locally. The tip-enhanced electric field can induce a local temperature rise, which facilitates the TCM for nucleation and CF growth. This approach can overcome the problem of unreliable TCM-based resistance switching in conventional RRAM by achieving position selectivity.

In Chapter 4, the effect of local electric field enhancement achieved through block copolymer (BCP)/metal micelle nanostructures on the complementary resistive switch (CRS) behavior is described. The main portion of this chapter has been prepared for submission as Han-Hyeong Choi, Hyun Jin Kim, Jinwoo Oh, Minsung Kim, Jeong Gon Son, Jae Young Jho, Keun Hyung Lee, and Jong Hyuk Park, "Facile Achievement of Complementary Resistive Switching Behaviors via Self-Assembled Block Copolymer Micelles." In this work, we offer a facile approach to achieving the CRS architecture with nanostructures of self-assembled BCP/metal compound micelles. Based on numerical

simulation, the spherical metal nanostructures enhance the electric fields locally. The enhanced electric fields promote Joule heating and redox reactions of electrochemically active metals, leading stable ECM type CRS behavior. The resulting memory devices exhibit reliable CRS behavior with four distinct threshold voltages in a single cell and cell-to cell tests. Therefore, this approach can provide a solution to the sneak-path issue in crossbar array architecture for ultra-high density.

1.4. References

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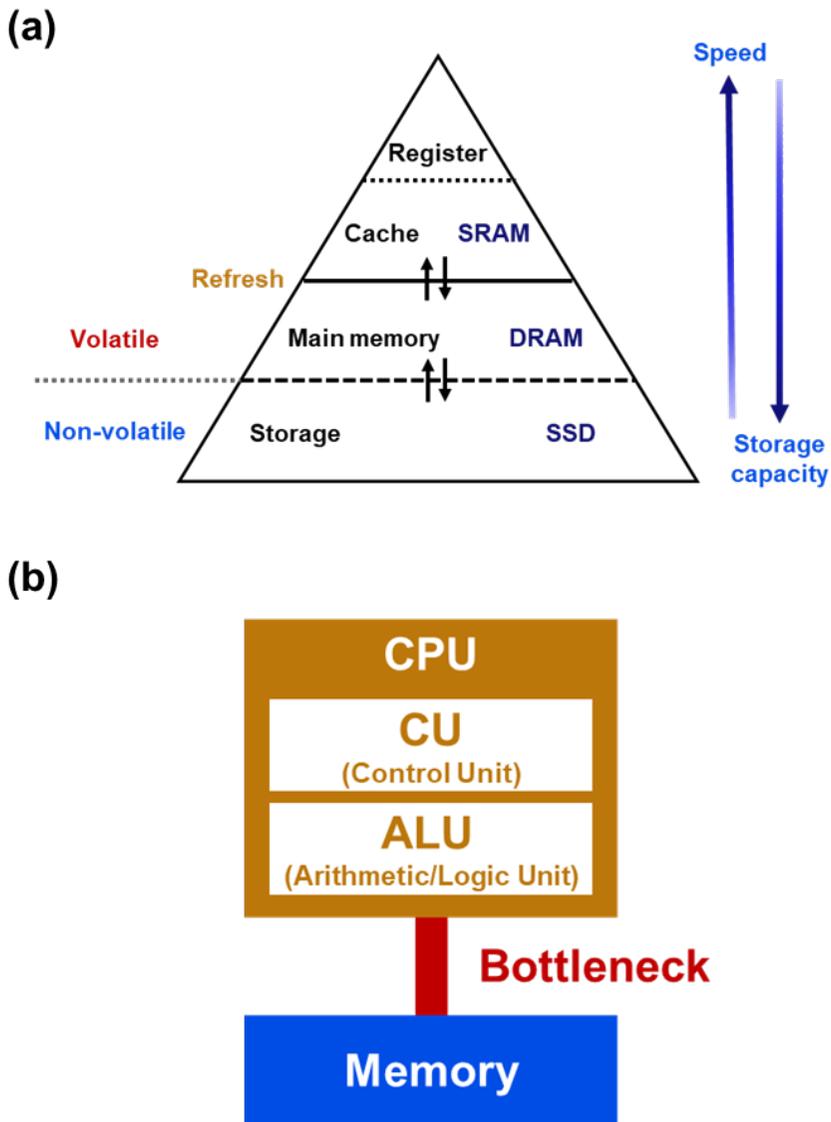
Figure 1.1. Schematic illustration of (a) memory hierarchy and (b) Von-Neumann bottleneck.
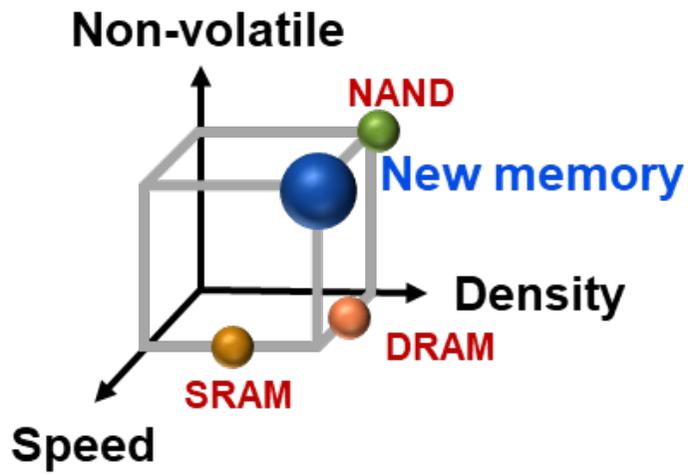
Figure 1.2. The characteristics of the functional elements of conventional memory and new memory.
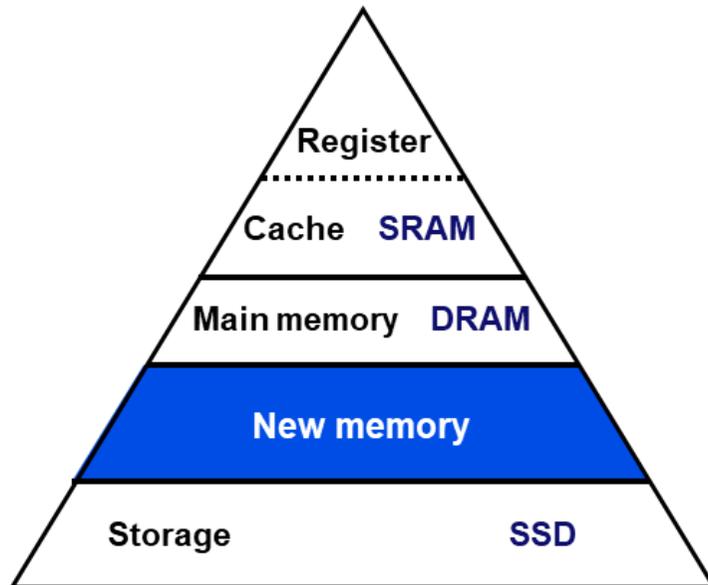
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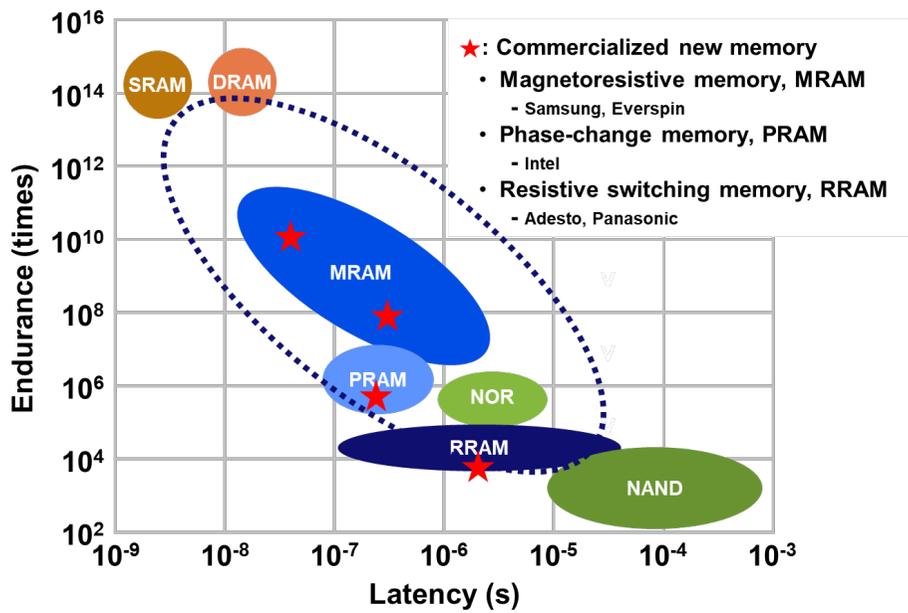
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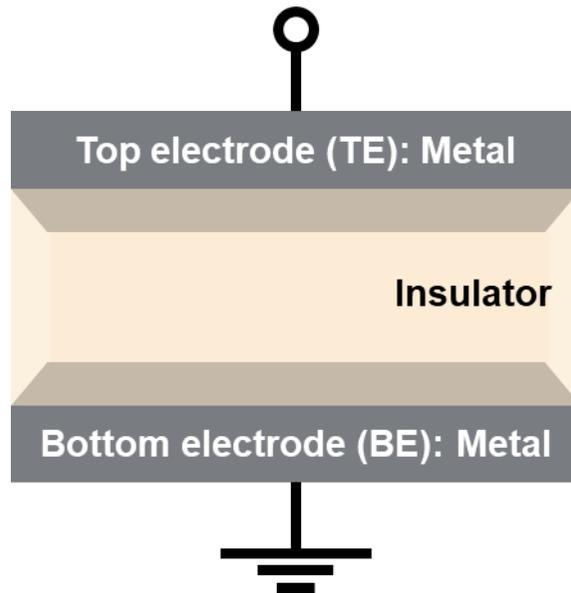
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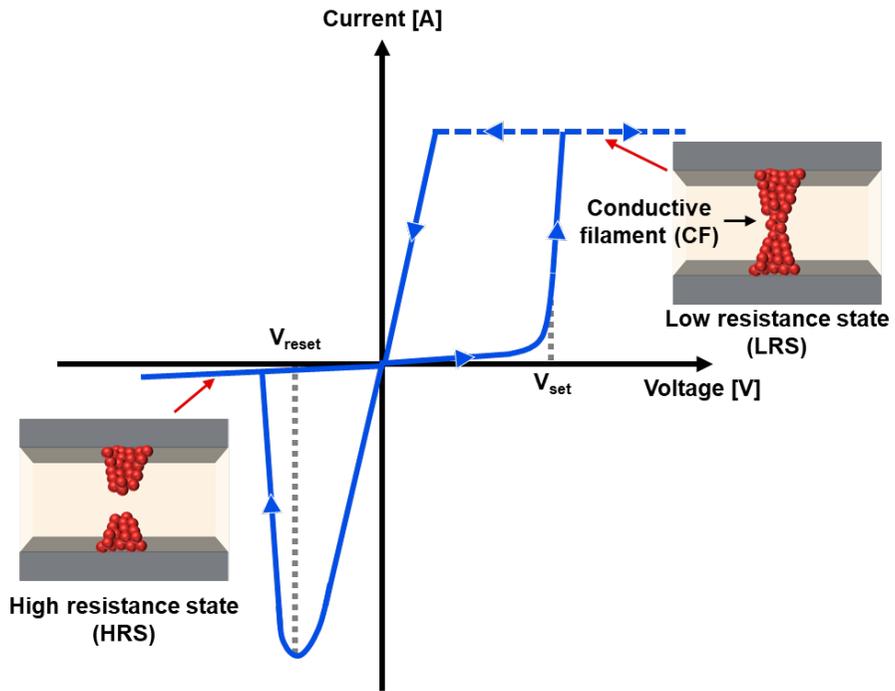
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Chapter 2. Tip-Enhanced Electric Field-Driven Efficient Charge Injection and Transport in Organic Material-Based Resistive Memories[*]

Organic materials show promise as switching layers for resistive random access memory (RRAM). However, practical application has been limited by inefficient charge injection and transport in typical organic materials. This study proves that local enhancement of electric fields through structured electrodes can improve charge injection and transport in organic RRAM. Specifically, pyramid-structured electrodes with an extremely sharp tip are introduced into RRAM with a polyimide (PI) switching layer. The electric field in the pyramid-structured RRAM can be significantly enhanced only at the tip, thereby facilitating charge injection at the electrode/PI interface and charge transport through the PI switching layer. Indeed, the resulting RRAM exhibits low and reliable operating voltages (SET: 1.76 V ± 0.41 V / RESET: −0.49 V ± 0.15 V) compared with conventional PI-based RRAMs with planar electrodes. The conductive path formed in the tip region is observed directly using conductive atomic force microscopy, demonstrating that resistive switching occurs by tip-enhanced electric fields. Also, the charge transport mechanism follows the

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space-charge limited current model modified by the Poole–Frenkel effect. These results provide an effective strategy to control the charge concentration, injection, and transport in organic RRAM, for realization of low-cost, large-area, shape-deformable data storage devices.

2.1. Introduction

Resistive random access memory (RRAM) operates according to resistance changes of dielectric materials induced by electrical stimulation [1]. RRAM has been actively investigated as a next-generation non-volatile memory device, owing to its simple structure, fast operating speed, low power consumption, excellent durability, and high integration density [2,3]. The dielectric materials in RRAM play an important role in determining the resistive switching mechanism [4,5]. In many cases, inorganic materials have been exploited as the resistive switching layer for RRAM. However, the promising properties (including flexibility and solution processability) exhibited by organic switching materials suggest the potential of organic RRAM for low-cost, large-area, shape-deformable data storage devices [6-8].

Although a complete understanding of the resistive switching mechanism in organic RRAM has not yet been achieved, the charge injection at the electrode/organic layer interface and charge transport through the organic switching layer determine the resistive switching behavior of organic RRAM [9-11]. However, charge injection and transport in typical organic materials are inefficient, resulting in poor performance of organic RRAM [12]. Many techniques for incorporating organic switching materials into RRAM have been developed to address this issue. For example, single macromolecules containing both electron-donating and -accepting groups have been synthesized [13,14], and polymer composites incorporated with metal nanoparticles [15,16], nanocarbons [17], and conducting polymers [18] have been prepared. While significant progress has been made with these strategies, a simple and

convenient approach should still be pursued to further enhance the performance of organic RRAM by facilitating charge injection and transport.

The enhancement of local electric fields has been explored to control the formation and removal of conductive paths in RRAM [19]. Indeed, improved performance of RRAM based on inorganic switching materials has been reported through the introduction of nanoparticles or additional layers, to enhance the local electric fields [20,21]. However, these techniques have not been effective in organic RRAM and only a modest increase (< 2 times) in electric fields has been observed. Recently, inorganic RRAMs with structured metal electrodes have been demonstrated to significantly enhance local electric fields [22-25]. The electric fields at a sharp metal tip can be amplified up to ~6.6 times, thus increasing the efficiency of both charge injection and transport in organic switching materials. Moreover, utilizing structured metal electrodes can improve systematic understanding of the resistive switching mechanism in organic RRAM, because precise control of conductive paths in the organic switching material is feasible.

Herein, we describe the introduction of a pyramid-structured electrode to organic RRAM, to achieve tip-enhanced electric fields, and our investigation of the influence of the generated electric field on the resistive switching characteristics of the device. Al pyramid arrays and polyimide (PI) were used as a metal electrode and resistive switching layer, respectively. Based on simulation and experimental results, we confirmed that the pyramid-structured electrode greatly enhances the electric field at the tip, and facilitates charge injection and transport in the PI layer, thus creating location-controlled

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conductive paths. The resulting RRAM exhibited reliable resistive switching behavior and highly improved performance compared with PI-based RRAM with planar electrodes. Thus, our approach offers an effective strategy to overcome the limitations of conventional organic RRAM.

2.2. Experimental

Preparation of pyramid-structured electrodes

Metal structures with a sharp tip was fabricated using the template-stripping method [26]. Figure 2.5(a) shows a schematic diagram of the preparation of pyramid-structured metal electrodes via template stripping. Si templates having inverted pyramids were prepared by photolithographic techniques and anisotropic etching of Si (100) wafers using a potassium hydroxide (KOH) solution. After cleaning with a piranha solution, a 50-nm-thick Au layer was placed on the prepared Si templates via an e-beam evaporator (KVE-E2006; Korea Vacuum Technology, Gyeonggi-do, Korea). Heat-curable epoxy (EPO-TEK 377; Epoxy Technology, Billerica, MA, USA) was applied to the Au layer, and a glass substrate was then placed thereon for use as a supporting layer. After curing the epoxy at 150°C, the Au pyramid structures were peeled off the templates. Pyramid-structured electrodes were obtained by depositing a 30-nm-thick Al layer on the Au pyramids (Figure 2.5(b)).

Preparation of PI-based resistive memories

The manufacturing procedure for the PI-based memories with pyramid-structured electrodes is illustrated in Figure 2.5(c). Poly(3,3′,4,4′-biphenyltetracarboxylic dianhydride-*co*-1,4-phenylenediamine) (BPDA-PPD, Sigma-Aldrich, St. Louis, MO, USA) was dissolved in N-methyl-2-pyrrolidone (NMP, Sigma-Aldrich); the weight ratio of BPDA-PPD to NMP was 1:2. The PI precursor solution was spin-coated at 2,000 rpm for 40 s on the pyramid-structured electrodes. The PI layer was heated at 60°C for 10 min, followed by

hard baking at 200°C for 1 h. A 30-nm-thick Al layer and a 50-nm-thick Au layer were deposited on the PI layer through a metal mask with 50-μm-diameter holes, to produce individual memory cells. For comparison, controlled devices with planar electrodes were also prepared. The PI switching layer was about 30-nm-thick, as shown in Figure 2.6(a).

Characterization

The morphology of the PI-based memory devices was analyzed using a scanning electron microscopy (SEM, Sigma 200; Carl Zeiss AG, Oberkochen, Germany). To observe the cross-section of the memory devices, the specimens were coated with epoxy and Pt and then cut via focused ion beam (FIB, Helios Nanolab 600; FEI Company, Hillsboro, OR, USA) milling. The electrical properties of the memory devices were measured using a source measurement unit (2643B; Keithley Instruments, Cleveland, OH, USA) under ambient conditions. During the current–voltage (*I–V)* measurement, bias was applied to the isolated island-shaped top electrode (TE), and the bottom electrode (BE) was grounded. The surface morphology and local conduction path of the pyramid-structured memory devices were characterized simultaneously using conductive atomic force microscopy (C-AFM, XE-100; Park Systems, Suwon, South Korea).

Modeling of electromagnetic systems

The electromagnetic simulation for the PI-based memory devices containing pyramid-structured and planar electrodes was performed with multiphysics

simulation software (ALTSOFT, V5.4, AC/DC module). The electric field (E) is given by

$$E = -\nabla V \tag{1}$$

where V is the electrical potential.

The geometric parameters of the pyramid-structured memory devices used in the simulation were obtained from SEM measurements (Figure 2.1(b)). The multilayered pyramid structure consisted of the following five layers: Au, Al, PI, Al, and Au (from top to bottom). These layers had thicknesses of 50, 30, 30, 30, and 50 nm, respectively. The pyramid structure had a taper angle of 70.6°. The tip radius was 25 nm at the BE, 55 nm at the PI layer, and 135 nm at the TE, respectively. The remaining part of the structure was epoxy. The material parameters were taken from the software library.

2.3. Results and Discussion

PI has been commonly utilized in organic electronics, due to its excellent mechanical properties, thermal and chemical stability, and solution processability, which renders the fabrication of devices easy and inexpensive [27]. However, the use of PI itself as a switching material in RRAM has been restricted due to the large bandgap [28]. In addition, the resistive switching behaviors of the PI layer proceed through charge trapping/detrapping mechanisms [29]; thus, the energy barrier of traps should be lowered to facilitate charge injection and transport in the PI layer [30]. Exploiting the charge concentration and enhanced electric field achieved by the structured electrodes could be a simple but effective solution for RRAM with a PI switching layer [31,32].

The template-stripping method, a low-cost, high-throughput, nanofabrication method, can be used to provide structured metal electrodes [26,33]. Figure 2.1(a) shows a SEM image of the Au pyramid electrode with an extremely sharp tip and smooth surfaces, obtained by application of lithographic techniques followed by template stripping (see Figure 2.5(a) for details on the fabrication process). A thin Al layer was then deposited on the Au pyramids to improve the affinity between the metal electrode and the PI switching layer, as well as to form a uniform PI layer. After sequentially stacking the PI, Al, and Au layers, the cross-section of the pyramid structure was prepared through FIB milling (Figure 2.1(b)). The thickness of the PI switching layer was 30–40 nm, and the tip radius of the pyramid was only ~25 nm. As reported previously, the taper angle of the pyramid electrodes was ~70.6°, due to anisotropic etching of a Si

template via KOH; in this case, the etching rate was much faster in the <100> crystal direction than in the <111> direction [34,35].

The three-dimensional electric fields in the pyramid-structured memory device were calculated through finite element modeling. Figure 2.1(c) shows the enhanced electric fields near the tip when a potential of 2 V was applied to the TE and the BE was grounded. The maximum magnitude of the tip-enhanced electric fields was 2.65×10^8 V/m, which is four-fold larger than that in the planar structure (6.67×10^7 V/m) under the same applied potential (Figure 2.6(c)). The significantly enhanced electric field at the tip facilitates effective resistive switching behavior in the PI layer, and improves the performance of PI-based RRAM [31,32].

Figure 2.1(d) shows a schematic diagram of the switching behaviors for the pyramid-structured memory device. The tip-enhanced electric fields achieved by the pyramid structure provide three key benefits: (i) facile charge concentration at the tip, and efficient charge (ii) injection and (iii) transport. Applying a potential to the structured electrode causes the charges to concentrate on the sharp tip rather than on the plane [36]. This charge concentration effect can be estimated by a simple electrostatic model [37]. The surface charge density (σ) is given by

$$\sigma = q/4\pi r^2 \qquad (2)$$

where q is the charge quantity, and r is the tip radius of the electrode. The equation indicates that with a smaller the tip radius, more charges concentrate at the tip. Accordingly, the pyramid-structured electrode prepared in this study can be highly effective for locally increasing the charge density, that is, the

charge concentration at the tip. The electric field (E) is proportional to the charge density (ρ), as follows [37]:

$$\nabla \cdot E = \rho/\varepsilon_0 \tag{3}$$

where ε_0 is the vacuum permittivity of dielectric materials. This equation suggests that as the charge density increases, so too does the areal integration of the electric fields, correspondingly enhancing the electric field at the tip.

In addition, these tip-enhanced electric fields can promote charge injection at the electrode/organic interface. The charge injection barrier height (ϕ) into the organic layer under the Schottky effect is represented by [38]

$$\phi(x) = \phi_B - qEx - \frac{q^2}{16\pi\varepsilon_r\varepsilon_0 x} \tag{4}$$

where ϕ_B is the Schottky barrier height (difference between the work function of the electrode and the electron affinity of the organic material), x is the distance from the interface, and ε_r is the relative permittivity of dielectric materials. Based on this equation, as the electric field increases, the charge injection barrier height is lowered, thereby improving the charge injection efficiency.

Moreover, the tip-enhanced electric fields enable efficient charge transport in the PI switching layer. The traps distributed throughout the energy bandgap of the PI layer help the charge carriers overcome the energy barrier, resulting in their release and transport. Based on the space-charge limited current (SCLC) model [39], the barrier height of the traps is constant over the applied electric field range. In practice, however, high electric fields ($> 10^8$ V/m) can lower the barrier height of traps between localized states for disordered systems, leading

to an increased emission rate of trapped charge carriers [40]. This phenomenon is known as Poole-Frenkel (P-F) effect, which means that the excited electrons by a strong electric field overcome the trap barrier [41]. The relationship between the electric field (E) and charge carrier mobility (μ) is given by [42]

$$\mu = \mu_i exp[\beta_{PF}(\frac{1}{k_BT} - \frac{1}{k_BT_0})\sqrt{E} - \frac{\Delta\phi_t}{k_BT}] \qquad (5)$$

where μ_i is the intrinsic mobility at the zero barrier, β_{PF} is the P-F constant, k_BT is the Boltzmann-energy-term, $\Delta\phi_t$ is the average trap barrier height, and T_0 is an empirical constant. According to this equation, the charge flow through the PI layer can be largely increased by the tip-enhanced electric fields, thus allowing efficient charge transport. Considering these effects achieved by the pyramid-structured electrodes, PI-based RRAM is expected to exhibit effective resistive switching behaviors.

To investigate the tip-enhanced electric field-driven switching behaviors, the electrical properties of PI-based RRAM were characterized. Figure 2.2(a) shows the I–V curve of the pyramid-structured device obtained through a direct current (DC) voltage sweep. Asymmetric bipolar switching behaviors were observed and the SET/RESET voltages (V_{SET}/V_{RESET}) were 2.04 and −0.44 V, respectively. For comparison, a planar memory device having a PI switching layer of the same thickness was prepared (Figure 2.6(a)). As shown in Figure 2.6(b), no resistive switching occurred for the planar device even at a high potential (between −10 and 10 V.) At the maximum applied potential (±10 V), the magnitude of the electric fields for the planar device can rise to ~3.33×10^8 V/m. This value is greater than the magnitude of the tip-enhanced electric fields

$(2.65 \times 10^8$ V/m) when resistive switching behavior is observed in the pyramid-structured device (Figure 2.1(c)). This result implies that resistive switching is not induced by simply applying strong electric fields to the PI-based RRAM. Only pyramid-structured devices with comprehensive charge concentration, and efficient charge injection and transport, allow proper resistive switching in the PI-based RRAM (Figure 2.2(a) and 2.6(b)).

Figure 2.2(b) shows the cycle-to-cycle variation in current values in low resistance state (LRS) and high resistance state (HRS) for the pyramid-structured device under the DC sweep condition. Average current values in LRS (I_{LRS}) and HRS (I_{HRS}) were $\sim 2 \times 10^{-3}$ and $\sim 6 \times 10^{-7}$ A, respectively and they had a narrow distribution. Thus, the I_{LRS}/I_{HRS} ratio of the pyramid-structured device was maintained above 10^3, which is sufficient to ensure the reliability and fault tolerance of PI-based RRAM [5,10]. Figure 2.2(c) illustrates its retention performance at room temperature. The current levels in LRS and HRS were constant for over 10^4 s at a read voltage of 0.1 V, indicating durable resistance states and thus providing stable information storage [5,10].

A comparative study on the V_{SET} and V_{RESET} of the pyramid-structured RRAM was carried out based on previous results [15,18,43-50]. Devices were selected that improved resistive switching behavior in the PI layer in previous studies, through the modification of chemical structure [45-50] or incorporation of conductive additives [15,18,43,44]; V_{SET} and V_{RESET} are given in Figure 2.2(d). In the DC sweep analysis (50 cycles), the average and standard deviation of V_{SET} and V_{RESET} for the pyramid-structured RRAM were 1.76 ± 0.41 and -0.49 ± 0.15 V, respectively. Detailed data are presented in Figure 2.7(a).

Surprisingly, the pyramid-structured device had much lower V_{SET} and V_{RESET} values than previous PI-based RRAMs, allowing low-power operation for energy savings. In previous studies, organic RRAMs were prepared by dispersing conductive additives (phenyl-C61-butyric acid methyl ester) in the same PI layer as used in this study [18]. Their operating voltage was 4.27 ± 0.63 V, which is larger and less reliable than that of the pyramid-structured device. This result indicates that introducing structured electrodes can be more effective for inducing resistive switching in the PI layer than using conductive additives. Some of the previously reported PI-based RRAMs showed operating voltages similar to the pyramid-structured devices, as illustrated in Figure 2.2(d) [46,50]. However, because these RRAMs use structurally modified PI layers through fine chemistry, this approach is not a simple and effective strategy for improving the performance of organic RRAMs. Moreover, when resistive switching occurs in the entire area of the PI layer to form conductive paths, the reproducibility of the switching behavior is significantly lower compared with pyramid-structured devices capable of controlling the switching area [22]. Therefore, via pyramid-structured electrodes, tip-enhanced electric fields can improve the performance of organic RRAM more simply and effectively compared with chemical structure modification of PI or the introduction of conductive additives. Figure 2.7(b) shows the cell-to-cell distribution of the V_{SET} and V_{RESET} for 30 cells. The average and standard deviations of V_{SET} and V_{RESET} were 1.64 ± 0.38 and -0.52 ± 0.16 V, respectively. These values are similar to those of the single cell shown in Figure 2.7(a), demonstrating high consistency between the unit cells.

To reveal the switching area of the pyramid-structured device, the locations of conductive paths in the HRS and the LRS were examined using C-AFM. In the HRS, the three-dimensional C-AFM image in Figure 2.3(a) and the corresponding I–V profiles in Figure 2.3(b) confirm the negligible current flows throughout the entire device, due to the wide energy bandgap of the PI layer. To form the conductive path of the PI layer, the C-AFM tip with a threshold voltage of 2.6 V was scanned over the entire region, and the current image was obtained at a read voltage of 0.03 V. As shown in Figure 2.3(c), high currents were measured only near the tip, indicating resistive switching from the HRS to the LRS due to the efficient charge concentration, injection, and transport that occurred in the tip area. The maximum current (1.342 µA) was observed at point 1 (the apex of the pyramid). Figure 2.3(d) describes the I–V curves of the pyramid-structured device in the LRS. Regardless of the applied voltages, points 2 and 3 exhibited low current, indicating that the areas were still in the HRS. In contrast, point 1 exhibited a linear current curve as the applied voltages increased, indicating the formation of conductive paths in that region. These results are consistent with the schematic diagram shown in Figure 2.1(d), in which tip-enhanced electric fields resulted in controllable formation of the conductive path in the switching layer. This location-controlled conductive path can lead to reliable resistive switching behaviors in cycle-to-cycle or cell-to-cell tests. Furthermore, that the switching occurred only in the confined region provides insight into the operating mechanism of organic RRAM.

To investigate the conduction mechanism of the PI switching layer, the I–V curves of the pyramid-structure device were characterized at different

temperatures. Figure 2.4(a) shows the temperature dependence of the current in the LRS. When the temperature increased from 298 to 418 K, the current value gradually increased and the resistance gradually decreased, indicating that the PI switching layer in the LRS exhibits semiconducting characteristics as opposed to metallic behavior. At this point, we can conclude that the conduction mechanism of the PI layer is not affected by the electrochemical metallization of Al/Au electrodes. The proposed charge transport mechanism will be discussed later.

The *I–V* data plot analysis of the pyramid-structure device in the HRS and LRS was carried out using conduction models. As shown in Figure 2.4(b), the *I–V* curve of Figure 2.2(a) was plotted on a double-logarithmic scale graph. The inset contains the *I–V* curve in the LRS, which is linear with a slope of ~0.98 (yellow line). This suggests that the electrical conduction of the PI layer in the LRS is dominated by ohmic conduction, as reported previously [47,50]. The *I–V* curve in the HRS can be divided into two regions in which the voltage is lower or higher than 0.75 V; the blue line corresponds to low voltages with a slope of ~1.09, and the green line corresponds to high voltages with a slope of ~1.45. These results indicate that the charge transport of the PI layer in the HRS follows the ohmic conduction at low voltages, and the SCLC model at high voltages [50,51]. This behavior is the same as that of typical organic switching materials controlled by charge trapping/detrapping. However, the unique effects of resistive switching due to the tip-enhanced electric field occur via a different charge transport mechanism.

Given that a tip-enhanced electric field can greatly increase the magnitude of

the applied electric field at a controlled position, the P-F effect must first be taken into account to understand the switching behaviors of the pyramid-structured RRAM [40]. The P-F effect can increase the emission rate of charge carriers trapped in both shallow and deep states under high electric fields ($> 10^8$ V/m). P-F emission can be applied to any organic device if $\ln\left(\frac{J_{PF}}{E}\right)$ and $\sqrt{E}$ show a linear relationship in the following P-F effect equation [9,40,52]:

$$\ln\left(\frac{J_{PF}}{E}\right) = \frac{\sqrt{\frac{q^3}{\pi \varepsilon_r \varepsilon_0}}}{k_B T}\sqrt{E} - \frac{q\Delta\Phi_t}{k_B T} + \ln(qN_C\mu) \tag{6}$$

where J_{PF} is the current density and N_C is the density of states in the conduction band, respectively. P-F plot analysis was performed based on the *I–V* curve of Figure 2.2(a) at high voltages (> 0.75 V). As shown in Figure 2.4(c), $\ln\left(\frac{J_{PF}}{E}\right)$ and $\sqrt{E}$ have a linear relationship in the applied voltage region, which means that P-F emission occurs due to the tip-enhanced electric field [9,52].

Figure 2.4(d) shows a schematic diagram of the charge transport model modified by the tip-enhanced electric field. Even under an external electric field (E_A), the charge carriers in the conventional planar device still have difficulty in overcoming the trap energy barrier height ($q\Phi_t$), such that charge transport in the PI switching layer is impeded considerably. In contrast, the tip-enhanced electric field for the pyramid-structured device significantly lowers the barrier height, leading to P-F emission [40]. As a result, trapped charge carriers are more likely to escape from the traps, allowing efficient charge transport in the PI layer. Therefore, the switching mechanism of the pyramid-structured RRAM

with a PI layer is governed by the SCLC model modified by the P-F effect.

2.4. Conclusions

We have demonstrated that the tip-enhanced electric fields achieved by the pyramid-structured electrode can provide PI-based RRAM with three key benefits: (i) facile charge concentration, and efficient charge (ii) injection and (iii) transport. In particular, the local enhancement of electric fields can facilitate charge injection at the electrode/PI interface and charge transport through the PI switching layer. As a result, the pyramid-structured RRAM exhibited greatly improved performance over those of previous studies. Moreover, controlling the location of the conductive path through structured electrodes helped to systematically clarify the switching behavior of PI-based RRAM. These results will make an important contribution to the development of high-performance organic RRAM and promote its practical use.

2.5. References

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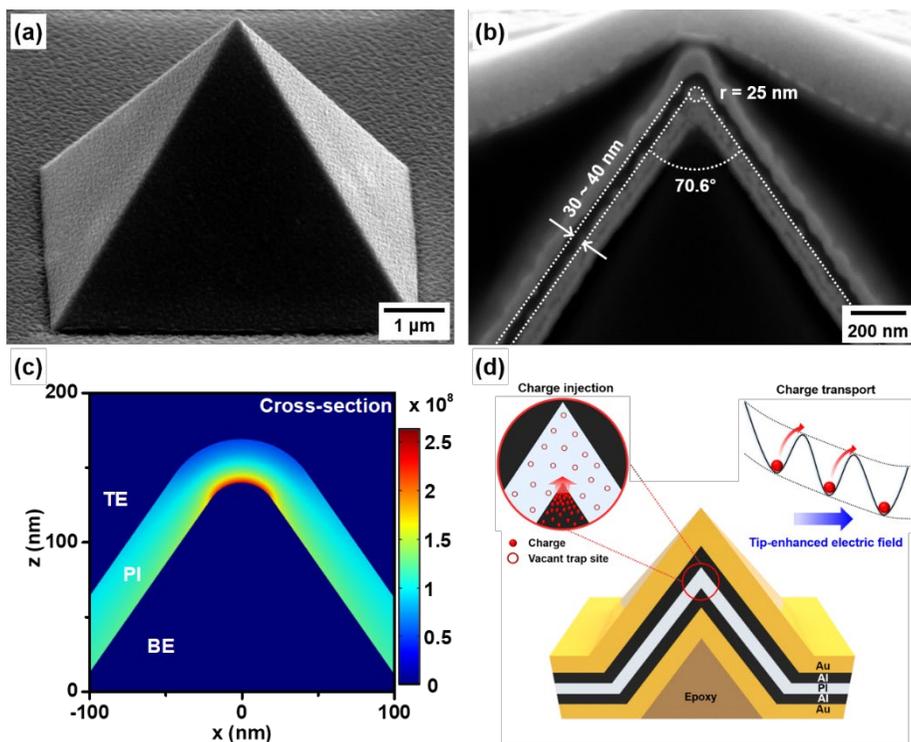
Figure 2.1. (a) A SEM image of the pyramid electrode. (b) A cross-sectional image of a multilayered pyramid-structure consisting of Au/Al/PI/Al/Au layers. (c) Finite-element modeling of the electric field in the pyramid structure. (d) Schematic diagram of switching behavior in the pyramid-structured RRAM.
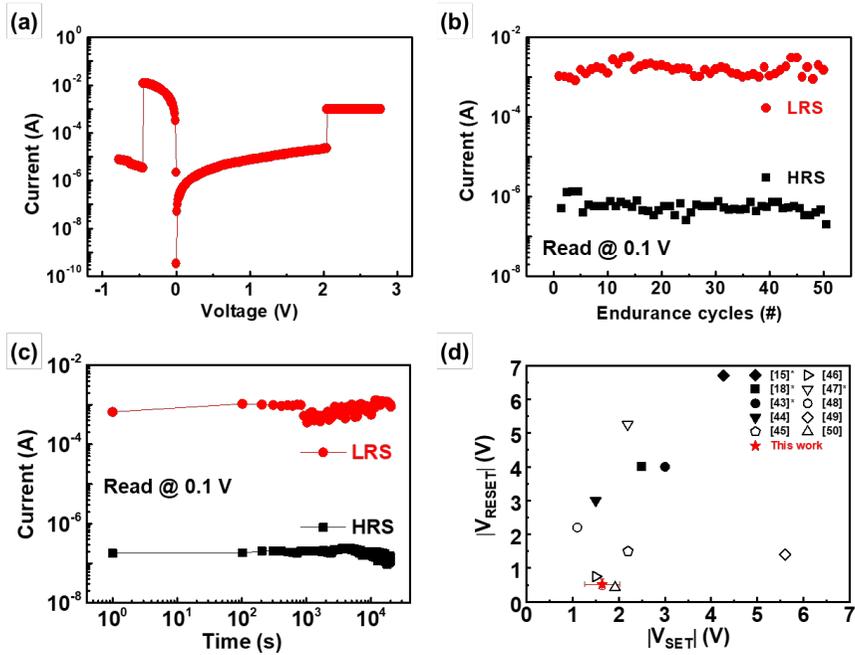
Figure 2.2. Electrical properties of the pyramid-structured memory devices with the PI switching layer. (a) Representative *I–V* curve on a semi-logarithmic scale. (b) The variation in current in the LRS (red) and HRS (black) under DC sweep mode (50 cycles). (c) Retention performance at room temperature. (d) Comparative study on the SET/RESET voltages of PI-based RRAM. The numbers represent reference numbers, and the asterisks indicate the unipolar switching memory devices.
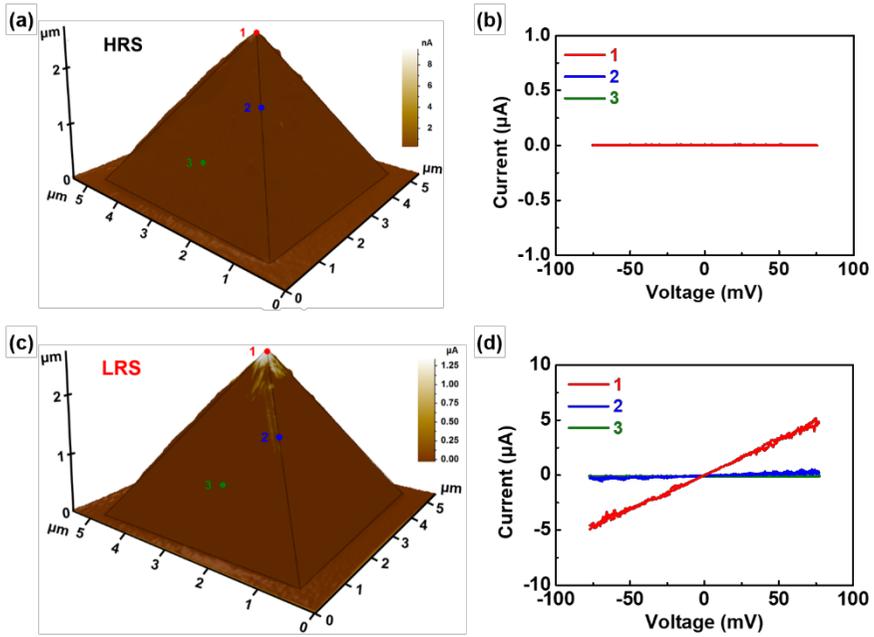
Figure 2.3. C-AFM images and *I–V* curves of the pyramid-structured device. (a) C-AFM image in the HRS and (b) *I–V* curves at points 1–3 in (a). (c) C-AFM image in the LRS and (d) *I–V* curves at points 1–3 in (c).
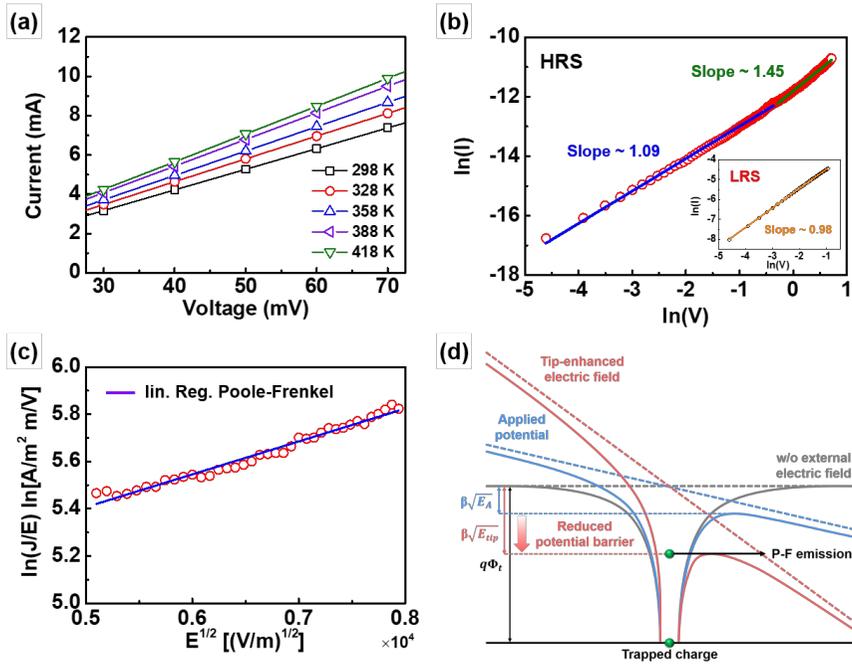
Figure 2.4. (a) *I–V* curves of the pyramid-structured device in the LRS at different temperatures. (b) *I–V* curve for the PI pyramid-structured device plotted on a double-logarithmic scale. (c) The P-F plot at high voltages (> 0.75 V). (d) Schematic diagram of the charge transport model modified by the tip-enhanced electric field. β represents $\frac{\sqrt{\frac{q^3}{\pi \varepsilon_r \varepsilon_0}}}{k_B T}$ in Equation (6)
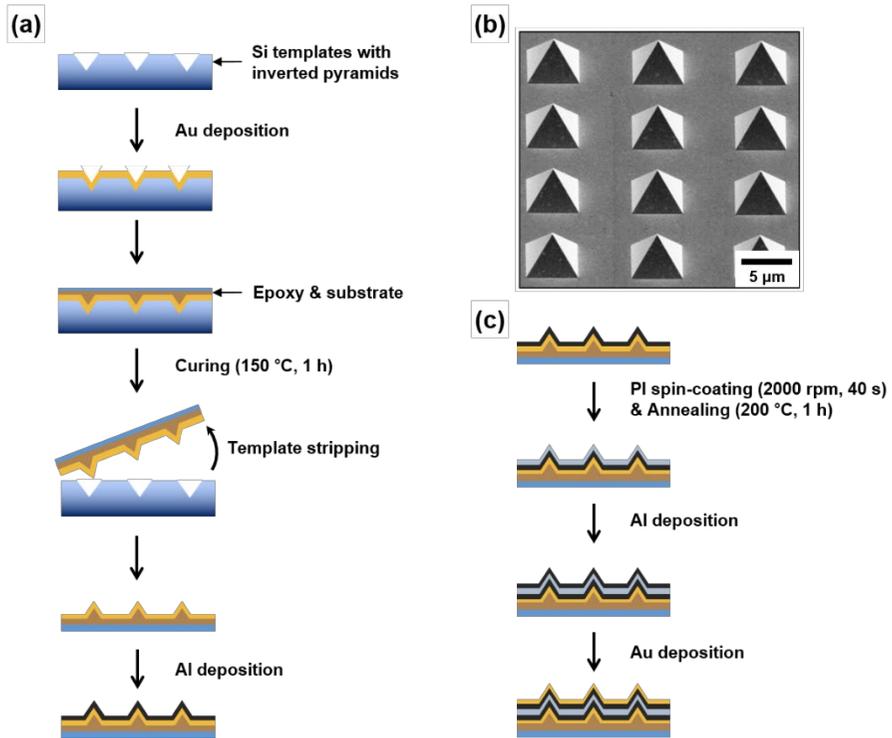
Figure 2.5. (a) Schematic diagram of the preparation of pyramid-structured electrodes via template stripping. (b) A SEM image of pyramid-structured electrodes in wide view. (c) Schematic diagram for the preparation of a pyramid-structured RRAM device.
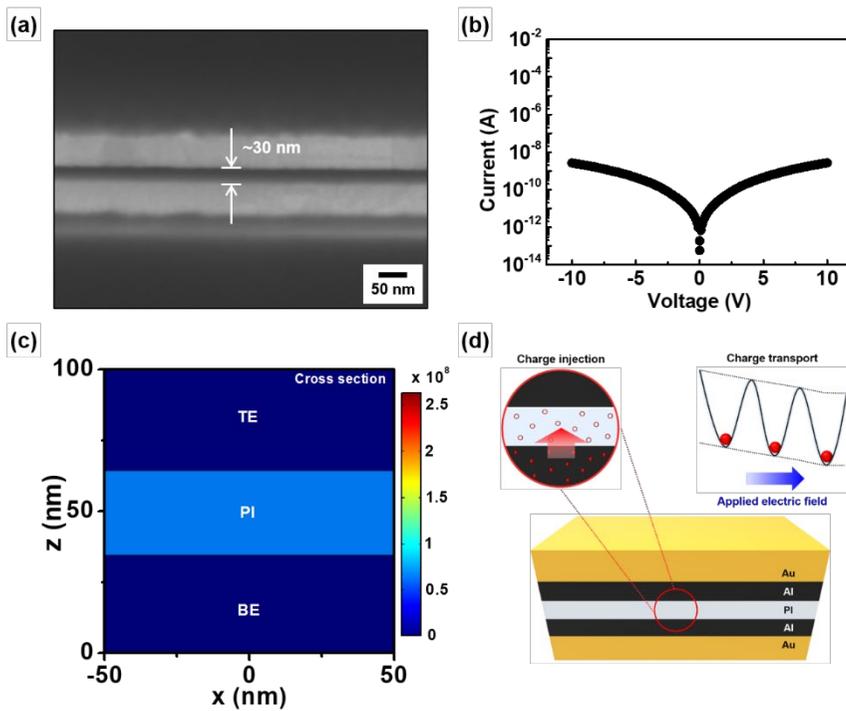
Figure 2.6. (a) Cross-sectional image of a multilayered planar-structured memory device consisting of Au/Al/PI/Al/Au layers. (b) The *I–V* curve on a semi-logarithmic scale from the PI planar device during DC voltage sweep. (c) The three-dimensional simulation result of the planar PI device. (d) Schematic illustration of resistive switching behaviors in the planar memory device.
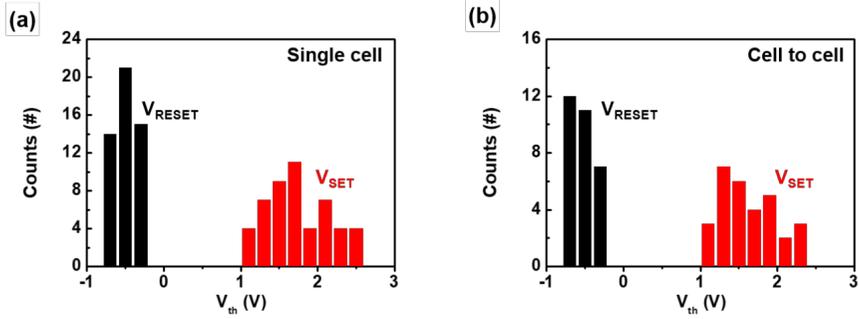
Figure 2.7. Distribution of V_{SET} (red) and V_{RESET} (black) for (a) 50 cycles in a single cell and (b) 30 cells of pyramid-structured memory devices with a PI switching layer.

Chapter 3. Facilitation of the Thermochemical Mechanism in NiO-Based Resistive Switching Memories via Tip-Enhanced Electric Fields[*]

Transition metal oxides have attracted considerable attention as a switching material for resistive random access memory (RRAM) based on the thermochemical mechanism (TCM). However, the heat energy required for resistance switching is applied to the entire area of the RRAM without position selectivity, causing random growth of conductive filaments (CFs) and degrading device performance. This study showed that structured electrodes can promote the TCM in nickel oxide (NiO)-based RRAM by enhancing the electric field within the switching material and controlling Joule heat generation locally. Pyramid-structured electrodes with an extremely sharp tip prepared by the template-stripping method achieve an electric field in the tip region that is ~5 times larger than that of conventional planar electrodes. The tip-enhanced electric field can induce a local temperature rise, which facilitates the TCM for nucleation and CF growth. The resulting RRAMs exhibit low and reliable forming, SET and RESET voltages (1.96 ± 0.14 V, 1.44 ± 0.12 V, and $0.64 \pm$

0.05 V, respectively). Moreover, their retention time and resistance ratio (R_{HRS}/R_{LRS}) are greatly improved, by 10 and 10^2 times, respectively, compared to planar devices. This approach can achieve position selectivity in TCM-based resistance switching, and could lead to the development of high-performance RRAM.

3.1. Introduction

Resistive random access memory (RRAM) is a data storage device that exploits dielectric materials with switchable resistance [1]. RRAM has great potential as non-volatile memory, owing to its simple structure, fast operating speed, low power consumption, and high scalability [2,3]. Furthermore, resistive switching behaviors can be applied to the future memory devices such as the memristive and neuromorphic memories [4,5]. However, unreliable resistive switching behaviors caused by random nucleation and the growth of conductive filaments (CFs) have limited the practical application of RRAM [6, 7]. Many techniques have been developed to achieve reliable switching and position selectivity in CFs. For example, resistance switching in the controlled region has been pursued by introducing metal nanoparticles, doping materials, and interfacial layers into the switching layer [8-10]. Despite considerable progress, CF formation at a controlled location has rarely been reported, and an effective approach to further improve the performance of RRAM is still required.

Understanding the resistive switching mechanism of materials is essential to control CF formation [11,12]. Many RRAMs based on transition metal oxides operate according to the thermochemical mechanism (TCM) [13,14]. Resistance switching with the TCM occurs through a current-induced temperature rise and, consequently, a phase change of the transition metal oxides [15]. To achieve position-selective formation of CFs in TCM-based RRAM, the local temperature of the switching layer should be precisely controlled. Since Joule heating governs the temperature rise of TCM-based

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RRAM, the heating zone can be selected by managing the current flow. However, providing different current flows in different areas is very challenging in conventional RRAMs due to their simple structure. Therefore, novel structures need to be developed to generate position-selective currents for TCM-based RRAM.

Previous studies have reported control of the electric field inside the RRAM with a structured metal electrode [16-18]. A pyramidal electrode with a tip radius of tens of nanometers was able to selectively enhance the electric field at the tip [19]. Through these tip-enhanced electric fields, electrochemical metallization-based RRAM can promote the ionization reaction of metals and transport of metal ions [20]. In addition, in organic RRAM with structured electrodes, charge injection and transport efficiency at the tip were greatly increased, providing position-selective CF formation and improved device performance [21]. These results suggest that the current flow and temperature inside TCM-based RRAM can be locally controlled by using a structured electrode and enhancing the electric field. However, this approach can also give rise to other phenomena in the TCM, such as migration of oxygen vacancies, charge injection at the electrode, and heat generation by Joule heating [22]. Hence, it is necessary to systematically investigate how the introduction of structured electrodes into TCM-based RRAM affects CF formation and device performance.

In this study, we report facilitation of the TCM via tip-enhanced electric fields for position-selective CF formation in RRAM. Platinum (Pt) pyramid arrays were prepared via the template-stripping method and introduced into the

RRAM as a structured electrode. Nickel oxide (NiO) was used as a dielectric layer and its resistive switching behavior based on the TCM was investigated. The simulation and experimental results confirmed that the tip-enhanced electric fields can induce a temperature rise at the tip alone, promoting thermochemical reactions and resistance switching. This RRAM enabling position-selective CF formation exhibited low and reliable operating voltages compared to conventional RRAM. Therefore, this approach can overcome the problem of unreliable resistance switching in conventional RRAM and should encourage the development of high-performance RRAM based on the TCM. Furthermore, this work can provide an excellent model to confirm the effect of three-dimensional nanostructures in future memory devices with very narrow scales.

3.2. Experimental

Preparation of Si templates

The template-stripping method was utilized to produce pyramid-structured metal electrodes with a sharp tip [23]. Si templates with inverted pyramid structures were fabricated by photolithographic and wet etching techniques (Figure 3.6(a)). Si (100) wafers covered with a 100 nm-thick silicon nitride (SiN) layer were used as the base substrates. After treating the surface with hexamethyldisilazane gas, a positive photoresist (PR) solution (GXR601; AZ Electronic Materials, Luxembourg, Luxembourg) was spin-coated on the substrates. The samples were mounted on a mask aligner (MA6; Karl Suss, Munich, Germany) and exposed under an ultraviolet lamp through a hole-array patterned mask. The PR layer in the exposed area was removed using a developing solution (AZ 325; AZ Electronic Materials). The hole-array patterns were transferred to the SiN layer via reactive-ion etching (RIE 80 Plus; Oxford Instruments, Abingdon, UK) using CF_4 and O_2 gases. The patterned SiN layer was employed as a mask for anisotropic etching. The inverted pyramid structures were prepared by etching the Si templates with a potassium hydroxide (KOH) solution at 60 °C for 20 min. The SiN layer was removed with a hydrofluoric acid solution.

Fabrication of pyramid-structured memory devices

The fabrication procedure for the pyramid-structured memory device is described in Figure 3.6(b). After cleaning the prepared Si templates with piranha solution, a 100-nm-thick Pt layer was deposited by sputtering (KVS-

2006; Korea Vacuum Technology, Gyeonggi-do, Korea). Heat-curable epoxy (EPO-TEK 377; Epoxy Technology, Billerica, MA, USA) was cast on the Pt layer, and a glass substrate was then placed thereon for use as a supporting layer. After curing the epoxy at 150 °C for 1 h, the Pt pyramid structures attached to the glass substrate were peeled from the templates. Layers of 100-nm-thick NiO and 100-nm-thick Pt were sequentially deposited on the stripped pyramid structures via sputtering. When depositing the Pt layers, the substrate was covered with a mask with 50-μm-diameter holes to provide individual memory cells. For comparison, planar NiO memory devices were also prepared. A flat Si wafer was used as the base substrate, and 10-nm thick Cr, 100-nm-thick Pt, 100-nm-thick NiO, and 100-nm-thick Pt layers were sequentially deposited on the substrate for fabrication of the planar devices.

Characterization

The morphology of the Pt pyramid structures was monitored using scanning electron microscopy (SEM) (Sigma 200; Carl Zeiss AG, Oberkochen, Germany). The pyramid-structured memory device was cut via focused ion beam (FIB) milling (Helios Nanolab 600; FEI Company, Hillsboro, OR, USA), and a cross-section consisting of Pt, NiO, and Pt layers was observed using transmission electron microscopy (TEM) (Tecnai F20 G2; FEI). The electrical properties of the memory devices were measured with a source measurement unit (2643B; Keithley Instruments, Cleveland, OH, USA) under ambient conditions. During the I–V measurements, a bias was applied to the bottom electrode (BE), and the isolated island-shaped top electrode (TE) was grounded.

Electromagnetic finite-element simulation

The electric field and temperature profiles in the pyramid-structured and planar memory devices were simulated using COMSOL Multiphysics software (ALTSOFT, V5.4, AC/DC module). The electric field (E) is given by

$$E = -\nabla V \tag{1}$$

where V is the applied electrical potential. The Joule heating (σE^2) generated by applying E to the devices can be described as follows:

$$\sigma E^2 = C_v \frac{\partial T}{\partial t} - \nabla \cdot (k\nabla T) \tag{2}$$

where σ is the electrical conductivity, C_v is the specific heat per unit volume, and k is the thermal conductivity of the switching material (NiO). The material parameters were obtained from the COMSOL material library. To simulate an instantaneous temperature rise, the SET voltage was set to a short pulse of 1.96 V. The geometric parameters of the memory devices used in the simulation were obtained from TEM measurements (Figure 3.1(b) and Figure 3.7(a)), and the thicknesses of the Pt, NiO, Pt layers were all the same at 100 nm. The taper angle for the pyramid-structured device was 70.6°. The tip radius of the pyramid structure was 25 nm at the BE, 55 nm at the NiO layer, and 135 nm at the TE. The magnitude of the electric field vector was measured along the normal direction of the structure.

3.3. Results and Discussion

To improve the reliability of resistive switching behavior in TCM-based memory devices, this study introduces a structured metal electrode. Pyramid-shaped metal electrodes with extremely sharp tips were fabricated through the template stripping method. This method can fabricate multiple copies of uniform nanometer-scale radius tips with high reproducibility by reusing the same template, preventing the variation in the reliability of the resistive switching behavior that arises when the tips have different radii [24]. NiO was used for the resistive switching layer because it is a well-known switching material for devices based on the TCM [25]. Figure 3.1(a) presents an SEM image of a Pt pyramid-structured electrode fabricated through the lithography technique and template stripping. The Pt pyramids had a uniform base length of 5 μm. The inset in Figure 3.1(a) shows a magnified view of the structure; an extremely sharp Pt tip can be seen. The lithography process can regulate the array size, resulting in good scalability for memory devices. The fabrication method is described in detail in Figure 3.6. After depositing an NiO layer on the structured Pt electrodes, the Pt-top layer was deposited using a sputtering method. The cross-section of the resulting structures was observed via FIB milling and TEM analysis (Figure 3.1(b)). The thickness of both the bottom and top Pt electrodes, and of the NiO layer, was~100 nm. The radii of the Pt-BE and NiO tips were 25 and 55 nm, respectively. The taper angle of the Pt-BE was ~70.6°, consistent with the theoretical value obtained with KOH anisotropic etching of silicon wafers [26].

The most important step for achieving reliable resistive switching behavior

is the forming process [27]. As mentioned in the Introduction, random nucleation and the formation of CFs can lead to unreliable resistive switching behaviors; thus, the forming process should be precisely controlled. To investigate the effect of the pyramid-structured electrodes on the forming behavior, the electroforming process of the device was observed using direct current (DC) sweep analysis. A memory device based on a Pt/NiO/Pt planar structure was also prepared as a reference cell, and Figure 3.2(a) and (b) show the current-voltage (I–V) curves for the electroforming process of the pyramid-structured and planar devices (20 cells of each on a semilogarithmic scale). The forming voltages ($V_{forming}$) of the pyramid-structured RRAM (1.96 ± 0.14 V) were significantly lower than those of the planar RRAM (2.74 ± 0.17 V), as shown in Figure 3.2(c) and (d). Although the standard deviations were not largely improved, it was clear that the pyramid-structured devices could easily form CFs at a lower applied voltage than the planar devices. The low $V_{forming}$ of the pyramid device suggests that robust filaments were produced by a higher-temperature forming process [28]. These robust filaments can greatly improve the reliability of the device because they contribute to stable and uniform resistive switching behavior in specific areas during repeated SET/RESET processes after forming [19,27,29].

Using the structural parameters employed in the TEM analysis and the electroforming results, the electrostatic and thermal properties of the pyramid-structured and planar devices were estimated by finite-element modeling using COMSOL Multiphysics software, to demonstrate the tip effects of the pyramid-structured device. In general, in the TCM-based RRAM devices, the forming

process corresponds to decomposition of the resistive switchable layer (through the redox reaction NiO $\rightarrow$ Ni + 2e⁻ + 1/2O$_2$(g)) via a current-induced temperature rise and consequent formation of metallic nickel (Ni) CFs [30]. When an electric potential of 1.96 V (the V$_{forming}$ of the pyramid-structured device) was applied between the Pt TE and the BE, the electric field was significantly enhanced near the tip region of the Pt BE. The maximum magnitude of the tip-enhanced electric field was 9.82×10^7 V/m, which is about five times larger (1.96×10^7 V/m) than that of the flat region in the pyramid structure, as shown in Figure 3.3(a) and Figure 3.8(a). Hole injection barrier height in the thermochemical reaction can be expressed by [31]:

$$\phi(x) = \phi_B - qEx - \frac{q^2}{16\pi\varepsilon_r\varepsilon_0 x} \tag{3}$$

where ϕ is the hole injection barrier height into the dielectric layer under the Schottky effect, ϕ_B is the Schottky barrier height (the difference between the work function of the electrode and the hole affinity of dielectric materials), q is the charge quantity, E is the electric field, x is the distance from the interface, ε_r is the relative permittivity of dielectric materials, and ε_0 is the vacuum permittivity of dielectric materials. From equation (3), the barrier height for hole injection will decrease due to the tip-enhanced electric field. Therefore, the pyramid-structured electrode with the sharp tip can promote the redox reaction by providing efficient hole injection, preventing recombination between Ni and electrons and promoting the formation of CFs in a confined region [32,33]. Consequently, the CFs could be predominantly formed at the tip region of the pyramid-structured cell. For the planar device, the magnitudes of

the electric fields were 1.96×10^7 and 2.74×10^7 V/m, with potentials of 1.96 and 2.74 V (the $V_{forming}$ of the planar device) applied to the Pt BE, respectively, as shown in Figure 3.2(c) and Figure 3.7(b). The electric field within the NiO layer is uniformly distributed over the entire region, which leads to competitive growth of multiple CFs (Figure 3.7(c)) [34]. The CFs formed in the planar cell can seriously reduce the operational reliability of the device, which will be discussed later.

The Joule heating effects in the pyramid-structured and planar electrodes arising from the applied electric field were also estimated. Several studies have shown that a phase change from the NiO to the Ni-rich phase requires a temperature of 900 K or more [35,36]. A temperature rise of the pyramid and planar structures was observed on application of an electric potential of 1.96 V. As shown in Figure 3.3(b) and Figure 3.8(b), heat was selectively generated only at the tip of the pyramid structure; when the temperature at the tip of the pyramid-structured reached 900 K, other regions remained colder. In other words, tip-enhanced electric fields can induce a temperature rise only at the tip. Hence, the pyramid-structured electrodes provide controlled CF formation at the tip and position-selectivity during resistance switching based on the TCM, unlike in conventional RRAM structures where filaments grow competitively over the entire area. Furthermore, when the temperature distribution in the planar structure was estimated under the same conditions as for the pyramid-structure (applying 1.96 V to the BE), the temperature at the interface between the Pt BE and the NiO layer was about 600 K, with a uniform distribution over the entire surface (Figure 3.3(d)).

To further evaluate the tip-enhanced electric field effect in TCM-based RRAM, the reliability of the pyramid-structured and planar devices under repeated SET/RESET cycles was investigated after the forming process. Figure 3.4(a) and (b) show I–V curves of the SET and RESET process for the pyramid-structured cell, for every 10th cycle out of 100 cycles of DC voltage sweep analysis. Figure 3.4(c) and (d) show the results for the planar reference device under the same conditions. Unipolar resistive switching behaviors were observed in both devices, which operate with the same bias polarity, as reported in previous fuse-antifuse mechanism studies [15,37,38]. As shown in Figure 3.4(e), the pyramid-structured memory device exhibited a relatively low and highly uniform SET/RESET operating voltage compared to the planar memory device. The average and standard deviation of the SET/RESET voltages for the pyramid-structured and planar memory devices were 1.44 ± 0.12 V/ 0.64 ± 0.05 V and 2.07 ± 0.61 V/ 0.90 ± 0.13 V, respectively. While the SET/RESET voltages in the pyramid-structured memory device were clearly distinct from each other, operational failure might occur in the planar memory device due to overlap of the SET/RESET voltages. Figure 3.4(f) presents a cumulative probability graph of the resistance changes for both memory devices over 100 cycles. Each high resistance state (HRS) and low resistance state (LRS) value in the pyramid-structured memory device fell within a narrow distribution compared to that of the planar device. A resistance ratio (R_{HRS}/R_{LRS}) of the pyramid-structured device was 10^2 times larger than that of the planar device. In the retention test, the pyramid-structured memory device was stable over 10^5 s, while the planar device exhibited unstable behavior (Figure 3.4(g) and (h)).

The lower resistance values in the LRS and long retention time for the pyramid-structured device support the conclusion that robust CF formation was promoted by the higher-temperature forming process [29].

Figure 3.5(a) shows a schematic illustration of the resistive switching phenomenon in the pyramid-structured memory device, based on the results obtained thus far. When applying an external potential to the pyramid-structured Pt BE, Joule heating and hole injection are promoted at the tip region of the NiO/Pt BE interface by the tip-enhanced electric fields. As shown in Figure 3.5(b), the enhanced electric field further lowers the energy barrier for the thermochemical reaction of NiO. Due to the Schottky effect, the electric field lowers the hole injection barrier height and increases the emission current [31]. In other words, tip-enhanced electric fields can achieve position-selective formation of CFs, suppressing filament growth outside the tip region. The pyramid-structured device with robust filaments grown only in selected local areas exhibited high reliability, including low and distinct SET/RESET voltages, as well as a long retention time under repeated resistance switching, compared to the planar structured RRAM device. The planar memory device has a higher risk of malfunction due to the large number of CFs grown in the NiO layer, which can lead to overlap of the SET and RESET voltages when the tip-enhanced electric field effect is not present [16,19,34]. It is therefore confirmed that the previously reported tip-enhanced electric field effect has a significant impact on the TCM-based resistive switching mechanism, permitting the implementation of high-performance RRAM in various resistive switching materials and operating mechanisms.

3.4. Conclusions

In this study, we demonstrate via structural and theoretical analysis that tip-enhanced electric fields in a pyramid structure can improve the effectiveness of a thermochemical reaction-based RRAM device. The electric field in the pyramid-structured memory device is enhanced in the tip region, and local heat generation caused by the tip-enhanced electric field lowers the transition barrier height from the NiO to the Ni-rich phase in the tip region alone. As a result, nucleation and growth of CFs are focused in the tip, providing position selectivity during conductive path formation. The resulting RRAM exhibits improved reliability compared to conventional structural devices, including low and distinct forming and SET/RESET voltages, as well as a long retention time. These results are expected to contribute significantly to the development of high-performance RRAM for practical use.

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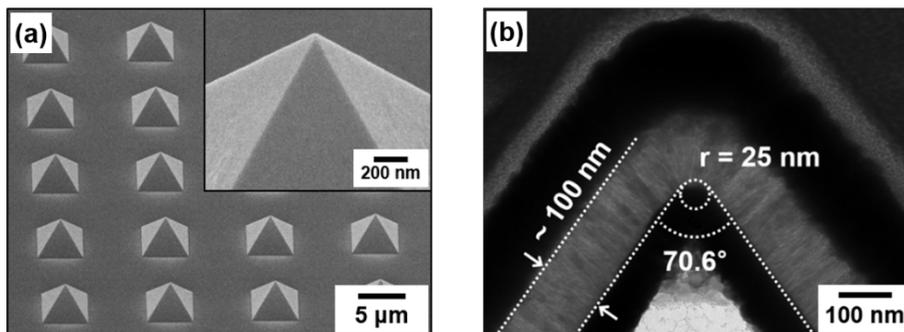
Figure 3.1. (a) SEM image of the Pt pyramid-structured electrode prepared via template stripping. The inset in (a) shows the extremely sharp tip of the Pt pyramid-structured electrode. (b) Cross-sectional TEM image of the memory cell consisting of Pt/NiO/Pt layers.
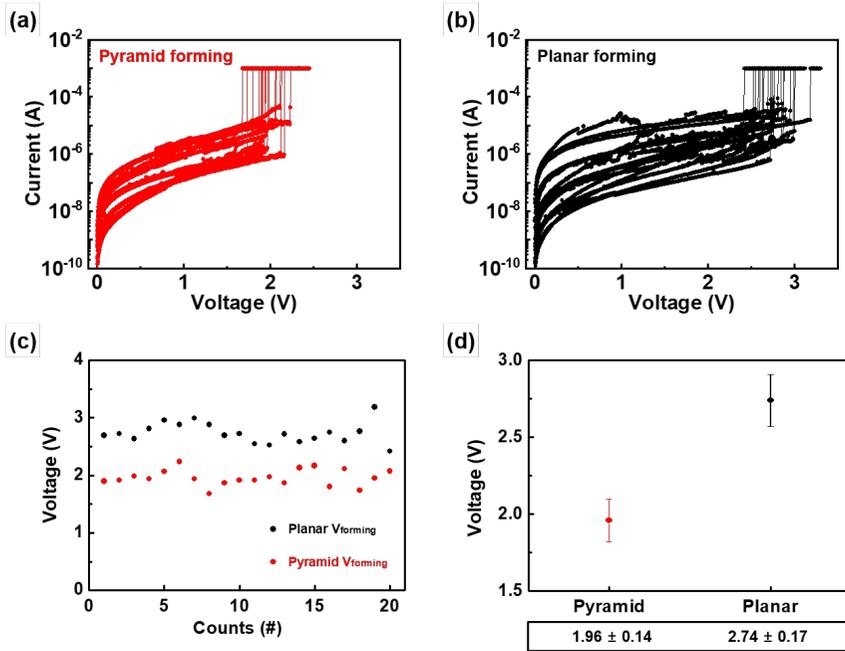
Figure 3.2. *I–V* curves of the electroforming process with the (a) pyramid-structured and (b) planar device, for 20 cells on a semi-logarithmic scale. (c) Variation in $V_{forming}$ during DC sweep analysis for 20 cells. (d) The average and standard deviation of the $V_{forming}$ for the pyramid-structured and planar RRAMs.
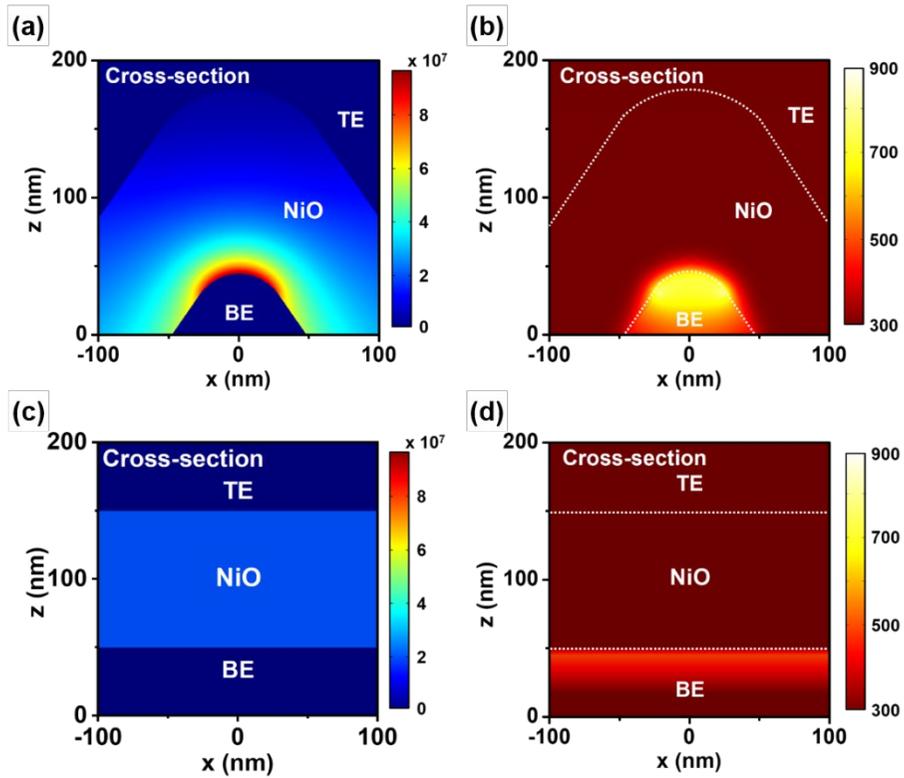
Figure 3.3. Finite-element modeling of the (a) electric field and (b) temperature near the tip with the pyramid structure. (c) Electric field and (d) temperature simulation results of the planar structure.

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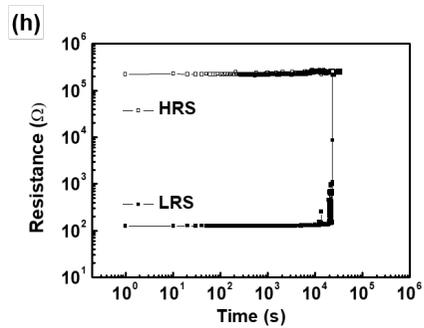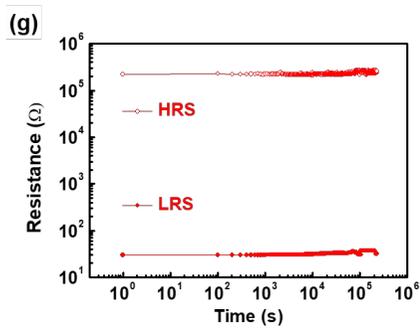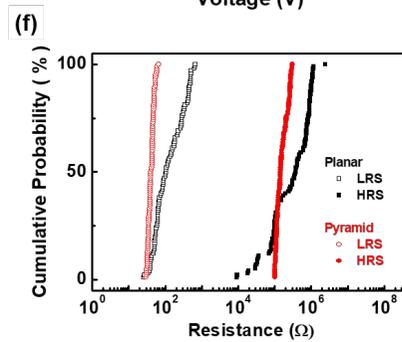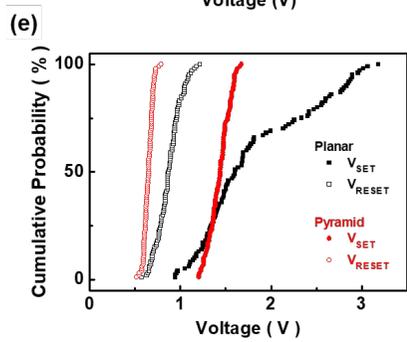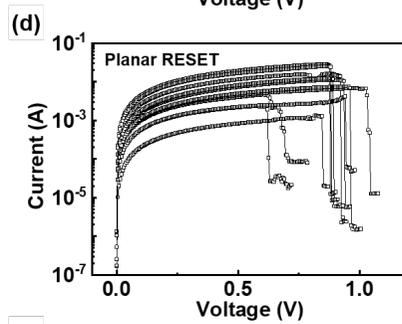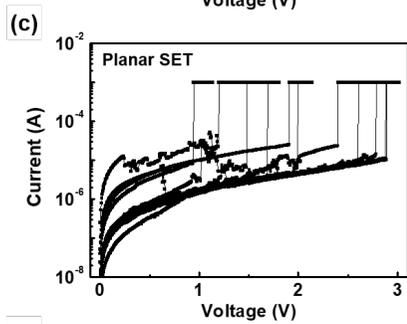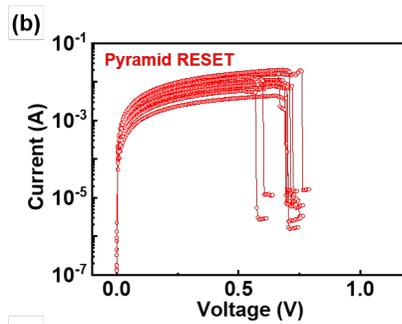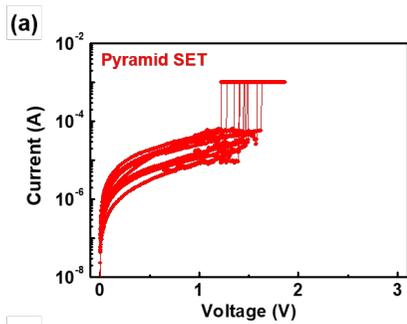
Figure 3.4. *I–V* curves of the memory devices during DC sweep analysis; (a) SET and (b) RESET process for the pyramid-structured memory device. (c) SET and (d) RESET process for the planar memory device. Curves (a) to (d) show every 10th cycle out of 100 cycles. Cumulative probability graph of the (e) SET and RESET voltage and (f) LRS and HRS at the corresponding voltage for 100 cycles. Retention performance of (g) pyramid-structured and (h) planar NiO memory devices.
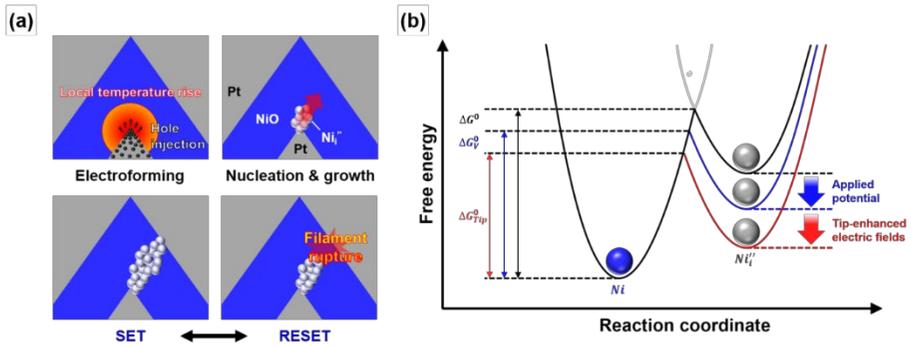
Figure 3.5. (a) Schematic illustration of resistive switching behavior in the pyramid-structured device. (b) Energy diagram of reduction reactions at the anode interface of the NiO pyramid-structured RRAM.

(a)

Si$_3$N$_4$

Si (100)

PR spin-coating & patterning → Si$_3$N$_4$ etching (RIE) → PR removal & Anisotropy etching → Si$_3$N$_4$ removal

~ 5 μm

(b)

Inverted pyramid-structured template → Pt (BE) deposition → Template-stripping → Pyramid-structured electrode → NiO & Pt (TE) deposition

Epoxy
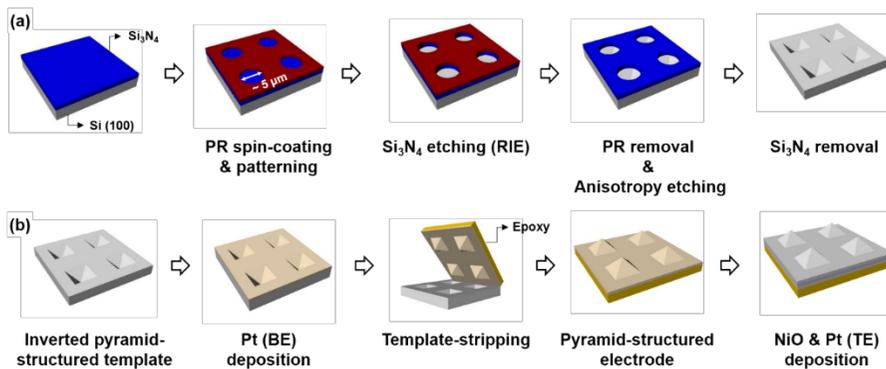
Figure 3.6. Schematic diagram of (a) inverted pyramid-structured Si templates and (b) pyramid-structured Pt electrodes prepared via template stripping.
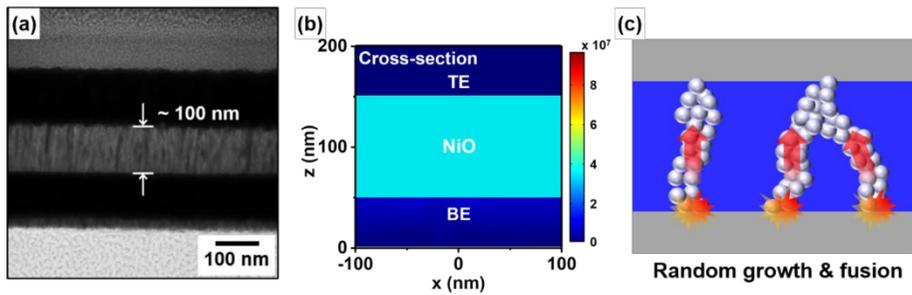
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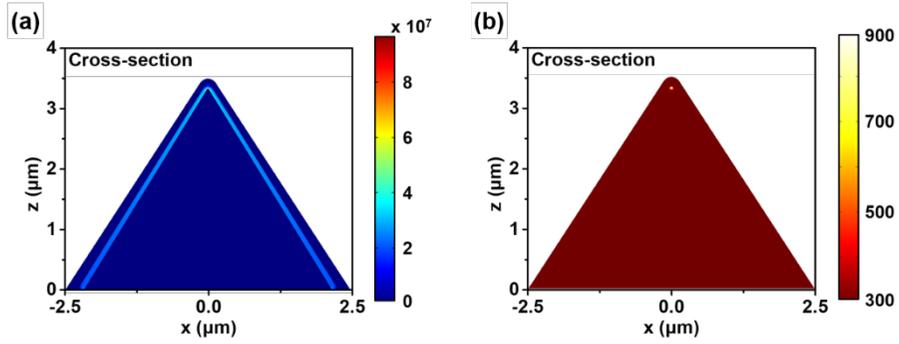
Figure 3.8. Finite-element modeling of the (a) electric field and (b) temperature data of the whole pyramid structure. The potential applied to the BE was 1.96 V, and the TE was grounded. The highest electric field and temperature occurred in the tip area.

	Platinum (Pt)	Nickel oxide (NiO)
Thermal conductivity (k) [W/(m·K)]	71.539	14.185
Heat capacity at constant pressure (C_p) [J/(kg·K)]	132.73	594.14
Density (ρ) [kg/m^3]	21385	7438.4
Relative permittivity (ε_r) [-]	-	11.9
Electrical conductivity (σ) [S/m]	8.68×10^6	$\sigma = \sigma_0 \exp\left(\frac{V}{V_0}\right)^*$

*σ_0 = 4.05 S/m, V_0 = 0.39 V

Table 3.1. The material parameters for the simulation from the COMSOL material library.

Chapter 4. Facile Achievement of Complementary Resistive Switching Behaviors via Self-Assembled Block Copolymer Micelles[*]

Complementary resistive switch (CRS) memory consisting of two anti-serial resistive random access memory (RRAM) cells have attracted considerable attention for its advantages such as leakage current suppression, ultra-high integration, and low power consumption. However, fabricating a multilayered cell by stacking two RRAM cells requires an additional complex fabrication process. This study shows that self-assembled block copolymer (BCP) micelles chelated with metal precursors can easily achieve CRS behavior through a simple process. The spherical metal nanostructures locally enhance the electric fields, and the enhanced electric fields promote Joule heating and redox reactions of electrochemically active metals. The resulting devices exhibit reliable CRS behavior with four distinct threshold voltages in both cycle-to-cycle and cell-to-cell tests. Also, the resistive switching mechanism and conducion model are demonstrated through the detemination of the temperature coefficient of resistance and the analysis of the current–voltage (I–V) data plot. This approach can easily achieve memory devices exhibiting CRS behavior, and can lead to the development of large area, high integration, and low energy consumption data storage devices.

4.1. Introduction

Resistive random access memory (RRAM) is a non-volatile memory in which resistance states can be modulated by external electrical stimuli [1]. RRAM has been actively researched due to its remarkable advantages such as simple structure and low power consumption [2]. Furthermore, ultra-high density can be achieved by setting the unit cell size to $4F^2$ (F is the feature dimension) through the passive crossbar array architecture [3]. However, the sneak-path problem, which reduces the read-out sense margin, increases the power consumption, and limits the array size, is a significant hurdle to realizing the practical use of RRAMs [4]. To suppress the undesired leakage current, many approaches have been attempted to make the nonlinear RRAM cells in a low resistance state (LRS). For example, nonlinear circuit elements such as diode, transistor, and selector were characterized, connecting in series with each RRAM cell [5-7]. Even though the integration of the elements and cells can mitigate the leakage currents, the applicable element type is different according to the RRAM type, so appropriate one should be adopted [3]. Therefore, a distinct method achieving current–voltage (I–V) nonlinearity is required.

The complementary resistive switch (CRS) cell consists of two RRAM cells that are anti-serially connected together by sharing an intermediate electrode [4]. In a CRS cell, the information of '0' or '1' is defined by indicating that one of the RRAM cells is in a high resistance state (HRS) and the other in a LRS [8]. The total resistance of the cell is always high even if a '0' or '1' is stored, so it can effectively suppress the leakage current through the unselected cells, as well as greatly reduce energy consumption under the steady state [9]. In

addition, CRS cells are made up of a series of known resistive switching materials, so they can be designed into a variety of material systems [10].

Many efforts have been made to fabricate multilayer structures showing CRS behavior. In general, devices based on electrochemical metallization (ECM) or valence change memory types of bias-polarity-dependent materials have been reported as suitable systems. For example, device structures of ECM type $Pt/SiO_2/GeSe/Cu/GeSe/SiO_2/Pt$ and $Pt/HfO_x:N/Ag/ HfO_x:N/Pt$ and VCM type $Pt/Ta_2O_{5-x}/TaO_{2-x} /Pt/TaO_{2-x} /Ta_2O_{5-x} /Pt$ and $IrO_x/GdO_x/Al_2O_3/TiN$ have been prepared [4,11-13]. However, stacking two RRAM cells to fabricate a multilayered structure requires an additional fabrication process, so techniques that simplify fabrication complexity should still be pursued.

The ability of the amphiphilic block copolymer (BCP) to self-assemble into regularly ordered nanostructures when dissolved in a selective solvent provides uniform and high-density features at nanoscale [14-16]. Micellar aggregates form a core-shell architecture in an aqueous media [17]. The core-shell structured micelles can form a BCP/metal compound through metal precursor salts that can be selectively dissolved into the core polymer, and then form a metal nanocrystal array at room temperature through a simple process [18]. In addition, it is feasible to change the size, density and type of nanoparticles by changing the molecular weight of the copolymer and the type of metal precursor [19,20]. Thus, designing materials constituting the BCP/metal compound micelles and forming the nanoparticles by self-assembly can be an effective strategy to fabricate the multilayered structure simply and easily.

In this study, we report a facile approach to achieving the CRS architecture

with nanostructures of self-assembled BCP/metal compound micelles. BCP and metal precursors were dissolved in selective solvent ia for use as BCP/metal compound micelles. These micelles were used as CRS layers and the mechanism of CRS behavior was investigated. Based on numerical simulation and experimental results, we confirmed that the devices exhibit CRS behavior through an ECM mechanism that promotes redox reactions and ion migration through locally enhanced electric field and Joule heating. The resulting memory device exhibited stable CRS behavior in the repeated DC cycle test, and in particular, the cell-to-cell test result was reliable owing to the uniformly arranged morphology over the entire area. Therefore, this approach can provide a solution to the sneak-path problem by easily achieving the CRS behavior through a simple process.

4.2. Experimental

Preparation of BCP/metal compound micelle

Polystyrene-*b*-poly(2-vinylpyridine) (PS-*b*-P2VP, PolymerSource Inc.) were used as purchased. The number average molecular weight of PS-*b*-P2VP was 40,000-*b*-18,000 g mol^{-1}. The polydispersity index was 1.07. PS-*b*-P2VP was dissolved in toluene (Sigma-Aldrich, 6.25 mg ml^{-1}), and stirred for 1 h at room temperature. A copper(II) chloride ($CuCl_2$, Sigma-Aldrich) was added to the micellar solutions and stirring for at least 48 h at room temperature. The molar ratio of CuCl2/vinyl pyridine unit was adjusted to 0, 1, and 4. The PS-*b*-P[2VP($CuCl_2$)] solution was centrifuged at 10000 rpm for 15 min and then filtered through a syringe filter.

Device fabrication

On a cleaned glass substrate (thickness of 0.7 mm and area of 15×15 mm^2), a 50-nm-thick Al was deposited on the substrate covered with metal mask (50 μm line width) via a thermal evaporator (KVE-T4004L; Korea Vacuum Technology) and used as the bottom electrode (BE). The BCP-metal compound micelles were spin-coated at 500 rpm for 5 s and then at 2000 rpm for 30 s on the BE. Finally, a 50-nm-thick Al was deposited by the thermal evaporator using the metal mask and used as the top electrode (TE). The TE was aligned perpendicular to the BE to form 8×8 cross-bar array architecture (individual cell junction area of 50×50 μm^2).

Characterization

The morphology of the BCP-metal compound micelle layer was observed using scanning electron microscopy (SEM, Sigma 300; Carl Zeiss AG). The dimensions of the micelle layer were measured with scanning transmission electron microscopy (STEM, Talos F200X; FEI Company) and atomic force microscopy (AFM, XE-100; Park Systems). The distribution of elements was performed using energy dispersive X-ray spectroscopy (EDS, XFlash 6-10, Bruker) and angle resolved X-ray photoelectron spectroscopy (ARXPS, K-Alpha$^+$, Thermo Fisher Scientific). The electrical properties of devices were measured with a source measurement unit (2643B; Keithley Instruments) under ambient conditions. During the I–V measurement, a bias was applied to the TE, and the BE was grounded. The applied voltage range was from 0 to 5 V for positive and 0 to -5 V for negative, and the voltage sweep rates were 0.1 and -0.1 V s^{-1}, respectively. The temperature dependence of the I–V characteristics was analyzed with a hot chuck controller (MST-1000B; MS TECH). The temperature was increased from 303K to 363K, (as a heating rate of 1K min^{-1}).

Finite-element simulation

The electric field and temperature profiles in the device were simulated using COMSOL Multiphysics software (ALTSOFT, V5.4, Electromagnetic heating module). The electric field (E) is given by

$$E = -\nabla V \tag{1}$$

where V is the applied electrical potential. The heat (Q_e) generated by an electric current in the device can be described as follows:

$$Q_e = J \cdot E \tag{2}$$

where J is the current density. J is the product of the electrical conductivity σ and E. The heat transfer equation in solids interface is given by

$$\rho C_p \mathbf{u} \cdot \nabla T = \nabla \cdot (k \nabla T) + Q_e \tag{3}$$

where ρ is the density, C_p is the specific heat capacity, T is a temperature, and k is the thermal conductivity of the dielectric material. The material parameters were obtained from the COMSOL material library. The electric potential was applied to the TE, and the BE was grounded. The geometric parameters of the device used in the simulation were established based on STEM. The geometries of the Cu and PS layer/electrode interfaces were assumed to be spherical and planar, respectively. The thicknesses of the TE, BE, and PS layer were 50, 50, and 50 nm, respectively. The diameter of the Cu sphere was set to 25 nm, and the thickness of the upper and lower PS layers were assumed to be the same. The direction of the electric field is indicated by arrows.

4.3. Results and Discussion

The detailed preparation process of the BCP micelles coordinated with metal precursors and fabrication method of the devices are described in the Experimental Section. Figure 4.1(a) is a schematic diagram of the formation process of the BCP micelles loaded with metal precursors. PS-*b*-P2VP (40,000-*b*-18,000 (g mol^{-1})) was used as the BCP to form micelles when dissolved in a hydrophobic solvent. The PS block of the copolymer is shown in red and the P2VP block is shown in blue. In toluene that selectively dissolves only the PS block, the BCP spontaneously self-assemble into spherical micelles with a soluble PS corona and an insoluble P2VP core [19,21]. After the PS-*b*-P2VP was completely dissolved in the toluene, Cu precursors were loaded and stirred. Cu ions can be selectively coordinated into the P2VP block by adding CuCl$_2$ (Cu precursors) into the solution [22]. Finally, the solution was centrifuged to remove the uncoordinated Cu precursors with the P2VP block.

A schematic diagram of fabricating memory devices using the prepared solution is shown in Figure 4.1(b). The BCP micelles coordinated with metal precursors were spin-coated on the BE deposited on the glass substrate. After drying the solvent completely at room temperature, the TE was deposited. The fabricated device consisted of Al / PS / P[2VP(CuCl$_2$)] / PS / Al layers, which correspond to the metal/insulator/metal/insulator/metal layers used in previous studies that achieved ECM type CRS behavior, respectively [4].

Figure 4.2 shows the dimension and structure analysis of the compound micelles and the distribution analysis of Cu ions in the micelles. Figure 4.2(a) presents a SEM image of the BCP-metal compound micelle layer spin-coated

on the BE. Spherical micelles spontaneously self-assembled in toluene formed periodic nanostructures with hexagonal packing over large areas. Figure 4.2(b) shows surface morphology of the micelles observed using AFM. The right side of Figure 4.2(b) shows the line scan extracted from the left side of Figure 4.2(b). The height from the valley to the top was up to 10 nm and the distance between the highest points was about 50 nm.

The morphology of the micelles and the horizontal distribution of Cu elements were observed through STEM with EDS (Figure 4.2(c)). The diameter of P2VP core was estimated ~25 nm and the center-to-center distance between micelles was estimated ~50 nm. The center-to-center distance corresponds to the distance between the highest points shown in Figure 2b. In addition, the EDS result indicated that the Cu ions were mostly present in the P2VP core blocks. The vertical distribution of the Cu elements was confirmed through ARXPS (Figure 4.6). The intensity of the C 1s spectra, which is the main component of the PS blocks and P2VP blocks, was maintained even when the tilt angle increased. However, the intensity of the Cu 2p spectra combined with the P2VP blocks and the N 1s spectra constituting the P2VP blocks gradually decreased. These results suggest the micelles consisted of P2VP core blocks and PS shell blocks, and that the added Cu ions were mainly located in the core blocks.

Figure 4.2(d) shows the schematic diagram and the determined dimensions of the nanostructured micelles coated on the electrode. Based on the above results, it is estimated that the diameter of the P2VP core block is ~25 nm, the length of the PS block corresponding to the distance between the core blocks is

~25 nm, and the height from the valley to the top of the PS block is ~10 nm.

To demonstrate the effect of the electric field enhanced by spherical micelle nanostructures on CRS behavior, the electrostatic and thermal properties of the PS-*b*-P[2VP(CuCl$_2$)] compound micelle devices were estimated through finite-element modeling using COMSOL Multiphysics software. As mentioned, when the CRS devices following the ECM mechanism operate, electrochemically active metals are oxidized and reduced by external electrical stimulation [24]. The electric field generated by the voltage difference between the electrodes acts as a driving force that migrates metal ions oxidized from the anode through the insulator (ion conducting medium) and reduces the ions to metal atoms on the cathode [25]. Therefore, the electric field generated in the insulator acts as a driving force for the ionization of the metals and the migration of the ions [26,27].

Figure 3 shows the *I*−*V* curve of the fabricated device obtained through a direct current (DC) sweep analysis and simulation results. The geometry used in the simulation was based on the dimensions in Figure 2, and the coordinated Cu ions in the core blocks were assumed to be spherical. In the CRS devices consisting of two anti-serial RRAM cells, it is called '0' state when the upper RRAM cell is in HRS and the lower one is in LRS [4]. The opposite case is referred to as '1' state, and when both cells are in LRS, this state is defined as 'ON' [4]. In this study, since a negative voltage was applied during the forming process, the device was in '1' state before DC sweep. As shown in Figure 4.3(a), under the positive voltage $V_{th,1}$, the electrical simulation result exhibited the locally enhanced electric field due to the spherical metal structure. Since the

enhanced electric field can lower the energy for ionization of Cu atoms and migration of the oxidized Cu ions to the cathode, a local CF could be easily formed toward the cathode.

Figure 4.3(b) shows the thermal simulation result of Joule heating effect by the current passing through the CF in the 'ON' state. By the current passing through the CF, the Cu filament was electrochemically dissolved with the help of local temperature increase due to Joule heating [28]. Furthermore, as an electron transfer reaction was thermally improved, redox reaction occurred near the hot spot of the filament. At this time, the oxidized Cu ions migrated to the direction of the electric field and were reduced back to Cu atoms at the cathode. Since these phenomena are affected by the electric field, they occurred predominantly in the locally enhanced electric field region until $V_{th,2}$.

As shown in Figure 4.3(c), in the voltage range higher than $V_{th,2}$, the upper CF was ruptured and switched to the '0' state. In the '0' state, even when the positive voltage is applied, the electric field hardly affects the lower CF, so that the state remained stable. Figure 4.3(d), 4.3(e), and 4.3(f) exhibit electric field and temperature simulation results when negative voltage is applied, suggesting that the same phenomenon that occurred at positive voltage could occur due to the locally enhanced electric field by spherical micelle nanostructures.

To evaluate the performance of the CRS memory devices, the electrical properties were characterized. Figure 4.4(a) shows semilogarithmic $I-V$ curves of the micelle device obtain through the repetitive DC voltage sweep for 20 cycles in a single cell. A representative curve is shown in red. Four threshold

voltages with abrupt changes in resistance state were observed. The $V_{th,1}$ and $V_{th,2}$ under the positive voltage were 1 and 3 V, respectively. Under the negative voltage, the $V_{th,3}$ and $V_{th,4}$ were -1.1 and -2.8 V, respectively, which were symmetrical to the positive voltage. These results suggest that the symmetrical CRS behavior and similar threshold voltage between positive and negative originated from the symmetric micelle structure. A resistance ratio (R_{HRS}/R_{LRS}) of the device was maintained about 10^3 during 20 cycles. The high resistance difference as the resistance state changes resulted of the formation of a robust CF by the locally enhanced electric field. Each threshold voltage that switches the '0' or '1' or 'ON' state was clearly distinguished.

The write and read operations of the device are determined based on the threshold voltage. In particular, the voltage for the read operation is determined between $V_{th,1}$ and $V_{th,2}$ or between $V_{th,3}$ and $V_{th,4}$, so it is important to no overlap the threshold voltages for repeated cycles in order to avoid operational failure. Figure 4.4(b) provides the cumulative probability of threshold voltages for 20 cycles. The average and standard deviation of the $V_{th,1}$, $V_{th,2}$, $V_{th,3}$, and $V_{th,4}$ for the micelle memory devices were 1.05 ± 0.29, 3.01 ± 0.41, -1.12 ± 0.27, and -2.84 ± 0.32 V, respectively. Threshold voltages that are clearly distinguishable in repetitive operation ensure the reliability and availability of read and write operations.

Figures 4.4(c) and 4.4(d) show the semi-log $I-V$ curve and the cumulative probability of the threshold voltage for randomly selected 20 cells. The $V_{th,1}$ and $V_{th,2}$ under the positive voltage were 1.3 and 3.4 V, respectively, and $V_{th,3}$ and $V_{th,4}$ under the negative voltage were -1.1 and -3.1 V, respectively. The

average and standard deviation of the $V_{th,1}$, $V_{th,2}$, $V_{th,3}$, and $V_{th,4}$ for 20 cells were 1.29 ± 0.17, 3.29 ± 0.21, -1.17 ± 0.15, and -3.09 ± 0.16 V, respectively. Each threshold voltage for 20 cells exhibited a very narrow distribution and did not overlap. These results indicate that the PS-*b*-P[2VP(CuCl$_2$)] compound micelles were uniformly coated over the entire area. Therefore, the micelle memory can implement uniformity and stable CRS switching between cells, manifesting that the reproducibility in cross bar array are guaranteed.

To investigate the resistive switching mechanism of the PS-*b*-P[2VP(CuCl$_2$)] compound micelles, the *I*−*V* curves of the devices were characterized at different temperatures. Figure 4.5(a) shows the temperature dependence of the current in the 'ON' state. To determine the temperature dependence of the current flowing through the CF between the electrodes, the state of the device was intentionally switched to the 'ON'. The threshold voltage and compliance current were 1.6 V and 0.1 mA, respectively. As the temperature increased from 303 to 363 K, the current value gradually decreased and the resistance gradually increased, indicating that the formed CF in the 'ON' state exhibits metallic behavior. The resistive switching mechanism can be supported by temperature coefficient of resistance (TCR). As shown in Figure 4.5(b), the resistance of the PS-*b*-P[2VP(CuCl$_2$)] compound micelles memory device in 'ON' state was observed in the temperature range of 303–363 K. According to the TCR equation, the value of resistance at a temperature T, R(T), is given by [29]

$$R(T) = R_0[1 + \alpha(T - T_0)] \qquad (4)$$

where R_0 is the resistance at temperature T_0 (303 K). The TCR was estimated to be about 1.46×10^{-3} K^{-1}, which is close to the value of Cu

nanowires with width of 44 nm (2.5×10^{-3} K^{-1}) [30]. Thus, it was confirmed that the Cu filament was formed in the insulating layer to participate in resistive switching behavior of the device.

The *I–V* data plot analysis of the devices shown in Figure 4a was carried out using conduction models. Figure 4.5(c) and 4.5(d) show the double-logarithmic *I–V* curves in HRS and LRS, respectively. The *I–V* curve in the HRS can be divided into two regions; the blue line with a slope of ~1.18, and the green line with a slope of ~1.74. These results indicate that the conduction mechanism follows the ohmic conduction model in a low voltage region and then changes to space-charge-limited current (SCLC) model until the threshold voltage [31]. The *I–V* curve in the LRS, which is linear with a slope of ~1.11 (yellow line). This suggests that the electrical conduction of the device in the LRS is dominated by ohmic conduction. This behavior in HRS and LRS is the same as that of resistive switching device based on ECM mechanism [32]. Therefore, the fabricated device is a ECM-type device by switching the resistance state through the formation and dissolution of the Cu filament.

4.4. Conclusions

In this study, we demonstrate the simple approach to fabricating the memory devices that exhibit CRS behavior can be easily fabricated using PS-*b*-P[2VP(CuCl$_2$)] compound micelles. A uniform spherical nanostructure layer is formed on the electrode by spin-coating the micelle solution chelated with the Cu precursors. The locally enhanced electric field achieved by the spherical nanostructure lowers the energy for ionization of Cu atoms and the migration of ionized Cu ions, facilitating ECM mechanism. The resulting RRAMs exhibit stable and reliable CRS operation, including the non-overlapping and narrow distribution of the threshold voltages. These results are expected to promote practical use of RRAM by providing a solution to the sneak-path issue through the facile achievement of CRS behavior.

4.5. References

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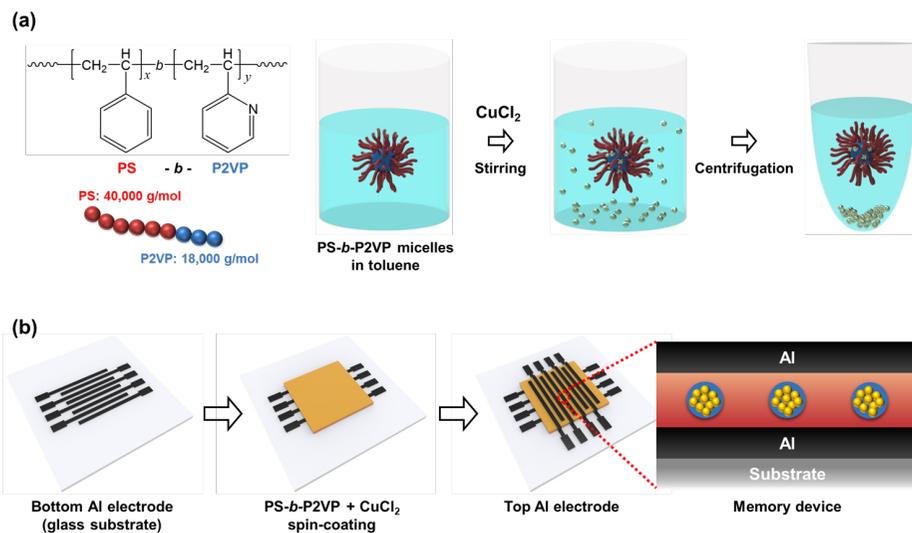
Figure 4.1. (a) Schematic diagram of preparation of PS-*b*-P[2VP(CuCl$_2$)] solution. The number average molecular weight of PS-*b*-P2VP was 40,000-*b*-18,000 g mol^{-1}. In toluene, PS-*b*-P2VP were spontaneously self-assembled into spherical micelles. (b) Schematic diagram of fabricating memory devices using the PS-*b*-P[2VP(CuCl$_2$)] solution. The fabricated devices consisted of Al / PS / P[2VP(CuCl$_2$)] / PS / Al layers.
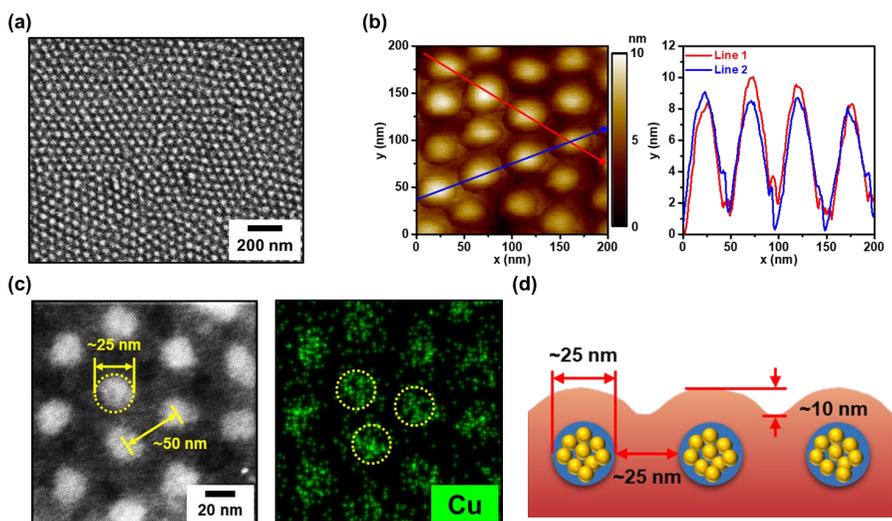
Figure 4.2. (a) A scanning electron microscopy (SEM) image of the PS-*b*-P[2VP(CuCl₂)] compound micelles spin-coated on the bottom electrode (BE). (b) An atomic force microscopy (AFM) image and line profile of the micelles. The height from the valley to the top was up to 10 nm and the distance between the highest points was about 50 nm. (c) A scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDS) images the micelles. The diameter of P2VP core was estimated ~25 nm and the center-to-center distance between micelles was estimated ~50 nm. (d) Schematic diagram and the determined dimensions of the micelles spin-coated on the BE.
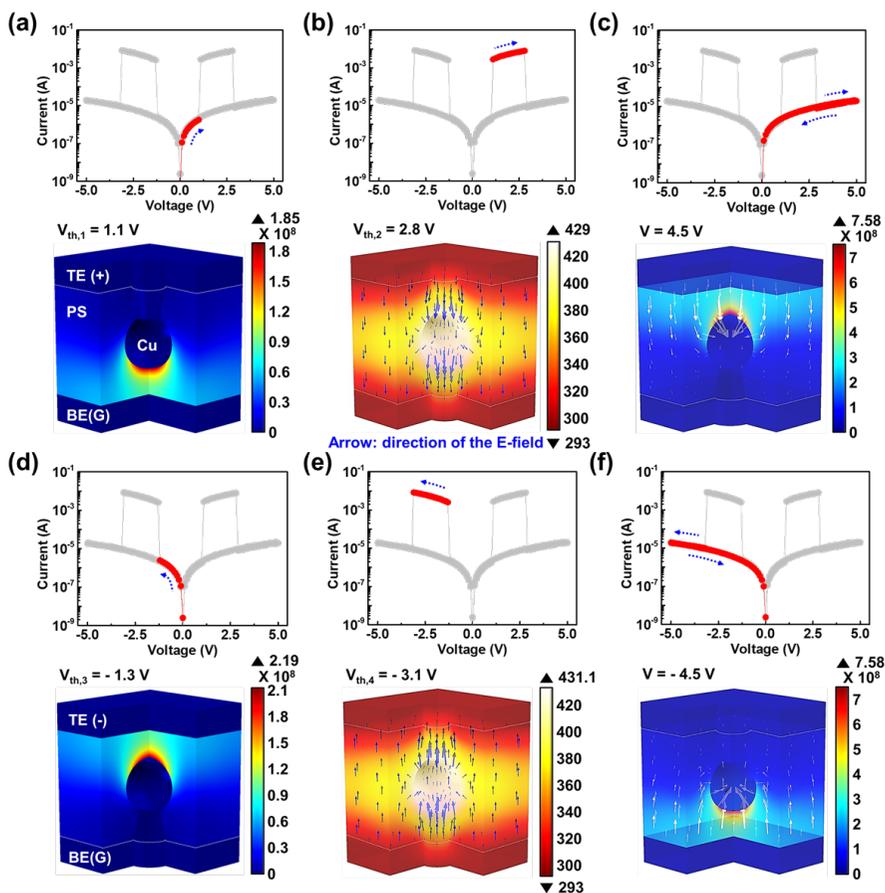
Figure 4.3. Representative current–voltage (I–V) curve of the micelle device and finite-element modeling of the electric field in the micelle device structure. The coordinated Cu ions in the P2VP blocks were assumed to be spherical. The potential applied to the top electrode (TE), and bottom electrode (BE) was grounded. The $V_{th,1}$ and $V_{th,2}$ under the positive voltage were 1.3 and 3.4 V, respectively. The $V_{th,3}$ and $V_{th,4}$ under the negative voltage were -1.1 and -3.1 V, respectively. The Cu diameter and the PS thickness for the structure were set to 25 nm and 50 nm, respectively. Arrows indicated the direction of the electric field.
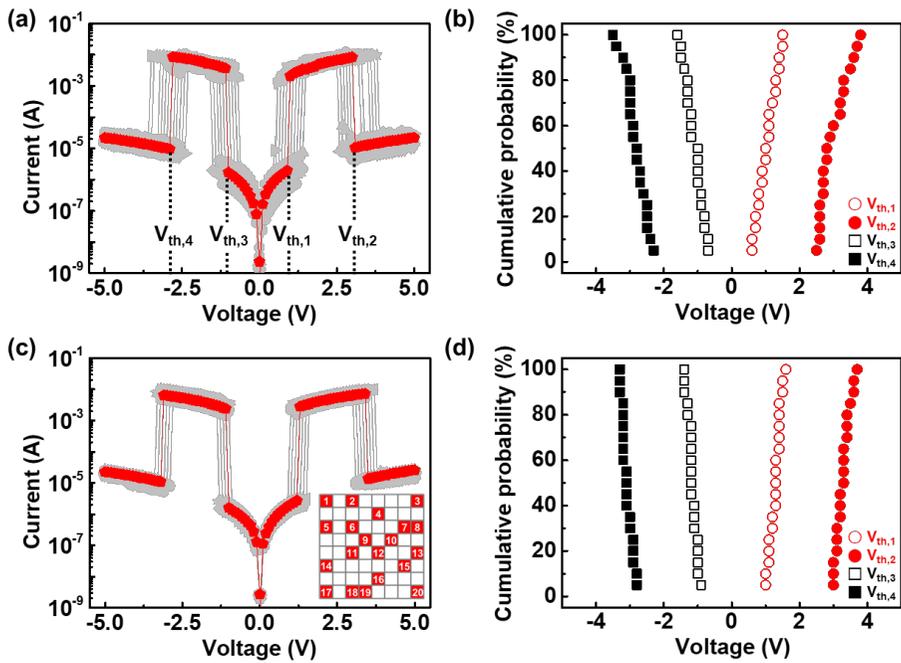
**Figure 4.4.** (a) Current–voltage (*I–V*) of the memory device during direct current (DC) sweep analysis for 20 cycles in a single cell and (b) cumulative probability graph of threshold voltages in the (a). (c) *I–V* curve of the memory device for randomly selected 20 cells of the micelle memory device and (d) cumulative probability graph of threshold voltages in the (c).
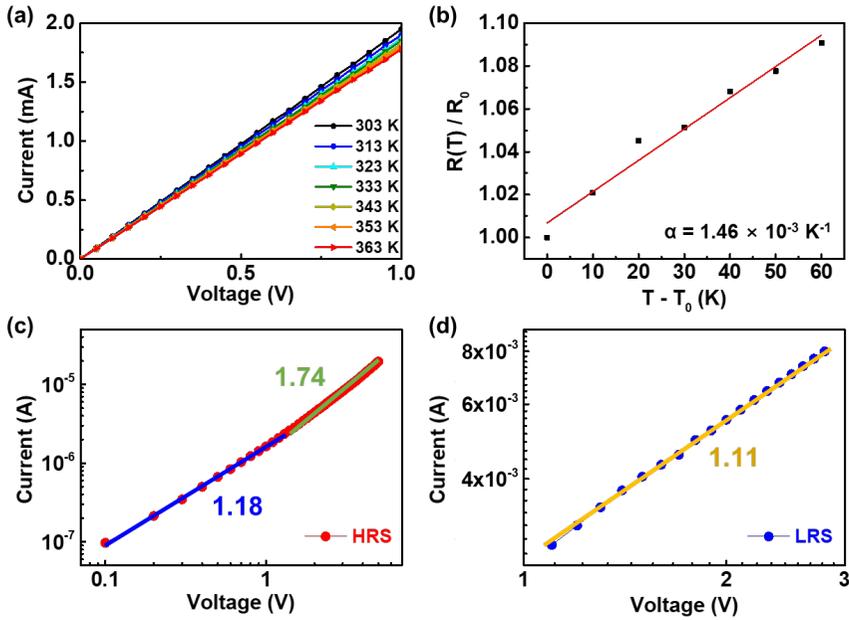
Figure 4.5. (a) Current–voltage (*I–V*) curves of the micelle device in the 'ON' state at different temperatures. The temperature range was 300–363 K. (b) Temperature coefficient of resistance (TCR) of the micelle device measured in the (a). According to the TCR equation of $R(T) = R_0[1 + \alpha(T - T_0)]$, where R_0 is the resistance at temperature T_0 (303 K). The TCR was estimated to be about 1.46×10^{-3} K^{-1}, which is close to the value of Cu nanowires with width of 44 nm (2.5×10^{-3} K^{-1}). Double-logarithmic *I–V* curves in (c) high resistance state (HRS) and (d) low resistance state (LRS) for the micelle device. The symbols are the measured data and the solid lines represent linear regression. The slope of the *I–V* curve in HRS changed from ~1.18 to ~1.74, indicating a change in the conduction mechanism from ohmic conduction to space charge limiting conduction (SCLC). The slope of the *I–V* curve in LRS was ~1.11, which indicates ohmic conduction.
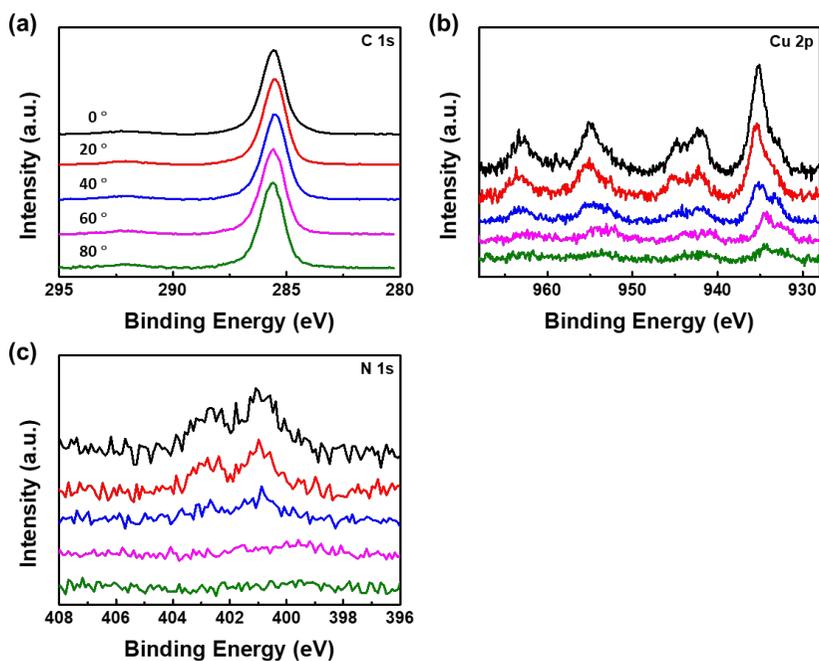
Figure 4.6. Angle-resolved X-ray photoelectron spectroscopy (ARXPS) spectra of PS-*b*-P[2VP(CuCl₂)] compound micelles for the (a) C 1s, (b) Cu 2p, and (c) N 1s regions. The angle was tilted from 0 to 80°. The intensity of the C1s spectra, which is the main component of the PS blocks and P2VP blocks, was maintained even when the tilt angle increased. However, the intensity of the Cu 2p spectra combined with the P2VP blocks and the N 1s spectra constituting the P2VP blocks gradually decreased. These results suggest the micelles consisted of P2VP core blocks and PS shell blocks, and that the added Cu ions were mainly located in the core blocks.
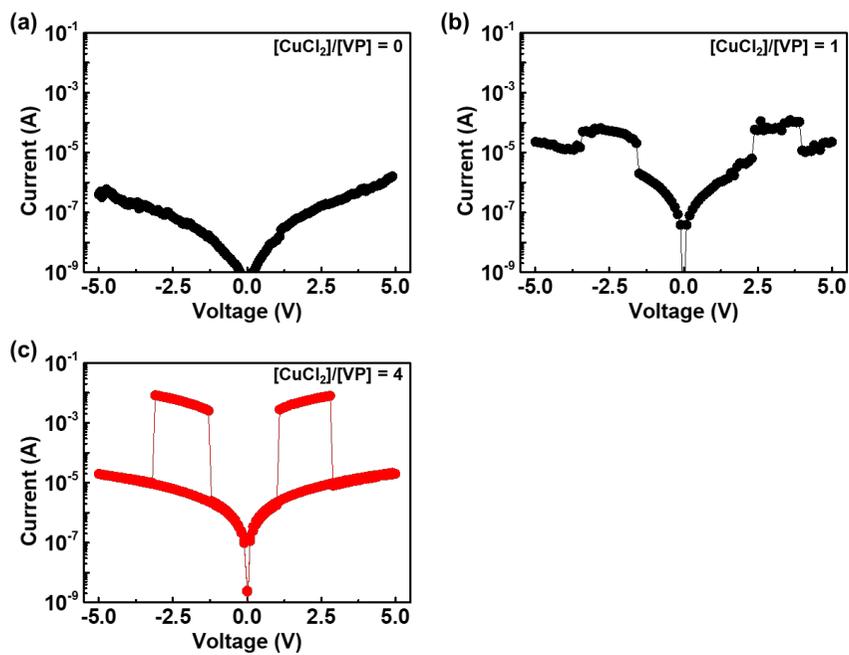
Figure 4.7. Representative *I–V* curves according to the molar ratio of CuCl$_2$/vinyl pyridine unit. The molar ratio of CuCl$_2$/vinyl pyridine unit was adjusted to (a) 0, (b) 1 and (c) 4.

Chapter 5. Conclusions

In this dissertation, the novel designs and methodologies were proposed to improve the operational performance and reliability of RRAM devices. Introduction of nanostructures for locally enhanced electric field in devices was suggested as the strategy to fabricate memory devices with low and reliable operating voltage, improved retention time, and large resistance ratio through stable resistive switching behavior. In particular, based on the simulation and experimental results, the effect of electric field enhancement on resistance switching behavior and device performance was systematically investigated in various mechanism systems.

For the charge trapping/de-trapping mechanism in the organic-based RRAM, the locally enhanced electric fields achieved by the pyramid-structured electrode can facilitates charge injection at the electrode/PI interface and charge transport through the PI switching layer, creating location-controlled conductive paths. As a result, the pyramid-structured PI-based RRAM exhibited considerably improved operational performance over those of previous studies. Moreover, controlling the location of the conductive path via the pyramid-structured electrode helped to systematically elucidated the switching behavior of PI-based RRAM.

For the thermochemical mechanism in the transition metal oxide-based RRAM, enhanced electric fields in the pyramid structured electrode with the sharp tip can improve the efficiency of the thermochemical reaction-based RRAM. The electric field in the pyramid-structured RRAM was enhanced in

the tip area, and local heat generation caused by the tip-enhanced electric field reduced the transition barrier height from the NiO to the Ni-rich phase at the tip area. As a result, nucleation and growth of CFs were focused in the tip, offering position selectivity during CFs formation. The resulting transition metal oxide-based RRAM exhibited enhanced reliability compared to the conventional planar structured devices, including low and distinct forming and SET/RESET voltages, as well as a long retention time.

For the electrochemical metallization mechanism in the CRS memory, the electric field enhancement of the spherical metal nanostructure utilizing BCP micelles can achieve the CRS behavior based on the ECM mechanism. The PS-b-P[2VP(CuCl$_2$)] compound micelles, in which the Cu precursors were selectively chelated to the P2VP block, were employed as the intermediate layer of the memory. The locally enhanced electric field achieved by the spherical Cu nanostructure lowered the energy for ionization of Cu atoms and the migration of ionized Cu ions. As a result, nucleation and growth of CFs were predominantly occurred in the selective regions, achieving location controlled CFs formation exhibiting CRS behavior. The resulting RRAMs exhibited stable and reliable CRS operation, including the non-overlapping and narrow distribution of the threshold voltages.

In conclusion, this dissertation provides experimental and theoretical bases for improving operational performance and reliability of RRAMs, focusing on (i) the charge trapping/de-trapping mechanism in organic material-based RRAM, (ii) the thermochemical mechanism in transition metal oxide-based RRAM, and (iii) the ECM type CRS memory via the local enhancement of

electric fields through nanostructures. Engineering of nanostructures that can manipulate electric fields is an effective strategy for improving the performance of memory devices. In particular, the proposed device designs and fabrication methods are expected to contribute significantly to the development of high-performance RRAM for practical use. Furthermore, the approach through engineering the nanostructure explained in the dissertation can be universally applied to other electronic devices that require improvements in device performance.

Abstract in Korean

   본 논문의 목적은 나노 구조체를 통한 전자 장치 내 국부적 전계 향상 효과를 조사하고, 이의 실제 사용을 위한 실험 및 이론적 기반을 제공하는 것이다. 저항변화메모리 (resistive random access memory)는 외부 전기 자극에 의해 저항 상태를 변화 시킬 수 있는 데이터 저장 장치이다. 두 전극 사이에 인가된 전위차에 의해 생성된 전기장은 저항 상태를 전환시키는 구동력으로써 작용하므로, 전자 장치 내에서 전기장을 제어하면 장치의 성능과 신뢰성을 향상시킬 수 있다. 장치 내에서 전기장을 제어하려는 많은 노력을 통해 상당한 진전이 있었지만, 안정적이고 균일한 저항 변화 거동을 위해 의도된 위치에서 전기장을 선택적으로 향상시키는 일은 아직 도전적 과제이다.

   구조화된 금속을 저항변화메모리에 접목시킴으로써 전기장을 효율적으로 조작할 수 있다. 금속 구조체의 반경이 감소함에 따라 전하 밀도가 증가하여 국부적 영역에서 전기장이 향상된다. 이 논문에서는 금속 구조체의 반경을 최소화하여 국부적으로 전기장을 크게 향상시키기 위해 저항변화메모리에 나노스케일의 금속 구조체를 도입하였다.

   첫 번째로, 팁 강화 (tip-enhanced) 전기장 효과를 달성하기 위해

날카로운 팁을 가지는 피라미드 금속 구조체를 전극으로 사용하였으며, 강화된 전기장이 소자의 저항 변화 거동에 미치는 영향을 조사하였다. 유한요소모델링과 실험결과를 바탕으로, 수십 나노 미터의 팁 반경을 가지는 피라미드 구조체 전극이 팁 부근에서 전기장을 국소적으로 향상시킬 수 있음을 확인하였다. 팁 강화 전기장은 전이 금속 산화물-기반 저항변화메모리에서 열화학 (thermochemical) 반응을 촉진시키고 유기-기반 저항변화메모리에서 전하 주입 (charge injection) 및 수송 (transport) 효율성을 향상시킬 뿐 아니라, 선택적인 위치에서만 전도성 필라멘트 (conductive filament)를 형성시킬 수 있었다. 그 결과 피라미드 구조체 저항변화메모리는 종래의 평판 구조체 저항변화메모리에 비해 안정적인 저항 변화 거동과 향상된 장치 성능을 보여주었다.

저항 변화 층 내의 전기장을 향상시키기 위한 또 다른 접근법으로, 자기조립 (self-assembled)된 블록공중합체 (block copolymer)/금속 복합체 미셀 (micelle)을 이용하여 구형의 나노구조체를 소자의 중간 층으로 도입하였다. 블록공중합체 및 금속전구체를 복합체 미셀로 사용하기 위해 선택적 용매에 용해시켰다. 해당 미셀을 메모리 소자의 상보적 저항 변화 (complementary resistive switch) 층으로 사용하였으며, 상보적 저항 변화 거동의 메커니즘을 조사하였다. 구형의 금속 나노구조체는 전기장을 향상시켜 전기화학적 금속화

(electrochemical metallization)에 기반한 저항 변화 메커니즘을 촉진시킬 수 있었다. 그 결과 상보적 저항 변화 메모리는 사이클 및 셀간 반복 시험 모두에서 4개의 임계 전압으로 안정적인 저항 변화 동작을 나타내었다. 또한 전류-전압 자료 플롯 (plot) 분석과 저항의 온도 계수 결정을 통해 장치의 전도 및 저항 변화 메커니즘을 실험적으로 입증하였다.

전반적으로 본 논문에서는 장치 내 전기장을 증폭시킬 수 있는 금속 나노구조체의 효율적인 엔지니어링을 통해 메모리 장치의 성능과 신뢰성 향상을 추구하였다. 지속적인 관심과 연구를 통해 저항변화메모리의 모든 과제를 극복한 후, 상용화된 저항변화메모리가 가까운 미래에 대중화될 것임을 믿어 의심치 않는다. 우리는 이 결과가 저항변화메모리를 포함한 모든 전자 장치의 획기적인 발전에 기여할 뿐만 아니라 전자 장치 분야의 연구 활동을 촉진하는 데에도 도움이 될 것이라고 믿는다.