Phase Control Modulation for Harmonics Reduction of Dual Inverter Fed Open-End Winding Induction Motor in Light-Load Condition

by

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A dissertation submitted in partial fulfillment

of the requirements for the degree of

DOCTOR OF ENGINEERING

at the

NAGAOKA UNIVERSITY OF TECHNOLOGY

February 2022

Acknowledgements

First and foremost, I would like to express my sincere gratitude to my supervisor, Associate Professor Hitoshi Haga, for providing tremendous levels of support for 7 years. His passion keeps me always moving forward. He has also provided me many rewarding opportunities to participate in national and international conferences.

I also wish to express my grateful to Associate Professor Masataka Minami, who is with Kobe City College of Technology, for taking part in the Ph. D. defense as a co-examiner and for advising in my dissertation. I would also like to express my gratitude and appreciation to Emeritus Professor Seiji Kondo, Professor Kiyoshi Ohishi, Professor Jun-ichi Itoh, Professor Toshimasa Miyazaki, Associate Professor Yuki Yokokura, and Specially Appointed Associate Professor for Academia-Industry Fusion Keisuke Kusaka, who are with the Power Laboratory from Nagaoka University of Technology.

I would also like to express my sincere gratitude for Professor Hiroshi Ohsawa, who is with National Institute of Technology, Kisarazu College, for teaching and supporting me during my research internship. I would also like to extend thanks to Assistant Professor Kodai Abe and Dr. Hiroki Watanabe, who are with Tokyo Metropolitan College of Industrial Technology and Nagaoka University of Technology, respectively, for teaching and supporting me. Further, I warmly thank everybody else in the Power Conversion Laboratory, in particular Mr. Mikiya Ishibashi, Mr. Shota Katayama, Mr. Kodai Okuzono, Mr. Shunsuke Sato, Mr. Shunya Imaizumi, Mr. Kazuyoshi Oguro, and Mr. Pablo Elosegui Garcia for their motivating and helpful discussions as well as for the good times we had in the laboratory.

Finally, I would like to express thanks to my family for their continued support, patience and encouragement. Thank you for helping push me towards this goal.

February 2022
Akihito Mizukoshi

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Chapter 1

Introduction

1.1 Background

According to global electricity estimation by the International Energy Agency, motor drive systems account for 53% of the world's electricity consumption [1-1]. Within the motor drive system region, 68% of power consumption is due to medium-sized motors of 0.75-350kW [1-2]. In particular, the field measurements of operating load on the induction motors (IMs), which were installed in 1992, prior to their removal from service reported in [1-3] that 29% of the IMs operating in the facilities were carrying less than 50% load (see Fig. 1.1). Fig. 1.2 shows the efficiency characteristics of squirrel-cage induction motors (IE1 and IE3) under partial-load. It has been reported that motors with lower rated output have reduced efficiencies at 50% and 25% loads compared to 100% load [1-2]. From Fig. 1.2, it can be confirmed that the motor efficiency is significantly reduced with a load of less than 50%. This makes reduction of the motor losses in the partial-load is effective for an energy-saving.

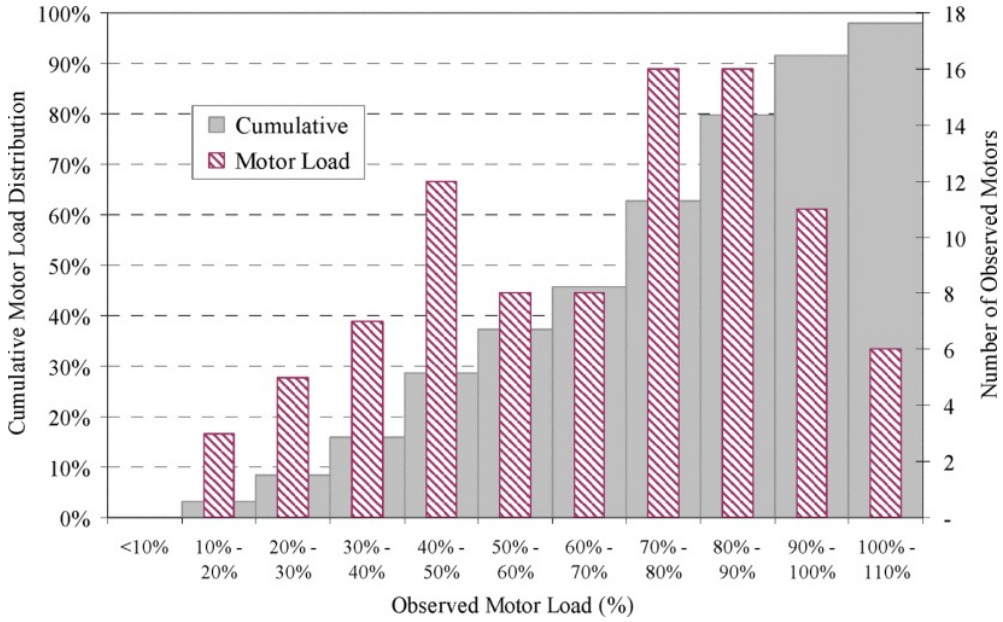

Fig. 1.1. Operating load of induction motors surveyed.
(Adapted from [1-3] in Fig. 3. E. B. Agamloh, "The partial-load efficiency of induction motors," *IEEE Trans. Ind. Appl.*, vol. 45, no. 1, pp. 332–340, 2009.)

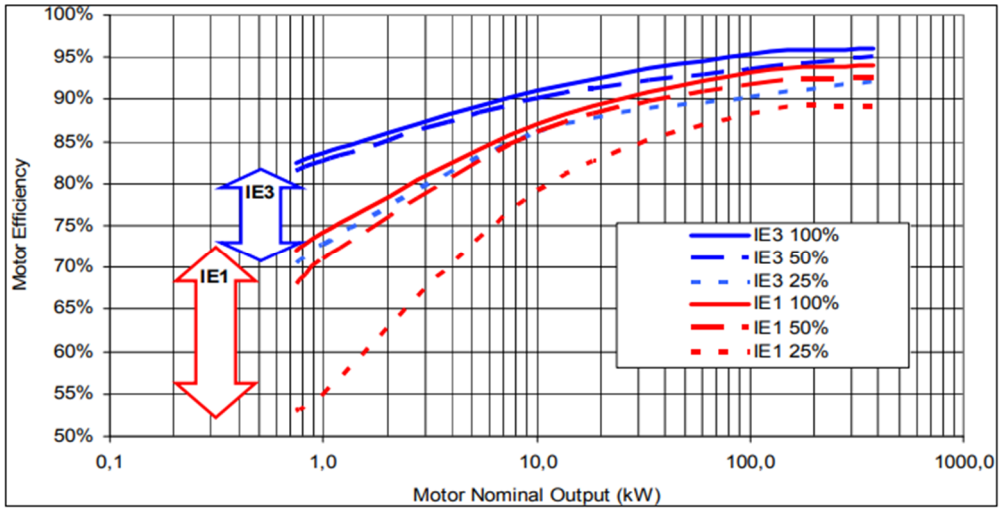

Fig. 1.2. Partial-load efficiency of IE3 and IE1 motors.
(Adapted from [1-2] in Fig. 14. Available: https://www.oecd-ilibrary.org/energy/energy-efficiency-policy-opportunities-for-electric-motor-driven-systems_5kgg52gb9gjd-en)

Interest in energy-saving has been increasing, and in the motor drive system region, variable speed motor drive using semiconductor power converters have been studied for a long time. Especially in recent years, some technologies such as, electric vehicles, flywheel energy storages, wind power generations, etc. [1-4]–[1-6] have been studied due to the situation of activities toward net zero carbon dioxide (CO_2) emissions (Net Zero by 2050 [1-7]). In terms of the semiconductor power converters as the alternating current (AC) motor driver, pulse width modulated (PWM) inverters are used to achieve variable speed drive. In particular, in air conditioner applications, efficiency improvement in the light to middle load range, in which the load is 75% or less, is required as follows [1-8]

$$IPLVc = 0.01 \times COP_{100\%} + 0.47 \times COP_{75\%} + 0.37 \times COP_{50\%} + 0.15 \times COP_{25\%} \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.1)$$

where, $COP_{X\%}$ (Coefficient Of Performance at $X\%$ load) is calculated by dividing the cooling or heating capacity by power consumption, and $IPLVc$ (Integrated Part Load Value, Cooling) means an energy-saving performance index close to the actual usage.

In terms of the AC motor structures, three-phase motors are qualified for most applications. However, for applications such as aircrafts and electric vehicles, the traditional three-phase motors and their motor drivers have issues to improve reliability; thus multi-phase motors and their motor drivers have been investigated for better fault-tolerant capability [1-9], [1-10]. Since variable speed motors are mainly driven by PWM inverters, it is necessary to improve both the inverter and the motor in order to improve the performance of the entire motor drive system. In terms of improving the performance of motors, the characteristics that change depending on the structure of the windings and cores have been analyzed [1-11]–[1-16]. It is known that the electric power losses generated by the motor such as copper loss of the winding, eddy current loss of the core, hysteresis loss, and harmonic loss, etc.

In terms of the PWM inverter, various approaches have been investigated in terms of circuit topologies and modulation strategies. Multi-level inverter topology is one of the effective solutions for improving the efficiency of motor drive systems (e.g., see Fig. 1.3). Since the multi-level inverter outputs a stair-step output voltage, the voltage harmonics decrease compared with using a traditional two-level inverter [1-17]. Another approach to improving the voltage waveform is to reduce the peak value of the PWM voltage by a direct current (DC) to DC converter [1-18] (e.g., see Fig. 1.4). The multi-level waveforms and lower peak value of the voltage can reduce the output harmonics and the motor's harmonic losses. Furthermore, the harmonics generated from the PWM inverter in the variable speed motor system is propagated to other electrical components via the DC-link of the PWM inverter.

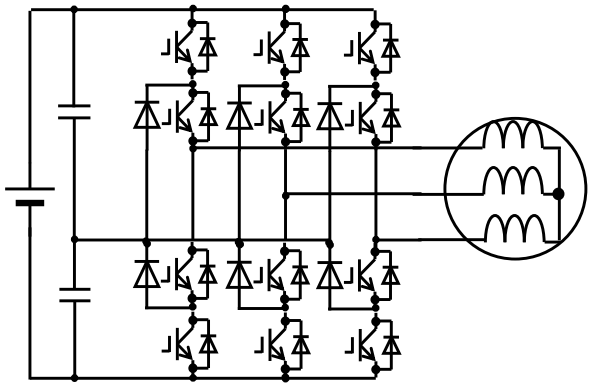

Fig. 1.3. Variable speed motor fed by neutral-point clamped three-level inverter system.

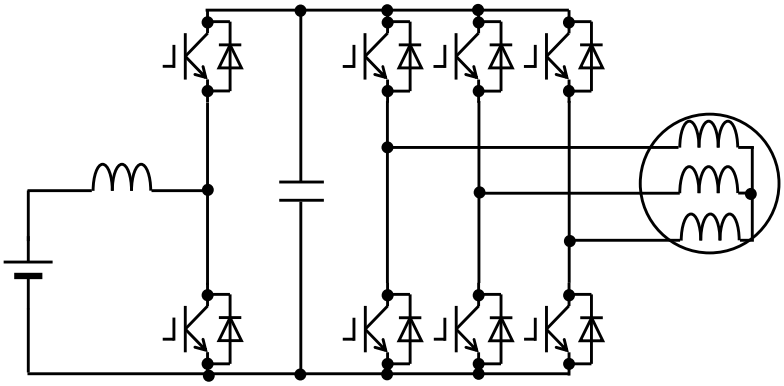

Fig. 1.4. Variable speed motor fed by two-level inverter with boost converter system.

This deteriorates the performance and reliability, and causes other electric components to malfunction [1-19]. In addition, higher harmonic currents flow to the battery, increasing the loss and reducing the life.

In recent years, with the development of semiconductor switching devices, the loss and cost of power converters have been reduced [1-20]. Instead of reducing the number of switching devices, which has been studied so far, studies on improving reliability and performance by adding devices are in progress. A dual inverter topology has been proposed as one of the method for improving the performance of variable speed motor systems [1-23]–[1-26]. The stator windings of a motor are generally star-connected (see Fig. 1.5), but in a dual inverter system, the stator windings are opened and another inverter is connected there (see Fig. 1.6). A circuit topology using the dual inverter has some advantages compared with the single inverter topology such as, expanded speed range [1-25]–[1-27], multi-level operation

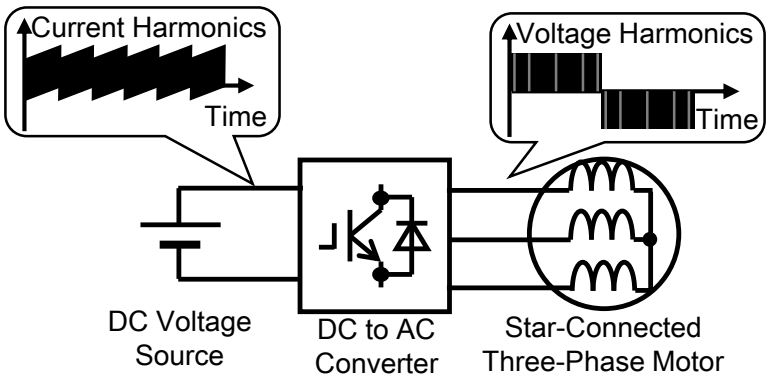

Fig. 1.5. Traditional single inverter topology and its issues.

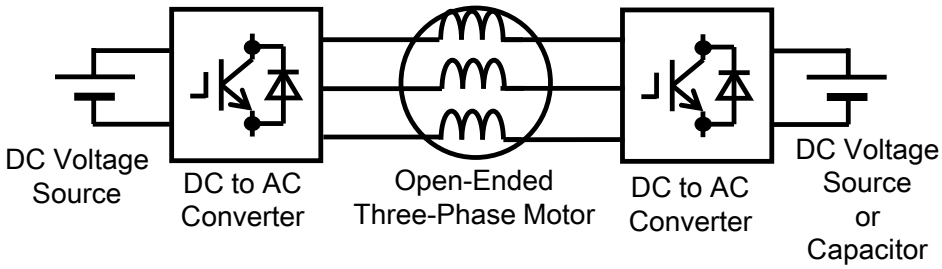

Fig. 1.6. Typical dual inverter topology.

[1-28]–[1-30], and fault tolerant functions [1-31]–[1-33]. In recent years, input current harmonic suppression methods have also been investigated in the dual inverter with floating capacitor (FC) topology, in order to satisfy harmonic regulation or suppress the stress of capacitors; it can be achieved by active and reactive power compensation [1-34], [1-35]. Conventionally, methods of reducing voltage harmonics by making the FC voltage the same as or half of the primary side DC voltage has been studied [1-28]. In contrast, a method of controlling the FC voltage variable, in order to improving the performance, depending on the load condition has been studied [1-36]. However, sufficient studies have not been conducted on the reduction of winding voltage and DC-link current harmonics, in the light-load region.

As an example of commercialization of dual inverters, air conditioners for buildings for high power density have been developed [1-37]. In addition, for electric vehicle applications, it has been reported that a dual inverter system for driving high-voltage motors using next-generation silicon-carbide (SiC) will be commercialized [1-38]. However, in the low load region, higher performance is still required for the traditional single inverter system.

1.2 Research Objectives

The motor structure of multi-phase motors or double winding motors are more complicated than that of a general three-phase motor [1-9]. However, the dual inverter topologies are constructed by opening the traditional star-connected winding. In addition, it is easy to implement hardware by developing semiconductor devices such as modularization of three-phase voltage source inverters (VSIs). In addition, the traditional three-phase multi-level inverter topologies are confronted with severe challenge in terms of fault-tolerant capability and output voltage boosting [1-39]. Therefore, research on improving the performance of dual inverters was conducted for the following objectives.

The research objective in this thesis is to reduce the input and output harmonics in the light-load region of the dual inverter fed open-end winding

IM system. In this research, the DC-link voltage of the secondary inverter is changed according to the power factor angle and output voltage of the motor, and the voltage difference between the two inverters is applied to the motor to reduce the voltage harmonics applied to the windings. Furthermore, harmonic analysis of the output voltage in the motor winding and input current in the DC-link of the primary inverter is carried out.

First of all, a modulation strategy for reducing the output voltage waveform at low motor torque, in the case of the dual inverter with variable DC-link voltage in the secondary side VSI, is studied. The original point of this method is that, in order to reduce the peak PWM value at low motor torque, the dual inverter outputs the voltage difference with small phase angle difference between the two inverters.

Second, a control strategy for improving the output voltage total harmonic distortion (THD) in the light-load condition with the FC topology is studied. The waveform improvement leads to increase the motor efficiency; thus, the total efficiency including inverter efficiency increases, and is experimentally obtained to clarify the effectiveness of the proposed method. Furthermore, an operating condition, that allows to reduce the THD of the phase voltage of motor winding, when the open-end winding IM driven by the dual inverter with sinusoidal PWM (SPWM) is theoretically described. Then, based on the previous analysis, output voltage harmonics when using various PWM methods such as, third-harmonic-injection PWM (THIPWM), and discontinuous-PWM (DPWM), space-vector-modulation (SVPWM), and near-state PWM (NSPWM) [1-40] with a reduced number of commutations, are theoretically analyzed. Originality of this study is to analyze the output voltage harmonics that change not only with the fundamental voltage but also with the power factor angle when typical PWM methods are applied to the dual inverter. Through analysis, the modulation method that minimizes the harmonic components depending on the operating conditions of open-end winding IM is clarified.

Finally, a control method to reduce the high-order harmonics caused by PWM in the DC-link current in a dual inverter with a FC topology, which has the same voltage ratings in two inverters, is studied. The proposed control method reduces the high-order harmonic current through a six-step operation at the primary inverter. The secondary inverter supplies a sinusoidal voltage to the motor using a low-rated voltage. The validity of the proposed control method is confirmed through an experiment using an open-end winding induction motor. Furthermore, the FC voltage dependencies of the input current harmonics are analyzed.

1.3 Thesis Organization

Fig. 1.7 shows the outline of this thesis divided into 6 chapters.

Chapter 1 introduces the typical configuration of the variable speed motor drive systems and the effects of input/output harmonics generated by DC to AC conversion. In addition, the objectives of reducing input/output harmonics in the partial load region are discussed.

Chapter 2 introduces the evaluation method of output voltage harmonics and input current harmonics in the dual inverter topology that realizes high performance of the motor drive system. In addition, conventional dual inverter drive methods that reduce input/output harmonics and their issues are discussed. Finally, proposed modulation strategies to reduce the input/output harmonics of the dual inverter topology using the motor power factor angle, which is the key concept of this thesis, are described and a beneficial position of the proposed strategies along with conventional methods is presented.

Chapter 3 discusses a control strategy for reducing voltage harmonics of an induction motor in a low-torque condition. The motor drive system consists of an open-end winding IM and two VSIs; the dual inverter has a DC voltage source and an FC. In proposed method, the use of the output voltage difference between the inverters constituting the dual inverter lowers

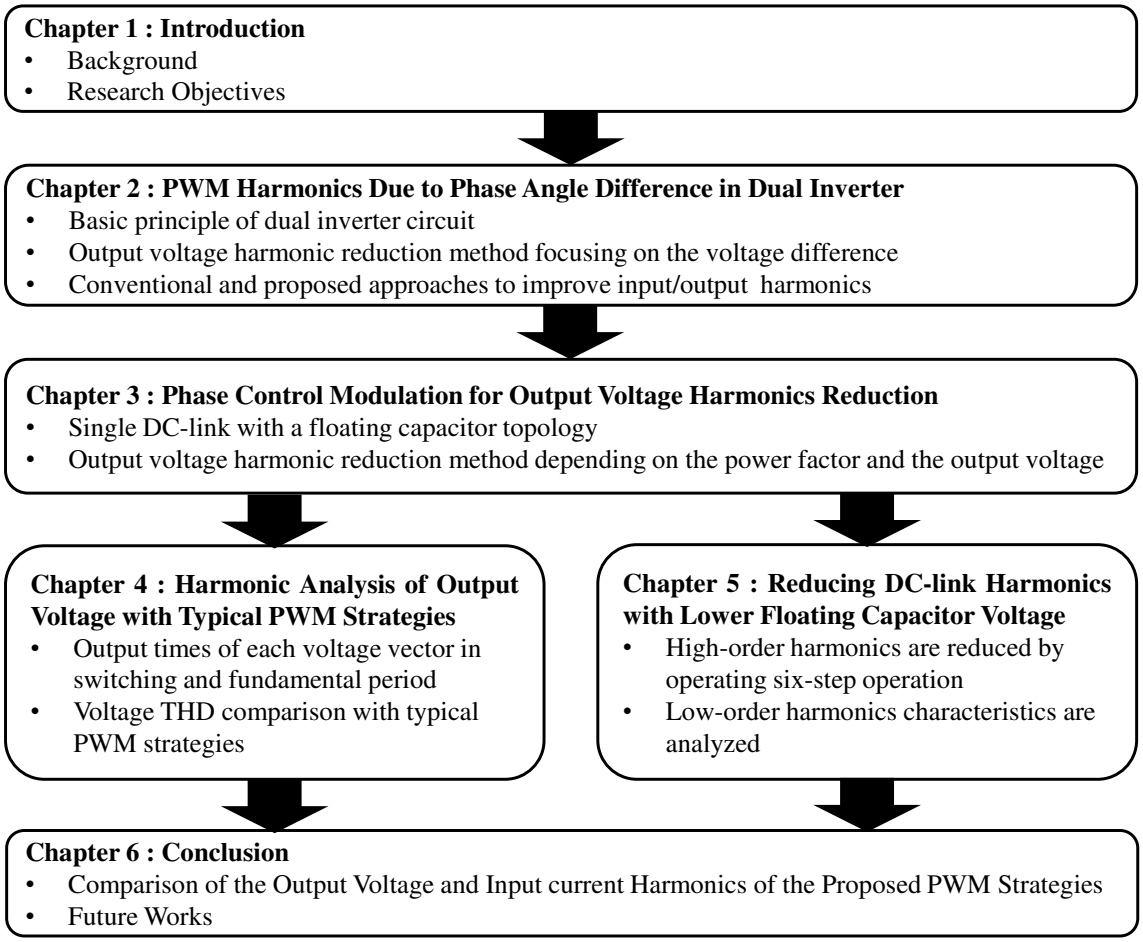

Fig. 1.7. Outline of this thesis.

the harmonics by keeping the modulation index high owing to the phase angle difference variation between the two inverters. The performance of harmonics reduction is theoretically analyzed and experimentally verified.

Chapter 4 discusses an analysis strategy for the output voltage harmonics, which depend on the fundamental voltage, power factor angle, and PWM strategies. Herein, SPWM, THIPWM, and DPWM are used as the conventional carrier-based modulation techniques, and SVPWM and NSPWM with reduced number of commutations are used as the proposed modulation methods. The validity of the theoretical analysis is then confirmed by experiments using an open-end winding IM.

Chapter 5 discusses a control method to reduce the high-order harmonics caused by PWM in the DC-link current in a dual inverter with the FC topology, which has the same voltage ratings in two inverters. The proposed control method reduces the high-order harmonic current through a six-step operation at the primary inverter. The secondary inverter supplies a sinusoidal voltage to the motor using a low-rated voltage. The validity of the proposed control method is confirmed through an experiment using an open-end winding induction motor. Furthermore, the FC voltage dependencies of the input current harmonics are analyzed.

Chapter 6 provides the conclusion of this thesis. In this chapter, the advantages and drawbacks of the proposed PWM strategies are classified clearly and compared alongside each other. Finally, future works necessary to improve the performance of dual inverters and popularize them in industry are described.

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Chapter 2

PWM Harmonics Due to Phase Angle Difference and Voltage Ratio in Dual Inverter

2.1 Introduction

In the previous chapter, research trends of motor drive systems and the need to improve the performance of light-load conditions were described. In addition, a dual inverter topology was described as a method for improving the performance of motor drive systems, and the need to reduce harmonics was shown.

This chapter describes research trends in dual inverter topologies and a generalized theory of input/output harmonics, which depends on the phase angle difference between two inverters. In addition, a voltage harmonic reduction method applied to the light-load conditions is proposed as opposed to the conventional dual inverter control and modulation method. Finally, the beneficial position of the proposed approaches along with other conventional approaches is presented to show the contribution of this research.

2.2 Basis of Dual Inverter Topology

2.2.1 Circuit Configuration of the Dual Inverter Topology

A system configuration of the dual inverter fed open-end winding motor is shown in Fig. 2.1. The system consists of an open-end winding motor and two voltage source inverters (VSIs), which are connected to the opposite terminals of stator windings. In a dual inverter system using VSI, two inverters and a motor are connected in cascade, thus the per-phase equivalent circuit is shown as Fig. 2.2. In contrast to a single inverter system in which the AC voltage of one inverter is directly applied to the motor, in a dual inverter system, the combined voltage of the two inverters is applied to the motor, thus the amplitude and phase of the voltage output by each inverter, which

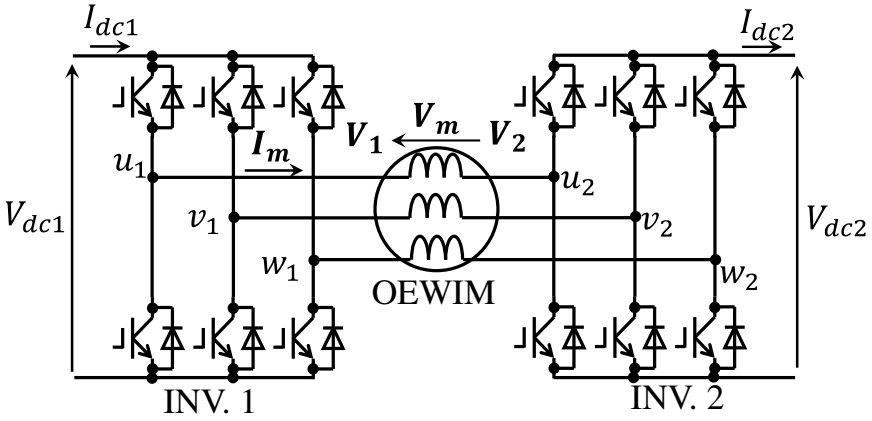


Fig. 2.1. Circuit configuration of the dual inverter fed open-end winding induction motor (OEWIM).

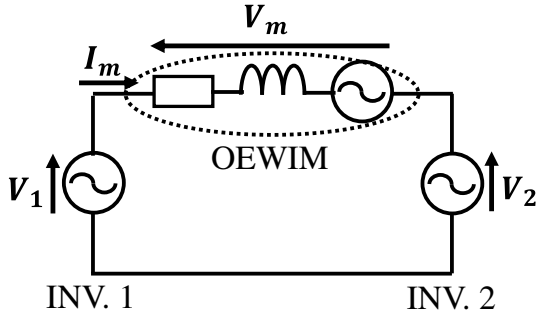


Fig. 2.2. Equivalent circuit of the dual inverter fed open-end winding induction motor (OEWIM).

increases the degree of freedom [2-1]–[2-3].

The output voltage difference between INV. 1 and INV. 2 is supplied to the stator windings in the dual inverter; thus, the winding voltage vector $\boldsymbol{V_m}$ is expressed as follows:

$$\boldsymbol{V_m} = \boldsymbol{V_1} - \boldsymbol{V_2} \quad \cdots\cdots (2.1)$$

$$|\boldsymbol{V_1}| = \frac{M_1}{2} V_{dc1} \quad \cdots\cdots (2.2)$$

$$|\boldsymbol{V_2}| = \frac{M_2}{2} V_{dc2} \quad \cdots\cdots (2.3)$$

Here, $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$ indicate the output voltage vectors of INV. 1 and INV. 2. As shown in (2.1), since the voltage of the difference between the two inverters is applied to the motor, each inverter outputs an arbitrary voltage under the condition that the combined voltage of the dual inverters follows the reference value. For example, the inverter combinations shown in Fig. 2.3 have been considered [2-4].

In particular, a dual cascaded inverter structure is adopted to connect the two considered energy sources to an open-end winding IM. This solution allows the achievement of a complete separation between the capacitor dc

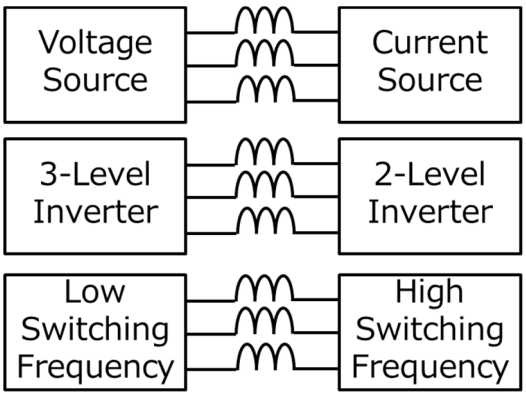


Fig. 2.3. Dual inverter configuration examples [2-4].

voltage and the floating capacitor (FC) voltage, which has following advantages [2-5].

1) Due to the low operating voltage of capacitors, it is not necessary to use high-ratio DC/DC converters between the capacitor bank and the rest of the drive because, in the cascaded configuration, the FC voltages are not connected in parallel on a common DC-link.

2) Since the capacitor bank is directly connected to the motor by means of an independent power conversion system, its output voltage can be instantaneously added to the FC inverter output voltage by means of proper modulation. Thus, this configuration allows the achievement of faster compensation of the FC voltage drop during power transients than a traditional configuration (single VSI fed by the two energy sources).

3) The cascaded configuration is equivalent to a multi-level inverter; several optimizations on the modulation strategies can be adopted to optimize the quality of the output waveforms without increasing the power losses. For instance, two different modulation frequencies could be used on the two VSIs to improve the overall efficiency of the power converter, without decreasing the quality of output waveforms. A separate and variable frequency modulation for each VSI of the cascaded configuration is proposed; It allows increasing the efficiency of the power conversion by adopting high switching frequencies for the low-voltage VSI and lower switching frequencies for the high-voltage VSI [2-4], [2-6]. Thus, a reduction in power losses is achieved without increasing the output current total harmonic distortion (THD), or alternatively, THD can be improved without increasing power losses.

4) VSI switches can work with a lower operating voltage.

5) Short acceleration and deceleration of the rotor, such as when driving in the traffic jam, can be directly managed by the capacitor bank, without involving the FC stack.

6) It will be possible to apply short overvoltage to the motor during the transient to increase dynamic performances.

7) VSI redundancy for security purposes: The motor can be fed by just

one side of the cascaded converter. For instance, if a fault on the FC inverter occurs, it is possible to keep the motor fed by the capacitor bank for an additional time period. These features can be very useful to guarantee auxiliary propulsion for an emergency parking on the hard shoulder or to activate stability control during emergency breaking if the FC VSI fault occurs during vehicle run.

2.2.2 DC-Link Configuration of the Dual Inverter Topology

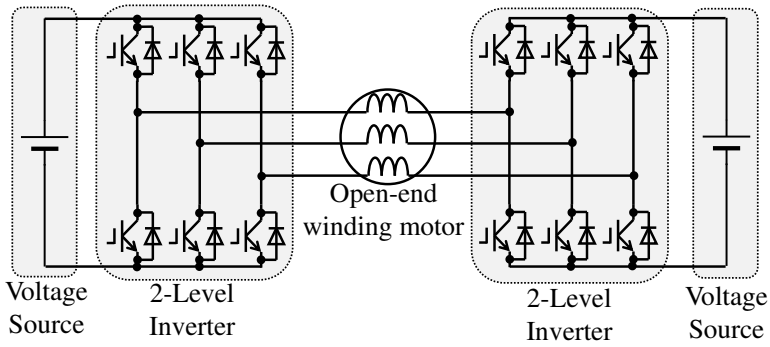
The difference in the power supply circuit system in the dual inverter topology will be described. As shown in Fig. 2.4, there are three different arrangements for DC-link power sources in a dual inverter. They can be either two isolated DC-links (2DC), a common DC-link (CDC), or a DC-link with an FC [2-5]. It can be seen from Fig. 2.4(a) only the dual inverter with 2DC needs a transformer or battery to achieve isolation [2-6]–[2-8]. It will increase the volume and weight of system significantly, which are not desired in such as electric aircraft applications.

The dual inverter with 2DC uses two isolated DC-links, thus the voltage utilization of the dual inverter with 2DC could be less than one [2-3]–[2-5], which means that the maximum output voltage of 2DC equals to the sum of the two DC-links voltages. The output levels of dual inverter with 2DC/FC can be more than three [2-2]–[2-4], [2-9]–[2-12], which is obviously an appealing feature. A higher number of output levels are conceivable for asymmetric supplies ($V_{dc1} \neq V_{dc2}$), and this will be presented in Section 2.3.

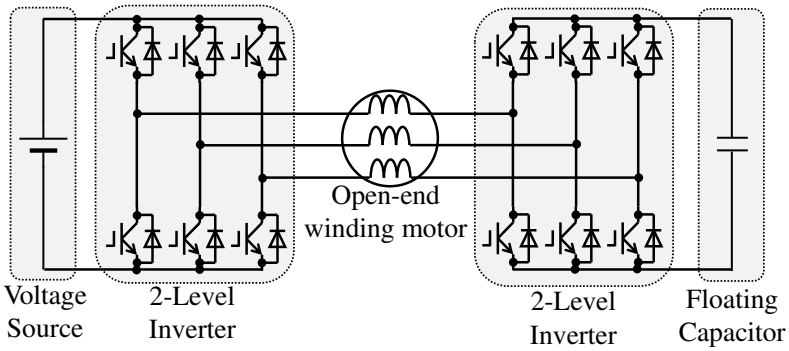
The dual inverter with CDC, which has a common DC-link in both inverters (see Fig. 2.4(b)), has the highest degree of fault tolerance and the double voltage utilization; this is because each phase winding has the same configuration as a full bridge inverter [2-13]–[2-15]. However, the zero-sequence current (ZSC) exists in this configuration. The ZSC is determined by the differential common-mode voltage (CMV) [2-16], [2-17], which is identical to the voltage difference between the neutral points of the voltage supplies on the two inverters. To suppress differential CMV, the dual inverter

with CDC may degrade from multilevel to two-level operation [2-15]. In addition, the DC-link voltage utilization may also be affected; the reason is that the phase difference between the two inverters cannot be reversed. On the other hand, since there is no zero-sequence current path in the dual inverter with 2DC/FC, ZCS is completely eliminated [2-5].

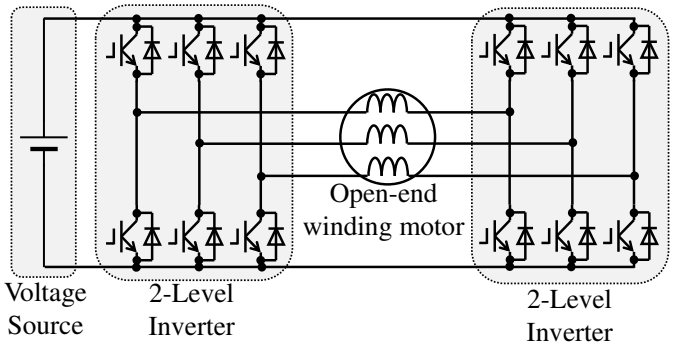
The dual inverter with FC, which has an FC in the secondary inverter,



(a) Two isolated DC-links topology (2DC).



(b) DC-link with a floating capacitor topology (FC).



(c) Common DC-link topology (CDC).

Fig. 2.4. Three configurations of dual inverter topology.

has the advantages of the other two configurations in terms of multilevel output voltage and voltage boosting capability due to avoiding ZSC circulation, and no need for isolation circuit because one inverter is floating. In particular, an attractive feature brought by FC is that its voltage utilization can be more than one thanks to the existence of the FC [2-18]–[2-21].

2.2.3 Input and Output Waveforms Due to Phase Angle Difference Between Two Inverters

As mentioned in Section 2.2.1, the equivalent circuit of the dual inverter supplies voltage to motor windings as voltage-source (see Fig. 2.2). Since the fundamental components of voltage vectors ($\boldsymbol{V_m}, \boldsymbol{V_1}, \boldsymbol{V_2}$) form a triangle, the relationship between the amplitudes of each vector is expressed as follows:

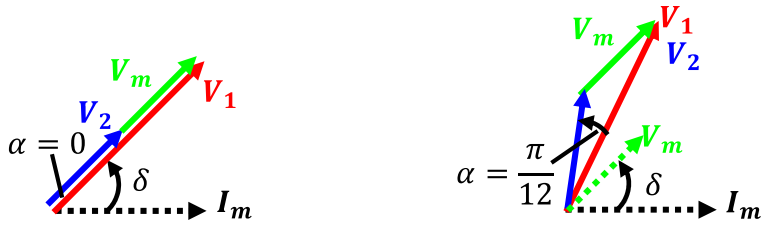
$$|\boldsymbol{V_m}|^2 = |\boldsymbol{V_1}|^2 + |\boldsymbol{V_2}|^2 - 2|\boldsymbol{V_1}||\boldsymbol{V_2}|\cos\alpha \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (2.4)$$

Here, α denotes the phase angle difference between voltage vectors of INV. 1 and INV. 2, which is a key element of this study. From (2.4), each inverter voltage ($\boldsymbol{V_1}$ and $\boldsymbol{V_2}$) required to realize an arbitrary output voltage $\boldsymbol{V_m}$ has a degree of freedom.

Fig. 2.5 and Fig. 2.6 show examples of the voltage vector diagram and the simulated waveforms of U-phase voltage references ($v_{u1-ref}, v_{u2-ref}, v_{um-ref}$), each phase currents ($i_{um}, i_{vm}, i_{wm}$), output U-phase voltage (v_{um}), and input DC-link current of INV. 1 (i_{dc1}). When $\alpha = 0$, the maximum value of the output voltage level is $2(V_{dc1} - V_{dc2})/3$, and the ripple of the input current is small (see Fig. 2.6(a)). In contrast, when $\alpha = \pi/12$, the number of output voltage levels increases and the negative side of the input current is relatively large (see Fig. 2.6(b)).

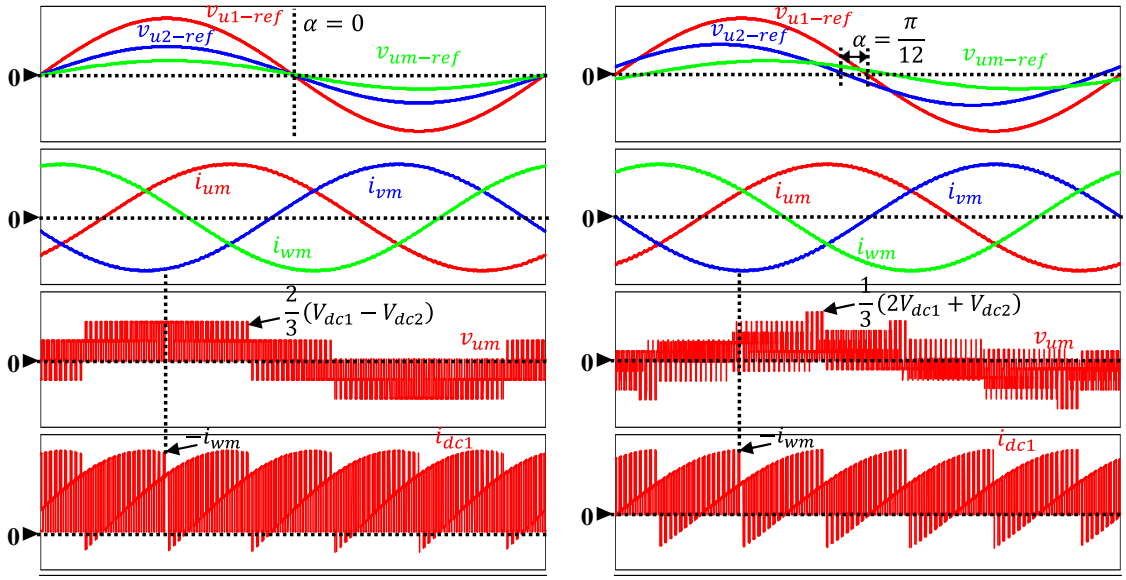
In the case of 2DC topology, a method for reducing output voltage harmonics by assigning the phase angle difference α to zero and maximizing the modulation indices of both inverters (M_1, M_2) has been reported [2-22],

[2-23]. However, from the features explained in the previous section, this thesis deals with input/output harmonic reduction in the FC topology.



(a) (b)

Fig. 2.5. Vector diagram of the dual inverter when (a) $\alpha = 0\text{deg}$ and (b) $\alpha = 15\text{deg}$.



(a) (b)

Fig. 2.6. Simulated waveforms of the dual inverter when (a) $\alpha = 0\text{deg}$ and (b) $\alpha = 15\text{deg}$.

2.2.4 Vector Relationship Between Dual Inverter and Motor Voltages and Current with Floating Capacitor Topology

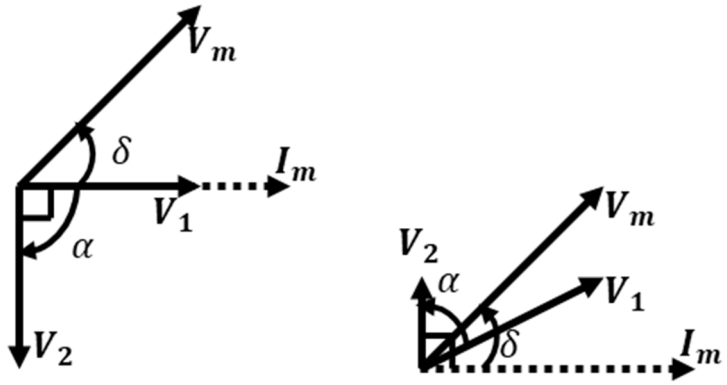
Fig. 2.7 shows the vector diagrams of the dual inverter with FC topology. Here, δ denotes the motor power factor angle. Because INV. 2 has no power supply, $\boldsymbol{V_2}$ leads or lags from the motor phase current $\boldsymbol{I_m}$ by $\pi/2$ radians at the steady state. One of the method for expanding the output range, the relation shown in Fig. 2.7(a) is used. In this method, INV. 1 can output the maximum active power by matching the phase angle of $\boldsymbol{V_1}$ and $\boldsymbol{I_m}$ [2-19], [2-24]. From the voltage vector relation, a ratio of amplitudes of $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$ at the steady state is expressed using α and δ as follows:

$$\frac{|\boldsymbol{V_2}|}{|\boldsymbol{V_1}|} = \frac{\cos(\alpha+\delta)}{\cos\delta} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2.5)$$

Due to equation (2.2) and (2.3), the ratio of INV. 2 DC voltage to INV. 1 DC voltage $G_{dc} = V_{dc2}/V_{dc1}$ is given by:

$$G_{dc} = \frac{V_{dc2}}{V_{dc1}} = \frac{M_1}{M_2}\frac{\cos(\alpha+\delta)}{\cos\delta} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2.6)$$

Since the number of switching devices increases in a dual inverter, it is desirable to reduce the V_{dc2} as much as possible from the viewpoint of switching loss; thus M_2 has to be high value which is indicated (2.6). Fig. 2.8 shows DC voltage ratio V_{dc2}/V_{dc1} characteristic with different power factor angle δ and phase angle difference α. Here, modulation indices of each inverter are assigned $M_1 = M_2$. The characteristic indicates that the FC voltage can be controlled by phase angle difference even if power factor angle changes.



(a) (b)

Fig. 2.7. Vector diagram of the dual-inverter with a floating capacitor when (a) INV. 1 leads INV. 2 and (b) INV. 1 lags INV. 2.

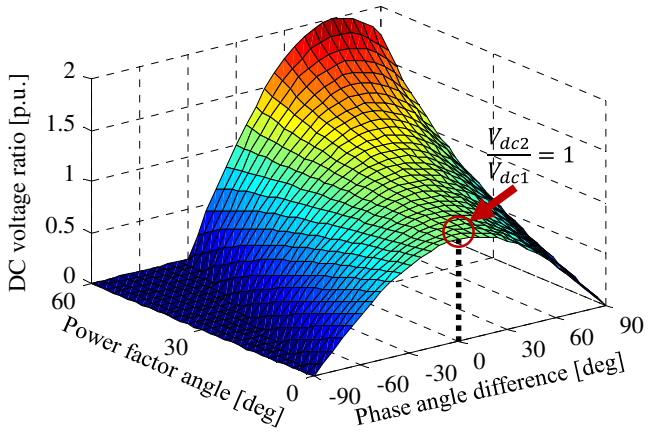


Fig. 2.8. DC voltage ratio V_{dc2}/V_{dc1} characteristic with different power factor angle δ and phase angle difference α in the case of $M_1 = M_2$

2.3 Generalization Theory of Input Current and Output Voltage Harmonics

2.3.1 Vector Identification and Voltage Levels in Dual Inverter

Three-phase voltage inverters that drive variable speed motors have long been studied, and various modulation methods have been proposed in traditional two-level single-inverter topologies. In addition, modulation methods and analysis methods have been proposed to reduce the output voltage harmonics on the AC side of the inverter and the input current harmonics on the DC side [2-24]–[2-30].

There are three levels of a PWM waveform in each phase of motor winding if the dual inverter uses two-level VSI, and those values are $\pm 2/3$, $\pm 1/3$, and 0 multiplied by DC-link voltage. Therefore, the number of levels of the output voltage in the dual inverter increases compared with the single inverter system. Space vectors on the individual 2-level VSIs are shown in Fig. 2.9(a). In this thesis, the switching states of INV.1 and INV.2 are respectively numbered as 0, 1, 2, ..., 7 and 0', 1', 2', ..., 7'. Here, a "+" means that the upper arm switch is in conduction, while a "-" means that the lower arm switch is in conduction. Hence, the dual inverter has 8×8=64 applicable switching states; the combined voltage space vectors in the dual inverter is shown in Fig. 2.9(b). The voltage vectors 1 to 6 and $1'$ to $6'$ are active vectors having the magnitude of $2/3V_{dc1}$ and $2/3V_{dc2}$, while vectors 0, 7, $0'$, and $7'$ are zero vectors having the magnitude of 0.

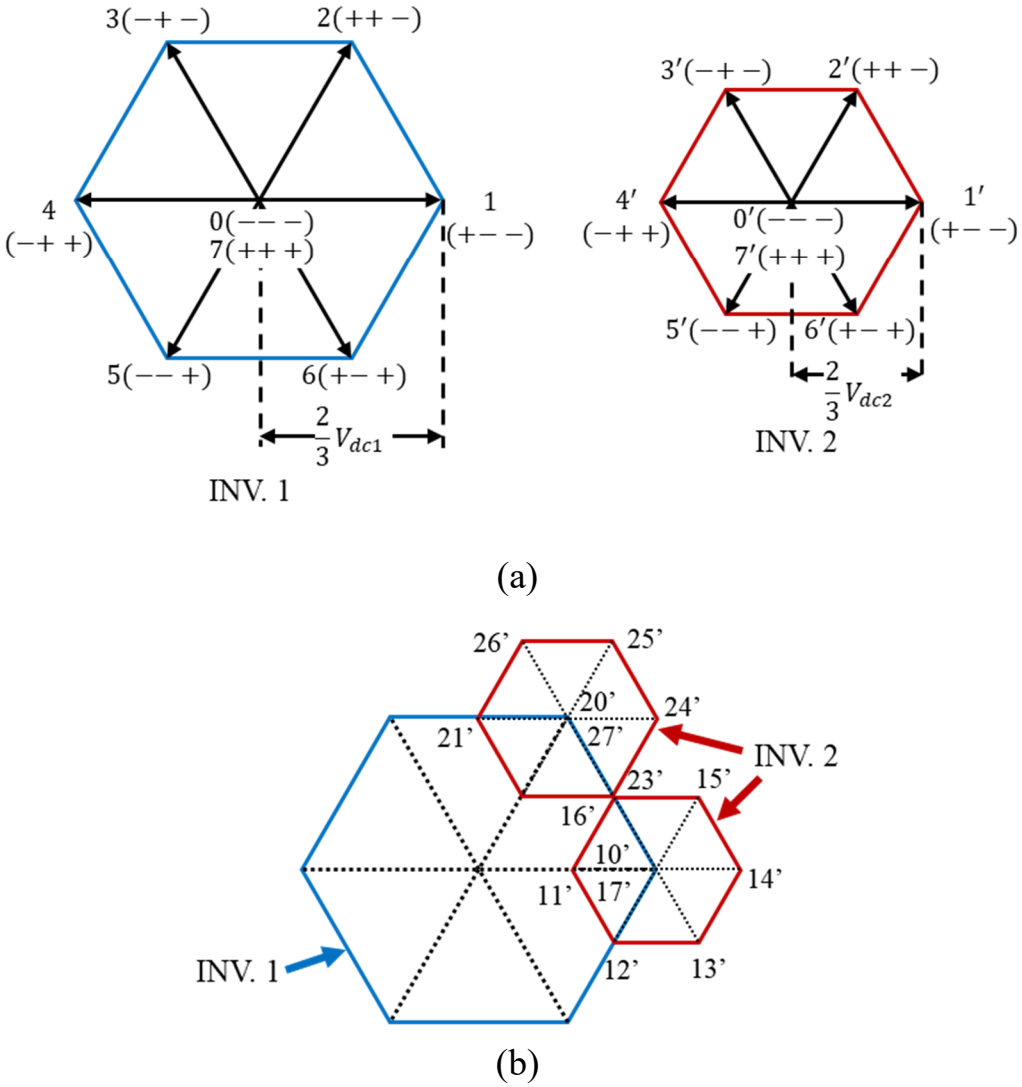


Fig. 2.9. (a) Individual space vectors and (b) combined space vectors.

The voltage vector of each inverter, their voltage value, and the examples of the combination of the winding voltage are shown in

Table 2.. Since V_{dc1} and V_{dc2} are related to the magnitude of the voltage vectors, in other words, the height of the PWM voltage, the voltage harmonics generated by the PWM can be reduced by appropriately controlling the value of V_{dc2}. By outputting the vectors of the same number (e.g. $V_{11'}$ and $V_{22'}$) in both inverters, it is possible to output the voltage level proportional to the DC voltage difference. It has been confirmed that carrier harmonics can be reduced by selecting these vectors.

The resulting vectors in the dual inverter V_{xy} are given by the difference between each vectors of INV. 1 and INV. 2 as follows:

$$V_{xy} = \begin{cases} \frac{2}{3}V_{dc1}\left(e^{j\frac{\pi}{3}(x-1)} - G_{dc}e^{j\frac{\pi}{3}(y-1)}\right), \\ (if\ \ x = 1\ \ to\ \ 6\ \ and\ \ y = 1\ \ to\ \ 6), \\ \frac{2}{3}V_{dc1}e^{j\frac{\pi}{3}(x-1)}, \\ (if\ \ x = 1\ \ to\ \ 6\ \ and\ \ y = 0{,}7), \\ \frac{2}{3}V_{dc1}G_{dc}e^{j\frac{\pi}{3}(y-1)}, \\ (if\ \ x = 0{,}7\ \ and\ \ y = 1\ \ to\ \ 6) \end{cases} \quad \text{.....} \quad (2.7)$$

where subscripts x and y denote the vector number. From (2.7), the resulting space vector diagram, as shown in Fig. 2.10, can be drawn as the hexagon by INV. 2 around vectors on the hexagon by INV. 1. The magnitudes of the resulting vector changes depending on the voltage ratio $G_{dc} = V_{dc2}{:}V_{dc1}$.

Table 2.1 Combination of the winding voltage.

Each INV. vectors	Each INV. voltages	Resulting vectors	Winding voltages
$\boldsymbol{V_0, V_7, V_{0'}, V_{7'}}$	0	$\boldsymbol{V_{00'}, V_{77'}}$	0
$\boldsymbol{V_1, V_{1'}}$	$\frac{2}{3}V_{dc1}, \frac{2}{3}V_{dc2}$	$\boldsymbol{V_{01'}}$	$-\frac{2}{3}V_{dc2}$
$\boldsymbol{V_2, V_6, V_{2'}, V_{6'}}$	$\frac{1}{3}V_{dc1}, \frac{1}{3}V_{dc2}$	$\boldsymbol{V_{11'}}$	$\frac{2}{3}(V_{dc1} - V_{dc2})$
$\boldsymbol{V_4, V_{4'}}$	$-\frac{2}{3}V_{dc1}, -\frac{2}{3}V_{dc2}$	$\boldsymbol{V_{21'}}$	$\frac{1}{3}(V_{dc1} - 2V_{dc2})$
$\boldsymbol{V_3, V_5, V_{3'}, V_{5'}}$	$-\frac{1}{3}V_{dc1}, -\frac{1}{3}V_{dc2}$	$\boldsymbol{V_{22'}}$	$\frac{1}{3}(V_{dc1} - V_{dc2})$
		$\boldsymbol{V_{27'}}$	$\frac{1}{3}V_{dc1}$
		$\boldsymbol{V_{72'}}$	$-\frac{1}{3}V_{dc2}$

For instance, the resulting vector diagrams for $G_{dc} = 2:3$ and $G_{dc} = 1:3$ are shown in Fig. 2.10(a) and (b), respectively. In this thesis, voltage vectors are categorized into seven types according to their magnitude as follows:

$$V_A = \frac{2}{3} V_{dc1}(1 - G_{dc}) \quad \text{(2.8a)}$$

$$V_B = \frac{2}{3} V_{dc1} G_{dc} \quad \text{(2.8b)}$$

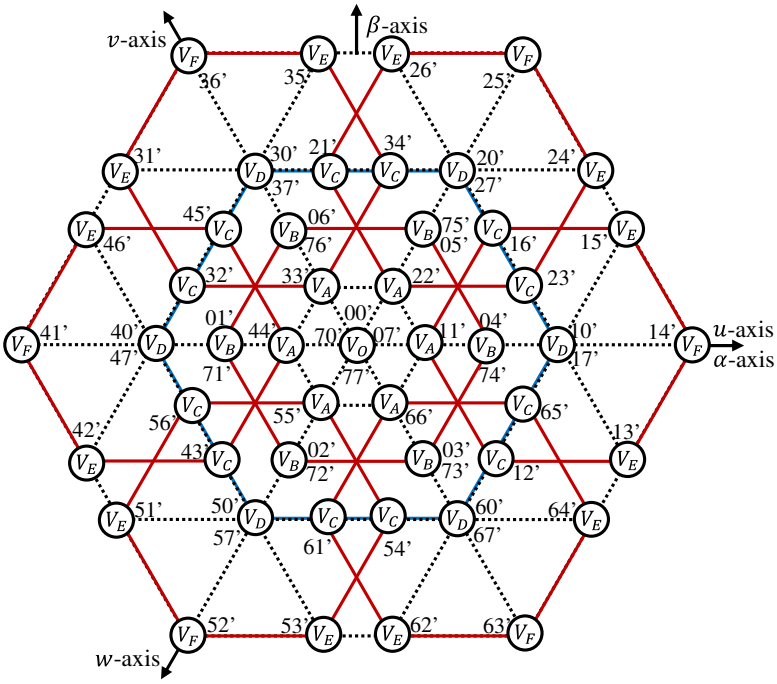
$$V_C = \frac{2}{3} V_{dc1} \sqrt{1 - G_{dc} + G_{dc}^2} \quad \text{(2.8c)}$$

$$V_D = \frac{2}{3} V_{dc1} \quad \text{(2.8d)}$$

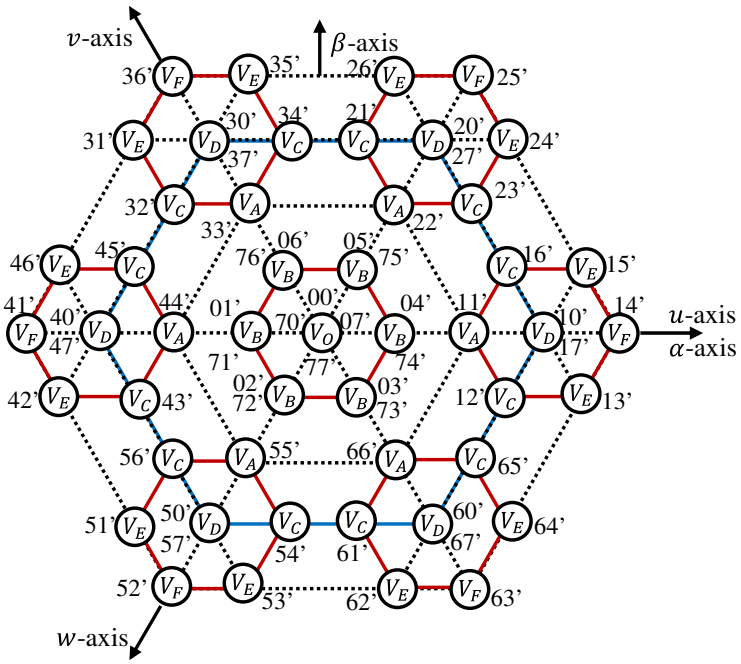
$$V_E = \frac{2}{3} V_{dc1} \sqrt{1 + G_{dc} + G_{dc}^2} \quad \text{(2.8e)}$$

$$V_F = \frac{2}{3} V_{dc1}(1 + G_{dc}) \quad \text{(2.8f)}$$

$$V_O = 0 \quad \text{(2.8g)}$$



(a)



(b)

Fig. 2.10. Combined voltage space vectors with different DC-link voltage ratios (a) $G_{dc} = 2:3$ and (b) $G_{dc} = 1:3$.

2.3.2 Output Voltage Harmonics Evaluation

When using carrier-based PWM, the output time T_{xy} of each vector, which normalized by a switching period T_s, is determined by the relation between voltage references of INV. 1, and INV. 2 as:

$$\begin{cases} v_{u1-ref} = M_1 \cos(\theta) \\ v_{v1-ref} = M_1 \cos\left(\theta - \frac{2}{3}\pi\right) \\ v_{w1-ref} = M_1 \cos\left(\theta + \frac{2}{3}\pi\right) \end{cases} \quad \begin{cases} v_{u2-ref} = M_2 \cos(\theta + \alpha) \\ v_{v2-ref} = M_2 \cos\left(\theta - \frac{2}{3}\pi + \alpha\right) \\ v_{w2-ref} = M_2 \cos\left(\theta + \frac{2}{3}\pi + \alpha\right) \end{cases} \quad \cdots\cdots\cdots\cdots \quad (2.9)$$

Here, $\theta = \omega t$ denotes the fundamental angular frequency, and INV. 2 voltage leads INV. 1 voltage by phase angle difference α. Fig. 2.11 shows the resulting vectors in a switching period T_s when $M_1 < M_2$, as an example. Voltage references are calculated by substituting M_1 or M_2 for M, and θ_1 or θ_2 for θ in equations (2.9), in which the electrical angle of INV. 1 and INV. 2 (θ_1 and θ_2) are given by $\theta - \delta - \alpha + \pi/2$, and $\theta_1 - \alpha$ respectively. Note that there are 64 switching states, $T_{xy}(\theta)$ are described below as examples:

$$\frac{T_{11}(\theta)}{T_s} = \min(v_{u1}, v_{u2}) - \max(v_{v1}, v_{w1}, v_{v2}, v_{w2}) \quad \cdots\cdots\cdots \quad (2.10)$$

$$\frac{T_{12}(\theta)}{T_s} = \min(v_{u1}, v_{u2}, v_{v2}) - \max(v_{v1}, v_{w1}, v_{w2}) \quad \cdots\cdots\cdots \quad (2.11)$$

As shown in Fig. 2.11, the output voltage vector is determined by the combination of the voltage vectors of the two inverters in the dual inverter topology.

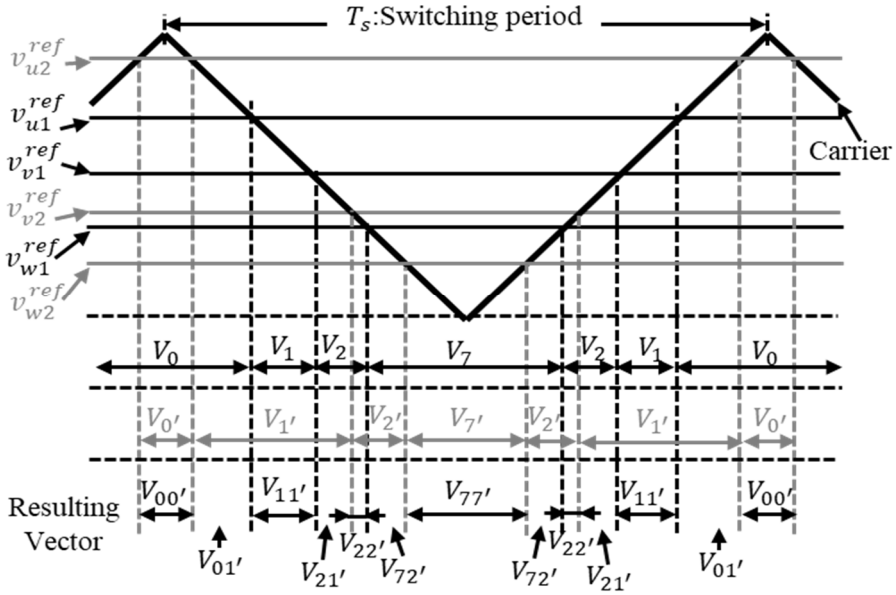


Fig. 2.11. Resulting vectors in a switching period T_s

The voltage applied to the load is calculated from those output time, and the generated harmonics are evaluated using root-mean-squared (RMS) value. Output voltage RMS in a fundamental period V_{RMS} is calculated by the sum of all combinations of the product of V_{xy}^2 and $T_{xy}(\theta)$ as follows:

$$V_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\sum_{x=0}^{7}\sum_{y=0}^{7} V_{xy}^2 T_{xy}(\theta)\right)d\theta} \quad \cdots\cdots\cdots\cdots \quad (2.12)$$

When the difference between V_{RMS} and the fundamental voltage V_{fun} is large, it means that more harmonics are superimposed. In this study, the voltage harmonics are evaluated based on the total-harmonic-distortion (THD) as follows:

$$THD = \frac{\sqrt{V_{RMS}^2 - V_{fun}^2}}{V_{fun}} \quad \cdots\cdots\cdots\cdots \quad (2.13)$$

2.3.3 Input Current Harmonics Evaluation

In recent years, research has been conducted on extending the life of batteries and electrolytic capacitors by reducing the input current harmonics on the DC side, which are mainly related to the shortening of the life of motor drive systems [2-31]–[2-34]. In these studies, the phase difference between the voltage and current of the motor (motor power factor angle) is focused on, and by changing the switching pattern according to the power factor angle, the input current harmonics on the DC side over a wide power factor range. It has been reported that the switching frequency component can be reduced.

Table 2. lists the instantaneous values of the DC-link current with regard to the voltage space vector. The DC-link current is the superposition summation of the switched current pulses from each leg and is calculated as:

$$i_{dc1}(\theta) = i_{um}s_{u1} + i_{vm}s_{v1} + i_{wm}s_{w1} \quad \cdots\cdots (2.14)$$

(2.14) indicates that the DC-link current is dependent on not only the switching patterns (s_{u1}, s_{v1}, s_{w1}) but also the motor current conditions (i_{um}, i_{vm}, i_{wm}). The RMS value of the DC-link current $I_{dc1-RMS}$ and normalized DC-link current harmonics I_{dc1-h} can be calculated in the similar way as voltage harmonics shown in (2.12) and (2.13) as:

$$I_{dc1-RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{dc1}^2(\theta)d\theta} \quad \cdots\cdots (2.15)$$

$$I_{dc1-h} = \frac{\sqrt{I_{dc1-RMS}^2 - I_{dc1\_ave}^2}}{I_m} \quad \cdots\cdots (2.16)$$

where, the average value of DC-link current in an electrical angle $I_{dc1-ave}$ is given by modulation index M_1, amplitude of the phase current I_m, and the power factor angle of INV. 1 θ_1 as [2-32]:

Table 2.2. DC-link current with regard to voltage space vector.

Voltage space vector	Switching function			DC-link current i_{dc1}
	s_{u1}	s_{v1}	s_{w1}	
$\boldsymbol{V_0}(---)$	0	0	0	0
$\boldsymbol{V_1}(+--)$	1	0	0	i_{um}
$\boldsymbol{V_2}(++-)$	1	1	0	$-i_{wm}$
$\boldsymbol{V_3}(-+-)$	0	1	0	i_{vm}
$\boldsymbol{V_4}(-++)$	0	1	1	$-i_{wm}$
$\boldsymbol{V_5}(--+)$	0	0	1	i_{wm}
$\boldsymbol{V_6}(+-+)$	1	0	1	$-i_{wm}$
$\boldsymbol{V_7}(+++)$	1	1	1	0

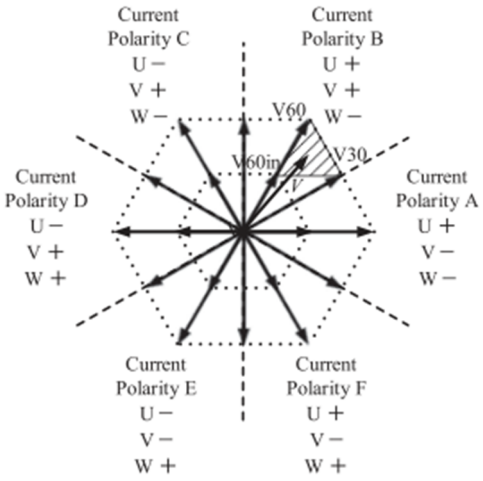
$$I_{dc1-ave} = \frac{3}{4} M_1 I_m \cos\theta_1 \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2.17)$$

In the case of a single inverter, it is known that the output voltage harmonics depend only on the modulation index of the inverter; the input current harmonics depend on the motor power factor in addition to the modulation index. In contrast, in a dual inverter system, since the switching pattern increases, the harmonics change depending on the modulation indices of the two inverters, the phase difference between two inverters, and DC-link voltage ratio.

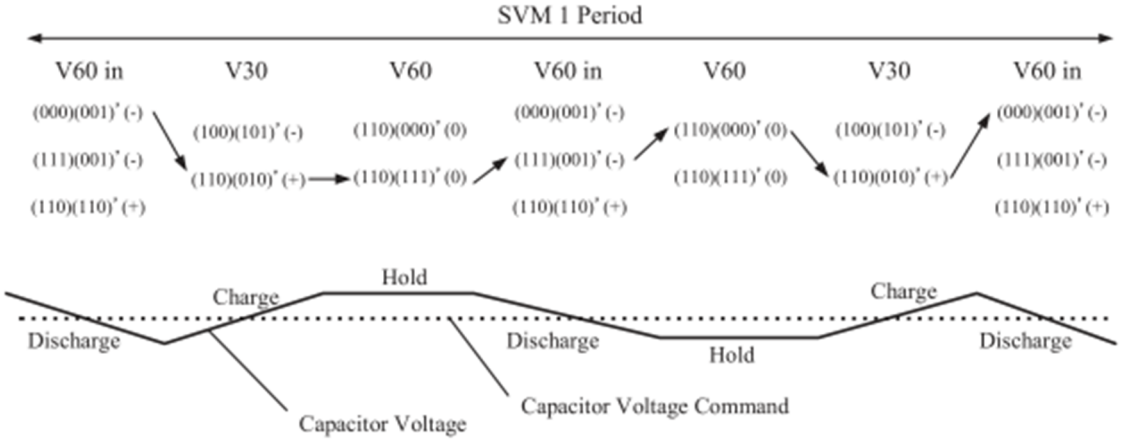
2.4 Conventional Strategies and Their Performances for Dual Inverter Topology

2.4.1 Coupled Modulation Approaches

For coupled modulation, a dual inverter can be treated as a single multi-level converter. To reduce the switching actions, modulation schemes can be used to switch one inverter while clamping the other inverter to one state during a switching period [2-4]. Especially in the FC method, control and modulation strategies of outputting a multi-level waveform by fixing the DC voltage ratio to 2:1 have been investigated [2-9], [2-11], [2-35]. In [2-11], switching patterns focusing on the current sector of the stator is examined (see Fig. 2.12), but it has been reported that the voltage ripple increases when the load is low because the amount of charging/discharging of the FC voltage is proportional to the output current. In addition, although multi-level can be achieved by clamping INV. 1, it has been reported that the FC capacitance increases to compensate for the power generated by the clamping [2-36].



(a)



(b)

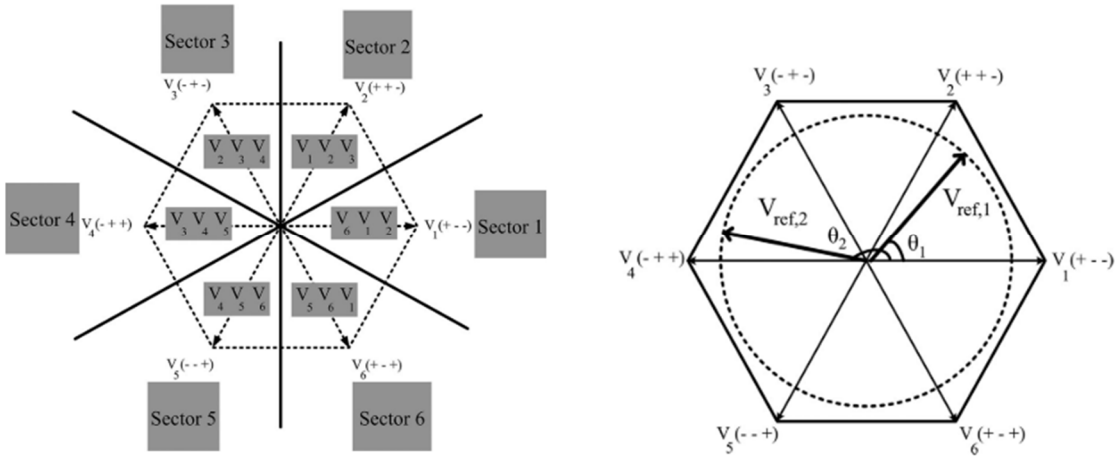
Fig. 2.12. Coupled modulation for multi-level operation. (a) Relationship between phase of current vector and directions of motor line currents, (b) Simultaneous control of capacitor voltage and multilevel voltage waveform generation with SVM.

(Adapted from [2-11] Y. Oto, T. Noguchi, T. Sasaya, T. Yamada, and R. Kazaoka, "Space Vector Modulation of Dual-Inverter System Focusing on Improvement of Multilevel Voltage Waveforms," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9139–9148, 2019)

2.4.2 Decoupled Modulation Approaches

As mentioned before, the output voltage of a dual inverter is the difference between the voltages generated by two inverters. When the decoupled modulation is applied, the voltage reference is feeding into two inverters separately. In the research based on the decoupled modulation strategy, modulation methods that reduce output voltage harmonics in 2DC system with a voltage ratio of 1:1 [2-16], and the unity power factor control of INV. 1 and motor current with variable FC voltage [2-24], [2-37], have been investigated.

In [2-16], the output voltage harmonics when near-state PWM (NSPWM) is applied by giving a phase angle difference to the voltage references of the two inverters are analyzed (see Fig. 2.13). In this method, the output voltage range is expanded by driving with two power supplies, but the low modulation region (low load region) is not supported.



(a) (b)

Fig. 2.13. Decoupled modulation. (a) Sector definition in NSPWM, (b) Voltage references of the dual inverter.

(Adapted from [2-16] A. D. Kiadehi, K. E. K. Drissi, and C. Pasquier, "Voltage THD Reduction for Dual-Inverter Fed Open-End Load with Isolated DC Sources," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2102–2111, 2017)

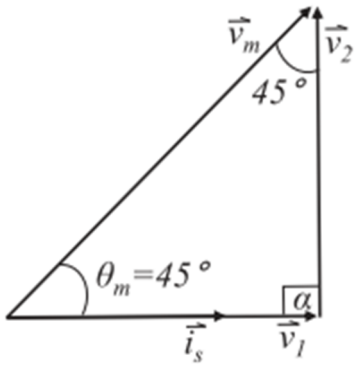


Fig. 2.14. Vector diagram in the unity power factor control.
(Adapted from [2-24] I. J. Smith and J. Salmon, "High-Efficiency Operation of an Open-Ended Winding Induction Motor Using Constant Power Factor Control," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10663–10672, 2018)

In unity power factor control reported in [2-24], INV. 2 compensates for the reactive power and INV. 1 supplies the maximum active power to expand the output voltage range (see Fig. 2.14). However, there are few studies have been conducted on high performance and modulation methods in the light-load region.

2.5 Proposed Phase Control Modulation with Floating Capacitor Topology

2.5.1 For Reducing Output Voltage Harmonics

A control strategy for improving the output voltage total harmonic distortion (THD) in the light-load condition with the FC topology is studied. As mentioned in Section 2.3, the harmonics in output voltage and input current change depending on the several parameters, such as motor power factor angle, output voltage, phase angle difference, and modulation indices of each inverter. In particular, by outputting the synchronized switching patterns in each inverter allows to reduce the peak voltage values applied motor winding (described in Section 2.3). However, in the FC topology, when the phase angle difference is set to zero, the voltage ratio is fixed at 1, which makes motor control impossible. Therefore, this study provides a phase control modulation method to maximize modulation indices of each inverter (M_1, M_2) with minimum phase angle difference α

In order to achieve the above conditions in the light-load region, the phase difference α and the FC voltage reference $V_{dc2-ref}$ are controlled depending on the power factor angle δ and fundamental component of the output voltage V_{fun} as follows.

$$\alpha = \mathrm{Sin}^{-1}\left(\frac{V_{fun}}{\frac{V_{dc1}}{2}M_1}\cos\delta\right) \quad \text{(2.18)}$$

$$V_{dc2-ref} = V_{dc1}\frac{\cos(\alpha+\delta)}{\cos\delta} \quad \text{(2.19)}$$

The waveform improvement leads to increase the motor efficiency; thus, the total efficiency including inverter efficiency increases, and is experimentally obtained to clarify the effectiveness of the proposed method. Furthermore, an operating condition, that allows to reduce the THD of the phase

voltage of motor winding, when the IM driven by the dual inverter with sinusoidal PWM (SPWM) is theoretically described. Then, based on the previous analysis, output voltage harmonics when using various PWM methods such as, third harmonic injection PWM (THIPWM), and discontinuous PWM (DPWM), space vector modulation (SVPWM), and near-state PWM (NSPWM) with a reduced number of commutations, are theoretically analyzed. Originality of this study is to analyze the output voltage harmonics that change not only with the fundamental voltage but also with the power factor angle when typical PWM methods are applied to the dual inverter. Through analysis, the modulation method that minimizes the harmonic components depending on the operating conditions of open-end winding IM is clarified.

2.5.2 For Reducing Input Current Harmonics

A control method to reduce the high-order harmonics caused by PWM in the DC-link current in a dual inverter with an FC topology, which has the same voltage ratings in two inverters, is studied. The proposed control method reduces the high-order harmonic current through a six-step operation at the primary inverter. The secondary inverter supplies a sinusoidal voltage to the motor using a low-rated voltage.

Conventionally, due to use a small capacitance for FC, the FC voltage V_{dc2} is needed to more than twice the input voltage V_{dc1} [2-38]. However, by the proposed phase control modulation, the FC voltage can be reduced while performing the six-step operation of INV. 1. The validity of the proposed control method is confirmed through theoretical analysis of the FC voltage and input DC-link current harmonics. Furthermore, the FC voltage dependencies of the input current harmonics are analyzed.

2.5.3 Beneficial Position of Proposed Phase Control and Modulation Strategies

Fig. 2.15 shows the process of generating gate signals from the output voltage reference. The conventional coupled modulation treats the dual inverter as a single multi-level converter, the identification of the switching states of the two inverters becomes complicated (see Fig. 2.15(a)). In contrast, the proposed phase control is based on decoupled modulation, thus each inverter has a degree of freedom in the modulation method (see Fig. 2.15(b)).

Table 2.Table 2.3 shows a comparison of dual inverter circuit design and

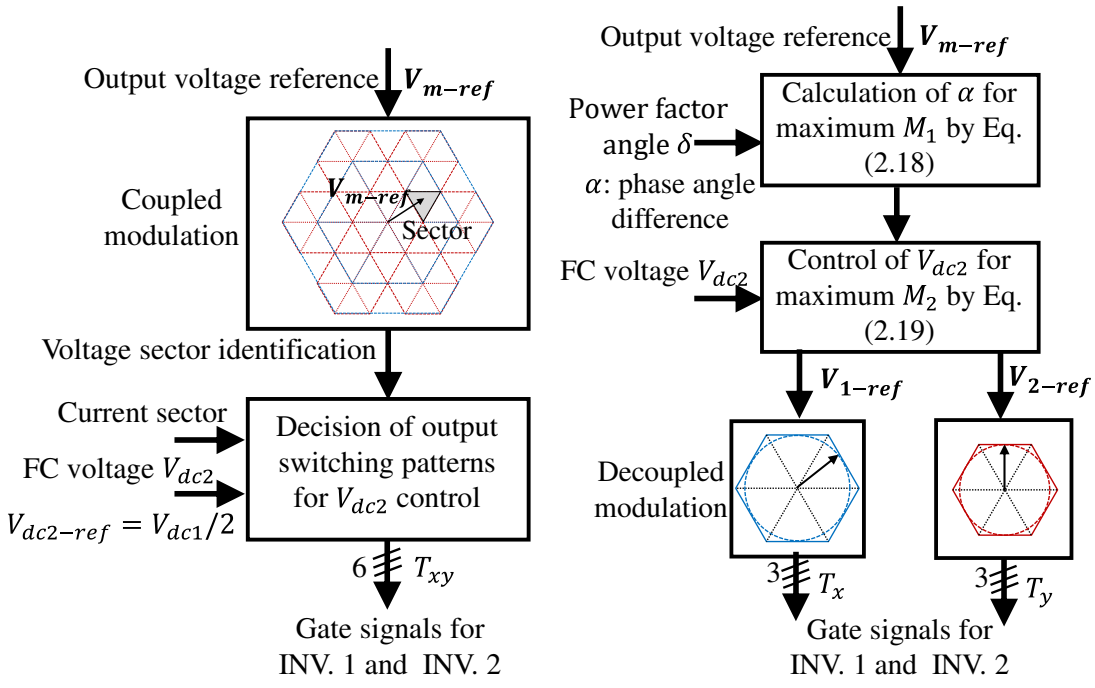


Fig. 2.15. Process of generating gate signals from the output voltage reference with (a) conventional coupled modulation strategy, and (b) proposed decoupled modulation strategy based on the phase controlling.

performance. Since multi-level waveforms can be achieved with coupled PWM, output voltage harmonics are reduced. In addition, the clamping operation of INV. 1 reduces the harmonics caused by the switching of the DC-link current. However, coupled PWM requires an isolated power supply or a large capacitor. In contrast, with decoupled PWM, the output voltage range can be expanded and the FC capacitance can be designed to be small. However, switching both inverters increases the DC-link current harmonics.

Fig. 2.16 shows a comparison of conventional method and proposed method in load area for high performance. In this study, improving the performance in light-load condition of the motor is achieved. Further, by making the DC-link voltage of INV. 2 variable and changing the phase difference between the two inverters depending on the load, it is possible to reduce the harmonics applicable to the light-load region.

Table 2.3. Comparison of dual inverter circuit design and performance

Inverter design				Performance		
Circuit configuration	Modulation strategy	Voltage ratios V_{dc1}:V_{dc2}	Secondary DC-link	Maximum output voltage	Output harmonics (No. of levels)	Input harmonics
Single inverter	PWM	N/A	N/A	1	High (2)	High
Dual inverter with a floating capacitor	Coupled PWM	1:0.5	Large capacitor	~1.5	Low (4)	Low
	Decoupled PWM	1:1	Small capacitor	~2	High (~3)	High
		Varied	Small capacitor	~2	Medium (2~4)	High

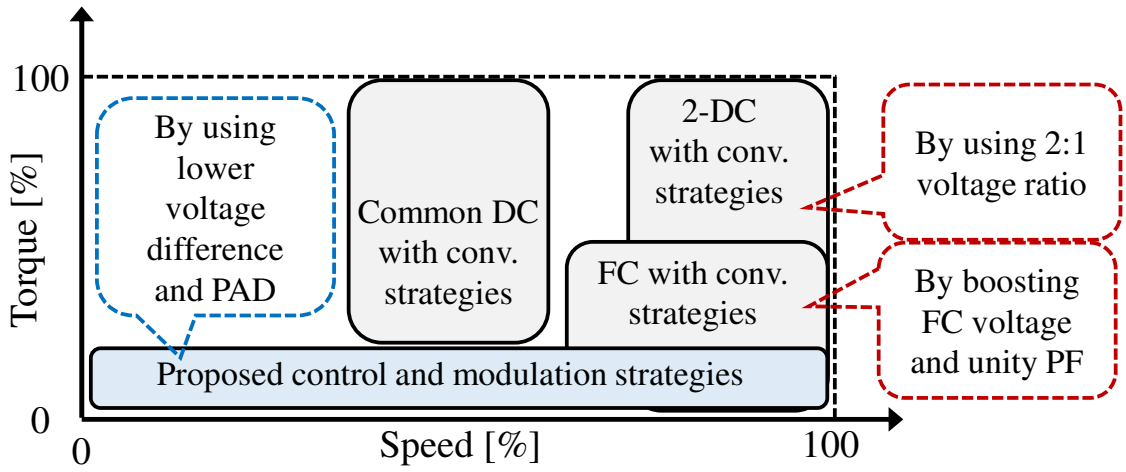


Fig. 2.16. Comparison of conventional method and proposed method in load area for high performance

2.6 Conclusion

In this chapter, research trends in dual inverter configurations are described, and a generalized theory of output voltage harmonics is proposed. The evaluation method of output voltage harmonics and input current harmonics in the dual inverter topology that realizes high performance of the motor drive system. In addition, conventional dual inverter drive methods that reduce input/output harmonics and their issues are discussed. Finally, proposed modulation strategies to reduce the input/output harmonics of the dual inverter topology using the motor power factor, which is the key concept of this thesis, are described and a beneficial position of the proposed strategies along with conventional methods is presented.

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Chapter 3

Phase Control Modulation for Output Voltage Harmonics Reduction in Light-Load Condition

3.1 Introduction

This chapter proposes a control strategy for improving the voltage total harmonic distortion (THD) of the dual inverter driven induction motor (IM) in the light-load condition. The waveform improvement leads to increase the motor efficiency; thus, the total efficiency including inverter efficiency increases, and is experimentally obtained to clarify the effectiveness of the proposed method. Furthermore, an operating condition, that allows to reduce the THD of the phase voltage of motor winding, when the IM driven by the dual inverter with sinusoidal PWM (SPWM) is theoretically described. The performance of the proposed method is demonstrated by experiment using an open-ended general-purpose IM. The proposed method allows to reduce the carrier harmonics compared with the conventional methods, which operates as a single-inverter at low-load condition for inverter loss reduction [3-1]–[3-3], and a method to expand the operating range by setting the power factor of main inverter and motor current to 1.

This chapter is organized as follows: firstly, the configuration of the dual

inverter fed open-end winding induction motor induction motor drive system and basis of the floating capacitor (FC) topology are introduced. Secondly, principle of voltage harmonics, which are related to fundamental voltage and power factor angle, in the case of dual inverter and single-inverter with SPWM, is theoretically analyzed. Thirdly, the proposed control strategy, which realizes the reduction of the voltage harmonics by phase angle difference between two inverters is described. Finally, the experimental validation, which demonstrates the reduction of voltage harmonics by proposed method is carried out.

3.2 Theoretical Analysis of Voltage Harmonics

3.2.1 Voltage Vectors and Outputting Times of Dual Inverter

In this study, theoretical voltage THD is calculated to evaluate the reduction in the voltage harmonics related to the carrier frequency. The circuit configuration of the dual inverter with the FC for the open-end winding induction motor is shown in Fig. 3.1. The system consists of an open-end winding induction motor and two 2-level voltage source inverters (VSIs), which are connected to the opposite terminals of stator windings, and the dual inverter is powered by a single DC voltage source. The primary inverter (INV. 1) has a DC power supply, and the secondary inverter (INV. 2) has a capacitor.

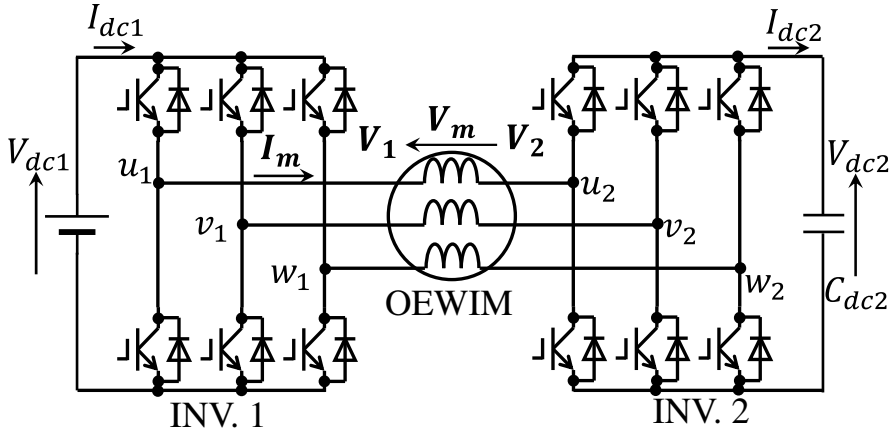
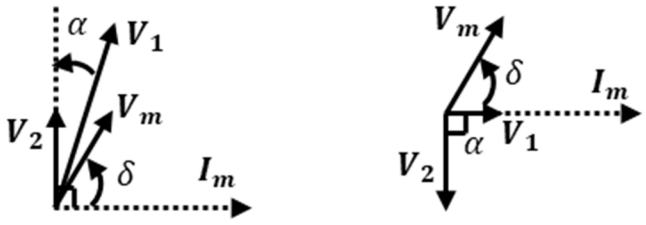


Fig. 3.1. Dual inverter circuit with a FC topology.



(a) (b)

Fig. 3.2. Vector diagram of the dual inverter with a FC when (a) INV. 1 lags INV. 2 and (b) INV. 1 leads INV. 2.

Fig. 3.2 shows the vector diagram of the dual inverter with an FC when (a) INV. 1 lags INV. 2 and (b) INV. 1 leads INV. 2.

The voltage harmonics are expressed as the difference between the RMS values of the modulated waveform and the fundamental component. The RMS value of the modulated waveform of the dual inverter system, which includes all harmonic components and the fundamental component, is calculated by (2.12). As mentioned in Section 2.3.2, the output time T_{xy-sw} of each vector V_{xy}, which normalized by a switching period T_s, is determined by the relation between voltage references of INV. 1, and INV. 2 as:

$$\begin{cases} v_{u1-ref} = M_1 \cos(\theta) \\ v_{v1-ref} = M_1 \cos\left(\theta - \frac{2}{3}\pi\right) \\ v_{w1-ref} = M_1 \cos\left(\theta + \frac{2}{3}\pi\right) \end{cases} \quad \begin{cases} v_{u2-ref} = M_2 \cos(\theta + \alpha) \\ v_{v2-ref} = M_2 \cos\left(\theta - \frac{2}{3}\pi + \alpha\right) \\ v_{w2-ref} = M_2 \cos\left(\theta + \frac{2}{3}\pi + \alpha\right) \end{cases} \quad \text{..... (3.1)}$$

Here, $\theta = \omega t$ denotes the fundamental angular frequency, and INV. 2 voltage leads INV. 1 voltage by phase angle difference α. Fig. 3.3. Resulting vectors in a switching period T_s when (a) $M_1 = M_2$ and (b) $M_1 < M_2$ shows the resulting vectors in a switching period T_s when (a) $M_1 = M_2$ and (b) $M_1 < M_2$, as an example. Under condition Fig. 3.3. Resulting vectors in a switching period T_s when (a) $M_1 = M_2$ and (b) $M_1 < M_2$(b), the output times of the same vector number ($V_{11'}$ and $V_{22'}$) decreases, and the output time of different vector numbers increases. When the same vector number is output, the voltage applied to the winding is proportional to the DC voltage difference; thus, the voltage peak value can be decreased by reducing the DC voltage difference. Furthermore, under condition Fig. 3.3. Resulting vectors in a switching period T_s when (a) $M_1 = M_2$ and (b) $M_1 <$

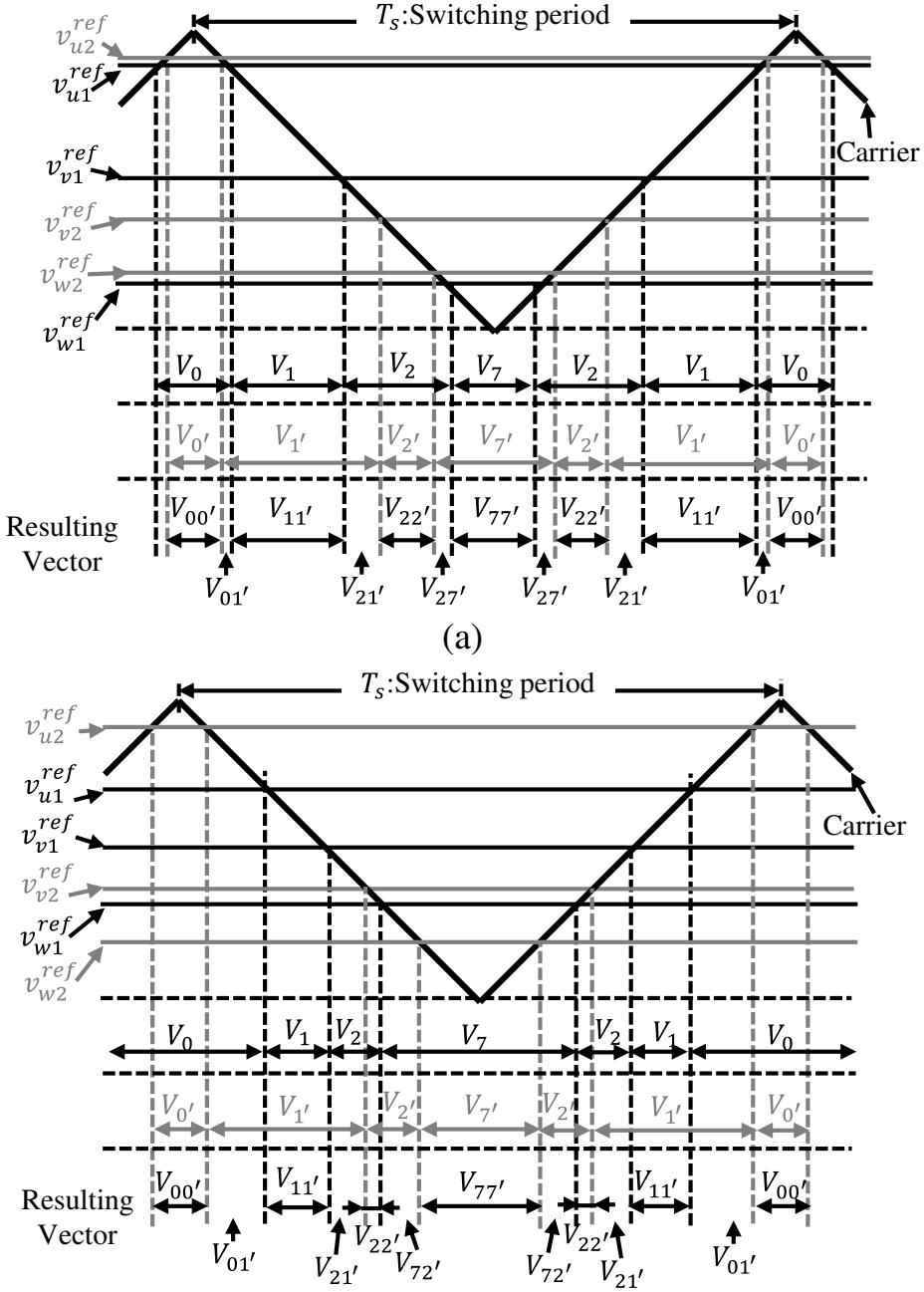


Fig. 3.3. Resulting vectors in a switching period T_s when (a) $M_1 = M_2$ and (b) $M_1 < M_2$

M_2(a), the output time of the same vector number increases by reducing α. Therefore, a method to control $M_1 = M_2$ is proposed in this study. The modulation indices are defined as $M_1 = M_2 = M$ in the following calculations. Note that there are 64 switching states, T_{xy-sw} are described below

as examples:

$$\begin{cases} T_{00-sw} = \left(1 - v_{u2}^{ref}\right)T_s & \text{if } \left(\frac{\alpha}{2} \le \omega t \le \frac{\pi}{3} + \frac{\alpha}{2}\right) \\ T_{01-sw} = \left(v_{u2}^{ref} - v_{u1}^{ref}\right)T_s & \text{if } \left(\frac{\alpha}{2} \le \omega t \le \frac{\pi}{3}\right) \\ T_{11-sw} = \left(v_{u1}^{ref} - v_{v1}^{ref}\right)T_s & \text{if } \left(\frac{\alpha}{2} \le \omega t \le \frac{\pi}{3}\right) \\ T_{21-sw} = \left(v_{v1}^{ref} - v_{v2}^{ref}\right)T_s & \text{if } \left(\alpha \le \omega t \le \frac{\pi}{3}\right) \\ T_{22-sw} = \left(v_{v2}^{ref} - v_{w2}^{ref}\right)T_s & \text{if } \left(\alpha \le \omega t \le \frac{\pi}{3} + \frac{\alpha}{2}\right) \\ T_{27-sw} = \left(v_{w2}^{ref} - v_{w1}^{ref}\right)T_s & \text{if } \left(\alpha \le \omega t \le \frac{\pi}{3} + \frac{\alpha}{2}\right) \\ T_{77-sw} = -v_{w1}^{ref}T_s & \text{if } \left(\frac{\alpha}{2} \le \omega t \le \frac{\pi}{3} + \frac{\alpha}{2}\right) \end{cases} \quad \cdots\cdots \quad (3.2)$$

where T_{xy-sw} varies in relation to the phase angle ωt, thus the average time T_{xy} can be calculated by integrating with the electrical angle. Note that 64 combinations of the vector are possible, and it is necessary to calculate each of these vectors.

$$\begin{cases} T_{00} = \frac{3}{\omega}\left\{\frac{\pi}{3} - M\sin\left(\frac{\pi}{3} + \frac{\alpha}{2}\right)\right\} \\ T_{01} = \frac{M}{\omega}\left\{-\frac{\sqrt{3}}{2} + \sin\left(\frac{\pi}{3} + \frac{\alpha}{2}\right)\right\} \\ T_{11} = \frac{\sqrt{3}M}{\omega}\left\{1 - \sin\left(\frac{\pi}{6} + \frac{\alpha}{2}\right)\right\} \\ T_{21} = \frac{M}{\omega}\left\{-\sqrt{3} + 2\sin\left(\frac{\pi}{3} + \frac{\alpha}{2}\right)\right\} \\ T_{22} = \frac{\sqrt{3}M}{\omega}\left\{1 - \sin\left(\frac{\pi}{6} + \frac{\alpha}{2}\right)\right\} \\ T_{27} = \frac{M}{\omega}\left\{-\frac{\sqrt{3}}{2} + \sin\left(\frac{\pi}{3} + \frac{\alpha}{2}\right)\right\} \\ T_{77} = \frac{3}{\omega}\left\{\frac{\pi}{3} - M\sin\left(\frac{\pi}{3} + \frac{\alpha}{2}\right)\right\} \end{cases} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (3.3)$$

3.2.2 Voltage RMS and THD Calculation

The voltage RMS value ($V_{RMS,dual}$), including carrier harmonics resulting from the use a dual inverter with SPWM, is calculated by inserting each value V_{xy} and T_{xy} into (2.12) as follows:

$$V_{RMS,dual} = \sqrt{\frac{V_{00}^2 T_{00} + V_{01}^2 T_{01} + \cdots + V_{77}^2 T_{77}}{T}} = V_{dc1}\sqrt{\frac{M}{\sqrt{3}\pi}\left\{1 + G_{dc}^2 - \sqrt{\frac{28}{3}} G_{dc}\cos\varphi\right\}} \quad \cdots\cdots \quad (3.4)$$

$$\varphi = \frac{\alpha}{2} + \mathrm{Tan}^{-1}\left(\frac{2}{\sqrt{3}}\right) \quad \cdots\cdots \quad (3.5)$$

where $G_{dc} = V_{dc2}/V_{dc1}$. Furthermore, the fundamental voltage of the dual inverter ($V_{fun,dual}$) is obtained by substituting (2.5), (2.6) into (2.4) as follows:

$$V_{fun,dual} = V_{dc1}\frac{M}{2\sqrt{2}}\sqrt{1 + G_{dc}^2 - 2G_{dc}\cos\alpha} \quad \cdots\cdots \quad (3.6)$$

Here, $V_{fun,dual}$ is the RMS value of the winding voltage, thus, $V_{fun,dual} = |\boldsymbol{V_m}|/\sqrt{2}$. Finally, the voltage THD is calculated by (2.13) as:

$$THD_{dual} = \sqrt{\frac{V_{RMS,dual}^2}{V_{fun,dual}^2} - 1} = \sqrt{\frac{8}{\sqrt{3}\pi M}\frac{1 + G_{dc}^2 - \sqrt{\frac{28}{3}} G_{dc}\cos\varphi}{1 + G_{dc}^2 - 2G_{dc}\cos\alpha} - 1} \quad . \quad (3.7)$$

In contrast, the RMS and THD values when the motor is driven by a single inverter with SPWM are calculated by substituting $V_{dc2} = 0$ into

(3.4)-(3.7) as follows:

$$V_{RMS,single} = V_{dc1}\sqrt{\frac{M}{\sqrt{3}\pi}} \quad \cdots\cdots (3.8)$$

$$V_{fun,single} = V_{dc1}\frac{M}{2\sqrt{2}} \quad \cdots\cdots (3.9)$$

$$THD_{single} = \sqrt{\frac{8}{\sqrt{3}\pi M} - 1} \quad \cdots\cdots (3.10)$$

In a dual inverter with an FC topology, $V_{fun,dual}$ and $V_{RMS,dual}$ depend on G_{dc}, α, and M as in (3.4) and (3.6). This means that the these variables can be obtained by reducing $V_{RMS,dual}$ even if V_{fun} remains constant. However, for single-inverter operation, THD_{single} depends only on M as shown in (3.10).

3.2.3 Characteristics of Voltage THD

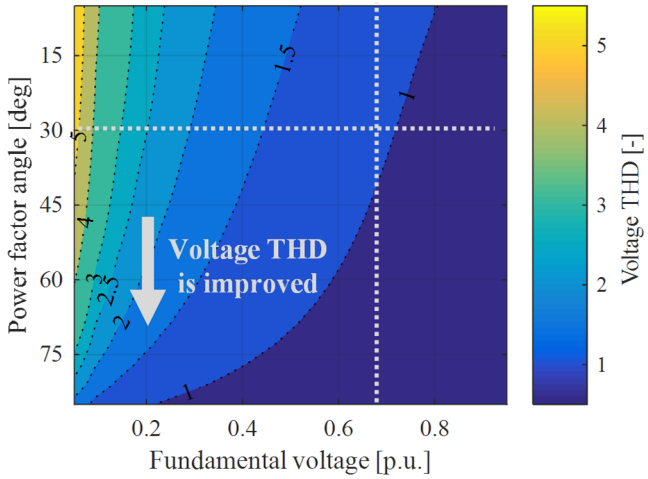
In the proposed phase modulation control, the phase angle difference α are calculated as follows (see Section 2.5.1):

$$\alpha = \mathrm{Sin}^{-1}\left(\frac{|\boldsymbol{V_m}|}{|\boldsymbol{V_1}|}\cos\delta\right) \quad \cdots\cdots (3.11)$$

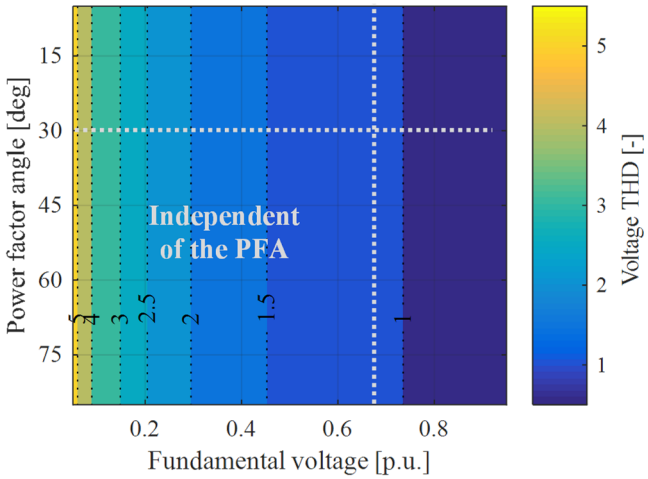
Here, $|\boldsymbol{V_m}|$ equals $\sqrt{2}V_{fun,dual}$. By (3.6) and (3.7), the characteristic of THD_{dual} can be theoretically calculated, where $V_{fun,dual}$ and δ are given parameter according to the motor load condition.

The theoretical calculation of the voltage THD is carried out to clarify the condition under which the voltage THD is reduced by a dual inverter compared with a single inverter drive, as shown in Fig. 3.4 (a) and (b). The modulation index of the dual inverter M is set to 1, while M of the single

inverter is proportional to the fundamental voltage. Here, 1 p.u. of the fundamental voltage indicates that the inverter outputs a voltage of $V_{dc1}/(2\sqrt{2})$, which equals the maximum voltage of the single inverter. In the dual inverter, α and V_{dc2} change depending on δ; Hence the voltage THD is improved as increasing δ. In contrast, the voltage THD characteristic of the single inverter is drawn according to (3.10), which indicates that the voltage THD is only related to M. This means that the voltage THD does not depend on δ. Therefore, voltage THD can be improved in the region where δ is more



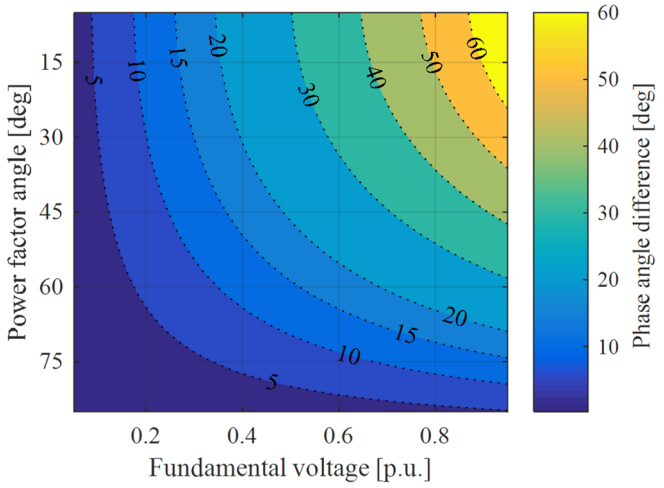
(a)



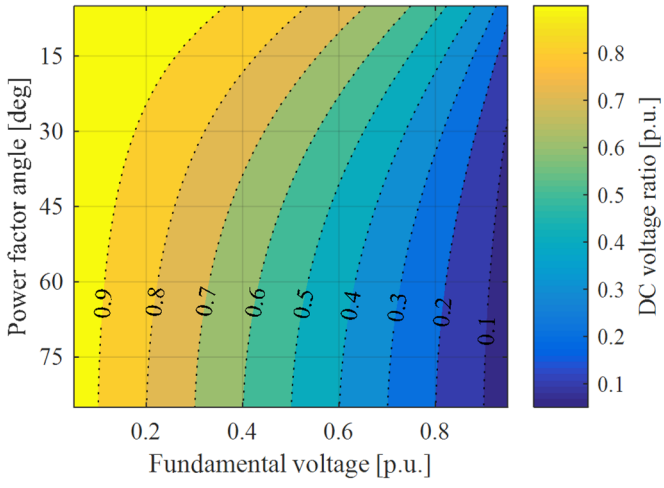
(b)

Fig. 3.4. Theoretical analysis of (a) THD with dual inverter and (b) THD with single inverter for different fundamental voltage with different power factor angle.

than about 30 deg. Fig. 3.5(a) and (b) indicate that a lower THD is achieved by assigning values to α and V_{dc2}/V_{dc1} that are close to 0 and 1, respectively. In general, the fundamental component of the stator voltage is proportional to the motor speed, whereas the power factor angle varies depending on the motor torque; thus, the THD characteristic indicates that the dual inverter with the proposed operation can reduce the THD when the motor is driven at a low-torque condition.



(a)



(b)

Fig. 3.5. Theoretical analysis of (a) phase angle difference and (b) DC voltage ratio for different fundamental voltage with different power factor angle.

3.3 Control Strategy for Voltage THD Reduction

3.3.1 Method for Setting Modulation Index at Maximum

According to previous study presented in Chapter 2.3 verified the reduction in the voltage harmonics by outputting a synchronized PWM waveform and maintaining the modulation indices in the dual inverter system, which has two-isolated DC power supply, at their maximum values. The results indicate that voltage harmonics can be reduced by assigning a low value to the phase angle difference α even in the case of the system in which the FC, instead of the power supply, is connected to INV. 2.

As mentioned in Section 3.2, the voltage THD can be reduced by assigning a large value to the modulation indices M_1 and M_2. This study proposes a method for setting the output voltage of each inverter ($\boldsymbol{V_1} = \begin{bmatrix} v_{d1} & v_{q1} \end{bmatrix}^T$ and $\boldsymbol{V_2} = \begin{bmatrix} v_{d2} & v_{q2} \end{bmatrix}^T$) to achieve the required motor voltage ($\boldsymbol{V_m} = \begin{bmatrix} v_{dm} & v_{qm} \end{bmatrix}^T$). A whole of proposed control system is shown in Fig. 3.6. Since $\boldsymbol{V_m}$ is given by the PI controller of the motor current $\boldsymbol{I_m} = \begin{bmatrix} i_{dm} & i_{qm} \end{bmatrix}^T$ and is represented as the voltage difference between INV. 1 and INV. 2, either $\boldsymbol{V_1}$ or $\boldsymbol{V_2}$ can be decided arbitrarily. To obtain the output $\boldsymbol{V_m}$ by setting the value of M_2 to 1, $\boldsymbol{V_2}$ is calculated as follows: the unit vector of $\boldsymbol{V_m}$ is rotated by θ_2, and multiplied by the maximum amplitude of $\boldsymbol{V_2}$ $(= M_2 V_{dc2}/2)$.

$$\boldsymbol{V_2} = \frac{M_2}{2} V_{dc2} \boldsymbol{T}(\theta_2) \frac{\boldsymbol{V_m}}{|\boldsymbol{V_m}|} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3.12)$$

$$\boldsymbol{T}(\theta_2) = \begin{bmatrix} \cos\theta_2 & -\sin\theta_2 \\ \sin\theta_2 & \cos\theta_2 \end{bmatrix} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3.13)$$

$$\theta_2 = \frac{\pi}{2} - \delta - \beta \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3.14)$$

where θ_2 is the phase difference between $\boldsymbol{V_m}$ and $\boldsymbol{V_2}$ and is given by

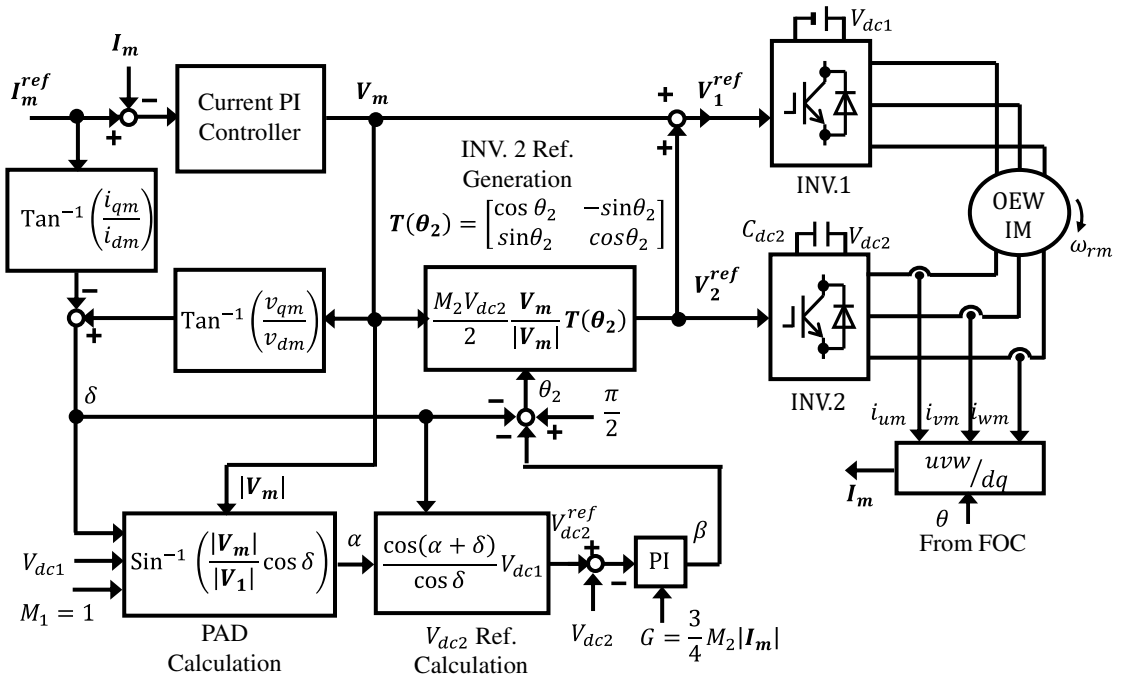


Fig. 3.6. Proposed control system (OEWIM: Open-End Winding Induction Motor).

(3.14), because $\boldsymbol{V_2}$ leads to $\boldsymbol{I_m}$ by $\pi/2$ at the steady state (see Fig. 3.2(a)). In addition, the power factor angle δ is calculated by the angle difference between $\boldsymbol{V_m}$ and $\boldsymbol{I_m}$ as follows:

$$\delta = \text{Tan}^{-1}\left(\frac{v_{qm}}{v_{dm}}\right) - \text{Tan}^{-1}\left(\frac{i_{qm}}{i_{dm}}\right) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3.15)$$

In equation (3.14), $(\pi/2 - \beta)$ indicates that the power factor angle between $\boldsymbol{V_2}$ and $\boldsymbol{I_m}$; thus when β is positive, the capacitor is charged, and when β is negative, the capacitor is discharged. In this proposed method, β is given by the PI controller of the FC voltage V_{dc2}, which is described in the next section. Finally, $\boldsymbol{V_1}$ is calculated by $\boldsymbol{V_2} + \boldsymbol{V_m}$ because the motor voltage is expressed as the voltage difference between INV.1 and INV. 2.

By the slip-frequency-type field-oriented control [3-4], [3-5], the fundamental angular frequency ω and phase angle θ are obtained, as shown in Fig. 3.7 Here, ω_{rm}, ω_{re}, and ω_s denote the mechanical angular frequency, electrical angular frequency, and slip angular frequency, respectively.

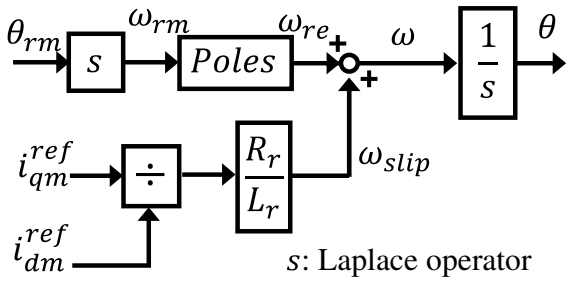


Fig. 3.7. θ calculation based on the slip-frequency-type field-oriented control (FOC) [3-4], [3-5].

3.3.2 Floating Capacitor Voltage Control

According to the relationship between M_1, V_{dc2}, and α represented Section 2.2.4, it is necessary to control V_{dc2} to the following value in order to assign M_1 to 1:

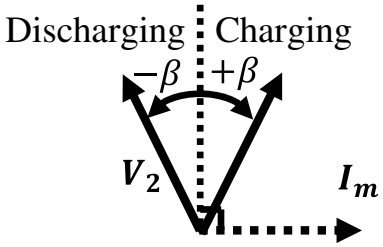
$$V_{dc2}^{ref} = \frac{\cos(\alpha + \delta)}{\cos\delta} V_{dc1} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3.16)$$

Here, α and δ are calculated using (3.11) and (3.15), respectively, thus the FC voltage reference V_{dc2}^{ref} varies depending on the motor operating condition.

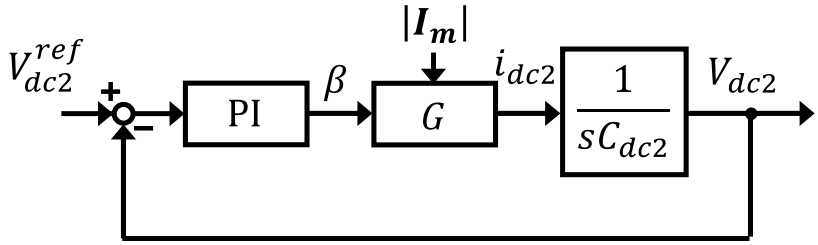
Generally,V_{dc2} is represented by the integral of I_{dc2} (the FC current) divided by the capacitance C_{dc2}, but I_{dc2} cannot be controlled directly. In this study, the FC voltage PI controller is applied, which method uses β. Control system of the FC voltage is shown in Fig. 3.8. Ignoring the losses caused by the AC/DC conversion, the active power of the INV. 2, P_2, is the same on the AC and DC sides. Therefore, the relation between I_{dc2}, and β is expressed as follows (see Fig. 8(a)) [3-6], [3-7]:

$$P_2 = V_{dc2} I_{dc2} = 3|\boldsymbol{V_2}||\boldsymbol{I_m}|\sin\beta \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3.17)$$

$$I_{dc2} = \frac{3}{4} M_2 |\boldsymbol{I_m}| \sin\beta \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3.18)$$



(a)



(b)

Fig. 3.8. Floating capacitor voltage control system in the proposed method.

Here, β is kept low because the active power is not used to drive the motor in this proposed method; thus, the gain factor G is given by:

$$G = \frac{I_{dc2}}{\beta} \cong \frac{3}{4} M_2 |\boldsymbol{I_m}| \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3.19)$$

where, G is a coefficient that converts I_{dc2}, which output from the PI controller, to β. In this voltage controller, G is proportional to the amplitude of $\boldsymbol{I_m}$ and M_2.

3.4 Experimental Results

3.4.1 Experimental Setup and Conditions

Experimental conditions and parameters of the open-end winding induction motor are shown in Table 3.1 and Table 3.2. A general-purpose induction motor (TFO-FK 0.75KW 4P 200V, made by HITACHI) is used for experiment. In this experiment, a DC power supply regulates the INV. 1 DC voltage at 300 V. The selection of the capacitance of the FC in various dual inverter drive methods is reported in [3-8]. It is known that in the operation method in which the sinusoidal voltage is output from both inverters, the sixth-order fluctuation of the DC voltage occurs due to the harmonic current caused by dead-time and spatial harmonics. This experiment focuses on verifying the reduction of voltage harmonics caused by PWM; thus, the capacitance was set to 330 uF to sufficiently reduce the fluctuation of V_{dc2}. Coupling modulation strategies require a capacitance of approximately 1000 to 3000 uF [3-9]–[3-11], but decoupling modulation strategies can be designed to be about 0.1 times of the capacitance [3-8].

Fig. 3.9 shows an experimental setup. Three-phase stator currents $\boldsymbol{I_m}$, a FC voltage V_{dc2}, and a rotor mechanical angle θ_{rm} are measured for controlling the motor and the dual inverter. The d-axis current reference i_{dm}^{ref} is set constant value 2.52 A, which achieves the rated flux 0.520 Vs/rad, while the q-axis current reference i_{qm}^{ref} varies depending on the load torque. In addition, for the verification of the proposed method, the open-end winding induction motor is loaded at a constant speed by the load motor, and is driven constant torque by the current control of the dual inverter.

Table 3.1. Experimental condition.

INV.1 DC Voltage: V_{dc1}	300 V
INV.2 DC Voltage: V_{dc2}	Varies according to (3.16)
INV.2 Capacitance: C_{dc2}	330 uF
Carrier Frequency: f_{c1}	5 kHz
Dead-time: T_{DT}	500 ns

Table 3.2. Parameters of the open-end winding induction motor.

Rated power	750 W	Poles	4
Rated voltage	200 V	Rated frequency	50 Hz
Rated current	3.5 A	Rated speed N_{rated}	1410 rpm
Stator resistance R_s	2.74 Ω	Leakage inductance l_s, l_r	10.5 mH
Rotor resistance R_r	2.08 Ω	Mutual inductance L_m	0.195 H

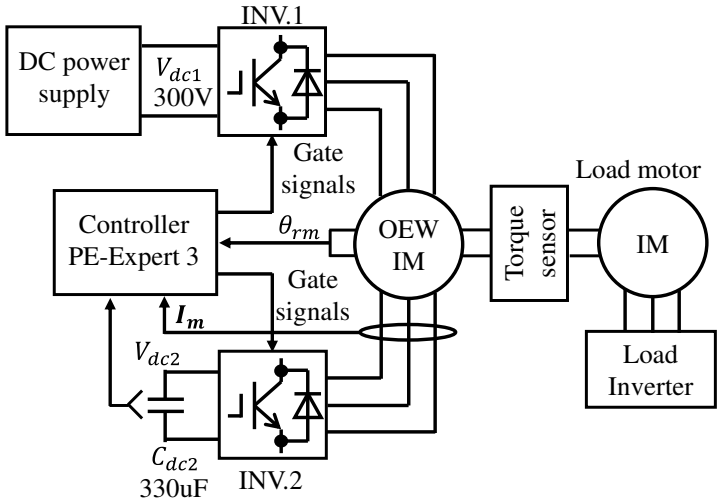


Fig. 3.9. Experimental setup.

In this experiment, in order to indicate the effectiveness of the proposed method, a comparison with two conventional methods is carried out. Fig. 3.10 shows the vector relationships with (a) single inverter, (b) dual inverter with conventional control, and (c) dual inverter with proposed control. The first is a method to improve the efficiency of the inverter by setting the FC voltage to zero, while the INV. 2 output voltage to zero in the low load region [3-12]. This method is called "single inverter operation" and can be achieved by setting $V_{dc2}^{ref} = 0$ V. The second method is to expand the output voltage range by setting the power factor between INV. 1 and the motor current to 1 and supplying reactive power from INV. 2 [3-1], [3-2]. This method is called

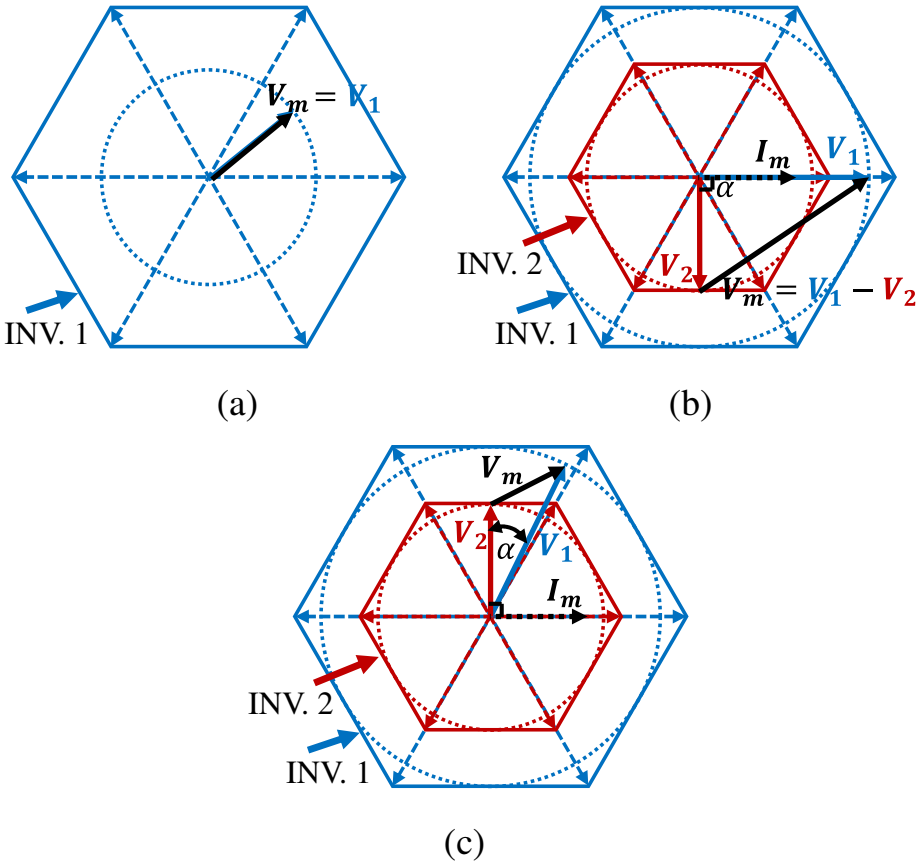
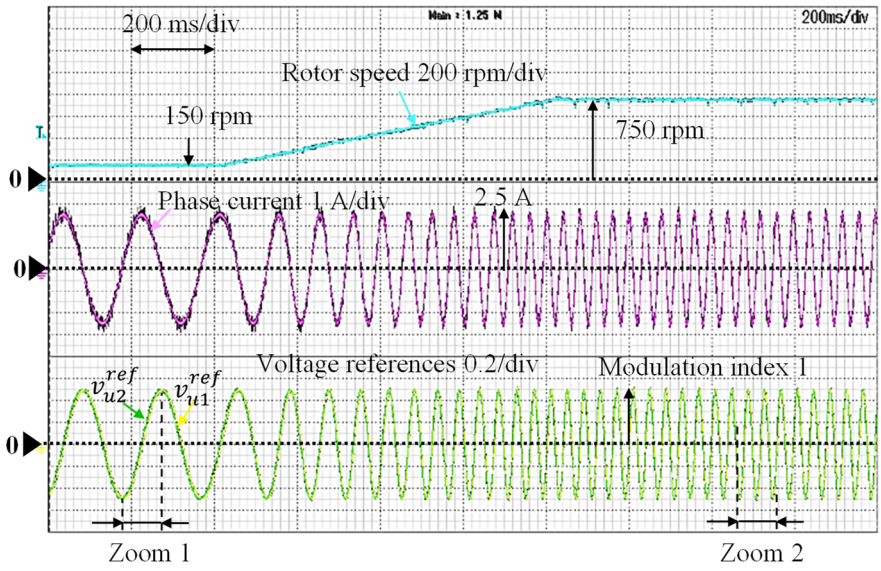


Fig. 3.10. Comparison of the vector relationships with (a) single inverter, (b) dual inverter with conventional control (α is fixed at $\pi/2$), and (c) dual inverter with proposed control (α is changed depending on the load condition).

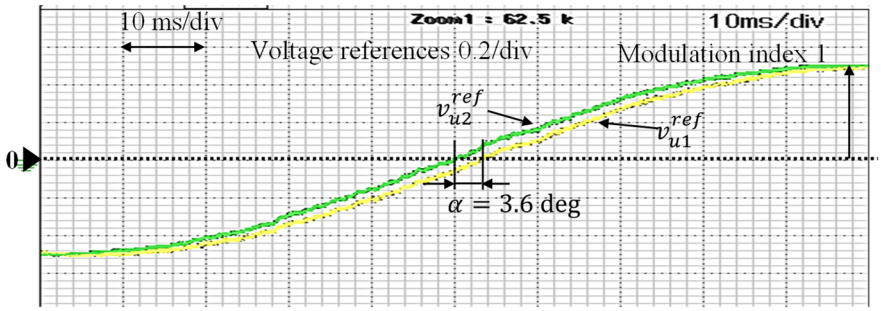
"dual inverter with conventional operation" and can be achieved by setting phase angle difference $\alpha = 90$ deg (see Fig. 3.10(b)). In contrast, “dual inverter with proposed operation” is a control method in which phase angle difference α is assigned smaller according to (3.11), to make the FC voltage closer to the power supply voltage (see Fig. 3.10(c)).

3.4.2 Performance of the Proposed Method

First, the basic operation of the proposed control method is confirmed. Fig. 3.11 shows the performance of the proposed method during a speed transient from 150 rpm to 750 rpm. From Fig. 3.11 (a), it is confirmed that the current control is stable even if the speed is changed, and the maximum value of the phase voltage references v_{u1} and v_{u2} are kept at 1. It means that modulation index can be controlled to 1. In addition, in order to confirm that the phase angle difference α changes, the zoomed waveforms of the voltage references at 150 rpm and 750 rpm are shown in Fig. 3.11 (b) and (c), respectively. From the results, it is confirmed that v_{u2} leads v_{u1} by 3.6 degrees and 9.0 degrees; it indicate that as increasing them motor speed (the motor voltage increase), current control is achieved by increasing the phase angle difference α.



(a)



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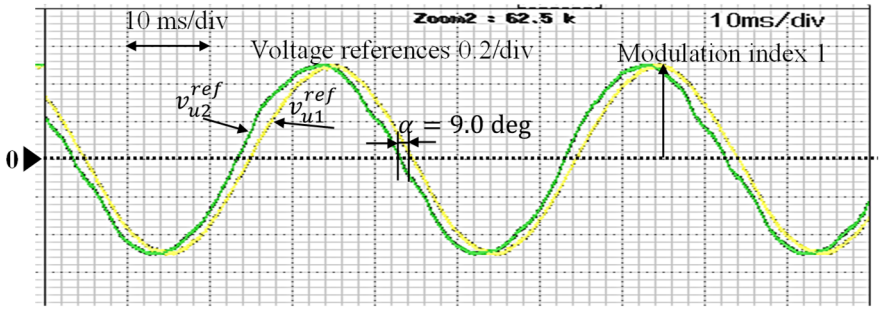

(c)

Fig. 3.11. Dynamic performance of the proposed method during a speed transient from 150 rpm to 750 rpm. (a) Motor speed, phase current, and phase voltage references v_{u1}, v_{u2}. Zoomed waveforms of voltage references v_{u1}, v_{u2} at (b) 150 rpm and (c) 750rpm.

3.4.3 Waveforms and Harmonics Analysis

Steady state performances of the proposed method and the conventional methods are experimentally obtained. Fig. 3.12 show U-phase voltage and current waveforms when the open-end winding induction motor is driven at a speed of 600 rpm and a torque of 0.5 Nm. From the voltage waveform shown in Fig. 3.12, it is confirmed that the number of voltage levels is increased in the dual inverter operation compared to the single-inverter operation. Here, the results of the dual inverter show that the output time of peak voltage is short when using the proposed method (see Fig. 3.12(b)). Furthermore, current waveforms indicate that the proposed current control is achieved as well as the single-inverter operation, even if the modulation index of each inverter is kept at 1. The bottom waveforms of Fig. 3.12 show the FC voltage reference V_{dc2}^{ref} and response V_{dc2}; the results indicate that V_{dc2} follows the reference without deviation, and is controlled constantly having approximately 10 V of the voltage fluctuation ΔV. In the result of the single-inverter operation, the FC voltage is regulated to 0 V (see Fig. 3.12(a)), while in the result of the conventional operation, it is confirmed that the FC voltage is controlled smaller than that of the proposed operation (see Fig. 3.12(b),(c)). Therefore, the proposed control method is operating stably.

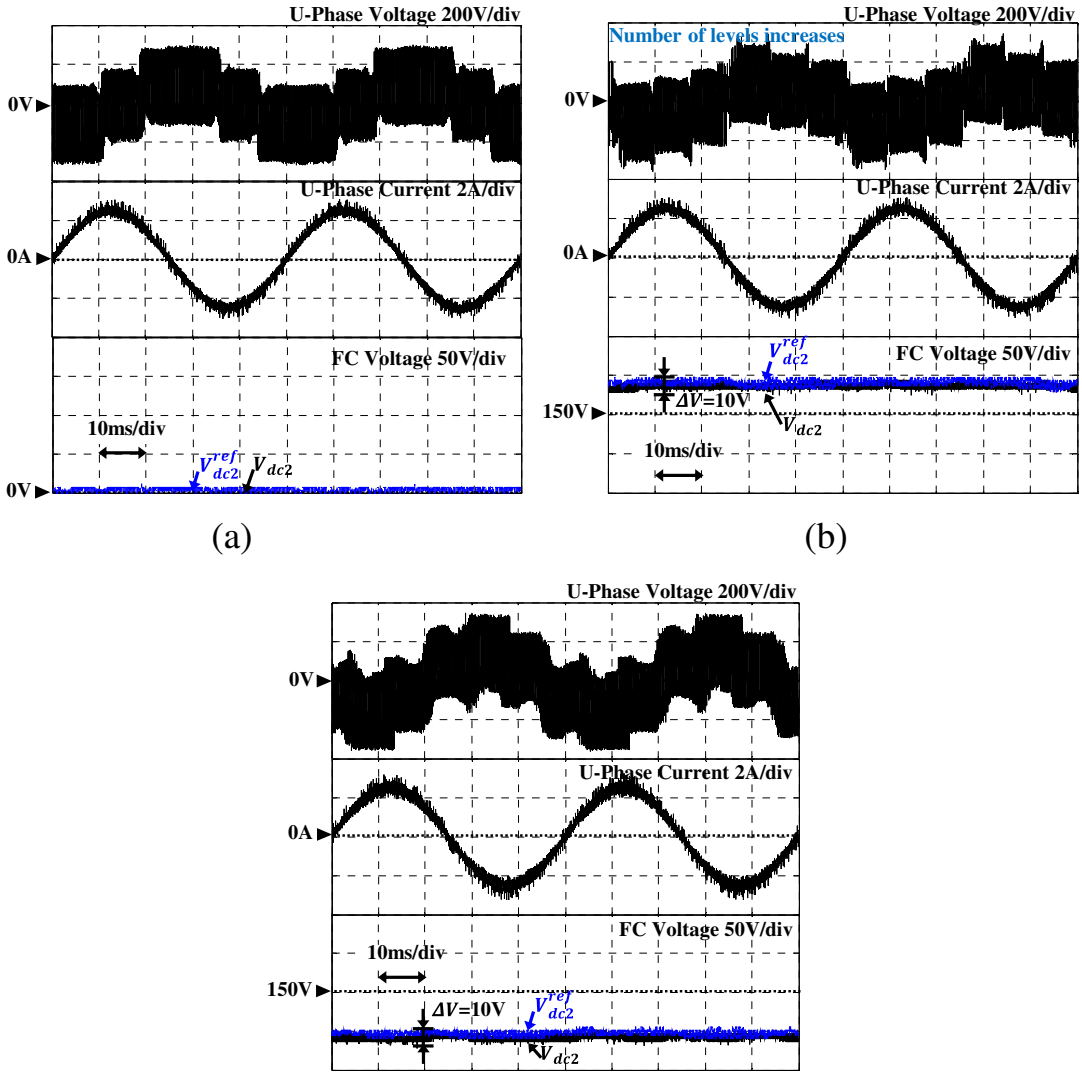

Fig. 3.12. U-phase voltage, current, and FC voltage waveforms when using (a) single-inverter operation, (b) dual inverter with proposed operation, and (c) dual inverter with conventional operation at a speed of 600 rpm a torque of 0.5 Nm.

Harmonics analysis of the U-phase voltage is carried out under the same condition (at a speed of 600 rpm and a torque of 0.5 Nm), as shown in Fig. 3.13, where V_{Cx} represents a harmonic component x times the carrier component. Here, the harmonic analysis and the THD calculation shown in Fig. 3.13 are performed up to 60 kHz. Since the switching frequency of the inverter is 5 kHz, the harmonic components up to 12 times are taken into account. Moreover, since the fundamental frequency is 20 Hz, up to the 300th order component are calculated. In the case of single-inverter operation (Fig. 3.13(a)), harmonic component, especially V_{C2} appears approximately more than two times value compared with other method. In contrast, using dual inverter with proposed operation (Fig. 3.13(b)), the harmonic components that are integer multiple of the carrier component are reduced by other methods. Here, the reason why the carrier frequency component V_{C1} is increasing is that, the two inverters are operated in the dual inverter system, and the components are strengthening each other. However, the voltage THD is reduced from 1.28 to 1.13 (-15 percentage points (pp)) compared with the conventional operation, and is reduced from 1.64 to 1.13 (-51 pp) compared with the single inverter operation, due to the overall reduction of other components.

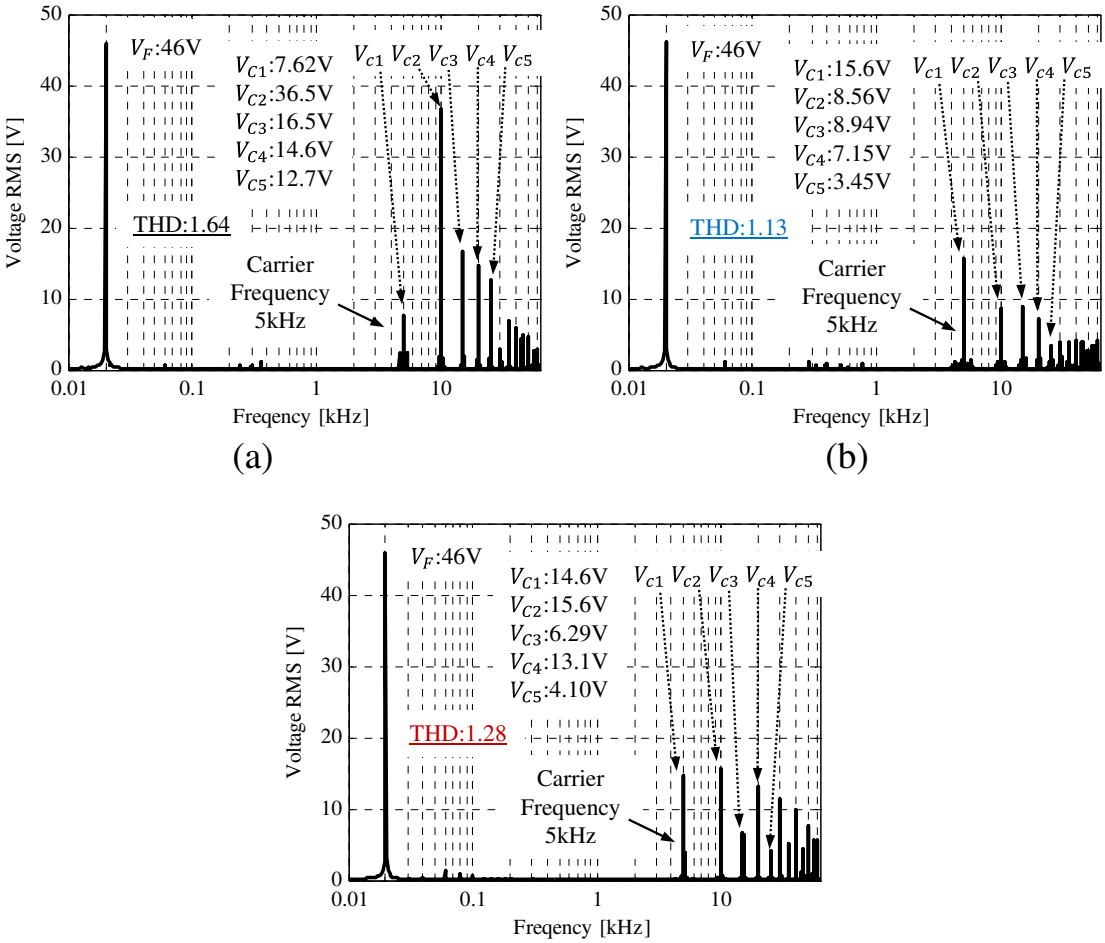

Fig. 3.13. Harmonic analysis of the voltage waveforms when using (a) single-inverter operation, (b) dual inverter with proposed operation, and (c) dual inverter with conventional operation at a speed of 600 rpm a torque of 0.5 Nm.

3.4.4 Voltage THD Characteristics

Experiments are conducted on the proposed method and the conventional method when the torque and speed are changed. Fig. 3.14 and Fig. 3.15 show the characteristics of the phase angle difference α and the DC voltage ratio V_{dc2}/V_{dc1} in the case of the proposed method. The phase angle difference characteristics indicate the phase angle difference increases with motor speed and torque. In contrast, the DC voltage ratio decreases with increasing motor speed, and torque dependence is low. The reason is that as the torque increases, the power factor angle decreases, which is offset by the increase in phase angle difference.

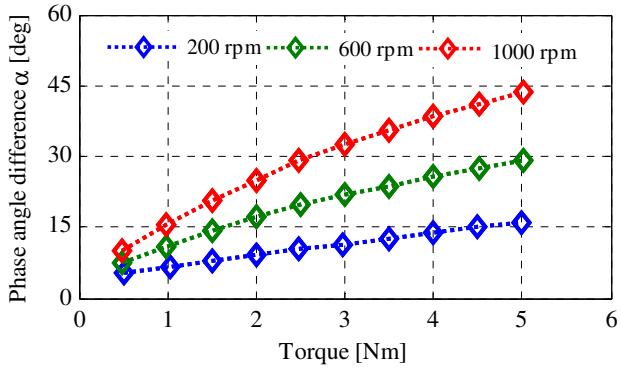

Fig. 3.14. Characteristics of the phase angle difference for the different speed and torque.

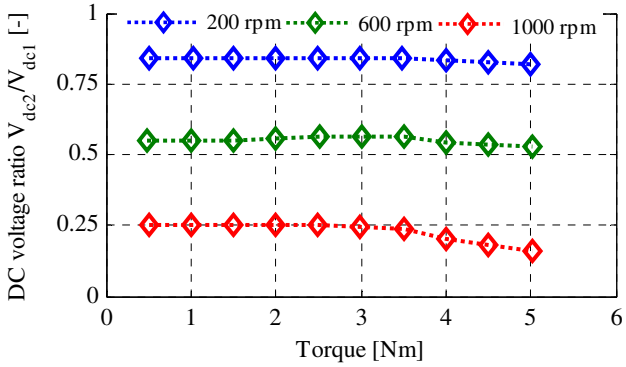

Fig. 3.15. Characteristics of the DC voltage ratio for the different speed and torque

Fig. 3.16 shows the THD characteristics when the motor is driven at a speed of (a) 200 rpm, (b) 600 rpm, and (c) 1000 rpm. Here, “Prop.”, “Conv.”, and “Single” mean the proposed operation, the conventional operation, and the single operation, respectively. Calculation and experimental results show that the voltage THD reduction is verified by the proposed method in the low-torque condition. In the high torque regions, THD of the proposed method is almost the same as the single-inverter operation. In the results of the conventional operation, the THD becomes relatively large as the speed increases (see Fig. 3.16(c)). Generally, the power factor angle increases in the high-speed region; thus the FC voltage increases in the conventional operation because phase angle difference α is assigned at 90 deg. This is the cause of the increase in THD in the conventional operation.

Since the theoretical value of voltage THD shown in Fig. 3.16 are calculated according to (3.7), all harmonic components except the fundamental component are taken into account. Therefore, it is considered that the effect of reducing voltage THD when using the proposed method does not change even if the calculation order of THD is changed. Here, the difference between the theoretical and experimental results is affected by dead-time and turn-on and turn-off time of switching devices, because the theoretical calculation assumes an ideal PWM waveform.

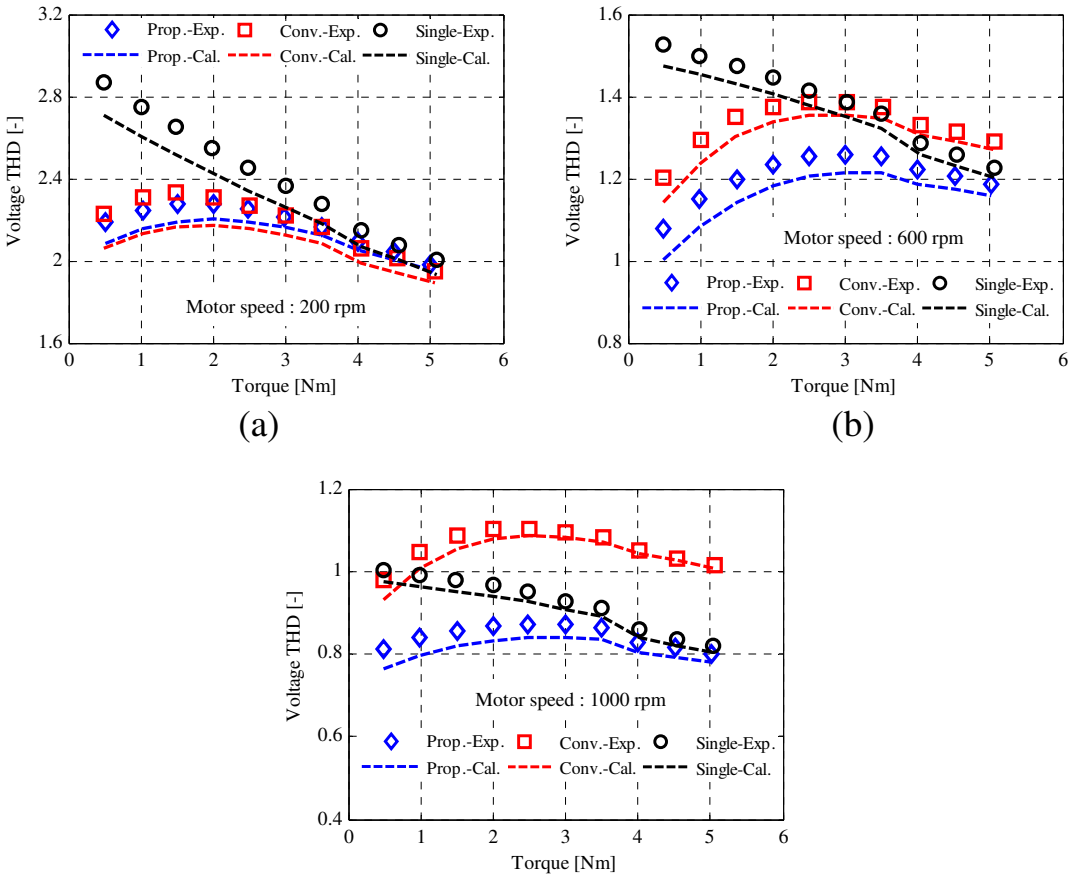

Fig. 3.16. Voltage THD characteristics for different torque when the motor is driven at a speed of (a) 200 rpm, (b) 600 rpm, and (c) 1000 rpm.

3.4.5 Motor, Inverter, and total Efficiencies

Motor efficiency is measured to confirm the improvement effect of the voltage THD reduction. In order to compare the efficiencies under various load conditions, the experiments are conducted by changing the speed from 150 rpm to 1050 rpm and the torque from 0.5 Nm to 5 Nm. Fig. 3.17(a), (b), and (c) shows the results of motor efficiency when using the single inverter operation, the dual inverter with proposed operation, and the dual inverter with conventional operation, respectively. Here, the color bar in (b) and (c) indicates the percentage relative to (a) in order to clarify the improvement effect. From these results, it is confirmed that the motor efficiency is improved under the condition that the voltage THD is reduced. In particular, at a torque of 0.5 Nm (0.1 p.u.) region, motor efficiency is improved by approximately 3% compared with single-inverter operation (see Fig. 3.17(b)). In contrast, the effect of improving motor efficiency is confirmed even when compared with the conventional operation (see Fig. 3.17(c)). In the conventional operation, the voltage THD increases as the speed increases (see Fig. 16), which causes decreasing the motor efficiency.

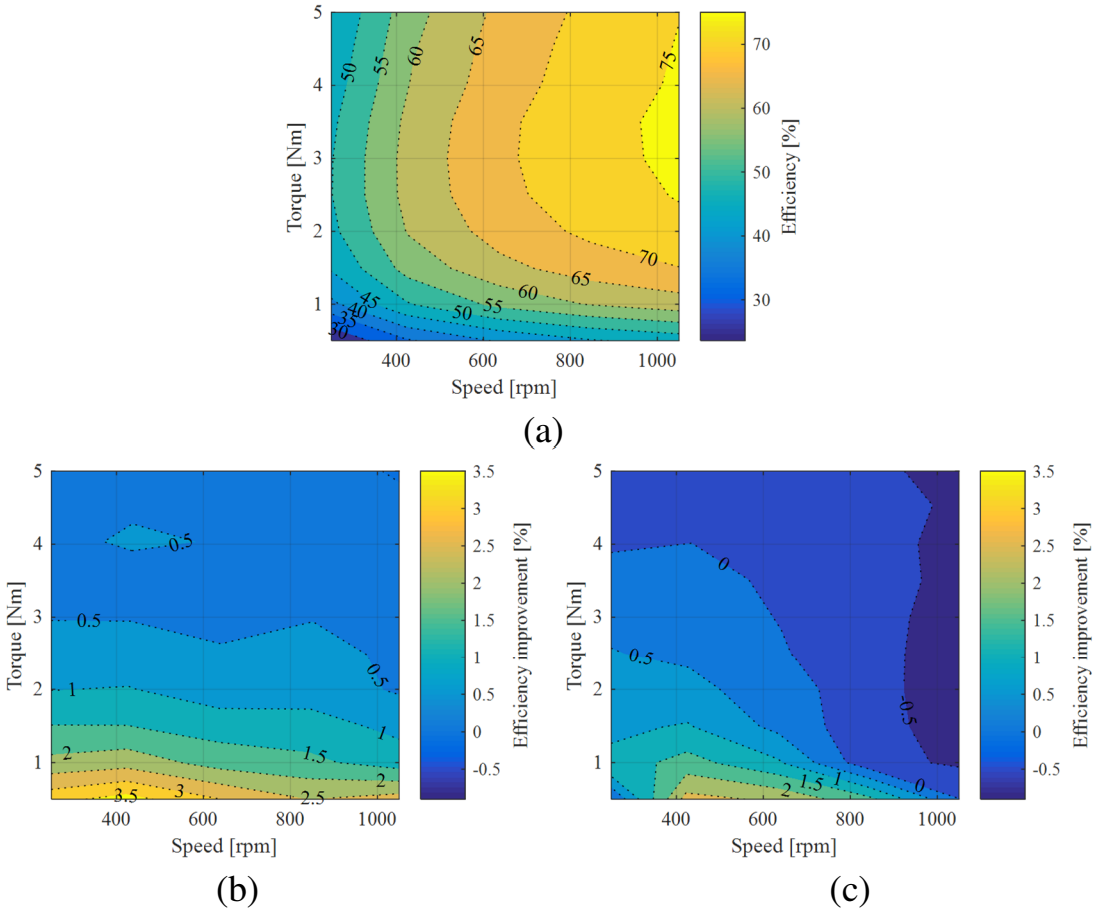

Fig. 3.17. Motor efficiency characteristics for different torque and speed when using (a) single-inverter operation, (b) dual inverter with proposed operation, and (c) dual inverter with conventional operation. The color bar in (b) and (c) indicates the percentage relative to (a).

Characteristics of the inverter efficiency and the total efficiency, which includes the inverter efficiency and the motor efficiency, are experimentally obtained as shown in Fig. 3.18 and Fig. 3.19. Here, the color bar in (b) and (c) indicates in % relative to (a) as well as Fig. 3.17. The results of the inverter efficiency (Fig. 3.18) show that a high-efficiency is achieved when using the single-inverter than other operations in all regions, due to the number of switching devices is doubled in the dual inverter operation. Compared with the conventional operation, the inverter efficiency is lower in the low-speed region, because V_{dc2} increases in the low-speed region as shown in Fig. 3.15. However, the inverter efficiency exceeds about 90 % even when using dual inverter; hence, the efficiency of the total system including the inverter efficiency and the motor efficiency is dominated by the motor efficiency. Finally, the results of the total efficiency (Fig. 3.19) indicate that the proposed method improved the total efficiency at the low-torque and high-speed condition. In particular, at a torque of 0.5 Nm and a speed of 1000 rpm, total efficiency is improved by approximately 2.0% compared with the singl -inverter (see Fig. 3.19 (b) and (c)).

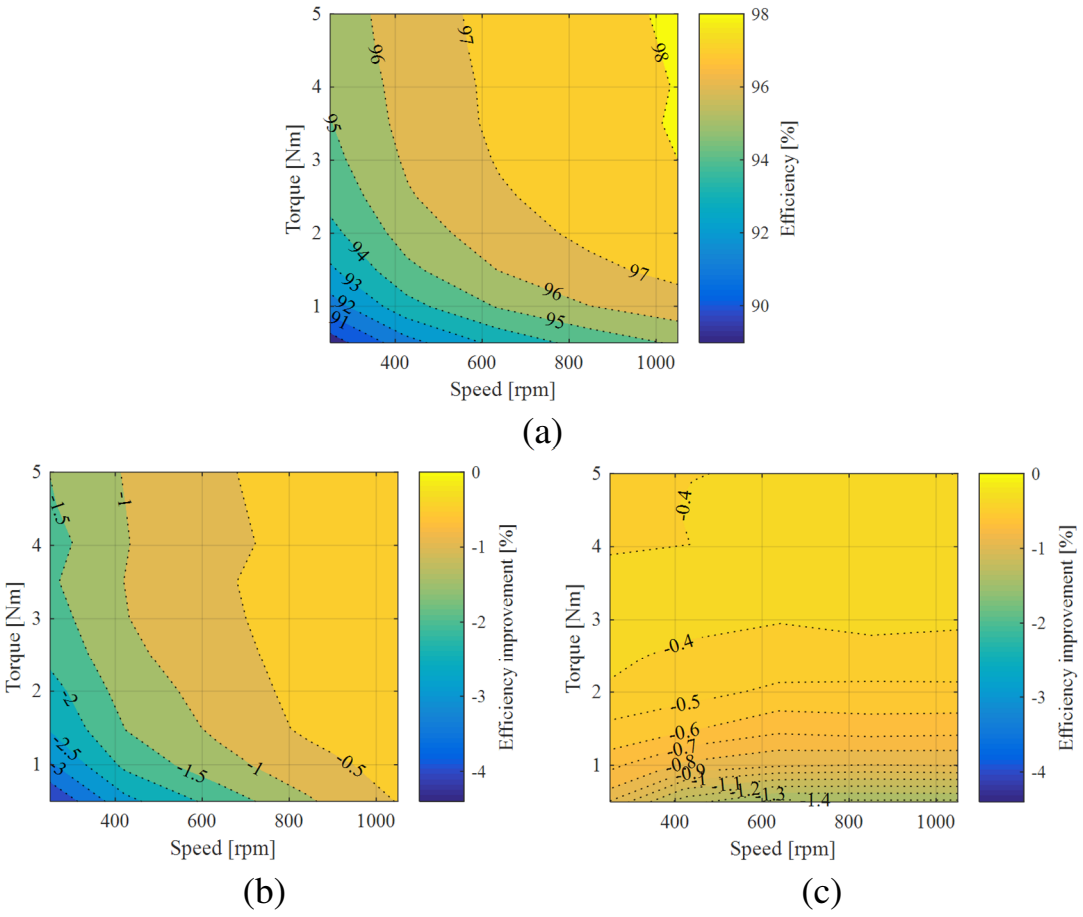

Fig. 3.18. Inverter efficiency characteristics for different torque and speed when using (a) single-inverter operation, (b) dual inverter with proposed operation, and (c) dual inverter with conventional operation. The color bar in (b) and (c) indicates the percentage relative to (a).

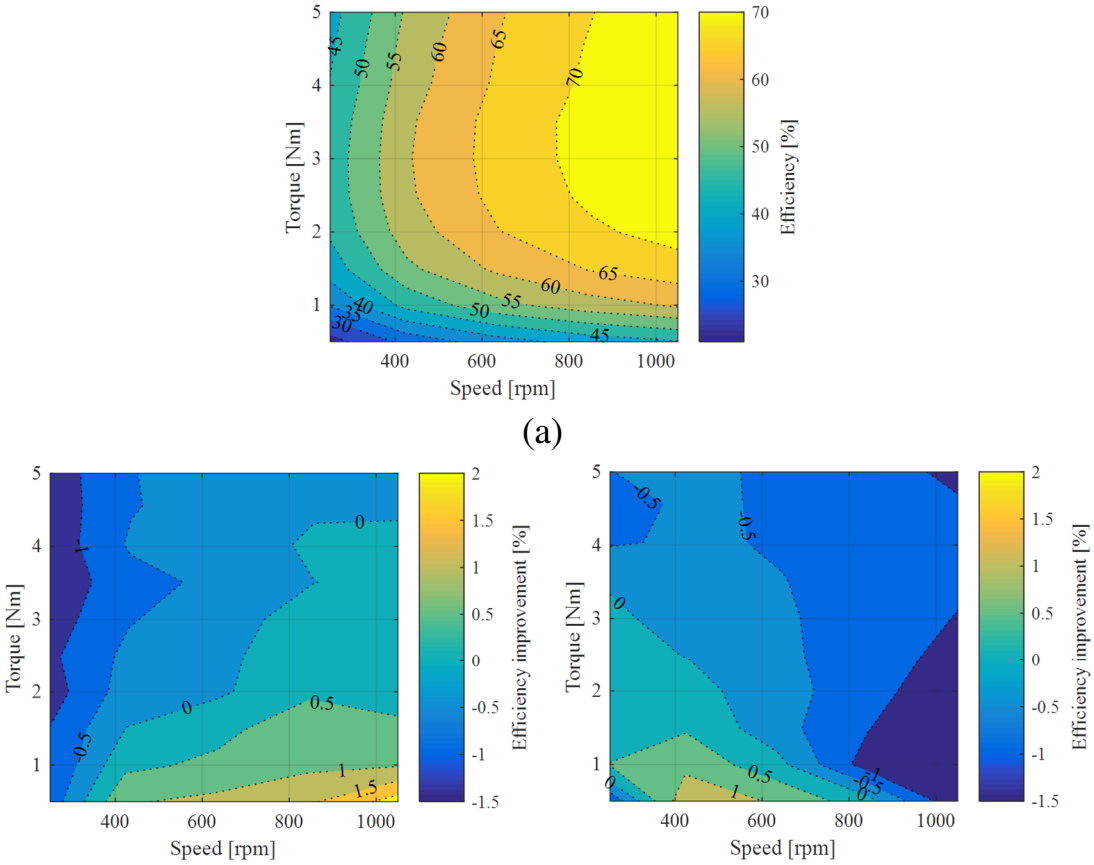

Fig. 3.19. Total efficiency characteristics for different torque and speed when using (a) single-inverter operation, (b) dual inverter with proposed operation, and (c) dual inverter with conventional operation. The color bar in (b) and (c) indicates the percentage relative to (a).

3.5 Conclusion

In this study, a motor and inverter condition, that allows to reduce the THD of the phase voltage of stator winding, when the induction motor driven by the dual inverter and the single-inverter with SPWM was theoretically described. Furthermore, a control strategy for improving the voltage THD in the low-torque region was proposed. The performance of the proposed operation was demonstrated by experiment using an open-end winding induction motor. The experimental results show the effectiveness of the proposed method due to: the proposed method reduced the voltage THD by 15 pp and 51 pp, thereby the total efficiency was improved by 1.0 pp and 1.5 pp compared with the single-inverter and the conventional dual inverter operation, respectively.

By the dual inverter topology, it is possible to improve the performance in the high-load region. In contrast, high efficiency is required in the light-load region, the proposed method contributes to energy-saving in the low-torque region without changing the circuit configuration.

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Chapter 4

Harmonic Analysis of Output Voltage with Typical PWM Strategies

4.1 Introduction

Through previous study, it has been confirmed that the voltage harmonics due to PWM switching can be reduced by keeping modulation indices of both inverters at maximum value and regulating the FC voltage at minimum. However, in the dual inverter with decoupled modulation strategy, there are few studies to PWM each of the two inverters. In particular, modulation methods for reducing the harmonics of the output voltage depending on the load conditions are not investigated. In this study, a theoretical analysis of output voltage harmonics when using various PWM methods are introduced. Here, sinusoidal PWM (SPWM), third harmonic injection PWM (THIPWM), and discontinuous PWM (DPWM) are used as conventional carrier-based modulation, and space vector modulation (SVPWM) and near-state PWM (NSPWM) [4-1] with a reduced number of commutations are used as proposed modulation. Originality of this study is to analyze the output voltage harmonics that change not only with the fundamental voltage but also with the power factor angle when typical PWM methods are applied to the dual inverter. Through analysis, this study clarifies the modulation method that minimizes the harmonic components depending on the operating conditions

of open-end winding IM. Since voltage harmonics are one of the cause of motor losses [4-2], [4-3], the efficiency of the motor drive system can be improved by selecting a modulation method that can reduce the harmonics in the light-load condition. Furthermore, there is almost no change in the low-order components due to these modulation methods shown in this study. Therefore, this study does not mention low-order harmonics.

This chapter is organized as follows: firstly, the configuration of the dual inverter fed open-end winding induction motor (IM) drive system and basis of the FC topology are introduced; secondly, principle of voltage harmonics, which are related to fundamental voltage and power factor angle is theoretically analyzed; finally, the experimental validation, which demonstrates the reduction of voltage harmonics and effectiveness of the voltage THD reduction by proposed modulation is carried out.

4.2 Theoretical Analysis of the Voltage Harmonics

4.2.1 Voltage Vectors and Levels Identification

As described in Chapter 2, the resulting vectors in the dual inverter $\boldsymbol{V_{xy}}$ (represented as (2.7)) are defined and can be drawn as the hexagon by INV. 2 around vectors on the hexagon by INV. 1. The magnitudes of the resulting vector changes depending on the voltage ratio $G_{dc} = V_{dc2}{:}V_{dc1}$. For instance, the resulting vector diagrams for $G_{dc} = 2{:}3$ and $G_{dc} = 1{:}3$ are shown in Fig. 4.1. Combined voltage space vectors with different DC-link voltage ratios (a) $G_{dc} = 2{:}3$ and (b) $G_{dc} = 1{:}3$.(a) and (b), respectively. Voltage vectors are categorized into seven types according to their amplitude as follows:

$$V_A = \frac{2}{3} V_{dc1}(1 - G_{dc}) \cdots\cdots \quad (4.1a)$$

$$V_B = \frac{2}{3} V_{dc1} G_{dc} \cdots\cdots \quad (4.1b)$$

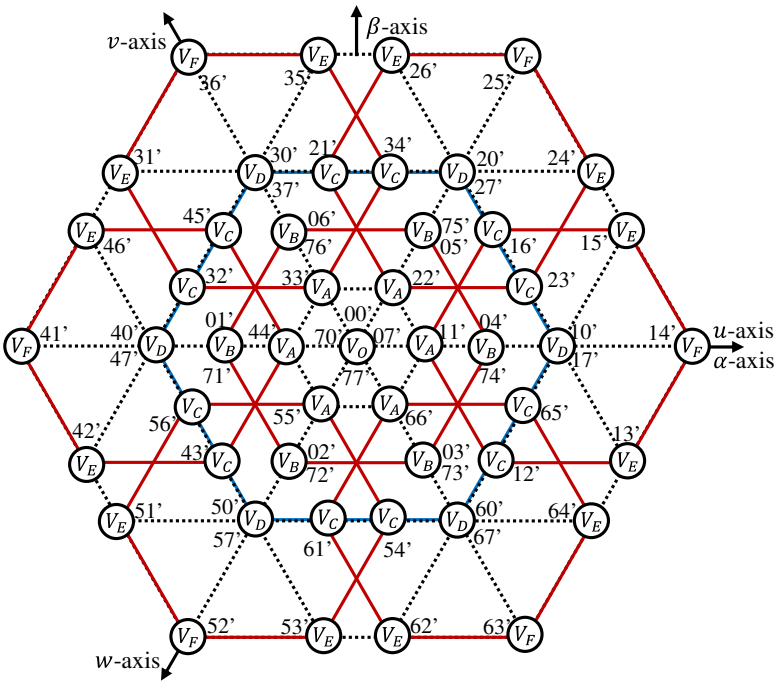
$$V_C = \frac{2}{3} V_{dc1} \sqrt{1 - G_{dc} + G_{dc}^2} \cdots\cdots \quad (4.1c)$$

$$V_D = \frac{2}{3} V_{dc1} \cdots\cdots \quad (4.1d)$$

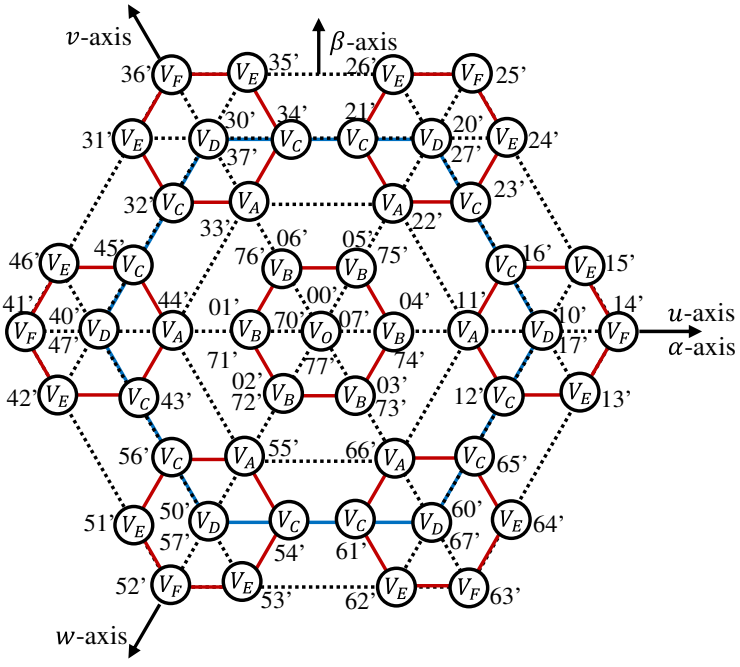
$$V_E = \frac{2}{3} V_{dc1} \sqrt{1 + G_{dc} + G_{dc}^2} \cdots\cdots \quad (4.1e)$$

$$V_F = \frac{2}{3} V_{dc1}(1 + G_{dc}) \cdots\cdots \quad (4.1f)$$

$$V_O = 0 \cdots\cdots \quad (4.1a)$$



(a)



(b)

Fig. 4.1. Combined voltage space vectors with different DC-link voltage ratios (a) $G_{dc} = 2:3$ and (b) $G_{dc} = 1:3$.

By the proposed control strategy introduced in Chapter 3, which achieves reducing the output voltage harmonics by maximize G_{dc} and minimize phase angle difference α, G_{dc} depends on the load conditions (fundamental voltage V_{fun} and power factor angle δ), according to following equations The magnitudes of each vector V_A to V_O with different fundamental voltage V_{fun} at power factor angle of 45 deg are shown in Fig. 4.2, where phase angle difference α is calculated by (2.18) and modulation indices are set at $M_1 = M_2 = 1.15$. Here, the vertical and horizontal axes are normalized by the maximum fundamental voltage ($V_{dc1}/2$), which value indicates the fundamental voltage at the maximum modulation index ($M_1 = 1$) that can be linearly modulated with SPWM. From Fig. 4.2, in proportion to V_{fun}, V_A tends to increase and V_B, V_E, and V_F tend to decrease; it indicates that, by increasing the output time of V_A compared with other vectors, it is possible to reduce the harmonics with respect to the voltage reference vector.

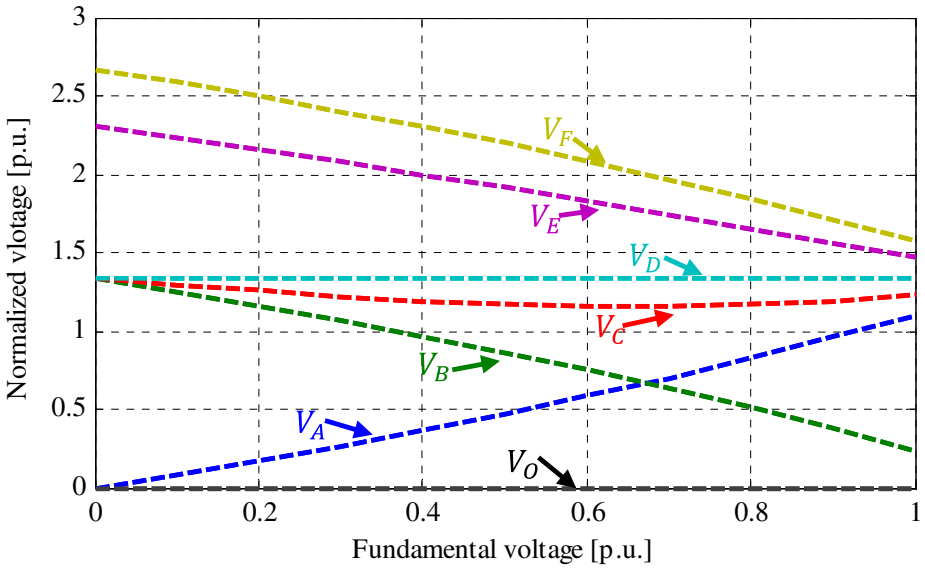


Fig. 4.2. Normalized magnitudes of voltage vectors V_A to V_O with different fundamental voltage V_{fun} at power factor angle $\delta = 45\text{deg}$ when using the proposed control.

4.2.2 Voltage References of Various PWM Strategies

Many three-phase VSI modulation methods have been studied in terms of voltage utilization and input and output harmonics. In reference [4-4], the output voltage harmonics and input current harmonics in each common-mode voltage reduction method are evaluated in the single inverter topology. It has been reported that the larger the modulation index, the smaller the output voltage harmonics. In this study, the output voltage harmonics when the modulation methods (THIPWM, DPWM, SVPWM, and NSPWM) that can maximize the voltage utilization is applied to the dual inverter system is evaluated.

The three-phase voltage references, in the case of SPWM strategy, are expressed by modulation index M and electrical angle θ as follows:

$$\begin{cases} d_{u-SPWM} = M\cos(\theta) \\ d_{v-SPWM} = M\cos\left(\theta - \frac{2}{3}\pi\right) \\ d_{w-SPWM} = M\cos\left(\theta + \frac{2}{3}\pi\right) \end{cases} \cdots\cdots\cdots\cdots \quad (4.2)$$

where θ is taken as the corresponding electrical angle when the rotor rotates. The methods of injecting zero-sequence component are well known as a method of expanding the modulation index keeping linearity, such as THIPWM and DPWM [4-5]. The three-phase voltage references of THIPWM and DPWM are given by injecting the zero-sequence component d_z into the sinusoidal references as:

$$d_{x-THIPWM} = d_{x-SPWM} - d_{z-THIPWM}, (x = u, v, w) \cdots\cdots \quad (4.3a)$$

$$d_{z-THIPWM} = \frac{1}{6}M\cos(3\theta) \cdots\cdots\cdots\cdots \quad (4.3b)$$

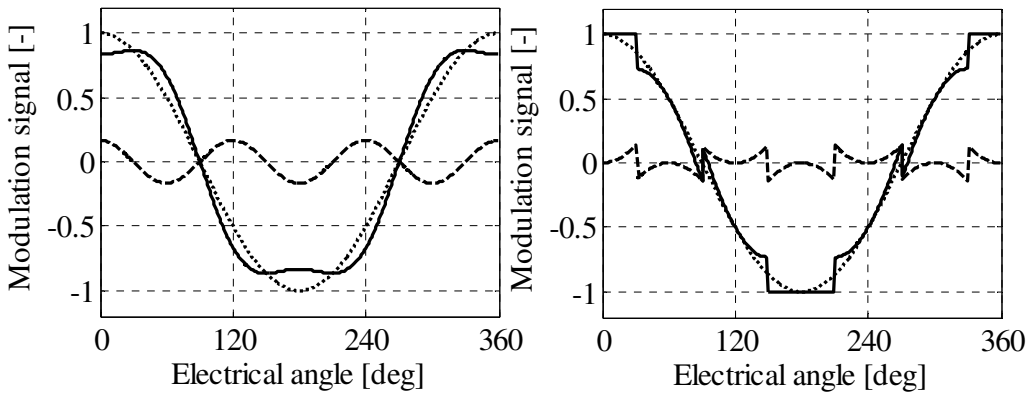
$$d_{x-DPWM} = d_{x-SPWM} + d_{z-DPWM}, (x = u, v, w) \cdots\cdots \quad (4.4a)$$

$$\begin{cases} d_{z-DPWM} = 1 - |d_{max}|, & \text{if } |d_{max}| > |d_{min}| \\ d_{z-DPWM} = -1 + |d_{min}|, & \text{if } |d_{max}| < |d_{min}| \end{cases} \quad \text{..... (4.4b)}$$

$$\begin{cases} d_{max} = \max(d_{u-SPWM}, d_{v-SPWM}, d_{w-SPWM}) \\ d_{min} = \min(d_{u-SPWM}, d_{v-SPWM}, d_{w-SPWM}) \end{cases} \quad \text{..... (4.4c)}$$

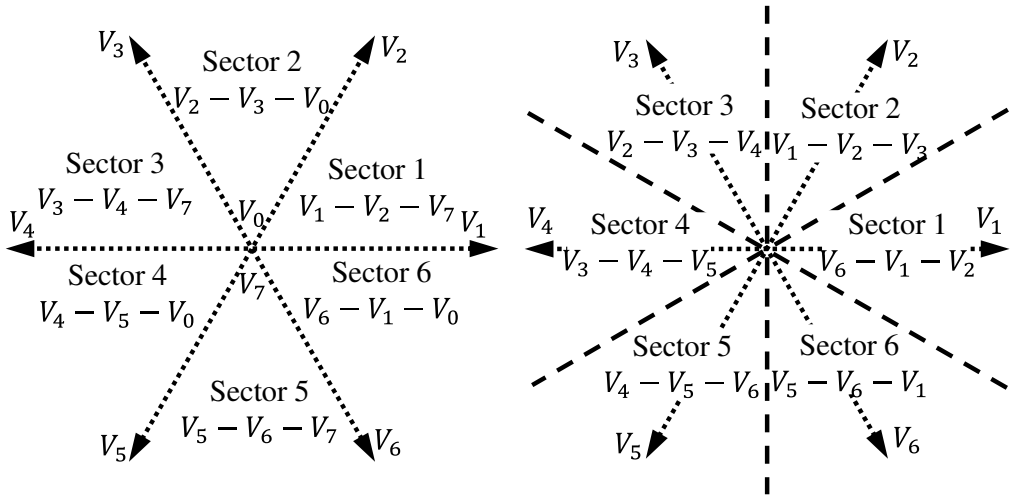
The U-phase voltage references d_u and zero-sequence component d_z of THIPWM and DPWM when the modulation index $M = 1$ are shown in Fig. 4.3(a) and (b), respectively. The switching states are directly obtained by comparing these voltage references and the carrier waveform (triangle waveform is used in this study).

In contrast, for the various purposes (e.g. reducing common-mode voltage and input current harmonics), a method of achieving a voltage reference vector by three voltage vectors and their output times has been proposed [4-1]. In this study, SVPWM and NSPWM are used in which each inverter can output the maximum voltage ($M = 2/\sqrt{3}$). Voltage sector definitions and output vector patterns of SVPWM and NSPWM are shown in Fig. 4.4. The normalized duty cycles of SVPWM, per switching period T_s for vectors of $V_i, V_{i+1}, V_{0,7}$ at sector i, are defined as:



(a) (b)

Fig. 4.3. Modulation signals of (a) THIPWM and (b) DPWM ($M = 1$).



(a) (b)

Fig. 4.4. Voltage sector definitions and output vector patterns of (a) SVPWM and (b) NSPWM.

$$\begin{cases} d_{i-SVPWM} = \dfrac{\sqrt{3}}{2} M \cos\left(\theta' + \dfrac{\pi}{6}\right) \\ d_{i+1-SVPWM} = \dfrac{\sqrt{3}}{2} M \sin(\theta') \\ d_{0,7-SVPWM} = 1 - \dfrac{\sqrt{3}}{2} M \cos\left(\theta' - \dfrac{\pi}{6}\right) \\ \text{where } 0 < \theta' < \dfrac{\pi}{3} \end{cases}, \cdots\cdots\cdots\cdots \quad (4.5a)$$

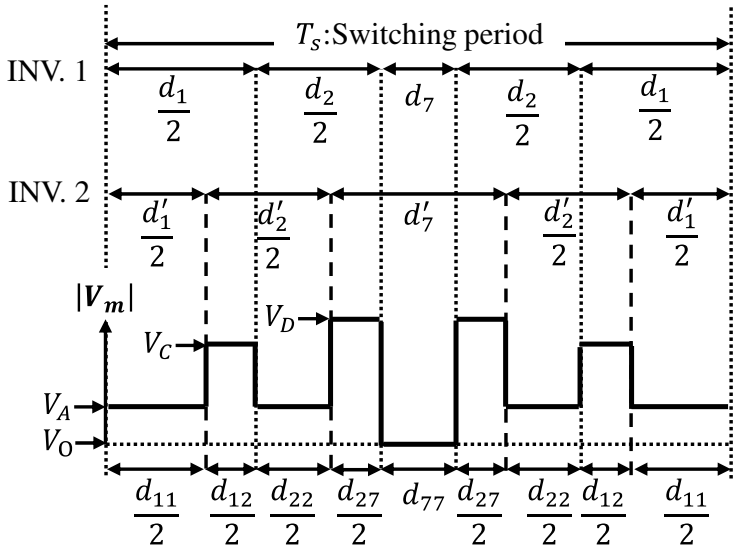
$$\theta' = \theta - \frac{(i-1)\pi}{3}, (i = 1,2,3,4,5,6) \cdots\cdots\cdots\cdots \quad (4.5b)$$

Similarly, the normalized duty cycles of NSPWM, per switching period T_s for vectors of V_{i-1}, V_i, V_{i+1} at sector i, are defined as:

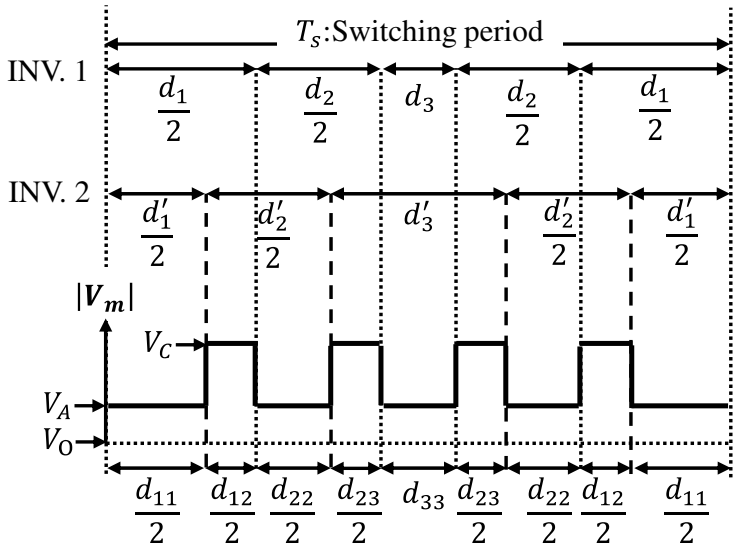
$$\begin{cases} d_{i-1-NSPWM} = 1 - \dfrac{\sqrt{3}}{2} M \cos\left(\theta' - \dfrac{\pi}{6}\right) \\ d_{i-NSPWM} = \dfrac{3}{2} M \cos(\theta') - 1 \\ d_{i+1-NSPWM} = 1 - \dfrac{\sqrt{3}}{2} M \cos\left(\theta' + \dfrac{\pi}{6}\right) \end{cases}, \cdots\cdots \quad (4.6a)$$

$$\theta' = \theta - \frac{(i-1)\pi}{3}, (i = 1,2,3,4,5,6) \cdots\cdots \quad (4.6b)$$

In this study, each vector is output in the switching pattern shown in Fig. 4.5 in order to reduce the number of commutations in a switching period in the case of SVPWM and NSPWM.



(a)



(b)

Fig. 4.5. Per-switching period view of each inverter states and output voltage by (a) SVPWM and (b) NSPWM.

4.3 Analytical Evaluations

4.3.1 Output Times of each Vector in Dual Inverter

As described in Chapter 2, the output time of the voltage vector categorized into 7 types V_A to V_O can be calculated as follows:

$$d_K(\theta) = \sum_x \sum_y d_{xy}(\theta) \quad \cdots\cdots (4.7)$$

Here, subscript $K = A, B, C, D, E, F, O$, and the output time d_{xy} of each vector, which normalized by a switching period T_s, is determined by the relation between voltage references of INV. 1, and INV. 2 defined as (4.2)-(4.6a). The characteristics of d_K, which change depending on the electrical angle θ according to (4.7), are shown in Fig. 4.6. Here, the fundamental voltage V_{fun} and the power factor angle δ are set to 0.67 and 45 deg, respectively. From the results, the following features are confirmed: In the four modulation methods, d_A is larger than the others, d_C is the second largest, and d_F is always zero. d_E is zero in SVPWM and NSPWM, which leads to a reduction in the maximum voltage level compared to THIPWM and DPWM. In NSPWM, the change in voltage level is reduced because the values other than d_A and d_C are zero.

d_K changes not only with the electric angle θ but also with the fundamental voltage V_{fun} and the power factor angle δ. Fig. 4.7 shows the average value of the output time D_K in a fundamental period T, according to (4.8).

$$D_K(V_{fun}, \delta) = \frac{1}{2\pi} \int_0^{2\pi} d_K(\theta)\, d\theta \quad \cdots\cdots (4.8)$$

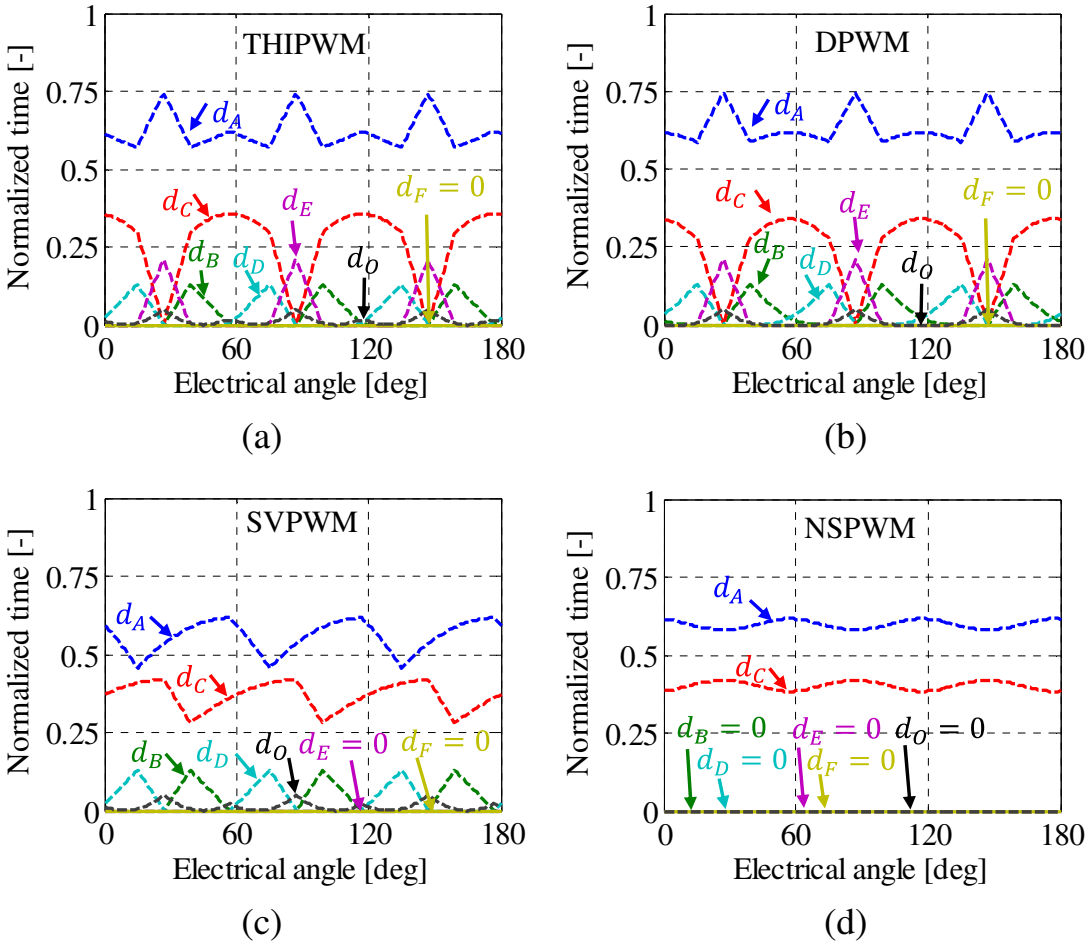


Fig. 4.6. Angle dependencies of the normalized output times ($V_{fun} = 0.67$ p.u., $\delta = 45$ deg).

Here, the horizontal axis indicates the fundamental component of the output voltage, and the vertical axis is normalized by a fundamental period. From Fig. 4.7, it can be seen that D_A and D_C are dominant because D_B, D_D, D_E, and D_O are smaller than D_A and D_C. In Fig. 4.7(a), D_A decreases as V_{fun} increases, and D_A is the largest in NSPWM at low V_{fun}. In contrast, at high V_{fun}, D_A is large in DPWM and THIPWM. In Fig. 4.7(c), D_C increases as the voltage increases, and D_C is relatively larger in the case of NSPWM and SVPWM.

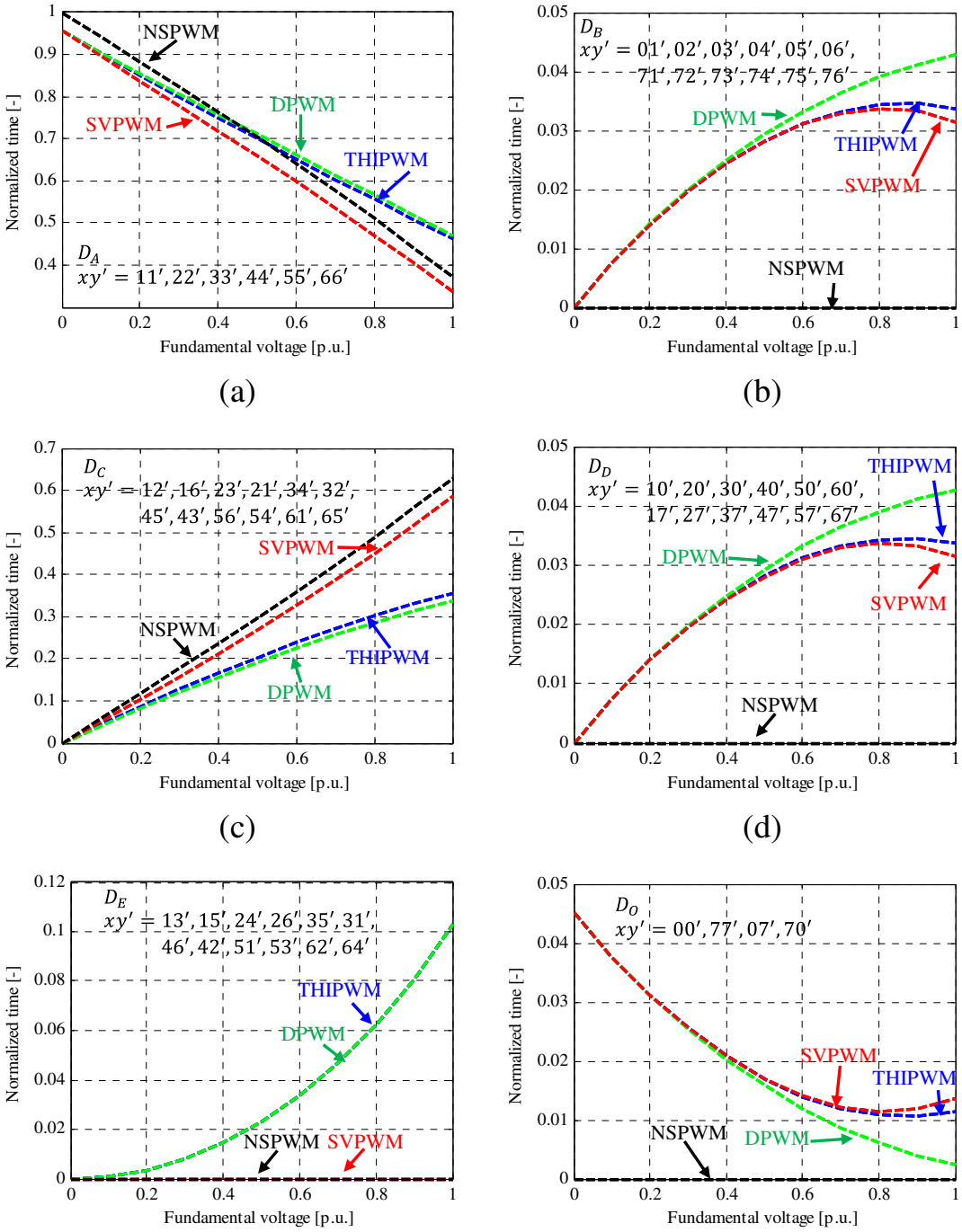


Fig. 4.7. Normalized output times of voltage vectors (a) V_A, (b) V_B, (c) V_C, (d) V_D, (e) V_E, and (f) V_O when different fundamental voltage V_{fun} and power factor angle δ is 45 deg

4.3.2 Harmonic Voltage in Per-Switching Period

In the above section, the output time of each vector in various modulation methods is described. The harmonic voltage V_{hn} applied to the motor winding are expressed as:

$$V_{hn}(\theta) = \frac{\sqrt{V_{RMS-SW}^2(\theta) - V_{m-ref}^2(\theta)}}{V_{fun}} \quad \text{(4.9)}$$

Here, output voltage RMS in per-switching period V_{RMS-SW} is calculated by the sum of all combinations of the product of V_{xy}^2 and $d_{xy}(\theta)$ as:

$$V_{RMS-SW}(\theta) = \sqrt{\sum_{x=0}^{7}\sum_{y=0}^{7} V_{xy}^2 d_{xy}(\theta)} \quad \text{(4.10)}$$

In addition, the output voltage reference V_{m-ref} is defined in (4.11) as a three-phase voltage having a fundamental amplitude of V_{fun}.

$$\boldsymbol{V_{m-ref}} = \begin{bmatrix} v_{um-ref} \\ v_{vm-ref} \\ v_{wm-ref} \end{bmatrix} = V_{fun} \begin{bmatrix} \cos(\theta) \\ \cos\left(\theta - \frac{2}{3}\pi\right) \\ \cos\left(\theta + \frac{2}{3}\pi\right) \end{bmatrix} \quad \text{(4.11)}$$

Fig. 4.8 shows the harmonic voltage characteristics (according to (4.9)) when the four modulation methods (THIPWM, DPWM, SVPWM, NSPWM) are used. As described in Section 4.2, the magnitude of each voltage vector changes depending on the fundamental voltage V_{fun} and power factor angle δ, thus the characteristics are calculated by changing V_{fun}. The vertical axis indicates the harmonic voltage V_{hn}, and the horizontal axis indicates the electric angle θ. From this result, it can be seen that THIPWM and DPWM have almost the same characteristics even if V_{fun} is changed. This is because the output time characteristics shown in Fig. 4.6 and Fig. 4.7

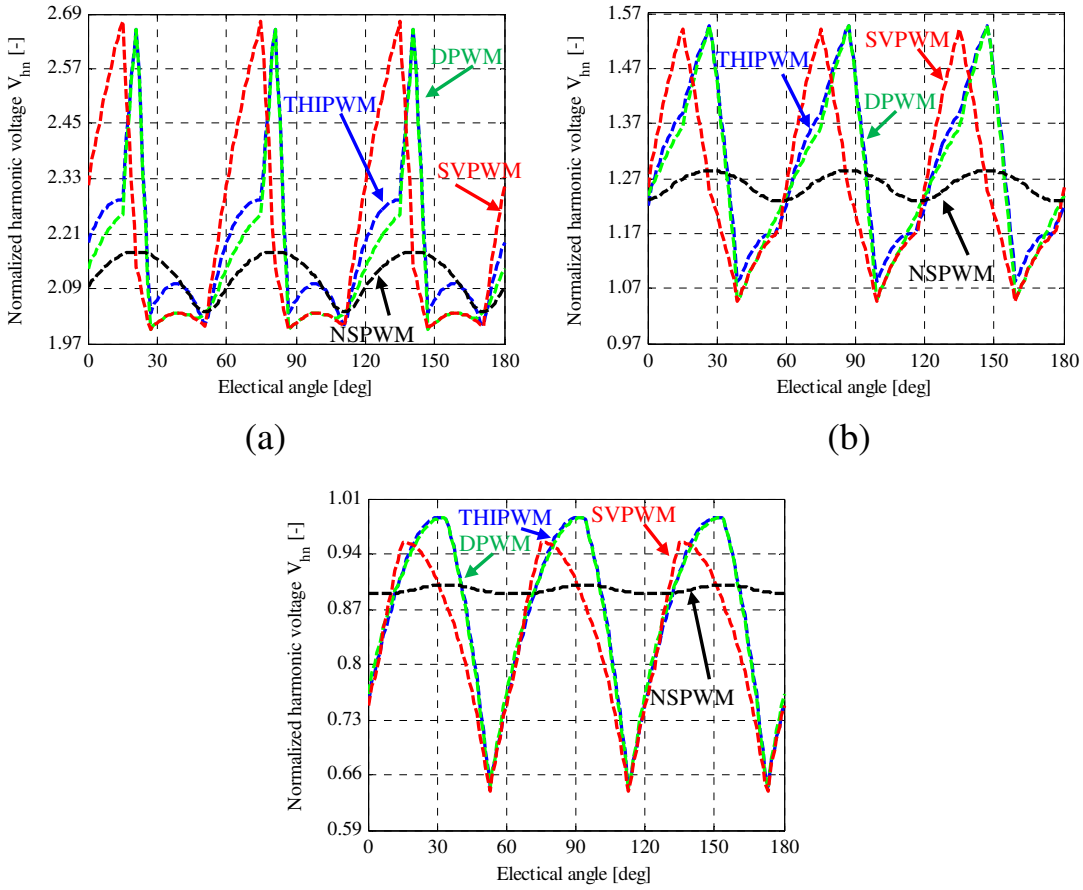


Fig. 4.8. Normalized harmonic voltage – angle characteristics at power factor angle of 45 deg with (a) $V_{fun} = 0.33$ p.u., (b) $V_{fun} = 0.67$ p.u., and (c) $V_{fun} = 1.0$ p.u.

are almost the same. When V_{fun} is 0.33 p.u., the peak of V_{hn} is the largest in SVPWM and the smallest in NSPWM (see Fig. 4.8(a)). In contrast, when V_{fun} is 1.0 p.u., the average value is the smallest in SVPWM and the largest in NSPWM (see Fig. 4.8(c)).

4.3.3 Characteristics of Voltage THD

In the previous section, the calculation of the harmonic voltage in per-switching period is compared. In this section, the voltage harmonics that

change depending on the fundamental voltage V_{fun} and the power factor angle δ are evaluated using total-harmonic-distortion (THD). Since THD is given by calculating the difference between the RMS value including all harmonics and the fundamental component, thus THD is obtained by calculating the RMS of the harmonic voltage V_{hn} (expressed in (4.9)) as follows:

$$THD(V_{fun}, \delta) = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_{hn}^2(\theta)d\theta} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (4.12)$$

In this study, in order to evaluate the voltage THD reduction for each modulation method, comparisons are carried out with the THD calculation result when SPWM is used. Fig. 4.9 shows the numerical calculation results of the output voltage THD in a fundamental period, according to (4.12), when the fundamental voltage V_{fun} and power factor angle δ are changed. Here, the color bars in Fig. 4.9(b)-(e) show the reduction rate (in %) based on the calculation results in SPWM. By SPWM, the voltage THD reduction compared with the single inverter operation has been confirmed, in the region where δ is large and V_{fun} is small, which result is reported in Chapter 3. The following features is confirmed from the THD calculation results: THD is reduced compared to SPWM in all areas. In THIPWM, DPWM, and SVPWM, THD is reduced by about 20% in the region of high voltage ($V_{fun} = 1$ p. u.) and high power factor angle ($\delta = 75$ deg) (see Fig. 4.9 (b), (c) and (d)). In SVPWM and NSPWM, the THD is most reduced at high voltage ($V_{fun} = 1$ p. u.) and low power factor angle ($\delta = 75$ deg), and the reduction rates are -22% and -18%, respectively (see Fig. 4.9 (d) and (e)). In NSPWM, the reduction rate is large in the region where V_{fun} and δ are low (see Fig. 4.9 (d) and (e)).

From the numerical calculation results in this chapter, it is confirmed that the load conditions that can reduce the output voltage harmonics differ depending on the modulation method. The validity of the above theoretical calculation is demonstrated by experiments.

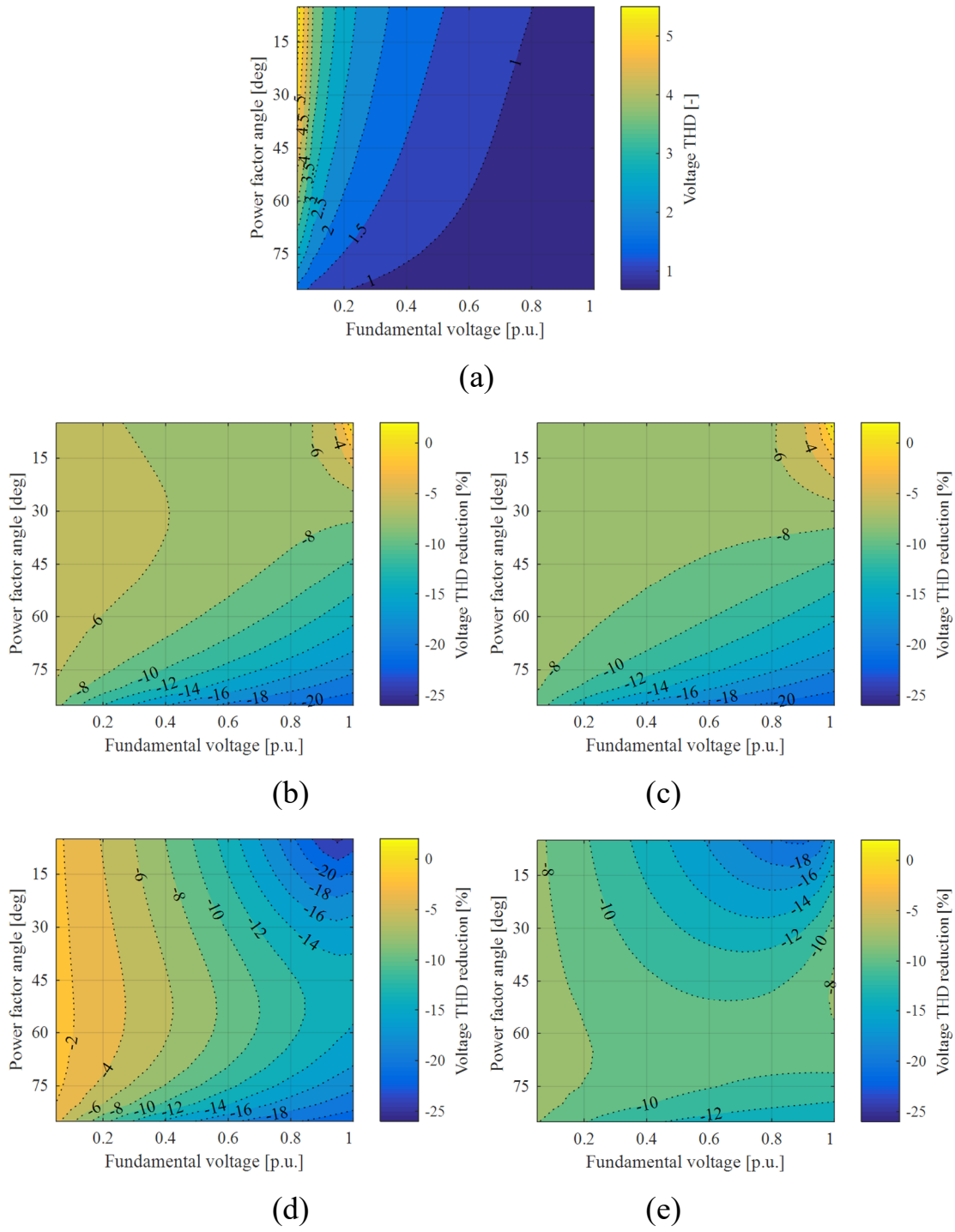


Fig. 4.9. Voltage THD characteristics for different fundamental voltage and power factor angle with (a) SPWM, (b) THIPWM, (c) DPWM, (d) SVPWM, and (e) NSPWM. Note that the color bars in (b)-(e) show the reduction rate (in %) based on the calculation results in (a).

4.4 Experimental Results

4.4.1 Experimental Setup and Conditions

Experiments using a general-purpose induction motor as open-end winding IM are carried out in order to compare the voltage harmonics in each modulation methods. The dual inverter conditions and parameters of the open-end winding IM are shown in Table 4.1 and Table 4.2. In this experiment, a DC power supply regulates the INV. 1 DC voltage at 300 V. The selection of the capacitance of the FC in various dual inverter drive methods is reported in [4-6].

In order to control the torque and speed of the open-end winding IM, which are related to the power factor angle and output voltage, the motor current control and FC voltage control are performed using the control block

Table 4.1. Experimental condition.

INV.1 DC voltage: V_{dc1}	300 V
INV.2 DC voltage: V_{dc2}	According to (2.18)
INV.2 DC capacitance: C_{dc2}	330 uF
Carrier Frequency: F_{c1}	5 kHz
Dead-time: T_{DT}	500 ns

Table 4.2. Parameters of the open-end winding IM.

Rated power	750 W	Poles	4
Rated voltage	200 V	Rated frequency	50 Hz
Rated current	3.5 A	Rated speed	1410 rpm
Leakage inductance	10.5 mH	Rated torque	5.0 Nm
		Stator resistance	2.74 Ω
Mutual inductance	0.195 H	Rotor resistance	2.08 Ω

as shown in Fig. 4.10. Through previous chapters, the output voltage harmonics reduction has been verified by outputting the voltage of the difference between the two inverters with M_1 and M_2 as the maximum. In this control method, the maximum voltage of INV. 2 is output (M_2 is the maximum), and the INV. 1 voltage reference $\boldsymbol{V_{1-ref}}$ is obtained by adding the INV. 2 voltage reference $\boldsymbol{V_{2-ref}}$ to the motor voltage $\boldsymbol{V_{m-ref}}$, which is obtained by the current PI controller. In this study, the modulation part, which converts the voltage references $\boldsymbol{V_{1-ref}}$ and $\boldsymbol{V_{2-ref}}$ into gate signals of each inverter is changed. In this experiment, SVPWM and NSPWM generate gate signals according to the switching table using FPGA, and SPWM, THIPWM, and DPWM generate gate signals by comparing the triangular carrier and the three-phase voltage reference (see Fig. 4.10).

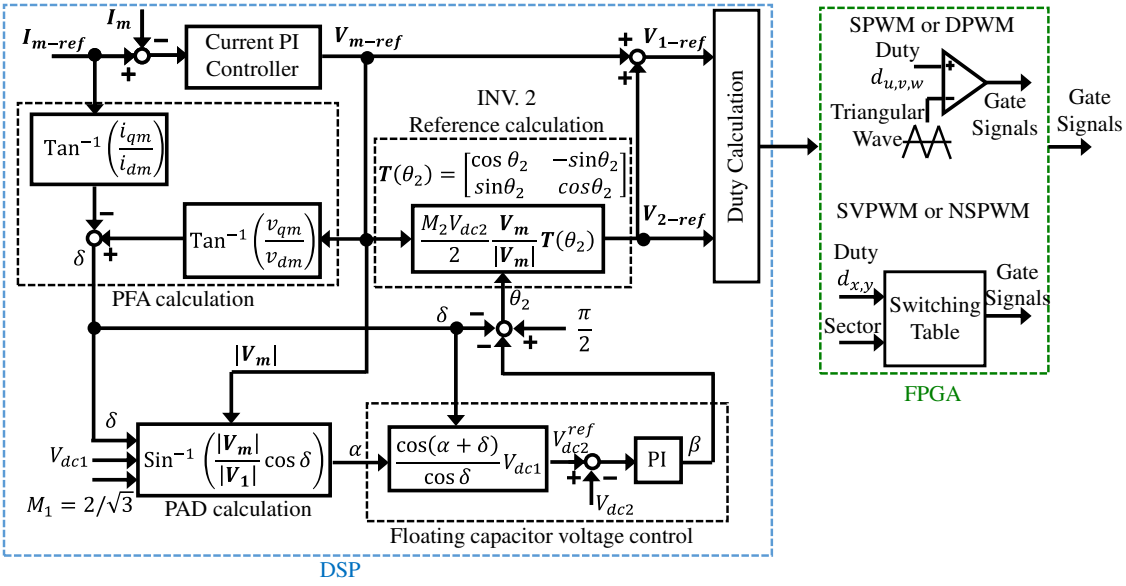


Fig. 4.10. Proposed control system.

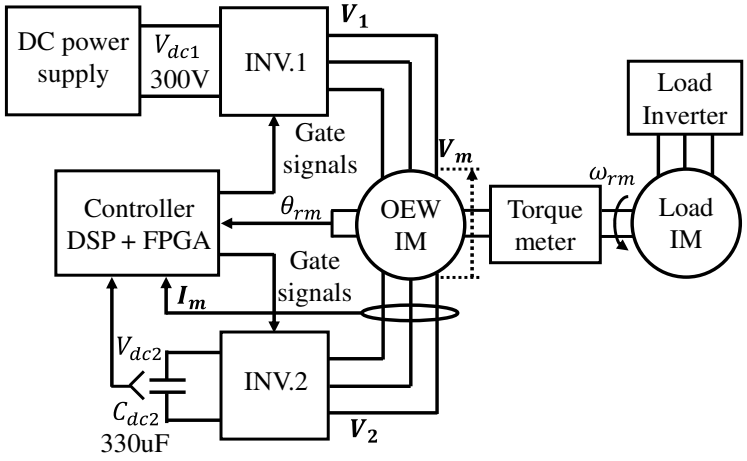


Fig. 4.11. Experimental setup.

Fig. 4.11 shows an experimental setup. The three-phase stator current I_m, the FC voltage V_{dc2} (DC voltage of INV2), and the mechanical angle θ_{rm} of the rotor are measured for control. Here, the slip-frequency-type field-oriented control is used. In order to change the torque in proportion to the q-axis current, the d-axis current is controlled to be constant at 2.0 A. The torque is set from approximately 0.5 Nm to 3.5 Nm (10 % to 70 % of the rated torque) to verify the improvement effect in the light-load condition.

4.4.2 Experimental Waveforms and Harmonic Analysis of the Output Voltage

In this experiment, the steady state performances, in the case of using five modulation methods, are demonstrated, when the motor is driven with a torque of 0.5 Nm and a fundamental frequency F_{fun} of 50 Hz; Under this condition, power factor angle δ of 75 deg and a fundamental voltage V_{fun} of 97.0 V (0.9 p.u.) are obtained.

Fig. 4.12 shows the experimental waveforms of the motor phase voltage v_{um}, phase current i_{um}, FC voltage V_{dc2}, and each inverter voltage references d_{u1} and d_{u2}. Here, the bottom waveform of SVPWM and NSPWM (shown in Fig. 4.12 (d) and (e)) indicates the equivalent output voltage of

each inverter. Since the maximum value of each voltage reference are 1.0 in all modulation methods, it can be confirmed that the proposed control method has been realized (see the bottom of Fig. 4.12). The reason why the FC voltage V_{dc2} (third waveform from the top) is approximately 40 V in (a) SPWM and about 70 V in other cases is because the modulation index is set to 1.00 and 1.15, respectively, and $V_{dc2-ref}$ is determined by (2.19). During the period when the voltage references are constant at 1.0 (which can be seen by (c) DPWM, (d) SVPWM, (e) NSPWM), the change in the phase voltage level is small, hence the switching ripple in the current waveform is reduced. In particular, the voltage waveform in NSPWM has less change in voltage level than other methods (which can be seen in Fig. 4.7 in Section 3.2).

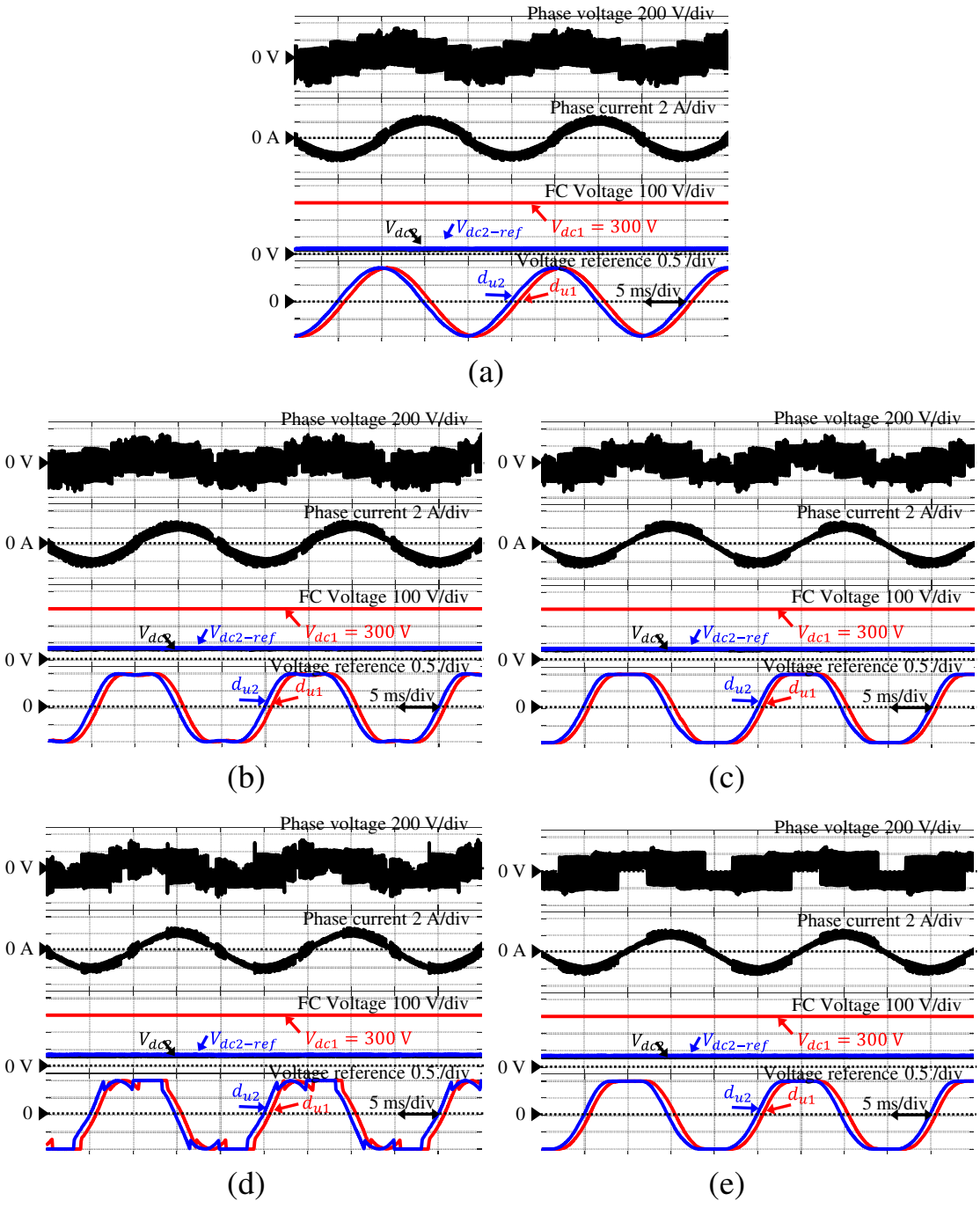


Fig. 4.12. Experimental waveforms for each modulation methods at a torque of 0.5 Nm and a fundamental frequency F_{fun} of 50 Hz (Phase voltage, phase current, FC voltage, and voltage references).

The harmonic analysis results of the phase voltage waveform (top waveforms in Fig. 4.12) are shown in Fig. 4.13, in which the vertical axis is normalized by the fundamental voltage $V_{fun} = 97.0$ V. Here, V_{Cx} represents the peak of the harmonic component at a x times of the carrier frequency. V_{Cx} in each methods indicate that: V_{C1} is the largest in the case of (e) NSPWM, and it is small in the case of (b) THIPWM, (c) DPWM, and (d) SVPWM. In contrast, V_{C2}, V_{C3}, and V_{C4} are the largest in the case of (a) SPWM and decrease in other methods. Furthermore, the sideband of the carrier frequency is shown on the right side of Fig. 4.13, where $\pm xF_{fun}$ denotes a sideband component x times of the fundamental frequency ($F_{fun} = 50$ Hz) centered on the carrier frequency ($F_{C1} = 5$ kHz). In (a) SPWM, (b) THIPWM, and (c) DPWM, F_{C1} and even-numbered components of F_{fun} exist, and in THIPWM and DPWM, the zero-phase component is added to the voltage reference, thus the 4th and 6th-order components increase compared with SPWM (see Fig. 4.3). In contrast, in (d) SVPWM and (e) NSPWM, odd-numbered multiple components exist, and it can be confirmed that the 7th-order component in SVPWM is larger than NSPWM. Note that the low-order harmonics (harmonic components below the carrier frequency) appear less than approximately 1/10 of the high-order components and do not change depending on the modulation method, thus the low-order harmonics are not mentioned in this study.

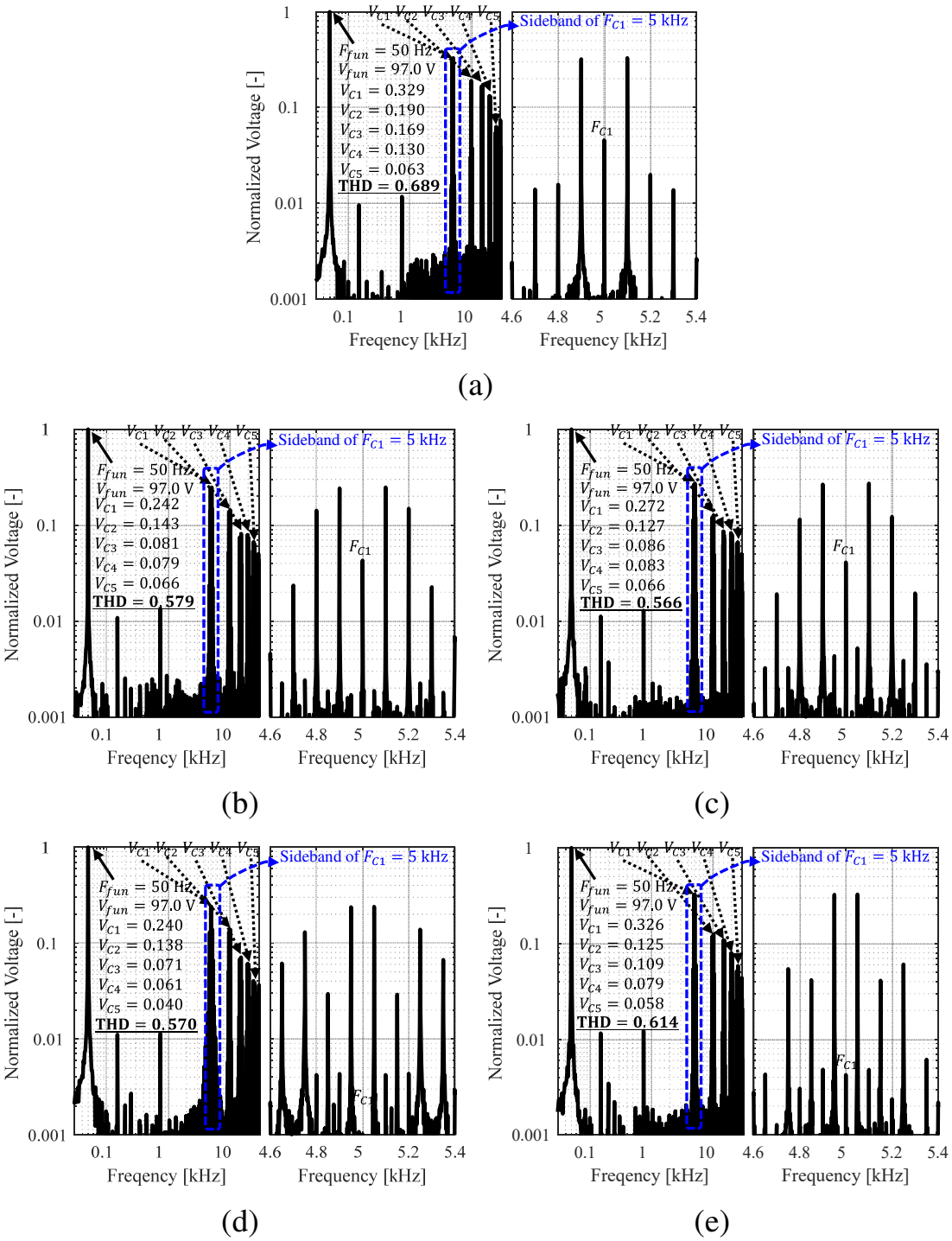


Fig. 4.13. Results of the phase voltage harmonic analysis for each modulation methods at a torque of 0.5 Nm and a fundamental frequency F_{fun} of 50 Hz (Right side: Sideband of carrier frequency F_{c1} = 5kHz).

4.4.3 Characteristics of the Voltage THD

Experiments are carried out when the load torque and the fundamental frequency are changed as shown in Fig. 4.14, which shows the characteristics of the fundamental voltage V_{fun} and power factor angle δ. Here, the fundamental voltage V_{fun} (vertical axis on the left side) is normalized by the maximum phase voltage ($V_{dc1}/2$) when SPWM is used. This result indicates that power factor angle decreases as the load torque increases, and the fundamental voltage increases as the frequency (rotor speed) increases.

In order to verify the effect of reducing voltage harmonics in each modulation methods described in Section 4.3, the voltage THD characteristics are experimentally obtained under the conditions shown in Fig. 4.14. Fig. 4.15 (a) shows the experimental results of voltage THD characteristics, in which the dotted and dashed lines denote the theoretical calculation results in the case of F_{fun} is 10 Hz and 50 Hz, respectively. In addition, the reduction rate of the voltage THD based on the SPWM result are shown in Fig. 4.15 (a) and (b). Note that THD calculation are performed up to 30 kHz; since the carrier frequency is 5 kHz, up to 6 times of the carrier harmonic components are taken into account in this experiment. The voltage THD is small in the low torque and high speed region, and is large in the opposite condition; this result is similar to Fig. 4.9 (a), and it can be confirmed that the other methods also agrees with the theoretical calculation (see Fig. 4.15 (a)). The THD reduction rate when compared with SPWM is smaller than 0 % under all conditions in four methods, thus the voltage THD can be reduced by increasing the modulation index. In particular, it is verified that the voltage THD is reduced by 10.9 % by NSPWM at low speed ($F_{fun} = 10$ Hz), and is reduced by 17.3 % by SVPWM at high speed ($F_{fun} = 50$Hz). Furthermore, in the case of using DPWM at the torque of 0.5 Nm, which means the low power factor angle condition, the same reduction rate as NSPWM and SVPWM is obtained.

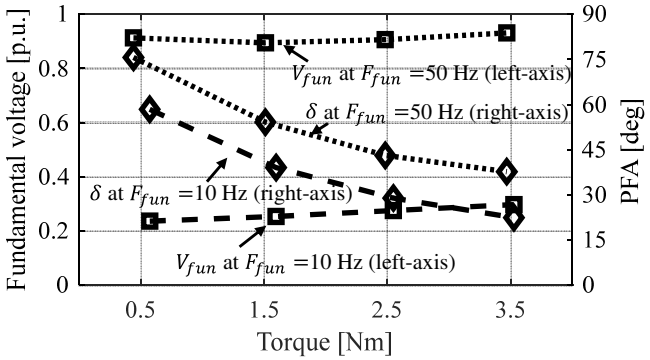
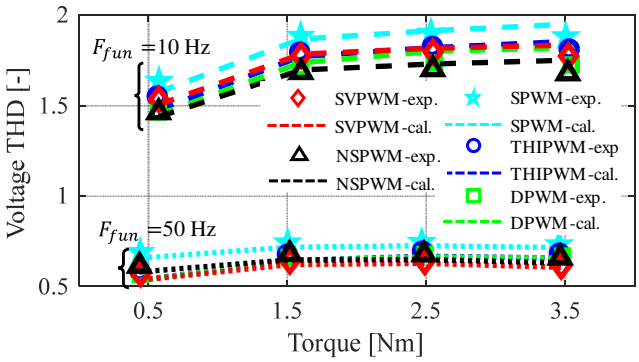
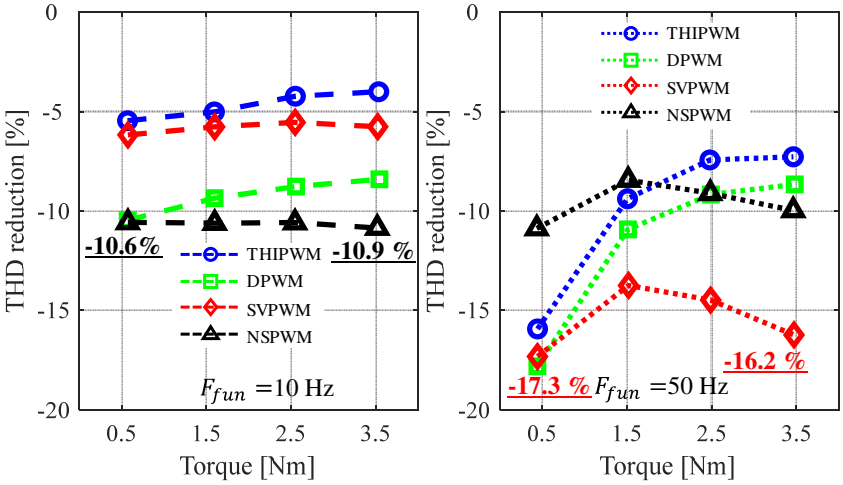


Fig. 4.14. Load torque and fundamental frequency dependencies of the fundamental voltage and power factor angle.



(a)



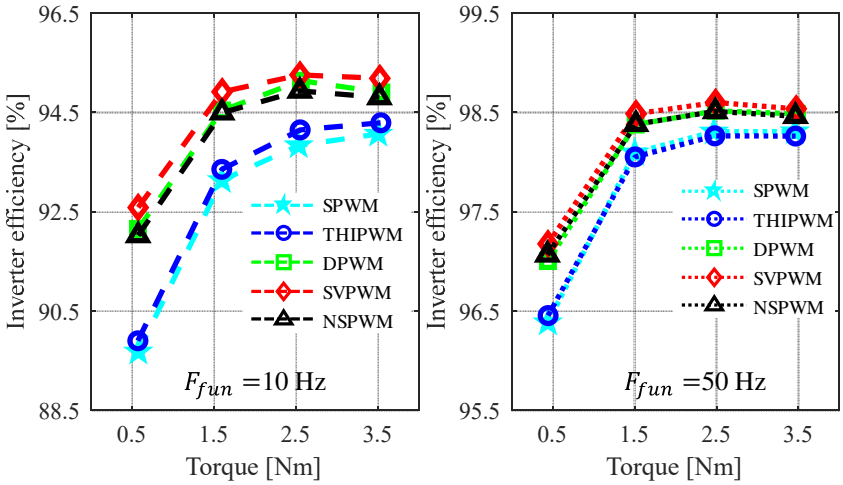
(b) (c)

Fig. 4.15. Experimental results of (a) voltage THD, (b) and (c) THD reduction rate based on THD of SPWM with different operating condition.

4.4.4 Inverter, Motor, and total Efficiency Characteristics

Inverter efficiency and motor efficiency are measured to confirm the effect of decreasing the number of commutations and the effect of reducing the voltage THD due to changing modulation methods.

Fig. 4.16 shows the experimental results of inverter efficiency at the same condition as shown in Fig. 4.14. In DPWM, SVPWM, and NSPWM, the number of commutations in a switching period is 2/3 of that in the case of SPWM and THIPWM, hence the inverter efficiency is increased. In particular, at the lowest load (torque of 0.5 Nm, fundamental frequency of 10 Hz), an improvement in inverter efficiency of 2.9 percentage points (pp) is confirmed. Here, [4-7] reported that the switching loss of DPWM is significantly reduced compared with SPWM; However, in the dual inverter with proposed operation, the difference in efficiency is 2.9 pp at maximum because the power factor angle between each inverter and the motor current is large. In addition, the difference in inverter efficiency between SVPWM,

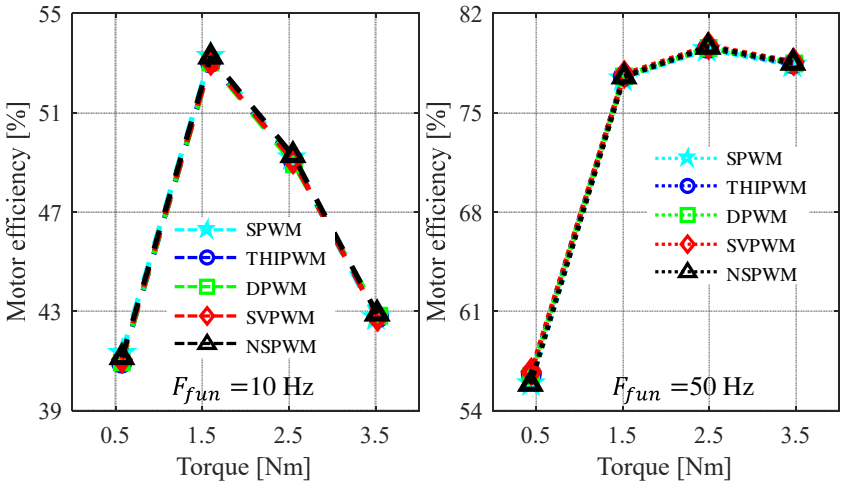


(a) (b)

Fig. 4.16. Experimental results of the inverter efficiency with different operating condition when the fundamental frequency F_{fun} is (a) 10 Hz and (b) 50 Hz.

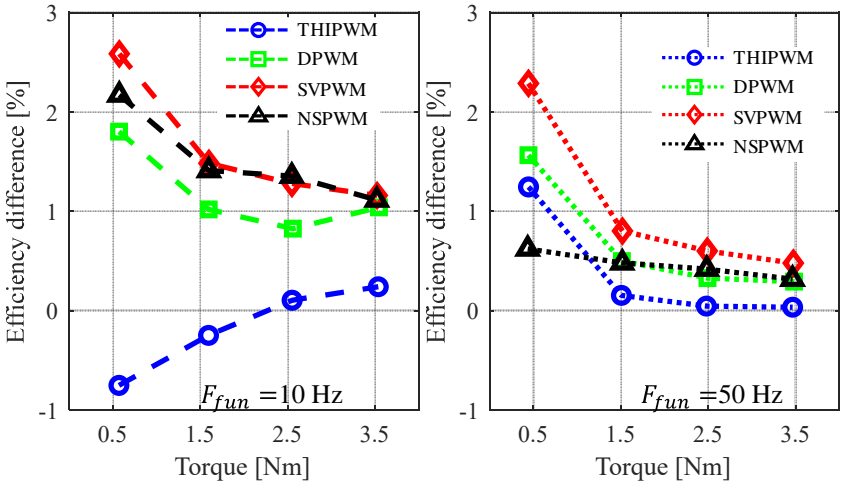
DPWM, and NSPWM is considered to be related to the output time of the zero vector. The output time of the zero vector is absolutely zero in NSPWM, and exists in SVPWM and DPWM, which matches the magnitude relationship of efficiency (see Fig. 4.7 (f)).

Fig. 4.17 and Fig. 4.18 show the experimental results of motor efficiency and total efficiency obtained under the same conditions as the inverter efficiency. Note that in the results of total efficiency, to clarify the difference in total efficiency depending on the modulation method, the vertical axis represents the difference based on the total efficiency in the case of using SPWM in % (shown in Fig. 4.18); hence when the result is a positive value, the total efficiency is higher than SPWM, and when the result is negative, the total efficiency is lower than SPWM. The results of total efficiency when using SPWM are shown in the appendix. Here, the reason why the maximum motor efficiency is obtained at the fundamental frequency of 10 Hz and the torque of 1.5 Nm, and at 50 Hz and 2.5 Nm is that: the maximum efficiency can be obtained when the motor power factor angle is approximately 45 deg [4-8]. The change in motor efficiency due to the modulation method is small compared that due to the load condition. However, the improvement effect is confirmed from the total efficiency (see Fig. 4.18). In the region where the torque is 1.5 Nm or more, the total efficiency is improved in the case of SVPWM and NSPWM compared with other methods. At 10Hz (shown in Fig. 4.18 (a)), the efficiencies of SVPWM and NSPWM are similar, which is the improvement effect of the output voltage THD (see Fig. 4.15 (b)). In addition, it is confirmed that SVPWM at 0.5 Nm improved the total efficiency by 2.6 % compared with SPWM. The reason why the total efficiency in THIPWM is worse than in SPWM is considered as, the number of commutations is the same as SPWM, and the FC voltage is large.



(a) (b)

Fig. 4.17. Experimental results of the motor efficiency with different operating condition when the fundamental frequency F_{fun} is (a) 10 Hz and (b) 50 Hz.



(a) (b)

Fig. 4.18. Efficiency difference of the total efficiency (in %) based on the total efficiency of SPWM with different operating condition when the fundamental frequency F_{fun} is (a) 10 Hz and (b) 50 Hz.

4.5 Conclusion

In this study, the output voltage harmonics when operating the dual inverter, based on a method for reducing the voltage harmonics, in the case of using typical modulation methods (SPWM, THIPWM, DPWM, SVPWM, and NSPWM) are theoretically analyzed. Analysis is performed focusing on the change in the output time of the voltage vector in each modulation method due to the fundamental voltage and the load power factor angle in the dual inverter with FC topology. In addition, the improvement of voltage THD and efficiency is verified by a dual inverter fed open-end winding IM in the experiment. By the method for maximizing modulation index of both inverters in each modulation method, the following are confirmed from the experimental results: voltage THD reduction of 10.9 % with NSPWM and 17.3 % with SVPWM are obtained compared with SPWM; by reducing the number of commutations to 2/3, the inverter efficiency in DPWM, SVPWM, and NSPWM is improved by up to 2.9 pp; and the total efficiency is improved by up to 2.6 % in the low load region by SVPWM.

By the modulation methods based on the analysis results shown in this study, it is possible to contribute to energy-saving at light-load condition.

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Chapter 5

Reducing DC-link Harmonics with Lower Floating Capacitor Voltage

5.1 Introduction

Recently, in terms of lifetime and efficiency of the motor drive system, a harmonic reduction method focused on a DC-link current have been investigated. A dual inverter with a floating capacitor (FC) topology, which consists of two voltage source inverters (VSIs) and an open-end winding induction motor, have been researched to reduce the harmonics of the DC-link current and buffer capacitor. The reduction of the capacitance of the FC and switching frequency component of the DC-link current can be achieved by operating the primary side VSI in six-step [5-1],[5-2]. However, a voltage rating of the secondary side VSI is double or more than that of the primary side VSI. In addition, low order harmonics of DC-link current was not investigated well. In this study, a control method to reduce the high order harmonics of the DC-link current with lower voltage rating at the secondary side VSI is proposed.

This study proposes a control method to reduce the high order harmonics caused by PWM in the DC-link current in a dual inverter with a FC topology, which has the lower voltage ratings in two inverters. The proposed control method reduces the high order harmonic current by six-step operation at a

primary side inverter. The secondary inverter supplies a sinusoidal voltage to the motor using a low rated voltage. The validity of the proposed control method is confirmed by an experiment using an open-end winding induction motor. Furthermore, the FC voltage dependencies of the input current harmonics are analyzed.

5.2 Method to Reduce Floating Capacitor Voltage

5.2.1 Six-step Operation for Reducing DC-link Harmonics

In the proposed method discussed in the previous sections, to reduce output voltage harmonics, INV. 1 outputs PWM waveforms by a maximum modulation index under linear modulation. Hence, the input DC-link current harmonics due to PWM are large, which adversely affects the loss and lifetime of the input battery or capacitors [5-3]. In order to reduce the input current harmonics caused by PWM switching, a six-step operation in INV. 1 has been proposed [5-1] [5-2].

By switching INV. 1 six times in a fundamental period, the harmonics of the carrier frequency component can be reduced. As described in Section 2.3.3, the DC-link current is the superposition and summation of the switched current pulses from each leg (see (2.14)). It indicates that the DC-link current is dependent on not only the switching patterns but also the motor current conditions.

A concept of the six-step operation in INV. 1 is shown in Fig. 5.2 In order to output the sinusoidal voltage to motor winding, INV. 2 outputs a voltage that compensates for the low-order harmonics generated by the six-step operation of INV. 1.

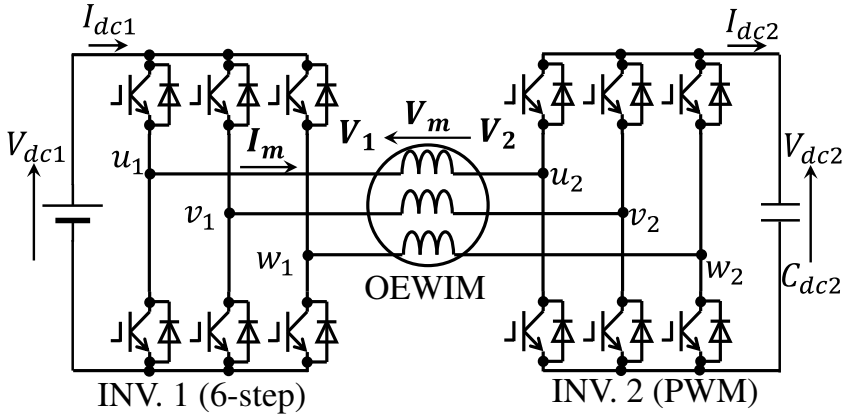


Fig. 5.1. Circuit configuration of the dual inverter fed open-end winding induction motor (OEWIM) with FC system.

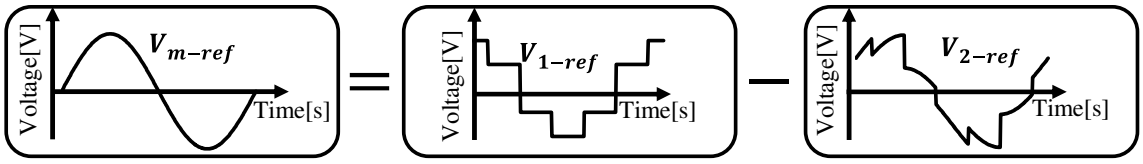


Fig. 5.2. Conceptual voltage references by six-step operation.

5.2.2 Comparison of Floating Capacitor Voltage between Conventional and Proposed Strategies

As mentioned in previous study, in the dual inverter with FC topology, DC-link voltage ratio is expressed as follows:

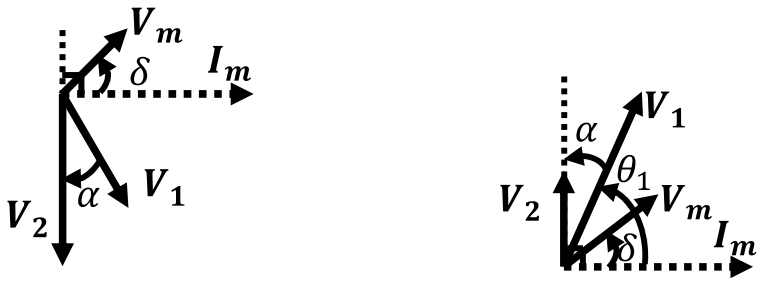
$$\frac{V_{dc2}}{V_{dc1}} = \frac{M_1}{M_2}\frac{\cos(\alpha+\delta)}{\cos\delta} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (5.1)$$

where, M_1 is fixed at $4/\pi$ in six-step operation [5-3], thus the voltage ratio depends on δ, α, and M_2. Here, δ and α denote the motor power factor angle and the phase angle difference between $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$ respectively. Because an active power is supplied by INV. 1 in the FC topology, phase angle difference α is given by:

$$\alpha = \mathrm{Sin}^{-1}\left(\frac{|\boldsymbol{V_m}|}{|\boldsymbol{V_1}|}\cos\delta\right) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (5.2)$$

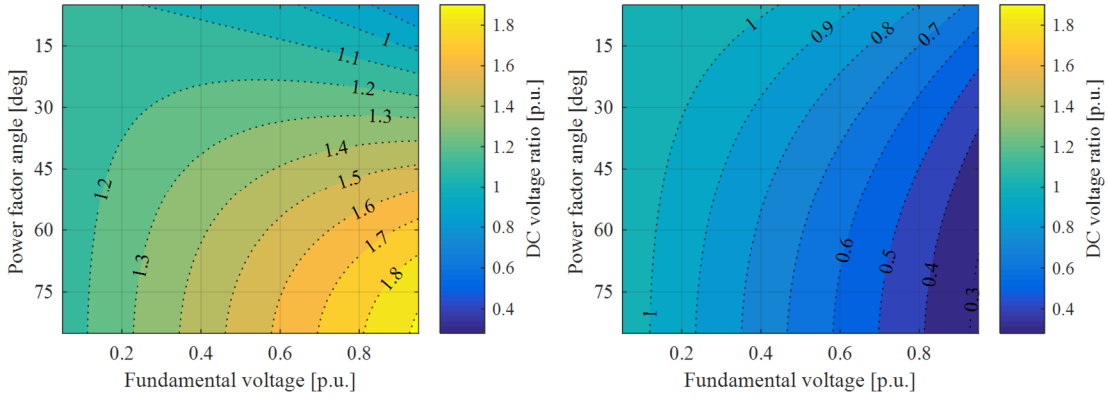
This equation indicates that phase angle difference only depends on the load condition and INV. 1 setting.

In the FC topology, INV. 2 has no power supply thus $\boldsymbol{V_2}$ lags or leads the motor current $\boldsymbol{I_m}$. Conventionally, V_{dc2} is larger than V_{dc1} because $\boldsymbol{V_2}$ lags $\boldsymbol{I_m}$ to increase the compensation power (see Fig. 5.3(a)). In the proposed method, by applying the phase angle of INV. 1 θ_1 achieving the vector relation as $\boldsymbol{V_2}$ leads $\boldsymbol{I_m}$ (shown as Fig. 5.3 (b)), the reduction of the FC voltage compared with the conventional method is achieved.



(a) (b)

Fig. 5.3. Vector diagram of the dual inverter with a FC when (a) $\boldsymbol{V_2}$ lags $\boldsymbol{I_m}$ (conventional method) and (b) $\boldsymbol{V_2}$ leads $\boldsymbol{I_m}$ (proposed method).



(a) (b)

Fig. 5.4. Theoretical results of the DC voltage ratio ($G = V_{dc2}/V_{dc1}$) characteristics with different power factor angle δ and fundamental voltage V_{fun} by (a) conventional and (b) proposed method, where M_2 is assigned at $2/\sqrt{3}$.

Fig. 5.4 shows theoretical calculation results of the DC voltage ratio ($G = V_{dc2}/V_{dc1}$) according to (5.1) and (5.2), where the result of conventional operation is calculated as ($\alpha = -\alpha$). Here, modulation index M_2 is assigned at $2/\sqrt{3}$. The results shows that: in the conventional method, it is necessary to increase the FC voltage except in the region of low power factor angle (15 deg) and high output voltage (0.8 p.u.) (see Fig. 5.4(a)); by the proposed method, the FC voltage can be reduced in regions other than the low power factor angle and low output voltage (see Fig. 5.4(a)).

5.3 Theoretical Analysis of Input DC-Link Current Harmonics

As introduced in Section 2.3.3, the RMS value of the DC-link current $I_{dc1-RMS}$ and normalized DC-link current harmonics I_{dc1-h} can be calculated in the similar way as voltage harmonics mentioned in Chapter 3 as:

$$I_{dc1-RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{dc1}^2(\theta)d\theta} \quad \cdots\cdots (5.3)$$

$$I_{dc1-h} = \frac{\sqrt{I_{dc1-RMS}^2 - I_{dc1\_ave}^2}}{I_m} \quad \cdots\cdots (5.4)$$

where, the average value of DC-link current in an electrical angle $I_{dc1-ave}$ is given by modulation index M_1, amplitude of the phase current I_m, and the power factor angle of INV. 1 θ_1 as:

$$I_{dc1-ave} = \frac{3}{4} M_1 I_m \cos\theta_1 \quad \cdots\cdots (5.5)$$

Next, the theoretical calculation of the input current harmonics I_{dc1-h} are performed using (5.3)-(5.5). In this calculations, the operable area and input current when G_{dc} is fixed are calculated. Here, modulation index of INV. 2 M_2 is calculated by transforming (5.1) as:

$$M_2 = \frac{M_1}{G_{dc}} \frac{\cos(\alpha+\delta)}{\cos\delta} \quad \cdots\cdots (5.6)$$

In addition, the case where $M_2 > 2/\sqrt{3}$ is defined as the inoperable region, because INV. 2 operates in the over-modulation region, which causes the output voltage cannot be controlled to a sinusoidal waveform.

The theoretical calculation results are shown in Fig. 5.5 and Fig. 5.6. Here, the conventional method is calculated with $G = 2.0$ and $G = 1.2$,

and the proposed method is calculated with $G = 1.2$ and $G = 1.0$. A common matter is that the input current harmonics I_{dc1-h} are reduced in the high output voltage and low power factor angle (high power) region. This is because when δ is small and $|\boldsymbol{V_m}|$ is large, α becomes large which leads to be θ_1 small (see Fig. 5.3 (b)). Comparing Fig. 5.5 and Fig. 5.6, the proposed method can operate in the all load region with $G_{dc} = 1.2$; however, twice the FC voltage is required in the conventional method.

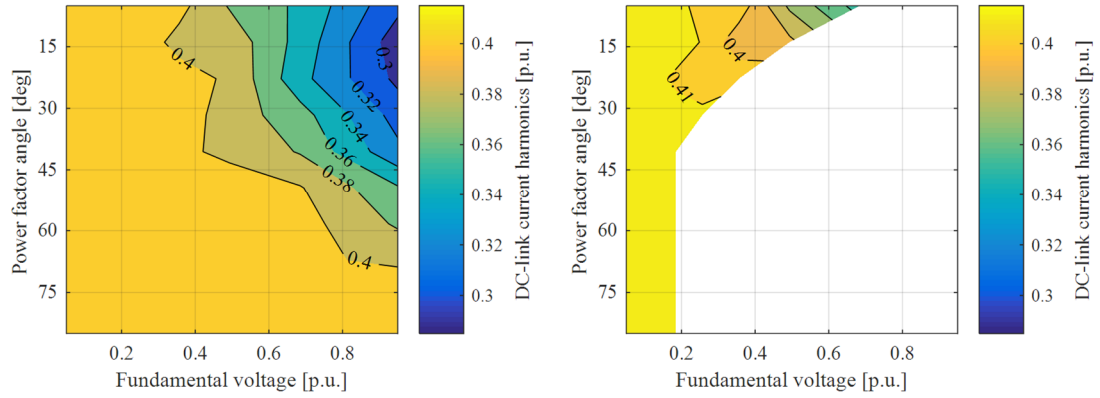


Fig. 5.5. Theoretical results of the input DC-link current harmonics I_{dc1-h} characteristics with different power factor angle δ and fundamental voltage V_{fun} when (a) $G_{dc} = 2.0$ and (b) $G_{dc} = 1.2$.

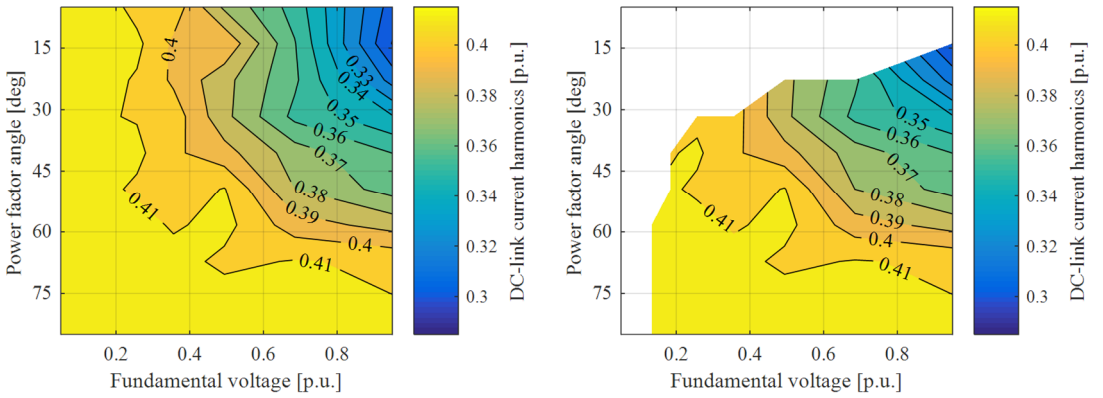


Fig. 5.6. Theoretical results of the input DC-link current harmonics I_{dc1-h} characteristics with different power factor angle δ and fundamental voltage V_{fun} when (a) $G_{dc} = 2.0$ and (b) $G_{dc} = 1.2$.

5.4 Experimental Results

5.4.1 Control Strategy and Experimental Setup

Fig. 5.7 shows a control block diagram and an experimental setup of this proposal, which is based on a control strategy of the reduction of the output voltage harmonics in the dual inverter system. In the proposed control method, INV. 1 operates in six-step thus the INV. 1 voltage reference $\boldsymbol{V_{1-ref}}$ is defined as:

$$\boldsymbol{V_{1-ref}} = \frac{V_{dc1}}{2}\begin{bmatrix} \text{sign}\{\cos(wt+\theta_1)\} \\ \text{sign}\{\cos(wt-2\pi/3+\theta_1)\} \\ \text{sign}\{\cos(wt+2\pi/3+\theta_1)\} \end{bmatrix} \quad \cdots\cdots\cdots\cdots \quad (5.7)$$

$$\theta_1 = \frac{\pi}{2} - \alpha - \beta \quad \cdots\cdots\cdots\cdots \quad (5.8)$$

where, the wt denotes an electrical angle of the motor voltage reference $\boldsymbol{V_m}$ and θ_1 denotes the phase angle difference between $\boldsymbol{V_{1-ref}}$ and $\boldsymbol{I_m}$

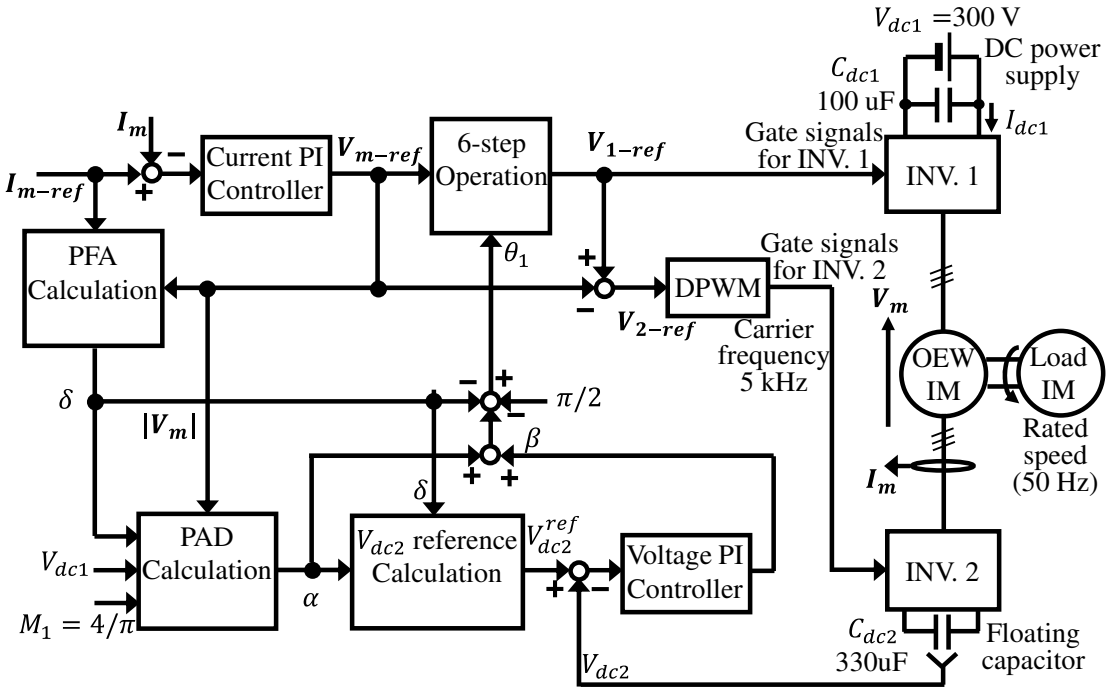


Fig. 5.7. Control block diagram and experimental setup.

(see Fig. 5.3(b)). Here, a charging/discharging angle β is given by the FC voltage PI controller (described in Chapter 3). Finally, INV. 2 outputs the compensation voltage to supply a sinusoidal voltage in the motor, where discontinuous pulse width modulation (DPWM), which can maximize the modulation index and reduce the number of switching by injecting the zero-sequence component into the sinusoidal reference, is used as modulation method in INV. 2 (described in Chapter 4).

A general-purpose induction motor (TFO-FK 0.75KW 4P 200V) is used for experiment. The experimental condition and open-end winding IM parameters are shown in Table 5.1 and Table 5.2 In this experiment, a DC power supply regulates the INV. 1 DC-link voltage at 300 V. The open-end winding IM is controlled at rated speed (50 Hz) and 0.5 Nm (approximately 0.1 p.u. of rated torque). To obtain the characteristic of the DC-link current harmonics, the FC voltage reference V_{dc2} is changed from 330 V to 210 V.

Table 5.1. Experimental condition.

INV.1 DC voltage: V_{dc1}	300 V
INV.2 DC voltage: V_{dc2}	According to (5.1)
INV.2 DC capacitance: C_{dc2}	330 uF
Carrier Frequency: F_{c1}	5 kHz
Dead-time: T_{DT}	500 ns

Table 5.2. Parameters of the open-end winding IM.

Rated power	750 W	Poles	4
Rated voltage	200 V	Rated frequency	50 Hz
Rated current	3.5 A	Rated speed	1410 rpm
Leakage inductance	10.5 mH	Rated torque	5.0 Nm
		Stator resistance	2.74 Ω
Mutual inductance	0.195 H	Rotor resistance	2.08 Ω

5.4.2 Experimental Waveforms

Fig. 5.8 shows experimental waveforms of the proposed method when the FC voltage is regulated at (a) 300 V ($G_{dc2} = 1.0$ p.u.) and (b) 240 V ($G_{dc2} = 0.8$ p.u.); The results indicate that the FC voltage is regulated less than the INV. 1 DC-link voltage and the motor phase current control is achieved even if V_{dc2} is changed.

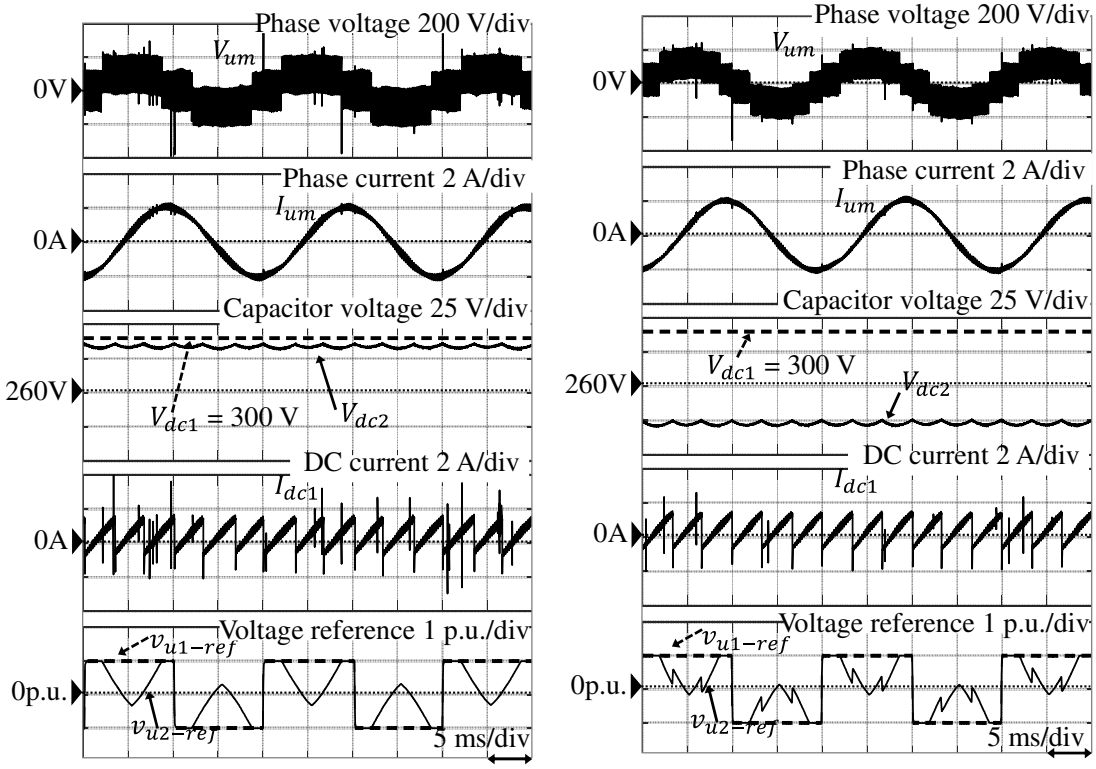
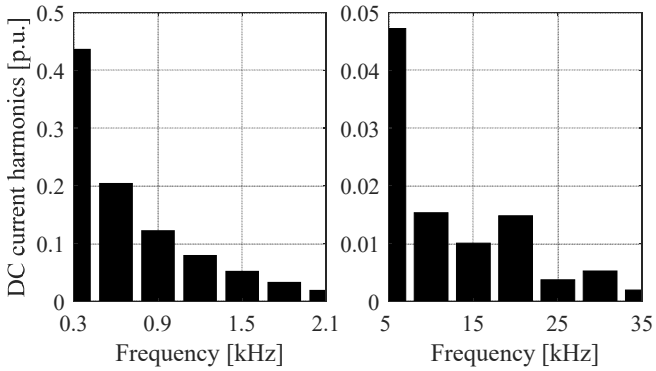


Fig. 5.8. Experimental waveforms of the phase voltage V_{um}, phase current I_{um}, FC voltage V_{dc2}, DC-link current I_{dc1}, and voltage references v_{u1-ref} and v_{u2-ref}, when the FC voltage reference is (a) 300 V and (b) 240 V.

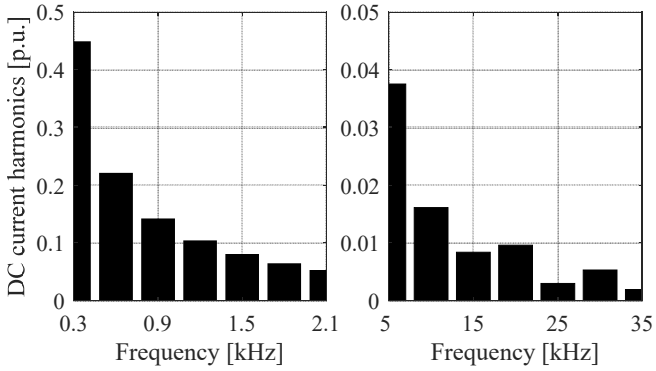
5.4.3 Harmonic Analysis of the DC-link Current

Fig. 5.10 shows results of the harmonic analysis of the INV. 1 DC-link current, which are separated into low order region (300 Hz to 2100 Hz) and high order region (5 kHz to 35 kHz); Compering each harmonic components, the low order harmonics when $G_{dc2} = 1.0$ p.u. are smaller than that when $G_{dc2} = 0.8$ p.u.; In contrast, the high order harmonics when $G_{dc2} = 1.0$ p.u. decrease compared with that when $G_{dc2} = 0.8$ p.u.

Fig. 5.10 shows an FC voltage dependency of the INV. 1 DC-link current harmonics, which are obtained by sum of each component separated into low order and high order harmonics; The results show that high order harmonics



(a)



(b)

Fig. 5.9. Harmonic analysis of the DC-link current I_{dc1} separated into low-order (left-side) and high-order (right-side), when the FC voltage reference is (a) 300 V and (b) 240 V.

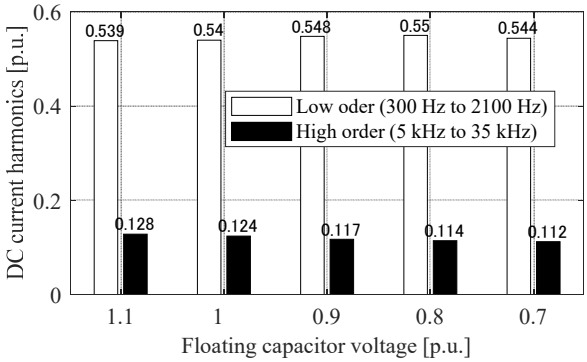


Fig. 5.10. Floating capacitor voltage dependency of the DC-link current harmonics, which are separated into low order region (300 Hz to 2100 Hz) and high order region (5 kHz to 35 kHz).

of DC-link current decreases as the FC voltage decreasing due to the switching ripple in the phase current decreases; In contrast, the low order harmonics slightly increase as the FC voltage increasing.

5.4.4 Inverter and Motor Efficiencies

Fig. 5.10 shows the FC voltage dependency of the input DC-link current harmonics and output voltage harmonics, which are calculated by RMS values ($I_{dc1-RMS}, V_{RMS}$), and the average or fundamental components ($I_{dc1-ave}, V_{fun}$), respectively. The results show that: as the FC voltage decreases, the input current harmonics increase; in contrast, the output voltage harmonics decrease. This is because the output voltage has a multi-level waveform as decreasing the FC voltage (see Fig. 5.8).

Fig. 5.10 shows the FC voltage dependency of the inverter efficiency and the motor efficiency. As the FC voltage decreases, both of efficiencies are improved. The reason why the inverter efficiency is improved from the result shown in Chapter 4 (shown as Fig. 4.16) is that, the number of switching of INV. 1 is few (six times in an electrical period). In addition, the motor efficiency is improved because the output voltage harmonics shown in Fig. 5.10 are reduced.

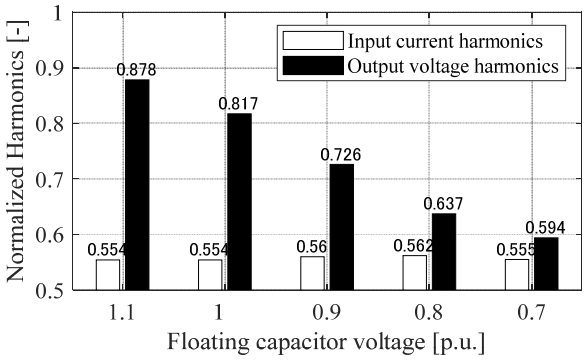


Fig. 5.11. Experimental results of the FC voltage dependency of the input current harmonics and output voltage harmonics.

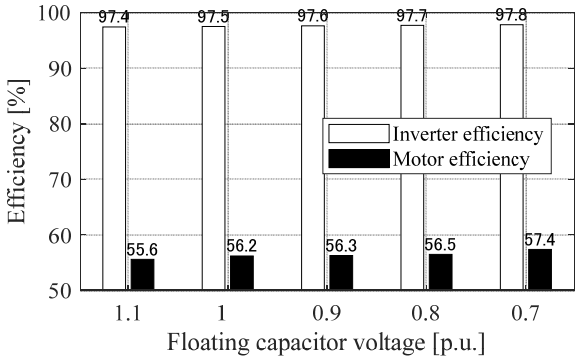


Fig. 5.12. Experimental results of the FC voltage dependency of the Inverter efficiency and motor efficiency.

5.5 Conclusion

In this study, a control method that reduces the FC voltage for low voltage ratings of the switching devices and capacitor in the dual inverter fed open-end winding IM was proposed and was experimentally demonstrated. The FC voltage dependency of the input DC-link current was analyzed separately for low order and high order harmonics in this experiment. This result will be useful when selecting DC capacitors and batteries.

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Chapter 6

Conclusion

6.1 Discussion

Compared to the traditional single inverter topology, the dual inverter topology offers more flexibility in switching, which has advantages such as improved reliability, extended output range, multi-level operation, and input/output power compensation. In addition, with the improvement of performance and cost reduction of semiconductor switching components, power converters having many switching components have been installed in electric vehicles and air conditioners, etc., and dual inverters have being studied as one method to achieve high performance. In this thesis, the trend of motor drive systems were shown; the necessity of improving the efficiency of induction motor drive systems in the light-load region of approximately 50% or less. In addition, the input/output harmonics generated by the motor drive system were introduced, and a dual inverter drive motor system was presented. This study contributed to the high performance of the motor drive system in the light-load region in terms of the control strategy for dual inveter.

Chapter 2 reviewed the state of arts of the current approaches of the dual inverter topology. An evaluation method of output voltage harmonics and input current harmonics in the dual inverter topology that realizes high performance of the motor drive system was proposed. In addition, conventional

dual inverter drive methods that reduce input/output harmonics and their issues are discussed. Finally, proposed phase modulation control to reduce the input/output harmonics of the dual inverter topology using the motor power factor, which is the key concept of this thesis, were described and a beneficial position of the proposed strategies along with conventional methods was presented.

Chapter 3 described a control strategy for reducing voltage harmonics of an induction motor in a low-torque condition. The motor drive system consists of an open-end winding induction motor and two voltage source inverters; the dual inverter has a DC voltage source and a floating capacitor. In proposed method, the use of the output voltage difference between the inverters constituting the dual inverter lowers the harmonics by keeping the modulation index high owing to the phase angle difference variation between the two inverters. The performance of harmonics reduction was theoretically analyzed and experimentally verified.

Chapter 4 described an analysis strategy for the output voltage harmonics, which depend on the fundamental voltage, power factor angle, and PWM strategies. Herein, sinusoidal PWM (SPWM), third-harmonic-injection PWM (THIPWM), and discontinuous PWM (DPWM) are used as the conventional carrier-based modulation techniques, and space-vector PWM (SVPWM) and near-state PWM (NSPWM) with reduced number of commutations are used as the proposed modulation methods. The validity of the theoretical analysis was confirmed by experiments using an open-end winding induction motor.

Chapter 5 described a control method to reduce the high-order harmonics caused by PWM in the DC-link current in a dual inverter with an FC topology, which has the same voltage ratings in two inverters. The proposed control method reduces the high-order harmonic current through a six-step operation at the primary inverter. The secondary inverter supplies a sinusoidal voltage to the motor using a low-rated voltage. The validity of the proposed control method was confirmed through an experiment using an open-end winding

induction motor. Furthermore, the FC voltage dependencies of the input current harmonics was analyzed.

6.2 Comparison of Proposed PWM Strategies

This section compares the proposed PWM strategies. Table 6.1 lists the comparison of the proposed control and modulation strategies. Here, the methods introduced in this thesis are compared from the following viewpoints: Hardware demand (thigs that necessary for operation), Reducing switching loss, Output quality (voltage harmonics applied to the stator winding), and Input quality (DC-link current harmonics of the primary inverter).

In terms of the hardware demand, 2-isolated DC-links topology (2DC) with synchronized SVPWM (presented in Chapter 2) literally needs the additional DC power source compared with other strategies. In addition, Field Programmable Gate Array (FPGA) are required for synchronous SVPWM, which changes the commutation timing of the two inverters depending on the magnitude of the current (shown in Chapter 3), and SVPWM/NSPWM,

Table 6.1. Comparison of the proposed control and modulation strategies.

Comparison aspects	For output harmonics (Chapter3, 4)		For input harmonics (Chapter 5)
Modulation strategy	SPWM and THIPWM / DPWM	SVPWM and NSPWM	six-step with DPWM
Hardware demand	Small floating capacitor	Small floating capacitor, FPGA	Medium floating capacitor
Reducing switching loss	No / Yes	Yes	Yes
Output harmonics (Voltage THD)	Middle (>0.69)	Low (>0.55)	High
Input harmonics	High	High	Low

which cannot realize switching patterns by comparing triangular carriers (shown in Chapter 5).

In DPWM, SVPWM, and NSPWM introduced in Chapter 5, since there is a period which one leg does not switch, reducing the switching loss can be achieved. Further, in the method of operating INV. 1 in six-steps, introduced in Chapter 6, INV. 1 switches only 6 times within the fundamental period, thus the switching loss can be reduced. In the 2DC method introduced in Chapter 2, the DC-link voltage of the INV. 2 is changed proportional to the fundamental output voltage, and both inverters operate at an modulation indices of $2/\sqrt{3}$ (maximum modulation index under the linear modulation). In that case, the THD of the voltage applied to the winding can be calculated as (3.10):

$$THD = \sqrt{\frac{8}{\sqrt{3}\pi M} - 1} \cong 0.52 \quad \cdots\cdots\cdots\cdots \quad (6.1)$$

Furthermore, the output voltage THD in SPWM in the FC topology is expressed by (3.7), the smallest THD can be calculated (at power factor angle = $\pi/2$ rad and the fundamental voltage is 1 p.u.) as:

$$THD = \sqrt{\frac{8}{\sqrt{3}\pi M}\frac{1+\left(\frac{V_{dc2}}{V_{dc1}}\right)^2 - \sqrt{\frac{28}{3}}\frac{V_{dc2}}{V_{dc1}}\cos\varphi}{1+\left(\frac{V_{dc2}}{V_{dc1}}\right)^2 - 2\frac{V_{dc2}}{V_{dc1}}\cos\alpha} - 1} \quad \cdots\cdots \quad (6.2)$$
$$\cong 0.69$$

Here, the phase angle difference α and the voltage ratio V_{dc2}/V_{dc1} are

$$\alpha = \mathrm{Sin}^{-1}\left(\frac{|\boldsymbol{V_m}|}{|\boldsymbol{V_1}|}\cos\delta\right) \cong 0 \quad \cdots\cdots\cdots\cdots \quad (6.3)$$

$$\frac{V_{dc2}}{V_{dc1}} = \frac{\cos(\alpha+\delta)}{\cos\delta} \cong 1 \quad \cdots\cdots\cdots\cdots \quad (6.4)$$

In addition, as a result of theoretical analysis, DPWM, SVPWM, and NSPWM can improve THD by about 20% compared to SPWM method (see Chapter 4); thus the minimum THD is about 0.55. Therefore, the method that can improve the output voltage THD most is 2DC with synchronous SVPWM.

6.3 Future Works

6.3.1 Analytical Approach

This thesis has demonstrated that the proposed PWM strategies are capable of achieving the output voltage harmonics reduction and the DC-link current harmonics reduction for the variable speed motor system in the light-load condition. However, reduction of both output voltage harmonics and input current harmonics has not been realized. Therefore, a future work is to study a switching pattern that minimizes both input current and output voltage harmonics.

6.3.2 Hardware Approach

For industrial applications, the number of elements in the system is required to be as small as possible, thus it would be good if the elements for gate drive could be omitted. In the common DC-link (CDC) topology introduced in Chapter 2, since the emitter (or source) of the bottom arm switches is common, the gate drivers can be shared. In contrast, the DC link cannot be shared, thus it is necessary to separately insulate the gate driver and FC voltage measurement in the FC topology. In addition, in the study of sensorless dual inverters, the FC voltage can be estimated by fixing the phase angle difference of the inverters and measuring the load power factor offline. Finally, by identifying the FC voltage, the current flowing into the secondary inverter can be estimated from the switching pattern, and current sensor-less can be realized.

List of Achievements

Publication Journals

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