Silicon on Isolator Ribbon Field-Effect Nanotransistors for High-Sensitivity Low-Power Biosensors

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Highlights:

- The electrophysical characteristics of 3D nanoscale low-voltage silicon sensors as surface charge detectors in an electrolyte medium were studied theoretically and experimentally.
- It was established that thin structures with a width of slightly than more 100 nm, a thin layer of silicon oxide, and a reduced level of doping have promising sensor characteristics.
- The considered technique opens up an effective approach to scaling pH sensors, providing high resolution per unit of occupied area with minimal energy consumption.

Abstract. Silicon field-effect transistors (FETs) are an established technology for sensing applications. Recent advancements and the use of high-performance multigate FETs in computing technology raise new opportunities and questions about the most suitable device sensing architecture. In this work, we propose pH sensors exploiting ribbon (tri-date) FETs fabricated on investigated silicon nanowires and silicon-on-insulator substrates by a fully CMOS compatible approach. The FET characteristics were optimized using 3D modeling performed by the TCAD computer-aided design software package, depending on the topological parameters of the transistor and the level of control voltage. N-channel fully depleted ribbon FETs with critical dimensions in the order of 30 nm and SiO_2 as a subgate insulator were developed and characterized. It was established that thin structures with a width of slightly than more 100 nm, a thickness of 40 nm, and a reduced doping level have high sensitivity and low energy consumption. They showed excellent electrical properties, subthreshold swing (SS) was about 90 mV/dec, and the on-to-off current ratio, Ion/Ioff, was about 10^5. The same architecture was tested as a highly sensitive, stable and reproducible pH sensor. The average internal sensitivity, S, was equal 34 mV/pH or 360 nA/pH. Sensitivity to pH, estimated in terms of relative changes in the threshold voltage, was 74%, and the maximum drain current was 40%. The maximum drain current of 85 μA at V ds = 1.0 V suggests successful low-power operation of the proposed device.

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1   Introduction

Silicon nanowire field-effect transistors have long been studied as biological sensors because of their increased sensitivity due to having a large surface-to-volume ratio (SVR) and high selectivity with respect to a significant number of analytes [1-4]. In this field, nanoscale multi-gate transistors, which are designed for high-performance solid-state bio- and chemical sensors, have evolved into a separate group due to their excellent properties of converting electrostatic potential into electric current, which can be advantageously used for pH measurement [5-7].

In solving the problem of developing a scalable sensor designed for pH detection with high technological repeatability, we were guided by the availability of the well-tested SOI (silicon on insulator) technology for analog-digital applications. In this case, we took a successfully functioning software-technology hub. With its help, a new technological process was effectively developed for the production of ribbon field-effect transistors applicable for pH detection. As recent research has shown, spintronics-based sensors have attractive characteristics [8-10]. However, the issue of technological repeatability is still unresolved.

With the help of the computer-aided design software package TCAD [11], we developed prototypes of SOI devices based on technological processes compatible with CMOS technology [12-14]. The use of technological requirements provides a high level of control over technological variations and allows to produce real transistors with high accuracy in a wide range of topological parameters. In this study, low-voltage electrophysical characteristics of silicon field-effect nanowire transistors with a ribbon cross-section of the working area were investigated using TCAD models to optimize their sensor properties [15-17]. Based on the obtained simulation results, a chip was manufactured on an SOI substrate based on self-aligning CMOS-compatible technological processes from top to bottom with an accuracy of up to 5 nm. The use of a semi-industrial process provides a high level of control over technological variations [18] and allows the production of high-integration nanowire field-effect transistors with a well-defined orientation and a wide range of technological parameters. Our results allowed us to estimate the minimum sensor resolution (0.2 pH) that can be achieved at a low supply voltage. It was also shown that ribbon devices represent an effective approach to reducing the size of high-resolution pH sensors per unit of occupied area with minimal power consumption. This feature is of particular interest for integrated pH bio analytics based on CMOS technology [1,5,19].

2   TCAD simulation

We initially tested the basic transistor architecture shown in Figure 1. Here, both the front (Π-shaped) and back (planar) gates were solid-state. Using 3D TCAD simulation, the electro-physical characteristics for various topological parameters were studied: length (Lg), width (W), height (tS), and doping concentration (NA) of the working area, dielectric coating over the channel in the form of silicon oxide thickness (tox), topology of the source/drain regions (S/D) and their doping concentration (Nds), and thickness of the buried oxide silicon oxide tb. These parameters were selected based on the general provisions of the technology of SOI multi-gate fin field structures [20]. The selected parameters were varied in order to find the optimal characteristics of the device for a low-power sensor with a large dynamic range [21, 22].
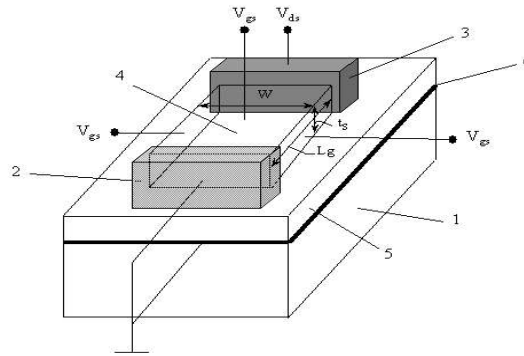
Figure 1   Sketch of the basic architecture, where 1 = silicon substrate, 2 = source, 3 = drain, 4 = ribbon working area with a Π-shaped front gate and a dielectric layer, 5 = buried oxide, 6 = back gate.

3D simulation of TCAD using Sentaurus Device.2010.12 [11] was performed for a dielectric coating over a channel with a minimum thickness of $t_{ox} = 2.3$ nm and a permittivity of 3.9. The t_{ox} parameter is very important. It is responsible for the transistor current level (with its decrease, the current increases) and for the breakdown of the gate voltage (with its decrease, the breakdown voltage decreases) [23]. We chose the t_{ox} value close to the minimum breakdown. The geometric dimensions of the working area varied in the following ranges: length L_g from 1,000 to 4,000 nm, height t_S from 30 to 50 nm, and width W from 100 to 250 nm. The working area of the transistor was doped with boron with a concentration ranging from 1×10^{22} m^{-3} to 1×10^{24} m^{-3}. The thickness of the buried oxide t_b varied from 100 to 300 nm. The front gate was modeled as N+ polysilicon (with a concentration of 2×10^{27} m^{-3} and an output of 4.1 V). The source and drain were doped with phosphorus with a concentration of 2×10^{26} m^{-3}. The S/D regions were 500 × 500 nm. The S/D contacts were modeled as

ohmic. In the calculations, the drain voltage V_{ds} and the front gate voltage V_{gs} varied with a grounded source and a back gate. The V_{gs} voltage was applied simultaneously to all three faces of the front gate.

The drain current I_D was calculated by solving the Poisson equation and the equation of continuity for the main carriers over the entire cross-section of the working area [23]. The drift-diffusion model was used for carrier transport in a semiconductor, taking into account impact ionization [24]. A carrier mobility model was used, taking into account the effects of carrier scattering in high-doping semiconductors, as well as a Shockley-Reed-Hall model of carrier recombination/generation, which depends on the distribution of the electric field in the working area [23]. It should be noted that the behavior of all prototypes corresponded to the generally accepted behavior of a traditional CMOS transistor. At the same time, the subthreshold slope (SS) of all prototypes did not exceed 80 mV/dec. The threshold voltage (U_{th}) was 0.5-0.7 V and did not depend on the width, W, unlike the current of the I_D transistor [23].

Figure 2 shows the generalized results of the I-V data calculations for the prototypes. The maximum drain current I_{D_max} had the following dependences on the parameters L_g, W, t_S at the drain voltage $V_{ds} = 1.0$ V, and at the front gate $V_{gs} = 1.5$ V. The typical I_{D_ON}/I_{D_OFF} current ratio was from 10^4 to 10^6.
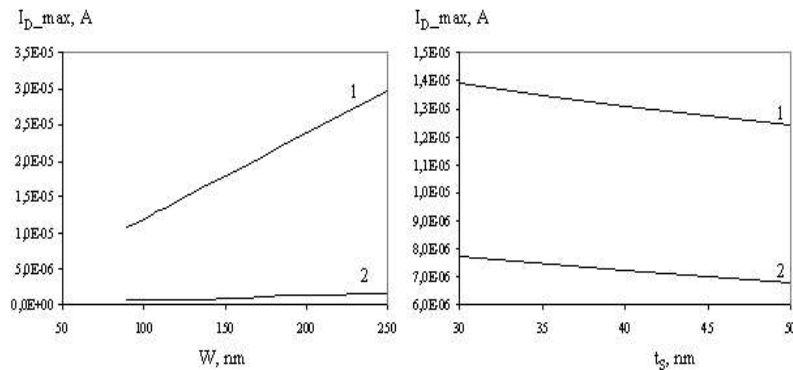
Figure 2 Dependences: (left) I_{D_max} from W at $t_S = 40$ nm, where (1) $L_{g} = 1150$ nm, (2) $L_{g} = 2250$ nm; (right) I_{D_max} from t_S at W = 150 nm, where (1) $L_{g} = 1150$ nm, (2) $L_{g} = 2250$ nm.

All the dependences were linear, but their slope depended on the L_g parameter. At the same time, with the growth of L_g, the slope decreased. The extracted values

of the slope of the $I_D(W)$ and $I_D(t_S)$ characteristics for different L_g are shown in Figure 3.
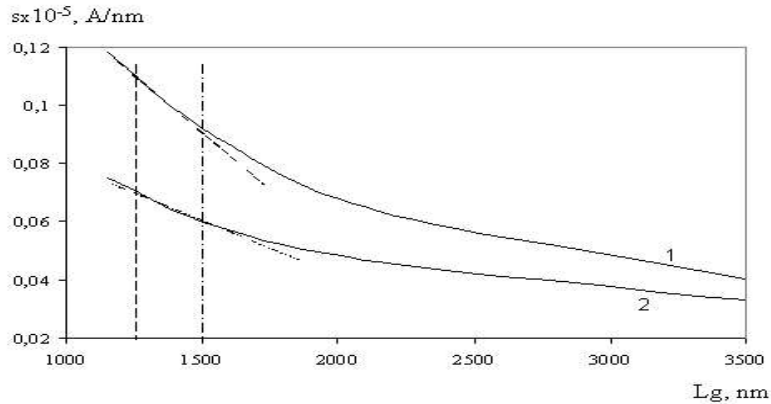
Figure 3 Dependence of the slope of (1) $I_{D\_max}(W)$ from Lg at $t_S = 40$ nm, (2) $I_{D\_max}(t_S)$ from Lg at W = 150 nm, the thick dotted line is the middle of the current range of parameters, the thick dash-dotted line is the border of the current range, and the thin dotted line is an approximating line.

Comparing the dependences in Figure 3, we note the areas on them where they have a greater slope, which is a criterion for increased sensitivity of the transistor current to the geometric dimensions of the working area. In this case, the following significant ranges were obtained: length L_g from 1,000 to 1,500 nm, height t_S from 30 to 50 nm, and width W from 100 to 200 nm. We conducted further research on these. It should be noted that the doping level of the working area practically did not affect the steepness of the dependencies shown in Figure 3. However, the value of the N_A parameter affected the current of the transistor [20], which is important when evaluating the pH sensitivity [25,26]. In further experiments, its influence was studied. In contrast, the value of the parameter t_b did not have a noticeable effect on the I-V data of the studied prototypes. The thickness of the t_b determines the capacitance connections in the transistor to a greater extent, i.e., it affects the dynamic characteristics of the device [23]. Therefore, we set its value to 150 nm for further research.

Figure 4 shows the key characteristic of the sensor's SVR for the selected range of geometric parameters of transistors. Here, the maximum value of the SVR parameter was 0.063. It should be noted that it did not depend on the length, Lg.
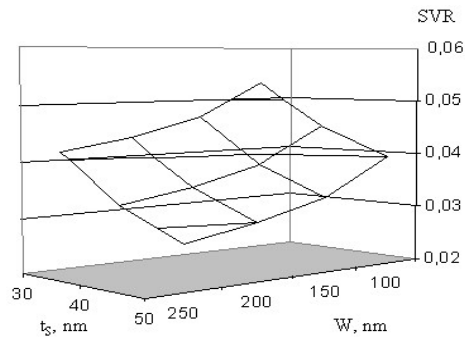
Figure 4   Dependence SVR(W, t_S)

It was expected that the maximum value of SVR corresponded to the minimum values of W and t_S. When they increased, it decreased gradually. In contrast, the current Ids increased with the increase of the W parameter.

## 3   pH Sensitivity of Single Transistor Sensors

The experimental transistor architecture differed from the basic design of a front gate. In the real case, there is a cavity between the front electrode and the front gate silicon oxide, which is filled with an electrolyte with different pH, i.e., experimental samples can work with a liquid front gate [1,27,28]. For the experimental studies, a chip of 96 transistors with a thickness of 40 nm and different widths, lengths, and doping levels was formed on a silicon wafer. The n+/p/n+ ribbon transistors were fabricated on SOI wafers and patterned by means of top-down hybrid deep ultraviolet and e-beam lithography, followed by reactive ion etching. The fabrication process was entirely developed at SRISA.

The wafers were composed of a 100 nm silicon layer on top of a 150 nm thick SiO_2 insulating bulk oxide layer. The silicon top layer was first thinned by chemical mechanical polishing and then by several steps of silicon thermal oxidation/desoxidation to obtain a 40 nm silicon top layer, which defined the thickness. High-quality 2.3 nm SiO_2 gate oxide was grown using thermal dry oxidation. In order to obtain n-type devices, the transistors were doped by boron implantation. A sacrificial polysilicon gate was used as a hard mask to dope the source and drain terminals with phosphorous, thus effectively defining the sensor length. The entire chip surface, with the exception of the contact pads and the sensitivity area, was passivated by a multi-layer insulator composed of 50 nm of Si_3N_4, 300 nm of tetraethyl orthosilicate, and 200 nm of phosphosilicate glass. This multilayer insulator was designed to withstand liquid environments and to

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avoid the propagation of pinholes in the passivation that could short-circuit the electrolyte with the contact lines.

The chip was combined with a microfluidic module (see Figure 5) with Ag/AgCl reference electrodes through which various solutions were injected [29]. All experimental samples operated in front-gating mode, where the V_{gs} voltage was applied between the electrolyte solution, the offset front electrode, and the source, while the back gate as well as the source were short-circuited [30]. This circuit with a grounded back gate prevents any spurious coupling between the electrolyte solution and the environment.

The geometric dimensions of one sensor, taking into account passivation, were 4.5 × 1.5 microns. The block of their three identical sensors occupied an area of 4.5 × 9.5 microns.
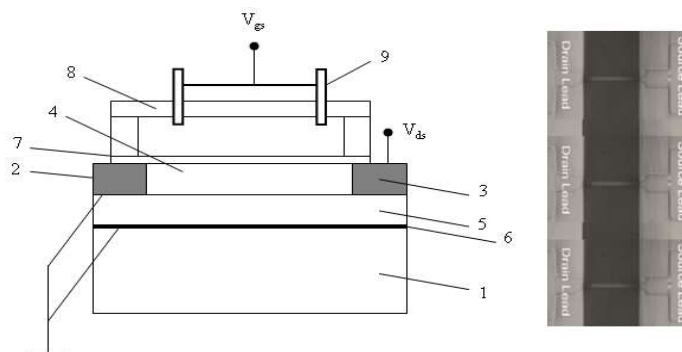
Figure 5 The longitudinal section of the transistor and the microfluidic module (left). Here, positions (1-6) are the same as in Figure 1, (7) silicon dioxide film, (8) 3M 9086 film, (9) Ag/AgCl electrode; right) SEM image of the FET block. Top view of the transistor with Lg = 1250 nm. The source and drain leads were passivated, while the body of the device was exposed.

4   Experimental Setup for pH Measurement

The surface of the chips was cleaned sequentially before the experiment by washing with ethanol/acetone/ethanol for 20 minutes each. In between, the chips were washed with deionized water and dried in nitrogen. The chips were then mounted with a microfluidic module. This was made on the basis of chemical resistant tape with a double coating of 3M 9086 and a thickness of 160 microns. The inlet and outlet tubes were hermetically inserted on top of the tape. A syringe pump was used to supply the solution to the microfluidics.

Solutions with different pH were interspersed with injections of 10 µM KCl. Each injection lasted 10 minutes at a fixed flow rate of 5 µL/min. Various pH solutions were prepared on the basis of a 10 mM phosphate buffer saline solution containing 100 µM KCl. The solutions were adjusted to the desired pH by adding either H_2SO_4 or NaOH, so that the difference in ionic strength of the solutions was negligible [31]. The I-V data samples were measured using an Agilent 4156C analyzer, which was used both in scan mode and in sampling mode, controlled by LabVIEW VIs and MATLAB scripts via the GPIB interface [32]. These measurements allowed us to determine the sensitivity to the change in pH (ΔpH) by changing the transistor current ΔIds.

5   Result and Discussion

Figure 6 shows the I-V data Ids (V_{gs}) at V_{ds} = 1.0 V of a nanotransistor with the following geometry: L_g = 1250 nm, W = 120 nm, t_S = 40 nm, and with frontal gating for solutions with different pH values. Here, we studied the process of sequential injection of solutions with an increase in pH at the same time intervals. In this experiment and the subsequent experiments, (i) the measurement error of the current I_D was equal to 10 nA; (ii) the measurement error of the pH was equal to 0.1; (iii) the influence of the parasitic resistance of the source and drain on the functioning of the sample was taken into account by extracting their values and compensating for the corresponding voltage losses [33].

In all cases, the sample operated similarly to a classic MOSFET [20]; the threshold voltage was ~0.46 V, and the subthreshold slope was less than 90 mV/dec. Here, the sequential administration of solutions with an increase in pH at the same time intervals was studied. Solutions with different pH values in contact with the frontal gate oxide induced a change in its surface charge as a result of the mechanism discussed above.

The surface of the front gate oxide becomes negatively charged when it is in contact with electrolyte solutions with pH values above its isoelectric point. The change in the surface charge affects the surface potential, which in turn changes the conductivity of the device at fixed control voltages [33]. The control voltages shift the transistor both well above the threshold (V_{gs}-U_{th}~1 V) and into saturation mode (V_{ds} = 1.0 V), thereby increasing the absolute value and linearity of the current response in ΔI_D/ΔpH coordinates as well as maximizing the dynamic range. For n-type devices, the drain current decreases with increasing pH, as more and more negative charges accumulate on the surface of the front oxide, thereby shielding the electrons in the channel [25]. The average voltage shift was about 34 mV/pH, which is consistent with other studies using SiO_2 as a gate dielectric [1,5,26,35-37].
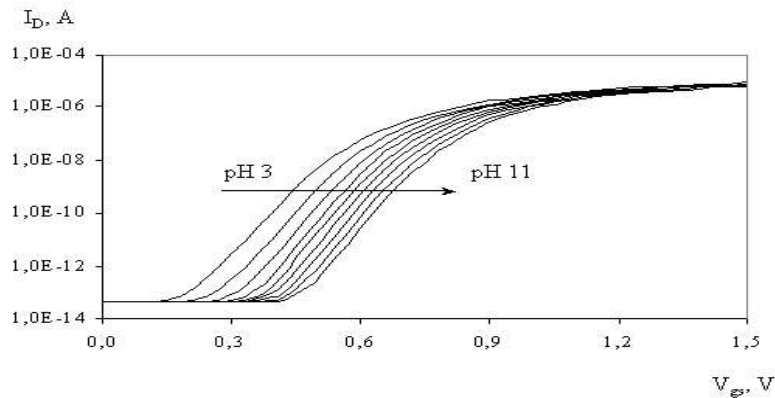
Figure 6 I-V data $I_D(V_{gs})$ at $V_{ds} = 1.0$ B for different pH.

The maximum sensitivity (38 mV/pH) was achieved at control voltages $V_{ds} = 2.0$ V and $V_{gs} = 1.8$, however, all experimental samples functioned stably at control voltages $V_{ds} = 1.0$ V and $V_{gs} = 1.5$ V. It should be noted that the behavior of the subthreshold current is determined by different mechanisms, both inside and outside the core of the device, but does not affect the sensitivity of the device as a whole [38].

For three identical transistors, we extracted the dependence of the current of the transistor in the saturation mode on the pH from the experimental data. The characteristic dependence of Ids (pH) (almost identical for the three samples) is shown in Figure 7, the slope of which determines the sensitivity to pH.
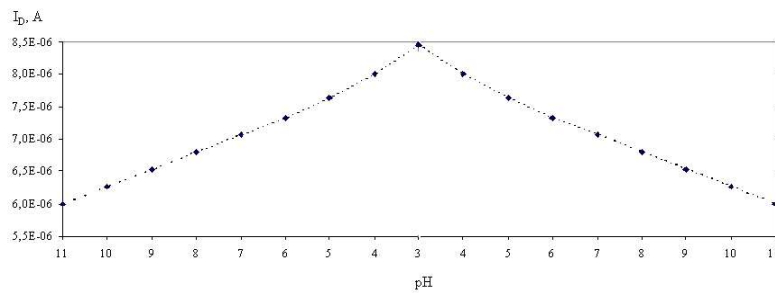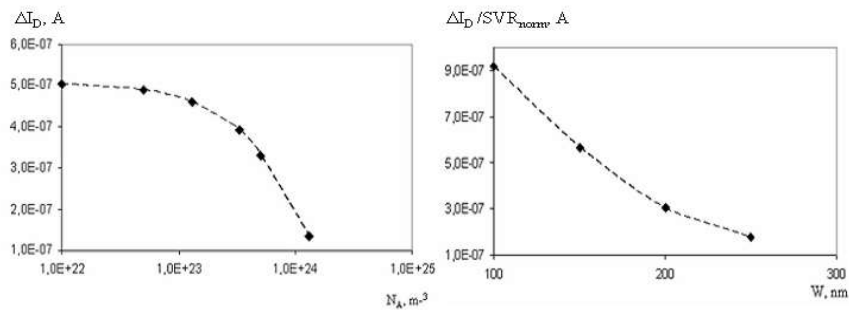

Figure 7 Dependence of $I_D(pH)$. Here, the symbols indicate the experimental points. The measurement error of the current I_D was equal to 10 nA.

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For a monotonic increase/decrease in the pH level, Figure 7 shows the $I_D(pH)$ dependences, which show that the sample current experienced a linear drift as a function of the pH gradient, which was not related to the pH change in any way [22,25].

Comparing the data obtained with recent studies where high-k dielectrics were used as gate oxide [39,40], we achieved some success, with current sensitivity at 40% (380 nA/pH) versus 31.7% and energy consumption at 85 μA at $V_{ds} = 1.0$ V and $V_{gs} = 1.5$ V versus 100 μA at $V_{ds} = V_{gs} = -2$ V. Obviously, with the selected power supply scheme, we lost voltage sensitivity by about one and a half times. However, by applying the double-gating method known in radio engineering, we will be able to repeat modern results in sensitivity close to the Nerst limit.

For the three samples under study, Figure 8 (left) shows the dependence of the change in the transistor current ΔI_D when changing ΔpH, depending on the doping concentration of the working area N_A. In the region of reduced doping (approximately to the value $N_A = 1 \times 10^{23}$ m^{-3}), the sensor response remained almost constant. As the doping level increased, the ΔI_D parameter decreased sharply. This behavior is associated with a change in the ratio of internal charges of the channel and external charges that are adsorbed from the electrolyte [6,22].

Figure 8 Dependence: (left) $\Delta I_D(N_A)$, (right) $\Delta I_D(W)$. Here, the symbols indicate the experimental points.

For the study prototype with $N_A = 1 \times 10^{22}$ m^{-3}, Lg = 1250 nm and t_S = 40 nm, Figure 8 (right) shows the dependence of the normalized sensor response ΔI_D/SVRnorm, where SVRnorm = SVR/SVRmax (see Figure 4), when changing ΔpH in accordance with Figure 8 (right), depending on the working width W.

The results showed that the normalized response ΔI_D to the change ΔpH increased with a decrease in the width W due to the greater conductivity of the transistor. This increase in electrical conductivity at smaller sizes was complemented by the

presence of pronounced angular effects characteristic of channels with high doping and a rectangular cross-section, in contrast to other cross-sections of the working areas [15,16]. It should be noted that the minimum resolution (ΔpH = 0.2) that can be obtained using a sensor with $N_A = 1 \times 10^{22}\, m^{-3}$, L_g = 1250 nm, W = 125 nm and t_S = 40 nm at V_{ds} = 1.0 V. In the case of a silicon dioxide surface this corresponds to a pH shift of ~0.8% at a supply power of less 1 μW. This value is more than an order of magnitude better than that of planar devices [26].

The simulation results indicated that the length L_g does not affect the sensitivity for the considered length range. The effect of the t_S fin height on the sensitivity can be attributed to second-order effects compared to the effect of the width W. The optimal topological parameters for pH detection were determined from the results of the experiments. It should be noted that when choosing parameters that do not affect the sensitivity of the sensor, one should be guided by the value of the signal-to-noise ratio [15,23,41], while taking into account the scaling of the measuring systems.

6   Conclusions

The electro-physical characteristics of 3D nanoscale low-voltage silicon sensors as surface charge detectors in an electrolyte medium were investigated. A three-gate configuration offers undeniable advantages over planar devices. The characteristics of the transistor were optimized depending on the topological parameters of the transistor and the level of control voltages using 3D modeling performed by the computer-aided design software package TCAD. Based on the obtained simulation results, a chip was manufactured on an SOI substrate based on self-aligning CMOS-compatible technological processes from top to bottom. It was established that thin structures with L_g = 1250 nm, W = 125 nm and t_S = 40 nm at V_{ds} = 1.0 V with a reduced level of doping have promising electrical characteristics: high relative sensitivity, high saturation current, subthreshold characteristic slope close to ideal, and low supply power. The use of transistor structures can be combined with a reduced noise level.

The considered methodology opens up an effective approach to scaling pH sensors, providing high resolution per unit of occupied area with minimal power consumption. This feature is of particular interest for integrated pH bio analytics based on CMOS technology. The results of this study provide useful recommendations for the development of nanowire sensors based on fin field-effect transistors that can be integrated into miniature low-power biosensor systems.

Acknowledgement

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