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ORIGINAL RESEARCH

Power factor correction stage and matrix zero voltage switching resonant inverter for domestic induction heating appliances

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Abstract

The technology of flexible cooking surfaces applied to domestic induction heating (IH) appliances offers several advantages that improve the experience of the users, not only because the safety or cleanness, but also due to the fast heating and flexibility. These cooktops have more challenging design requirements because of different mains connections, efficiency requirements, electromagnetic compatibility (EMC) standards, control complexity, and cost. In previous works, the use of a front-end power factor corrector (PFC) rectifier has been proposed to overcome these restrictions. In order to get a cost-effective implementation, this paper proposes the use of a front-end PFC stage and a matrix resonant inverter, which features zero voltage switching (ZVS), to achieve a reduced number of power devices, and get a high performance and reduced power losses in the converter. Finally, an experimental prototype with four outputs of 3.6 kW has been implemented to prove the feasibility of this proposal.

1 | INTRODUCTION

Flexible surfaces with several concentric coils or fully active surfaces [1–3] for domestic induction heating (IH) appliances significantly improve the final experience of the users because they allow the use of pots with different shapes and sizes in any position. All these advantages, along with the fast cooking, high efficiency, cleanness and safety, among others, improve the performance of typical IH cooking surfaces [4]. However, this technology has more challenging design requirements than the conventional IH cooking surface specifications due to additional requirements [5–7] such as higher efficiency and output power, or smaller space to allocate the power electronics, leading to higher power density specifications. Besides, electromagnetic compatibility (EMC) restrictions and power coupling issues are additional constraints because these surfaces can be powered from different mains phases using different connections. Finally, the cost of the coils and the power electronics is another relevant restriction to have into account.

The current limitations of domestic IH, in general, and the flexible surface technology, in particular, can be overcome by using an additional power conversion stage (Figure 1) to separate the IH inverters from the mains, as it has been previous discussed in [8–10]. This solution enables obtaining a good EMC performance [11–13] and decreasing the design constraints of IH inverters [14, 15]. Besides, the power factor corrector (PFC) stage merges the mains phases in the same bus, achieving a lower voltage ripple, avoiding using different electronics boards, and obtaining a relevant cost reduction. All these advantages provide additional benefits to domestic IH appliances. Furthermore, the current in the back-end inverters is decreased due to the increased bus voltage, decreasing consequently power losses in the power electronics and inductor system [16, 17].

Typical domestic IH cooking surfaces are usually composed of two to four cooking areas where the pan or the pot can be heated. However, flexible surface latest trends are leading to an increased count of windings that in the case of total active surfaces (Figure 2) can reach up to 50 coils. Considering that conventional topologies can power only a single load, new solutions become mandatory to properly power this increased number of loads in a cost-effective way. A straightforward implementation consists on using a micro-inverter per coil [18]. However, this solution leads to a costly implementation.

FIGURE 1 Induction cooktop for domestic application powered from a multi-phase mains connection

FIGURE 2 Fully active cooking surface

In order to find a balance between cost, performance, and control complexity, several multi-output power topologies have been proposed in the last years. Nowadays, there are two basic families of power converter topologies applied to multi-load systems.

On the one hand, configurations derived from the half-bridge or full-bridge topologies using electromechanical relays allow multiplexing several loads, as it is presented in Figure 3a [19]. In this case, the relays are periodically activated to power a single load, or a combination of them, during a certain period, achieving a cost-effective solution. However, it presents some drawbacks for the user, such as acoustic noise due to the relay activation or discontinuous heating of the cooking element, which can be perceptible by the user [20]. Besides, the output power control is limited in order to fulfill the flicker limits of the EMC regulations, and the mean time between failures (MTBF) of the converter is decreased due to the increased number of switching of the relays.

On the other hand, a cost-effective alternative is the use of multiple-output inverters. These converters can power several loads simultaneously and control the output power accurately using full solid-state implementations [5, 6, 21–23]. These advantages are achieved because additional power devices are placed at the cost of a more complex control. In this way, electromechanical relays can be removed from the design of the cooking surfaces, increasing their useful life and improving the user experience. In Figure 3b, a series resonant multi-inverter is shown. It consists of a common half-bridge inverter and an additional switch to activate or deactivate each load.

Finally, taking these multiple-output inverters as a starting point, a solution based on a matrix structure is proposed, allowing powering a high number of loads. In particular, this work proposes the use of these matrix topologies to get a multi-output inverter with a reduced count of power devices. In the past, a matrix zero current switching (ZCS) converter has been proposed [24]. However, the output power control is constrained to be frequency restrictions to avoid acoustic noise. For this reason, a zero-voltage-switching (ZVS) resonant matrix converter is preferred to perform this application [25]. This solution achieves a reduced number of power devices while ensuring high efficiency and proper power control in each coil. Unlike previous proposals, the proposed converter enables full output power control, ensuring the highest level of user performance and flexibility in any domestic IH appliances.

In this context, the main contribution of this work is the development of a two-stage converter composed of a front-end PFC and a matrix ZVS inverter using SiC MOSFET high-side transistor, providing a cost-effective solution for high-performance domestic IH cooking surfaces. This paper will cover the analysis and design of the converter, as well as the experimental verification using a four-load IH prototype.

The remainder of this paper is organized as follows. Section 2 presents the topology and the modulation strategies of the proposed converter, focusing on its main stages: the front-end PFC rectifier and the ZVS multiple output resonant inverter. Section 3 explains the matrix inverter operation and control, including its main states and equations. Section 4 presents the experimental results and waveforms, which have been obtained by means of a 11-kW and four-output implemented prototype. Section 5 discusses and compares the benefits of this proposal and Section 5 summarizes the main contributions of this work.

2 | PFC AND MATRIX CONVERTER

2.1 | PFC stage

In order to get a proper harmonic distortion (THD) and power factor (PF), controlled rectifiers are necessary to develop the front-end PFC stage instead of non-controlled rectifiers [26–28]. Despite the control of these converters is more complex, the achievable power density is higher, making them an interesting choice in many applications. The most interesting topologies for domestic IH are the boost topologies, because they get a higher voltage in comparison with buck topologies, decreasing the current in the IH inverters and coils, improving consequently the efficiency. In this way, [9] proposes a multi-phase stage. This front-end PFC merges the mains phases in the same bus voltage, v_b, getting a good PF and a decreased THD of the mains currents.

In Figure 4, a three-phase PFC topology featuring four half-bridge branches is shown. The switching devices are

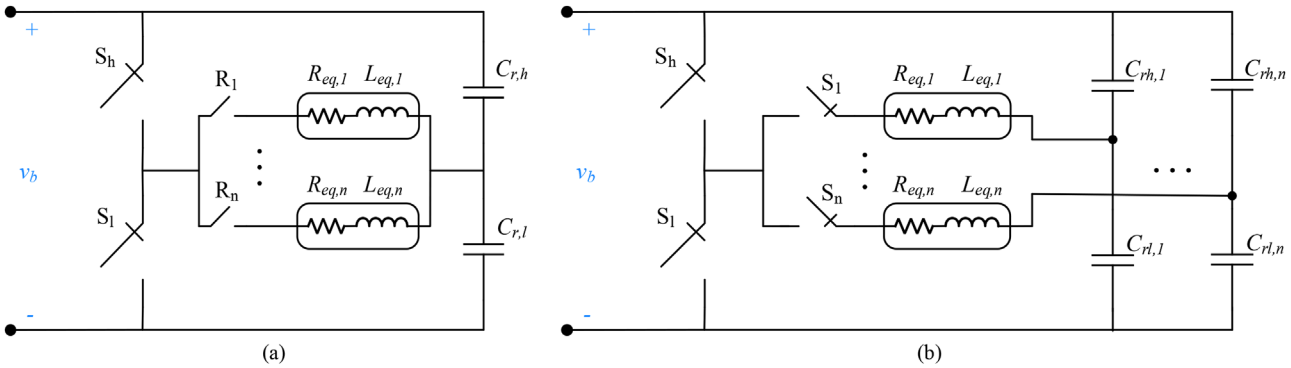

FIGURE 3 Multi-output power inverters: (a) Half-bridge resonant inverter using electromechanical relays, R_i, $i \in [1, n]$, to power n resonant loads, and (b) half-bridge series resonant multi-inverter using an additional semiconductor device per load, Si

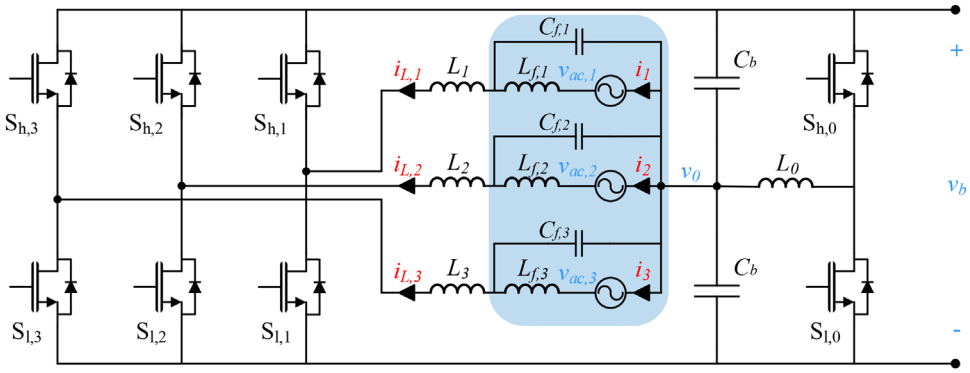

FIGURE 4 Boost controlled PFC rectifier for up-to-3-phase domestic IH appliances. IH, induction heating; PFC, power factor corrector

implemented using MOSFETs, $S_{h,i}$ and $S_{l,i}$ on the high and low side, respectively, $i \in [0, 3]$. The mains phase current, i_i, $i \in [1, 3]$, is controlled by short-circuiting the boost inductor, L_i, with the mains phase voltage, $v_{ac,i}$, the bus voltage, v_b, or the voltage of middle point of the split bus capacitor, v_0. A LC filter, $L_{f,i}$ and $C_{f,i}$, is used to remove the medium frequency ripple of the current through the boost inductor, $i_{L,i}$, getting a smoothed mains current. Besides, the split bus voltage is filtered using two capacitors, C_b. Finally, to get a well-balanced split capacitor, an additional half-bridge branch is placed along with the balancing inductor, L_0. Furthermore, this additional branch enables not balanced connections, such as single-phase or two-phase connections, because the mains phase currents can return through this path. This is a desired feature to be able to adapt the proposed architecture to different mains networks.

In order to perform the PFC function, different modulation strategies can be implemented [27–35]. However, each one of these strategies has some advantages and disadvantages that can ease or complicate its implementation according to the application area, control complexity, cost, device ratings, efficiency, EMC issues, or the operating frequency. For domestic IH applications, the hard switching fixed frequency continuous conduction mode strategy (Figure 5) is preferred due to the fact that it avoids zero-cross distortion, acoustic noise, and it operates at fixed frequency synchronized with the back-end IH inverter.

2.2 | Matrix ZVS inverter

In Figure 6, the matrix ZVS resonant inverter with a single-vector configuration is shown, using a single high-side switching device, T_h, and four low-side devices, $S_{l,j}$, $j \in (1, 2, 3, \text{and } 4)$. The high-side switch is a silicon carbide MOSFET whereas the low-side transistors are silicon MOSFETs with parallel diodes, $T_{l,j}$ and $D_{l,j}$, respectively. Additional parallel and series diodes, $D_{h,j}$ and $D_{s,j}$, respectively, are placed along with the high-side switch to allow inverse current and to block voltage, enabling an accurate regulation of the overall power in the output IH loads.

The control signals, $g_{l,j}$ and g_h, are used to activate the low-side and the high switches, respectively. This converter can control the power of up to four IH loads, which are allocated in the middle of the inverters and the bus capacitor, getting the half of the voltage, v_n. The loads are composed of the electrical equivalent parameters of coils, that is, their series inductance, $L_{eq,j}$, and resistance, $R_{eq,j}$, and a capacitor, $C_{r,j}$, on series to get resonant behaviour.

Using this topology, the count of power devices is decreased in comparison with a conventional inverter because a unique high-side transistor is required. In contrast, a half-bridge converter needs eight switching devices to effectively power four loads. However, using the matrix inverter, only five controlled power devices are necessary, also decreasing the

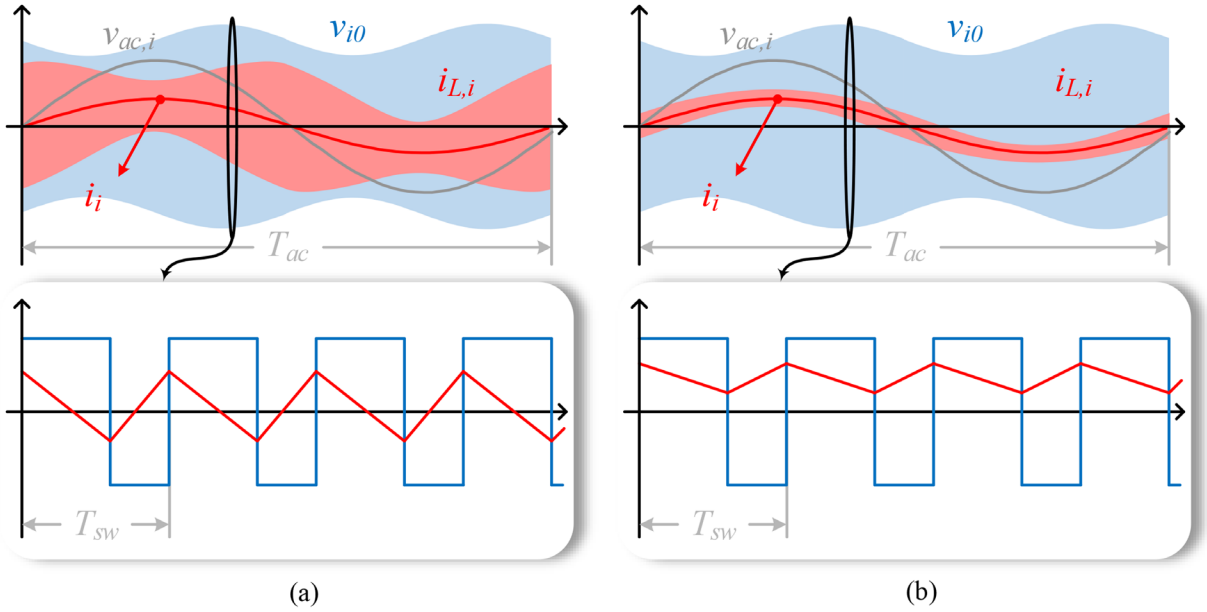

FIGURE 5 Fixed frequency continuous conduction mode modulation strategies of the 3-phase PFC rectifier for domestic IH applications: zero voltage switching (a) and hard switching (b)

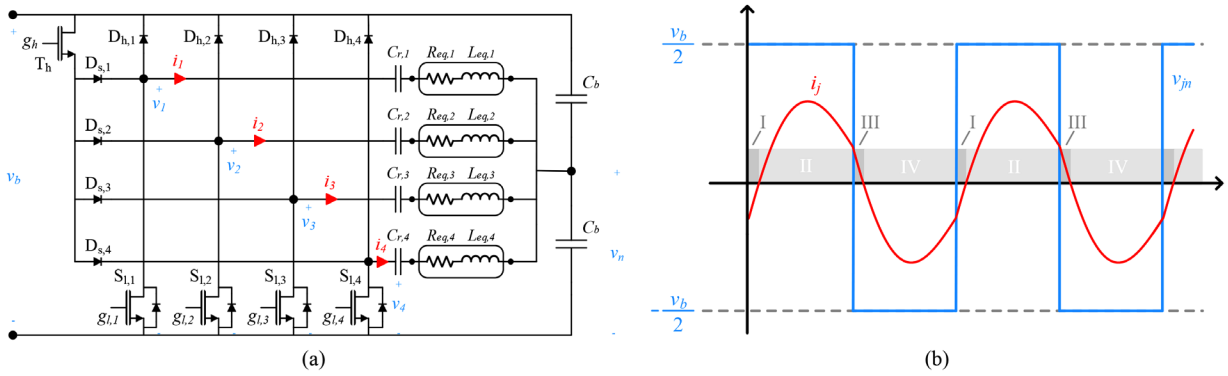

FIGURE 6 Topology (a) and main waveforms (b) of the proposed matrix inverter

quantity of other devices, such as activation drivers or DC—DC converters.

On the contrary, the main disadvantage of the proposed matrix inverter is that the single switch manages the current through all loads. In order to improve the conduction capabilities, silicon carbide technology has been proposed in this transistor, leading to a reduction of power losses and minimizing the influence of the temperature.

2.3 | Modulation strategies for controlling matrix inverter

Pulse density modulation (PDM) control and square wave (SW) control are the proposed strategies to manage the output power (Figure 7). All power transistors are switched at f_{sw} frequency, 0.5 fixed duty cycle, and zero phase-shift. In this way, the four low-side switches are activated simultaneously, avoiding inter-modulation noise between the different branches as it occurs in a typical half-bridge topology. This represents an additional advantage for the proposed topology.

The operating frequency is selected according to the necessary power in the most limiting load, achieving ZVS switching in all transistors. The low-side transistor of a load remains deactivated when this one is not to be powered. Normally, SW control is applied to the most restrictive load to supply the required power, whereas the power delivered to the other IH loads is managed using the PDM strategy at the same frequency.

3 | CONVERTER OPERATION AND CONTROL

Figure 6b shows the activation states and the main waveforms of the j load, voltage, v_{jn}, and current, i_j. Taking into account that $C_b >> C_{r,j}$, the bus voltage is evenly split between the bus

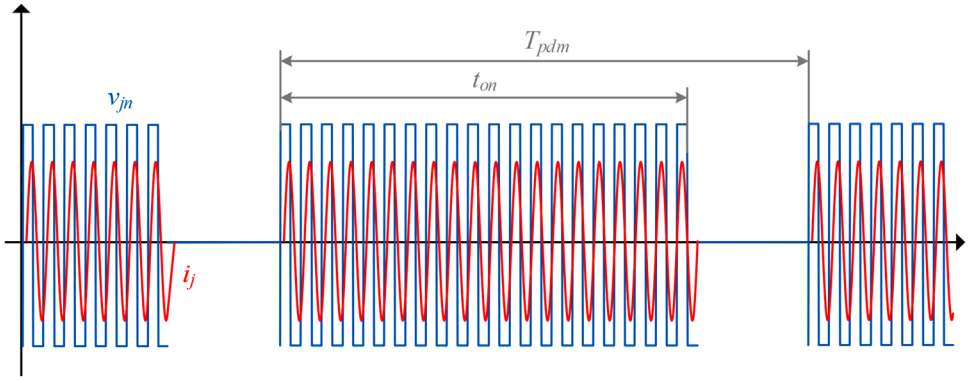

FIGURE 7 A representation of the mains waveforms of the pulse density modulation strategy

capacitors. Therefore, the load voltage according to the activation state is defined as

$$v_{jn} = \begin{cases} \frac{v_b}{2}, \text{ state : I and II} \\ -\frac{v_b}{2}, \text{ state : III and IV} \end{cases} \quad (1)$$

The activation state of transistors defines the voltage that is applied to the load. This is the half of the bus voltage, as it is shown in Equation (1).

The matrix inverter is designed to work above the resonant frequency of the load, getting an inductive behaviour and, consequently, assuring ZVS switching. When the operating frequency is close to the resonant frequency, the load behaves similarly to a resistive load, getting a sinusoidal current waveform in phase with the applied voltage. In this situation, the maximum power is delivered, $P_{o,j}$. The value of the maximum power can be approximated using the first harmonic approximation as

$$P_{o,j,max} = \frac{2v_b^2}{\pi^2 R_{eq,j}} \quad (2)$$

Moreover, when PDM strategy is applied, the effective delivered power is obtained using the activation time, t_{on}, and the period, T_{pdm}, as

$$P_{o,j} = \frac{2v_b^2}{\pi^2 R_{eq,j}} \frac{t_{on}}{T_{pdm}} \quad (3)$$

The configuration sequence of the proposed matrix inverter topology is depicted in Figure 8 focusing on the j load. After the deactivation of the low-side transistor, $T_{l,j}$, the state I starts and the high-side parallel diode, $D_{h,j}$, is activated in order to allow current flow. When the current direction changes, the state II starts. Then, the high-side MOSFET, T_h, is activated getting ZVS switching and the current flows through of this transistor and the series diode, $D_{s,j}$. When this device is deactivated, the low-side parallel diode, $D_{l,j}$, is activated to allow the current flow, and a negative voltage is applied over the load. This is the state III. Finally, when the load current crosses zero again, the direction changes, and the low-side MOSFET, $T_{l,j}$, is activated, achieving ZVS condition in this power device and starting state IV. It is important to note that reverse current can flow through the low-side MOSFET during state III, decreasing conduction losses.

In order to ensure ZVS conditions in the whole operating range, the minimum operating frequency of the converter is selected to obtain the maximum desired power in the most restrictive load, close to the resonant frequency of this load. The power delivered to the loads can be decreased by using the PDM strategy or increasing the operation frequency. In this way, ZVS conditions are guaranteed in the complete operation range.

4 | EXPERIMENTAL RESULTS OF THE CONVERTER

4.1 | Matrix stage implementation

The experimental results are obtained using the matrix prototype that is shown in Figure 9. It is designed to deliver 3.6 kW per load, and 11-kW overall power using its four outputs, at 800-V bus voltage.

Two DF11MR12W1M1_B11 EasyPACK modules from Infineon composed of 50-A and 1200-V SiC MOSFET and diodes are used to implement the low-side switches and high-side diodes. Four fast recovery 50-A and 1200-V diodes from IXYS in SOT-227 packages are used to implement the series diodes whereas the IXFN50N120SK SiC MOSFET from IXYS is selected for the single high-side power device. It features 1200-V, 48-A, and 50-mΩ in an isolated baseplate SOT-227 package too.

The selected drivers for activating the controlled power devices are the 1EDI60N12AF from Infineon whereas the bus capacitor is composed of two 450-μF aluminium electrolytic capacitors from Wurth.

The experimental prototype is completed with voltage and current measurements. These parameters are measured using voltage dividers and shunts, respectively. The 1-MSPS and 12-Bit ADCS7476 from Texas Instruments has been selected to perform the analog to digital conversion, whereas the control

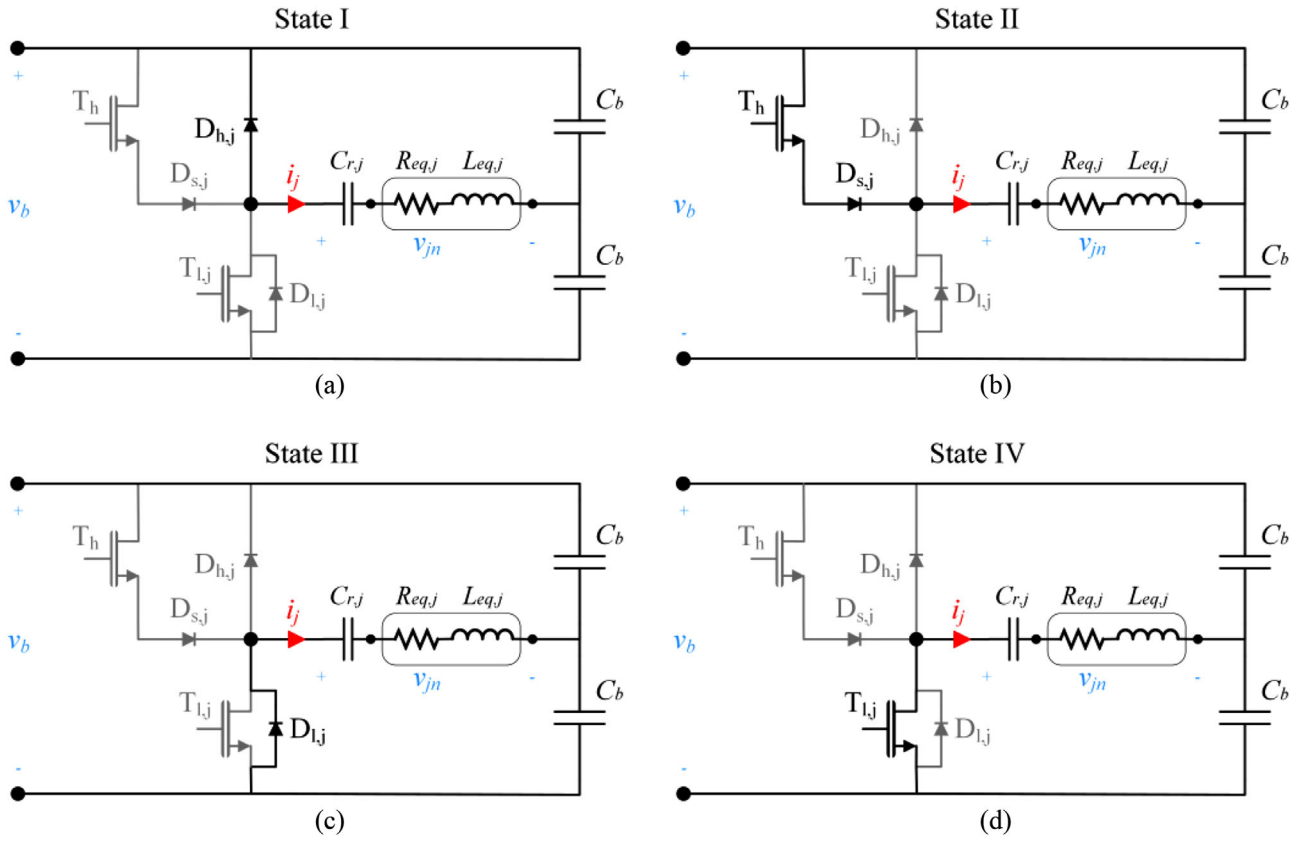

FIGURE 8 Configuration sequence of the matrix ZVS resonant inverter: (a) state I, (b) state II, (c) state III, and finally, (d) state IV. ZVS, zero voltage switching

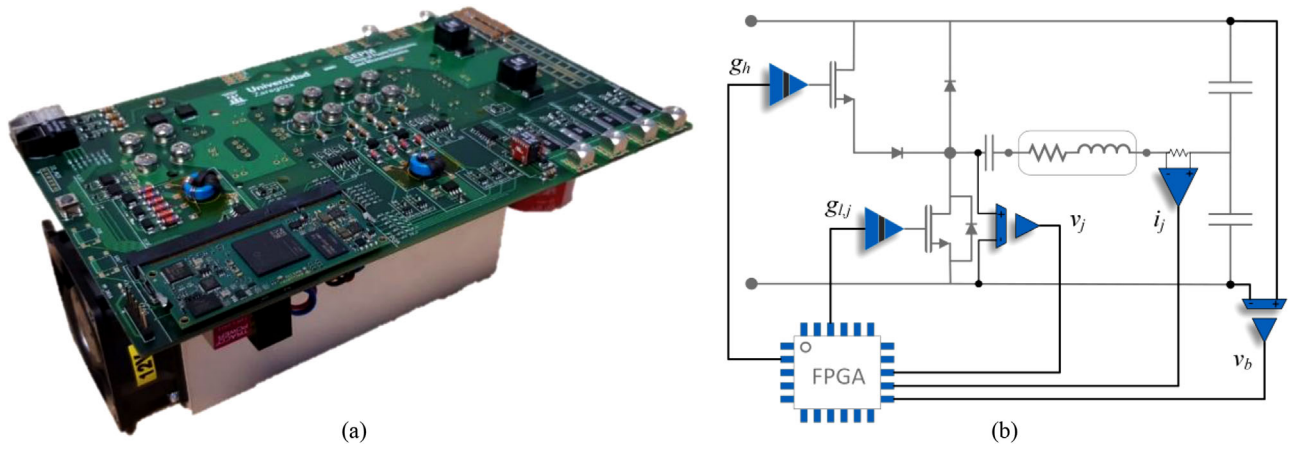

FIGURE 9 (a) 11-kW and four-output matrix ZVS converter for domestic IH applications. (b) Detail of the schematic of the circuit control including isolated drivers, voltage measurements using resistive dividers, and current measurements using shunt resistance

of the prototype is performed using a Zynq FPGA from Xilinx. This control architecture is used for research and verification purposes, whereas the final implementation will feature a combination of microprocessor and ASIC which has been successfully used in commercial products in the past. Besides, the experimental converter is operated from the PC using a visual basic application and optical fibre to provide isolation. Table 1 sums up the main converter design parameters.

4.2 | Experimental results

In this subsection, the full converter and its modulation strategies have been tested, verifying the proper operation of the front-end PFC stage along with the implemented back-end IH matrix inverter. The converter efficiency has been measured, reaching 97.6% maximum efficiency at maximum power (Figure 10). Firstly, the prototype has been tested at maximum

TABLE 1 Converter design parameters

Parameter	Value
IH loads	4
Input mains phases, n	1, 2, or 3
Bus voltage, V_b	800 V
Maximum load power, $P_{o,j,max}$	3.6 kW
Total output power, P_o	11 kW
Operating frequency, f_{sw}	20–150 kHz

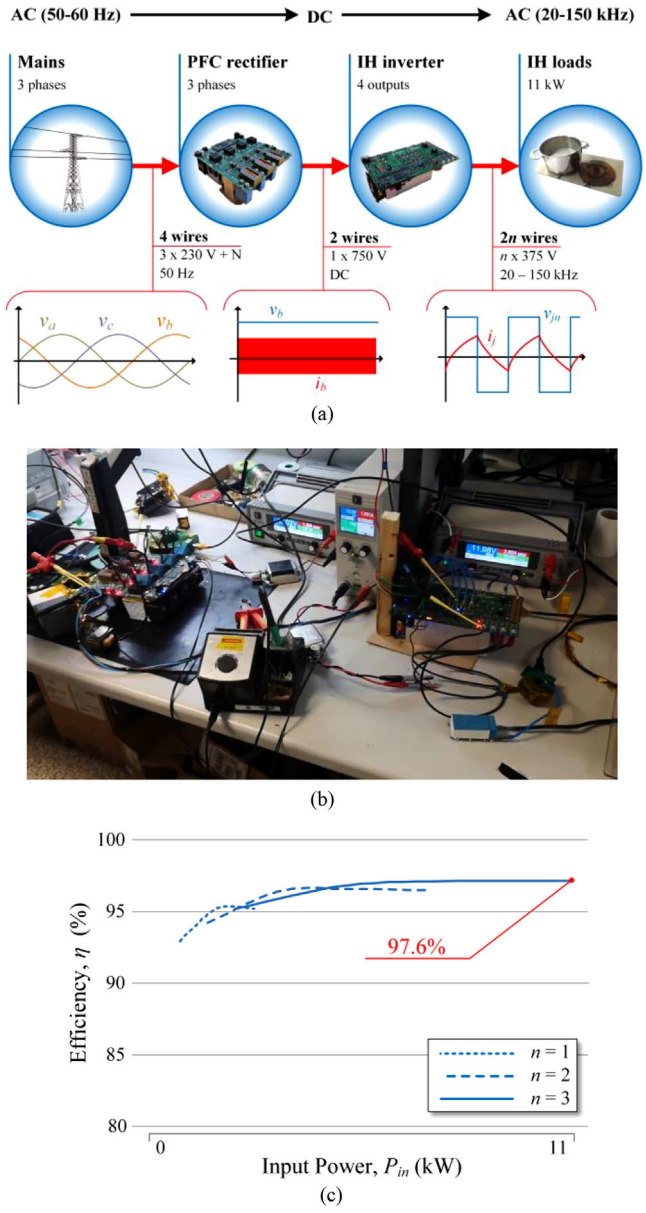

FIGURE 10 Experimental prototype: (a) Block diagram of the experimental implementation of the proposed converter, including the front-end PFC rectifier stage and the matrix ZVS inverter; (b) experimental set-up of the converter including both stages; and (c) efficiency of the converter for different number of activated input mains phases, n

power, using a single IH load, a 750-V bus voltage, and paralleling the four outputs of the prototype. The load has been custom made using two circular 21-cm inductors on series and a pot. The load is composed of a 10.5-Ω equivalent resistance and a 57-μH equivalent inductance. A 123-nF series resonant capacitor has been placed to obtain the maximum desired power at the operating frequency, that is, 63 kHz. The main waveforms of this operating point are shown in Figure 11. The prototype is delivering 11 kW, 2.75 kW per output, keeping a suitable temperature in electronics devices and heatsink, that is, 58°C. The operating frequency is close to the resonant frequency of the load and, for this reason, the waveform of the IH load current is sinusoidal. More in detail, the operating frequency is slightly higher to get an inductive load and achieve ZVS switching in the inverter. The experimental measurements prove the feasibility of the topology and the suitable operation of the implemented prototype.

Secondly, in order to verify the modulation strategies of the matrix topology, two coils and two pots with different materials have been used. The equivalent parameters are 145-μH inductance and 31-Ω resistance using A material, and 120-μH inductance and 25-Ω resistance using B material. A 100-kHz resonant frequency is obtained by using 22-nF resonant capacitors. The main waveforms measured at 100 and 120-kHz operating frequency are depicted in Figure 12. In the first example, the load with A material is full active, obtaining 2.2-kW power, whereas the load with B material is half active using the PDM strategy and obtaining 1.9 kW. The experimental waveforms of the current show that the B-material pot is closer to the resonant frequency. In the example of Figure 12c, the loads are powered with 1 kW and 750 W, respectively, working at 120-kHz operating frequency.

Finally, two additional loads, C and D, have been included using 22-nF resonant capacitors in order to test all outputs of the implemented prototype. All the load currents are shown in Figure 13 with the converter operating at 110 kHz. A load is fully active whereas the remaining ones are 33% active using PDM strategy. Different periods, T_{pdm}, have been used to prove the feasibility and the capabilities of the proposed modulation strategies to control the output power. It is important to remark that both Figures 12 and 13 show operation above the resonant frequency, that is, inductive region, ensuring ZVS soft-switching.

5 | DISCUSSION

This paper has proposed a multiple-output series resonant inverter with PF correction capability for high-performance IH appliances. The main benefits of the proposed topology are derived from the multi-output structure, which reduces the number of power devices and provides a versatile implementation, and the higher bus voltage, which increases efficiency. As a consequence, the main benefits of the proposed approach are reduced EMC issues in high power due to improved PFC stage, improved control due to controllable low-ripple bus voltage

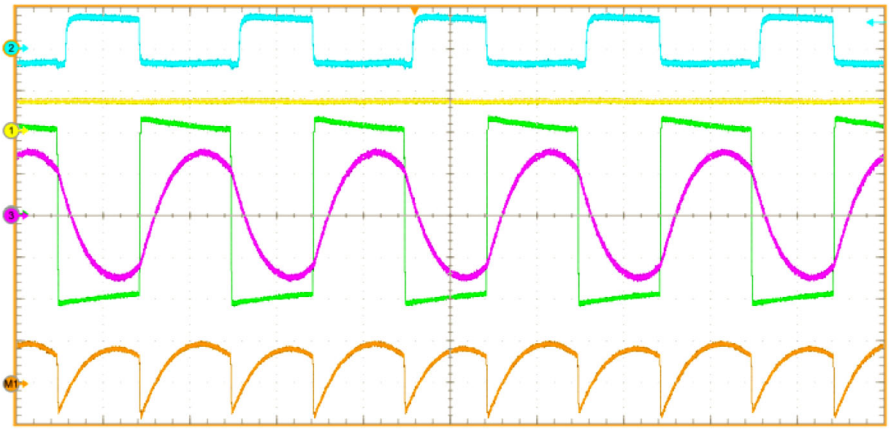

FIGURE 11 Main waveforms of the matrix IH inverter powering a domestic IH load. The converter is operating at maximum power, 11 kW and 100-kHz frequency. From top to bottom: low-side control signal, g_1 (20 V/div, blue), voltage of the medium point of the split capacitor, v_n (500 V/div, yellow), load voltage, v_{jn} (200 V/div, green), load current, i_j (30 A/div, pink), and output power, p_o (20 kW/div, brown). Time: 5 μs/div

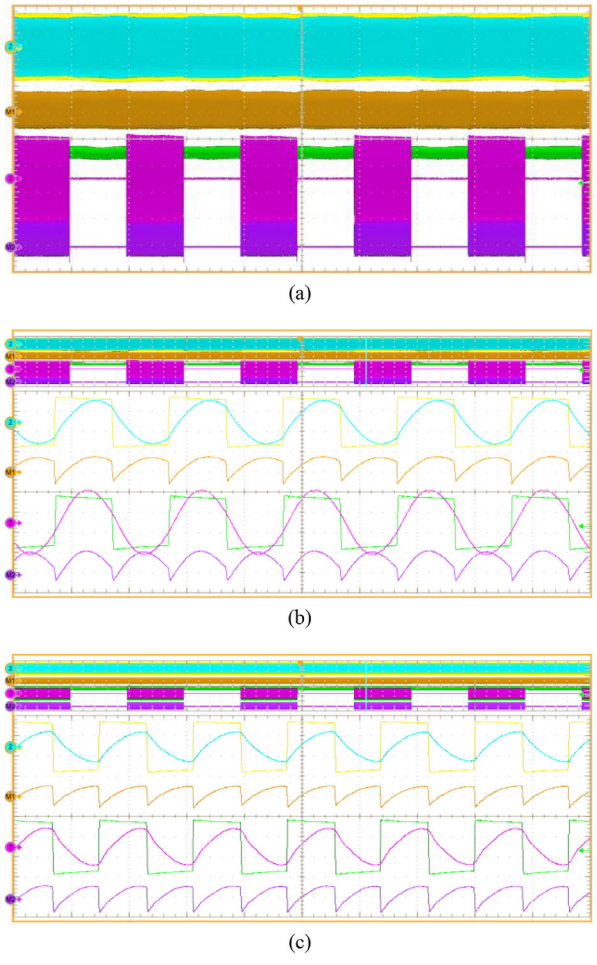

FIGURE 12 Waveforms of the converter powering two IH pots with different materials, A and B. The operating frequency is 100 kHz (a) and (b), and 120 kHz (c). From top to bottom: A-pot load voltage, v_{1n} (300 V/div, yellow), A-pot load current, i_1 (10 A/div, blue), A-pot output power, p_1 (5 kW/div, brown), B-pot load voltage, v_{2n} (300 V/div, green), B-pot load current, i_2 (10 A/div, pink), and B-pot output power, p_2 (5 kW/div, purple). Time: 10 ms/div (a), 5 μs/div (b), and 5 μs/div (c)

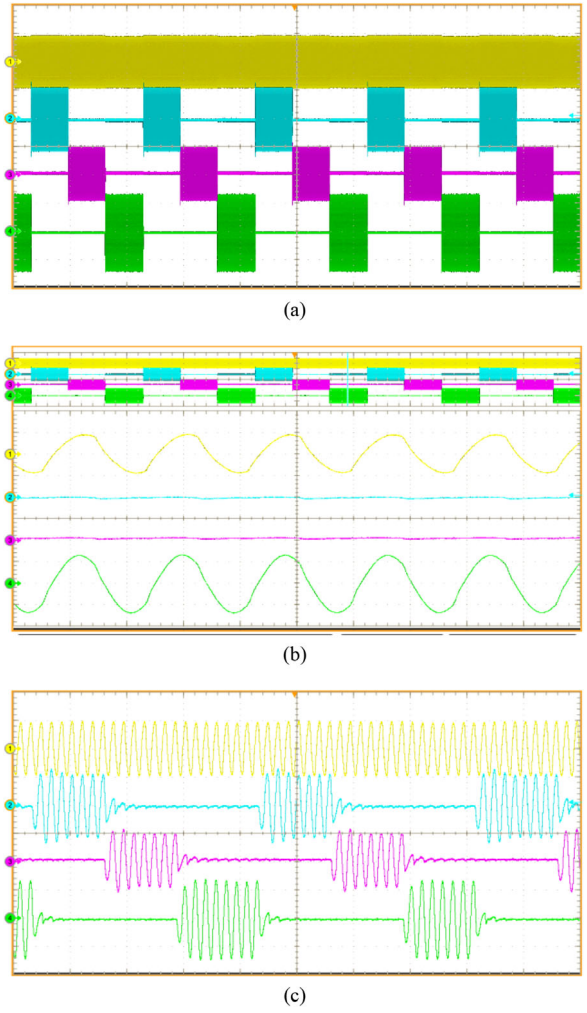

FIGURE 13 Main waveforms of the matrix IH inverter powering four domestic IH loads with the converter operating at 110 kHz using a 20-ms PDM period (a, b), and 200-μs PDM period (c). From top to bottom: A load current, i_1 (10 A/div, yellow), C load current, i_2 (10 A/div, blue), D load current, i_3 (10 A/div, pink), and B load current, i_4 (10 A/div, green). Time: 10 ms/div (a), 5 μs/div (b), and 50 μs/div (c)

TABLE 2 Comparison with state-of-the-art domestic induction heating power converter implementations

Topology	PFC	#Load	Power (load/total)	Devices (transistor/diode)	Peak efficiency
Proposed: PFC + matrix resonant inverter	Yes, three-phase	4	3600/11,000 W	13/8	97.6%
Soft-switching PFC + inverter [14]	Yes, one-phase	–	– /2500 W	1/8 + inverter	94.5% (only PFC)
Bridgeless ZVS ad-ac converter [36]	Yes, one-phase	1	3000 W	2/4	94%
Series-resonant multi-inverter [5]	No, passive	6	600/3600 W	8/4	97% (only DC–AC)
Multi-resonant half-bridge [2]	No, passive	2/3	700 /1200 W	2/4	–
Matrix ZCS/ZVS converter [24]	No, passive	24	800/3600 W	10/48	–
Three-switch multi-load class-D inverter [3]	No, passive	3	2500/2500 W	3/4	–
Dual-output full-bridge [23]	No, passive	2	–/3200 W	6/4	–

when compared with state-of-the-art high-ripple topologies, and lower current through the devices due to the higher bus voltage, which leads to improved efficiency. Besides, the proposed structure uses a common PFC stage, enabling the design of high-power cost-effective multi-load systems.

When compared with state-of-the-art solutions, the proposed topology opens a new design scenario for high-power multi-load systems. As is shown in Table 2, when compared with other state-of-the-art solutions, the proposed converter represents a clear step-forward in the high-performance high-power multi-load IH appliance area. The proposed converter takes advantage of a high-power high-efficiency design to offer the highest output power and efficiency in the domestic area. Besides, the matrix implementation allows us to minimize the required number of power semiconductors, enabling a cost-effective implementation. Despite that a direct comparison is not easy due to different design constraints, the proposed converter clearly shows its strengths in terms of maximum power, performance, and implementation cost.

6 | CONCLUSIONS

In this work, a multiple-output converter along with a front-end PFC rectifier has been proposed for domestic IH applications. On the one hand, the PFC stage enables a common and low-ripple bus voltage, while ensuring a good EMC performance and decreasing the control requirements of the back-end IH inverter. On the other hand, the matrix ZVS resonant inverter and its modulation strategies allow a relevant reduction in control power devices, while ensuring the full power control and allowing a notable cost reduction, significantly improving the performance of the power converter.

The feasibility of the proposed converter has been proved with the implementation of an 11-kW and four-output prototype. The experimental results using different IH loads and control parameters demonstrate the proper operation of the proposed converter. As a conclusion, the combination of a PFC stage and a matrix ZVS resonant inverter is a high-performance and cost-effective solution to improve modern IH appliances. As a conclusion, the combination of a PFC stage and a matrix ZVS resonant inverter is a high-performance solution to improve modern IH appliances, and the prototypes addressed in this work lay the groundwork for cost-effective implementations for commercial purposes.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

Data available on request from the authors.

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