SoC-based In-Cycle Load Identification of Induction Heating Appliances

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***Abstract*—The equivalent load of an induction hob is strongly dependent on many parameters such as the switching frequency, the excitation level, the size, type and material of the vessel, etc. However, real-time methods with the ability to capture the variation of the load with the excitation level have not been proposed in the literature. This is an essential issue as most of the commercial induction hobs are based on an ac bus voltage arrangement. This paper proposes a method based on a phase sensitive detector that offers an online tracking of the equivalent impedance for this type of arrangements. This algorithm enables advanced control functionalities such as clustering of vessels, material recognition and premature detection of ferromagnetic saturation, among others. After simulation and experimental validation, the method is implemented into a prototype with a system-on-chip (SoC) to verify its real-time behavior. The proposed approach is applied to different real-life situations which prove its great performance and applicability.**

***Index Terms*—Home appliances, Induction heating, Load identification, System-on-chip (SoC).**

I. Introduction

INDUCTION heating has been used in many fields, from industry [1], [2] to domestic applications [3], during the last decades. Domestic induction heating (DIH) has precisely experienced a noticeable growth due to its implicit efficiency, cleanness and security compared to the traditional heating methods (resistive and gas) [4]. However, one of the drawbacks of this heating technology is its great dependence on the vessel features [5], [6], that depends on the user choice. Moreover, the interaction of the user with the vessels entails a huge number of unpredictable scenarios.

The equivalent load of the system, which represents the electromagnetic interaction between the inductor and the ferromagnetic material of the pot, is usually modeled as a resistive-inductive ($R-L$) series circuit [7], [8]. These two variables depend on many parameters: the switching frequency, the temperature, the pot type and its material, misalignments and distances between the inductor and the pot, the magnetic flux density, etc.

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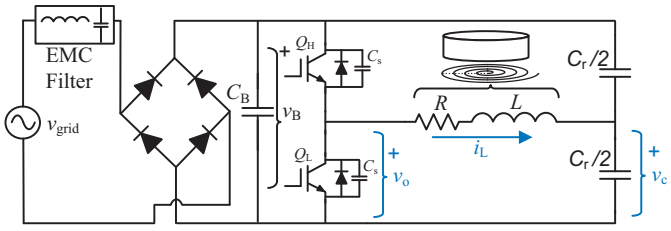


Fig. 1. Simplified schematic of the HBSRI.

The magnetic flux density, B, is the response of the ferromagnetic material to the magnetic field strength, H, generated by the inductor:

$$B = \mu(H)H, \tag{1}$$

where $\mu(H)$ is the magnetic permeability of the material and, as it can be noticed, depends on H which, in turn, also depends on the load current, i_{L}.

One of the most used topologies in this type of appliances is the half bridge series-resonant inverter (HBSRI). The main reason lies in its good ratio between performance and number of components [9]. A simplified schematic of the mentioned topology is shown in Fig. 1. The mains voltage is full wave rectified and filtered with a bus capacitor that is designed to allow a big ripple in order to obtain a power factor close to one, so avoiding the cost of additional power electronics [10]. The resulting voltage is called bus voltage, v_{B}.

The power supplied to the load is usually controlled by varying the duty cycle, D, and the switching frequency, f_{sw}, whose values span from 20 to 75 kHz. Since a relatively wide range of f_{sw} is available to control the power, the duty cycle is commonly kept constant at 0.5, and power density modulation (PDM) strategies are applied when the required power is less than the one supplied at maximum switching frequencies.

According to a recent paper [11], the impedance parameters present a significant variation with the excitation level. Theoretically, if a dc bus voltage and steady-state conditions are considered, the excitation level applied to the load would be constant, and so would be the equivalent impedance. However, when v_{B} is an ac wave, the amplitude of the voltage drop of

the load, v_{L}, and its current, i_{L}, continuously change with the alternating bus voltage, meaning that the excitation level applied to the load also varies. This could be avoided, for instance, by generating a dc bus through expensive power factor correction (PFC) stages [12]. Although technically possible, this type of approaches would strongly raise the cost of the home appliance. Therefore, for cost reasons, it is preferred to keep an ac bus voltage, even if this leads to a continuously varying impedance due to the variable excitation level [11].

Given the great variability of the system loads in the context of DIH, identification algorithms seem to be of great value in this application. For this reason, several methods regarding certain class of load identification have been reported in the literature [13]–[20]. For instance, in [13] a recursive least-squares (RLS) algorithm is proposed, but the computational burden of such math-intensive algorithm is quite significant. A different approach was proposed in [14], where a first-harmonic identification of the load parameters is presented. Both time-domain and frequency-domain approaches [13], [14] provide a single impedance value per bus period, obtaining an averaged value but providing no information about the variation of the load with the excitation level.

Machine learning has also been applied to implement a detector of sizes and types of vessels [15]. The algorithm is based on the spectral analysis of the output voltage and the load current and on the power factor of the load. This algorithm is not based on a first-harmonic approach, but on the first four harmonics of the waveforms. Nevertheless, the authors only apply the algorithm at a predefined switching frequency and over 1 ms, what may interrupt the normal cooking process and only gives local information of the load at a restricted and short interval of the bus period. Moreover, this algorithm does not provide a continuous identification and, in the proposed implementation, the identification of a single pot takes a long computing time (half a bus cycle).

Another noteworthy application is hardware in the loop (HIL), which is a widely used tool in domestic induction heating (DIH) [21], [22]. In this application, a real-time identification may be suitable for a more convenient validation of new software and hardware designs. For instance, in [16] an online identification of the load is used to estimate the power converter efficiency and hard-switching conditions. However, it does not take into account the variation of the load with the excitation level, what may lead to unrealistic values due to a smoothed and averaged information.

Additionally, phase-sensitive detector (PSD) algorithms are reported in the literature to identify the load [17], [18]; they show the variation of R and L with the switching frequency and with different pots, and they can even detect events like pot removal. Nevertheless, as in [13], [14], only one value of the $R-L$ parameters is obtained per bus cycle.

As it can be noticed, great effort has already been made to identify the equivalent load and even the pots because this is a tracked milestone by DIH manufacturers. Unfortunately, the equivalent impedance varies with the excitation level in the considered ac bus voltage arrangement, and none of the methods already proposed in the literature [13]–[20] is able to capture this continuous impedance variation as they only provide a single and averaged value of the $R-L$ parameters per bus cycle. A continuous tracking of the impedance variation with the excitation level would be desirable in order to extract insightful information about the induction vessel placed by the user. For instance, more advanced control functions such as clustering of vessels, material recognition, prediction of ferromagnetic saturation and underlying information about total harmonic distortion of the grid current, among others, would only be possible with an in-cycle load identification algorithm.

This work aims to develop such algorithm that provides a continuous tracking of the first-harmonic impedance at any switching frequency, no matter what the excitation level is and without interrupting or affecting the cooking process. This algorithm is supposed to provide new information about the load, to enable the possibility of applying advanced control functionalities and to open new research lines related to electromagnetic compatibility. After simulation and validation, the method is finally implemented in a prototype with a system-on-chip (SoC).

The rest of the paper is organized as follows. In Section II the DIH application is further explained. The proposed method, as well as its real-time implementation, is presented in Section III. The prototype and the experimental results are shown in Section IV. Then, in Section V real-time applications and use cases of the proposed algorithm are presented. Finally, the main conclusions are drawn in Section VI.

II. The induction heating application

First-harmonic approximations are extensively applied to the study of resonant inverters [8], [23], [24]. Moreover, for relatively high values of the quality factor, Q, of the load (as it is common in DIH), the fundamental harmonic of the inverter signals is the main contribution. Additionally, the information of the load variation with the excitation level is expected to give more insightful information about the load than considering a greater number of harmonics because the variation of the excitation level is more related to the physics behind the response of the materials of the pots [11]. For these reasons, the proposed method is focused on a first-harmonic approximation.

Let $x(n)$ be a discrete-time signal with period N. Its discrete-time Fourier series (DTFS) coefficients for the h^{th} harmonic are:

$$\begin{aligned}\mathbf{X}(h) &= \frac{1}{N}\sum_{n=0}^{N-1}\left[x(n)e^{-\mathrm{j}\frac{2\pi hn}{N}}\right] = a_h - \mathrm{j}b_h \\ &= \frac{1}{N}\sum_{n=0}^{N-1}\left[x(n)\left(\cos\left(2\pi\frac{hn}{N}\right) - \mathrm{j}\sin\left(2\pi\frac{hn}{N}\right)\right)\right],\end{aligned} \tag{2}$$

where a_h and b_h are the real and imaginary Fourier coefficients of the h^{th} harmonic, respectively.

As mentioned before, in the HBSRI topology the equivalent impedance is an RL circuit. The first-harmonic equivalent impedance, $\boldsymbol{Z}_{1h,\mathrm{RL}}$, can be calculated by obtaining the DTFS

coefficients of the voltage drop in the load, $v_{\rm L}$, and its current $i_{\rm L}$, which are referred as $\boldsymbol{V}_{{\rm L},1h}$ and $\boldsymbol{I}_{{\rm L},1h}$, respectively:

$$\boldsymbol{Z}_{1h,{\rm RL}} = \frac{\boldsymbol{V}_{{\rm L},1h}}{\boldsymbol{I}_{{\rm L},1h}} = R_{1h} + {\rm j}L_{1h}\omega_{\rm sw}, \tag{3}$$

where $\omega_{\rm sw}$ is the angular switching frequency.

However, given the low-cost framework of DIH, the resonant-capacitor voltage is not usually measured. In such case, the equivalent impedance seen by the inverter is an RLC series circuit and the first-harmonic equivalent impedance, $\boldsymbol{Z}_{1h,{\rm RLC}}$, can be calculated by obtaining the DTFS coefficients of the output voltage, $\boldsymbol{V}_{{\rm o},1h}$, and the load current, $\boldsymbol{I}_{{\rm L},1h}$, as:

$$\boldsymbol{Z}_{1h,{\rm RLC}} = \frac{\boldsymbol{V}_{{\rm o},1h}}{\boldsymbol{I}_{{\rm L},1h}} = R_{1h} + {\rm j}X_{1h,{\rm RLC}}, \tag{4}$$

where the resistance, R_{1h}, is directly obtained from the real component of the impedance, as in (3) and, given that the value of the resonant capacitor, $C_{\rm r}$, is known, the equivalent inductance, L_{1h}, can be obtained from the reactance, $X_{1h,{\rm RLC}}$, as:

$$L_{1h} = \frac{X_{1h,{\rm RLC}}}{\omega_{1h}} + \frac{1}{C_{\rm r}\omega_{1h}^2}, \tag{5}$$

where $\omega_{1h} = \omega_{\rm sw} = 2\pi f_{\rm sw}$ and negligible equivalent series resistance (ESR) values of the resonant capacitor are assumed.

In this case, the identification of the equivalent inductance depends on the value of the resonant capacitor, i.e. on its tolerance, its variation with the temperature, its ageing, etc. Both perspectives are considered in the implementation of the method but, in terms of accuracy, digitizing $v_{\rm c}$ is preferred over assuming a constant and known $C_{\rm r}$ value. This is the reason why the results throughout this paper are focused on the approach that fulfills (3) instead of (4) and (5).

III. The Identification Method

A. Phase-sensitive detector (PSD)

The first-harmonic identification of the load is based in a PSD, which is typically applied to signals with low signal-to-noise ratio (SNR) from which a specific frequency component needs to be extracted [25], [26]. A block diagram of the algorithm is shown in Fig. 2.

Let $x_{\rm i}(t)$ be a sinusoidal signal with angular frequency ω_i and a dc term, $d_{\rm i}$ (a dc term is assumed to make the demonstration also valid for (4) and (5)):

$$x_{\rm i}(t) = d_{\rm i} + a_{\rm i}\cos(\omega_{\rm i}t + \varphi_{\rm i}), \tag{6}$$

and let $r_{\rm c}$ and $r_{\rm s}$ be two reference sinusoidal signals in quadrature with angular frequency $\omega_{\rm r}$:

$$\begin{aligned} r_{\rm c}(t) &= \cos(\omega_{\rm r}t) \\ r_{\rm s}(t) &= \sin(\omega_{\rm r}t). \end{aligned} \tag{7}$$

Multiplying the signals in (7) by the signal $x_{\rm i}(t)$ in (6):

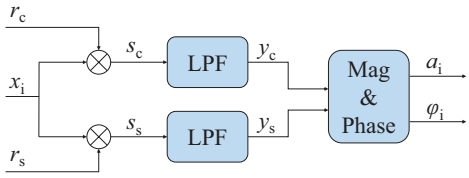


Fig. 2. Block diagram of the PSD algorithm.

$$\begin{aligned} s_{\rm c}(t) &= d_{\rm i}\cos(\omega_{\rm r}t) + \frac{a_i}{2}\cos\left[(\omega_{\rm i}+\omega_{\rm r})t + \varphi_{\rm i}\right] \\ &\quad + \frac{a_{\rm i}}{2}\cos\left[(\omega_{\rm i}-\omega_{\rm r})t + \varphi_{\rm i}\right] \\ s_{\rm s}(t) &= d_{\rm i}\sin(\omega_{\rm r}t) + \frac{a_{\rm i}}{2}\sin\left[(\omega_{\rm i}+\omega_{\rm r})t + \varphi_{\rm i}\right] \\ &\quad - \frac{a_{\rm i}}{2}\sin\left[(\omega_{\rm i}-\omega_{\rm r})t + \varphi_{\rm i}\right] \end{aligned} \tag{8}$$

If $\omega_{\rm r} = \omega_{\rm i}$, $s_{\rm c}$ and $s_{\rm s}$ have ac components at frequencies $\omega_{\rm i}$ and $2\omega_{\rm i}$. Applying a low pass filter (LPF) to (8) with a cutoff frequency below $\omega_{\rm i}$, a dc term is obtained:

$$\begin{aligned} y_{\rm c} &= \frac{a_{\rm i}}{2}\cos(\varphi_{\rm i}) \\ y_{\rm s} &= \frac{-a_{\rm i}}{2}\sin(\varphi_{\rm i}). \end{aligned} \tag{9}$$

The amplitude, $a_{\rm i}$, and the phase, $\varphi_{\rm i}$, of the signal $x_{\rm i}(t)$ respect to the sinusoidal reference signals in (7) can be calculated as:

$$\begin{aligned} a_{\rm i} &= 2\sqrt{y_{\rm c}^2 + y_{\rm s}^2} \\ \varphi_{\rm i} &= -\arctan\left(\frac{y_{\rm s}}{y_{\rm c}}\right). \end{aligned} \tag{10}$$

If this algorithm is applied over $v_{\rm L}$ and $i_{\rm L}$, and $\omega_{\rm i}$ is forced to be $\omega_{\rm sw}$, the sine and cosine components (corresponding to the imaginary and real components, respectively) of the inverter signals can be obtained which, from now on, will be referred as: $V_{\rm L,c}$, $V_{\rm L,s}$, $I_{\rm L,c}$ and $I_{\rm L,s}$ (the rightmost subindex refers to sine or cosine component and the subindex referring to the first harmonic is omitted). Once these values are computed, the equivalent load of the system, $R_{1h} - L_{1h}$, can be calculated by applying (3) or, what is equivalent:

$$\begin{aligned} R_{1h} &= \frac{V_{\rm L,c}I_{\rm L,c} + V_{\rm L,s}I_{\rm L,s}}{I_{\rm L,c}^2 + I_{\rm L,s}^2} \\ L_{1h} &= \frac{V_{\rm L,c}I_{\rm L,s} - V_{\rm L,s}I_{\rm L,c}}{\omega_{\rm sw}(I_{\rm L,c}^2 + I_{\rm L,s}^2)}, \end{aligned} \tag{11}$$

where it is assumed that the phasors of the load voltage and the current are given by $\boldsymbol{V}_{{\rm L},1h} = V_{\rm L,c} - {\rm j}V_{\rm L,s}$ and $\boldsymbol{I}_{{\rm L},1h} = I_{\rm L,c} - {\rm j}I_{\rm L,s}$, respectively.

B. Low Pass Filter Design

A fundamental piece of the PSD algorithm is the design of its low pass filter. The inverter signals, $v_{\rm L}$ and $i_{\rm L}$ are multiplied by the sinusoidal waves in (7), hence the sampling period has to be high enough to obtain an acceptable resolution of the

sinusoidal signals. The sampling rate of the analog-to-digital converters (ADC) mounted in the prototype later introduced is 2.78 Msps, which is a perfectly feasible sampling frequency in the state-of-the-art of embedded systems.

Since the goal of this work is to obtain the variation of the load with the excitation level, the cutoff frequency of the LPF has to be above the bus frequency, f_{B}, but below the minimum switching frequency, f_{sw}, otherwise the ac terms in (8) would not be attenuated. However, the appearance of sidebands, inherent to the modulation over an ac bus voltage, can introduce undesired noise in the load identification, hence a quite lower cutoff frequency than the minimum f_{sw} is preferred. Thus, a cutoff frequency of 600 Hz is established, with a stop-band attenuation of 60 dB above 2 kHz.

Given the complexity of the filter with the actual sampling rate, its implementation in a fixed-point representation would lead to unreasonable coefficient lengths and overutilization of resources. In these cases, multi-rate techniques allow reducing the sampling rate of the signals in order to relax the filter coefficients.

In this work, a decimation factor of 32 is chosen, obtaining a final sampling rate of 86.8 ksps for the $R_{1h} - L_{1h}$ parameters. For such high decimation factors, cascaded integrator comb (CIC) filters are widely used thanks to their economical use of resources [27]. Their filter response does not provide many degrees of freedom, so these filters are often followed by other type of filters whose response is more tunable and whose coefficients are then less restrictive because of the lower sampling rate.

The proposed filter is a three-stage cascading filter consisting of a CIC filter, with a decimation factor of 8, followed by two finite impulse response (FIR) filters, each of them with a decimation factor of 2. The order of the first and second FIR filters is 3 and 210, respectively. In this case FIR filters are preferred over infinite impulse response (IIR) filters because of their linear phase and constant group delay which, for the proposed filter, is 53.3 samples (referred to the output sampling rate of 86.8 ksps), i.e. 614 μs.

C. Simulation verification

The control of the inverter in the real prototype is implemented through a phase-accumulator-based modulator due to its implicit advantages compared to the counter-based modulators [28]. The value of the accumulator is used to generate and synchronize the sinusoidal signals in (7) with v_{L} and i_{L}. This modulator was simulated, together with the proposed algorithm and the circuit of the HBSRI shown in Fig. 1 in Matlab-Simulink assuming an ideal rectified-mains voltage of 50 Hz and 230 V rms. The switching frequency spans from 35 to 75 kHz, and the values of R and L are modified following symmetric patterns respect to the bus voltage (excitation level). Positive, negative, and constant dependences of the $R - L$ parameters with the bus voltage have been considered. The goal of this simulation is not to represent the exact behavior of a real load, but to put under test the proposed algorithm and to prove that it can track constant and variable values of the resistance and the inductance, whose range is [2, 10] Ω and [10, 70] μH, respectively (most of the DIH loads for the given appliance lie within this range [14]). In Fig. 3 the results of a 10-bus-cycle simulation are shown, where it can be observed that the algorithm offers a perfect tracking of the load impedance.

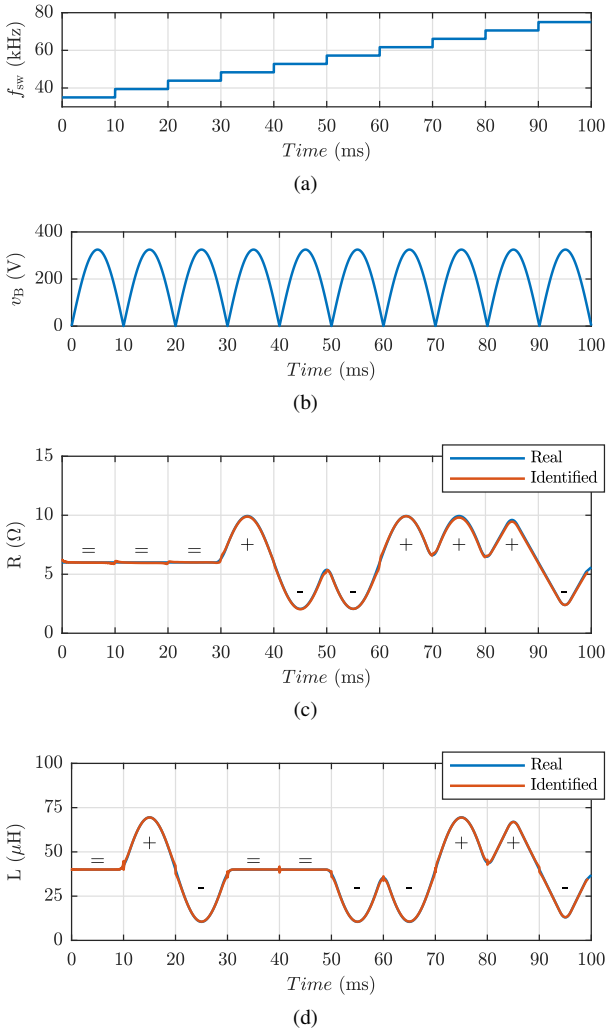


Fig. 3. Simulation results. (a) Switching frequency. (b) Bus voltage. (c) Real and identified resistance. (d) Real and identified inductance.

D. Implementation

To implement this algorithm into the SoC, Vivado and System Generator are used. System Generator is an FPGA designing tool provided by Xilinx which allows developers to work in the flexible Matlab-Simulink environment while exploiting the optimized and ready-to-use intellectual-property (IP) cores designed by Xilinx [29]. Several IP cores are available, but in this case only four of them are used: scalers, time division multiplexers, CIC compilers and FIR compilers. The entire algorithm is described in VHDL, except the LPF, which is implemented in System Generator. The justification for such procedure lies in the ease and agility of the LPF design and reconfiguration. The VHDL design and the LPF are merged into a single custom IP core which, in turn, behaves as an ARM peripheral.

TABLE I
RESOURCE UTILIZATION

LUTs	DSPs	BRAMs	FFs
1484	12	4	2579

The ADCs available in the prototype have a resolution of 12 bits, its sampling frequency is 2.78 Msps and the clock frequency of the programmable logic is 100 MHz.

The modulator that controls the inverter is based in a 25-bit accumulator, whose 10 most significant bits (MSBs) are used to generate and synchronize the sinusoidal signals in (7) with the inverter signals. To do so, a quarter of an 18-bit sine cycle is discretized in 256 values and stored in a block RAM.

The resource utilization in terms of look-up-tables (LUTs), digital signal processing (DSPs) slices, block RAMs (BRAMs) and flip-flops (FFs) of the load-identification IP core is shown in Table I. It is worth mentioning that this IP core was not designed to identify one load but two independent loads simultaneously, hence the number of resources required for a single load would be approximately halved.

IV. EXPERIMENTAL RESULTS

A. Experimental prototype

Fig. 4 shows the experimental setup where the load-identification algorithm is implemented. The prototype consists of two HBSRIs that are fed by the rectified mains. The inverters are loaded with two planar inductors with external diameters of 21 and 15 cm. More specific characteristics of the prototype are given in Table II.

To build this prototype some parts of a commercial induction hob were utilized and two printed circuit boards (PCBs) were designed: the first one includes the power electronics, while the second one includes the signal conditioning circuitry, and the ADCs (LTC2315-12 from Linear Technology). Moreover, this second PCB was designed to be compatible with the carrier board TE0703 from Trenz Electronics which, in turn, is connected to the system on module (SoM) TE0720. Likewise, this SoM mounts the Zynq-7020 SoC, which integrates in a single chip the programmable logic (PL) through FPGA fabric and the processing system (PS) through a dual-core ARM Cortex-A9 processor. Additionally, the SoM mounts other devices such as a 1 GB DDR3/L SDRAM (Double Data Rate type 3 Low-voltage Synchronous Dynamic Random-Access Memory).

A Xilinx's direct memory access (DMA) controller is configured in direct register mode to transfer the load-identification data on the string-to-memory-map (S2MM) channel to the SDRAM device. The configuration of this controller is implemented in one of the ARM processors, which is also in charge of high-level tasks like power control, monitoring of electrical variables, switching frequency settings, configuration of peripherals (IP cores), etc.

The phase-accumulator-based modulator, the control of the ADCs, and the identification method itself are implemented in the PL (packaged as IP cores) due to the requirements in terms of high speed and parallelism. The ADCs are controlled through a serial peripheral interface (SPI), the communications between the IP cores and the ARM processor is accomplished through the Advanced eXtensible Interface 4 Lite (AXI4-Lite), and the AXI4-Stream protocol is used to send the load-identification data from the PL to the DMA controller.

TABLE II
PROTOTYPE CIRCUIT PARAMETERS

Symbol	Description	Value
$\hat{V}_{\mathrm{B}}$	Peak bus voltage	325 V
f_{mains}	Mains frequency	50 Hz
C_{r}	Resonant capacitor	1080 nF (1st load) 540 nF (2nd load)
C_{B}	Bus capacitor	6.6 μF
C_{s}	Snubber capacitor	15 nF

The second processor runs an operating system called petalinux that facilitates the communication with a laptop in which a graphical user interface was programmed in Matlab. This communication is based on TCP/IP protocol and allows the system to send the load-identification data from the SDRAM to the laptop. To limit the ARM utilization and for post-processing reasons, instead of transferring the $R_{1h} - L_{1h}$ values to the laptop, the components $V_{\mathrm{L,c}}$, $V_{\mathrm{L,s}}$, $I_{\mathrm{L,c}}$ and $I_{\mathrm{L,s}}$, and the instantaneous switching frequency are transferred, and (11) is computed directly in Matlab. All these systems together enable a quasi real-time visualization of the load, as well as a greatly efficient test bench for pots identification and data logging.

B. Experimental validation

High-accuracy instruments like impedance analyzers and LCR-meters are frequently used to identify the impedance parameters of the inductors [30]. However, these instruments only apply to small-signal conditions. Given the non-linearities of DIH, the identification under small-signal conditions does not give enough information, hence in this work a different approach is applied to validate the measurements of the prototype.

A bus period, T_{B}, of the signals v_{L} and i_{L} was captured and saved with a digital oscilloscope sampling at 100 Msps. At the same time, the SoC run the load-identification algorithm, and the data was transferred to the laptop.

To validate the algorithm, the waveforms captured with the oscilloscope during T_{B} were divided into 100 slots, and for each of them, the average first-harmonic equivalent impedance was computed. To do so, (2) was applied substituting N by the number of samples per slot, i.e. a million samples. Previously, a *Blackman* window was applied to every slot of v_{L} and i_{L} to reduce the spectral leakage.

These 100 values of R and L were compared to the real-time identification obtained with the PSD algorithm implemented into the SoC, and this process was repeated for several switching frequencies and different pots. An example of the mentioned comparison can be observed in Fig. 5,

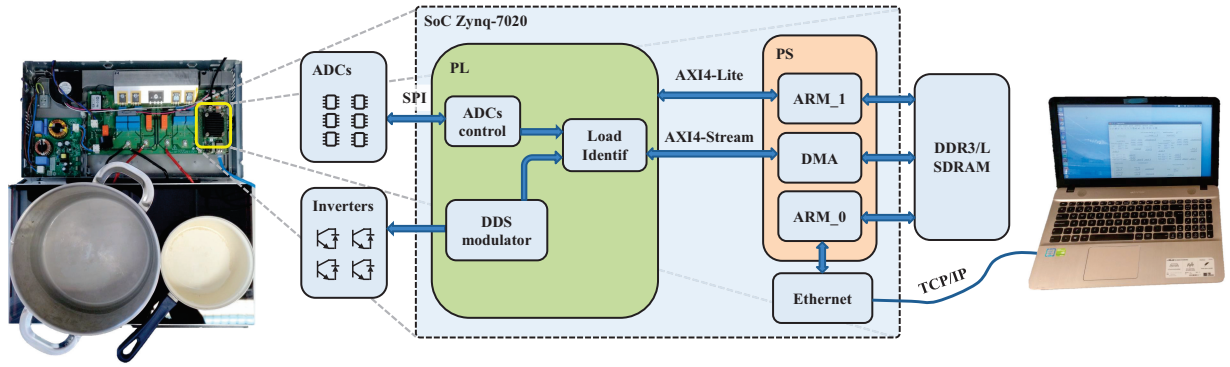


Fig. 4. Experimental setup and conceptual block diagram.

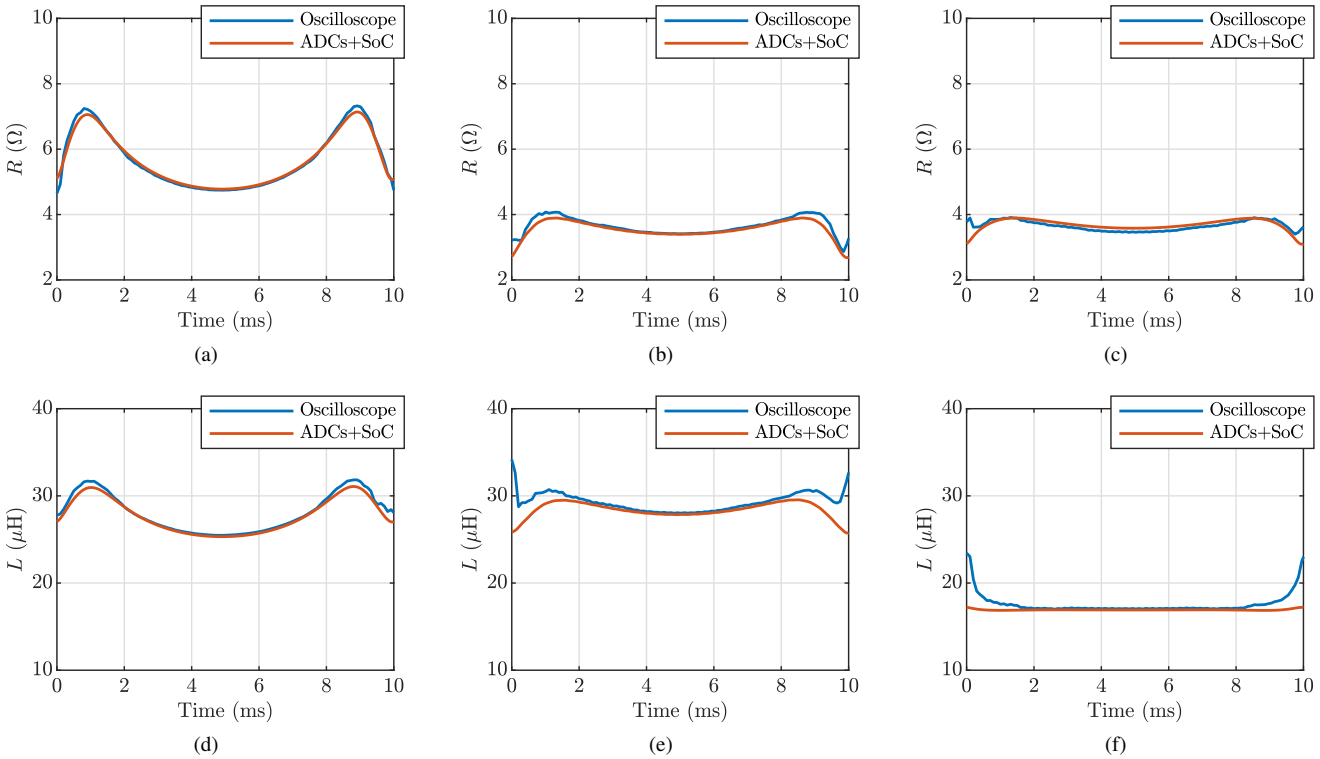


Fig. 5. Comparison between the equivalent $R-L$ load obtained with data captured through oscilloscope versus the real-time implementation (variation during an ac bus period, crest value of bus voltage at 5 ms). Three different types of pots are shown: (a),(d) Enameled pot. (b),(e) Sandwich-type pot. (c),(f) Multi-layered pot.

where the equivalent impedances of three pots with different material properties are shown. It can be seen that the online implementation offers an accurate tracking of the equivalent impedance, although larger differences are given during the two outer milliseconds of T_{B}. This can be due to the fixed-point implementation of the algorithm and the quantization of the ADCs, which do not take advantage of their whole dynamic range when the bus voltage is low (outermost sides of T_{B}).

The waveforms obtained with the oscilloscope were captured with high resolution at 100 Msps and the offline calculations were performed in double precision. Taking into account that the ADCs of the prototype sample at 2.78 Msps and the low-pass filtering is implemented in fixed-point precision, the accuracy of the results is promisingly good.

V. Applications

There are many use cases where the presented identification algorithm could provide the appliance with relevant improvements. Some of which are presented in this section.

In the literature, the average equivalent impedance (only one value per bus cycle) was already utilized to detect substitutions of different pots [18]. It is worth mentioning that the in-cycle identification would not provide much improvement respect to the mentioned work for relatively slow dynamic events (around a few tens of milliseconds) like pot removals or temperature changes of pot content (e.g. pouring cold water in boiling one). Therefore, the importance of the proposed method does not lie in slow dynamic behaviors, but in faster frequency phenomena. Some of the potential features are presented in this section.

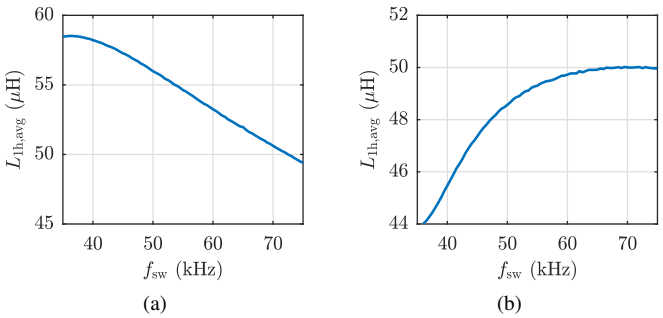


Fig. 6. Averaged equivalent inductance during a bus period. Materials with: (a) soft saturation level, (b) deep saturation level.

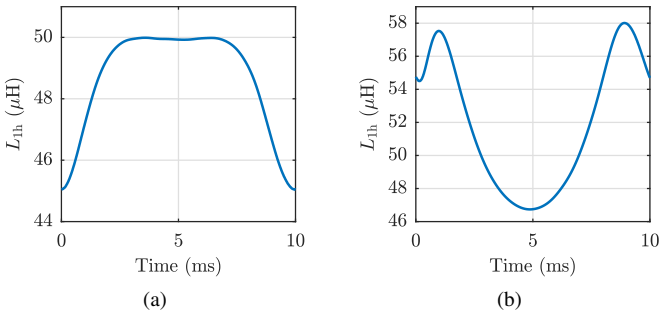


Fig. 7. Instantaneous equivalent inductance during 10 ms (peak bus voltage at 5 ms). Materials with: (a) soft saturation level, (b) deep saturation level.

A. Identification of pot material

It is shown that the $R-L$ parameters vary with f_{sw} and i_{L}: $R(f_{\mathrm{sw}}, i_{\mathrm{L}})$ and $L(f_{\mathrm{sw}}, i_{\mathrm{L}})$. The physics behind this dependence lies in the magnetic permeability, μ, of the pot material [31]. Different ferromagnetic materials have different penetration depths, and this phenomenon is mainly reflected on their equivalent inductance. The equivalent inductance of a pot with soft saturation level is more dependent on the switching frequency, meaning that as f_{sw} decreases, the equivalent L increases. Whereas the inductance of pots with soft saturation level is inversely related to the switching frequency, the inductance of pots with deep saturation level is directly related to the frequency due to the material saturation and magnetic permeability reduction [11]. This effect can be observed in Fig. 6, where the averaged (during T_{B}) equivalent inductance of two pots, one with soft and another one with deep saturation level, is shown for different switching frequencies.

The response of these two materials (in terms of equivalent inductance) to a change of f_{sw} is the opposite, meaning that to presume which kind of material is being heated, the appliance may have to sweep a bunch of switching frequencies to calculate that relative variation or slope sign. However, since the bus voltage is an ac wave, the application of different excitation voltages and, consequently, currents, can also be used to identify the material without the need of modifying the switching frequency. In Fig. 7 the instantaneous inductance (during a bus cycle) of the pots whose averaged equivalent inductance was shown in Fig. 6 is depicted. These inductances were obtained at $f_{\mathrm{sw}} = 75$ kHz, frequency at which the hob normally starts the modulation. This means that as soon as

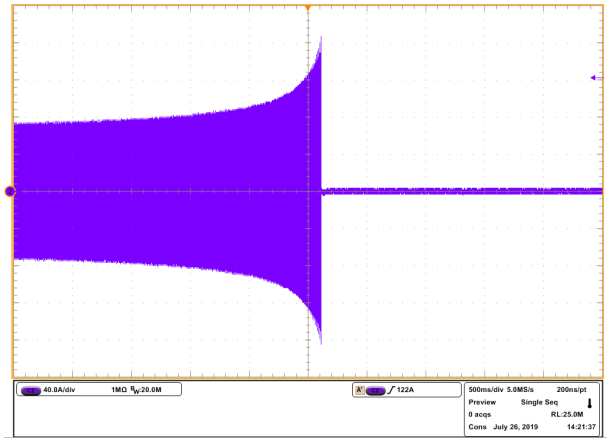


Fig. 8. Load current (40 A/div) when material is saturated by Curie temperature. Power supply automatically cuts power if mains current is greater than 16 A.

the user places the pot over the inductor, and only a bus cycle later, the system can presume the type of material that is to be heated.

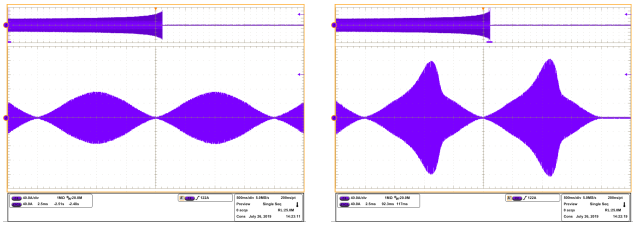
One of the advantages of presuming the saturation level of the material is that it would be possible to predict how the average equivalent inductance would change with a variation of f_{sw}. This information could be used, for instance, to know how far the system is from its resonant frequency at each excitation level (assuming C_{r} is known), to predict how the resonant frequency of the system would change with a variation of f_{sw} (due to the variation of L), to enable newer power-control strategies and to adapt the controller coefficients depending on the type of pot.

B. Detection of pot saturation

Apart from deeper or softer saturation levels, there exist a characteristic parameter of ferromagnetic materials that limits the maximum temperature at which they remain ferromagnetic, which is called Curie temperature [32].

When a ferromagnetic material is heated above its Curie temperature it losses its ferromagnetic properties and turns into a paramagnetic material, which is not suitable for DIH. This can happen, for instance, when water is boiled in a pot with a relatively low Curie temperature and it runs out of water. Then, the power cannot be dissipated and its temperature increases. When the Curie temperature is reached, the behavior is similar to a sudden "load disappearance", which quickly decreases the equivalent resistance and inductance. If the system cannot predict this phenomenon, the current drastically increases, compromising the integrity of the electronic components. This effect is shown in Fig. 8, where the switching frequency is constant and the load current almost doubles its peak value from 90 to 170 A in less than half a second (final current values are zero because of the power supply protection).

In Fig. 9 a zoom-in of the load current under normal operation of the system and under saturation is shown. This effect can be seen in the equivalent impedance, and it can be predicted before it happens. In Fig. 10 the equivalent inductance under normal operation and at different instants



(a) (b)

Fig. 9. Zoom-in of load current (40 A/div) under constant switching frequency, 40 kHz. (a) Normal operation. (b) Saturated material by Curie temperature.

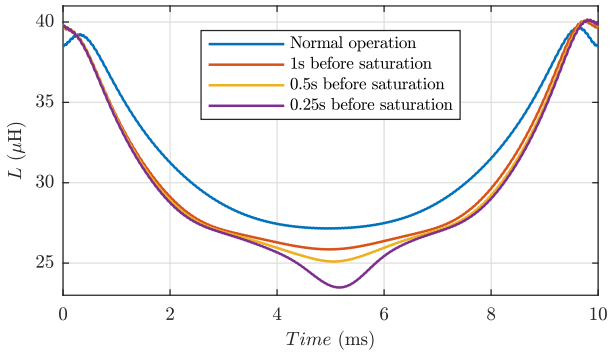


Fig. 10. Equivalent inductance under normal operation and saturated conditions (1, 0.5 and 0.25 seconds before power supply protects the appliance). Data extracted through the SoC.

before the power supply protects the appliance is shown. It can be seen how the shape of the equivalent inductance starts to warp. This information can be used to prevent the system before larger saturation happens and, consequently, limiting the peak currents and protecting the appliance.

C. User-patterns detection

When sauteing, it is quite common among end-users to toss or stir the ingredients by shaking the pan instead of mixing them with a spoon. This has no negative effect on traditional stoves (resistive or gas), but concerns DIH manufacturers because the equivalent impedance of the load varies continuously and relatively quickly.

When the appliance initially turns on, the modulation starts at the maximum switching frequency, i.e. 75 kHz. Since the power – f_{sw} curve is not known beforehand, the power level required by the user is gradually reached through a hill-climbing control method. When a sudden change of the electrical parameters is detected, the processor, in order to protect the appliance, resets the action, starting again at 75 kHz and repeating the same hill-climbing process. This sudden change can be generated by sauteing, leading to a continuous reset of the control, and deteriorating the response time of the supplied power and the user perception.

In Fig. 11 the equivalent resistance of the load under sauteing conditions is shown. Contiguous bus cycles are split along a third dimension to ease the interpretation.

It can be observed that this phenomenon can be easily detected looking at the equivalent resistance in the crest of v_{B} (at 5 ms). Thanks to the real-time identification of the

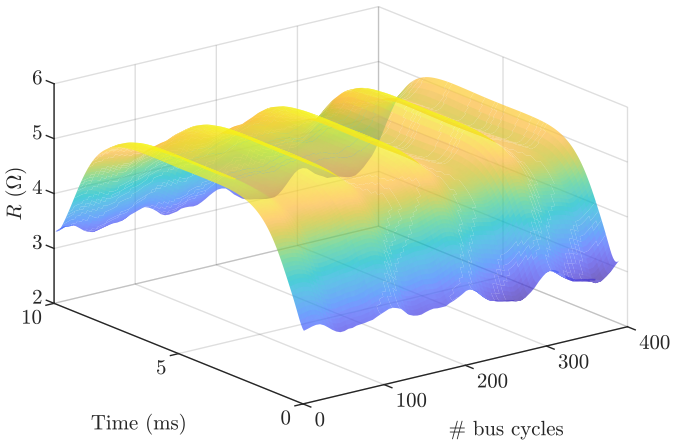


Fig. 11. Identified resistance of a soft-saturating material under the described sauteing conditions.

impedance it would be possible to avoid the unwanted effect of continuous action resets and enable faster response times.

In this case, the importance of the proposed method lies, rather than in fast-dynamic phenomena, in the local information of R_{1h} at high values of v_{B} (this effect is less significant at low values of v_{B}).

D. Standard fulfillment

Induction hobs need to comply with many standards regarding the electromagnetic compatibility with the grid. One of them imposes limits in the harmonic distortion of the mains current [33]. The resonant frequency, f_0, of a series RLC circuit is given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC_{\mathrm{r}}}} \tag{12}$$

The resonant capacitor is constant, so that f_0 is inversely related to L. Let's assume a constant f_{sw} is applied during the entire bus cycle and the pot material has a deep saturation level. Looking at Fig. 5(b), it can be seen that in the center of T_{B}, L decreases with the excitation level, hence as the system gets closer to the resonant frequency, the power supplied increases. This means in the crest of the bus cycle, i_{L} is higher than it would be if the impedance was constant. Furthermore, the resistance is also smaller for high excitation voltages (see Fig. 5(b)) and, referring to the ohm law, the current is also higher than it should. These two effects overlay, deteriorating the total harmonic distortion (THD) of the mains current.

To illustrate this effect, the HBSRI is simulated at four different conditions (see Fig. 12). To simulate the variable impedance whether a non-linear model or a large dataset is needed. The identification algorithm was executed together with the information of the $f_{\mathrm{sw}}(t)$ and $v_{\mathrm{B}}(t)$ when a deep-saturating pot was placed above the inductor. With this information it is possible to simulate in Simulink-Matlab variable $R-L$ values based in real data and an interpolated look-up table. This look-up table is based on more than 30 thousand values of R and L at different f_{sw} and v_{B}.

When constant $R-L$ values are considered, the envelope of i_{L} is sinusoidal, as the mains voltage is, but when variable

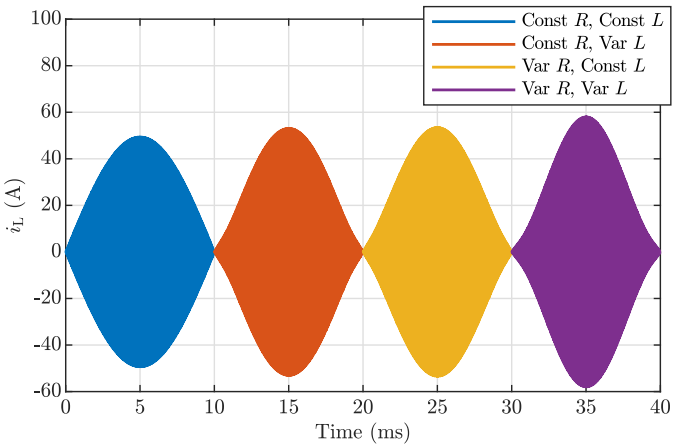


Fig. 12. Effect on i_{L} of the variable $R-L$ parameters.

$R-L$ values are simulated, which is the case when using a real deep-saturating pot, the harmonic content of the envelope of i_{L} greatly increases in detriment of the IEC 61000-3-2 standard fulfillment [33]. The THD of the envelopes of the load current are calculated as:

$$\mathrm{THD} = \frac{\sqrt{\sum_{h=2}^{40} I_h^2}}{I_1}, \tag{13}$$

where I_h denotes the rms current of the h-th harmonic, being 1 the fundamental harmonic of the 50 Hz envelope. The THD values for the conditions shown in Fig. 12 are:

a) 0.11 % (constant R and L).
b) 7.60 % (constant R and variable L).
c) 7.22 % (variable R and constant L).
d) 13.22 % (variable R and L, real situation).

The identification of this phenomenon in a real appliance could be used to generate variable switching-frequency profiles to compensate this unwanted effect of the $R-L$ variation and, more importantly, these profiles could be adapted in real time to every single pot, minimizing the THD of the mains current.

VI. Conclusion

In this paper a method based in a PSD algorithm that allows a real-time identification of the equivalent load of a DIH appliance is proposed. The method, once validated in simulation, is designed in Vivado and System Generator and implemented into a SoC. Then, the experimental verification, based in data captured with an oscilloscope is also performed. Additionally, the experimental results obtained with the real prototype and the SoC have been used to simulate the HBSRI with non-linear impedances.

Although the results are based on measuring the resonant-capacitor voltage, the method proposed is also valid when only v_{o} and i_{L} are measured, even though, the tolerance and variation of C_{r} could affect the accuracy of the identification.

Some useful applications and use cases of the proposed identification are presented. They all imply fast-dynamic phenomena or local information at a specific instant of the bus period. Some of the main improvements the proposed algorithm provides are:

- Information about the ferromagnetic material of the pots (penetration depth): discrimination between soft and deep saturation levels.
- Over current protection thanks to the premature detection of ferromagnetic saturation by Curie temperature.
- Detection of vessel movements generated by users, leading to a potential improvement of the resetting behavior of the power control.
- Information about harmonic distortion due to the equivalent impedance variation.

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