Conductance Control for Electromagnetic-Compatible Induction Heating Appliances

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***Abstract*—The design requirements of induction hobs are strongly restricted by efficiency, heating performance, cost, the generation of acoustic noise and electromagnetic compatibility (EMC). These two latter topics, cost and EMC, motivated the research presented in this work. The different levels at which the equivalent load of the induction hob is excited generate a variation of the equivalent impedance throughout the grid period even if all the other parameters are kept constant. This can cause a non-sinusoidal consumption of the grid current which goes against the compliance with EMC standards. This paper proposes an online controller which controls the conductance seen by the inverter by only modifying the switching frequency throughout the bus period. This greatly reduces the harmonic distortion of the grid current no matter what is the type of the vessel used. Moreover, it requires neither power-factor correction rectifiers nor any additional circuitry and it has a faster dynamic response with respect to the traditional solutions used in induction hobs due to its higher bandwidth.**

***Index Terms*—Home Appliances, Induction Heating, Total Harmonic Distortion.**

I. Introduction

OVER the last decades, domestic induction heating (DIH) has shown its potential benefits in terms of security, cleanness and efficiency compared to the traditional domestic heating methods (resistive and gas) [1]–[3].

The equivalent load of an induction hob, which represents the electromagnetic interaction between the inductor and the ferromagnetic material of the pot, is usually modeled as a resistance, R, in series with an inductance, L, [4].

One of the most used topologies to generate the alternating current that, in turn, generates the alternating magnetic field, is the half-bridge series resonant inverter (HBSRI). Its simplified schematic is shown in Fig. 1.

Since DIH generally belongs to a low-cost market, the grid voltage is full-wave rectified and filtered through a small bus capacitor, C_{B}, which generates the bus voltage, v_{B}, that directly feeds the inverter. The bus capacitor has a low capacitance to obtain a high-rippled bus voltage and a power factor close to one so that no additional power factor correction (PFC) circuitry is required. Let us emphasize the importance of avoiding additional circuitry to achieve cost-optimized solutions, which also becomes one of the aims of this work. Additionally, in this topology the power supplied to the pot is controlled by means of the switching frequency, f_{sw}, while the duty cycle, D, is kept constant at 0.5 in order to ease the control and balance the stress generated in the semiconductor devices.

One of the most challenging characteristics of DIH is that the equivalent impedance $R-L$ varies with many parameters such as the temperature, the excitation level applied to the load, the distance between the pot and the inductor, the ferromagnetic material of the pot, the switching frequency, etc. [5]. This fact is quite relevant because even the control action (f_{sw}) leads to an intrinsic variation of the load. Additionally, it is the user who selects the pot, leading to an even wider range of loads.

Regarding power control, the most typical approach is based on a hill-climbing method: once the pot is placed above the inductor and the user selects the power target, the modulation starts at a safe (usually maximum) switching frequency; the power is calculated every bus period, T_{B}, and f_{sw} is modified upwards or downwards by a fixed amount depending on whether the measured power is less or greater than the requested one [6], [7]. The main drawback of this method is its low bandwidth and slow time response, which would not present a problem as long as the system was only governed by low-frequency phenomena. However, as soon as other events arise such as the user interaction with the vessel, controllers with higher bandwidths would be desirable.

If faster controllers are required, it would be advantageous to know the angular switching frequency (ω_{sw}) - to - output power (P) transfer function, G_{pw}. However, the load cannot be characterized beforehand because it depends on the user choice. Fortunately, at low frequencies, the transfer function G_{pw} can be approximated by a dc gain [8]. This could increase the bandwidth of the controller by using a variable step of f_{sw} instead of a fixed one. As in other applications such as solar and photovoltaic [9], [10], this gain can be locally computed by perturbation and observation. In DIH, this ap-

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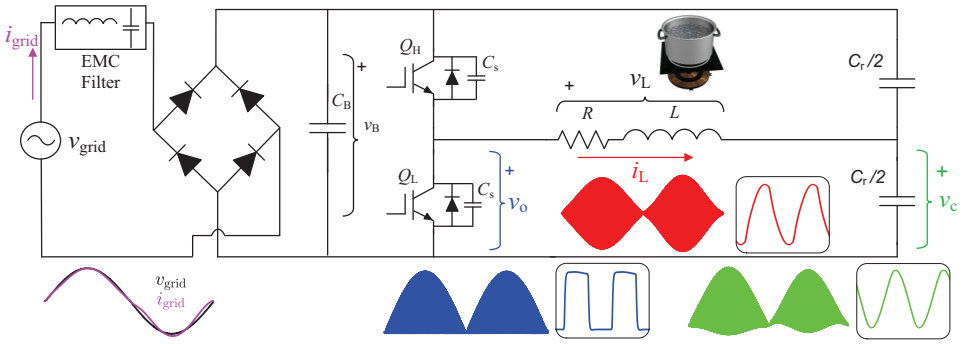


Fig. 1. Simplified schematic of the power electronics of an induction hob. The main waveforms during a grid period are shown (a couple of switching cycles of the high-frequency signals are also depicted in small frames).

proach is based on slightly changing the switching frequency and compute the ratio between the variation of power and the variation of f_{sw} [11]. However, at least two bus cycles are required to compute the gain, and this limits the bandwidth of the control. To overcome this issue, a more advanced method, although based on a similar principle, estimates this gain in a single bus cycle by imposing different switching frequencies within T_B [12]. In [13], the dc gain is estimated from analytical expressions of the partial derivative of the power with respect to the switching frequency, but this method is based on keeping a constant switching frequency throughout T_B, which is a very uncommon approach. More advanced proposals have been published, such as the use of model predictive control [14] or a gain-scheduling model-based PI controller that is offline calculated and whose scheduling is based on the online measurement of the load impedance [15].

However, in [11]–[15] the authors only tried to find faster controllers that could enable faster settling times for the active power. Nevertheless, they did not take into account neither the standards the induction hobs have to comply with nor the fact that the equivalent impedance varies with the excitation level.

Additionally, the switching frequency is rarely kept constant during the bus period, and the main reason lies in two standards that induction heating appliances have to comply with. The first one establishes limits in the harmonic current emissions of the grid [16], while the second one establishes limits in the emissions of radio-frequency disturbances in the frequency range from 9 kHz to 30 MHz [17].

It is well known that the equivalent impedance varies with the excitation level [18]: normally, at higher excitation levels the resistance decreases and the inductance increases, what generates a non-sinusoidal consumption from the grid (more current is consumed in the crest of the bus voltage) and, consequently, the total harmonic distortion (THD) of the grid current increases. To compensate this phenomenon and ease the compliance with [16], variable switching-frequency profiles (VSFPs) are usually imposed throughout the bus period with higher f_{sw} at the crest of the bus voltage. However, the purpose of these VSFPs is twofold because they are also used as a spread spectrum technique (SST) to reduce the conducted emissions above 9 kHz, what helps complying with [17]. Nevertheless, these VSFPs are usually based on a worst-case situation and they are often the same hardcoded profile for every pot, what represents a sub-optimal solution based on experimentation and observation in the laboratory.

Some research has already been carried out in this field. For instance, in [19]–[21], different modulation techniques are analyzed from the point of view of electromagnetic interference (EMI) reduction. To reduce the THD of the grid current, the addition of PFC rectifiers has also been proposed [22] at the expense of a significant cost increase.

In this paper, a real-time, high-bandwidth control of the power supplied to the pot is proposed. The aim of this work is to generate VSFPs that will be automatically and online adapted for any pot type and will improve compliance with the standards [16], [17]. The presented work is the first implementation of such algorithm in an induction hob that actively tries to reduce the harmonic distortion of the grid current while providing a quick power response without additional power electronics circuitry and only modifying the switching frequency. The proposed method is implemented in a prototype with a system-on-chip (SoC).

The rest of the paper is organized as follows: in Section II the equivalent model of the topology and more insights about the equivalent impedance are presented. The proposed method to control the power while keeping a low harmonic distortion in the grid current is presented in Section III. The results obtained through simulation are shown in Section IV. The implementation in a prototype and the experimental results are presented in Sections V and VI, respectively. Finally, the main conclusions are drawn in Section VII.

II. Equivalent Model and Impedance

The extended describing function (EDF) has been widely used to model frequency-modulated topologies in a systematic way [15], [23]–[25]. This technique approximates the nonlinear terms by the harmonic ones to obtain a linear model. However, one of the disadvantages of this method is that this harmonic decomposition leads to an increase of the system order. For instance, the series RLC circuit of the half-bridge topology, which can be modeled as a second-order system, is converted into a fourth-order model when EDF is applied (considering only the first harmonic).

Besides, when high-order plants are to be controlled, model-order reduction techniques are commonly applied to obtain

simpler models at the expense of accuracy losses and a reduction of the validity range. In [8] reduced-order models derived from the EDF modeling of the HBSRI are proposed. In this work, the slowly varying amplitude derivative and phase (SVADP) model from [8] is used. This model assumes the amplitude derivative of the resonant capacitor voltage, $dv_{\mathrm{c,1h}}(t)/dt$, and its phase, ϕ_{1h}, as slowly varying functions of time (subindex 1h refers to first harmonic) and it has a validity range of up to a tenth of the switching frequency.

The study carried out in [8] takes into account both variables, f_{sw} and D, but given that this work is focused on the variation of the switching frequency, at a constant duty cycle, from here on, all the equations extracted from [8] will assume $D = 0.5$. Thus, assuming a first-harmonic approximation, the load current can be expressed as:

$$i_{\mathrm{L}}(t) = i_{\mathrm{L,c}}(t)\cos(\omega_{\mathrm{sw}}t) + i_{\mathrm{L,s}}\sin(\omega_{\mathrm{sw}}t), \tag{1}$$

and the SVADP model can be written as:

$$\frac{d}{dt}\begin{pmatrix}\hat{i}_{\mathrm{L,c}}\\ \hat{i}_{\mathrm{L,s}}\end{pmatrix} = \begin{pmatrix}-R/L_{\mathrm{e}} & -X/L_{\mathrm{e}}\\ X/L_{\mathrm{e}} & -R/L_{\mathrm{e}}\end{pmatrix}\begin{pmatrix}-I_{\mathrm{L,s}}\\ I_{\mathrm{L,c}}\end{pmatrix} + \begin{pmatrix}1/L\\ 0\end{pmatrix}\hat{\omega}_{\mathrm{sw}}, \tag{2}$$

where variables with hat represent the small signal deviations respect the steady-state ones (represented with uppercase letters). Subindexes "c" and "s" refer to the cosine and sine components and L_{e} is defined as:

$$L_{\mathrm{e}} = L + \frac{1}{C_{\mathrm{r}}\Omega^2} = L\left(1 + \frac{1}{\Omega_{\mathrm{n}}^2}\right), \tag{3}$$

where Ω_{n} is the normalized angular frequency and it is calculated as $\Omega_{\mathrm{n}} = \Omega/\Omega_{\mathrm{o}}$. In turn, Ω_{o} is the resonant angular frequency and, for the HBSRI topology can be obtained as:

$$\Omega_{\mathrm{o}} = \frac{1}{\sqrt{LC_{\mathrm{r}}}}, \tag{4}$$

Additionally, X is the reactance of the series RLC circuit:

$$X = L\Omega - \frac{1}{C_{\mathrm{r}}\Omega} \tag{5}$$

From this model, the transfer function of the small signal angular switching frequency-to-output power is obtained as:

$$G_{pw}(s) = \frac{P(s)}{\omega(s)} = -\frac{2XP_{\mathrm{e}}}{L_{\mathrm{e}}}\frac{1}{(s + R/L_{\mathrm{e}})^2 + (X/L_{\mathrm{e}})^2}, \tag{6}$$

where P_{e} is:

$$P_{\mathrm{e}} = 2\left(\frac{V_{\mathrm{g}}}{\pi}\right)^2\frac{R}{Z^2}, \tag{7}$$

where V_{g} is the amplitude of a considered dc bus voltage and Z is the equivalent impedance of the series RLC circuit and is defined as:

$$Z = \sqrt{R^2 + X^2} \tag{8}$$

However, the aim of this paper is not only to increase the bandwidth of the power control, but to reduce the THD of the grid current. To do so, the power will be indirectly controlled through another variable called conductance.

If the output voltage is approximated by a square waveform with $D = 0.5$, the first-harmonic conductance, G_{1h}, can be defined as:

$$G_{\mathrm{1h}} = \frac{P_{\mathrm{1h}}}{V_{\mathrm{o,1h}}^2} = \frac{P_{\mathrm{1h}}}{(\sqrt{2}V_{\mathrm{g}}/\pi)^2}. \tag{9}$$

As it is shown in (9), the conductance can be understood as a scaling coefficient between the active power and the square of the voltage (this is also somehow a scaling coefficient between the "active" current responsible for the active power and the voltage [26]). Thus, a conductance controller, which is able to maintain a constant conductance, would generate an "active" current consumption that mimics the voltage waveform reducing the harmonic distortion of that current. In fact, the concept of the conductance has already been used in applications for power quality improvement and THD reduction [26], [27]. In the DIH case, a great advantage of using (9) is that the value of the conductance can be easily obtained from the power P which, in the end, is the variable that controls the cooking process.

From (6), (9) the angular switching frequency-to-conductance transfer function, G_{gw}, is obtained as:

$$G_{gw}(s) = \frac{G(s)}{\omega(s)} = -\frac{2XR}{Z^2L_{\mathrm{e}}}\frac{1}{(s + R/L_{\mathrm{e}})^2 + (X/L_{\mathrm{e}})^2} \tag{10}$$

It can be observed that, unlike G_{pw}, the transfer function G_{gw} is no longer dependent on the bus voltage. Additionally, this model assumes that the resistance and the inductance are constant. However, the equivalent impedance varies with the excitation level so that, even if a constant f_{sw} is applied to the inverter, the impedance would vary due to the considered ac bus voltage arrangement [5], [18]. Nevertheless, to apply the method presented in the following section and to achieve the pursued objective, the presented model is completely valid.

III. The Proposed Controller and SST

The model that is used in this work is based on a first harmonic approximation. In fact, this assumption is valid because the quality factor of the domestic-induction heating loads is high and, thus, the first harmonic of the inverter signals represents the main contribution to the power. Although this statement is true, an induction hob does not usually control the power supplied by the first harmonic, but the total power supplied to the pot; thus, the variable to be controlled is the total conductance, G, which will be calculated as:

$$G = \frac{P}{v_{\mathrm{o,rms}}^2} = \frac{\frac{1}{T}\int_0^T v_{\mathrm{o}}(t)i_{\mathrm{L}}(t)dt}{\frac{1}{T}\int_0^T v_{\mathrm{o}}^2(t)} \tag{11}$$

where T is the sampling time of P and $v_{\mathrm{o,rms}}$ or, in other words, the reference period during which P and $v_{\mathrm{o,rms}}$ are integrated.

In the traditional approach, the variable that is controlled is the power, P, and its sampling time, T, is equal to the bus period, T_{B}. However, the value of the conductance varies during T_{B} due to the variation of the equivalent impedance;

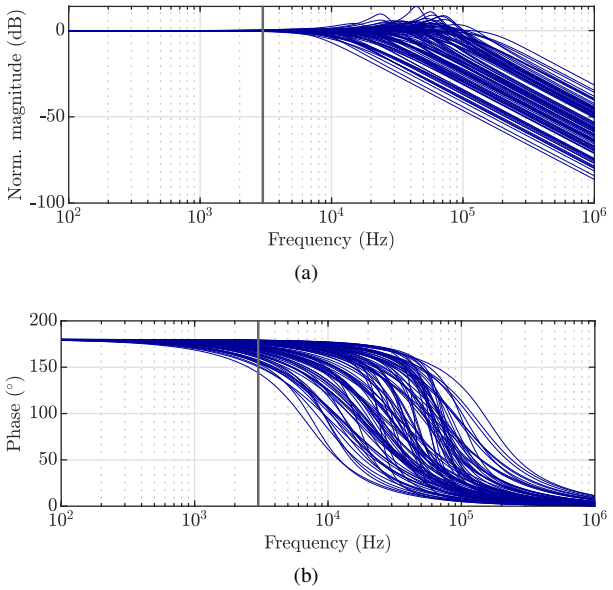


Fig. 2. Bode plot of G_{gw} for several random loads (RLC) and random $\Omega_{\rm n}$. The vertical gray line is placed at 3 kHz. (a) Normalized magnitude. (b) Phase.

thus, if the conductance has to be controlled throughout the bus period, a different approach has to be applied.

Given that $f_{\rm sw}$ spans from 30 to 75 kHz and the SVADP model is valid up to a tenth of $f_{\rm sw}$ [8], the model is valid up to 3 kHz. Moreover, the transfer function G_{gw} can be approximated as a gain up to approximately 3 kHz as well. Although this conclusion can be obtained from [8], Fig. 2 shows the bode diagram of G_{gw} for different random values of $R \in [2, 10]\ \Omega$, $L \in [10, 70]\ \mu$H, $C_{\rm r} \in [540, 1080]$ nF and $\Omega_{\rm n} \in [1.1, 3]$. These ranges were obtained from a large experimental dataset based on commercial pots, and they represent most, if not all, of the DIH loads for an inductor with a diameter of 21 cm (where the method will be put under test). In any case, the validity range is much greater than what is needed for the proposed method and, fortunately, the fact of approximating G_{gw} as a gain will greatly simplify the design of the controller.

By making $s = {\rm j}\omega = 0$ and after doing some maths, the dc gain of the transfer function $G_{gw}(s)$, G_{gw0}, is obtained:

$$G_{gw0} = G_{gw}(s=0) = \frac{-2XRL_{\rm e}}{Z^4} \tag{12}$$

In this work, an inverse-based controller design [28] is applied. This technique is based on inverting the transfer function of the plant and applying a loop shape which has a gain slope of -1. Although this controller design technique can not be applied to plants with more poles than zeros (because it would lead to a non-realizable controller), given that $G_{gw}(s)$ is approximated by its dc gain, the following controller, $C(s)$, can be obtained:

$$C(s) = \frac{w(s)}{e(s)} = \frac{\omega_{\rm gc}}{s} G_{gw0}^{-1}, \tag{13}$$

where $\omega_{\rm gc}$ is the gain crossover frequency and $e(s)$ is defined as $G(s) - G_{\rm T}(s)$, where $G_{\rm T}$ is the target conductance.

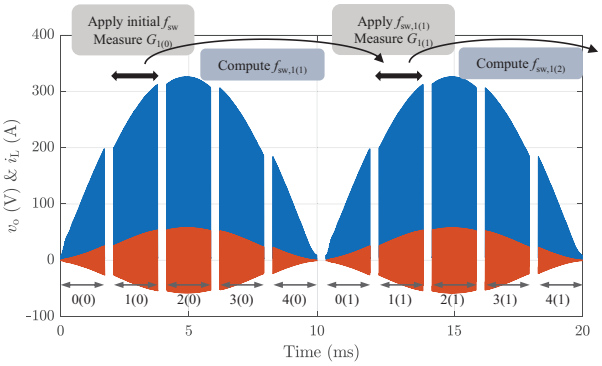


Fig. 3. Simplified example of the proposed method for $N_{\rm s} = 5$ focused on slot $i = 1$ and bus periods $m = 0$ and $m = 1$ (the control is applied to every slot but only the variables related to slot $i = 1$ are depicted).

Once the controller is selected, the closed loop bandwidth, $\omega_{\rm bw}$, has to be tuned. The closed loop-transfer function, $G_{\rm CL}$, is defined as:

$$G_{\rm CL}(s) = \frac{G(s)}{G_{\rm T}(s)} = \frac{1}{s/\omega_{\rm gc} + 1}. \tag{14}$$

One particularity of this type of controllers is that a phase margin of 90º is obtained and, for such phase margin, the gain crossover frequency is equal to the closed loop bandwidth [28], $\omega_{\rm gc} = \omega_{\rm bw}$.

Once the controller is tuned, the most direct approach would be to discretize and apply the controller with a sampling period of $1/f_{\rm sw}$. However, since the plant is based on a small-signal model it is valid near a steady-state or equilibrium operating point defined by constant R, L, $C_{\rm r}$, $f_{\rm sw}$ and D [8]. Thus, this work proposes a different approach: to divide a bus period into $N_{\rm s}$ slots which are identified with a number from 0 to $N_{\rm s} - 1$ and to control the conductance independently for every slot. To do so, at the beginning of the slot $i(m)$ (m represents the current bus period), a specific switching frequency $f_{{\rm sw},i(m)}$ is applied. During slot $i(m)$ the conductance is computed and at the end of this slot, the switching frequency that will be applied in the slot $i(m+1)$ of the following bus period is calculated and stored for future use. This process is repeated for every single slot. The main advantage of this method is that, for a specific slot $i(m)$, the bus voltage can be approximated by a dc voltage and, at steady-state, constant $f_{\rm sw}$ will be applied over time, which will result in a constant excitation level applied to the load and so, R and L will remain constant, leading to an also constant operating point around which the small-signal model is perfectly valid.

A graphical example of the proposed algorithm is shown in Fig. 3. In this case, a total number of slots $N_{\rm s} = 5$ was chosen to simplify the representation and its understanding.

In this approach, the sampling period is $T_{\rm B}$, and a closed loop bandwidth of a tenth of the bus frequency, $f_{\rm B}$, seems enough, as many of the dynamics that appear in the cooking process are generated by the user (change of power target, displacements of pots, change of temperature of the pot content, etc.). The advantage of this approach is that it will generate a variable switching-frequency profile which is adaptive in real time to any type of pot. However, given that $f_{{\rm sw},i_m}$ is

calculated independently for each slot no matter what the f_{sw} of their neighboring slots, $f_{\mathrm{sw},i-1(m)}$ and $f_{\mathrm{sw},i+1(m)}$, are, and the real grid voltage can include non-fundamental harmonic components, once the VSFP is calculated, a moving average is applied to the VSFP to generate smoother transitions of f_{sw} between slots.

By applying a backward Euler discretization, the discrete controller is expressed as:

$$w_{\mathrm{sw},i(m+1)} = w_{\mathrm{sw},i(m)} + \frac{\omega_{\mathrm{bw}} T_{\mathrm{B}}}{G_{\mathrm{g}\omega 0,i(m)}} (G_{\mathrm{T}} - G_{i(m)}) \quad (15)$$

where, let's remind that m refers to the bus period, i refers to the slot and for a single bus period, (15) should be applied N_{s} times.

In (15) the sampling period is constant and equal to T_{B}, but the gain of the plant, $G_{\mathrm{g}\omega 0,i(m)}$, still depends on the slot i. However, in the next section it will be shown that a constant value can be applied for the entire bus period and this is something that will greatly simplify the implementation of the controller in the prototype.

While the proposed method is mainly focused on the compliance with [16], the home appliances also have to comply with [17]. In this regard, it was already mentioned that different hardcoded VSFPs and their performance as SSTs were analyzed in the literature. Thus, an additional feature based on this concept was added to the proposed algorithm to force a larger variation of the switching frequency. A simple way to force a larger variation of the switching frequency without excessively penalizing the THD of the grid current is to move the whole adaptive VSFP upwards and downwards over time (between bus periods). However, by changing the switching frequency it would be difficult to ensure that the desired average power is supplied and that the conductance is kept constant. The solution is to take advantage of the high bandwidth of the proposed controller and to do it the other way around.

Therefore, our proposal is to vary the target power over time following, for instance, a triangular wave. Thus, the average power supplied to the load is controlled, the conductance controller itself adapts the switching frequency inside the bus period to ensure a constant conductance is obtained and, finally, the variation of the power over time forces a wider variation of the switching frequency which will ultimately behave as a SST and will improve the compliance with [17].

Throughout this paper, the original method, without this additional feature used as a SST, will be referred as "conductance control" or "G control" and the original method plus the SST feature will be referred as "G control + SST".

IV. Simulation Results

Most of the algorithms and new proposals in the field of DIH are simulated assuming the equivalent impedance is constant during the entire bus period [11]–[15]. As a preliminary approach or in applications based on averaging the electric magnitudes throughout a bus period or on a dc bus voltage, such procedure and simplification are logical. However, this assumption can not be made to test the proposed idea.

In this work, a simplified model of the HBSRI is simulated in Matlab/Simulink, but the simulated equivalent impedance varies with the switching frequency and with the bus voltage (see Fig. 6.(a) to gain an idea of how the impedance varies within the bus period). To do so, the load identification algorithm presented in [5] was used. This algorithm tracks the variation of the equivalent impedance due to the variation of the excitation level throughout the bus cycle. Several pots were experimentally identified with this algorithm at different switching frequencies, following a similar procedure as in [29]. The simplified model of the HBSRI assumes the switches are ideal and neither snubber capacitors nor bus capacitors are considered. The model is described through the state equation of a series RLC circuit as:

$$\frac{d}{dt}\begin{pmatrix} i_{\mathrm{L}} \\ v_{\mathrm{c}} \end{pmatrix} = \begin{pmatrix} -R/L & -1/L \\ 1/C_{\mathrm{r}} & 0 \end{pmatrix} \begin{pmatrix} i_{\mathrm{L}} \\ v_{\mathrm{c}} \end{pmatrix} + \begin{pmatrix} 1/L \\ 0 \end{pmatrix} v_{\mathrm{o}} \quad (16)$$

The fundamental sampling frequency of the simulation is set at 50 MHz and the parameters R and L are updated at that rate thanks to two two-dimensional interpolated lookup tables whose input breakpoints are v_{B} and f_{sw}. Before the simulation is launched, each lookup table is preloaded with more than 30 thousand values of R and L at different v_{B} and f_{sw}.

The bus period is divided into $N_{\mathrm{s}} = 100$ slots, but for the first and last 10 slots the control action is kept constant at its last calculated value (the accuracy in the calculation of G for such small values of v_{o} and mainly of i_{L} is not good enough). The bus voltage is an ac waveform of 230 V rms. Just for reference, with such a bus voltage, the tenth slot corresponds to a bus voltage of approximately 100 V. The bus period, T_{B} is 10 ms and the bandwidth ω_{bw} is set to $2\pi 10$ rad/s (far below the validity range of the model) .

The maximum step in f_{sw} for a specific slot between two consecutive bus periods is limited to ± 2 kHz. This value may seem high but let us remind that when the inverter is far from resonance, the gain of the plant is very small and a relatively large change on f_{sw} barely affects its operational conditions.

The results of the simulation are shown in Fig. 4, where several variables are depicted: the output voltage of the inverter and the load current, the target and measured power, the instantaneous switching frequency applied to the inverter, and the gain of the controller, k_{c}, which is calculated as:

$$k_{\mathrm{c},i(m)} = \frac{\omega_{\mathrm{bw}} T_{\mathrm{B}}}{G_{\mathrm{g}\omega 0,i(m)}} \quad (17)$$

In Fig 4.(b) the conductance is not expressed in its corresponding units. The reason is that instead of showing the value of the conductance, G, in Siemens or Ω^{-1}, it was preferred to plot the value of the conductance times the square of the rms output voltage computed during T_{B} (this is where subindex "B" comes from), $G v^2_{\mathrm{o,B,rms}}$, in watts. Given that v_{o} can be approximated by a square or a trapezoid signal and $D = 0.5$, the value $v^2_{\mathrm{o,B,rms}}$ is just a constant scale factor that, in authors' opinion, easies the interpretation of the figure by the reader.

Additionally, in Fig 4.(d) the value of the gain k_{c} is shown and it can be observed how its value gets more and more constant when a steady state is reached. This is because

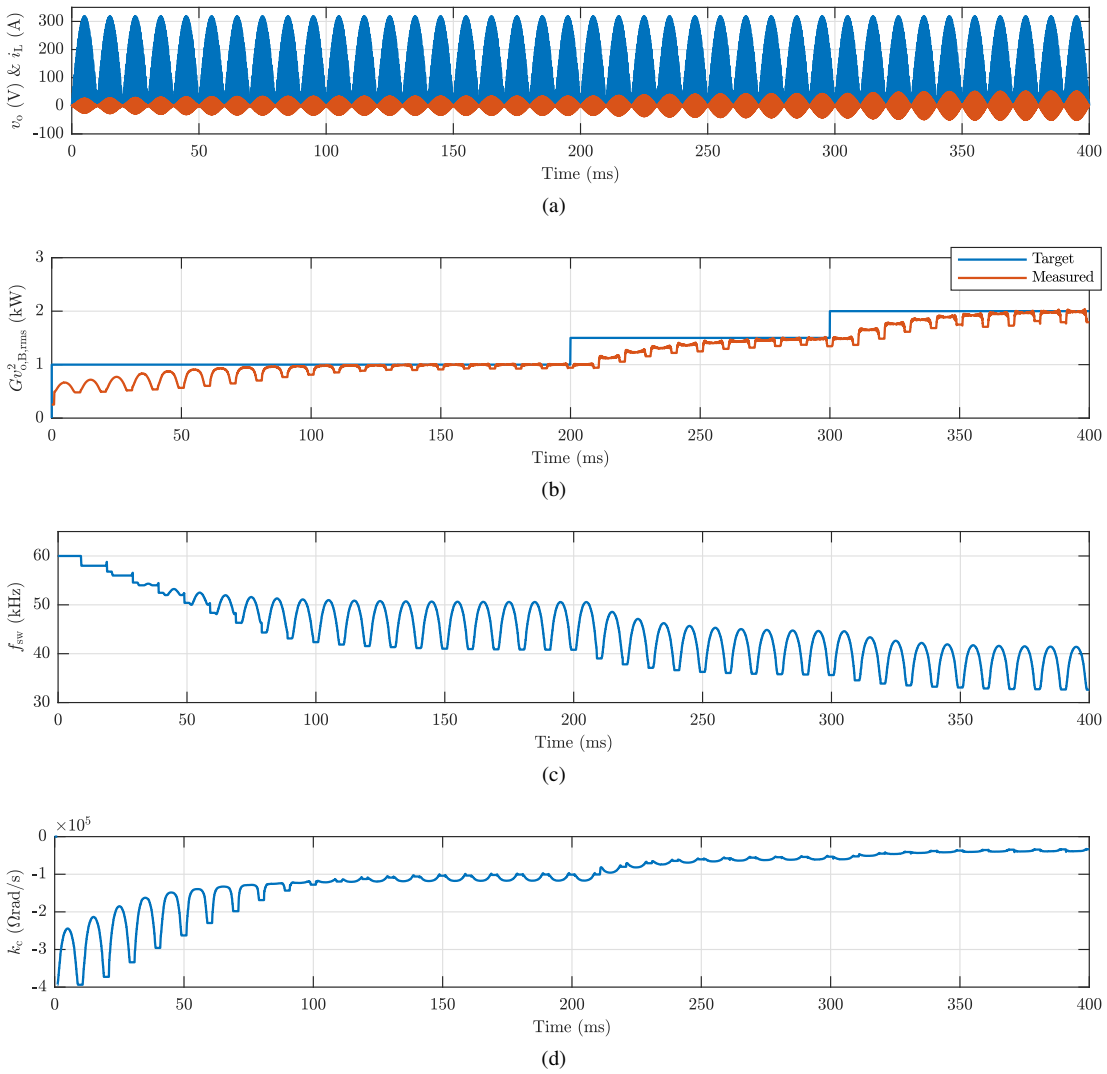


Fig. 4. Simulation results. (a) v_o and i_L. (b) Target power and measured $Gv^2_{o,B,rms}$. (c) Switching frequency. (d) Controller gain, k_c.

the application of such switching frequency also flattens the equivalent impedance within the bus period. It can be observed that in the beginning of the simulation (when constant f_{sw} is applied) the span of the controller gain is large. The uncertainty on this parameter k_c would be equivalent to changing the desired bandwidth of the controller. Nevertheless, the desired bandwidth chosen for the controller is on the safe side (a tenth of f_B with respect to the limit value of $f_B/2$ was chosen) and the action is saturated at ± 2 kHz. This is the reason why although in simulation the gain k_c of the controller is calculated for every slot, in the experimental implementation this gain will only be computed once per bus period and will remain constant for every slot of each T_B.

V. Implementation

The proposed algorithm is implemented in a prototype with a system on chip. While some parts of the prototype are directly taken from a commercial hob (inductors, vitroceramic glass, etc.), the printed circuit boards (PCBs) were specifically designed for research purposes. Two PCBs were designed: one of them mounts the power electronics circuitry and the other one mounts the conditioning and acquisition circuits. They are both connected to each other and the latter is connected to the Zynq-7020 System-on-Chip (SoC) through the commercial TE0720 System-on-Module and the TE0720 carrier board from Trenz Electronics. This SoC contains in a single chip the programmable logic (PL) and the processing system (PS) based on a dual core ARM Cortex A9.

The prototype has two independent half-bridge series resonant inverters that are connected to two inductors with an external diameter of 21 and 15 cm. For simplicity, in this work only the largest inductor is used.

The prototype also mounts LTC2315-12 analog-to-digital converters (ADCs) to digitize the grid voltage, v_{grid}, the bus voltage, v_B, the load current, i_L, and the output voltage, v_o. These 12-bit ADCs run at 2.78 Msps and are controlled form the PL through a serial peripheral interface (SPI). Moreover, the IGBTs are controlled through a phase-accumulator based direct digital synthesis (DDS) modulator. The main circuit parameters of the prototype are given in Table I.

The conductance controller is implemented in very high speed integrated circuits hardware description language

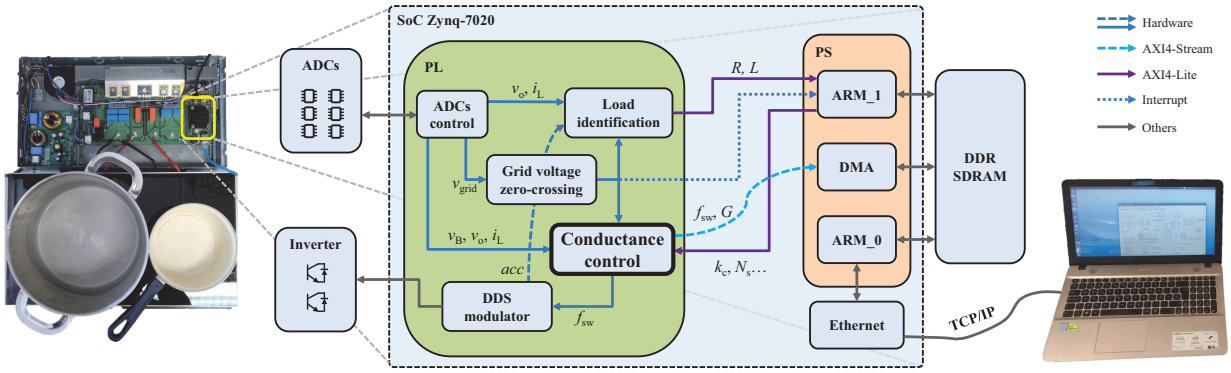


Fig. 5. Simplified block diagram of the proposed implementation.

TABLE I
PROTOTYPE CIRCUIT PARAMETERS

Symbol	Description	Value
$\hat{V}_{\mathrm{B}}$	Peak bus voltage	325 V
f_{grid}	Grid frequency	50 Hz
R	Equivalent resistance	[2, 10] Ω
L	Equivalent inductance	[10, 70] μH
C_{r}	Resonant capacitor	1080 nF
C_{B}	Bus capacitor	6.6 μF
C_{s}	Snubber capacitor	15 nF

TABLE II
DIGITAL RESOURCE UTILIZATION IN SOC

LUTs	DSPs	BRAMs	FFs
3014	40	3	5618

(VHDL). Apart from our own VHDL design, two Xilinx IP (intellectual property) cores are used: a divider generator, which is used for the calculation of G in (11) and the finite impulse response (FIR) compiler, which is used for the computation of the moving average filter of the switching frequency.

To divide the bus period into N_{s} slots, a zero-crossing detector of the grid voltage, v_{grid}, was also implemented as a separated IP core. This IP core outputs a flag when a zero-cross is detected. Then, a process counts the number of clock cycles between two zero-crossings of v_{grid} or during a bus period. By using this information, the ARM computes how many clock cycles fit into every slot, by assuming a constant number of slots N_{s}.

The VHDL implementation makes sure that (11) is applied to complete switching cycles thanks to a rising edge detector of v_{o}. This is accomplished by comparing v_{o} with $v_{\mathrm{B}}/2$, although it could also be done by detecting the zero crossings of i_{L}.

As in simulation, in the real-time implementation the number of slots N_{s} is 100. The switching frequencies of all the slots $f_{\mathrm{sw},i}$ are stored in a dual-port block random access memory (BRAM). Once enough switching frequencies are stored in the BRAM to fill the moving average filter, another process reads these switching frequencies and overwrites them after applying the filter.

Additionally, another IP core was designed to identify the average equivalent impedance $R-L$ during a bus period [5]. These values are required to compute k_{c}, which is calculated in the ARM according to (17).

The resource utilization of the whole algorithm is shown in Table II. It is worth mentioning that although the results in this paper are based on the 21 cm inductor, this implementation allows to control the conductance of two independent loads simultaneously, so that the resource estimation for one load would be approximately a half of the one shown in Table II.

To obtain the data, the conductance controller IP core is connected to a Xilinx's direct memory access (DMA) controller, which allows writing data (conductance, switching frequency, etc.) at a high rate in a double data rate synchronous dynamic random-access memory (DDR-SDRAM).

Given that the PS of the SoC is made of a dual-core ARM Cortex A9, one of the processors is used for high-level tasks such as monitoring of electrical variables, power-electronics safety processes, the computation of G_{gw0} and k_{c}, etc. The other processor runs an operating system called petalinux and it is in charge of establishing a TCP/IP communication protocol with a laptop. Here, a graphical user interface was programmed in Matlab to control the prototype, to plot the results through the monitor in real time and to save DDR-SDRAM data in the hard disk for later use. In fact, all the experimental results presented in Section VI that are based neither on oscilloscope nor on instrumentation from an electromagnetic compatibility laboratory were captured with this custom application.

A block diagram of the whole system is shown in Fig. 5, where acc states for the accumulator of the DDS modulator and is used to generate the sine and cosine signals at the switching frequency with which the first-harmonic equivalent impedance of the load is obtained.

VI. EXPERIMENTAL RESULTS

One of the reasons why the hardcoded VSFPs work for the manufacturers is that [16] states that the test should be carried out with enameled-steel pots. This type of pots shows

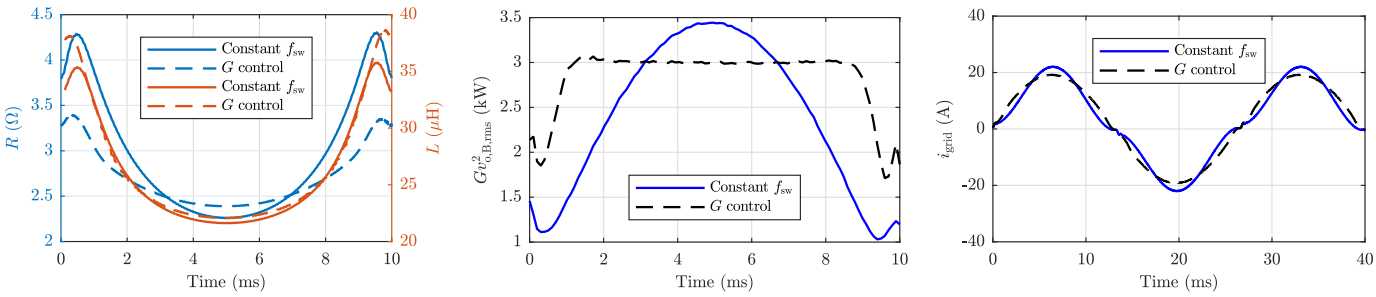


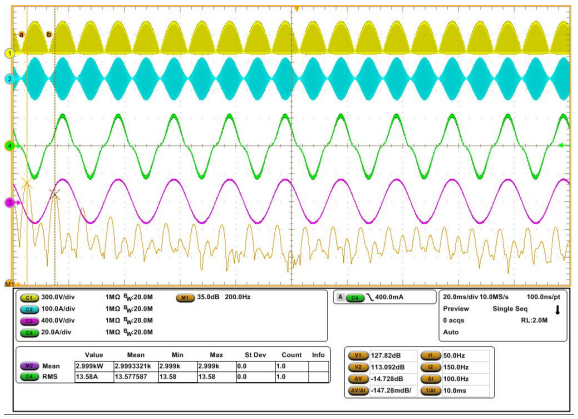
Fig. 6. Experimentally measured electrical variables for an enameled-steel pot receiving 3 kW with constant f_{sw} throughout the bus period versus applying the conductance control. (a) R and L during a bus period. (b) $Gv^2_{\mathrm{o,B,rms}}$ during a bus period. (c) i_{grid} during four bus periods.

the greatest variation of the impedance with the excitation level compared to other construction types such as sandwich or multi-layered. Thus, if a constant f_{sw} is applied during the whole bus cycle, enameled pots lead to the greatest THD of the grid current, so the regulators make sure the appliance complies in this worst-case situation. However, it is obvious that a hardcoded VSFP specifically designed for an enameled-steel pot is not optimal in terms of THD of grid current for a multi-layered pot. What is more, it could even happen that applying this VSFP to a multi-layered pot leads to a worse THD than maintaining a constant f_{sw} during the bus cycle.

In Fig. 6 a comparison between the approach based on applying a constant f_{sw} during T_{B} and the one based on applying the proposed conductance control in terms of equivalent $R-L$, conductance (expressed in watts as before) and grid current is shown. It is worth focusing the attention on the grid current and observe how the conductance control greatly reduces its harmonic distortion and its maximum values. In both cases the power supplied to the pot is 3 kW. A similar behavior can be observed in Fig. 7, where waveforms captured with the oscilloscope are shown for two situations: constant switching frequency vs the proposed conductance control. The power supplied is the same in both cases (see "mean" measurement at the bottom of the oscilloscope screenshots). The magnitude of the i_{grid} harmonics up to 2 kHz is also plotted.

The algorithm was also tested in an electromagnetic compatibility (EMC) laboratory according to the requirements and recommendations stated in [16], [17]. In Fig. 8, the magnitude of the grid-current average harmonics from 2nd to 40th are shown for a power of 3.4 kW supplied to an enameled-steel pot. Bars are represented with respect to the limits in the standard: positive bars means the test failed and viceversa; the more negative the bar is, the more margin with respect to the limit there is. It can be seen how the proposed approach greatly improves the third harmonic of the grid current by reducing it by more than 2 A. This could also be anticipated looking at the waveform shown in Fig. 6.(c) and Fig. 7.

Additionally, Table III shows the THD of the grid current for three types of pots when a constant f_{sw} is applied during the entire bus period and when the proposed conductance control is applied. The proposed approach is able to reduce the THD by a factor of more than 7 under the tested conditions (in this case, the supplied power is 3 kW).



(a)

(b)

Fig. 7. Waveforms of inverter signals v_{o} (C1, yellow), i_{L} (C2, cyan) and grid signals i_{grid} (C4, green) and v_{grid} (C3, purple). The magnitude of i_{grid} harmonics up to 2 kHz are shown in orange color and cursors are placed at 50 and 150 Hz. (a) Constant f_{sw}. (b) Conductance control.

TABLE III
COMPARISON OF GRID CURRENT THD FOR THREE TYPES OF POTS ($P = 3$ KW IN ALL CASES)

Method	Enameled steel	Multi-layered	Sandwich
Constant f_{sw}	17.43 %	7.09 %	7.3 %
G control	2.33 %	0.89 %	0.86 %

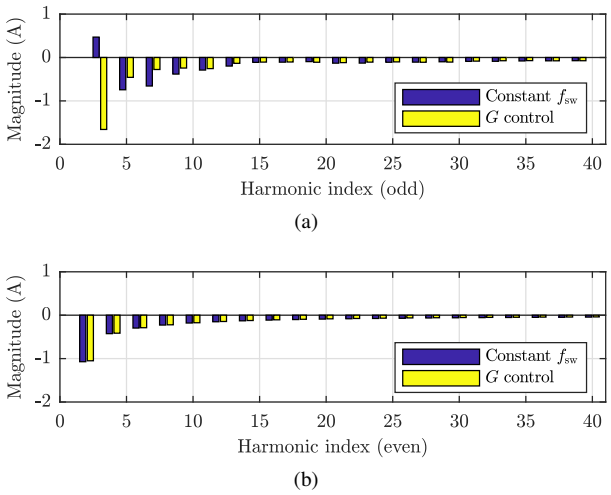


Fig. 8. Magnitude (relative to the limits of standard) of grid-current average harmonics when constant f_{sw} and when conductance control are applied. (a) Odd harmonics. (b) Even harmonics.

It was already mentioned that one of the advantages of the proposed method is that it adapts the switching frequency in real time, and it does so adaptively for any type of pot. An example of this statement can be observed in Fig. 9, where the average power supplied during a bus cycle and the switching frequency are shown when a multi-layered pot is manually substituted by an enameled-steel pot. This figure gives an idea of the response time of the controller and the different operating conditions of the inverter for different types of pots. Additionally, in Fig. 10 two zoom-ins of Fig. 9 are shown. It can be seen that within the bus cycle and in steady state, the conductance is kept constant, while the span of the switching frequency is completely different from one pot to another.

In order to experimentally support (with oscilloscope measurements) the promised improvement in terms of time response of the proposed method, in Fig. 11, the grid current is shown when the traditional method is applied (average power is computed during T_{B} and f_{sw} is modified upwards or downwards by a constant step of 100 Hz every T_{B}) and when the proposed conductance control is applied. The starting power target is set at 500 W and it is suddenly raised to 2 kW. The great difference in time response can be easily observed in i_{L} and i_{grid} waveforms.

Regarding the spread-spectrum technique feature, after several experimental measurements, a peak-to-peak value, $\Delta P = 400$ W and a period of one second was chosen for the triangular wave of the power target due to the good EMC results obtained with this configuration. To complete the explanation of the SST feature, in Fig. 12, the power and the switching frequency are shown for $\Delta P = 1$ kW and a period of one second (ΔP was intentionally oversized for the figure in order to easier observe its effect on the switching frequency).

The results of the tests regarding [17] and carried out in the EMC laboratory are shown in Table IV, where the quasi-peak values for the second harmonic of f_{sw} (this is the most problematic harmonic for our prototype due to the split of the resonant capacitor, see Fig. 1) are shown in dBμV. Once again, a positive margin means that the test did not comply with the

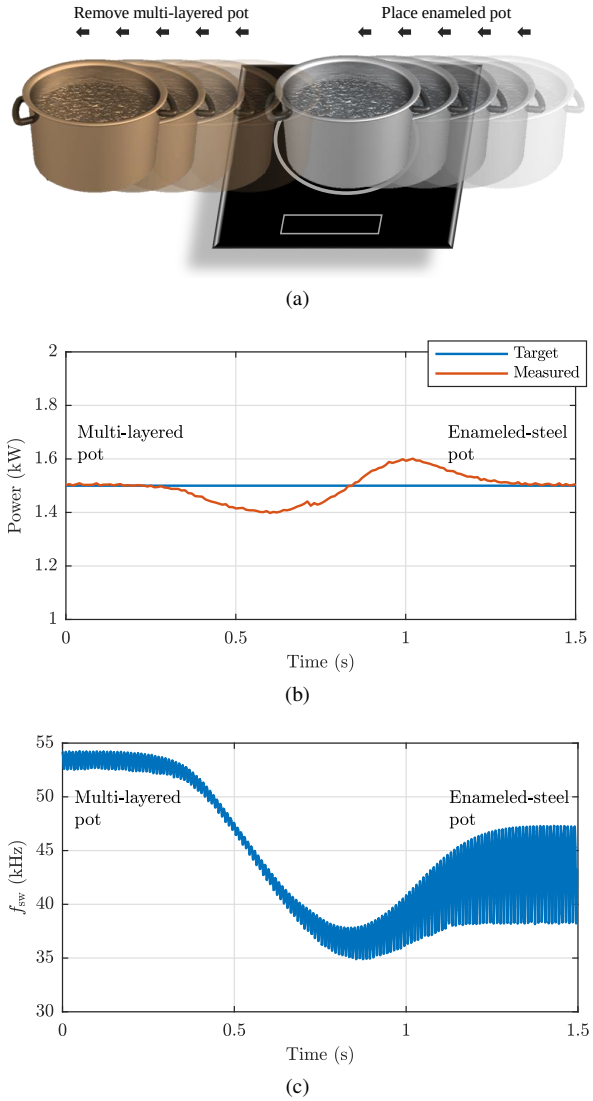


Fig. 9. Evolution of power and switching frequency when a multi-layered pot is manually substituted by an enameled-steel pot. (a) Graphical representation of the pot swapping. (b) Target and measured power (averaged during the bus period). (c) Instantaneous switching frequency.

TABLE IV
EMC RESULTS (QUASI-PEAK OF SECOND HARMONIC OF SWITCHING FREQUENCY) FOR A MULTI-LAYERED POT ($P = 3$ KW)

Method	Quasi-Peak	Quasi-Peak Limit	Margin
Constant f_{sw}	93.6	87.7	5.9
G control	87.1	87.6	-0.5
G control + SST	79.6	87.8	-8.2

standard and viceversa. It can be seen that "G control + SST" leads to an improvement of more than 14 dBμV with respect to maintaining a constant switching frequency. This table is shown for a multi-layered pot because, among the pots that were tested, the worst results were obtained for this type of pots. The results for the THD of the grid current when the "G control + SST" method is applied are not shown because they are almost identical to the "G control" alone.

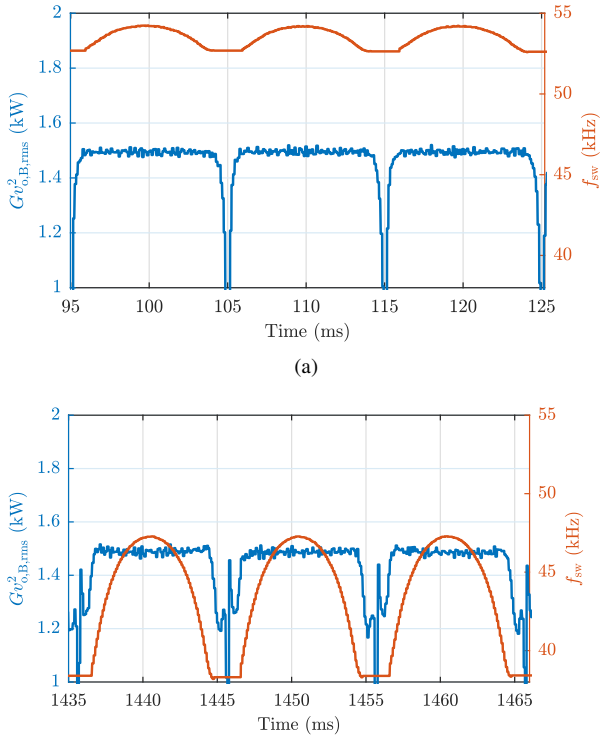


Fig. 10. Zoom-in of conductance and f_{sw} of Fig. 9. It can be observed that at low v_{B} voltages the calculation of the conductance is not accurate, and this is the reason why the conductance control is deactivated under this situation. (a) Multi-layered pot. (b) Enameled-steel pot.

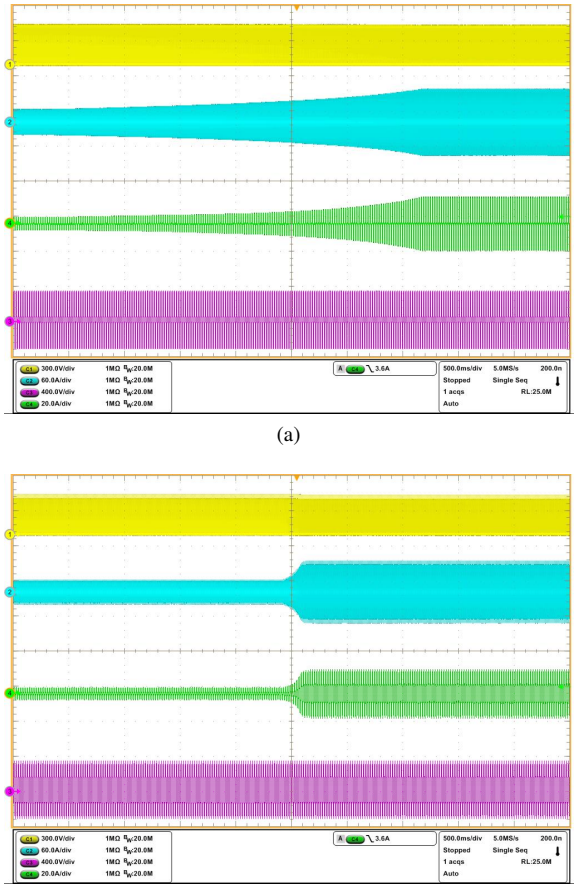


Fig. 11. Waveforms of of inverter signals v_{o} (C1, yellow), i_{L} (C2, cyan) and grid signals i_{grid} (C4, green) and v_{grid} (C3, purple) when the power target is raised from 500 W to 2 kW. (a) Traditional approach with f_{sw} step of 100 Hz between bus periods. (b) Proposed model-based conductance controller.

Finally, a comparison between the proposed "G control + SST" and the constant switching frequency approach regarding conducted emissions is shown in Fig. 13. In this figure, the maximum peak of both line and neutral voltages are shown from 9 kHz to 30 MHz. The quasi peak of the second harmonic of the switching frequency is shown with a blue cross. These results are obtained with a multi-layered pot (quasi peak values can be compared to the ones reported in Table IV). Note that the high magnitudes at very high frequencies (above tens of MHz) are not due to the conductance controller, they also appear when constant switching frequency is applied and can appear due to the influence of the SoC clock, noise introduced from the PC to the prototype, non-optimal design of the PCB, etc.

VII. Conclusion

In this paper, a controller to reduce the harmonic current emissions of the grid and the emissions of radio-frequency disturbances above 9 kHz of induction heating appliances has been proposed.

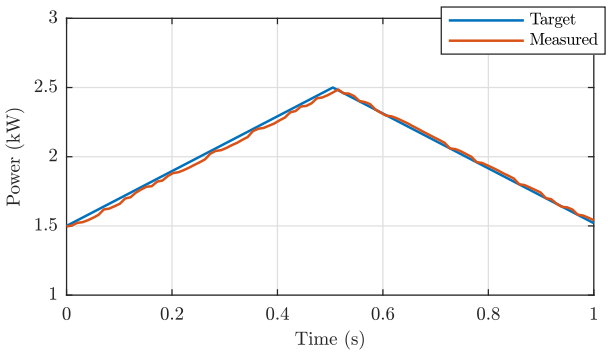
This is the first control proposed in the field of DIH that actively tries to reduce the harmonic distortion of the grid current by just modifying the switching frequency within the bus cycle without using a hardcoded VSFP. Moreover, the fact of reducing the THD of the grid current without requiring additional power electronics is of great importance for such application given its well-established low-cost context.

The controller is based on a reduced EDF-based model which is updated in real time depending on the equivalent load thanks to a first-harmonic impedance identification. The obtained analytical expressions are simple enough to be implemented in the state-of-the-art technology and the algorithm does not require an unmanageable quantity of logic or processing resources, as it has been shown through its implementation in the real device.

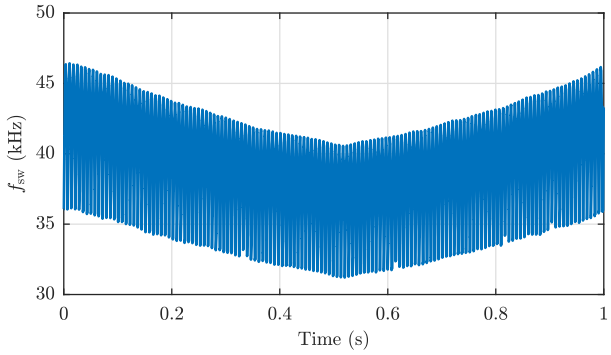
Moreover, the bandwidth of the controller has been greatly improved with respect to the traditional implementations, and this is a clear advantage due to the user-related dynamics involved in domestic induction heating such as pot lifting or pot swapping (see Fig. 9).

Finally, by overlapping two features: the conductance control itself, which reduces the harmonic distortion of the grid current, and the spread spectrum technique (SST) that forces a low-frequency power variation, which spans the radio-frequency disturbances above 9 kHz, promising results are obtained. Compared to maintaining a constant switching frequency during T_{B}, the THD of the grid current is reduced by a factor of more than seven when high powers are supplied. Moreover, the experimental results show that the quasi-peak limit is reduced by more than 14 dBμV in the worst-case. These two facts lead to a more comfortable margin and relaxed compliance with the standards.

In summary, these are the main advantages of the proposed

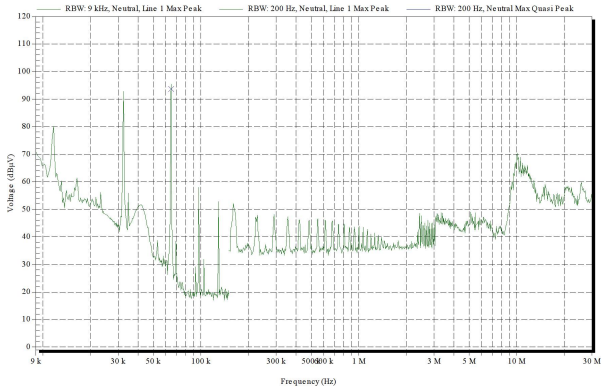


(a)

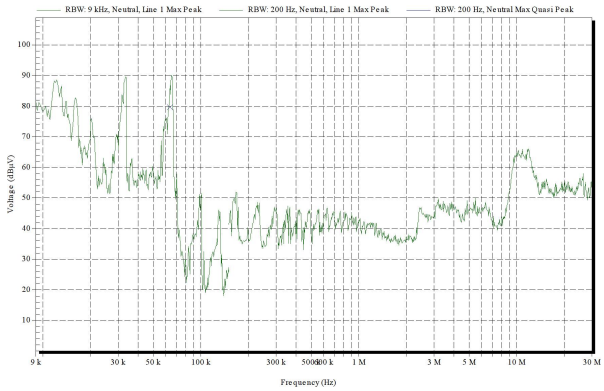


(b)

Fig. 12. Power and switching frequency when "G control + SST" is applied for an average power of 2 kW, $\Delta P = 1$ kW and a period of one second. (a) Target and measured power. (b) Instantaneous switching frequency.



(a)



(b)

Fig. 13. Conducted emissions in the range 9 kHz - 30 MHz with a multi-layered pot and a supplied power of 3 kW. (a) Constant switching frequency of 32.2 kHz. (b) G control + SST.

controller:

- Reduction of grid-current THD (better standard compliance).
- Wider spread of radio-frequency disturbances above 9 kHz (better standard compliance).
- Improved bandwidth and faster response times.
- Adaptive switching frequency within the bus cycle with any type of pot and without using hardcoded VSFPs.
- Reduction of maximum currents through power electronics devices and through inductor.

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