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Electrical optimization of AlGaN/GaN devices for power and RF applications

Electrical Optimization of AlGaN/GaN Devices for Power and RF Applications

Hard-Switching, Trapping Effects, Breakdown and Gate Leakage

By

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Abstract

The reliability issues of AlGaN/GaN HEMTs for power and RF applications have attracted much attention from the research community in order to improve their application range. In this thesis, multiple reliability issues of AlGaN/GaN HEMTs are covered with detailed characterizations, simulations and analysis, which include hard-switching, trapping effects, breakdown and gate leakages.

By comparing a set of wafers with different SiN_x passivation stoichiometries, HEMTs with Si-rich passivation layer stand out and show negligible dynamic ON-resistance after stress. In measurements of the hard- and soft-switching with tens of nano seconds switching time, it turned out that hard-switching would lead to significant self-heating and produce hot electrons. However, the temperature cools down after a few hundreds nano seconds after the switching while the surface charge trapping is the dominant reason for the dynamic ON-resistance increase.

The study of multiple types of stress including ON-state, OFF-state and substrate bias were performed on the same devices. The dynamic ON-resistance shows a 60% increase after the ON-state stress compared to OFF-state stress on the sample with a stoichiometric Si_3N_4 passivation layer. The devices with additional sense node contacts enable the potential mapping between the gate and drain for ON-state and OFF-state, which helps to determine the distribution the charge trapping. By comparing the trap information extracted from the transient dynamic ON-resistance, the charge trapping appeared after the ON-state stress is proven to be associated with the deep buffer traps, likely due to the carbon acceptors in the GaN. Moreover, electroluminescence measurements show agreements with the potential mapping, and it also implies that the field plates possibly blocked the light emitted from the gate edge.

RF AlGaN/GaN-on-SiC HEMTs are used for the breakdown study. The drain injected technique is used for avoiding device degradation while measuring the breakdown voltage as a function of the gate voltage. The drain current was kept as a constant while the gate voltage was swept during the measurements. The devices show a 2-stage breakdown feature as the first breakdown plateau is associated with the punch-through within the GaN channel layer under the gate, whereas the second breakdown plateau is due to the increasing carbon doping density as the punch-through current is forced down to the doped GaN layer. The electroluminescence results suggest that additional leakage paths are triggered with a high drain bias.

Finally, a gate leakage study is carried out on the MIS AlGaN/GaN HEMTs. The bell-shape gate leakage curves for semi-ON state suggest the gate current is contributed by the electron current and hole current independently. The electrons mainly pass through the SiN_x barrier by Poole–Frenkel emission whereas the hole current comes from the impact ionization. In addition, the peak shift of the bell shapes between the electroluminescence and the gate leakage indicates a potential competition mechanism.

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Author's declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

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CHAPTER 1

INTRODUCTION

Life has been dramatically changed since the information revolution as more than 7 billion people around the world are connected together through the internet. Nowadays, not only the human beings, but also machines, buildings, even animals and most of physical objects on the earth can be interacted through built-in sensors or chips theoretically, which is known as internet of things (IoT) [1]. This branch of fast growing technology gives more and more convenience for human's daily life since 21st century. How could it possibly happen? A big thanks goes to the invention of semiconductor devices.

The first semiconductor transistor, a bipolar point-contact transistor, was developed by John Bardeen, Walter Hauser Brattain and William Shockley at Bell Labs in 1947 [2, 3]. A transistor can either act as a switch or an amplifier and therefore, it helps to builds more complex circuits for more advanced applications. In the modern society, the big family of transistor has been classified into several categories according to the specific demands. Some of the transistors are fabricated into nano-range (gate pitch) to increase the density of integrated circuit (IC); Some of the transistors are made to be suitable for high frequency operation for 5G applications; Some of the transistors are designed to tolerate the high power environment for device charging. Sometimes different demands are mixed in some situations and the traditional silicon device faces strong challenges. Therefore, a lot of semiconductor materials (i.e. GaAs, SiC, GaN, Ga_2O_3...) have attracted the research community for investigation in order to meet the criteria of these complicated situations. In particular, AlGaN/GaN high electron mobility transistors (HEMTs) have exhibited both a high electron mobility (up to 2000 $cm^2V^{-1}s^{-1}$ [4]) due to the 2 dimensional electron gas (2DEG), and a high breakdown voltage (3 MV/cm [5]) due to the wide bandgap. All these features are making the GaN HEMT a promising candidate for high power and radio frequency (RF) applications.

1.1 Developments and Challenges for AlGaN/GaN HEMT

The development of AlGaN/GaN HEMTs has started since 1990s and many researchers have contributed their knowledge to it. In early 1990s, the study about how to grow the GaN thin film by molecular-beam epitaxy (MBE) and chemical vapor deposition (CVD) techniques was carried out [6], and it enabled the technologies about the growth of bulk GaN and the AlGaN/GaN heterojunction. Khan et al. [7] reported the first HEMT with AlGaN/GaN heterojunction in 1993 and it was grown on the sapphire. At that time, with a large dislocation density in the GaN epitaxy and a poor substrate thermal conductivity, making it unsuitable for real applications. Soon in 1997, the first GaN-on-SiC HEMT is developed by Binari et al. [8] in order to improve the device performance. The AlN nucleation layer was deposited above the SiC, which reduces the lattice mismatch between the substrate and the GaN layer, therefore, it successfully mitigates the dislocation density in GaN. On the mean time, the SiC substrate with a high thermal conductivity helps to improve the thermal dissipation rate. However, with a relatively high cost for the SiC substrate, the development of GaN HEMTs is mainly pushed by the defense industry. In 2001, Chumbes et al. [9] developed the first GaN-on-Si HEMT and a thin GaN layer was adopted to prevent the substrate cracking caused by the different thermal coefficients and the lattice mismatch. The AlN nucleation layer and the AlGaN strain relief layer are together to make the GaN layer strain-free in nowadays [10]. The major advantage of use the Si substrate is its low cost compared to SiC.

Despite the development in device fabrication of, there are other studies related to the device application and reliability. Khan et al. [11] developed the enhanced-mode (E-mode) GaN HEMTs, also known as the normally-off GaN HEMTs, with a thin AlGaN barrier (10 nm) in 1995. The major advantage of the E-mode device over the depletion-mode (D-mode) device is that it allows the amplifier circuit with single-polarity voltage supply [12]. The E-mode GaN HEMTs can also be achieved by the recessed gate[13], the Fluorine implantation [14] and the p-gate [15]. Carbon is doped to the GaN buffer layer to reduce the vertical leakage in power GaN devices [16, 17], as carbon acceptors in GaN pinned the Fermi level in the mid gap, and therefore increase the GaN buffer resistivity. However, carbon in the GaN buffer layer also induces the buffer charge trapping [18], which leads to the dynamic R_{ON} (R_{ON}) increase, so it is a trade-off for the vertical leakage and the dynamic R_{ON} with a C-doped GaN buffer layer. Fe is also a common type of dopant to make the GaN buffer semi-insulating [19]. For the some RF GaN HEMTs, ensuring the linearity of waveform is more important than controlling the leakage, therefore, Fe is a better choice than C, as Fe will not lead to the significant dynamic R_{ON} increase as C. GaN HEMTs used to suffer from the surface charge trapping as it acts as a virtual gate to deplete the 2DEG after stress. In 2001, Vetury et al. [20] found that by using the sillicon nitride passivation layer above the AlGaN barrier, the surface states in GaN HEMTs can be suppressed. To increase the breakdown voltage of the GaN HEMTs, Karmalkar et al. [21] used the field plate to smooth the electric field, avoiding the a field peak in vicinity of the gate edge in 2001.

In 2014, GaN material becomes a famous semiconductor since the invention of the blue LED by Akasaki, Amano and Nakamura, and a Nobel Price in Physics was awarded as it enables white light generation with a high efficiency [22]. This exciting news also attracted more researches on the GaN/HEMT technology in the following years. Recently, after nearly 30 years development of the AlGaN/GaN HEMTs technology, its commercialization path is mature and people all around the world have already benefited from it. According to the Yole Développement market report 2021 [23], the power GaN market has achieved around $46 million in 2020 and will surpass $1.1 billion in 2026, with a fast growing market in GaN-based chargers for consumers as well as for the telecom and automotive applications.

Several semiconductors have been considered for the power application, such as the power converter which modulate the voltage or power, a good transistor should have a low ON-resistance and a high breakdown voltage [24]. The device with a low ON-resistance will dissipate less heating energy during the ON-state and therefore increase the energy efficiency. The breakdown field of a semiconductor is associated with the band gap as it determines the energy required for triggering an electron from the valence band to the conduction band whereas the ON-resistance mainly depends on the carrier mobility and carrier density. β - Ga_20_3 is a potential semiconductor for the high power application which has a breakdown field around 8 MV/cm while the disadvantages of β - Ga_20_3 are the low electron mobility (300 $cm^2V^{-1}s^{-1}$) and low thermal conductivity (10 - 30 W/(m·k)) [25, 26]. Therefore, it is only suitable for some specific applications and it is at the early stage of researching. Diamond shows both the high breakdown field (10 MV/cm) and the high electron mobility (4500 $cm^2V^{-1}s^{-1}$) simultaneously [27], making it the best material for the power application theoretically, but since it lacks of n-type dopants and has a relatively high resistance, it is unsuitable for making good power devices currently. For the RF application, such as the wireless networks, the ideal semiconductor should have a high carrier mobility to enable the fast switching with a low ON-resistance. GaAs and InP show electron mobilites of 8500 $cm^2V^{-1}s^{-1}$ and 5400 $cm^2V^{-1}s^{-1}$ respectively, making than suitable for working with a frequency range of GHz. However, they have much narrow bandgaps compared to GaN ($E_{g,\,GaAs}$ = 1.42 eV, $E_{g,\,InP}$ = 1.34 eV), which makes them more vulnerable for under the high voltage. Hence, GaN HEMTs are more suitable for the high power RF application (i.e. 5G base station).

Apart from the recent developments of the AlGaN/GaN HEMT technology, there is still some space for pushing the device performance to the limit of the GaN material. There are many challenges regarding the device reliability that wait to be solved, such as the dynamic R_{ON} increase (also known as the current collapse) after device stress [28], the instability of threshold voltage [29], the high channel temperature during the high power application [30].

1.2 Thesis Structure

This thesis mainly focuses on the the electric reliability issues of GaN HEMTs, such as hard-switching, buffer charge trapping and breakdown and also the physical mechanisms behind the gate leakage and electroluminescence (EL). Possible solutions on improve device performance have been outlined based on the analysis in the study. Both of power and RF devices are chosen for investigation.

Chapter 2 introduces the theoretical background of AlGaN/GaN HEMTs and their applications. Chapter 3 covers the characterization techniques used in this thesis. In Chapter 4, a set of power AlGaN/GaN-on-Si HEMTs with different SiN_x stoichiometry for passivation layers are used for investigating the reliability issues for hard- and soft-switching conditions. The switching time in pulsed IV measurement has been controlled precisely to show how the dynamic R_{ON} is affected by the switching type. With the aid of simulation tools, the possible mechanism of self-heating effect is ruled out as it the temperature cools down very fast after hard-switching but the surface charge trapping is more likely to be present as it shows a small recovery time. The discussion of how to improve the device performance under hard-switching with a Si-rich passivation layer is presented in this study. In Chapter 5, the same set of devices from Chapter 4 are used to investigate the buffer charge trapping under different stress conditions. Three stress conditions are discussed in this chapter, including the OFF-state stress, ON-state stress and the back bias stress, and they show different types of R_{ON} recovery curves. Based on the experimental results, analysis of the reason behind the possible trapping mechanisms is illustrated and it helps to show how to mitigate the dynamic R_{ON} under stress conditions. Chapter 6 reports the breakdown mechanism in RF AlGaN/GaN-on-SiC HEMTs by adopting the drain injected technique, which helps to prevent a permanent device failure while observing how the drain breakdown voltage evolves with the gate voltages. The breakdown measurements show apparent two-stage breakdown behaviour and the electroluminescence measurements show aligned results. Throughout the analysis of measurements and simulation, a complete picture of two-stage breakdown mechanism is formed. The difference of carbon doping density is the primary reason while the localized leakage current path triggered under high voltages is the the side effect shown in the electroluminescence measurements. Breakdown is a crucial regime for transistor reliability and this study gives a hint of RF GaN HEMTs optimization. Chapter 7 discusses the origin of the gate leakage current in metal-insulator-semiconductor (MIS) GaN HEMTs, and its relationship with the electroluminescence. An additional SiN_x passivation layer is under the gate metal to suppress the gate leakage [31], thus leads to a big reduction in electron current through the gate but the hole current remains. The electrons pass the SiN_x through the Poole-Frenkel emission whereas the holes can pass freely into the gate with almost no barrier under the negative gate voltage. Therefore, the hole current reflects the impact ionization rate within the device. The electroluminescence has been proven to be a consequence of the Bremsstrahlung effect in GaN HEMTs [32]. The obvious mismatch of the bell shape curves between the electroluminescence

and gate leakage current against the gate voltages hint a physical mechanism behind the GaN HEMTs, that the Bremsstrahlung effect and the impact ionization effect occurs in different domains. The Bremsstrahlung effect is more likely to take effect when carrier density is low while the impact ionization effect becomes dominant when the carrier density is higher. This study improves the physical understanding of the electroluminescence and gate leakage in GaN HEMTs and gives a suggestions for controlling the gate leakage through MIS structures. Conclusions of this thesis and future outlook of research on GaN HEMTs are summarized in Chapter 8.

CHAPTER 2

THEORETICAL BACKGROUND

In this chapter, the physical background of gallium nitride properties and the structure of AlGaN/GaN HEMTs and device fabrication methodologies are presented. In order to explain the study on AlGaN/GaN HEMTs in later chapter, the device physics such as the electroluminescence, the trapping effect, the self-heating effect, the transport mechanism and impact ionization are included. Some relevant reliability issues and the industrial applications are also illustrated for understanding the major challenges in AlGaN/GaN HEMTs.

2.1 Gallium Nitride

2.1.1 GaN Properties

Gallium nitride is a wide bandgap III-V semiconductor that has a crystal structure of zinc blende or wurtzite. In the zinc blende structure, the Ga atoms form a fcc lattice whereas the wurtzite structure shows a hcp lattice of Ga atoms. In both crystal structures, the N atoms occupy the tetrahedral vacancies as each N atoms have 4 nearest Ga neighbors in connection. The symmetry groups of zinc blende and wurtzite are $F\bar{4}3m$ and $P6_3mc$ respectively.

For GaN devices, the wurtzite structure is widely used as it is thermodynamically more stable than zinc blende, which is determined by the first-principles calculation [34]. The primitive cell of the wurtzite GaN crystal is depicted in Figure 2.1 and the structure has a six fold screw symmetry, a mirror plane and a glide plane. However, in wurtzite GaN structure, the crystal has no central symmetry which means that the crystal structure can not be recovered by exchanging the positions of atoms through a central inversion in a primitive cell. Considering that the electronegativity of Ga and N elements are different, the wurtzite GaN has an intrinsic polarization and is piezoelectric [35]. It also causes the differences of GaN growth on the (0001) and $(000\bar{1})$

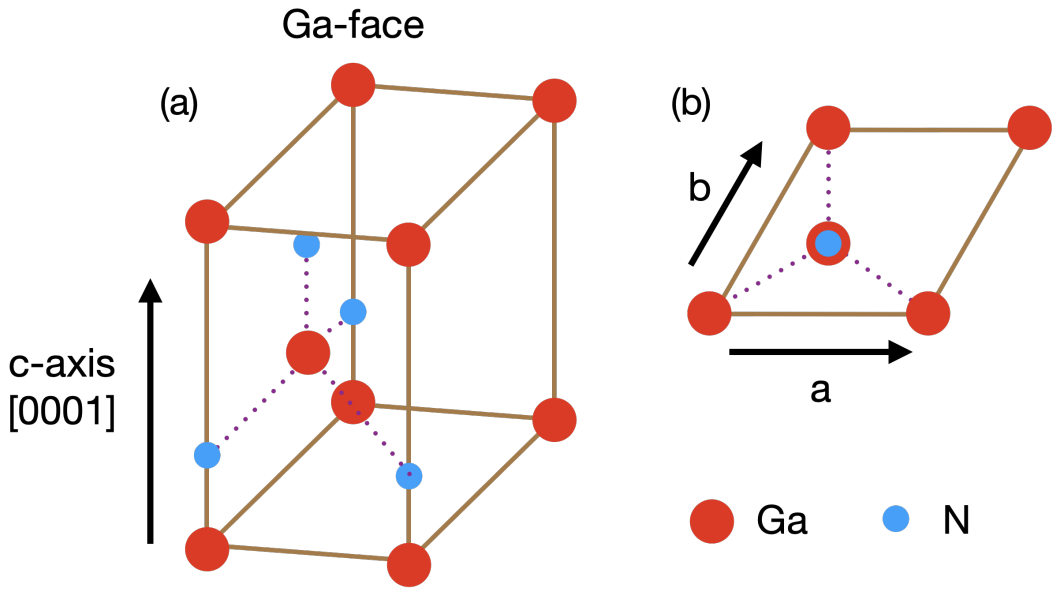

FIGURE 2.1. (a) Primitive cell of the hexagonal wurtzite GaN structure along the c-axis direction, showing the positions of Ga and N atoms. The Ga-face is on the top. (b) A top view of the primitive cell from the Ga-face.

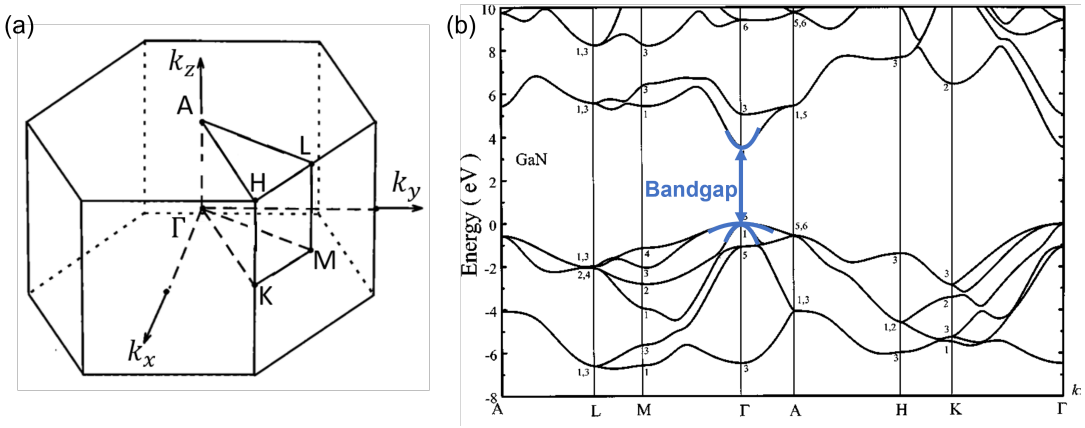

FIGURE 2.2. (a) First Brillouin zone of the wurtzite GaN structure with high symmetry points in reciprocal space. (b) Band structure of wurtzite GaN structure along high symmetry points. These two figures are adapted from [33].

plane. The [0001] direction and (0001) plane are referred as Ga-polar and Ga-face, whereas the [000$\bar{1}$] direction and (000$\bar{1}$) plane correspond to N-polar and N-face respectively. GaN can be either grown on the Ga-face or the N-face as they show different surface chemical properties and adatom mobilities [36]. Most of GaN HEMTs are fabricated on the Ga-face with a few reports about N-face devices [37]. Throughout this thesis, the Ga-face HEMTs are used for study.

Many useful electronic properties of GaN can be obtained from the energy band structure.

In Figure 2.2 (a), the first Brillouin zone in reciprocal space (also known as **k** space) of GaN is illustrated. **k** is the wave vector of the electron wave in the periodical crystal structure. The Γ point has zero momentum. The band structure can be derived by solving the Schrödinger equation with the electron wave function and the periodical crystal potential field. The energy band structure of GaN along **k** with the high symmetry points highlighted is shown in 2.2 (b). The bandgap sits between the top of the valence band and the bottom of the conduction band. The wurtzite GaN has a direct bandgap just at the Γ point and the bandgap is 3.44 eV [38].

The carrier mobility μ is an important parameter for semiconductor materials and it is determined by the equation below

$$\mu = \frac{e\tau_c}{m^*} \tag{2.1}$$

where e is the electron charge, τ_c is the mean free time for the carrier, m^* is the effective mass. Therefore, the carrier mobility is inversely proportional to the effective carrier mass and the carrier mass is inversely proportional to the band curvature. For intrinsic bulk GaN, the effective electron masses differs along the Γ-M and Γ-A directions due to the different curvatures of the conduction band in Figure 2.2 (b). First-principles calculation shows that $m^*_{e\perp}$ = 0.18m$_0$, $m^*_{e\parallel}$ = 0.2m$_0$, where $m^*_{e\perp}$ is the electron mass along the Γ-M direction, $m^*_{e\perp}$ is the electron mass along the Γ-A direction and m$_0$ is the free electron mass [39]. The hole effective masses at the Γ point splits with the valence bands, and the holes are usually heavier than the electrons so they are not the minority carriers in GaN devices as they show relatively small mobilites.

Semiconductor materials also suffer from breakdown under a high electric field due to impact ionization. According to [40], the critical electric field of a direct bandgap semiconductor has been derived as a function of bandgap

$$E_c(V/cm) = 1.73 \times 10^5 E_g(eV)^{2.5} \tag{2.2}$$

where E$_c$ is the value of critical electric field and E$_g$ is the value of bandgap. GaN has a bandgap of 3.44 eV [38], and a critical electric field of 3 MV/cm [5]. It makes GaN suitable for high power applications.

2.1.2 GaN and Other Semiconductors

Each semiconductor material has its own unique feature and can fit for different applications. For the power application, the transistor should have a high breakdown voltage and a low ON-resistance, which demands the semiconductor to have a high critical field and a high carrier mobility. Many wide bandgap semiconductors have been investigated for power applications. The properties of major wide bandgap semiconductor materials are shown in Table 2.1. The semiconductors are usually described with the Baliga's figure of merit (BFOM) [41] as follows,

$$BFOM = \epsilon\mu {E_c}^3 \tag{2.3}$$

Table 2.1: Comparison of bulk semiconductor material properties [5, 25, 27].

	Si	GaAs	4H-SiC	GaN	β - Ga_20_3	Diamond
Bandgap (eV)	1.1	1.4	3.3	3.4	4.9	5.5
Dielectric Constant	11.8	12.1	10	9.5	10	5.3
Electron Mobility ($cm^2V^{-1}s^{-1}$)	1350	8500	720	900	300	4500
Breakdown Field (MV/cm)	0.3	0.4	2	3	8	10
Baliga figure of merit (BFOM)	1	17	134	537	3444	51627

where ϵ is the dielectric constant. In Table 2.1, BFOM is normalized to that of Si.

Si is the most common and widely used semiconductor, however, it is not good for high power application due to its relatively low breakdown field. GaAs has a higher electron mobility than other material with a low breakdown field, making it a suitable for the RF application. SiC has determined its advantages not only due to its cheap fabrication price, but also the high thermal conductivity. In some power switching circuits, the devices will generate a large amount of joule heating energy during the switching, thus they require a high thermal dissipation rate to stabilize the temperature. GaN is a more promising wide bandgap semiconductor than SiC in many circumstances. Although its bulk electron mobility is only around 900 $cm^2V^{-1}s^{-1}$, the polarization nature of GaN crystal leads to the formation of 2DEG which has a electron mobility up to 2000 $cm^2V^{-1}s^{-1}$ at room temperature [4] and a high electron density. However, the GaN fabrication is expensive than the previous semiconductors, and it usually consists of a large dislocation density, making it hard for commercialization. β - Ga_20_3 is a potential semiconductor for future high power application which has a breakdown field around 8 MV/cm. The disadvantages of β - Ga_20_3 are the low electron mobility and low thermal conductivity. Therefore, it is only suitable for some specific applications and it is at the early stage of researching. Diamond materials have a high breakdown field and a high mobility simultaneously, making it the best material for the power application theoretically, but since it lacks of n-type dopants and shows a high resistance due to the 0.3 eV deep acceptor, it is hard to make good commercial devices yet.

For the RF application, the ideal semiconductor should have a high carrier mobility to enable the fast switching and low resistance. GaAs and InP (1.34 eV) have exhibited their advantages in the RF application due to their high electron mobility. However, with relatively low bandgaps, GaAs and InP (5400 $cm^2V^{-1}s^{-1}$) are less appropriate for the high power RF application, such as the power amplifier used for 5G base station. Thanks to the wide bandgap of GaN and the high electron density within the 2DEG of AlGaN/GaN heterojunction, GaN becomes a promising candidate for the high power RF application. Micovic et al. have shown the GaN HEMTs with a cutoff frequency larger than 500 GHz and a similar RF gain with GaAs and InP in power

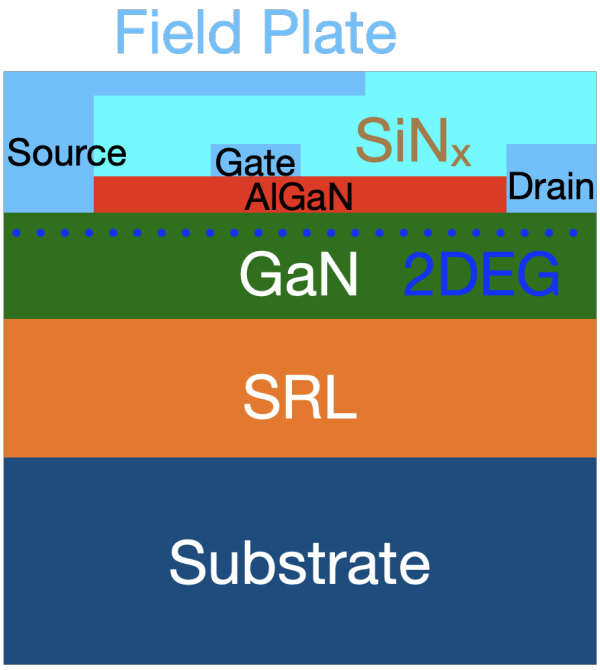

FIGURE 2.3. Schematic of a AlGaN/GaN HEMT structure.

amplifiers [42].

2.2 Structure of AlGaN/GaN HEMT

A typical AlGaN/GaN HEMT structure is shown in Figure 2.3. It consists of the substrate, the strain relief layer (SRL), the GaN epitaxy , the AlGaN/GaN heterojunction with 2DEG in between, the passivation layer (SiN_x), contacts and field plates. There is also a thin GaN cap layer (1 - 2 nm) between the AlGaN barrier and the passivation layer, and a nucleation layer between the substrate and SRL (not shown in Figure 2.3).

2.2.1 Substrate

There are multiple substrate choice for the GaN device epitaxy as shown in Table 2.2. The ideal substrate for GaN should have a high thermal conductivity, a small lattice mismatch with GaN, large wafer size availability and a low cost. Although the bulk GaN can be grown and fits with GaN epitaxy, it is hard to commercialize due to its high cost and small wafer size [44]. The Si wafer is a good substrate choice due to its mature fabrication process, the large wafer size and low cost. However, considering that GaN HEMTs are widely used for the power and RF applications and a high thermal conductivity of substrate is often required. Therefore, SiC becomes a better choice for GaN HEMTs not only due to its high thermal conductivity but also the small lattice mismatch with GaN. Meanwhile, the demand of a low substrate loss makes SiC better than Si

Table 2.2: Comparison of substrate material properties for the GaN device [43].

	GaN	Si	SiC	Sapphire	Diamond
Bandgap (eV)	3.4	1.1	3.3	9.9	5.5
Thermal conductivity (W/(m·K))	2	1.5	4.9	0.35	180
Lattice mismatch with GaN (%)	0	17	3.5	14	89
Size (mm)	30	300	150	150	10
Cost	Very high	Very low	High	Medium	Extremely high

for RF operation [9]. Diamond benefits from its extremely high thermal conductivity and is a potential option for the next generation of GaN HEMTs [30].

2.2.2 Nucleation and Strain Relief Layer

For GaN-on-Si devices, the lattice mismatch Si and GaN will results in a large dislocation density and even cracks on the wafer. AlN is a common choice for nucleation followed by the strain relief layer to mitigate the strain due to the lattice mismatch. The SRL can be either graded layer or superlattice. The Al concentration will be gradually decreased for the graded SRL during growth whereas in the superlattice structure, the AlGaN layers with high and low Al concentrations change periodically. A study showed that the superlattice SRL is capable of suppressing the dynamic R_{ON} increase compared to the step-graded SRL [45]. For GaN-on-SiC devices, AlGaN can be used as the nucleation layer with small lattice mismatch and then GaN can be grown on the AlGaN layer.

2.2.3 GaN Epitaxy

The GaN epitaxy comprises of the doped GaN layer and the unintentionally doped (UID) layer. For power devices, the doped GaN layer is usually doped with carbon to reduce the vertical leakage down to the substrate, preventing the drain-source leakage through the vertical paths with the substrate. However, the deep acceptors in the GaN buffer due to carbon doping result in the dynamic R_{ON} increase. Therefore, it is a trade-off to control the dynamic R_{ON} with the vertical leakage by carbon doping. Fe doping is more common for RF devices, as the RF amplifier usually requires the device to have good linearity, which means there should be small RF-DC dispersion. Fe pins the Fermi level on the upper half of the forbidden band of GaN and does not lead to severe current collapse. Molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD) are two common types of growth techniques for semiconductor devices. Epitaxial process may induce impurities such as carbon and oxygen into GaN expitaxy even with an ultra high vacuum environment, results in the UID GaN layer.

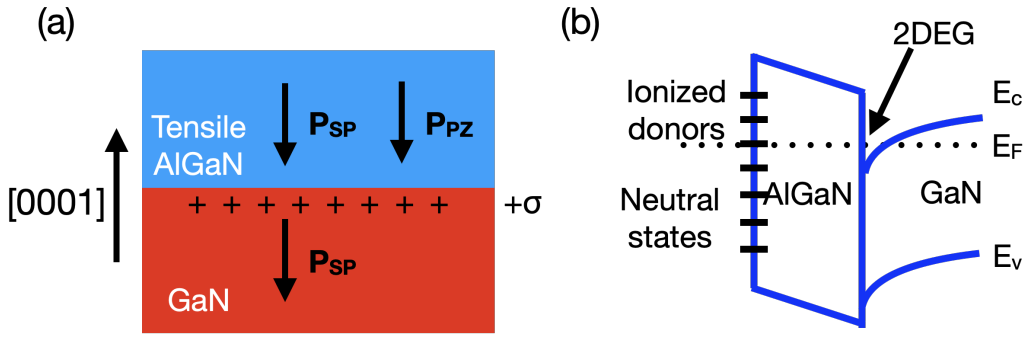

FIGURE 2.4. (a) AlGaN/GaN heterojunction with the spontaneous polarization ($\mathbf{P_{SP}}$) and the piezoelectric polarization ($\mathbf{P_{PZ}}$). The thin AlGaN layer is under the tensile stress and the bulk GaN is unstrained. (b) Band diagram of the AlGaN/GaN heterojunction with the formation of 2DEG. A part of donors on the AlGaN surface is ionized, proving the electron source for 2DEG.

2.2.4 AlGaN/GaN Heterojunction and 2DEG

The AlGaN barrier is deposited above the GaN channel to form the AlGaN/GaN heterojunction in order to generate the 2DEG. For wurtzite GaN and AlN, there is spontaneous polarization ($\mathbf{P_{SP}}$) along the [000$\bar{1}$] direction, which is due to the non-centrosymmetric structure. The spontaneous polarization is AlGaN is between that of AlN and GaN [46]. If the AlGaN layer is grown on a bulk GaN, the lattice discontinuity will induce a tensile stress within the AlGaN layer, which is perpendicular to [0001] direction. The tensile stress results in the piezoelectric polarization ($\mathbf{P_{PZ}}$) also along the [000$\bar{1}$] direction. The schematic of polarization in AlGaN/GaN heterojunction is shown in Figure 2.4 (a). The net polarization charges on the AlGaN/GaN interface is described as

$$\sigma = P_{SP,AlGaN} + P_{PZ,AlGaN} - P_{SP,GaN} \tag{2.4}$$

where $P_{SP,AlGaN}$ is the spontaneous polarization of AlGaN, $P_{PZ,AlGaN}$ is the piezoelectric polarization of AlGaN and $P_{SP,GaN}$ is the spontaneous polarization of GaN. Note that the spontaneous polarization of AlGaN is larger than that of GaN, so there will be net positive polarization charge on the AlGaN/GaN interface. The sign of the interface charge determines the band bending direction, as shown in Figure 2.4 (b). The conduction band of GaN near the interface is pushed down to the Fermi level due to the net positive polarization charge, which gives a rise to the 2DEG. However, due to the electron conservation, there should be an electron source providing the free electrons to 2DEG. According to [47], the surface donors of AlGaN take this role. The donors above the Fermi level become ionized and leave the positive charge on the AlGaN surface. It is the main reason for the formation of the 2DEG in the AlGaN/GaN heterojunction.

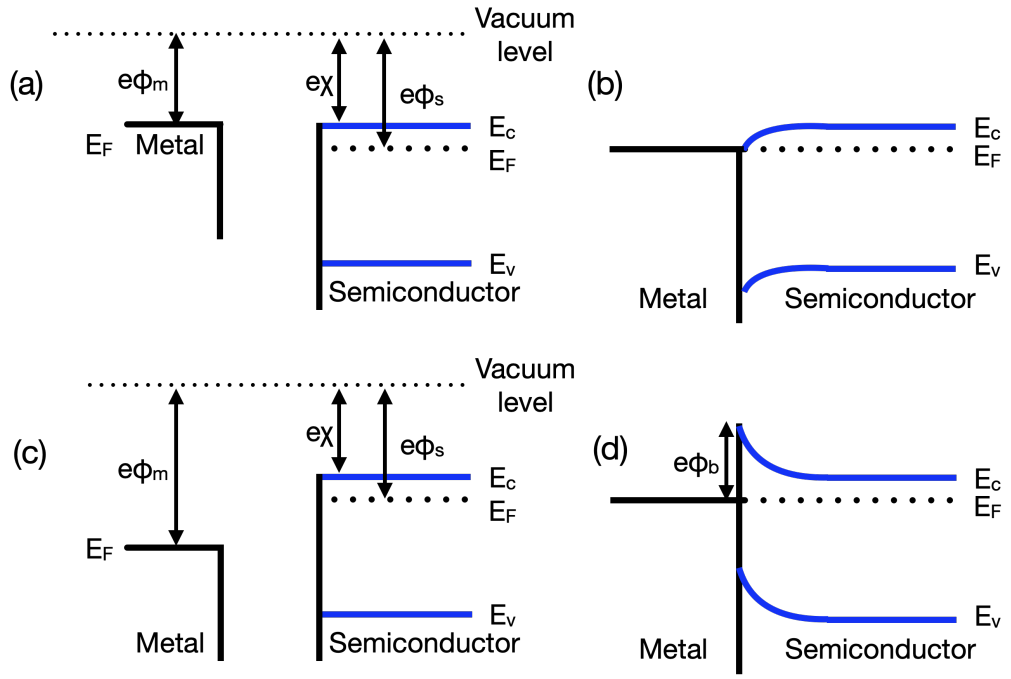

FIGURE 2.5. Ideal band diagrams of the Schottky contact and the Ohmic contact (n-type semiconductor). (a) Band diagram of a metal and semiconductor before contact ($\phi_m < \phi_s$). (b) Band diagram of the Ohmic contact. (c) Band diagram of a metal and semiconductor before contact ($\phi_m > \phi_s$). (d) Band diagram of the Schottky contact with a barrier (ϕ_b). These figures are adapted from [48].

2.2.5 GaN Cap

A GaN cap layer with a thickness in a range 1 - 2 nm is usually grown on the AlGaN barrier to suppress the leakage current. Sheu et al. [49] discovered that the leakage current would be reduced by a factor of 3 – 4 in GaN Schottky barrier diode. The thickness of the GaN cap layer should be controlled as a too thick GaN layer will induce addition polarization charge which reduces the 2DEG density [50].

2.2.6 Passivation

The passivation layer is deposited above the AlGaN barrier and the GaN cap to reduce the surface traps and the leakages. Without the passivation, charges will be stored on the AlGaN surface and act as a virtual gate to increase the channel resistance [51]. Arulkumaran et al. [52] compared different passivation options such as SiO_2, Si_3N_4 and SiON deposited by plasma enhanced chemical vapour deposition (PECVD) and it turned out that the Si_3N_4 would suppress the surface traps most but also lead to a low breakdown voltage. Wang et al. [53] showed a robust SiN_x/AlGaN interface by depositing SiN_x with low pressure chemical vapour deposition (LPCVD) technique.

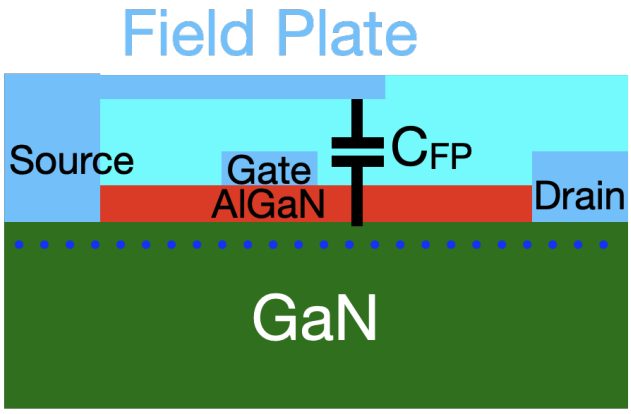

FIGURE 2.6. Schematic of the source field plate where the capacitance between the field plate and 2DEG is denoted as C_{FP}.

2.2.7 Contacts

The metal-semiconductor junctions have two basic types, the Schottky contact and the Ohmic contact. The band diagrams of the Ohmic contact with a n-type semiconductor are depicted in Figure 2.5 (a) and (b). ϕ_m is the metal work function, ϕ_s is the semiconductor work function and χ is the semiconductor electron affinity. After contact, the Ohmic contact will form if $\phi_m < \phi_s$, and it has a linear IV characteristics allowing the current flow in both direction. In GaN HEMTs, the source and drain are made with Ohmic contacts. The metal stack Ti/Al/Ni/Au is used for fabrication the Ohmic contact with GaN [54].

The band diagrams of the Schottky contact with a n-type semiconductor are depicted in Figure 2.5 (c) and (d). After contact, the Ohmic contact will form if $\phi_m > \phi_s$, it only allows single polar current direction from the metal to the semiconductor if the applied voltage is larger than ϕ_b. ϕ_b is calculated by

$$\phi_b = \phi_m - \chi \tag{2.5}$$

In GaN HEMTs, Ni/Au alloy is used to choose for the Schottky gate with a barrier height around 0.5 eV [55].

2.2.8 Field Plate

The field plate is incorporated in order to reduce the field peak near the gate edge [56]. The field plate, the passivation layer, the AlGaN barrier and 2DEG together act as a capacitor (C_{FP}). When a high drain bias (V_D) is applied and the source is grounded, the potential drop across C_{FP} equals to 2DEG potential below the field plate V_{2DEG}. The maximum 2DEG potential below the field plate ($V_{2DEG,max}$) is calculated by

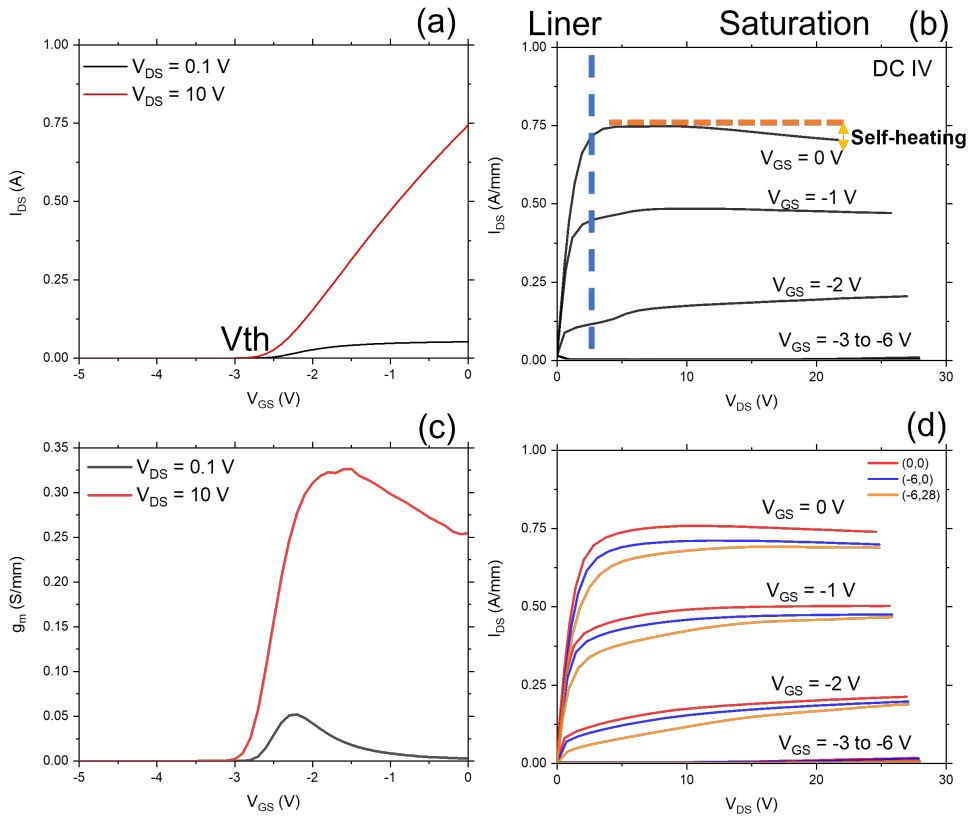

FIGURE 2.7. IV characteristics on a GaN-on-diamond HEMT. (a) Transfer characteristics. (b) DC IV output characteristics. (c) Transconductance characteristics. (d) Pulsed IV output characteristics (t_{ON}/t_{OFF} = 1 μs/1 ms).

$$V_{2DEG,max} = \frac{en_{2DEG}}{C_{FP}} \tag{2.6}$$

where n_{2DEG} is the initial 2DEG density. It considers that the 2DEG is fully depleted by the field plate. Therefore, if $V_D > V_{2DEG,max}$, the maximum potential under the field plate will be limited below $V_{2DEG,max}$.

2.3 Device Physics of AlGaN/GaN HEMT

Understanding device physics in AlGaN/GaN HEMTs behind the measurement data is crucial for device optimization. Some selected topics are discussed in this section.

2.3.1 DC and Pulsed IV performance

The direct current (DC) transfer characteristics and output characteristics measured in a GaN-on-diamond HEMT are shown in Figure 2.7 (a) and (b). The gate threshold voltage (V_{th}) is defined

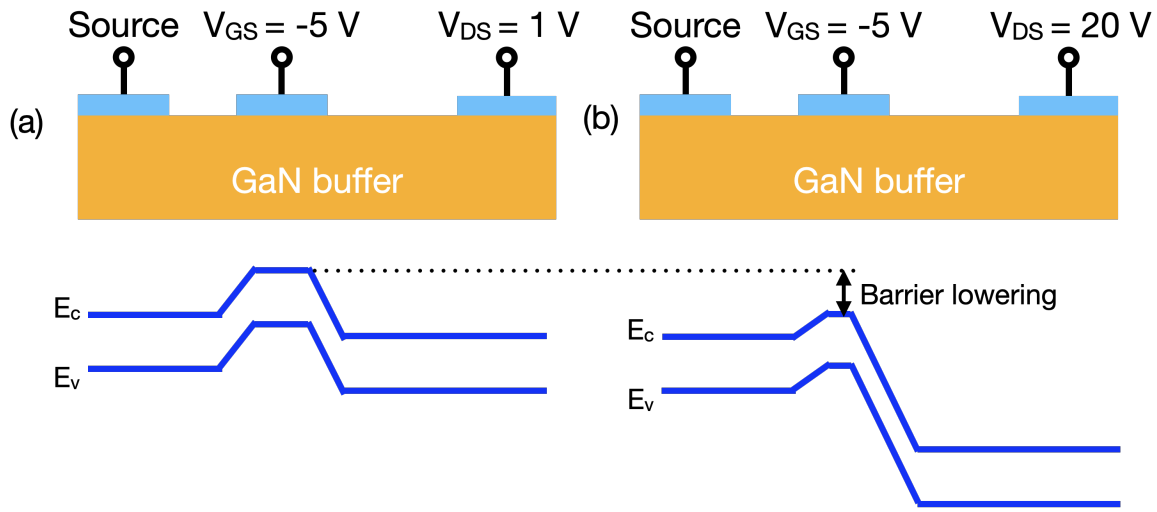

FIGURE 2.8. Schematic of drain-induced barrier lowering mechanism in a GaN device. (a) When V_{GS} = -5 V, V_{DS} = 1 V, there is a gate barrier preventing the lateral current flow. (b) When V_{GS} = -5 V, V_{DS} = 40 V, the gate barrier is lowered down due to the high drain bias.

as where the device is turned off and is around -2.5 V. For the output characteristics, in the linear region, the drain-source current (I_{DS}) increases with the drain-source voltage (V_{DS}) almost linearly. The ON-resistance (R_{ON}) is calculated by:

$$R_{ON} = \frac{dV_{DS}}{dI_{DS}} \tag{2.7}$$

In the saturation region, the velocity of electron in the 2DEG saturates and the self-heating effect leads to the current drop. The transconductance (g_m) is an important parameter for RF analysis and is defined as:

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{2.8}$$

The transconductance characteristics is shown in Figure 2.7 (c). The pulsed IV output characteristics is shown in Figure 2.7 (d) and (*,*) refers to (quiescent gate voltage,quiescent grain voltage). There is current collapse when comparing IV curves of (-6,0) and (-6,28) to (0,0). It can be due to the trap states near the gate and in the buffer.

2.3.2 Drain-Induced Barrier Lowering

The threshold voltage shift can happen due to drain-induced barrier lowering (DIBL). As depicted in Figure 2.8, the gate potential barrier will prevent the lateral current flow during OFF-state. However, when a high drain bias is applied, the gate potential barrier is lowered down and it

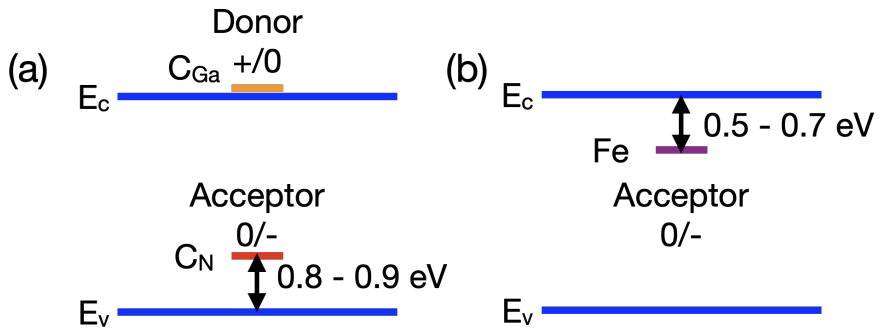

FIGURE 2.9. Trap energy levels in GaN HEMTs with (a) carbon and (b) iron.

increases the current flow. Therefore, V_{th} shifts to negative with a high drain bias. Park et al. found that Ga-polar HEMTs suffered more from DIBL than N-polar HEMTs. In Chapter 7, there is apparent DIBL in the MIS GaN HEMTs.

2.3.3 Trap

The GaN buffer layer is doped with carbon or iron to make it semi-insulating, which helps to reduce the vertical leakage and increase the breakdown voltage. Carbon, as shown in Figure 2.9 (a), can either act as an acceptor (0/-) if it occupies a nitrogen site (C_N) or as a donor (+/0) if it occupies a gallium site (C_{Ga}). C_N has an activation energy about 0.8-0.9 eV [57], while C_{Ga} is a shallow donor. Koller et al. [58] show that with a high carbon doping density in GaN (10^{19} cm^{-3}), carbon acceptor states will form a defect band as the charge can transport through it. It will lead to an underestimate of activation energy calculation at the high temperature. Rackauskas et al. determines the self-compensation ratio of carbon (donor density/acceptor density) in a range of 0.4 - 1 [59]. The Fe dopant will occupy the nitrogen site and behave as an acceptor (0/-) in GaN which is 0.5 - 0.7 eV below the valence band, as depicted in Figure 2.9 (b). Incorporation of Fe into GaN will pin the Fermi level in the upper band and make it n-type. GaN HEMTs have shown good RF performance with the Fe-doped GaN buffer layer [56].

2.3.4 Gate Leakage

The gate leakage is a major reliability issue for GaN HEMTs [60]. With a low gate leakage level, the device can improve the energy efficiency by reduce the power loss. There are two major transport mechanisms for an electron traveling through the AlGaN or the SiN_x barrier. Fowler-Nordheim tunnelling is a field-assisted tunneling mechanism, as depicted in Figure 2.10 (a). A high electric field can narrow down the barrier width which makes tunneling easier to occur. The tunneling current density J_{FN} of Fowler-Nordheim tunnelling is described by

$$J_{FN} = AE^2 exp[-\frac{B}{E}] \tag{2.9}$$

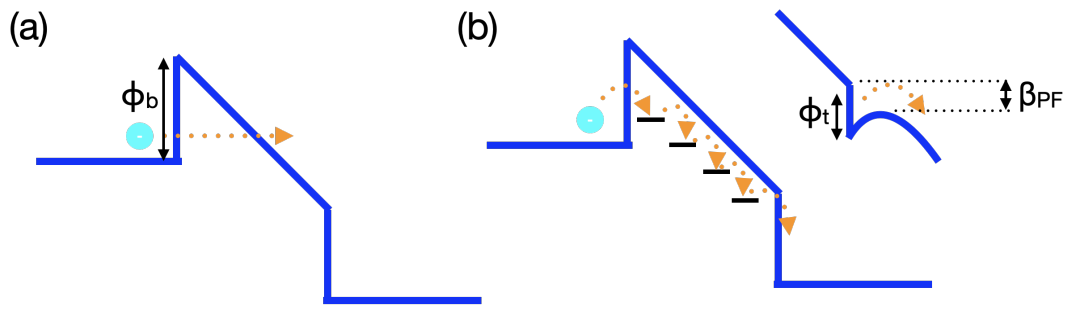

FIGURE 2.10. Schematic of Transport mechanisms. (a) Fowler-Nordheim tunnelling. ϕ_b is the barrier height. (b) Poole–Frenkel emission. ϕ_t is the trap energy and β_{PF} is the barrier lowering for trap emission.

where A and B are physical constants, E is the electric field across the barrier [61].

Poole–Frenkel transport is also a field-assisted transport mechanism. As depicted in Figure 2.10 (b), some trap states are present within the barrier. As the external electric field lowers down the energy for trap emission, electrons can get through the barrier with the aid of trap states. The transport current density J_{PF} of Poole–Frenkel emission is described by

$$J_{PF} = CEexp[-\frac{e(\phi_t - \beta_{PF})}{k_B T}] \tag{2.10}$$

where C is a physical constant, k_B is the Boltzmann constant, T is the temperature, ϕ_t is the trap energy and β_{PF} is the barrier lowering for trap emission [61], as indicated in Figure 2.10 (b). Poole–Frenkel emission process is temperature-dependent, and Turuvekere et al. [61] found that the transport mechanism can switch from Fowler-Nordheim to Poole-Frenkel as the temperature increases.

2.3.5 Hot Electron

Hot electrons are these free electron with a high kinetic energy, therefore become "hot" with a high electron temperature. The hot electrons in GaN HEMTs can lead to severe degradation issues, such as generating charge trappings or lattice defects [62]. The hot electrons in GaN HEMTs can be characterized by the electroluminescence by extracting the electron temperature [63] and also its temperature dependency [64]. The dominant scattering mechanism for hot electrons in GaN HEMTs is the longitudinal optical phonon scattering [65]. As the temperature increases, the scattering rate increases and it leads to a reduction of the mean free time and the average electron energy. Therefore, the charge trapping becomes less prominent with the increase of temperature.

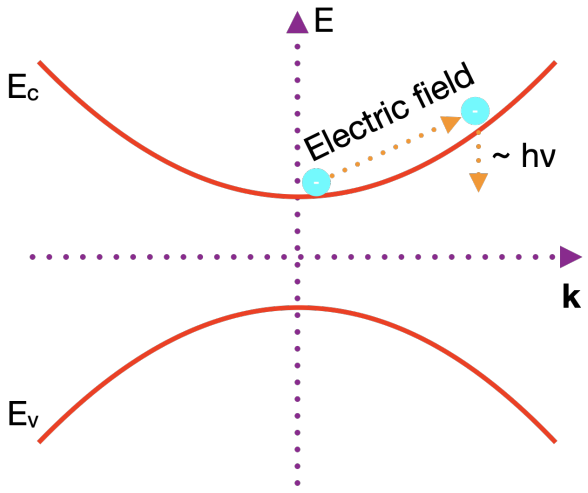

FIGURE 2.11. Schematic of electroluminescence generation within the band structure. The electron gains energy from the electric field and becomes "hot". It releases its energy by emitting a photon.

2.3.6 Electroluminescence

Electroluminescence is an electrical and optical phenomenon when the semiconductor device emits light applied with a high current and a high electric field. Brazzini et al. [32] showed that in AlGaN/GaN HEMTs, the EL emission has a continuing spectrum below GaN bandgap (3.4 eV), which suggesting that it is not due to the band-to-band recombination. On the contrary, it is considered a s result of the Bremsstrahlung effect as the hot electrons in the device decelerate and emits photons, as depicted in Figure 2.11. The hot electron temperature can be extracted by fitting with the form below,

$$I_{EL} \sim e^{-\frac{E_{photon}}{k_B T}} \tag{2.11}$$

where I_{EL} is the EL intensity, E_{photon} is the photon energy. The hot electron temperature increases with the drain voltage during ON-state in GaN HEMTs [63].

2.3.7 Impact Ionization

Impact ionization occurs when a high electric field is applied in a semiconductor. As shown in Figure 2.12, when a free electron travels along the electric field, it gains more kinetic energy and there is a possibility of the free electron collides with the electron in the valence band (bound state). The free electron loses energy which equals to the bandgap, and a new electron-hole pair generates. Through this process, new electron-hole pairs can be generated exponentially if the electric field is enough high. The dependence of the impact ionization rate α on the electric field is described by Chynoweth's equation [66]

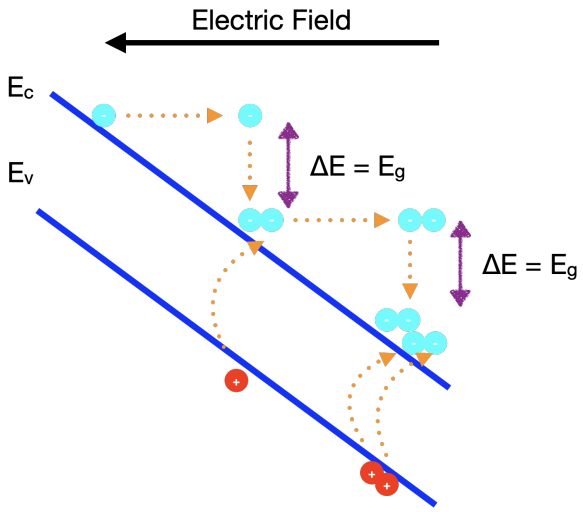

FIGURE 2.12. Schematic of impact ionization process. The electron-hole pairs can be generated if the impact electron gains enough energy.

$$\alpha = ae^{-\frac{b}{E}} \tag{2.12}$$

where E is the electric field, a and b are constant coefficients. In GaN, a is 1.5 × 10^5 cm^{-1} for electrons and 6.4 × 10^5 cm^{-1} for holes, and b is 1.41 × 10^7 Vcm^{-1} for electrons and 1.46 × 10^7 Vcm^{-1} for holes [67]. These values are used for the simulations in Chapter 6.

2.3.8 Breakdown

The OFF-state lateral breakdown in GaN HEMT can be due to impact ionization and punch-through [68]. With a high drain bias, impact ionization can occur in the vicinity of the gate edge where there is a high electric field. It leads the generation of a large amount of electron-hole pairs. Consequently, the drain current dramatically increases. The punch-through mechanism is depicted in Figure 2.13. Although the 2DEG has been fully depleted, the band structure in the GaN layer indicates that there are few free electron carriers present at a certain depth as the conduction band is not far from the Fermi level. It allows a current path through the GaN buffer under the gate.

2.4 Industrial Application of AlGaN/GaN HEMT

AlGaN/GaN HEMTs have shown multiple industrial applications in both power and RF fields as a results of the large breakdown field, the low ON-resistance and the fast switching capability.

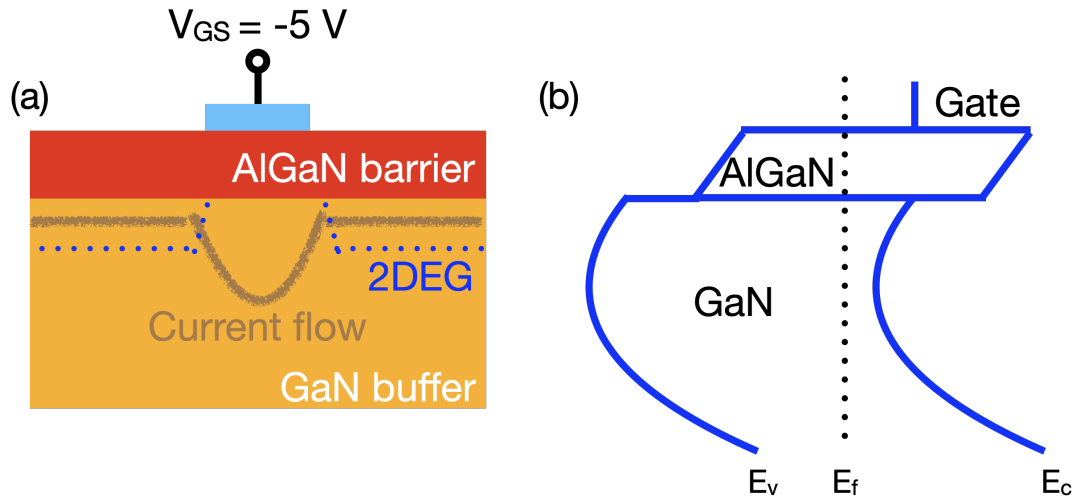

FIGURE 2.13. (a) Schematic of punch through current during OFF-state in a GaN HEMT. (b) Band diagram under the gate during OFF-state with punch-through current.

2.4.1 Power Application

The switching power supply, or the switch-mode power supply (SMPS) is a common type of circuit that is widely used for high power DC-DC, DC-AC or AC-AC conversion. For example, a boost power converter can step up DC voltage while a buck power converter can step down the DC voltage. For electrical vehicles, DC-AC conversion is very common as it is required to transfer the energy between the AC grid, the DC battery, and the AC electric motors. A DC-AC inverter is frequently used for this purpose. Thanks to the high breakdown voltage and the high frequency operation features, GaN HEMTs have found a significant place in the SMPS application.

Fig. 2.14 (a) shows a typical DC-DC boost power converter circuit. The control circuit generates a pulse wave with a duty circle (D = $t_{on}/(t_{on} + t_{off})$) to turn on and off the transistor. When the transistor is turned off, the inductor releases its energy and the diode is under the forward bias, given the total output voltage (V_{out}) as a sum of the input voltage (V_{in}) and the inductor voltage (V_l). The capacitor will be charged to the same output voltage during this period. When the transistor is turned on, the diode is under the reverse bias and serve to cut the output circuit with the input circuit. During this period, the capacitor releases its energy to the output voltage. This process finally lead to a boost in the DC voltage and the output voltage can be calculated by the following equation when it is operated in a continuous mode.

$$V_{out} = V_{in}(\frac{1}{1-D}) \tag{2.13}$$

The buck power converter, on the contrary, which steps down the DC voltage, follows the equation bellow when it is operated in a continuous mode.

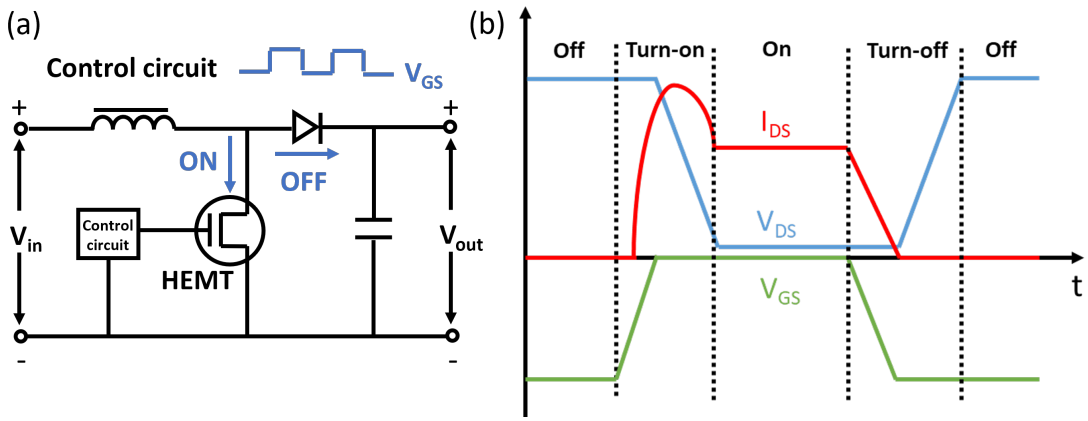

FIGURE 2.14. (a) Schematic of a DC-DC boost power converter circuit which is able to step up the voltage while reduce the current. The control circuit generates a square wave to turn on and off the HEMT periodically. (b) The IV waveform of the transistor inside the DC-DC boost power converter circuit under the hard-switching condition.

$$V_{out} = DV_{in} \tag{2.14}$$

Fig. 2.14 (b) shows the IV waveform of the transistor within the DC-DC boost converter. As the control circuit turn on and off the transistor periodically, the LC circuit responses with a short time delay, resulting in that the drain voltage always switches later than the gate voltage. During the turn-on transient, the gate voltage switches from off to on state first, then the drain voltage falls from a high voltage (equal to V_{in} + V_l) to a low voltage. This process will finally contribute to a high current spike during this period, and it usually refers as hard-switching. The strong self-heating effect and the hot electron effect may arise during the hard-switching. By contrast, if the gate is turned on before the drain voltage falls from high to low, it refers as soft-switching. For the soft-switching, the switching condition is moderate and usually will not show any side effect in the device.

2.4.2 RF Application

Monolithic microwave integrated circuits (MMICs) usually operate at microwave frequency ranges (300 Mhz to 300 GHz) and are widely used for radar, satellite and especially, the fast growing 5G technology. MMICs include amplifiers that amplify the input signal to the output signal with a certain gain, and filters that only allow the signal with certain frequency band to pass.

The amplifier has multiple Class types (i.e. A, B, AB, C...) which depend on the distortion of the output waveform, as shown in Figure 2.15. The Class A amplifier is the simplest one and it does not distort the waveform and keeps the linearity. The other Class types will distort the

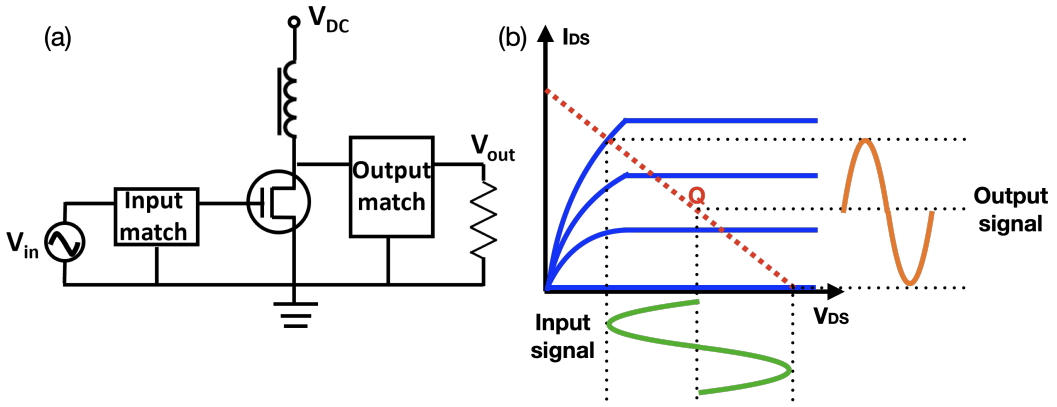

FIGURE 2.15. (a) Schematic of a RF power amplifier circuit, which can be Class A, B and AB by selecting different operating point [69]. (b) Schematic of the input and output signals from a Class A amplifier and follow the same waveform. Q is the operating point.

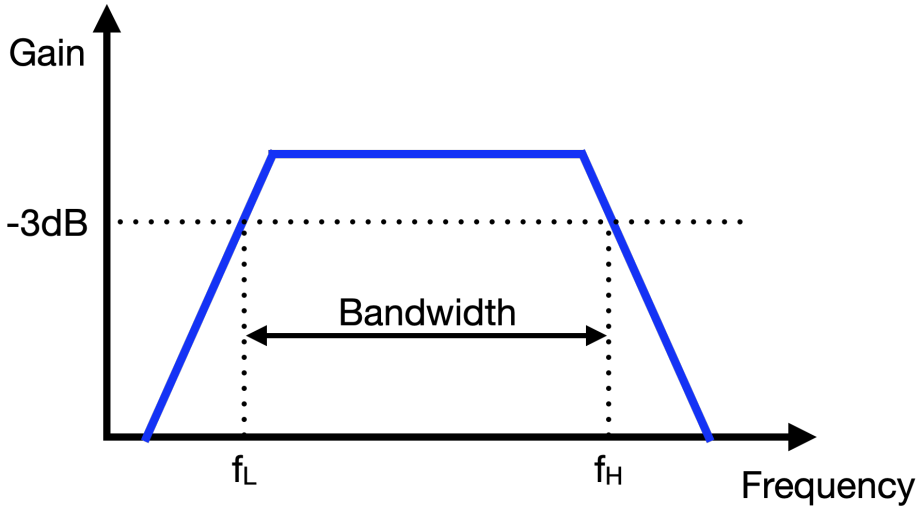

FIGURE 2.16. Schematic of the frequency response of a filter. The lower and upper cutoff frequencies denote as f_L and f_H respectively.

waveform but also increase the efficiency (reduce the power loss). The gain of an amplifier is defined as the ratio between output and input signals. The signal can be in current, voltage or power. The power added efficiency (PAE) is usually adopted to describe the efficiency of an amplifier, which is described as follows,

$$PAE(\%) = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.15}$$

where P_{in}, P_{out} and P_{DC} are the the input power, the output power and the applied DC power.

The gain of amplifiers is a function of the operating frequency with a lower and upper limit,

and therefore some of the operational amplifiers can be used as filters. The typical frequency response of a filter is shown in Figure 2.16. The allowed frequency range is between f_L and f_H (when Gain = -3 dB), and is also referred as bandwidth.

CHAPTER 3

CHARACTERIZATION TECHNIQUES

To get a deep understanding of the detailed electrical devices studied in this work, various new technologies are required for investigation. This chapter begins with the detailed experimental environments and then followed by the electrical characterization methods used in this thesis. The last section introduces the simulation techniques for the electrical and thermal purposes.

3.1 Experimental Environments

Throughout this work, all the measurements are performed on wafers instead of package devices. The on-wafer test avoids the need of packaging the devices and enables to straightforward control the device conditions such as light and temperature. However, a complex setup is required to use for the accurate on-wafer characterization. It includes a probe station, characterization equipment, coaxial/triaxial cables and the test structures.

3.1.1 Probe Station

A probe station, as shown in Figure 3.1, usually comprises a chuck, a microscope, a lighting system and an external black enclosure. The chuck is made by conductive metals like steel or aluminum and are usually grounded during the measurements. For some thermal measurements that require to heat up devices, a specific thermal chuck with a proportional-integral-derivative (PID) temperature controller system is used. The thermal chuck used in this thesis allows to heat devices up to 200 °C. The microscope with multiple objective lens and a lighting system is built together to provide light while observing and connecting the devices. The black enclosure builds

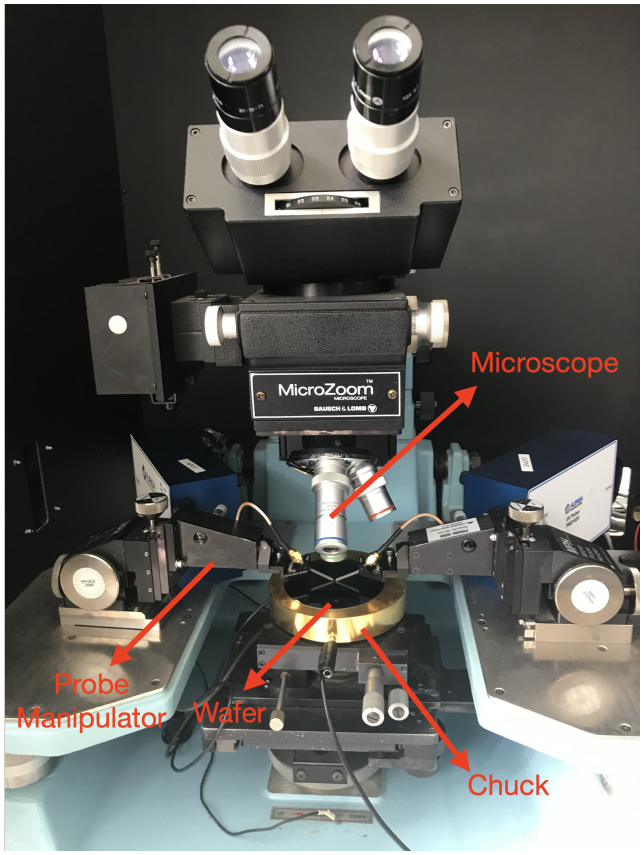

FIGURE 3.1. Probe station with a wafer laid on the chuck and connected to the external circuit through the probe manipulators.

up a dark environment to reduce the photon excitation and in addition it acts like a Faraday cage to screen the external electromagnetic noises.

Several probe manipulators (also known as micro-positioners), which are able to control the movement of probes precisely, are placed on the stage for device connection. During the measurements, these manipulators are attached to the metallic stage by the magnetic force, avoiding any unexpected vibrations. Metallic tips can be fixed with the manipulators to contact the device under test.

3.1.2 Characterization Equipment

A source measuring unit (SMU) has the capability to source and measure the voltage and the current simultaneously. The characterization equipment used in this thesis consists of Keithley 4200-SCS, Keithley 2636B, HP 4156A, HP 41501B, and Auriga 4850, as shown in Figure 3.2. Each characterization equipment has multiple SMUs which can be controlled by either built-in software or LabView/Test script builder (TSB) programs by general purpose interface bus (GPIB)/local area network (LAN) connections.

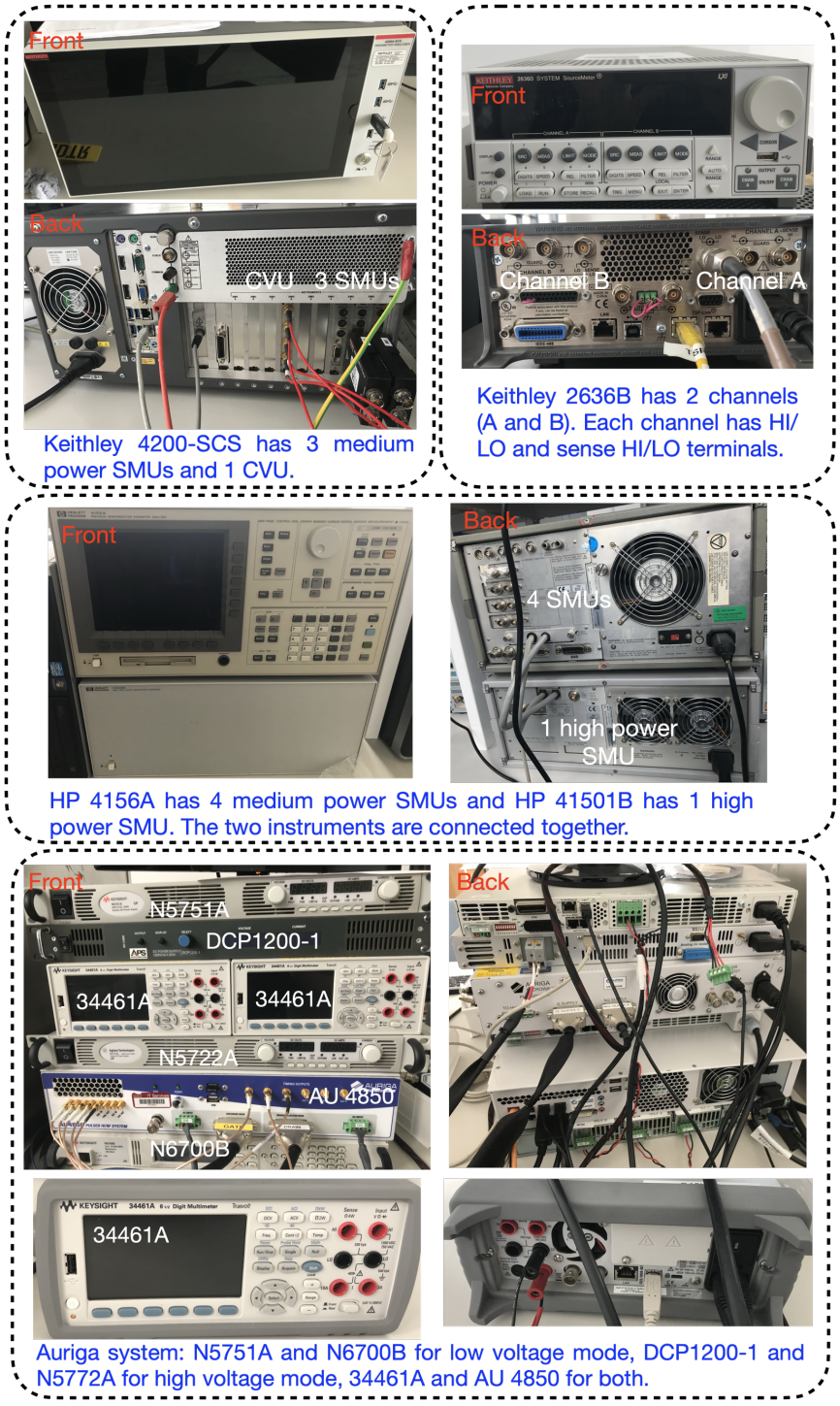

FIGURE 3.2. Characterization instruments in the laboratory used for the measurements in this thesis.

Keithley 4200-SCS has 3 medium power SMUs (maximum voltage 210 V, maximum current 100 mA, maximum power 2 W) with a current resolution down to 1 pA. It is capable for most

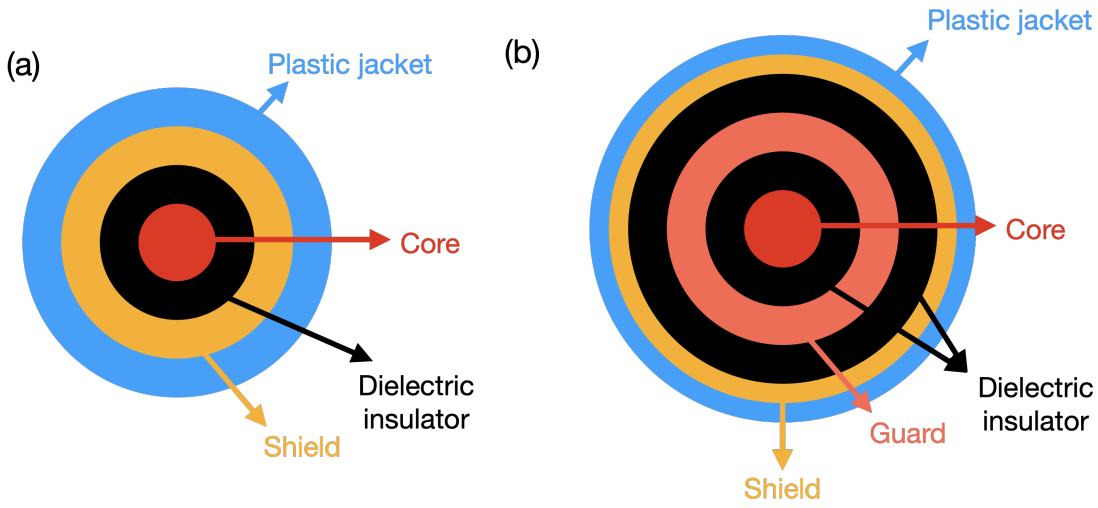

FIGURE 3.3. Cross-section of (a) a coaxial cable, (b) a triaxial cable.

of DC measurements in this thesis. Keithley 2636B has 2 SMUs labelled as channel A and B (maximum voltage 210 V, maximum current 1.5 A, maximum power 30 W) with a current resolution ranging from 20 fA to 50 μA. Keithley 2636B can be controlled by TSB program through the LAN connection and is suitable for applying voltage stress (i.e. for EL measurements). HP 4156A can source and measure voltage up to 100 V with a current resolution of 1 fA and HP 41501B is capable for voltage up to 200 V with a current resolution of 1 nA. These two instruments are connected together and are suitable for measurements with multiple terminals. Auriga 4850 system can be modified to low voltage mode (maximum voltage 220 V, maximum current 30 A) and high voltage mode (maximum voltage 1200 V, maximum current 100 A) with 0.01% current resolution and a time resolution down to 1 ns. The Auriga system is suitable for pulsed IV measurements when either high voltage or small time resolution is required.

3.1.3 Cabling

Both of coaxial and triaxial cables have been used for the measurements, of which the cross-section are shown in Figure 3.3. For both structures, the central core is conducting the signal, and the outside shield is grounded and protects the core from the external interference. However, for low current measurements (i.e. current resolution smaller than 1 nA), the leakage through the dielectric insulator between the core and the shield can be significant in the coaxial structure. Therefore, an additional conducting layer (guard) is included in the triaxial structure to suppress the leakage. The guard is connected with an unity amplifier to the signal within the SMU, so that it has the same potential with the core and screens the core from the shield.

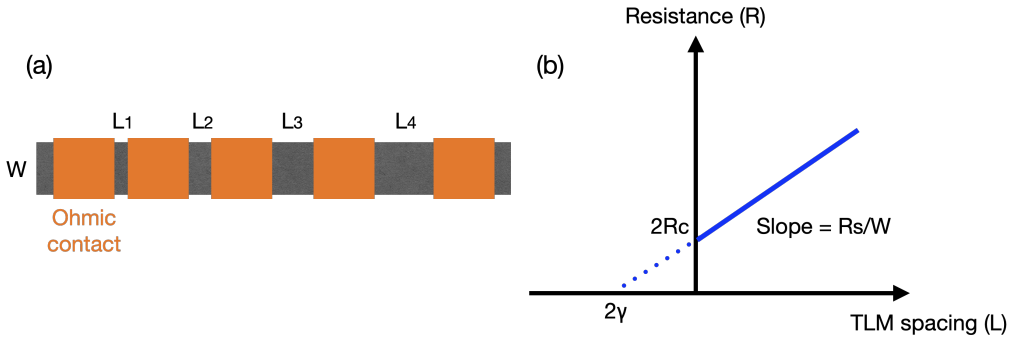

FIGURE 3.4. (a) Top view of the TLM structure. The Ohmic contacts are connected together by the 2DEG with different spacing. (b) By extrapolating the fitted line of the measured resistance between the Ohmic contacts against the contact spacing, the contact resistance (R_c) and the sheet resistance (R_s) can be calculated.

3.1.4 Test Structures

Different special test structures have been designed for certain purposes. The transfer length measurement (TLM) structure is designed for measuring the contact resistance (R_c) and the sheet resistance (R_s), as shown in Figure 3.4 (a). A series Ohmic contact are connected with 2DEG with different spacing. By measuring the resistance between each contact and plotting it against the contact spacing, as illustrated in Figure 3.4 (b), it is able to calculate R_c and R_s. The fitted line follows the equation below,

$$R = \frac{R_s}{W}L + 2\frac{\sqrt{\rho_C R_s}}{W} \tag{3.1}$$

where W is the width of Ohmic contact, ρ_c is the contact resistivity. To ensure the accuracy of resistance, the 4-wire method is used for the TLM measurement to determine the contact resistance and the sheet resistance. Both of force and sense of SMU are contacting to the one single contact with the aide of the Kelvin probe during this measurement, which helps to mitigate the effect of the resistance from the cable and the probe.

There are gate leakage structure and buffer leakage structure for leakage measurements, as shown in Figure 3.5 (a) and (b). The gate leakage structure separate the gate leakage into two parts, one is the surface leakage (surface hopping mechanism [70]) on the AlGaN surface and the other is the leakage through AlGaN barrier. In the buffer leakage structure, the guard contact is located at where the device has been mesa-etched, so that there is no 2DEG connecting the two Ohmic contacts. If the current flowing from Ohmic to guard (surface leakage) is small enough, then the buffer leakage current can be determined by measuring the current between two Ohmic contacts.

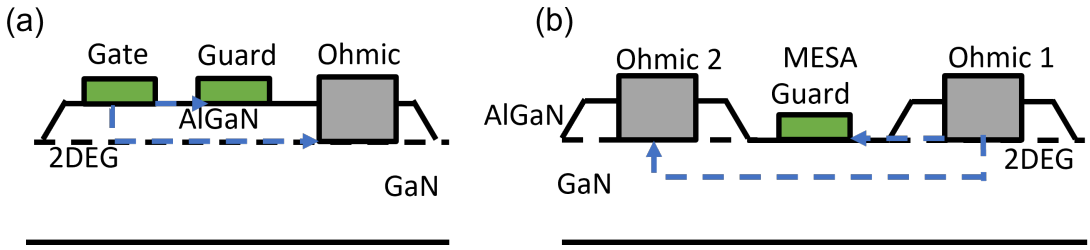

FIGURE 3.5. (a) Cross-section of the gate leakage structure. (b) Cross-section of the buffer leakage structure.

3.2 Electrical Characterization Techniques

3.2.1 DC IV Measurement

The DC IV measurement is the fundamental measurement to extract the basic information of a transistor. It usually uses three terminals, grounding the source, sourcing the gate and drain for measurements. Key parameters can be extracted from the $I_D V_D$ and $I_D V_G$ plots, such as V_{th}, R_{ON}, g_m, ON/OFF ratio. Plotting $I_D V_D$ curves is also a good way to analyse the self-heating effect and the trapping effect.

3.2.2 Transient Measurement

The transient measurement is useful to extract the charge trapping information. Each trap has its own finger print such as the activation energy and the capture/emission cross-section. These information can be gathered by analysing the transient current or resistance after a certain type of stress. The transient current I(t) at time t can be fitted with the equation below,

$$I(t) = I_{final} - \sum_{i}^{N} A_i e^{(-\frac{t}{\tau_i})^{\beta_i}} \tag{3.2}$$

where I_{final} is the final current, N is the number of traps, τ_i is the time constant for trap i, A_i and β_i are the fitting parameters for the trap i.

3.2.3 Back bias Measurement

The back bias measurement in GaN HEMTs is an useful method to determine the buffer charges, as 2DEG screens the surface charges and only buffer effect will dominate during the measurements [18]. It sometimes referred as the substrate bias measurement. For safety consideration, the chuck used for the back bias measurement should have a triaxial structure as shown in Figure 3.6 (a) with SiC insulating layers. The back bias measurement is usually carried out on the TLM structure which has an homogeneous 2DEG layer between the two Ohmic contacts, as shown in Figure 3.6 (b). One contact is grounded and the other is applied with a small bias

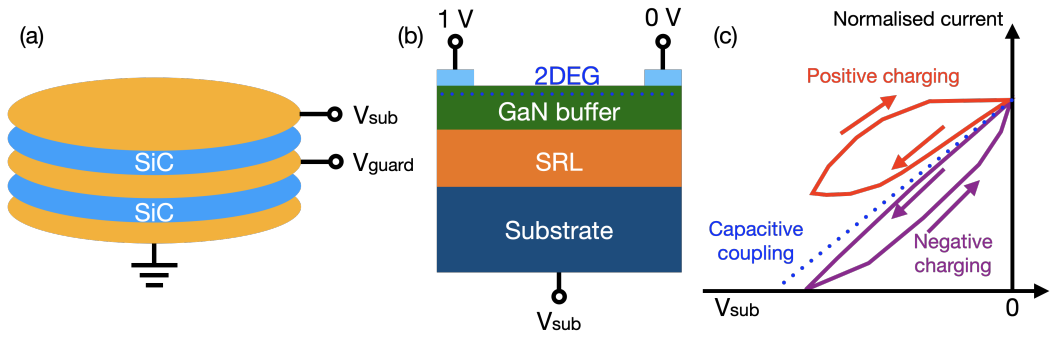

FIGURE 3.6. (a) Exploded view of the chuck used for the back bias measurement with a triaxial structure. The SiC inter-layer serves as an insulating layer. (b) Schematic of back bias measurement on a TLM structure. (c) An example of ideal back bias measurement results with positive or negative charging in the buffer.

(i.e. 1 V) for current measuring. If the measured current is plotted against the substrate voltage, it can be determined the charging type within the buffer. An example of ideal positive and negative charging behaviour is depicted in Figure 3.6 (c). The capacitive coupling line suggests the situation when the buffer stack is purely capacitive and no charges will be stored during the ramp. It is calculated by the 2DEG density as the following equation,

$$n_{2DEG} = n_0 + \frac{\varepsilon V_{sub}}{d} \tag{3.3}$$

where the n_0 is the initial 2DEG density, ε and d takes into account the permittivity and thickness of each layer. The normalized current that is higher than the capacitive coupling line suggests an increase of 2DEG density and therefore, there must be some positive charges under the 2DEG and vice versa.

3.2.4 Pulsed IV Measurement

The pulsed IV method characterization method has been developed for predicting the nonlinear RF operation on GaN HEMTs, especially when there is a strong trapping effect in the device [71]. Meanwhile, the self-heating effect can be precisely controlled with appropriate pulsing parameters, thus it becomes possible to extract the thermal resistance in GaN devices [72]. With the assistant of Auriga 4850, the pulsed measurements up to 600 V are able to implement on GaN HEMTs. In this thesis, the pulsed IV method is used in chapter 4 to investigate the GaN HEMT reliability during hard-switching.

A schematic of the square pulse waveform used in Auriga 4850 is shown in Figure 3.7. There are several key parameters to set the pulse waveform. Under the quiescent conditions, the voltages applied to each terminals are fixed and the devices usually undergo OFF-state. For the non-quiescent conditions, the voltages (V_{DSNQ} and V_{GSNQ}) are adjustable for each pulse and the

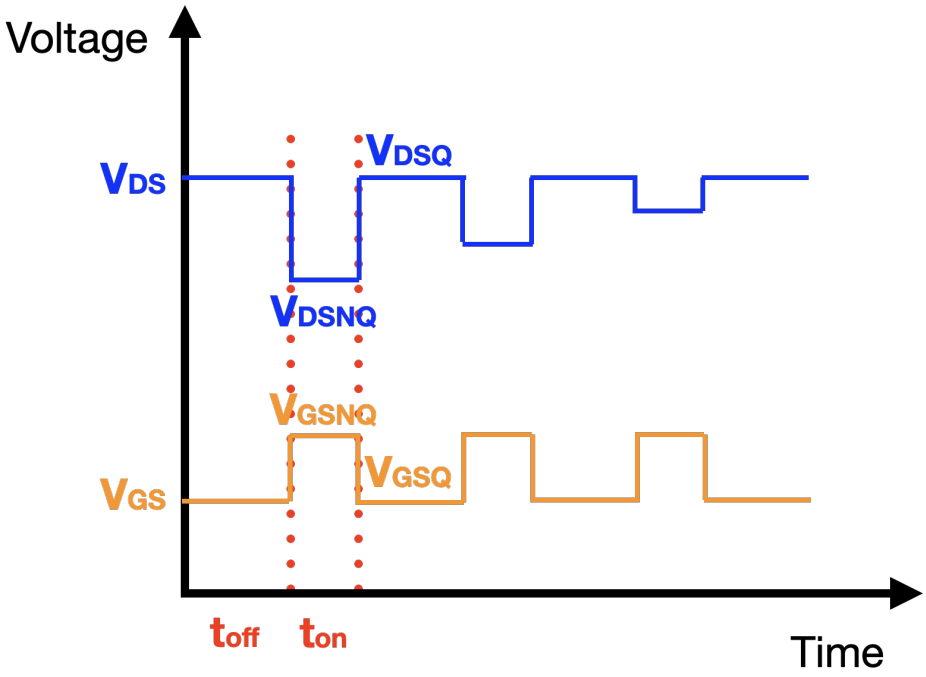

FIGURE 3.7. Schematic of a square pulse waveform generated by Auriga 4850. V_{DSQ} and V_{GSQ} represent the drain-source voltage and drain-gate voltage under the quiescent condition, while V_{DSNQ} and V_{GSNQ} represent the drain-source voltage and drain-gate voltage under the non-quiescent condition. t_{on} and t_{off} show the quiescent (usually when device is off) and non-quiescent (usually when device is on) time period.

devices can be either OFF-state or ON-state. The ON-state time (t_{on}) is referred as pulse width and the sum of ON-state and OFF-state time (t_{on} + t_{off}) is referred as pulse period. In Auriga 4850, t_{on} and t_{off} are independent parameters for drain and gate pulses, although in most cases they are aligned together. To avoid overheating during the switching time, the drain pulse is usually set ahead of the gate pulse in the beginning of a pulse, and behind the gate pulse in the end of a pulse to ensure a soft-switching condition. It finally results in that the drain pulse width is slightly larger than the gate pulse width.

The pulsed IV measurement requires to use ground-signal-ground (GSG) probes to contact the device, which has a coplanar waveguide structure. This configuration offers good isolation from the external interference and is suitable for high frequency operation.

3.3 Electroluminescence Measurement

Electroluminescence measurement is one of the vital characterization methods for GaN devices. It has been helps to to proven gathering the information of device degradation mechanism [73], and the hot electron temperature [74]. In this thesis, the EL measurements on GaN HEMTs has

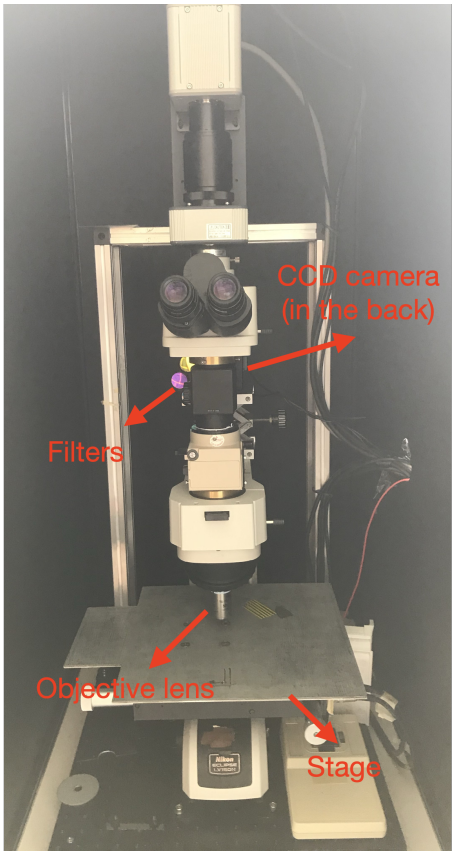

FIGURE 3.8. EL set up with a CCD camera in the back. Samples are placed on the stage with bias applied during the measurements. The 50 x objective lens are used for better resolution. Filters with different allowed wavelength are located in the light path ahead of the camera.

been carried out to determine the electrical fields and other analysis.

The EL images in this thesis were taken with the set up shown in Figure 3.8. The EL set up is equipped with a Hamamatsu digital charge-coupled device (CCD) camera to collect the light image. No optical filters are used throughout the measurements in this thesis. The EL measurements requires a dark environment to minimize the external light interference. Therefore, it is better to conduct the measurements during the night and to turn off any shining screens in the lab. To calculate the EL intensity accurately from the figures taken by the camera, a background noise figure without any bias applied on the device should be taken first. The EL intensity is then determined by counting the grayscale in each pixel of the EL figure and subtracting the background noise figure in the software ImageJ. For the spectrum measurement in chapter 6, the spectra is measured by the spectrometer (Maya 2000-Ocean optics QEPro, wavelength 200 - 1100 nm) from the backside of the device.

3.4 Simulation

3.4.1 Electrical Simulation - Silvaco Atlas

The 2D technology computer-aided design (2D-TCAD) simulator Atlas designed by Silvaco Atlas enables to simulate multiple unintuitive situations for semiconductor devices. It helps to visualize the devices properties in nano-scale which is usually hard to characterized by common experimental methods.

To implement simulation, the precise 2D device cross-section with the specification of the materials used in each part needs to be built firstly in the program named as DevEdit. Then, the mesh with triangle elements is required to constructed for the finite element analysis. The mesh should be well-defined for different regions to get a better solution. For example, near the 2DEG channel region of a GaN HEMT structure, the maximum height of the elements needs to be limited around 1 nm as the electron concentration varies dramatically within this region. However, for the substrate region, the mesh can be very sparse to avoid a reduction in the simulation speed. Figure 3.9 shows a general GaN HEMT structure with mesh built in DevEdit. The circular boundary conditions will be applied to solve the physical models for both in and out of the plane.

The device structure is then loaded in the program DeckBuild to specify the physical models and to run the simulator. The fundamental physics models used in Atlas include the Poisson's equation, the carrier continuity equations and the drift-diffusion equations. In the Poisson's equation, which describes the relationship between the electrostatic potential distribution and the local space charge density,

$$\nabla^2 \varphi = -\frac{\rho}{\varepsilon} \tag{3.4}$$

where φ is the electrostatic potential, ρ is the space charge density and ε is the permittivity. In the carrier continuity equations,

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \mathbf{J_n} + G_n - R_n \tag{3.5}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \mathbf{J_p} + G_p - R_p \tag{3.6}$$

where n(p) is the local electron (hole) concentration, $\mathbf{J_n}$ ($\mathbf{J_p}$) is the electron (hole) current density, G_n/R_n (G_p/R_p) is the generation/recombination rates for electrons (holes), q is the elementary charge and t is the time. In the drift-diffusion equations,

$$\mathbf{J_n} = qn\mu_n \mathbf{E_n} + qD_n \nabla n \tag{3.7}$$

$$\mathbf{J_p} = qn\mu_p \mathbf{E_p} - qD_p \nabla p \tag{3.8}$$

where $\mathbf{E_n}$ ($\mathbf{E_p}$) is the effective electric fields for electrons (holes), μ_n (μ_p) is the electron (hole) mobility and D_n (D_p) is the electron (hole) diffusion coefficient. Other general physical models (i.e. Fermi-Dirac distribution, field-dependent mobility) will also be specified and all the parameters

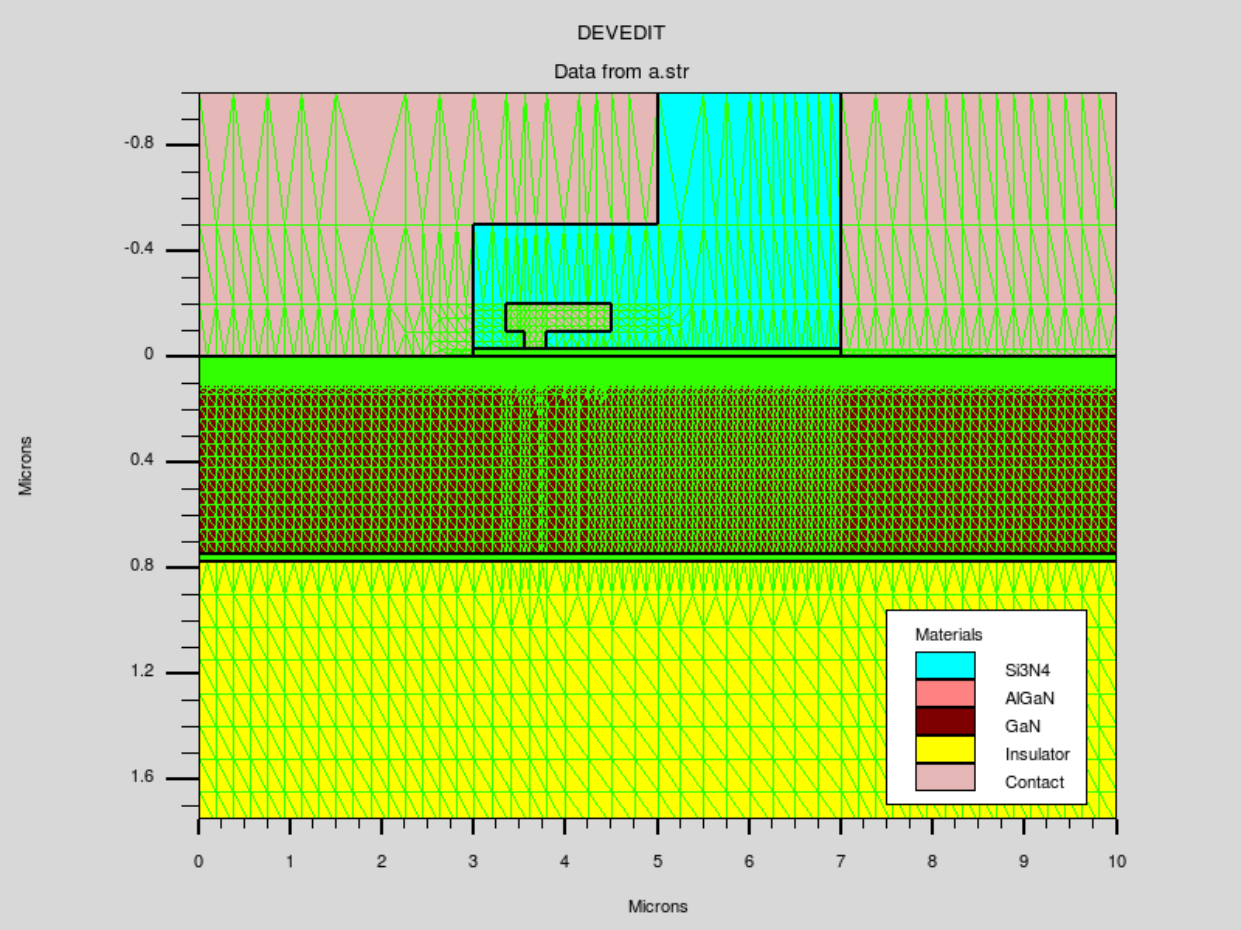

FIGURE 3.9. A gerneral GaN HEMT cross-section built in DevEdit showing the materials of each layers and the mesh. Note that the mesh density near the 2DEG region has been refined for a better simulation solution.

(i.e. doping, mobility, interface charges) for models and material properties need to be input in DeckBuild. Some specific models (i.e. Joule heating model, impact ionization model) can be also be enabled if the situation required. To solve the results, the voltages applied on the electrodes with fine voltage steps are to be specified. The Atlas simulator will solve the physical models at the nodes from the constructed structure with the finite element mesh and follow the commands step up/down the voltages gradually.

This simulation method has been implemented in Chapter 4 and Chapter 6 with the purpose of simulating self-heating and hot electron effects, and the punch-through effect. The simulation is only used as a qualitative tool to discuss and investigate the physical mechanisms in AlGaN/GaN HEMTs throughout this thesis.

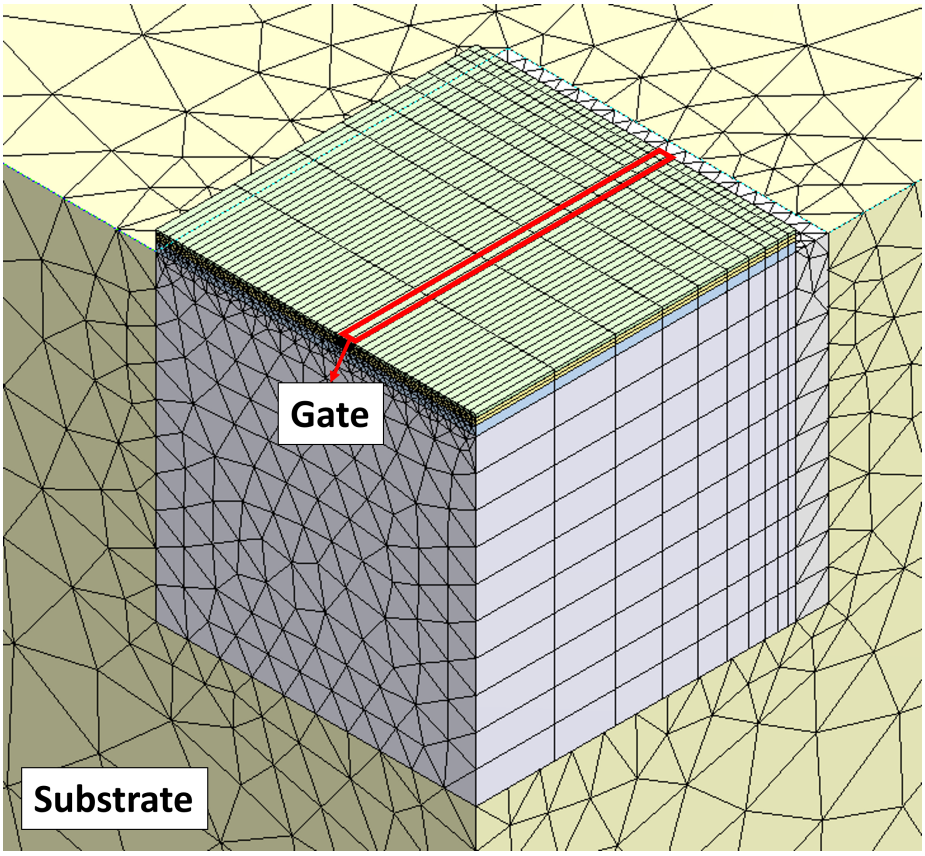

FIGURE 3.10. A general 3D GaN HEMT structure built in DesignModeler showing the mesh in each layer. The gate finger is built along the top side. Note that the mesh is more dense within the top GaN layer where the joule heat generates.

3.4.2 Thermal Simulation - Ansys

Apart from the electrical simulation, the thermal simulation is also crucial to characterize the reliability of GaN HEMTs, especially for the RF applications. However, the 2D models used in Silvaco Atlas do not take into account the heat dispersion in the third dimension, leading to inaccuracy of thermal simulations. Meanwhile, the 3D thermal simulation of the GaN HEMTs in the program Ansys has been reported to be aligned well with the Raman measurement results. The advantage of Ansys is that it allows for both steady-state and transient thermal simulations, while the drawback for this program is that it can not directly simulate the joule heating distribution from the electrical input of the device. Therefore, it is necessary to incorporate a cuboid heat source under the gate edge to simulate the temperature.

The 3D structure is initially constructed in DesignModeler, a built-in Ansys program allowing to generate different geometries. For GaN HEMT simulation, the structure usually consists of the top Si_3N_4 layer, the AlGaN barrier, the GaN buffer, the AlGaN SRL and the substrate. As shown in Fig. 3.10, the dimension of the epitaxy layer is usually made as same as the device size

as the high temperature region has little impact on the neighbor device, while the substrate size is much larger where the heat is easily to spread far away. The periodic boundary condition will be automatically applied except the bottom face of substrate where a fixed ambient temperature is used. The mesh construction is a vital step for Ansys simulation. The 3D mesh elements can be tetrahedron, cuboid or triangular prism which rely on the direction of the heat dispersion. For example, in Fig. 3.10, the substrate is meshed with tetrahedron elements as the heat diffuses in all 3 dimensions, while the region surrounding the gate finger is filled with triangular prisms as the heat generates homogeneously along the finger. The closer to the heat source, the denser the elements should be.

For the transient thermal simulation, the heat flow equation gives

$$\rho c(\frac{\partial T}{\partial t}) = \nabla \cdot (\kappa \nabla T) + Q \tag{3.9}$$

where ρ is the density of material, c is the specific heat capacity, T is the temperature, κ is the thermal conductivity and Q is the rate of heat generation per unit volume. Therefore, it is required to assign the key parameters (i.e. density, specific heat capacity and thermal conductivity) for different materials. For the steady-state thermal simulation, only the thermal conductivities of materials need to be specified.

The last step for the thermal simulation is to add the heat source into the device structure. According to the previous study, GaN HEMTs usually show a strong hot spot beneath the gate edge (on drain side). The most convenient way is to add a cuboid heat source in that region with the calculated heat input. A more accurate way is to transfer the joule heating map from the Silvaco Atlas model to the Ansys model. It requires a good alignment of the models in both programs. The Ansys simulation for the device temperature prediction has been implemented in Chapter 4.

CHAPTER 4

HARD- AND SOFT-SWITCHING IN POWER ALGAN/GAN-ON-SI HEMTS

AlGaN/GaN HEMTs exhibit excellent performance due to their high breakdown field, high electron density and high mobility [75]. These outstanding characteristics make it possible to have low on-resistance as well as sustain a high OFF-state drain voltage (600 V), thus being a prime choice for high-power switching applications. However, when operating at high voltages, it was found that charge trapping phenomena could cause dynamic R_{ON} [18, 76], a transient charge storage during OFF-state which impacts R_{ON} during on-state, limiting the performance and leading to reliability problems [77].

This chapter focuses on the reliability issues of GaN HEMTs under the hard- and soft-switching conditions, which occur in the power switching circuit. A set of samples with different SiN_x passivation stoichiometries is provided by Nexperia and is used here to investigate this topic. Section 4.1 introduces the research background of hard- and soft-switching and the Section 4.2 illustrates the devices under test. In Section 4.3, the experimental results are presented, showing how hard-switching affects the dynamic R_{ON}. In Section 4.4, the simulation methodology is introduced, and in Section 4.5, the results are analyzed and demonstrate that the measured degradation is consistent with hot-electron-induced surface trapping. Finally, Section 4.6 concludes this work.

4.1 Introduction

The operation regime in power converters can impact on the dynamic R_{ON}. For instance, in a DC-DC boost power converter which steps up the input voltage, a pulsed gate signal is applied to switch the transistor ON and OFF continuously. However, a short time delay is present between drain and gate pulses. During the turn-on transient, V_{GS} is stepped up first before V_{DS} drops, resulting in a high transient drain current flow, referred as hard-switching. If the circuit topology pulses V_{DS} down first during the gate turn-on transient, it refers to soft-switching and there is no drain current transient [79].

The presence of simultaneous high channel current and high electrical field is the major concern in hard-switching, since it can lead to significant self-heating and generation of hot electrons. Lu et al. [80] found an increase of R_{ON} after hard-switching compared to soft-switching in AlGaN/GaN HEMTs. They suggested that it was possibly due to the charge trapping induced by hot electrons during hard-switching. Joh et al. [81], on the contrary, found that the current collapse after soft-switching is larger than that after hard-switching in GaN HEMTs with gate dielectric. The authors suggested that the holes generated from impact ionization would compensate the surface electron trapping during hard-switching, and thus it leads to a reduction in current collapse. Bahl et al. [82] reported that both self-heating and hot electrons generated during hard-switching might be the cause of R_{ON} increase after hard-switching. They employed 2D-TCAD simulations to demonstrate that hot electrons would be generated under the hard-switching condition, and they could be either injected to the buffer or dielectric layers causing charge trapping. Rossetto et al. [64] demonstrated that the device degradation after hard-switching was recoverable, and electroluminescence and high temperature measurements were taken to show the existence of hot electrons during hard-switching.

Here a set of wafers consisting of different stoichiometries of LPCVD SiN_x passivation was used in this work. Waller et al. [83–85] have discussed the dynamic performance of the same set of wafers. They found that the stoichiometry of the LPCVD SiN_x layer had a significant impact not only on the effectiveness of the passivation, but also on the GaN buffer leakage and the bulk related dynamic R_{ON}. In particular, the wafer with Si-rich LPCVD passivation displays an optimum combination of low dynamic R_{ON}, together with acceptable leakage.

In this chapter, a pulsing setup is used to control the time delay between the drain and gate pulses precisely and measure the dynamic R_{ON} after hard- and soft-switching on AlGaN/GaN HEMTs. It is able to adjust the time delay with a resolution of ten nanoseconds, which is comparable to real circumstance, while in the previous study [64], the minimum time delay is 0.4 µs. More importantly, by analyzing the experimental data with supporting simulation data, it is suggested that instead of self-heating and buffer trapping, it is surface trapping that mainly affects the device performance after hard-switching.

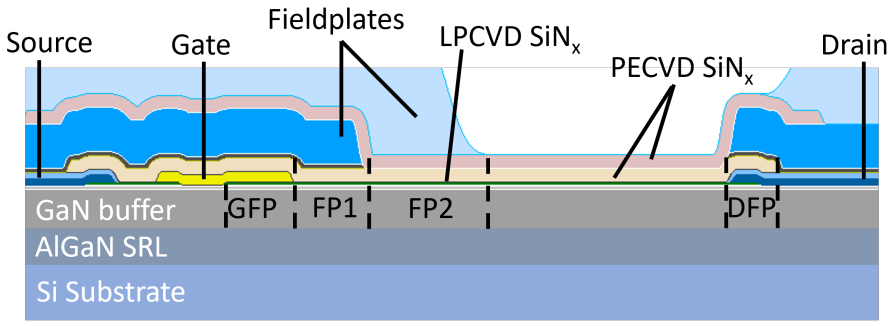

FIGURE 4.1. Schematic of GaN HEMTs used in Chapter 4 and 5 (not to scale). GFP is the gate connected field plate, and FP1 and FP2 are two source field plates.

4.2 Device under Test

Table 4.1: LPCVD SiN_x properties by wafer.

Wafer	DCS/NH_3	Refractive Index
A	0.33	2.01
B	2.49	2.10
C	3.30	2.14
D	4.38	2.21

Measurements have been carried out on 600 V AlGaN/GaN HEMTs fabricated on a 150-mm diameter GaN-on-Si process. As shown in Figure 4.1, the devices employ two source connected field plates separated by PECVD Si_3N_4 layers, with a 70-nm LPCVD SiN_x passivation layer covering a 3-nm GaN cap and a 20-nm AlGaN barrier above the GaN buffer. The buffer uses an UID GaN channel layer, a carbon-doped GaN layer as well as an AlGaN strain relief layer. The set of wafers used in this chapter have previously been described in [83–85], so for consistency the same labelling nomenclature is employed with wafers A, B and D studied here. The different dichlorosilane (DCS)/NH_3 precursor ratios and refractive indexes of the LPCVD SiN_x layer are listed in Table 4.1. Wafer A has a stoichiometric LPCVD Si_3N_4 layer and the Si/N ratio increases from wafer A to D.

The LPCVD SiN_x contains less hydrogen impurities than the PECVD SiN_x and thus works better to suppress any diffusion or trapping. In addition, the PECVD technique needs a lower temperature (200 ~ 400 °C) to deposit SiN_x than the LPCVD (700 ~ 800 °C), so it is suitable for deposition after the gate metal [86].

The devices under test are field-plated HEMTs with two Schottky gate fingers (L_{SG} = 3.5 μm, L_G = 1 μm, L_{GD} = 13.4 μm, W_G = 2 × 0.1 mm). The 2DEG carrier density is 5.87 × 10^{12} cm^{-2} and the sheet resistance was about 600 Ω/square. The measured threshold voltage for the devices is ~ -2 V.

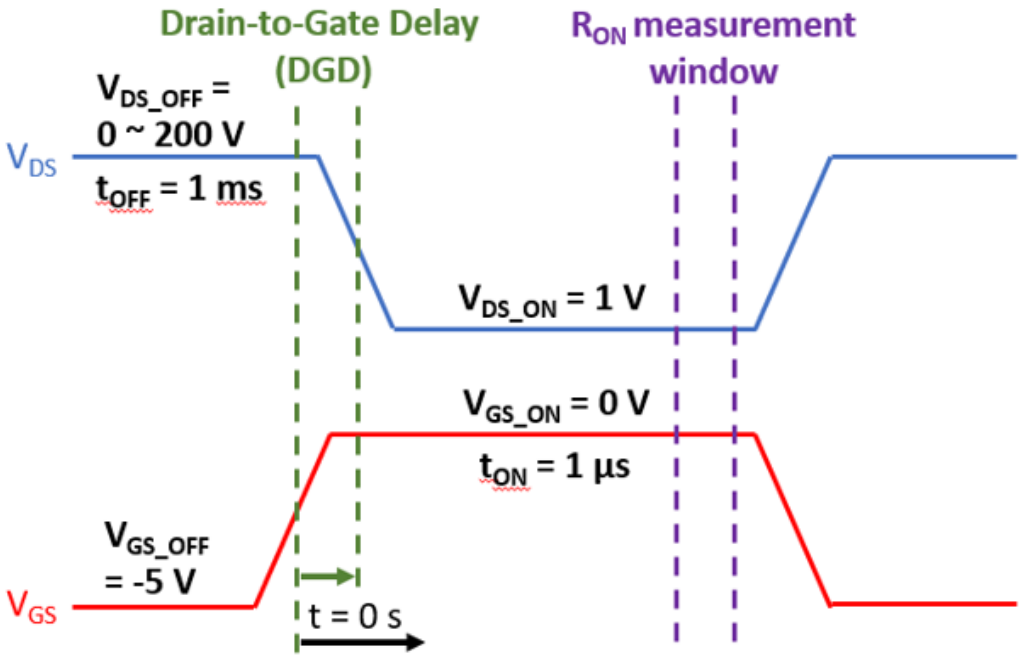

FIGURE 4.2. Drain and Gate voltages waveforms with hard-switching. The drain-to-gate delay (DGD) is defined as the time range between V_{DS} = (V_{DSON} + V_{DSOFF})/2 and V_{GS} = (V_{GSON} + V_{GSOFF})/2. Positive and negative DGD values correspond to the hard-switching and soft-switching respectively. The time t starts from the mid of gate switching and this definition is used throughout this work (in both experimental and simulation results). ©2020 IEEE.

4.3 Experimental Results

Figure 4.2 sketches the waveforms used to investigate the dynamic R_{ON} during hard-switching in an Auriga 4850 pulse system capable of V_{DS} up to 200V. The drain-to-gate delay (DGD) is defined as the time difference between V_{DS} = (V_{DSON} + V_{DSOFF})/2 and V_{GS} = (V_{GSON} + V_{GSOFF})/2. The DGD is positive if a hard-switching condition is applied while it is negative with a soft-switching condition. During the OFF-state, V_{DS} varies from 0 V to 200 V when V_{GS} = -5 V where the device is fully pinched-off. When the device is switched to the ON-state, the dynamic R_{ON} is measured in the linear region (V_{GS} = 0 V, V_{DS} = 1 V). The ON-state and OFF-state times are 1 µs and 1 ms respectively (duty cycle = 0.1 %). The fall time of the drain pulse is about 70 ns and the rise time of the gate pulse is about 100 ns. This is comparable to real usage since in power switching applications the slew rate is in the range of 10-100 V/ns, and thus the rise time and fall time can be tens of nanoseconds [64].

Figure 4.3 shows the measured current and voltage waveforms of soft- and hard-switching in wafer D when V_{DSOFF} = 150 V. During soft-switching (Figure 4.3 (a)) where DGD = 0 ns, the drain voltage has already dropped to a sufficiently low voltage when the gate voltage rises above

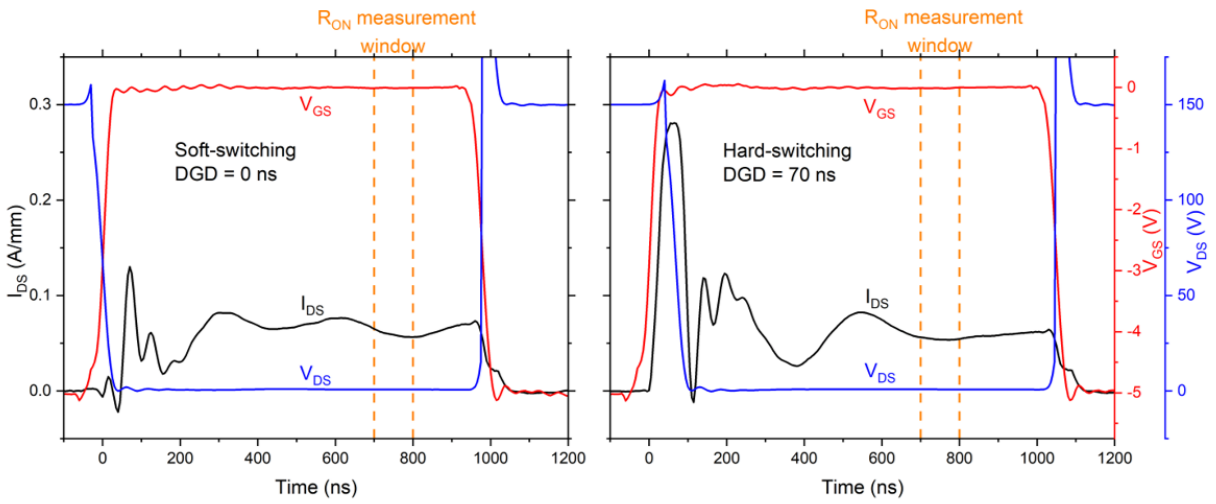

FIGURE 4.3. (a) Measured current and voltage waveforms with soft-switching (DGD = 0 ns, V_{DSOFF} = 150 V). (b) Measured current and voltage waveforms with hard-switching (DGD = 70 ns, V_{DSOFF} = 150 V). Measurements are performed on wafer D. ©2020 IEEE.

the threshold voltage, resulting in a low channel current. On the contrary, during hard-switching (Figure 4.3 (b)) where DGD = 70 ns, the drain voltage is still 150 V when the gate voltage reaches 0 V, leading to a high drain current spike. The R_{ON} measurement window is put at 700 – 800 ns after switching when the ringing associated with the on-wafer measurement is damped.

Figure 4.4 (a) displays the static I-V curves measured in wafer D. Wafer A and B have broadly same I-V curves. Figure 4.4 (b) shows the I-V curves (loadlines) during switching with varying DGDs (-70 – 130 ns) in the pulsed measurements. During the turn-on transient, the V_{DS} is swept from 150 V to 1 V while the measured IDS follows different paths from 0 A/mm to around 0.05 A/mm at the end of switching. Hard-switching curves (DGD > 0 ns) appear in the upper part of the I-V plane, showing a high current and a high voltage stress; in this region the maximum current increases monotonically until DGD > 50 ns, when the maximum current saturated at 0.28 A/mm. Conversely, soft-switching curves (DGD $\leqslant$ 0 ns) show negligible current.

Figure 4.5 (a) depicts the dependence of normalized dynamic R_{ON} on DGD measured in wafers A, B and D for V_{DSOFF} = 150 V. Figure 4.5 (b) depicts the measured normalized R_{ON} versus DGD for V_{DSOFF} ranging from 50 – 200 V in wafer D. The dynamic R_{ON} is measured in the measurement window shown in Figure 4.3 and normalized to the R_{ON} with no OFF-state stress (V_{DSOFF} = 0 V, V_{GSOFF} = 0 V), which is around 11.7 ± 1.0 Ω·mm in the 3 wafers. After soft switching (DGD $\leqslant$ 0 ns), the normalized dynamic R_{ON} was dramatically suppressed from wafer A to D and there is almost no variation of R_{ON} in wafer D with varying V_{DSOFF}. However, under the hard-switching condition (DGD > 0 ns), the normalized R_{ON} increases with DGD

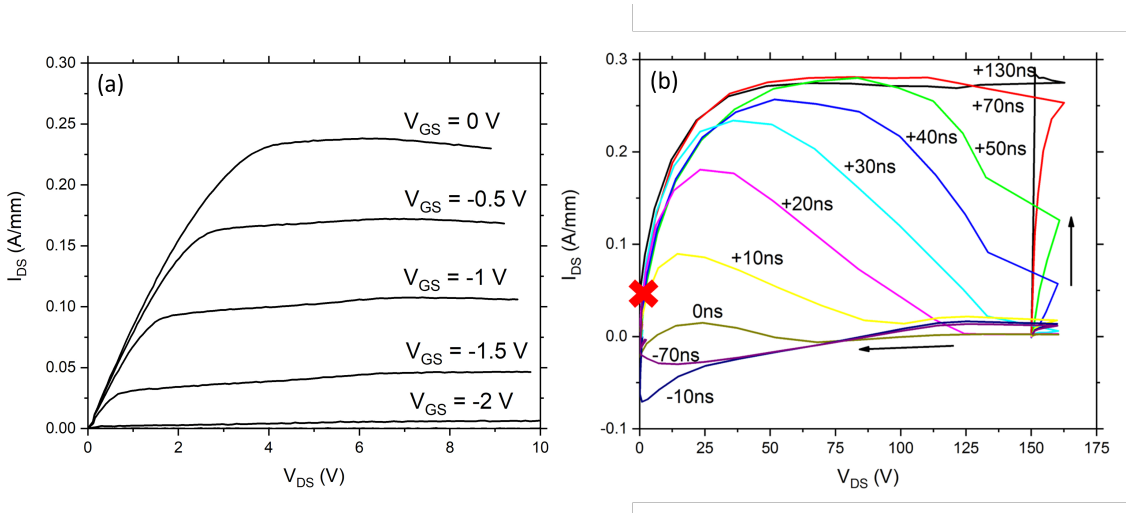

FIGURE 4.4. (a) Static I-V curves for V_{GS} ranging from -2 to 0 V in the DC measurements. (b) I-V curves (loadlines) during switching while the DGD falls in the range of -70 – 130 ns in the pulsed measurements. Measurements are performed on wafer D. ©2020 IEEE.

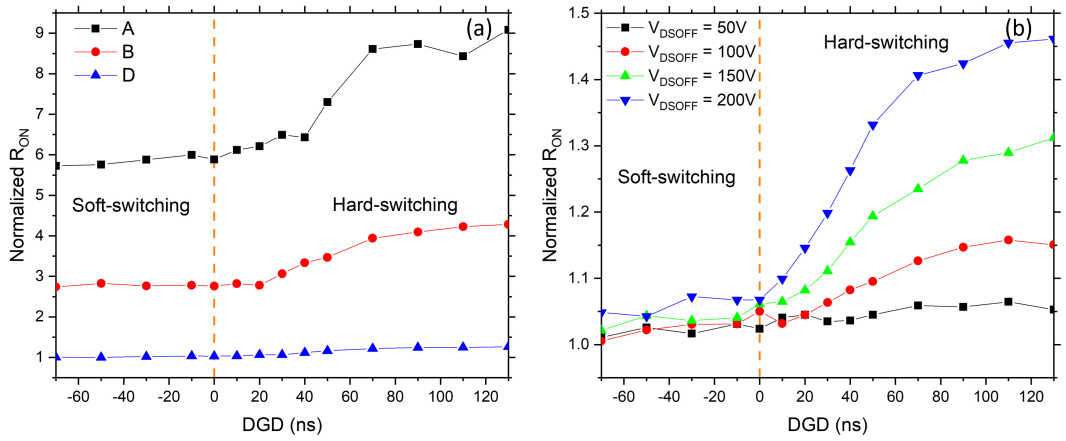

FIGURE 4.5. (a) Dependence of normalized R_{ON} on DGD in wafer A, B and D (V_{DSOFF} = 150 V). (b) Dependence of normalized R_{ON} on DGD in wafer D for V_{DSOFF} ranging from 50 V to 200 V. ©2020 IEEE.

and saturates when DGD > 70 ns. The magnitude of the dynamic R_{ON} during hard-switching increased monotonically with V_{DSOFF}.

Figure 4.6 shows the temperature dependence of R_{ON} against DGD on a range of temperature (40 - 90 °C) in wafer D. The measurements were implemented by manually setting different

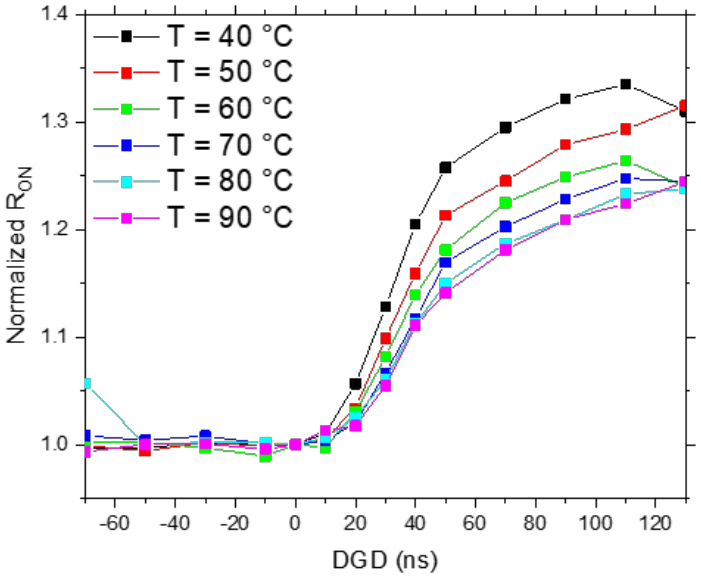

FIGURE 4.6. Dependence of normalized R_{ON} on DGD for temperature varying from 40 °C to 90 °C (V_{VDSOFF} = 150 V). Measurements were performed on wafer D.

background temperature with a thermal chuck on the bottom. In order to minimize the effect of temperature on the electron mobility, the R_{ON} is normalized to the case when DGD = 0 ns (assuming there is no hot electron or temperature effect at this condition). For soft-switching conditions, the temperature will not affect the normalized R_{ON} while for hard-switching conditions, the normalized R_{ON} decreases monotonically with the increase of temperature.

To further investigate the recovery of ON-resistance after hard-switching, the pulsed measurements with a longer ON-state time (t_{ON}/t_{OFF} = 1 ms/1ms, V_{DSOFF} = 150 V) were taken in wafers A and D, and the results are displayed in Figure 4.7. In wafer A, the large dynamic R_{ON} is dependent on DGD at short times but becomes independent of DGD by 1000 µs. However, in wafer D, the device has fully recovered in less than 10 µs after hard-switching (DGD = 130 ns).

4.4 Simulation

In order to help explain the dynamic performance of hard-switching, 2D-TCAD simulations were conducted by Silvaco Atlas. A device structure has been constructed including the gate field plate and two source field plates with the same dimensions as the device under test (L_{SG} = 3.5 µm, L_G = 1 µm, L_{GD} = 13.4 µm). The epitaxy is represented by a representative structure which consists of a 20-nm AlGaN barrier, a 300-nm UID GaN channel layer with a 2DEG carrier density 3×10^{12} cm^{-2}, a 700-nm carbon doped GaN layer and a 4-µm strain relief layer which is

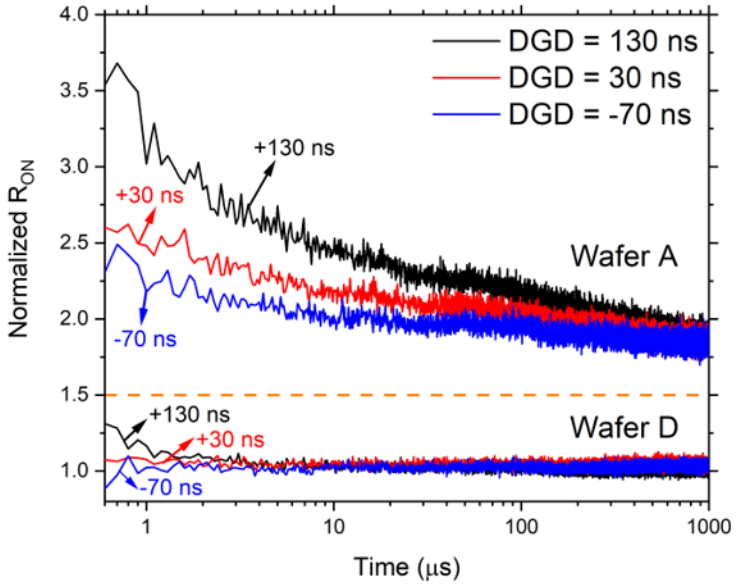

FIGURE 4.7. The transient normalized R_{ON} for different DGDs in wafer A and D (t_{ON}/t_{OFF} = 1 ms/1ms, V_{DSOFF} = 150 V, DGD = -70 ns, 30 ns, 130 ns). ©2020 IEEE.

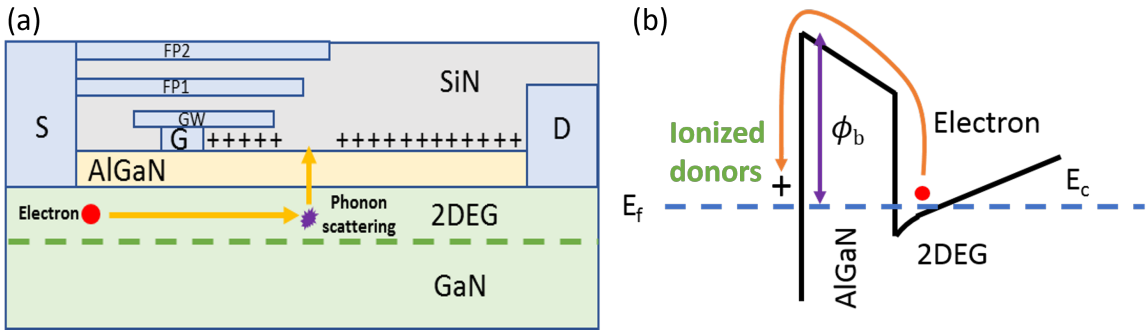

FIGURE 4.8. (a) Schematic of the hot electron injection model of GaN HEMTs in simulation. The electrons gains energy from the electric field and become hot electrons in the 2DEG, which are possibly scattered the phonons. Part of the scattered electrons may be re-directed to the top surface and penetrate the AlGaN barrier and neutralize the surface donors. (b) The path of hot electrons penetrating the AlGaN barrier (ϕ_b) in the band diagram.

implemented as undoped AlGaN. For wafer D which shows no dependence of dynamic R_{ON} on the drain voltages after the soft-switching, the carbon acceptor (C_N) energy level was set to 0.9 eV below the conduction band in order to suppress any bulk-related dynamic R_{ON} [2]. The UID GaN layer is doped with 1×10^{15} cm^{-3} shallow donors. The doped GaN layer is doped with 1×10^{19}

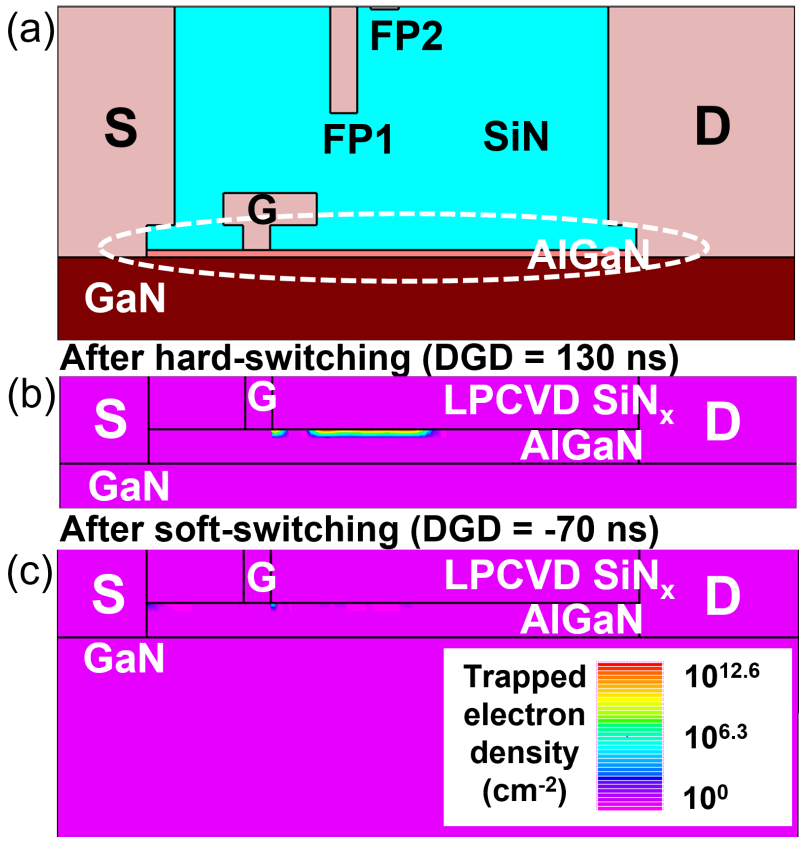

FIGURE 4.9. Simulated surface trapped electron distribution along the AlGaN barrier surface. (a) The device structure built in Devedit for Silvaco Atlas simulation. FP1 and FP2 refer to the two source field plates. (b) Simulated surface trapped electron distribution after the hard-switching (DGD = 130 ns, V_{DSOFF} = 150 V). (c) Simulated surface trapped electron distribution after the soft-switching (DGD = -70 ns, V_{DSOFF} = 150 V). ©2020 IEEE.

cm^{-3} carbon acceptor (C_N) and 3×10^{18} cm^{-3} shallow donors giving a compensation ratio of 0.3.

The simulation includes the Hansch model to calculate the charge trapping [87, 88]. This model was initially built for the hot carrier degradation in Si metal oxide semiconductor field effect transistor (MOSFET). The basic assumption in the Hansch model is that the hot carriers have a probability to be scattered by the lattice and penetrate through the SiO_2 layer and trapped in the pre-existed SiO_2/Si interface traps. Considering the similarity between the GaN HEMT and Si MOSFET structures, some adaptions have been made for this work. In GaN HEMTs, the source of electrons in the 2DEG are generally from the AlGaN surface donors and positive charges are left on the surface [47]. Therefore, when hot electrons are re-directed to the AlGaN surface randomly by the scattering from the lattice, these electrons have a chance to get through the the AlGaN barrier (ϕ_b) and neutralize the surface donors. This mechanism is illustrated in Fig. 4.8. The rate of the charge neutralization is expressed as

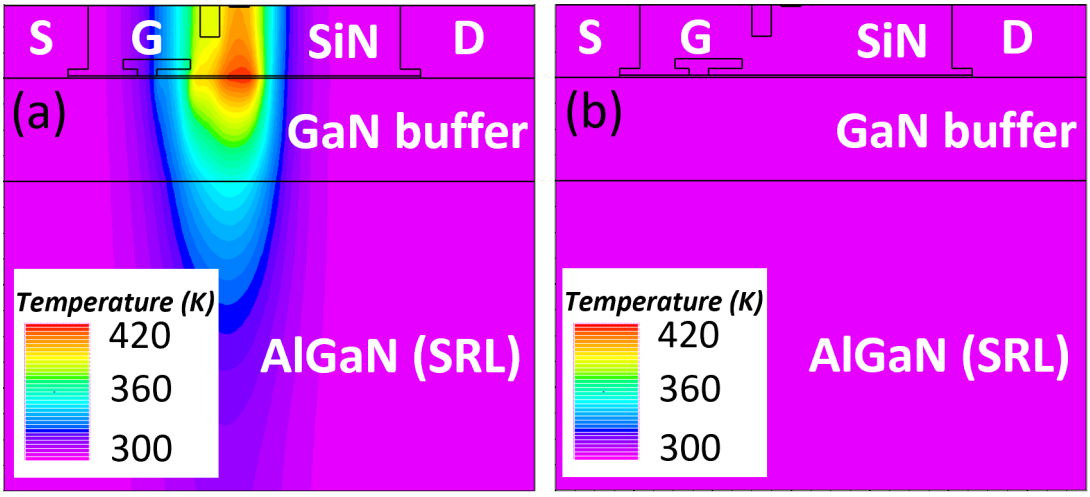

FIGURE 4.10. Simulated 2D device temperature distribution (choose the time when the maximum temperature peak appears during the switching). (a) The temperature distribution during the hard-switching (DGD = 130 ns, V_{DSOFF} = 150 V). The hot spot around 420 K is under the source field plates. (a) The temperature distribution during the soft-switching (DGD = -70 ns, V_{DSOFF} = 150 V). There is almost no temperature increase during the soft-switching.

$$\frac{dN(x,t)}{dt} = \frac{\sigma}{e} J_{inj}(x,t)(N_{+}(x) - N(x,t)) \tag{4.1}$$

where N(x,t) is the neutralized charge density at position x and time t, σ is the cross-section of the donors, $J_{inj}(x,t)$ is the injected electron current density towards the AlGaN barrier at position x and time t, and $N_{+}(x)$ is the ionized donor density at position x. The injected electron current takes into account the probability of the electron phonon scattering and the probability of the electron overcome the energy barrier ϕ_b. The drawback of this model is that it only includes the trapping and does not consider any detrapping processes.

To implement soft-switching and hard-switching in simulation, the device is ramp up to the static OFF-state bias point (V_{GS} = -5 V, V_{DS} = 150 V) first, followed by the switching waveform to the ON-state (V_{GS} = 0 V, V_{DS} = 1 V) with different DGDs as shown in Figure 4.2. The V_{GS} rise time used in simulation is 100 ns and the V_{DS} fall time is 70 ns which are aligned with measurement results. The codes used for this simulation can be found in Appendix C.

Figure 4.9 (a) shows the device structure built in Devedit. Figure 4.9 (b) and (c) illustrates the simulated surface trapped electron distribution immediately after hard- and soft-switching. Note that there is almost no surface charge left after soft-switching while distributed surface charge can be found on the top of AlGaN after hard-switching.

The self-heating effect has also been simulated for hard- and soft-switching in Silvaco Atlas. To pursue better convergence in simulation, the hot electron model is disabled and the thermal

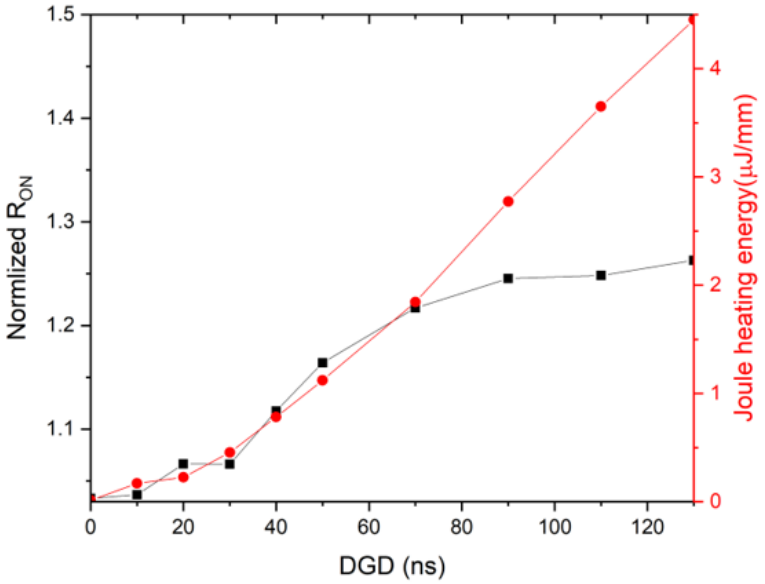

FIGURE 4.11. Normalized R_{ON} and total Joule heating energy dissipated during hard-switching versus DGD in wafer D (V_{DSOFF} = 150 V). The Joule heating energy is calculated by the integration of I-V curves during hard-switching. ©2020 IEEE.

model (to calculate the joule heating generation and the heat dissipation) is enabled for this particular purpose. The simulation results are shown in Figure 4.10 (a) and (b), as the maximum temperature during hard-switching arises to around 420 K and negligible temperature rise has been noticed during soft-switching.

4.5 Discussion

In Figure 4.5, it is observed that after soft-switching, there was a significant increase of dynamic R_{ON} in wafers A and B, but not in wafer D. This is fully consistent with published measurements on these wafers, and can be explained by the previous finding that leakage paths within the UID GaN layer in wafer D strongly suppress the accumulation of negative charge trapping in the buffer [83–85]. However, after hard-switching, an additional increase of R_{ON} has been found which recovers in less than 10 μs (Figure 4.7) and shows a V_{DSOFF}-dependent behavior. To explain that, here two possible mechanisms are considered that can be involved in this phenomenon: the self-heating and the hot electrons.

For the self-heating effect, the presence of simultaneous high electric field and high channel current during hard-switching will contribute to high power dissipation and result in a channel temperature rise. This temperature rise can be possibly responsible for the dynamic R_{ON} [64, 82].

In order to investigate this hypothesis, the total heat energy dissipated is calculated during hard-switching by integrating the I-V curves and plot it with the dynamic R_{ON} against DGD in Figure 4.11. The heat energy increases almost linearly with the DGD which implies that the temperature of the channel during switching would increase with DGD without saturation. However, the dynamic R_{ON} actually saturates when DGD > 70 ns indicating the temperature no longer affects the device. Based on this observation, a conclusion can be drawn that the self-heating effect does not play a major role in the increase of R_{ON} after hard-switching. The simulation results tell the same story. As shown in Figure 4.12 (a), for hard-switching (DGD = 130 ns) the cooling rate is so fast that there is only a small channel temperature rise (6 °C) within the measurement window. It also suggests that the self-heating is not responsible for the dynamic R_{ON} after hard-switching.

For the second mechanism which has been discussed in [64, 82], electrons become 'hot' under high electric field during hard-switching and are trapped either on the surface or in the buffer. An evidence of the presence of hot electron effect during hard-switching is shown in Figure 4.6. With a higher ambient temperature, there is a reduction of normalized R_{ON} after hard-switching. It is because of that the scattering rate of hot electrons with the lattice or impurities increases with the temperature, and in return, the mean free path of hot electrons reduces and it finally leads to an reduction of average hot electron energy. Therefore, at high temperature, it becomes harder for the hot electrons to overcome any energy barrier and to take effect.

In Figure 4.7, the recovery of R_{ON} after hard-switching was measured. In wafer A, apparently, there are at least two types of trapping showing different time constants. The results suggest that the time constant of the fast trapping in wafer A is < 1000 µs, and in wafer D is < 10 µs, which is much less than the time constant of carbon-related buffer trapping (10 ms – 1 s for vertical transport [58] and ~ 100 s for lateral transport [18, 89]). This fast detrapping observation suggests that the traps responsible are relatively shallow. Consequently, surface trapping is a more plausible explanation for the increase of R_{ON} after hard-switching. Tanaka et al. [90] have also argued that hot electrons generated during hard-switching would be trapped on the surface in GaN-based gate injection transistors (GIT) in their observation of electroluminescence results. In addition, according to [83], the wafer D with a Si-rich LPCVD passivation shows no negative charge trapping in the carbon-doped GaN layer under a high substrate bias. It implies that the negative charge will not be trapped in the buffer layer due to the vertical conductive dislocation path. Therefore, even if there are any negative charge induced by the hard-switching, it can hardly observed by the from wafer D. However, in wafer A and B, due to the significant increase of R_{ON} after the soft-switching, it is hard to distinguish the surface and bulk charge trapping.

Besides, notice that in Figure 4.4 (b) the maximum V_{DS} and I_{DS} during switching will no longer increase for DGD > 70 ns, while in Figure 4.5 the R_{ON} becomes saturated for the same condition. It implies that the increase of R_{ON} after hard-switching mainly relies on the energy of the hot electrons during hard-switching, and further accumulation of trapped electrons becomes

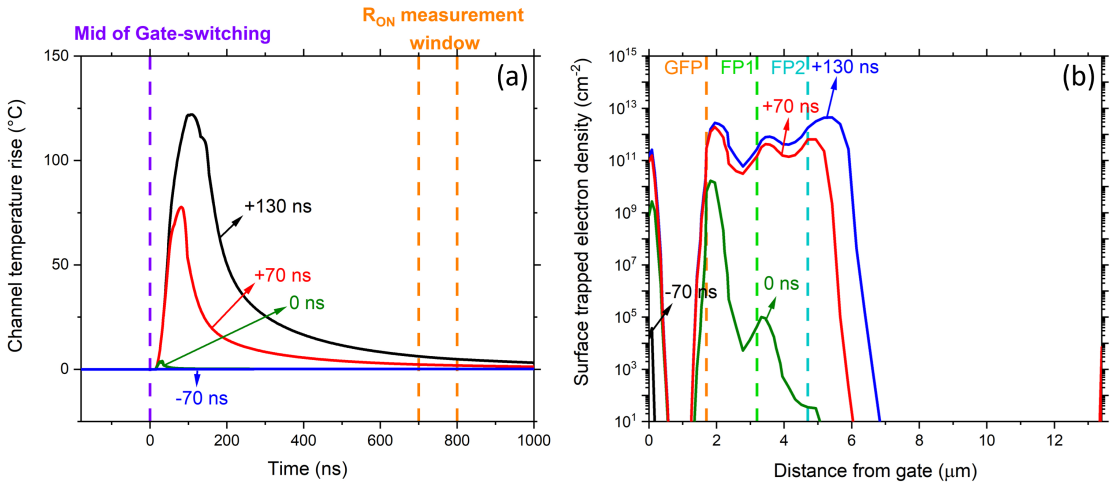

FIGURE 4.12. Simulation of soft- and hard-switching with self-heating and surface trapping models. (a) Simulated channel temperature rise against time under the soft- and hard-switching conditions (V_{DSOFF} = 150 V). (b) Simulated surface trapped electron density along the AlGaN barrier surface from the gate edge to the drain edge after switching (V_{DSOFF} = 150 V). ©2020 IEEE.

weak if DGD > 70 ns. Similarly, in Figure 4.12 (b), it is observed that after switching, the simulated trapped surface electron density increased dramatically when DGD changed from -70 ns to 70 ns, but then increasing more slowly for DGD > 70 ns (the continuing increase being consistent with the absence of detrapping in this simulation). In the meantime, the field plates show a significant impact on the electron distribution as trapped electrons accumulate near the edges of field plates. This occurs because the electric field reaches its peak near the edge of field plates and thus hot electrons can easily gain high energy there.

Simulation results in Figure 4.13 (a) and (b) provide insight into how different V_{DSOFF} affects the dynamic R_{ON} after hard-switching. In Figure 4.13 (a), as V_{DSOFF} increases from 50 to 150 V, the lateral electric field expends from the gate wing to the edge of two source field plates. Figure 4.13 (b) shows the simulated surface trapped electron density and it follows the same pattern of the lateral electric field. It is because of that the electrons can easily get high energy where the electric field is high. Consequently, with the expansion of trapped electron range, the dynamic R_{ON} after hard-switching will increase with the V_{DSOFF}.

To suppress this effect, in principle, a more aggressive design of field plates could reduce the peak electric field within the 2DEG to avoid the formation of hot electrons with extremely high energy. Meanwhile, by comparing wafers from A to D, where the LPCVD passivation layer becomes Si-rich, the device shows better robustness under the hard-switching condition. It is due to two facts. Firstly, as described in [83], wafer A shows strong negative buffer trapping under high voltage stress while wafer D does not. Secondly, Figure 4.6 implies that wafer A also tends

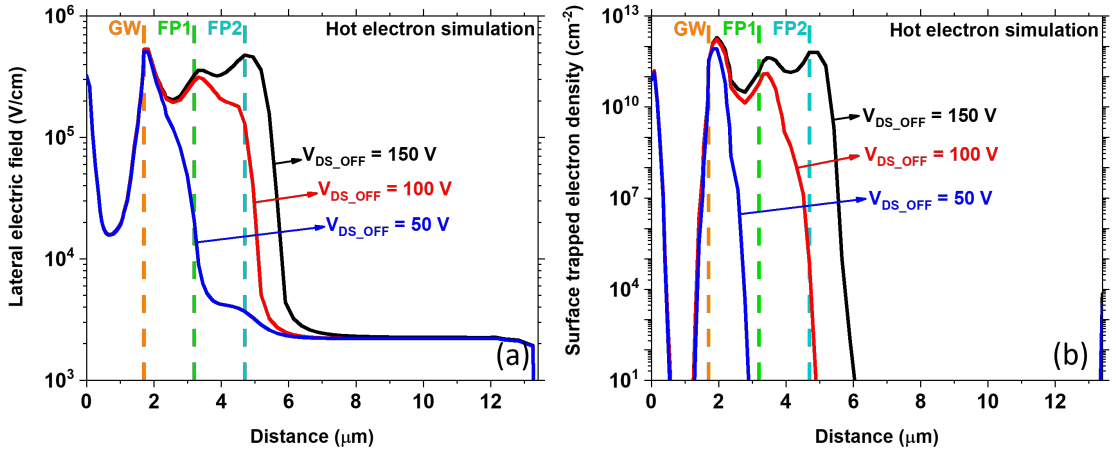

FIGURE 4.13. (a) Simulated lateral electric field within 2DEG from the gate edge to the drain edge after hard-switching with DGD = 70 ns for V_{DSOFF} = 50, 100, 150 V. (b) Simulated AlGaN surface trapped electron density from the gate edge to the drain edge after hard-switching with DGD = 70 ns for V_{DSOFF} = 50, 100, 150 V. GW refers to the gate wing. FP1 and FP2 refer to the two source field plates.

to be more vulnerable to surface trapping under hard-switching condition compared to wafer D. Hence it appears that negative surface charge may be more easily stored in the device with the stoichiometric Si_3N_4 layer, with Si-rich SiN_x able to dissipate any hot electrons perhaps as a result of its higher AlGaN leakage [84]. By using the wafer with the Si-rich passivation layer it is able to achieve lower dynamic R_{ON} after both soft- and hard-switching.

4.6 Conclusion

In this chapter, the dynamic behavior is discussed after hard-switching in GaN-on-Si HEMTs with a set of wafers with different stoichiometries of LPCVD SiN_x layers. Pulsed measurements were taken showing an increase in dynamic R_{ON} after hard-switching compared to soft-switching.

Two mechanisms (self-heating and hot electrons) have been proposed to explain the dynamic R_{ON} after hard-switching and they are investigated separately. For the self-heating effect, the experimental results suggest that the temperature after hard-switching does not affect the device performance. 2D-TCAD simulations have been carried out for the same time frame which shows a fast cooling rate of the device and only negligible channel temperature rise in the measurement window. For the hot electrons, the recovery of dynamic R_{ON} is measured to investigate how long this effect will last. The results imply the presence of some fast trapping which cannot be linked to the dominant carbon-related buffer trapping. The simulation further shows hard-switching-induced surface electron trapping in the vicinity of the gate is consistent with the measurements.

Thus, the conclusion can be reached that hot electrons generated during hard-switching will be trapped on the surface and reduce the ON-resistance. By modifying the field plates and stoichiometries of SiN_x it is possible to solve this problem.

CHAPTER 5

BUFFER CHARGE TRAPPING IN POWER ALGAN/GAN-ON-SI HEMTS

Charge trapping is a major issue for power AlGaN/GaN HEMTs, which will lead to current collapse and efficiency losses during application. Charge trapping exists either on the surface [75] or in the GaN buffer [20]. Typically, in power GaN transistors where a carbon-doped buffer layer is used to prevent the punch through effect [91] and to suppress breakdown, the C_N carbon acceptor (E_a = 0.8 ± 0.2 eV) is reported as the major buffer trap. Several measures have been adopted to minimize trap-related current collapse, i.e. field plates [92] and epitaxy [93].

In this chapter, the buffer charge trapping appeared during ON-state operation (V_{DS} = 40 V, V_{GS} = 0 V, I_{DS} = 0.18 A/mm) in power AlGaN/GaN HEMTs has been investigated. The wafers used in this chapter are same as that in chapter 4 provided by Nexperia. Section 5.1 introduces the research background of charge trapping in GaN HEMTs and Section 5.2 illustrates the devices under test and the experimental results are presented in Section 5.3, showing the dynamic R_{ON}, potential mapping and EL measurements. In Section 5.4, the thermal simulation of On-state operation in GaN HEMTs is implemented. In Section 5.5 the results are analyzed and determine the distribution of buffer charge trapping under different situations. Finally, Section 5.6 concludes this work.

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5.1 Introduction

Simultaneous applied voltage and current operation is an important regime for power transistor application when the transistor is switched from OFF-state to ON-state, resulting in a high electrical field and a high current during switching [95]. Hot electrons and high temperature will be involved during this regime and the consequently induced charge trapping can be a reliability issue for GaN HEMTs [96]. The ON-state is sometimes referred to as semi-ON or hard-switching [82]. Meneghini et al [73] investigated the device degradation after the semi-ON-state stress (V_{DS} = 30 V) in GaN HEMTs, and found it was only partially recoverable with UV light illumination. Meneghini et al [96] also determined that an additional charge trapping (with short detrapping time constant < 1 s) can be induced during semi-ON-state compared to the OFF-state in GaN HEMTs. In Chapter 4, the study of hard-switching show that hot electrons could induce surface trapping causing an increase of R_{ON}.

Several studies have shown how SiN_x LPCVD passivation layers with different stoichiometries can affect charge trapping in the GaN HEMTs during OFF-state. In [83], using transient dynamic R_{ON} and substrate bias measurements, it is shown that negative charge trapping can occur due to the high vertical electrical fields in the devices; but it is suppressed by a Si-rich passivation. In [85], charge trapping distributions following OFF-state stress on the same wafers were measured by C-V using Schottky gate sensing probes to the channel and it was found that negative charges either accumulate locally at the field plate edge or spread along the gate-drain access region.

In this chapter, in contrast to these previous studies [78][83][85], the long-period ON-state stress (V_{DS} = 40 V, V_{GS} = 0 V for 10 s) has been investigated in power AlGaN/GaN HEMTs, a stress which is sometimes used in reliability tests, and show that long time constant charge trapping recovery can be induced, and that it can be strongly suppressed by the use of Si-rich passivation. In temperature-dependent measurements, ON-state stress and substrate stress induce buffer trap responses with an activation energy of 0.44 - 0.48 eV. By analysing the Schottky gate probe data, it is shown that the negative charges are distributed along the top of carbon-doped GaN layer, but especially accumulate under the gate in ON-state. The charge accumulation and relaxation are discussed in terms of the leaky dielectric model of the buffer [18][97]. The results show that the recovery time constants are all consistent with rate limiting hopping transport from the carbon-doped layer rather than trap emission, and explain the presence of two different time constants from just one trap state [89]. This data provides strong support for the leaky-dielectric model.

Electroluminescence measurements show apparent light emission from the drain edge, however using sense probe measurements it is shown that in fact the EL occurs under the gate with refraction/reflection of the light at the drain edge. This potentially important result suggests that care should be used when using EL to identify the location of high fields in GaN HEMTs.

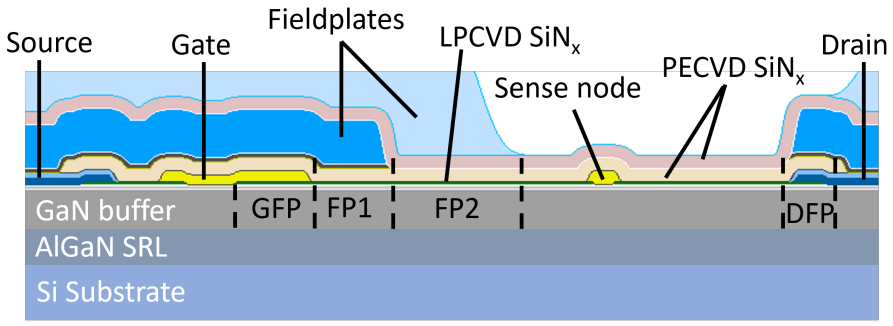

FIGURE 5.1. Schematic of GaN HEMTs with Schottky sense node structures (not to scale). GFP is the gate connected field plate, and FP1 and FP2 are two source field plates. ©2021 IOP Publishing.

5.2 Device under Test

The wafers used in this chapter are same as Chapter 4. To characterize the potential distribution in the devices, HEMTs with an additional Schottky contact (sense node) at different positions between gate and drain were used. A cross-section is shown in Figure 5.1. The positions of the sense nodes are 4.5, 5.5, 7.5, 9.5, 10.5 μm away from the gate edge [85].

5.3 Experimental Results

Figure 5.2 (a) presents measurements of time-dependent dynamic R_{ON} of GaN HEMTs after 10 s OFF-state and ON-state stress for wafers A, B and D, measured at V_{DS} = 1V, V_{GS} = 0V. In the OFF- and ON-state stress, V_{DS} is always kept at 40 V while V_{GS} = 0 V for ON-state and V_{GS} = -5 V for OFF-state (Vth = -2 V). After OFF-state stress, less than 10 % increase in R_{ON} can be observed in all three wafers. However, after ON-state stress increased dynamic R_{ON} is seen and especially in wafers A and B which are closer to Si_3N_4 stoichiometry.

In Figure 5.2 (b), the potential distributions during OFF- and ON-state are characterized by using the HEMTs with sense nodes. In these measurements, the source is grounded and the gate is biased at -5 V for OFF-state and 0 V for ON-state. Meanwhile, the sense node is forced with 1 nA constant current while the drain is swept from 0 V to 40 V slowly (~ 0.83 V/s). Thus, it is able to obtain the potential of the sense node in nearly steady state when V_{DS} = 40 V [83][85].

During OFF-state, as expected all three samples show the same potential distribution with all the voltage drop occurring near the gate edge; there is no potential change in the gate-drain access region where the probes are located. However, during ON-state operation, a variation of potential distribution between the gate and the drain can be observed between the three wafers. From wafer D to A, the potentials in the ungated region start to drop, and eventually lead to a significant potential drop in the vicinity of the drain edge in wafer A.

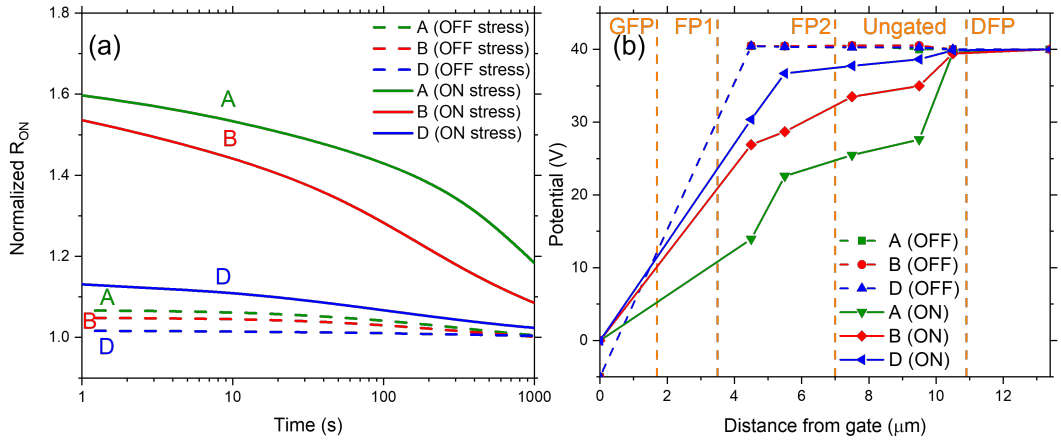

FIGURE 5.2. (a) Dynamic R_{ON} measured after the OFF-state stress (V_{DS} = 40 V, V_{GS} = -5 V for 10 s) and ON-state stress (V_{DS} = 40 V, V_{GS} = 0 V for 10 s) in wafer A, B and D. The average measured currents during ON-state stress are 0.179, 0.172 and 0.176 A/mm for wafer A, B and D respectively. (b) Potential distribution measured in the gate-drain access region during OFF-state (V_{DS} = 40 V, V_{GS} = -5 V) and ON-state (V_{DS} = 40 V, V_{GS} = 0 V) in wafer A, B and D. The OFF-state potential distributions of three samples are almost overlaid.

Electroluminescence measurements are carried out with a 50 × objective and Opticstar charge-coupled device (CCD) camera by biasing HEMTs in ON-state. Figure 5.3 shows the measured EL intensity against V_{GS} in wafer A, B and D. Wafer D shows visible EL emission, however, no significant EL emissions were recorded in wafers A and B for V_{DS} up to 40 V. As seen in the inset of Figure 5.3, it is able to determine that in wafer D, the EL emission appears to come from the edge of the drain, and at the side contact to the gate and drain.

In Figure 5.4, temperature-dependent drain current transient measurements following OFF-state stress (V_{DS} = 40 V, V_{GS} = -5 V for 10 s), ON-state stress (V_{DS} = 40 V, V_{GS} = 0 V for 10 s) and Si substrate stress (V_{SUB} = -150 V, V_{DS} = 1 V and V_{GS} = 0 V for 10 s) have been performed in order to extract the apparent activation energy of the possible trap responses in wafer A. This technique to characterize the charge trapping is also known as current mode deep-level transient spectroscopy (I-DLTS) [98]. The substrate bias stress, in contrast to the drain stress which has a high lateral field component, primarily applies a vertical electric field between the 2DEG and the Si substrate. Figure 5.4 (a) and (b) show the temperature-dependent recovery of dynamic R_{ON} after the OFF- and ON-state stress; the S-shape curves suggest the existence of a dominant detrapping process (labelled as type X and Y). In Figure 5.4 (c), after the substrate stress, the recovery curves show two quite distinct detrapping processes (labelled as type I and II). Figure 5.5 shows conventional Arrhenius plots assuming that trap emission is the rate limiting step

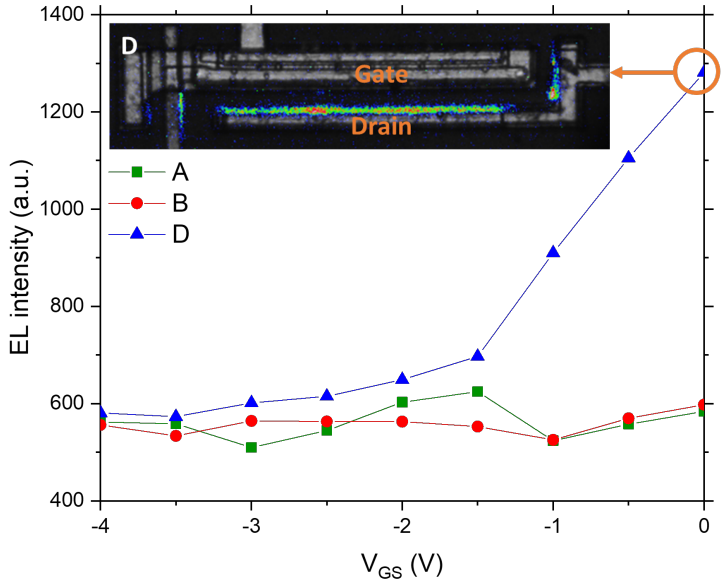

FIGURE 5.3. Measured electroluminescence intensity against V_{GS} in wafer A, B and D (V_{DS} = 40 V, exposure time = 10 s). The inset shows the captured image in wafer D (V_{DS} = 40 V, V_{GS} = 0 V). ©2021 IOP Publishing.

for the responses found in Figure 5.4. The emission process can be described by the Arrhenius function

$$ln(\tau T^2) = \frac{E_a}{k_B T} + ln(\frac{1}{\lambda\sigma}) \tag{5.1}$$

where τ is the emission time constant, E_a is the activation energy for the electron to emit from the trap, σ is the capture cross-section, and λ is a physical constant and its expression is

$$\gamma = 2\sqrt{3}(2\pi)^{\frac{3}{2}} k^2 m^* h^{-3} \tag{5.2}$$

where m^* is the effective electron mass, and h is the Planck constant [98]. All the responses, type I, II, X and Y show a similar apparent activation energy with Type I ~ 0.43 eV, Type X ~ 0.40 eV, while type Y and II have ~ 0.50 eV and similar apparent capture cross-section. However, according to [58], in heavily carbon-doped devices, the measured time constant is dominated by the transport through a defect band and not activation to the band edge. Hence, the fitted activation energies would not represent trap energy levels but be related to the transport process.

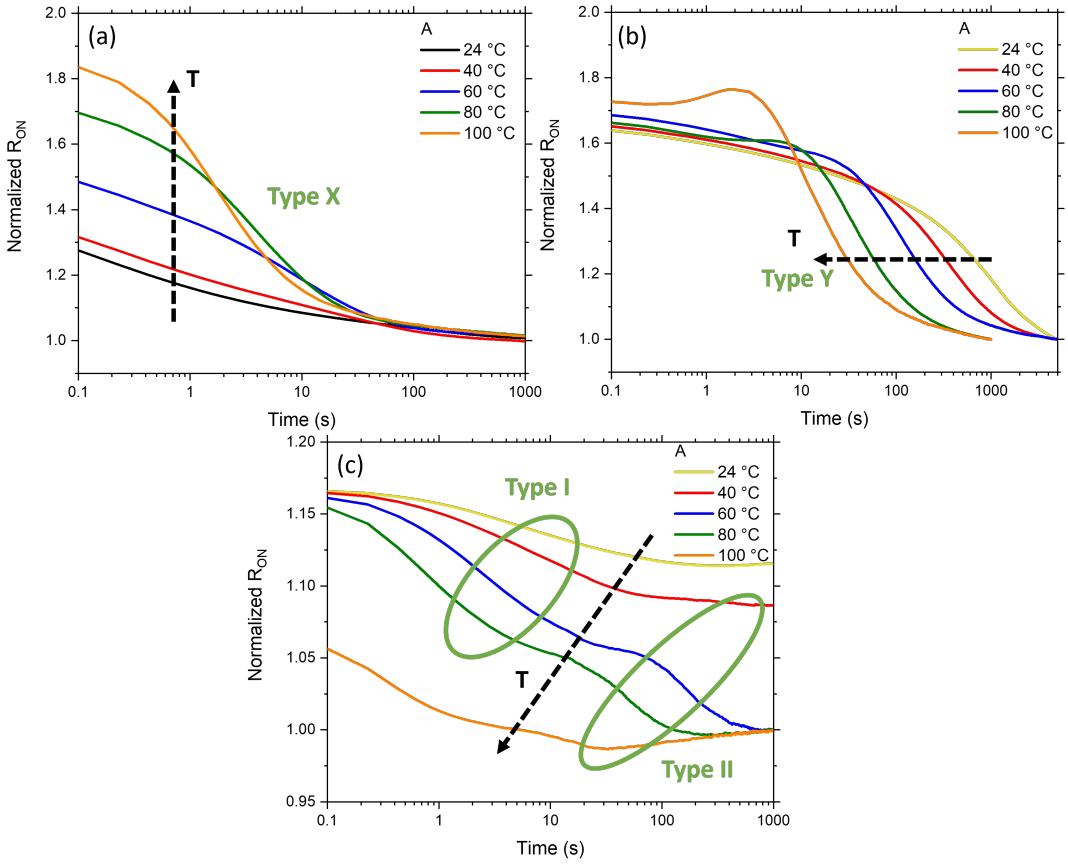

FIGURE 5.4. (a) Temperature-dependent dynamic R_{ON} measured after the OFF-state stress (V_{DS} = 40 V, V_{GS} = -5 V for 10 s) in wafer A. (b) Temperature-dependent dynamic R_{ON} measured after the ON-state stress (V_{DS} = 40 V, V_{GS} = 0 V for 10 s) in wafer A. (c) Temperature-dependent dynamic R_{ON} measured after the substrate stress (V_{SUB} = -150 V, V_{DS} = 1 V and V_{GS} = 0 V for 10 s) in wafer A. Measurement conditions during transient are V_{DS}=1 V, V_{GS}= 0V. The apparent trap responses are highlighted as type X, Y, I and II.

5.4 Simulation

In this section, to estimate the thermal effect from the measurement condition, the thermal simulations with a broadly similar structure (AlGaN barrier thickness = 20 nm, GaN thickness = 2 µm, AlGaN SRL thickness = 3 µm, Si thickness = 1 mm) were implemented in Ansys, as shown in Figure 5.6. The thermal parameters used in the simulation are given in Table 5.1. In this simulation, an equilibrium ON-state condition of V_{DS} = 40 V, V_{GS} = 0 V, I_{DS} = 0.18 A/mm has been adopted, which gives a power of 7.2 W/mm. This leads to a maximum channel temperature increase of about 218 °C (from the ambient temperature 22 °C). A drain bias of 40 V

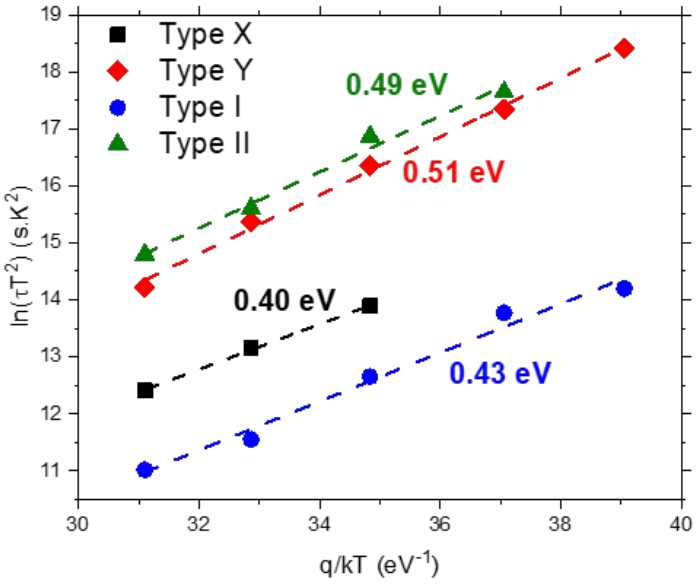

FIGURE 5.5. Arrhenius plot of the acceptor-like trap responses (Type X, Y, I and II) as identified in Figure 5.4.

Table 5.1: Thermal conductivities κ and their temperature-dependent coefficients η at room temperature [99][100].

	GaN	Si	SRL
κ, $Wm^{-1}K^{-1}$	160	148	12
$\kappa(T^{-\eta})$	$T^{-1.4}$	$T^{-1.28}$	-

was the highest bias that could be applied without permanent degradation, and the calculated temperature rise is quite consistent with this being thermally driven.

5.5 Discussion

5.5.1 Dynamic R_{ON} and Potential Distribution

In Figure 5.2 (a), the relatively low 40 V OFF-state stress in a device designed for 650 V results in small increase of R_{ON} at room temperature, although it can be significant under a higher temperature. In contrast, there is a much larger increase of R_{ON} after the ON-state stress which is dependent on LPCVD stoichiometry. The self-heating [101] can potentially be the reason for the dynamic R_{ON} as the thermal simulation reveals a relatively high channel temperature (240 °C). However, during ON-state stress, wafers A, B and D show a similar current level (0.17 – 0.18

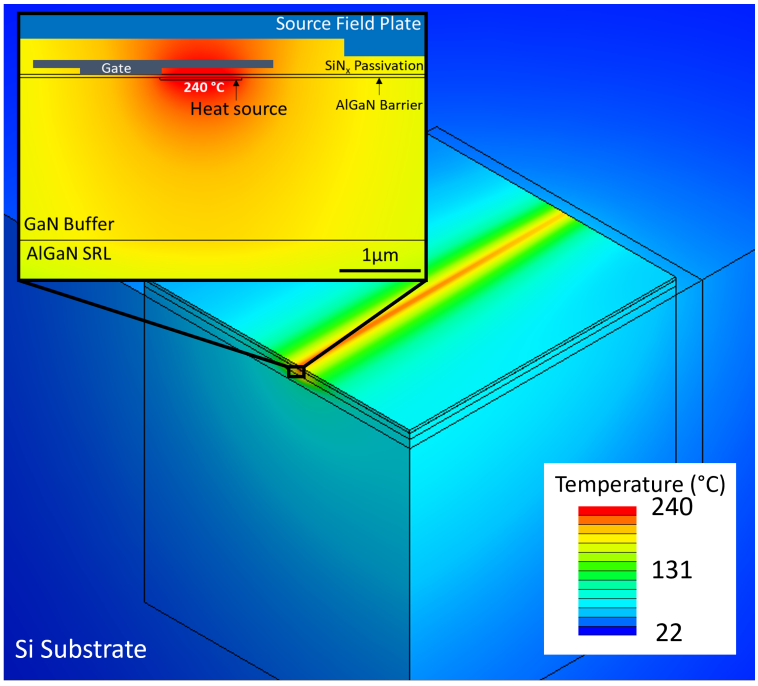

FIGURE 5.6. The 3D finite element model shows the simulated temperature distribution during the ON-state. This structure includes the Si substrate, the AlGaN SRL, the GaN buffer, the AlGaN barrier and the SiN_x passivation. The model assumes a constant heat input (2.4×10^{17} W/m^3) inside the heat source (30 nm × 1 µm × 1 mm) in vicinity of the gate edge. The inset shows the maximum equilibrium channel temperature of about 240 °C. ©2021 IOP Publishing.

A/mm) suggesting that they are experiencing a similar temperature. Hence, the self-heating is not the major reason here as wafer A does not exhibit a large increase of R_{ON} after the ON-state stress.

In Figure 5.2 (b), there are almost no differences between the potential distribution between wafer A, B and D during OFF-state, since the potential is almost entirely dropped under the gate foot and the gate wing edge. Meanwhile during ON-state stress, as the Si content decreases in the LPCVD passivation from wafer D towards stoichiometry of wafer A, the potential drops in the ungated region, and the electric field peak near the gate edge partially moves to the drain edge. The presence of a current in the channel makes any reduction in 2DEG density in the gate-drain gap visible since the region under the gate is no longer necessarily the highest resistance part of the channel. It suggests that there are trapped negative charges accumulated not just under the gate edge (saturated HEMT operation always results in negative ionized acceptor charge near the gate edge to support the lateral field in this region [102]) but also in the entire gate-drain gap during ON-state, and the density of these negative charges increases from wafer D to A. Related effects have been observed previously such as in OFF-state in [85], and Meneghini et al [103] have reported in p-Gate HEMTs, the electrical field peak can gradually shift from the gate edge

towards the drain edge as time goes by due to the negative charge trapping in the gate-drain access region. Optical measurements have also revealed a peak field at the drain [104].

5.5.2 Electroluminescence

In Figure 5.3, it can be observed that the high EL emission largely from the edge of the drain in wafer D. EL is primarily originated from the Bremsstrahlung effect in GaN HEMTs, where the electron loses its energy and emits photons near scatterers in the high electric field [32]. However, the potential measurements indicate that the electric field peak in wafer D only appears near the gate edge, not the drain edge. The explanation is that the EL emission occurs under the field plates near the gate but is only visible where there are no field plates giving optical access, and light, guided along the GaN layer, is reflecting/refracting from the drain contact metal. That is also why EL emission was observed near the drain and also the source contacts at the device sides where there is no current. Based on that explanation, the EL results are consistent with the potential measurements. This result suggests that care needs to be taken when interpreting the location of EL emission based purely on the EL images. From wafer D to A, the peak electric field near the gate edge is significantly reduced during the ON-state, thus no EL emission can be found in wafer A and B.

5.5.3 Charge Trapping

According to Figure 5.4, the negative charge trapping type X under the OFF-state stress, type Y under the ON-state stress, and type I and II under the substrate bias in wafer A can be extracted. In substrate bias measurements, any surface or upper barrier traps have been completely screened by the presence of the 2DEG during stress. Therefore, the type I and II trapping must be located in the buffer (most likely carbon-doped GaN layer where there is a high density of deep acceptors). Figure 5.5 shows the Arrhenius plots of all three types and in particular, the type Y and II share similar activation energy and apparent capture cross-section, while the type I and X do not. Hence, the type Y and II are supposed to have the same origin in the buffer.

The potential measurements can help to determine the location of the charge associated with the type Y response. Negative charge trapping will partially deplete the 2DEG and increase the resistance through the backgating effect [105]. Thus, a higher resistance suggests a higher density of negative charge. In the ungated region, the derivative of the potential with respect to the distance from the gate (x) is proportional to the local resistance of the 2DEG (R(x)=V(x)/I and I is a constant throughout 2DEG). Figure 5.7 (a) shows a schematic of negative charge distribution in wafer A during the ON-state by applying this rule (consistent with the detailed simulations in [97]). Some negative charges are accumulated under the drain and gate edges leading to the peak lateral electrical fields, and uniform negative charges are distributed within the ungated region. In contrast, the wafer D shows little negative charge storage in the GaN buffer apart from below the gate edge. The basic difference between wafers A and D can be explained in the leaky

dielectric model [18][97], in terms of the relative vertical leakage through the UID GaN channel. For wafer A, the UID GaN is highly resistive, so under the influence of the drain bias, the less resistive buffer (p-type carbon-doped layer) potential is mostly close to the source potential in the gate-drain gap, resulting in a high back-gate bias in the gate-drain gap. By contrast, for wafer D the leaky undoped channel layer allows the carbon-doped buffer layer to follow the 2DEG potential in the gate-drain gap preventing the formation of a back-gate bias [97].

For wafer A, the charge distribution during the substrate bias is shown in Figure 5.7 (b), where the carbon-doped layer is more conductive than the layers above and below it allows a negative charge to accumulate at its top surface and a positive charge at its bottom surface (Maxwell-Wagner effect [106]) under the influence of the vertical field. Previous substrate ramp measurements have shown that wafer A has a higher leakage to the buffer under the contacts than in the source-drain gap [83], and this results in the negative charge being partly suppressed under the contacts.

During the recovery following stress, the charges in the buffer must eventually leak away via the leakage paths under the contacts (presumably decorated threading dislocations). However the carbon-doped layer has a lower resistivity than the layers above and below, so first charge redistribution and recombination will occur within this layer. Therefore, as shown in Figure 5.7 (c), after the ON-state stress, the localised negative charges at the gate edge will spread out first and then the negatively charged layer will ultimately flow to the Ohmic contact, corresponding to the type Y response. Noticing that there is a small increase of R_{ON} at ~ 10 s for 80 - 100 °C in Figure 5.4 (b), as discussed in [97] it is very likely due to the initial transport of the localised negative charges at the gate edge as they move closer to the top of the carbon-doped layer and then spread, resulting in a transient increase of source resistance and thus the overall resistance.

After the substrate stress, there are two discharging paths as depicted in Figure 5.7 (d). The first path is vertical current flow leading to recombination between the positive and negative charges within the carbon-doped GaN layer [97][89]. The second path is the same as the mechanism discussed for ON-state stress, as the remaining negative charges spread laterally and flow to the contacts. Consequently, it can be concluded that the type Y/II is largely associated with the lateral charge flow to the Ohmic contacts, while the type I is due to the vertical charge flow within the carbon-doped GaN layer. Since ON-state stress for wafer A results in only a small positive charge at the bottom of the carbon-doped layer in the gate-drain gap, any vertical transport is insignificant and cannot be clearly distinguished in Figure 5.4 (a).

The charge trapping in the carbon-doped GaN buffer is expected to be due to the carbon atoms substituted for the N atoms and acting as a deep acceptor 0.8 ~ 0.9 eV above the valence band [57]. Despite this many publications report activation energies in the 0.5 ~ 0.6 eV range and attribute it to a deep level [98], here all the responses are in the range 0.40 ~ 0.51 eV. Based on the results of Koller et al [58], an alternative and more likely explanation is that the rate limiting step determining the activation energy is hopping transport to the acceptor rather than

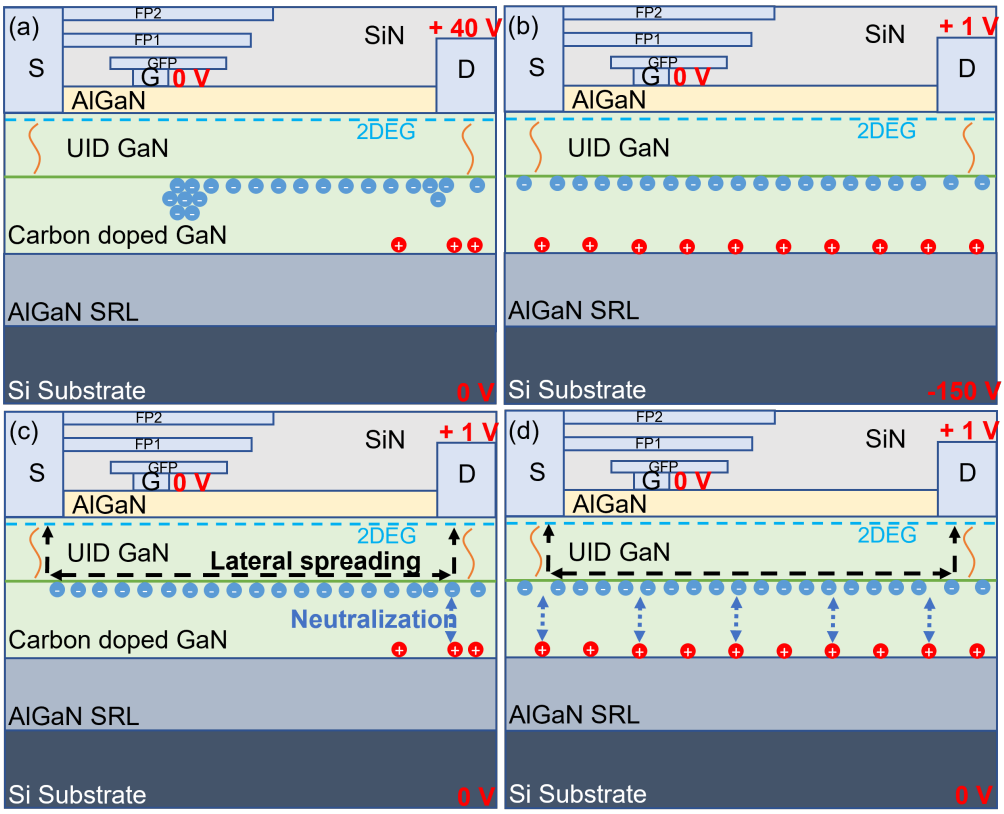

FIGURE 5.7. Schematic of the charge distribution within the GaN buffer layer in wafer A. (a) During the ON-state stress, negative charges are distributed along the interface between the UID GaN and the carbon-doped GaN layer, and localized under the gate edge, affecting the 2DEG through the back-gating effect. Some positive charges may be present on the bottom interface of the carbon-doped GaN layer under the drain contact due to the vertical electric field. (b) During the substrate stress, negative and positive charges accumulate on the top and bottom interfaces of the carbon-doped GaN layer. (c) After the recovery of the ON-state stress, the localized negative charges under the gate spread laterally and then flow to the contacts (type Y).(d) After the recovery of the substrate stress, vertical current flow first neutralizes the positive charges on the bottom interface (type I), while subsequently the remaining negative charges spread laterally and flow to the contacts (type II).

capture/emission to the band edge. They found that if the carbon density is $\geqslant 10^{19}$ cm^{-3}, charge transport occurred primarily in a defect band, instead of the valence band. The temperature dependence was non-Arrhenius but in the vicinity of room temperature, fitting an Arrhenius law over a limited temperature range gave an activation energy of ~ 0.5 eV. The physical presence of type X response is unknown, but it is also possible related to the buffer traps according to [83].

5.5.4 Impact of Passivation Stoichiometry

In Chapter 4, the behavior of the same devices in ON-state conditions at 150 V during hard-switching ($\leqslant$ 130 ns stress) has been characterized. This resulted in hot electron stress leading to charge trapping with a small time constant (< 1 ms) that was attributed primarily to surface trapping. That trapping was dramatically reduced for the non-stoichiometric SiN_x wafer D. By contrast, in this chapter, a much more moderate ON-state bias condition but with significant self-heating and longer stress time of 10 s was used, and the charge trapping with long time constant (~ 1000 s at room temperature) has been characterized. The time constant here, as discussed before, relates to transport within a defect band through a hopping process rather than activation to the valence band edge. As for the hard switching stress study, the wafer D exhibits much reduced sensitivity to dynamic R_{ON} in Figure 4.5 (b). However, in this case the long time constant recovery is primarily consistent with buffer trapping. It suggests that, in hard-switching applications of GaN HEMTs, one will encounter dynamic R_{ON} due to surface and buffer trapping simultaneously, with the surface trapping only affecting the device properties for milliseconds while the buffer trapping can cause performance issues for hours.

An important finding in our study is that the Si-rich LPCVD passivation can suppress both surface and bulk trapping. Currently, no direct evidence has been found to show how the LPCVD layer changes trapping states both at the surface and in the bulk of the device. However a plausible explanation for the suppression of surface trapping is based on the fact that the excess Si in the SiN_x results in a resistive passivation allowing lateral charge leakage leading to recovery of any surface charging [83]. The suppression of bulk trapping is less obvious, however the conduction along dislocations can occur in an impurity band whose conductivity is dependent on the charge state of the surrounding trap states [107]. Hydrogen incorporation in the bulk will be passivation recipe dependent, and it is quite reasonable that the Fermi level in the dislocation core can be shifted sufficiently to change the impurity band occupancy dramatically, changing the electrical properties of threading dislocations. The resulting change in leakage path from the 2DEG to the carbon-doped GaN layer will in turn dramatically modify dynamic R_{ON} [97]. More work is required to obtain a more accurate physical model for the trap emission, charge transport process, and how the SiN_x affects this process.

5.6 Conclusion

A set of AlGaN/GaN HEMTs with different SiN_x passivation layers have been tested for its impact on the ON-state-induced charge trapping. About 60 % increase of R_{ON} after the ON-state stress has been found in the sample with the stoichiometric Si_3N_4 LPCVD layer, while a small (< 20 %) increase of R_{ON} has been found after the OFF-state stress at room temperature, suggesting the presence of negative charge trapping in the device under test under the ON-state stress. The potential mapping on the devices with sense nodes shows significant drop of potential in the

gate-drain access region during ON-state rather than OFF-state, indicating that the negative charge is distributed within that region. The electroluminescence measurements show agreement with our analysis, and demonstrates that there is potential for misinterpretation of the location of EL emission. EL emission from the drain edge does not necessarily mean that the high field region is located at the drain, in this case it was actually located at the gate edge.

All features of the stress induced charge distributions and the recovery process can be explained using the leaky dielectric model. This includes the difference between substrate bias and ON-state bias recovery, and the presence of two different time constant responses with the same activation energy. The results are consistent with hopping transport in a defect band being the limiting step in determining trap responses, rather than the normally assumed emission to the band edge. Finally, the passivation of GaN HEMTs with Si-rich LPCVD passivation can dramatically suppress this charge trapping after ON-state stress.

CHAPTER 6

DRAIN INJECTED BREAKDOWN IN RF ALGAN/GAN-ON-SIC HEMTS

Breakdown mechanism in 0.25 μm gate length RF AlGaN/GaN-on-SiC iron-doped HEMTs with background carbon is investigated through the drain current injection technique in this chapter. This technique enables to measure the breakdown voltage while avoiding permanent failure during measurements. The results show a 2-stage breakdown combined with EL results in the device. A well self-consistent model has been established to explain the findings with the assistance of TCAD simulation.

Section 6.1 introduces the research background of GaN HEMTs breakdown and Section 6.2 illustrates the device details. In Section 6.3, the experimental results are presented, showing the 2-stage breakdown and EL results found in the device. Section 6.4 shows the 2D-TCAD simulation results with ideal conditions. In Section 6.5, the results are analyzed and a self-consistent model is presented. Finally, Section 6.6 concludes this work.

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6.1 Introduction

The breakdown voltage is a crucial parameter for device reliability. Large bandgap enables GaN to withstand high breakdown fields which makes it suitable for high power applications. However, the high-power RF application is still a vulnerable regime for device breakdown since a high voltage may be reached for instance during switching or with a mismatched load.

Several drain breakdown mechanisms have been suggested taking part in different regions of the device. Meneghesso et al. [68] summarized four types of breakdown mechanisms – vertical breakdown, drain-gate breakdown due to surface/gate issues, source-drain punch-through and impact ionization. Vertical breakdown is usually limited by the maximum breakdown voltage of the bulk GaN buffer and the substrate. An increase in drain current at high drain voltages (and in pinch-off conditions) can be ascribed to punch-through effects [91], i.e., to the flow of source-drain current within the bulk of the GaN layer under the gate. Using a 2D-TCAD simulation it was demonstrated that like other types of field-effect devices AlGaN/GaN single heterojunction devices are vulnerable to short-channel effects and demonstrated the necessity for deep acceptors to be incorporated in the GaN buffer to make it more insulating and confine the carriers in the channel. This is now normally achieved by the use of iron (Fe) or carbon deep acceptors. In another model, Tan et al. [109] explained the surface breakdown model as they attributed the breakdown at high drain voltages to a thermal surface-hopping process, which occurs when a certain power threshold is reached by surface current conduction, however, the current generation of devices shows much-improved surface passivation which suppresses that effect.

Most conventional breakdown measurements involved irreversible damage or degradation to the device until Bahl et al. [110] first reported a current controlled breakdown method and called it drain-current injection technique, which enabled a study of the physics of breakdown in InAlAs/InGaAs HEMTs. In this method, the source is kept grounded, and a constant drain current is injected into the device. The gate voltage is then ramped down to shut the device off leading to a rise of the drain-source voltage. This off-state drain-source voltage in-principle represents an unambiguous definition of three-terminal breakdown voltage. This unique technique gives the advantage of avoiding repetitive scanning and reduced the risk of burnout in unstable and fragile devices. Using this technique Wang et al. [111] suggested that the source injection through the buffer can also induce impact ionization and cause a premature three terminal breakdown in conventional AlGaN/GaN HEMTs.

In this chapter, a new breakdown study using drain current injection and electroluminescence for an Fe doped GaN-on-SiC HEMT with known distribution of unintentionally incorporated carbon is presented. Simultaneous measurements of the drain, source and gate current enable to present direct evidence of high source current injection under OFF-state condition through the buffer (punch-through effect) dominating over gate current. In these devices the breakdown can be divided into two distinct stages with varying gate voltages.2D-TCAD device simulation was used to replicate the uniform current flow measurement scenario, and it is proposed that the two stages can be explained by background carbon density as a function of depth. From the EL measurements, the results show that in the second phase uniform punch-through is suppressed and replaced by a strongly localized breakdown with associated negative resistance requiring significantly lower field than punch-through. This study provides further insights into the range of possible breakdown mechanisms for AlGaN/GaN HEMTs.

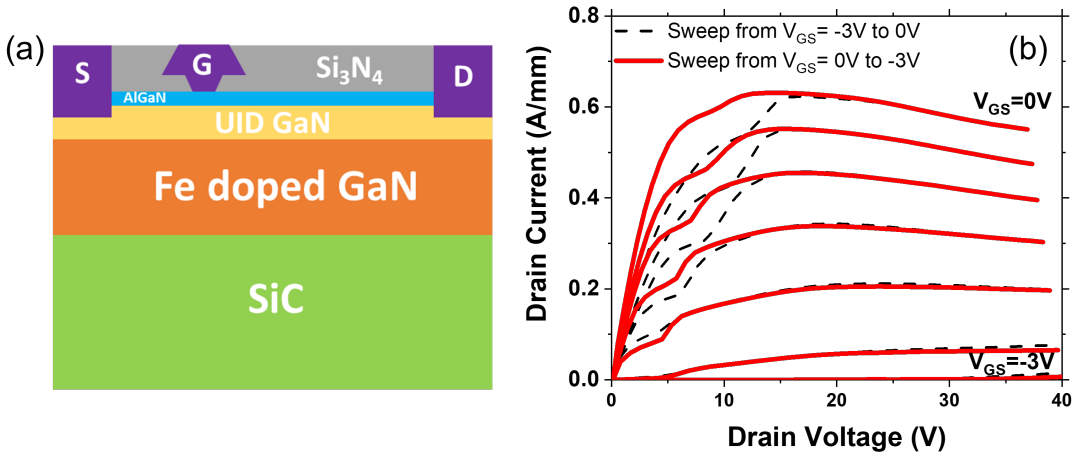

FIGURE 6.1. (a) Schematic of the device under test. (b) DC measurements performed on the device under test. ©2020 IEEE.

6.2 Device under Test

The device under test has a MOCVD grown structure of an AlGaN barrier, a GaN buffer and an AlGaN nucleation layer on an insulating SiC substrate. Fe as a dopant has been used and secondary-ion mass spectroscopy (SIMS) measurements show a conventional Fe doping profile in the GaN bulk with a peak density of 3×10^{18} cm^{-3} which decreases exponentially to 7×10^{15} cm^{-3} at the surface. Carbon is always incorporated unintentionally during MOCVD growth. In this case, SIMS measurements showed that as a result of a change in growth conditions 0.2 μm below the AlGaN barrier, the carbon density was 5×10^{16} cm^{-3} in the 0.2 μm channel layer whereas the deeper bulk of the GaN had a higher carbon density of $3 \pm 1 \times 10^{17}$ cm^{-3} (note that a density of carbon contaminants in the 10^{17} cm^{-3} range has been reported for Fe doped Cree epitaxy [112]). Oxygen and silicon were below the SIMS background of 5×10^{15} cm^{-3}. The device schematic can be seen in Figure 6.1 (a). The device under study has a width of 2×125 μm, a gate length of 0.25 μm, a source-drain spacing of 4 μm, and source-gate spacing of 1 μm. It was fabricated using Ti/Al/Ni/Au and Ni/Au for Ohmic and Schottky contact respectively, and with silicon nitride as a passivation layer. The 2DEG Hall mobility, the 2DEG sheet density and the sheet resistance are 1770 cm^2/(V·s), 1.143×10^{13} cm^{-2} and 340 Ω/sq.

6.3 Experimental Results

DC measurements up to 40 V drain bias with 1 V/sec sweep rate are shown in Figure 6.1 (b) with kink seen at 3-5 V above the knee. A detailed study on the origin of kink in this sample,

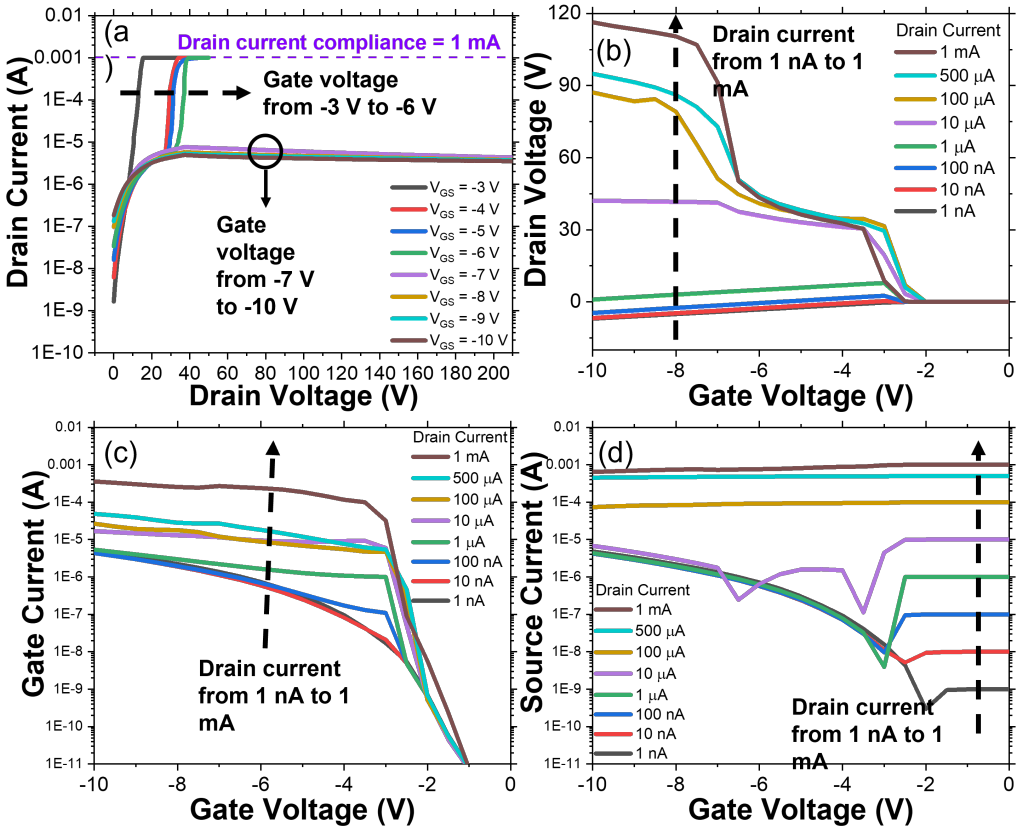

FIGURE 6.2. (a) Shows off-state breakdown measurement results with a drain current compliance 1 mA (V_{GS} is swept from -3 V to -10 V). (b) Shows the measured drain voltage during the drain injected breakdown measurements for a range of I_D bias changing from 1 nA up to 1 mA (V_{GS} is swept from 0 V to -10 V). (c) Shows the measured gate current during the drain injected breakdown measurements for a range of I_D bias changing from 1 nA up to 1 mA (V_{GS} is swept from 0 V to -10 V). (d) Shows the measured source current during the drain injected breakdown measurements for a range of I_D bias changing from 1 nA up to 1 mA (V_{GS} is swept from 0 V to -10 V). ©2020 IEEE.

explained using the p-type floating buffer that results from the presence of the relatively high background carbon level in the bulk, can be found in [113][97] and RF measurements in [71].

Conventional voltage-driven off-state breakdown measurements were performed as shown in Figure 6.2 (a). When the gate-source voltage (V_{GS}) is below threshold and between -3 and -6 V, the breakdown voltage (at the compliance current of 1 mA) increases from -10 to -40 V. For V_{GS} < -6 V, the off-state breakdown voltage increases rapidly to above 210 V. However when measured using the current-driven drain injected breakdown technique, as shown in Figure 6.2 (b), (c) and (d), a complementary and somewhat different behavior is observed. A fixed predefined current is injected into the drain, V_{GS} is ramped down from 0 V to below the threshold, and the

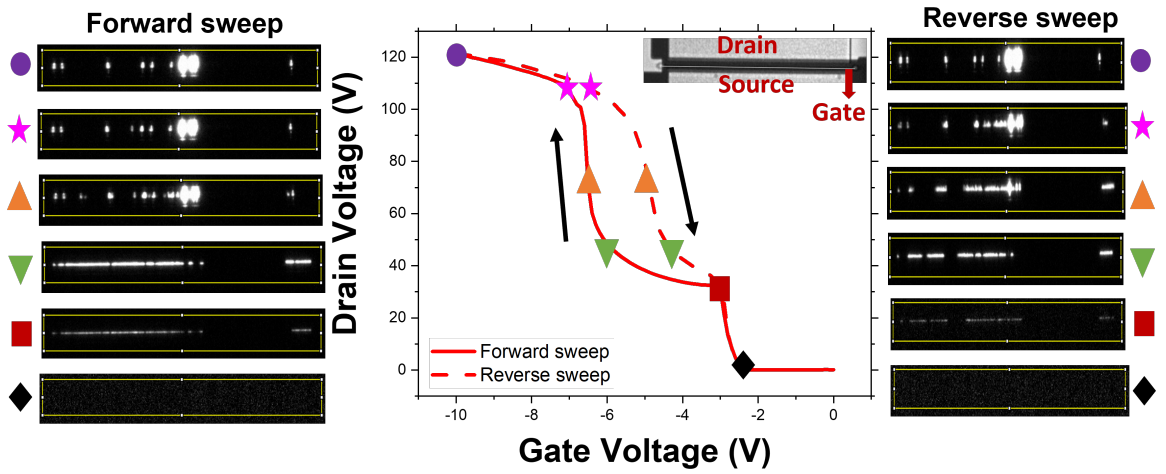

FIGURE 6.3. Measured EL intensity for range of V_{GS} bias between 0 V and -10 V (I_D = 1 mA) with forward and reverse sweeps. ©2020 IEEE.

drain voltage, gate current (I_G) and source current (I_S) are monitored. Figure 6.2 (b) shows the measured V_{DS} for different I_D starting from 1 nA and all the way up till 1 mA. At low drain current ($I_D \leqslant \mu$A), the drain voltage appears to be almost negligible with the current supplied from the gate leakage, and there is no breakdown. At higher drain current which exceeds the gate leakage ($I_D \geqslant 100$ μA), the results show there are two distinct stages of drain breakdown. The first stage appears below the threshold when V_{GS} = -2.5 V with V_{DS} in the range 30 - 40 V, with the 2nd stage when V_{GS} < -7 V associated with a rapid increase in V_{DS} to 90 - 120 V. It is noted that this is significantly lower than that observed with the voltage-driven measurement where the breakdown voltage was > 210V. To clearly identify the leakage/breakdown paths, in Figure 6.2 (c) and (d) the gate and source currents are plotted as V_{GS} is swept from 0 V to -10 V. For I_D < 100 μA, the gate-to-source leakage current is significant and is much larger than the drain injected current as V_{GS} swept to -10 V. For $I_D \geqslant 100$ μA, the drain-to-source current dominates, although the gate current starts to contribute to the drain injected current for more negative V_{GS} (nevertheless drain-source dominates with $[I_G/I_D]_{max}$ < 35% and $[I_S/I_D]_{min}$ > 65%).

To help understand the breakdown mechanism, electroluminescence microscopy was carried out with a 50× objective and Opticstar charge-coupled device (CCD) camera under bias conditions. EL emission measured is shown in Figure 6.3 for I_D of 1mA, together with the points on the V_{DS}-V_{GS} curve at which the EL was measured. Although there is significant hysteresis between forward and reverse sweeps, they show basically similar EL results. In Figure 6.3, at the first stage of the breakdown (-6 V $\leqslant V_{GS} \leqslant$ -3 V), the EL is observed reasonably uniformly across the width of the gate finger. However, at the second stage when V_{GS} < -6 V, the EL emission splits into several localized bright spots which appear in the middle of the gate finger in the reported

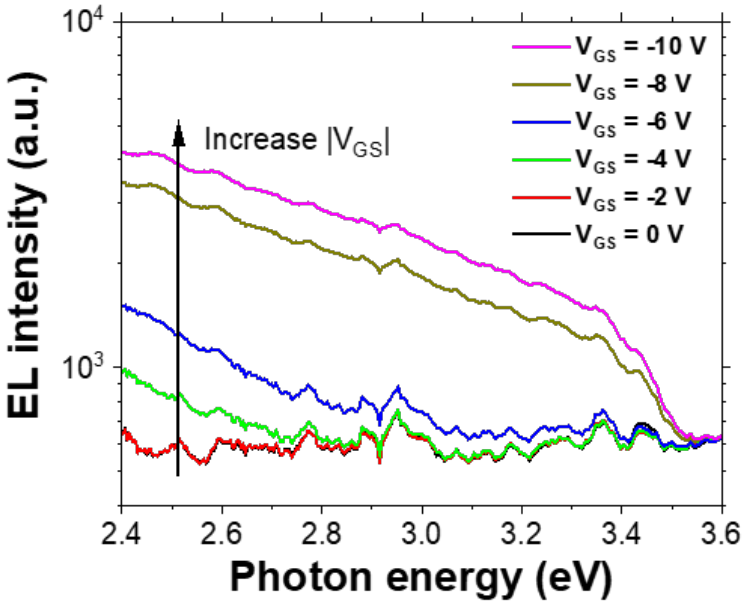

FIGURE 6.4. EL spectra measured from the backside of the device at different gate bias (I_D = 500 μA). ©2020 IEEE.

device, and are associated with locations where there was no EL emission during the first stage. The second stage was accompanied by a strong reduction in uniform emission across the width of the gate, and this suppression was not simply due to the change of the image contrast but was a real reduction of the EL emission. This suppression, and the associated increase in breakdown voltage, means that this stage is not just the result of the onset of localized gate leakage. This measurement has been repeated across several devices on two different processed wafers with the same epitaxy design, and similar behavior was observed and was repeatable.

EL spectra were recorded with a broad-spectrum fibre coupled to a compact spectrometer (Maya 2000–Ocean optics QEPro) sensitive in the range 200–1100 nm and measured across different bias points shown here in Figure 6.4. To access light emitted under the gate, the EL spectra measurements were performed from the back site of the device through the transparent GaN layer and SiC substrate. No significant EL signal was observed till V_{GS} = -4 V and beyond that broad EL distributions can be found between the photon energy of 2.4 to 3.6 eV. Correction of interference fringes due to the multi-layer buffer/substrate has not been applied to Figure 6.4, so the data was not used for quantitative analysis of the electron temperature [32].

The temperature dependence of the gate leakage current has been measured in order to determine the gate leakage mechanism during the breakdown measurements, and the results are shown in Figure 6.5. Two conditions (V_{GS} = -4 V, V_{DS} = 30 V; V_{GS} = -10 V, V_{DS} = 60 V) have been used corresponding to the two measured stages in Figure 6.2 (b). Both cases show an increase

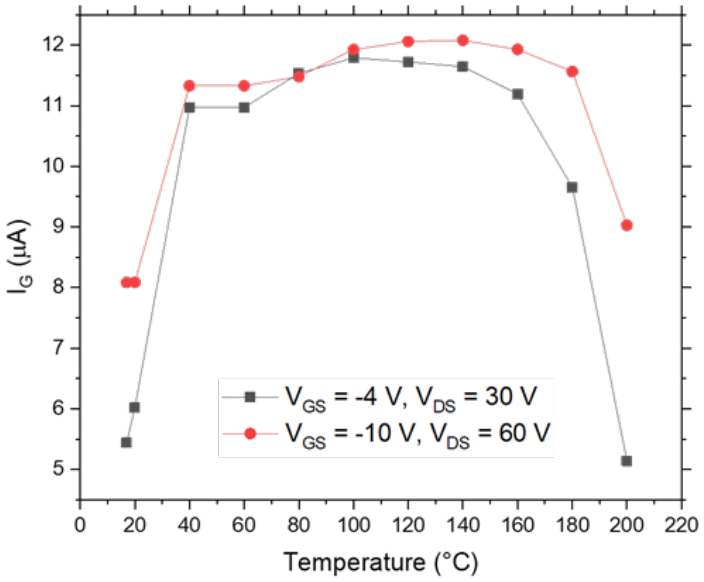

FIGURE 6.5. Temperature-dependent gate leakage current (17 – 200 °C) with two measurement conditions (Stage 1: V_{GS} = -4 V, V_{DS} = 30 V, Stage 2: V_{GS} = -10 V, V_{DS} = 60 V).

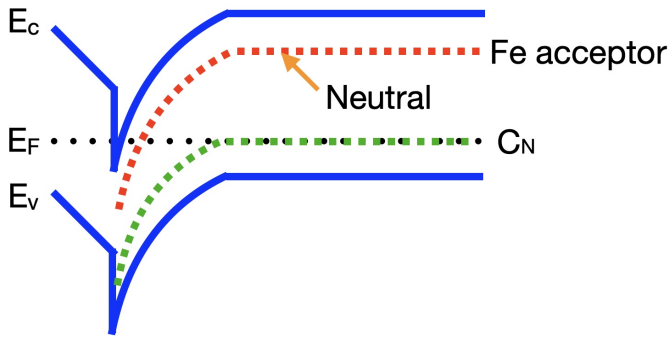

FIGURE 6.6. Band diagram of the simulated GaN epi-layers showing the location of Fe acceptors and C deep acceptors (C_N).

of gate leakage current with temperature from 17 to 40 °C, and then show a decrease of gate leakage current with temperature from 140 to 200 °C.

6.4 Simulation

2D-TCAD simulation using Silvaco Atlas has been implemented to help to interpret our measurement results. The simulated device is represented by a broadly similar structure which consists

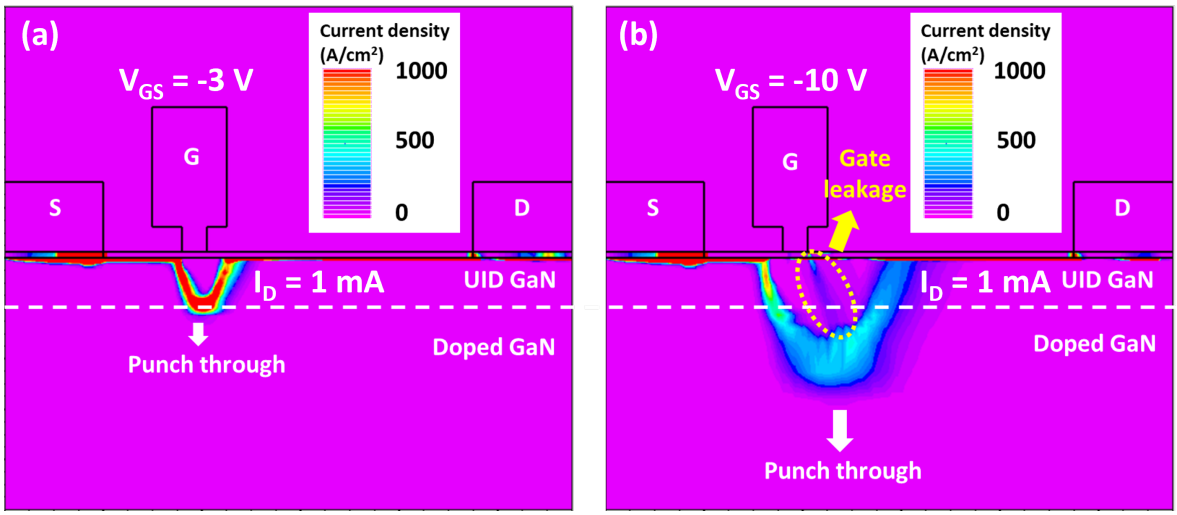

FIGURE 6.7. Simulated current density distribution (a) When V_{GS} = -3 V and I_D = 1 mA, the 2DEG under the gate is fully pinched-off and the remaining electrons within the UID GaN provide a path for the punch-through current. (b) When V_{GS} = -10 V and I_D = 1 mA, the punch-through path has been pushed down to the heavily doped GaN layer. ©2020 IEEE.

of a 22-nm AlGaN barrier, a 0.2-μm UID GaN channel layer, a 1.6-μm doped GaN layer, and a 2-μm SiC substrate. The doping density profile matches the measured SIMS profiles of Fe and C [113]. The Fe acceptor (Ec-0.7 eV) has been doped with the density of 7×10^{15} cm^{-3} on the GaN surface and it increases exponentially with depth to 3×10^{18} cm^{-3} at 1.1 μm below the GaN surface and then keeps constant. The C atoms in GaN can be deep acceptors (C_N), shallow donors (C_{Ga}), complexes, and there can also be intrinsic donors. The UID GaN is doped with 3×10^{16} cm^{-3} carbon deep acceptor (C_N, Ev+0.9 eV) and 2×10^{16} cm^{-3} shallow donors (C_{Ga} and intrinsic donors, Ec-0.03 eV). The doped GaN is doped with 2×10^{17} cm^{-3} C deep acceptor (C_N, Ev+0.9 eV) and 1×10^{17} cm^{-3} shallow donors (C_{Ga} and intrinsic donors, Ec-0.03 eV) giving a compensation ratio of 0.5. This doping profile will finally result in a p-type buffer as the Fermi level is pinned at about Ev+0.97 eV with the Fe neutral except near the surface, as shown in Figure 6.6 [97]. Band-to-band leakage paths have been added under the source and drain contacts by adding heavily doped p-type shorts, which allows hole flow from the contact to the buffer [18]. The impact ionization model is enabled in this simulation. Figure 6.7 (a) and (b) shows the simulated current density profiles with I_D = 1 mA and V_{GS} = -3 and -10 V respectively. In Figure 6.7 (a), the 2DEG under the gate is just fully depleted, and a punch-through current path can be found within the UID GaN. In Figure 6.7 (b), when V_{GS} = -10 V, the trace of punch-through current is pushed down further into the p-type doped GaN layer. In this simulation, the high electric field near the gate edge in Figure 6.7 (b) leads to impact ionization which generates free holes and the hole current to the gate which is labelled as “gate leakage”. However, in the real device, the gate

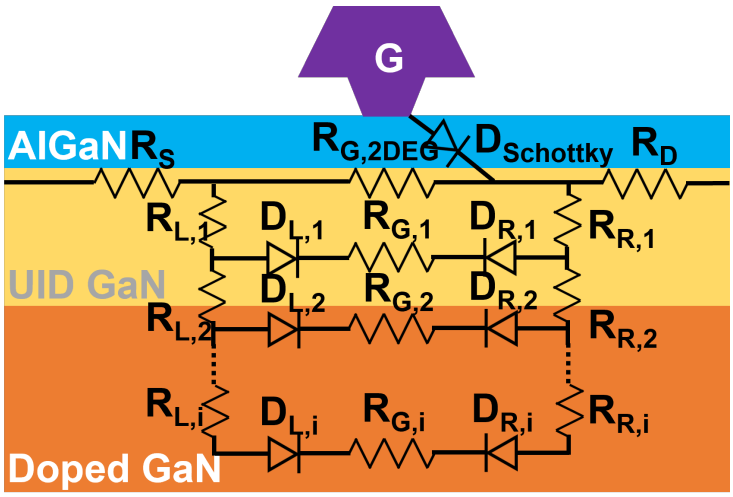

FIGURE 6.8. Shows the equivalent circuit under the gate. The resistances of the resistors in parallel ($R_{G,2DEG}$, $R_{G,1}$, $R_{G,2}$,..., $R_{G,i}$) under the gate are dependent on the gate voltage. As the gate voltage is swept to negative, these resistors ($R_{G,2DEG}$, $R_{G,1}$, $R_{G,2}$,..., $R_{G,i}$) will become less conductive from the top to bottom. The diodes ($D_{L,i}$, $D_{R,i}$) represents the condition for the electron current when a pinched-off gate voltage is applied. ©2020 IEEE.

leakage mechanism can be defect-related, and the impact ionization is not be the primary reason for the gate leakage.

6.5 Discussion

The primary questions here to answer are, why do devices with this epitaxial design show the unusual and interesting feature of a two-stage breakdown, and why is the breakdown voltage in the second stage different for voltage and current-driven measurements. To help understand this phenomenon, an equivalent circuit of the device is plotted in Figure 6.8, where the channel is represented by resistors (R_S, $R_{G,2DEG}$, R_D) in series, and the gate is represented by a Schottky diode ($D_{Schottky}$) under reverse bias. The highly resistive buffer is connected by diodes and resistors in parallel, and the left diodes ($D_{L,i}$) are under reverse bias and the right diodes ($D_{R,i}$) are under forward bias with a pinched-off gate voltage. However, for the GaN buffer, the barrier on the left side of the gate ($D_{L,i}$) for electron flow can be lowered (as gate voltage becomes less effective in the deep GaN buffer) as a result of back-gating by the drain field. This would result in a punch-through minority carrier electron current flowing through $R_{G,i}$ to the drain [91].

The first drain voltage stage is observed below the threshold voltage once the 2DEG channel at the AlGaN/GaN interface has been depleted by the gate. That means, in the equivalent circuit, $R_{G,2DEG}$ is highly resistive and it requires the punch-through electron current flowing through $D_{L,1}$, $R_{G,1}$ and $D_{R,1}$. It finally leads to a high drain voltage plateau. The simulation in Figure 6.7

(a) shows the same process. The EL plots in Figure 6.3 indicate that the punch-through current is flowing reasonably uniformly across the entire width of the gate.

As the gate voltage is swept to beyond -6 V, a second drain voltage plateau can be found. Guided by the simulation in Figure 6.7 (b), it is proposed that during the 2^{nd} stage the UID GaN channel layer has been depleted completely by the gate and as a result the punch-through current path has been pushed down further into the more heavily doped GaN layer. In the epitaxy used here, the C concentration is higher than that in the channel UID GaN guaranteeing that the doped GaN layer is p-type. Note that the Fe doping is also more heavily doped, but it is neutral and therefore has relatively little effect on the transport, as illustrated in Figure 6.6. Meanwhile, the junction between the UID GaN and the doped GaN serves as a potential barrier for the current flowing through it. The higher doping and Fermi-level pinning in the lower half of the gap increases the barrier for punch-through, and lowers electron lifetime, providing a plausible explanation for an abrupt increase of drain voltage during the 2^{nd} stage required to force a current-driven punch-through current to flow through $D_{L,i}$, $R_{G,i}$, $D_{R,i}$.

The EL results show a key difference between the stages. In the second stage, the EL distributed across the gate width is suppressed as bright spots appear somewhere near the gate finger. For these locations with the bright spots, a plausible explanation is that these are associated with defect regions which will only conduct when the electric field is high enough. Once these preferential leakage paths are formed locally, they show strong conductivity, and sustain the majority of the injected source-drain current, while the resulting voltage drop across the rest of the gate width is still not sufficient to allow punch-through. Therefore, the regions without localized leakage do not show EL emission during the 2^{nd} stage. This new breakdown mechanism is highly localized and it is worth reiterating that the bright spots found in the second stage correspond to the dark spots in the first stage, consistent with a defect origin. Therefore, the simulation result in Figure 6.7 (b) only shows the ideal case without the localized leakage paths. The fact that the measured off-state voltage-driven breakdown voltages are larger than that of the drain injected measurements during the 2^{nd} stage in Figure 6.2 suggest the presence of a snap-back or negative-resistance mechanism associated with the localized transport through the more heavily carbon-doped layer. Koller et al. [114] have reported negative resistance and a localized breakdown mechanism in carbon-doped bulk GaN structures, with associated localized EL light emission. Some of their localized breakdowns were pinned to dislocations, although here the precise nature of the defects is unknown. The forward and reverse sweeps shown in Figure 6.3 confirm that the process is reversible and does not lead to a permanent device failure. The strong hysteresis observed in the transition between uniform conduction in stage 1 and localized conduction in stage 2 is also consistent with the presence of negative resistance region. There may also be negative charge trapping in the buffer. Negative charges due to ionized carbon deep acceptors (C^N) can accumulate under the high drain bias and back-gate the channel and reduce the carrier density in the UID GaN leading to hysteresis [18].

The broad emission spectra in Figure 6.4 suggest that the EL emission in both stages primarily originates from Bremsstrahlung radiation as hot electrons lose their energy when deflected by charged particles rather than band-to-band emission [32]. Hence, the presence of EL emission indicates where the high electrical fields and current densities are simultaneously present [115][116] but does not necessarily indicate strong impact ionization. The increase in gate leakage seen as the injected drain current and drain current increase is presumably associated with the presence of impact ionization. However since the majority of drain current flows to the source, it is reasonable that a mechanism is occurring which does not rely on impact ionization as is suggested here.

To investigate the gate leakage mechanism during the breakdown measurements, the temperature-dependent measurements of stage 1 and 2 have been conducted as shown in Figure 6.5. S. Arulkumaran et al. [117] have studies how to distinguish the impact ionization and the temperature assisted tunneling mechanism . It is convinced that a negative temperature dependence of the gate leakage current is more likely related to the impact ionization while a positive temperature dependence of gate leakage is usually associated with defects. Figure 6.5 suggests that in the room temperature, the impact ionization is not the dominant gate leakage current mechanism as the impact ionization rate has a negative coefficient with temperature. Considering that the gate leakage is in the microamp range in the devices, it is most likely to be related to defects (i.e. surface hopping or trap-assisted tunnelling). More efforts should be made for further study of the origin of gate leakage.

6.6 Conclusion

In this chapter, the conventional voltage-driven and the drain-current injection technique have been compared to investigate how the breakdown mechanism evolves under different bias conditions in a Fe-doped AlGaN/GaN-on-SiC HEMT with moderately high lower-buffer carbon concentration. It is shown that the measurement approaches are complementary and together deliver additional insight. Initially, when the device is pinched-off, the punch-through mechanism dominates the process. However, as the channel is fully depleted, the punch-through path will be forced down into the heavily doped and Fermi-level pinned p-type GaN buffer, and the drain voltage reaches a higher plateau. At this stage, the EL results reveal a new breakdown mechanism where the localized current associated with pre-existing defects becomes dominant while the punch-through current flow in the rest of the device is not significant due to the high potential barrier between the GaN layers. This study helps to understand the relationship between the breakdown mechanism, the punch-through effect and the buffer conditions in RF GaN HEMTs.

CHAPTER 7

INVESTIGATION OF GATE LEAKAGE AND ELECTROLUMINESCENCE IN POWER MIS-ALGAN/GAN-ON-SI HEMTS

The gate leakage is a main reliability issue for GaN HEMTs and how to mitigate it has been a major target for research. The electroluminescence technique is often adopted for the reliability analysis as it can "see" leakage currents. In this study, gate leakage current and electroluminescence have been measured simultaneously and analysed in power MIS-AlGaN/GaN HEMTs. A potential competition mechanism between EL and the impact ionization effect has been proposed in order to explain the results. The wafers used in this chapter are same as that in Chapter 4 and 5, provided by Nexperia.

The structure of this chapter is as follows. Section 7.1 introduces the research background of the gate leakage and EL in GaN HEMTs and Section 7.2 shows the devices under test. In Section 7.3, the experimental results are presented, showing the bell-shape curves of the gate leakage and EL in the sample with a Si-rich insulating layer and the peak shift of two curves. In Section 7.4, the physical model is constructed revealing the origin of bell shape curves of I_G and EL. Finally, Section 7.5 concludes this work.

7.1 Introduction

The gate leakage can be suppressed by a dielectric layer such as SiN_x and Al_2O_3 under the gate. The gate mechanism with a small drain bias has been investigated [118, 119], and has attributed to Poole–Frenkel emission, Fowler–Nordheim tunneling and trap-assisted tunneling to the gate leakage under the positive gate bias in GaN MIS-HEMTs. Dutta et al. [120] showed a comprehensive study on SiN_x/GaN cap/AlGaN/GaN MIS-HEMTs, and suggested that the defect-assisted tunneling and Poole–Frenkel emission are the main reasons for the gate leakage under

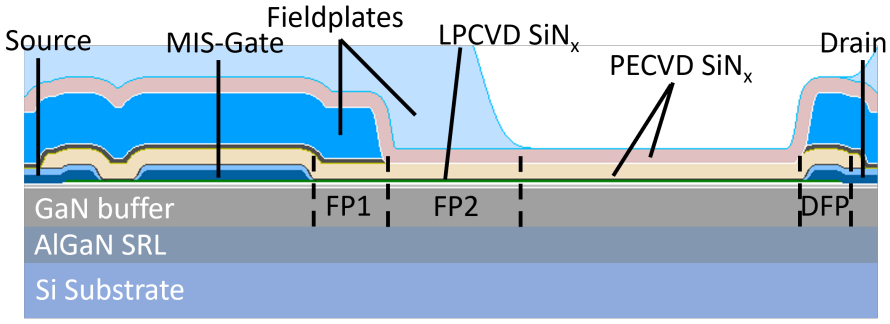

FIGURE 7.1. Schematic of MIS-GaN HEMTs used in this chapter (not to scale). GFP is the gate connected field plate, and FP1 and FP2 are two source field plates.

the negative gate bias.

Electroluminescence measurements have been considered as a powerful tool for analysing power GaN HEMTs [73]. However, few reports have been made for the analysis of the interaction between the EL and gate leakage in GaN MIS-HEMTs. Bisi et al. [115] reported the finding of a bell-shape gate leakage against V_{GS} under a high drain voltage in N-Polar GaN MIS-HEMTs and they associated it with the impact ionization effect. They also found an alignment between the bell-shape curves between the gate leakage and the EL and claimed that the EL was due to the band-to-band recombination followed by the impact ionization. In this study, a comprehensive story of the gate leakage and the EL in Ga-Polar GaN MIS-HEMTs is presented and shows a potential competition mechanism between them.

7.2 Device under Test

The devices under test are MIS-AlGaN/GaN HEMTs fabricated on 150-mm diameter GaN-on-Si wafers, as shown in Figure 7.1. The structure of MIS-HEMTs used in this chapter are same with these in Chapter 4 and 5, except the gate. The gate has a metal-insulator-semiconductor (MIS) structure which has a 70 nm LPCVD SiN_x sited between the gate metal and the GaN cap. The device parameters are as follows, L_{SG} = 2.5 μm, L_G = 3 μm, L_{GD} = 12.4 μm and W_G = 100 μm.

7.3 Experimental Results

Measurements of DC-I_DV_G plots in MIS-HEMTs of wafer A, B and D are shown in Figure 7.2. Three samples show similar ON-state drain current level, and an increase of OFF-state leakage from wafer A to D. The V_{th} is ranging from -10 V to -15 V for different conditions. The negative shift of V_{th} with the increase of V_{DS} is the consequence of the drain-induced-barrier-lowering. The variation of V_{th} between different wafers is is likely due to the small changes during the manufacturing process.

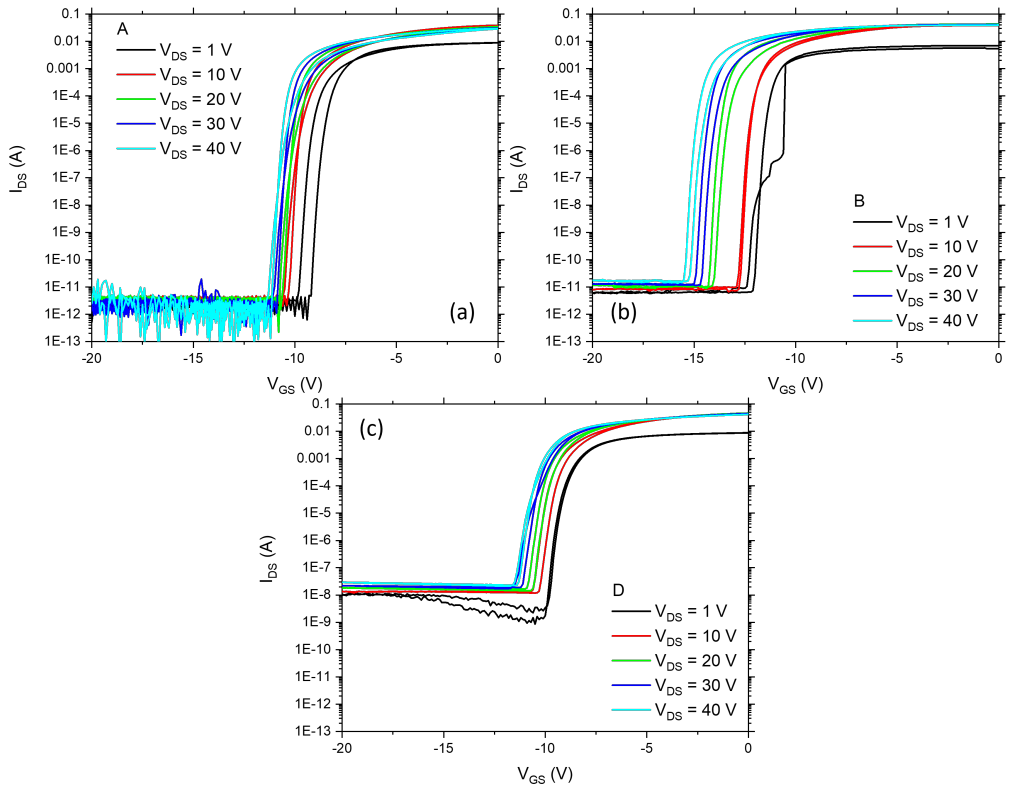

FIGURE 7.2. Measured drain current (I_{DS}) against gate voltage (V_{GS}) in MIS-HEMTs. (a) Wafer A. (b) Wafer B. (c) Wafer D.

Figure 7.3 shows the measured gate leakage current in for three samples. Wafer A has a relatively low value of gate leakage current and the measurement only shows noise around 1-10 pA. Both of Wafer B and C show the monotonic increase of gate leakage as V_{GS} moving towards negative for low drain bias ($V_{DS} \leqslant 10$ V). For higher drain bias, the ON-state gate leakages of wafer B and C show bell-shape curves. The OFF-state gate leakage levels in three samples match with that of $I_D V_G$ measurements.

The electroluminescence measurements on the MIS-HEMTs of 3 samples are conducted as shown in Figure 7.4. Wafer A and B do not show any EL light emission for V_{DS} up to 40 V. The EL of wafer D show a bell shape curve with a peak intensity when V_{GS} = -6 V and V_{DS} = 40 V. The EL light is mainly distributed near the drain edge and the two sides of the device. As discussed in Chapter 5, the EL light is reflected by the field plates and leaks out at the regions where there are not field plates shielding.

To investigate the relationship between the electroluminescence and gate leakage, simultaneous measurements of them have been carried out in a MIS-HEMT of wafer D, as depicted in Figure 7.5. There is a peak shift of the bell-shape curves between EL and I_G. The peak of EL

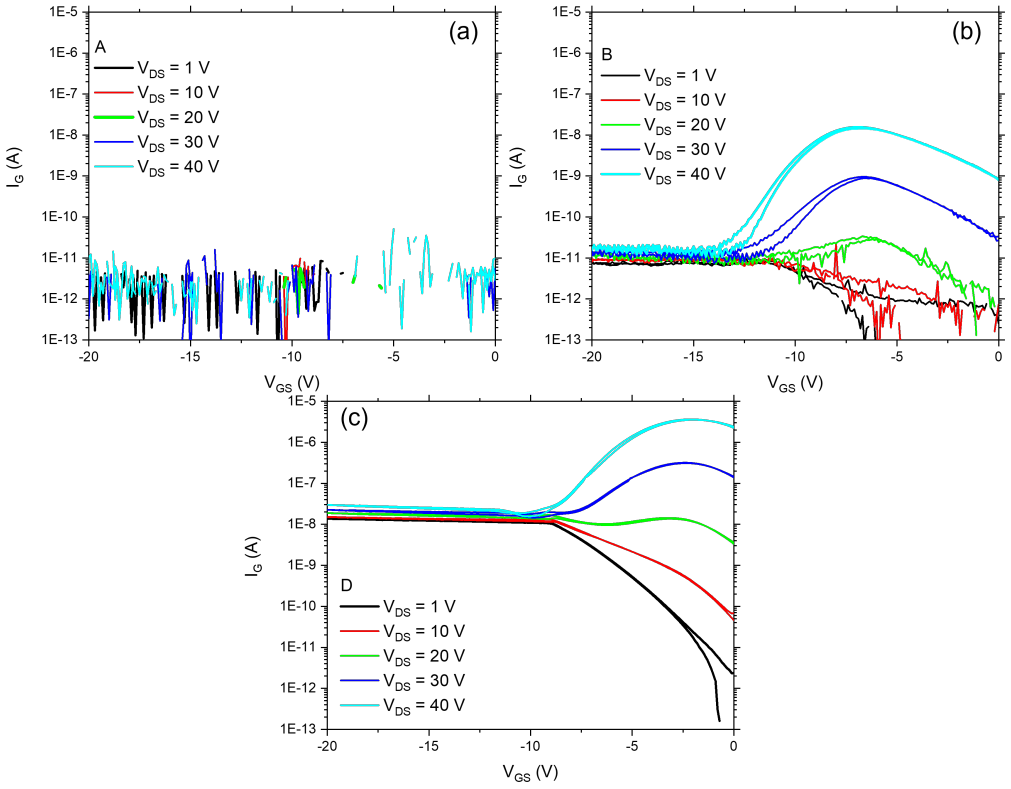

FIGURE 7.3. Measured gate leakage current (I_G) against gate voltage (V_{GS}) in MIS-HEMTs. (a) Wafer A. (b) Wafer B. (c) Wafer D.

curve is around - 6 V whereas that of I_G curve is around -2 V for I_G when V_{DS} = 40 V.

7.4 Discussion

7.4.1 Differences of Wafers

Results show apparent differences between leakages and EL across the wafers and only wafer D shows good results for analysing both phenomena. Firstly, the leakage levels of the 70 nm LPCVD SiN_x layer for each wafer has been measured by the Waller et al. [84] and it suggested that the leakage level has a positive correlation with the Si concentration. It explains why there is an increase of gate leakage from wafer A to D. Secondly, the reason why there is no EL signal detected from wafer A and B can be same as that explained in Chapter 5, as wafer D shows the largest electric field near the gate during ON-state. Based on the results, wafer D is chosen as the main sample for investigating the leakages and EL.

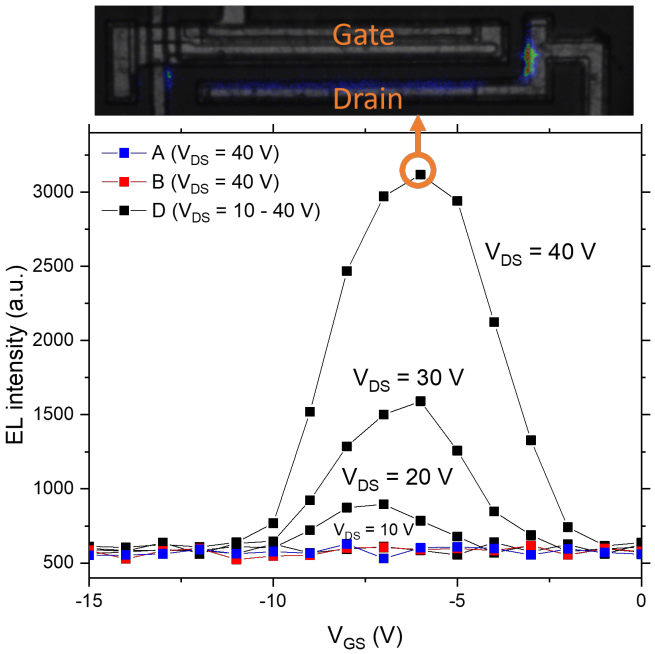

FIGURE 7.4. Measured EL intensity against the V_{GS} in MIS-HEMTs of wafer A, B and D for drain voltage up to 40 V. Only wafer D shows visible EL light and the top image shows the EL distribution for wafer D with a peak EL intensity (V_{GS} = -6 V, V_{DS} = 40 V).

7.4.2 Origin of Gate Leakages and EL

To understand the gate leakages and EL in MIS-HEMTs, the first question to ask is why both of them show the bell shape against V_{GS}. Some studies have been attributed the reason of the EL bell shape to the hot electron density and the electric field [121–123]. On the one hand, the hot electron density under the gate increases with V_{GS} so EL emission is promoted; On the other hand, the gate-drain field decreases with V_{GS}, so the hot electrons gain less energy within this range and the EL intensity drops. The reason of bell-shape curve for gate leakage is different from EL which is primarily due to the impact ionization effect.

Figure 7.6 shows the mechanism of the impact ionization effect and Bremsstrahlung effect. When an electron travels in the region with a high electric field near the gate edge, there are possibilities that the electron loses its energy by the lattice scattering, the impact ionization effect (Figure 7.6 (b)) and Bremsstrahlung effect (Figure 7.6 (c)). The impact ionization will generate holes which finally flow towards the gate. Figure 7.7 shows the band diagram under the MIS-gate. There are two paths for the gate leakage, the electron current and the hole current. According to [124, 125], there is no hole barrier for the n-type GaN and Si_3N_4. Considering that the measurement results of the gate leakages in the study [120] showed similar feature of the electron leakage current due to Poole–Frenkel emission as in Figure 7.3 (c), here it is assumed

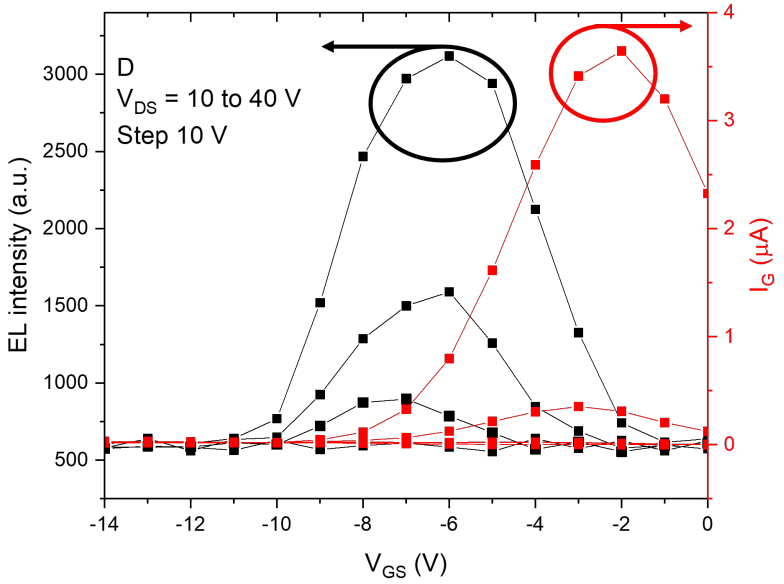

FIGURE 7.5. Simultaneous measurements of EL and gate leakage current (I_G) in MIS-HEMT of wafer D.

that the electron current follows the same mechanism. Based on the analysis above, it is easier for the hole current path for the semi-ON condition.

Under the semi-ON condition, With a low drain voltage (V_{DS} = 1 V), there is no impact ionization as lateral electric field is also low so the gate leakage mostly depends on the electron current path. When the drain voltage increases, the impact ionization effect becomes significant and the hole current dominates. The bell shape of I_G can be explained by the impact ionization rate and the band structure. The impact ionization rate relies on the hot electron density and the electric field which are affected by V_{GS} in the same way similar to the EL. V_{GS} also determines the band diagram of SiN_x. As V_{GS} moves to positive, the valence band of SiN_x drops and finally results in a barrier for the hole current path. It explains the bell shape of I_G against V_{GS}.

Figures 7.1 and 7.3 show that the OFF-state leakage keep constant when V_{GS} moves to negative. It is because of that the additional vertical potential increase beyond the V_{th} will fully drop on the GaN buffer and the substrate instead of the gate structure (SiN_x, the GaN cap and the AlGaN barrier). Therefore, the potential barriers for the electron current remain the same and the OFF-state electron leakage current does not change with V_{GS}, while the hole current is negligible during OFF-state.

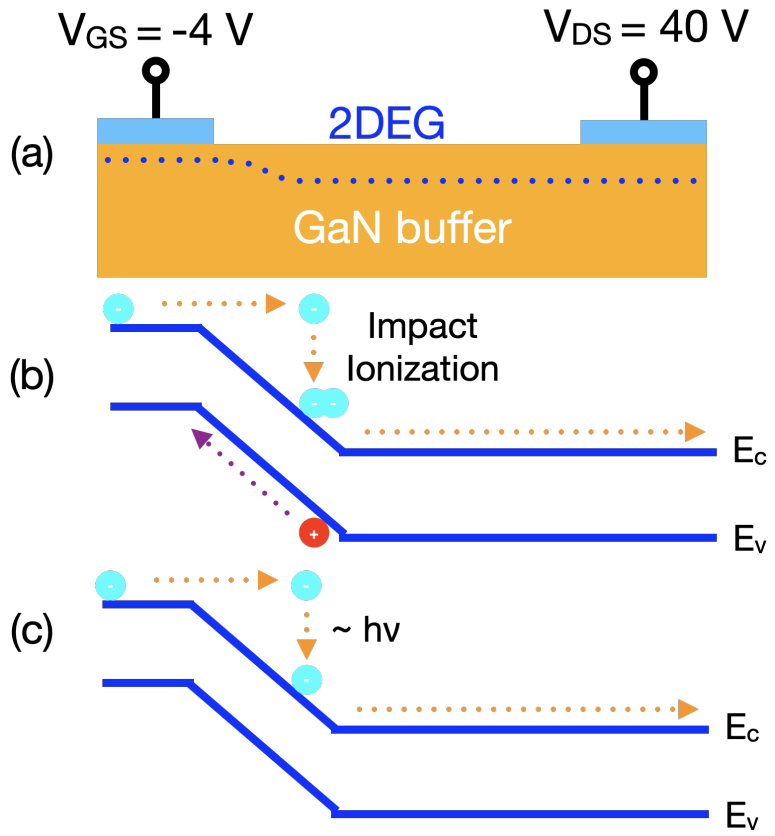

FIGURE 7.6. (a) Schematic of MIS-HEMT of wafer D and the 2DEG density profile when V_{DS} = 40 V and V_{GS} = -4 V. (b) Band diagram along the 2DEG and the impact ionization mechanism. (c) Band diagram along the 2DEG and the EL emission.

7.4.3 Competition Mechanism

The key story in this chapter is to explain the shift of the two bell-shape curves, EL and I_G. As shown in Figure 7.8, the measured EL, I_G, I_{DS} and the potential drop between the gate and drain are plotted in the same figure for analysis. As already stated earlier, the data are all collected from a single measurement for consistency. Based on the mechanism in Figure 7.6, the electron should require an additional energy equals to the 3.4 eV (GaN bandgap) to trigger the impact ionization, while it needs less energy for photon emission (less than GaN bandgap [32]). It implies that the hole gate leakage requires a higher gate-drain field than the EL based on the analysis above. However, the measurements tell a different story here so the electric field may not be the major reason to determine the peak position of two bell-shape curves.

A plausible explanation for the peak shift is the competition mechanism. The hot electron can lose its energy due to multiple mechanisms (scattering, impact ionization, EL) and the total energy that one electron is available to obtain is same. The rapid increase of I_{DS} with V_{GS} implies a fast increase of the electron density under the gate in the semi-ON range. As the

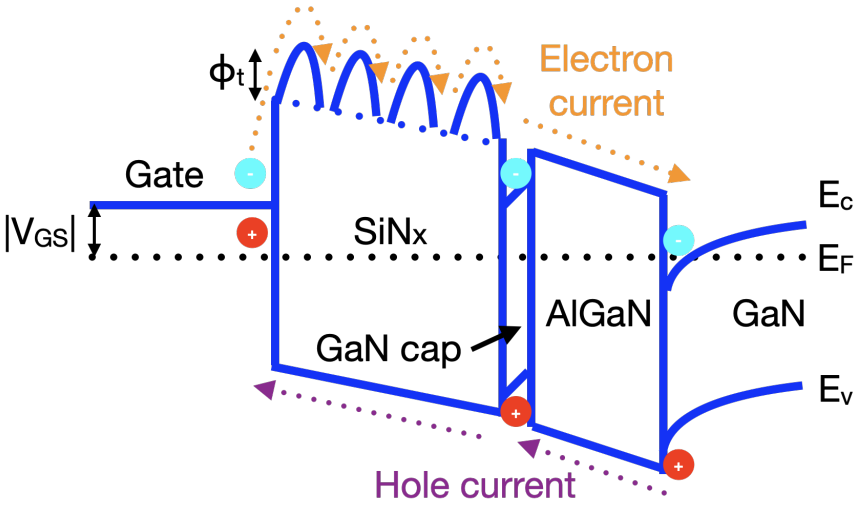

FIGURE 7.7. Band diagram under the MIS-gate with the electron and hole leakage current under the semi-ON condition. Electrons can pass the SiN_x layer by Poole–Frenkel emission with the aid of traps (trap energy level ϕ_t).

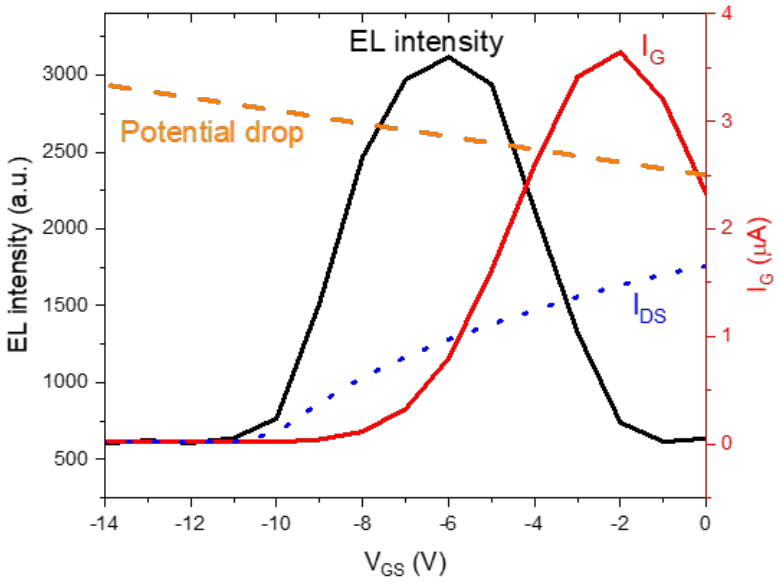

FIGURE 7.8. Measured EL, gate leakage current (I_G), drain current (I_{DS}) and the potential drop between gate and drain in MIS-HEMT of wafer D. The y-axis is linear scale for I_{DS} and the potential drop (not show here).

electron density increases, the impact ionization rate increases exponentially and it consumes more amount of energy from the hot electrons than the Bremsstrahlung effect. Therefore the EL

becomes weaker as V_{GS} approaching 0 V. It gives a new insight of the formation of bell-shape curves and the different peak positions.

7.5 Conclusion

In this chapter, the physical mechanism of gate leakage current and electroluminescence has been investigated with a GaN MIS-HEMT structure with a LPCVD SiN_x layer under the gate metal. Both of them show bell-shape curves against V_{GS}, however, with different peak position on the sample with the Si-rich LPCVD SiN_x. The analysis of the electron and hole leakage paths has been made to explain the bell-shape curve of I_G. A competition mechanism has been proposed to explain the feature of peak shift of I_G and EL curves. This study gives a new insight of the gate leakage and EL and how they are affected by each other.

CHAPTER 8

CONCLUSIONS

The market share of GaN devices has growing in a fast pace within the semiconductor industry, thanks to the high breakdown field (3 MV/cm [5]) of GaN material and the high 2DEG electron mobility (up to 2000 $cm^2V^{-1}s^{-1}$ [4]) of the AlGaN/GaN heterojunction. In particular, AlGaN/GaN HEMTs exhibit excellent performance in power and RF applications, such as radar, 5G and automotive. In the mean time, a lot of reliability issues have been reported during the scientific research and the industrial practice. Therefore, a large amount of effort has been made to solve problems and pursue improvements on the device performance. For example, the incorporation of carbon into the GaN buffer has been designed to increase the vertical breakdown field; The source field plates are used for the purpose of smoothing the electric field peak near the edge of the gate; The SiN_x passivation layer is deposited as it significantly suppress the surface trapping. None of these powerful design can be made without the deep understanding behind the corresponding reliability issues.

The motivation of this work is to further improving the understanding of the reliability issues appeared in AlGaN/GaN HEMTs that are crucial for the industrial applications. The research covers topics of hard-switching, trapping effect, breakdown, and gate leakage for on either power or RF transistors. With the aid of electrical, thermal and optical characterization methods and TCAD simulations, extensive analysis has been made in order to reveal the physical picture behind these reliability issues, which provides an insight into the device optimization.

8.1 Conclusions of the Work

This work starts from the study of hard-switching in power AlGaN/GaN-on-Si HEMTs which is mainly presented in Chapter 4. The switching-mode power supply, which is a type of electric

converter to ramp up/down the voltage or switch between AC and DC. The transistor inside SMPS controls the circuit with a pulse waveform and experiences the hard-switching periodically. In this study, the hard-switching characterization with a time control resolution of nano second range has been carrier out. The measurement results of the dynamic R_{ON} after OFF-state pulse stress on a set of wafer with different stoichiometries LPCVD SiN_x passivation suggest that the dynamic R_{ON} has been suppressed by the Si-rich LPCVD passivation (wafer D), which is likely due to the vertical dislocation paths within the GaN layer induced by the SiN_x defects. The Si-rich sample shows around more than 40% increase of dynamic R_{ON} after hard-switching compared to soft-switching for 200 V operation, however, it recovers after 1 μs which suggests a possible shallow trap on the surface. The self-heating effect can result in a dramatic increase of channel temperature during hard-switching, but the GaN channel cools down soon within a few hundreds of micro seconds according to the simulation. The simulation with hot electrons being scattered to the surface and neutralizing the ionized donors within AlGaN has visualized the charge trapping distribution, and it is highly associated with lateral electric fields. This study provides two ideas of reducing the dynamic R_{ON} after hard-switching. One is to adopt the Si-rich LPCVD SiN_x passivation, and the other is to smooth the peak electric field near the gate (i.e. use a slant source field plate [126]).

The story follows by a more comprehensive study on the analysis of ON-state and OFF-state stress on the same set of wafers in Chapter 5. Waller et al. [83] have reported that the wafer A with a stoichiometric Si_3N_4 passivation layer suffers from current collapse after high OFF-state stress (V_{DS} = 100 V) due to the buffer trap. In this study, measurements with a moderate drain bias condition (V_{DS} = 40 V) show around 60% dynamic R_{ON} increase after the ON-state stress compared to the OFF-state stress. The lateral potential mapping assisted by the sense node structures unambiguously show a reduced gate-drain potential during the ON-state stress (wafer D shows the smallest reduction), while all the electric field drops near the gate edge during the OFF-state stress. By comparing the charge trapping information of the substrate stress with the ON-state stress, a conclusion can be drawn that the ON-state stress condition leads to GaN buffer charge trappings related to carbon acceptors. These charges mainly localized under the gate edge and also distributed along the gate-drain access region. This study gives a picture of charge trapping mechanism for different types of stress, especially for the ON-state stress, and a Si-rich LPCVD SiN_x passivation can also suppress this effect. The electroluminescence measurements were performed to investigate the relationship between the electroluminescence and the potential distribution. However, unlike the previous reports [73, 127], the EL measurements on wafer D shows that EL emissions comes from the drain edge and the two sides of devices. It implies that the source field plates, which cover the gate and a part of gate-drain spacing, blocked the EL emission and EL light only leaked out at the region with no field plates. This finding suggests that care needs to be taken when interpreting the location of EL emission.

The breakdown voltage is a vital parameter for the reliability of GaN HEMTs for the high

power RF application, as the device may experience a high voltage during the RF switching or an overload. Conventional breakdown measurements by sweeping IV curves until the breakdown can sometimes bring a permanent device degradation to the device. Therefore, the drain-current injection technique is used in Chapter 6 for determining the breakdown voltages while avoiding the device failure. By sourcing a constant drain current and sweeping the gate voltage beyond the threshold voltage (V_{GS} = -2.5 V), the breakdown voltage is recorded as a function of the gate voltage. The results turns out that there are unambiguously two-stage breakdown regions. During the first stage (-6 V $\leqslant V_{GS} \leqslant$ -3 V, V_{BD} is around 30 V), the 2DEG is just depleted and the current conduction path is pushed down within the UID GaN layer where there are a few free electron carriers left. If the gate voltage went further negative (-10 V $\leqslant V_{GS} \leqslant$ -7 V, V_{BD} > 100 V), the depletion region extended to the doped GaN layer (doped with 3×10^{18} cm^{-3} Fe and $3 \pm 1 \times 10^{17}$ cm^{-3} C), the punch-through current path also penetrated through the doped GaN layer, where there has a relatively higher resistivity. As the drain current is kept as a constant throughout the measurement, a higher drain voltage is required for achieving the punch-through. It explains the finding of the two-stage breakdown in RF AlGaN/GaN HEMTs. Moreover, the electroluminescence measurements show a evenly distributed EL emission along the gate finger during the first stage while some bright light spots can be found while the evenly distributed EL faded away at the second stage. Note that these bright spots just correspond to the dark spots at the first stage. It provides a straightforward evidence that additional leakage paths have been triggered under a high drain bias during the second stage and they are relative more conductive to sustain a part of the current. Therefore, the other part of the current is suppressed and the EL distribution changes. This phenomena is also know as the negative resistance region as some conducting paths formed near the breakdown voltages [58]. This study shows that the incorporation of carbon dopants in GaN successfully increases the breakdown voltage, however, with the unintentionally n-type GaN channel layer, the low breakdown voltage is inevitable for the first stage. The study also suggests that the additional leakage paths may lead to a temporary negative resistance region which reduce the breakdown voltage, which are likely associated with the dislocations in GaN. Hence, care should be paid for fabrication device with less dislocations.

The gate leakage is another important parameter for the device reliability, with a low gate leakage the device can achieve low power loss for applications. The high-κ gate is therefore fabricated for the purpose of mitigating the gate leakages. In Chapter 7, the AlGaN/GaN HEMTs with a MIS gate structure are used for investigating the gate leakage mechanism. The MIS gate is incorporated with LPCVD SiN_x layer of which the stoichiometries are same as the devices used for Chapter 4 and 5. The gate leakage levels increases with the Si concentration of the SiN_x layer. However, the sample with the LPCVD Si-rich passivation also shows a relatively low ON-resistance after stress. Hence, there is a trade-off between the low ON-resistance and the low gate leakage in MIS GaN HEMTs with different SiN_x layer. ON the sample with a Si-rich SiN_x layer, the gate leakage increases as the gate voltage goes to negative and finally saturates

around the threshold voltage with a low drain bias (V_{DS} = 1 V). On the contrary, the gate leakage against the gate voltage shows a bell-shape curve for semi-ON state with a relatively drain bias (V_{DS} = 40 V). It suggests that there are two components of gate leakage current as the electron current and the hole current contribute to the electron current and hole current independently. The electrons mainly pass through the SiN_x barrier by the Poole–Frenkel emission whereas the hole current comes from the impact ionization. The electroluminescence measurement on the sample with a Si-rich SiN_x layer also shows shows a bell-shape curve against the gate voltage. However, the peak of EL curve is around - 6 V whereas that of I_G curve is around -2 V for I_G when V_{DS} = 40 V. It implies the presence of a competition mechanism that the impact ionization is the dominant mechanism to consume the hot electron energy with a more positive gate voltage, and the it suppresses the Bremsstrahlung effect and leads to a reduction in EL. This study shows the physical mechanism for the gate leakage in MIS GaN HEMTs and finds a potential competition mechanism between the gate leakage and the EL.

8.2 Future work

The dynamic R_{ON} increase after hard-switching has proven to be associated with the hot electrons. The hot electrons are likely trapped on the surface as it shows a fast recovery behaviour. However, with the Auriga 4850 system, it is hard to control the pulse switching delay in nano second range while improve the current resolution and increase the time range for the recovery measurement. A more sensible equipment can help to improve the measurements quality and give a better results for analysing the surface trapping behaviour. Moreover, the simulation for the hot electron used the simplified Hansch model, some improvements regarding the physical equations and the parameters can be made for better simulations in the future.

The study of charge trapping under the ON-state and OFF-state stress has shown significant buffer charge trapping under the ON-state for the device with Si_3N_4 LPCVD layer (wafer A) while the OFF-state induce less charge trapping. It implies that the hot electrons may also induce the buffer charge trapping as well as the surface charge trapping analysed in Chapter 4. The results are not contradictory to each other as the buffer trapping does not exist in the wafer D for the hard-switching study. However, it still raise the question about how the hot electrons can result in both surface and buffer charge trapping in GaN HEMTs. More study regarding this topic is an important direction for the future study.

The breakdown study shows a two-stage breakdown feature due to the differences in the carbon doping densities of UID and doped GaN layers. The research also shows EL pattern suggesting additional leakage paths are triggered during the second stage. However, it is still unknown what the physical presence behind the leakage path, i.e., where it is and how is it affected by the high drain voltage. Future work is still required to give a physical insight into the origin of the leakage path.

Chapter 7 discussed the origin of the gate leakage and electroluminescence in MIS GaN HEMTs and the possible competition mechanism. The electron and hole current for the gate leakage current can be quantitative analysed with a comprehensive physical model to calculate them in details. Meanwhile, there are apparently several mechanisms, involving the Bremsstrahlung effect, the impact ionization effect and the scattering mechanism which take effect simultaneously. A more comprehensive model to quantify each mechanism will be a part of the future work.

APPENDIX A

RESEARCH OUTPUT

A.1 Publications

- **F. Yang**, S. Dalcanale, M. Gajda, S. Karboyan, M. J. Uren, and M. Kuball, "The Impact of Hot Electrons and Self-Heating During Hard-Switching in AlGaN/GaN HEMTs", IEEE Trans. Electron Devices, vol. 67, no. 3, pp. 869-874, Mar. 2020, doi: 10.1109/TED.2020.2968212.

- **F. Yang**, M. J. Uren, M. Gajda, S. Dalcanale, S. Karboyan, J. W. Pomeroy, and M. Kuball, "Suppression of charge trapping in ON-state operation of AlGaN/GaN HEMTs by Si-rich passivation", Semiconductor Science and Technology, vol. 36, no. 9, p.095024, Aug. 2021, doi: 10.1088/1361-6641/ac16c3.

- **F. Yang**, M. Singh, M. J. Uren, T. Martin, H. Hirshy, M. A. Casbon, P. J. Tasker, and M. Kuball, "Study of Drain Injected Breakdown Mechanisms in AlGaN/GaN-on-SiC HEMTs", IEEE Trans. Electron Devices, vol. 69, no. 2, p.525-530, Jan. 2022, doi: 10.1109/TED.2021.3138841.

- T. Gerrer, J. W. Pomeroy, **F. Yang**, D. Francis, J. Carroll, B. Loran, L. Witkowski, M. Yarborough, M. J. Uren, and M. Kuball, "Thermal Design Rules of AlGaN/GaN-Based Microwave Transistors on Diamond", IEEE Trans. Electron Devices, vol. 68, no. 4, pp. 1530-1536, Apr. 2021, doi: 10.1109/TED.2021.3061319.

- Y. Cao, J. W. Pomeroy, M. J. Uren, **F. Yang**, and M. Kuball, "Electric field mapping of wide-bandgap semiconductor devices at a submicrometre resolution", Nat. Electron., vol. 4, no. 7, pp. 478–485, Jun. 2021, doi: 10.1038/s41928-021-00599-5.

A.2 Conference talks

- **F. Yang**, S. Dalcanale, M. Gajda, S. Pandey, S. Karboyan, M. J. Uren, M. Kuball, "The impact of hot electrons and self-heating during hard-switching in AlGaN/GaN HEMTs", UK Nitrides Consortium Winter Meeting 2019, Glasgow, UK
- **F. Yang**, S. Dalcanale, M. Gajda, S. Karboyan, M. J. Uren, M. Kuball, "The impact of hot electrons and self-heating during hard-switching in AlGaN/GaN HEMTs", Workshop on Compound Semiconductor Devices and Integrated Circuits 2019, Glasgow, UK
- **F. Yang**, M. Singh, M. J. Uren, H. Hirshy, P. J. Tasker, T. Martin, M. J. Uren, M. Kuball, "Study of drain injected breakdown mechanisms in AlGaN/GaN-on-SiC HEMTs", UK Nitrides Consortium Winter Meeting 2020, Cabourg, France
- M. J. Uren, S. Dalcanale, **F. Yang**, A. Nejim, S. P. Wilson, M. Kuball, "Simulation of leakage induced suppression of bulk dynamic R_{ON} in power switching GaN-on-Si HEMTs", International Conference on Compound Semiconductor Manufacturing Technology 2020, Tucson, US

APPENDIX B

LIST OF ABBREVIATIONS

2DEG	2-Dimensional Electron Gas
CCD	Charge-Coupled Device
CVD	Chemical Vapour Deposition
DC	Direct Current
DCS	DiChloroSilane
DGD	Drain-to-Gate Delay
DLTS	Deep-Level Transient Spectroscopy
EL	ElectroLuminescence
FP	Field Plate
GIT	Gate Injection Transistor
GPIB	General Purpose Interface Bus
GW	Gate Wing
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
LAN	Local Area Network
LPCVD	Low Pressure Chemical Vapour Deposition
MBE	Molecular Beam Epitaxy
MIS	Metal-Insulator-Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal Organic Chemical Vapour Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PAE	Power Added Efficiency
PECVD	Plasma Enhanced Chemical Vapour Deposition
PID	Proportional-Integral-Derivative

RF	Radio Frequency
SIMS	Secondary-Ion Mass Spectroscopy
SMPS	Switch-Mode Power Supply
SMU	Source Measurement Unit
SRL	Strain Relief Layers
TCAD	Technology Computer-Aided Design
TLM	Transfer Length Method
TSB	Test Script Builder
UID	UnIntentionally Doped

APPENDIX C

SILVACO ATLAS SIMULATION CODE

This appendix contains Silvaco Atlas simulation codes used in Chapter 4. The simulation codes consists of 3 parts, the design file with the definition of the device structure and mesh, the body file with the assignation of material properties and physical models, and the run file with the commands to execute the simulation. In particular, the design file should be compiled from the ".de" file to the ".str" file in Devedit for future simulation. The body file consists of the Hansch model and the hot electron model to simulate the additional surface charges. The run file only shows the simulation with DGD = 130 ns.

Design File

```
File Name: Nexperia_HEMT.de

DevEdit version=2.8.26.R # file written Sun Sep 26 2021 15:18:01 GMT+1 (BST)

work.area x1=0 y1=-0.7 x2=27 y2=5
# devedit 2.8.26.R (Tue Jan 26 05:23:40 PST 2016)
# libMeshBuild 1.24.23 (Tue Jan 26 05:22:55 PST 2016)
# libSSS 2.8.14 (Tue Jan 19 16:38:10 PST 2016)
# libSVC_Misc 1.28.13 (Tue Jan 19 16:37:06 PST 2016)
# libsflm 7.10.1 (Tue May 19 19:52:32 PDT 2015)
# libSDB 1.12.36 (Wed Jan 13 04:01:54 PST 2016)
# libGeometry 1.30.16 (Tue May 19 19:51:51 PDT 2015)
# libCardDeck 1.32.22 (Fri Jan 22 18:42:45 PST 2016)
# libDW_Set 1.28.13 (Tue Jan 19 16:36:26 PST 2016)
# libSvcFile 1.14.19 (Tue May 19 19:51:56 PDT 2015)
# libsstl 1.10.11 (Tue May 19 19:51:57 PDT 2015)
# libDW_Misc 1.40.20 (Tue Jan 19 16:14:10 PST 2016)
# libQSilCore 1.2.8 (Wed May 13 18:39:12 PDT 2015)
# libDW_crypt 3.0.0 (Mon May 18 04:43:00 PDT 2015)
# libDW_Version 3.8.0 (Fri Oct  3 16:08:41 PDT 2014)
region reg=1 mat=Si3N4 color=0xffff pattern=0x3 \
polygon="12.5,-0.69 12.5,-0.7 20.2,-0.7 20.2,-0.09 21.2,-0.09 21.2,-0.02" \
"7.8,-0.02 7.8,-0.09 9.5,-0.09 9.5,-0.39 6.1,-0.39 6.1,-0.09 6.8,-0.09" \
"6.8,-0.02 3.3,-0.02 3.3,-0.09 4.3,-0.09 4.3,-0.7 10,-0.7 10,-0.45 11,-0.45" \
"11,-0.7 11.5,-0.7 11.5,-0.69"
#
constr.mesh region=1 default

region reg=2 mat=AlGaN \
polygon="3.3,-0.02 6.8,-0.02 7.8,-0.02 21.2,-0.02 21.2,0 3.3,0"
#
constr.mesh region=2 default max.height=0.005 max.width=1

region reg=3 mat=GaN \
polygon="27,0 27,1 0,1 0,0 3.3,0 21.2,0"
#
constr.mesh region=3 default max.height=0.1 max.width=1
```

```
region reg=4 mat=AlGaN color=0xff8282 pattern=0x4 \
polygon="27,1 27,5 0,5 0,1"
#
constr.mesh region=4 default

region reg=5 name=source mat=Contact elec.id=3 work.func=0 \
    color=0xffc8c8 pattern=0xd \
polygon="0,0 0,-0.7 4.3,-0.7 4.3,-0.09 3.3,-0.09 3.3,-0.02 3.3,0" \
polygon="10,-0.45 10,-0.7 11,-0.7 11,-0.45" \
polygon="11.5,-0.69 11.5,-0.7 12.5,-0.7 12.5,-0.69"
#
constr.mesh region=5 default max.height=0.1 max.width=0.3

region reg=6 name=gate mat=Contact elec.id=1 work.func=0 \
    color=0xffc8c8 pattern=0xd \
polygon="6.8,-0.02 6.8,-0.09 6.1,-0.09 6.1,-0.39 9.5,-0.39" \
"9.5,-0.09 7.8,-0.09 7.8,-0.02"
#
constr.mesh region=6 default max.height=0.05 max.width=0.2

region reg=7 name=drain mat=Contact elec.id=2 work.func=0 \
    color=0xffc8c8 pattern=0xd \
polygon="21.2,0 21.2,-0.02 21.2,-0.09 20.2,-0.09 20.2,-0.7 27,-0.7 27,0"
#
constr.mesh region=7 default max.height=0.1 max.width=0.1


# Set Meshing Parameters
#
base.mesh height=10 width=10
#
bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001 line.straightening=1 \
    align.points when=automatic
#
imp.refine min.spacing=0.02
#
constr.mesh max.angle=90 max.ratio=300 max.height=0.2 \
```

```
max.width=2 min.height=0.0001 min.width=0.0001
#
constr.mesh type=Semiconductor default
#
constr.mesh type=Insulator default
#
constr.mesh type=Metal default
#
constr.mesh type=Other default
#
constr.mesh region=1 default
#
constr.mesh region=2 default max.height=0.005 max.width=1
#
constr.mesh region=3 default max.height=0.1 max.width=1
#
constr.mesh region=4 default
#
constr.mesh region=5 default max.height=0.1 max.width=0.3
#
constr.mesh region=6 default max.height=0.05 max.width=0.2
#
constr.mesh region=7 default max.height=0.1 max.width=0.1
Mesh Mode=TensorProduct
refine mode=x x1=4.56 y1=-0.848 x2=5.68 y2=5.227
refine mode=x x1=4.45 y1=-0.806 x2=6 y2=5.163
refine mode=x x1=13.16 y1=-0.834 x2=19.94 y2=5.319
refine mode=x x1=9.77 y1=-0.834 x2=19.98 y2=1.486
refine mode=x x1=9.61 y1=-0.784 x2=20.15 y2=1.189
refine mode=y x1=-0.34 y1=-0.162 x2=27.32 y2=-0.056
refine mode=y x1=-0.2 y1=0.022 x2=27.19 y2=0.1
refine mode=y x1=-0.14 y1=0.913 x2=27.1 y2=1.21
refine mode=y x1=-0.34 y1=0.012 x2=27.19 y2=0.082
refine mode=y x1=-0.21 y1=0.004 x2=27.13 y2=0.042
refine mode=y x1=-0.23 y1=0.272 x2=27.57 y2=0.353
refine mode=y x1=-0.32 y1=0.292 x2=27.33 y2=0.327
refine mode=y x1=-0.25 y1=0.953 x2=27.22 y2=0.976
refine mode=y x1=-0.32 y1=-0.075 x2=27.28 y2=-0.031
```

```
refine mode=x x1=7.54 y1=-0.388 x2=9.75 y2=0.482


base.mesh height=10 width=10

bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001 line.straightening=1 \
    align.Points when=automatic
```

Body File

File Name: bodytext_hot_electron.in

```
set Qp_AlGaN=3e13
set Qoffset=-1.5e12
set Qp_GaN=2.2e13
set Chi_AlGaN=3.8
set phib=1.4

mesh infile=Nexperia_HEMT.str width=1000

region modify number=2 material=AlGaN x.comp=0.25
region modify number=4 material=AlGaN x.comp=0.6

electrode name=substrate bottom

doping donor conc=1e15 region=3

doping donor conc=3e18 gaussian characteristic=0.001 \
y.min=0.3 y.max=1

trap acceptor density=1e19 degen.fac=2 \
  e.level=0.9 \
sign=1e-15 sigp=1e-15 \
y.min=0.3 y.max=1

models fermi bgn srh print temp=300 ni.fermi fldmob

# Hot electron model
model hei devdeg.e ig.eb0=1.4
degradation nta=1e13 sigmae=1e-14

mobility region=3 mun=1500  \
betan=2.3 \
tmun=1.5 \
vsatn=1.91e7 \
mup=8 \
tmup=1.5
```

```
# Gate
contact name=gate workfunction=($phib+$Chi_AlGaN)

# GaN buffer/AlGaN interface
interface charge=($Qp_AlGaN - $Qp_GaN) s.s. y.min=0.0 y.max=0.0

# AlGaN top surface charge
interface charge=$Qoffset s.s. \
y.min=-(0.02+0.001) y.max=-(0.02-0.001)

material region=2 affinity=3.8 PERMITTI = 10.7
material region=3 affinity=4.31 PERMITTI = 10.4
material region=4 affinity=3.2 PERMITTI = 10.7

method newton autonr maxtraps=10 itlimit=30 carriers=2 ^tauto trap

# Init
output band.param con.band val.band charge polar.charge qss devdeg hei
```

Run File

```
File Name:  run_hot_electron.in

go atlas simflags="-P 8"

source bodytext_hot_electron.in

method newton autonr maxtraps=10 itlimit=30 carriers=2 ^tauto trap

solve init
save outfile=Nexperia_HEMT_init.str

#Drain bias
log outfile=Nexperia_HEMT_Vg0Vd150.log master
solve vdrain=0.001
solve vdrain=0.01
solve vdrain=0.1 vstep=0.1 vstop=1 name=drain
solve vdrain=1.2 vstep=0.2 vstop=5 name=drain
solve vdrain=5.5 vstep=0.5 vstop=150 name=drain
save outfile=Nexperia_HEMT_Vg0Vd150.str master

#Gate bias
log outfile=Nexperia_HEMT_Vg-5Vd150.log master
solve vgate=-0.001
solve vgate=-0.01
solve vgate=-0.1 vstep=-0.1 vstop=-5 name=gate
save outfile=Nexperia_HEMT_Vg-5Vd150.str master

#Reload model
load infile=Nexperia_HEMT_Vg-5Vd150.str master
solve vgate=-5 vdrain=150

log outfile=HE_DGD130_Vg-5Vd150.log master
solve vgate=0 dt=1e-9 tstop=100e-9 ramptime=100e-9
solve dt=1e-9 tstop=145e-9
save outfile=HE_DGD130_Vg-5Vd150_v1.str master
solve vdrain=1 dt=5e-11 tstop=215e-9 ramptime=70e-9
save outfile=HE_DGD130_Vg-5Vd150_v2.str master
```

```
solve dt=2e-9 tstop=1200e-9
save outfile=HE_DGD130_Vg-5Vd150_v3.str master

log off
quit
```

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