



Zhou, W., Dlab, M., & Yuan, X. (2022). Impact of Parasitic and Load Current on the Attenuation of Motor Terminal Overvoltage in SiC-Based Drives. *IEEE Transactions on Industry Applications*, 58(2), 2229-2241. <https://doi.org/10.1109/TIA.2022.3141703>

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Impact of Parasitic and Load Current on the Attenuation of Motor Terminal Overvoltage in SiC-Based Drives

Wenzhi Zhou, *Student Member, IEEE*, Mohamed Diab, *Senior Member, IEEE*, and Xibo Yuan, *Senior Member, IEEE*

Abstract—In SiC-based adjustable speed drives, the high voltage slew rate (dv/dt) of the switching transitions results in excessive overvoltage at the motor terminals due to the reflected voltages across the drive power cables. Besides the cable length, the switching rise/fall times of the voltage pulses are a key parameter to quantify the motor overvoltage in PWM inverter-fed drives. These times are varying depending on the load current and parasitic elements of SiC MOSFETs, that is, a standard two-level converter typically results in a non-uniform overvoltage envelop at the motor terminals. This article analyses the switching mechanism of the two-level converter considering the impact of SiC parasitic elements and load current showing how they affect the motor overvoltage in cable-fed drives. The analysis is then extended to the mitigation of the motor overvoltage using quasi-three-level (Q3L) modulation as a candidate filter-less approach with a T-type converter. The theoretical analysis is validated through experimental tests by using the Q3L T-type converter. The analysis and results show that the instantaneous load current value critically determines the peak motor overvoltage, while it allows either a full or partial overvoltage mitigation when the Q3L modulation is adopted.

Index Terms— High dv/dt , cable-fed motor drives, overvoltage, parasitic, quasi-three-level PWM, reflected wave phenomenon, SiC MOSFET, T-type converter.

I. INTRODUCTION

THE emergence of wide bandgap (WBG) power semiconductor devices, such as silicon carbide (SiC) MOSFETs, has led to rapid and transformative advances in power electronics [1]. Promoted by the WBG material characteristics, such as wider bandgap, higher breakdown field, and elevated thermal conductivity, SiC MOSFETs can operate at higher switching speeds and operating temperatures than silicon (Si) IGBTs [2]. With these characteristic enhancements, the SiC MOSFET has become a promising device choice in power converters supplying electric motors in drives applications such as automotive, railway, and aerospace [3].

Although the fast-switching speed of SiC devices has clear

potential to reduce the switching loss and increase the switching frequency, it raises several undesired issues and technical challenges for both the inverters and motors [3]-[6]. Among them, the motor overvoltage oscillations, due to the reflected wave phenomenon (RWP), is one of the serious challenges that can cause premature failure of the motor winding insulation [3], [6]. The RWP is caused by high dv/dt voltage pulses travelling through power cables terminated by a motor that has significantly higher characteristic impedance than that of cables [7]. The resultant overvoltage depends on cable length and the rise/fall time of the inverter switching voltage [8], as depicted in Fig. 1, which shows how the motor overvoltage varies with the cable length under various switching speeds. Since the switching rise time of Si IGBTs is typically between 150-250ns, the motor overvoltage is usually observed in Si inverter-fed drives when the feeding cable is longer than 45 m [9]. Referring to Fig. 1, as the rise time decreases, the motor overvoltage increases at the same cable length. Also, the critical cable length, at which the motor experiences voltage doubling, decreases as the rise time is reduced [8]. Thus, the motor overvoltage is more common when fast switching (usually between 25-50 ns) SiC MOSFETs are used in inverter-fed drives where the motor voltage can be doubled with shorter cable lengths (e.g., a few meters) compared to those used in equivalently rated Si-IGBT-based counterparts [8]-[10]. The consequent overvoltage induces undesired stress on the motor winding insulation, increasing the possibility of partial discharge while degrading the motor reliability and lifetime.

Existing research investigates the RWP using the widely accepted double pulse test (DPT) based on a SiC half-bridge circuit, solely focusing on the rising transition of the output waveform [10], [11]. However, the motor is usually driven by either single-phase or three-phase inverters, that is, the continuous output voltage waveform is different to that of the DPT circuit, being synthesized by the interaction of two/three phase-legs rather than only a single phase-leg. Thus, the DPT

This Manuscript received December 29, 2020; revised June 7, 2021, and September 25, 2021; accepted January 1, 2022. Paper 2020-IPCC-1677.R2, presented at the 2020 IEEE Energy Conversion Congress and Exposition, Detroit, MI, USA, 11-15 Oct. 2020, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. This work was supported in part by the UK EPSRC under grant EP/S00081X/1. (Corresponding author: Xibo Yuan.)

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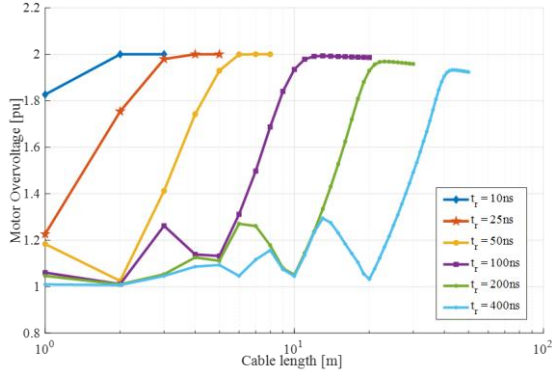


Fig. 1. Motor voltage at various cable lengths and rise/fall times (The rated motor voltage is selected as the base value for calculating the per unit value of the motor peak voltage.).

may not sufficiently reveal how motor drives operation is affected under RWP. Fig. 2 shows experimental results of the RWP in a SiC single-phase motor drive system supplied from a 300 V dc-link through a 5 m cable where the motor voltage V_m (green signal) unexpectedly has a non-uniform peak voltage envelop within the fundamental cycle. Since the peak motor overvoltage ultimately depends on the rise/fall time of the switched voltage pulse, for a given cable length, the rising and falling transitions of each individual SiC device should be examined under different load current conditions to assess the parameters influencing the switching transitions. This allows designing a proper overvoltage mitigation method.

The mainstream approach to mitigate the RWP/overvoltage effect is employing passive filters to suppress the overvoltage either by limiting the slew rate (dv/dt) of the inverter output switching voltage or matching the impedance between the cable and the motor [6], [12]-[14]. Despite their effectiveness, the filters have disadvantages such as increasing the drive system cost and size while inducing additional losses, which counters the benefits of employing SiC MOSFETs [15]. A filter-less mitigation approach is the quasi-three-level (Q3L) PWM technique which breaks the rising and falling transitions of each PWM voltage pulse into two equal steps separated by a proper dwell time such that the second voltage step cancels the reflection of the first voltage step [15]-[18]. Fig. 3 illustrated the overvoltage mitigation mechanism of the Q3L PWM scheme using a bounced diagram. As shown, If the second voltage step V_{s2} propagates synchronously with the reflected wave V_{r1}^- , V_{r1}^+ will be countered by V_{s2} . Compared with the commonly adopted approaches, the Q3L PWM scheme effectively mitigates the overvoltage while reduces the dv/dt of the inverter switching voltage. In [16], the T-type converter has been adopted to generate a Q3L voltage waveform for Si IGBT-based motor drives by temporarily employing the intermediate voltage state in each pole-to-pole voltage transition. This results in a line voltage with transitional employment of half the dc-link voltage at the rising and falling edges. The presented results showed a significant overvoltage mitigation, with 20% motor overvoltage at most. However, with shorter switching times of SiC MOSFETs compared with Si IGBTs, the performance of SiC-based T-type converter under

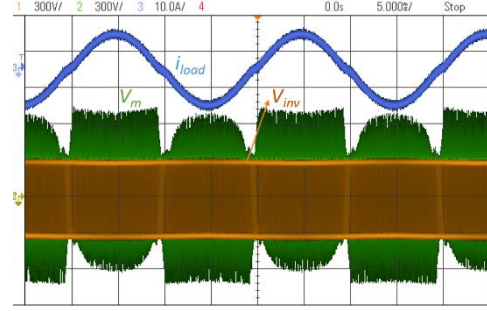


Fig. 2. Experimental result of the RWP in single-phase SiC-based motor drives

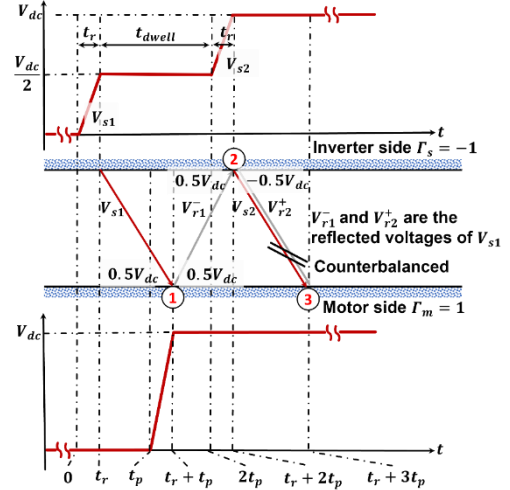


Fig. 3. A bounced diagram of the Q3L PWM scheme.

Q3L modulation needs reinvestigation since the switching device parasitic will have a more pronounced impact on the switching transitions. This can adversely affect the overvoltage mitigation ability of the Q3L T-type converter, resulting in higher motor overvoltage than expected.

This article is based on an earlier conference paper [19] in which the authors addressed the impact of load current and device parasitic on the switching transitions of SiC-based two-level power converters in cable-fed motor drives. This article summarizes the preliminary findings of the conference paper with further discussion, while extends the analysis to the Q3L T-type converter providing detailed reference to its operation, commutation process, and performance in mitigating the RWP in cable-fed drives. The contributions of this article are listed as follows:

- 1) This article has revealed how the load current and device parasitic will affect the motor terminal voltage with SiC motor drives, where it shows the overvoltage reaches its peak when the phase current polarities are different.
- 2) By analysing the commutation process of the Q3L T-type converter considering the impact of device parasitic and load current on the switching transitions, this article has proved that the SiC parasitic may adversely affect the ability of the Q3L T-type converter to fully mitigate the voltage reflections in certain cases, due to the consequent variation in the switching rise/fall times depending on the load current

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polarity and magnitude.

3) This article has proved that by using a fixed dwell time, overall, the Q3L T-type converter can successfully attenuate the motor overvoltage due to the inherent time-varying nature of switching transitions. However, when the polarities of the phase currents are the same and under light load conditions, only a partial overvoltage mitigation can be achieved due to the effect of parasitic capacitances.

The rest of this article is structured as follows. Section II describes the impact of load current and SiC parasitic elements on the switching transitions of standard two-level converters in cable-fed motor drives. Section III presents the Q3L PWM technique and its implementation strategy based on a T-type converter. Section IV analyses the switching commutation mechanism of SiC-based T-type converter considering the effect of load current and device parasitic capacitance. Experimental results are provided in Section V to validate the theoretical analysis. Finally, section VI draws the article conclusions.

II. MODELLING OF SWITCHING TRANSITIONS IN TWO-LEVEL CONVERTERS

A typical SiC-based motor drive system consists of a dc-voltage source supplying a PWM inverter which feeds a motor through power cables, as demonstrated in Fig. 4. Similar to travelling waves in transmission lines, the inverter PWM voltage pulses propagate back and forth between the cable and the motor due to the impedance mismatch between them, resulting in overvoltage oscillations at the motor terminals [12].

In SiC-based motor drives, the rise/fall time of the inverter switched voltage is one of the critical parameters affecting the RWP when the cable length is fixed. This section analyses how the motor currents along with the parasitic capacitance of SiC MOSFETs affect the switching transitions of the inverter's output voltage. The analysis is conducted for a half-bridge circuit, then extended for a three-phase inverter.

A. Switching Transitions of SiC MOSFETs in a Half-Bridge Circuit

Fig. 5 shows the circuit schematic of a SiC half-bridge inverter employing two SiC MOSFETs (S_H and S_L) with their main parasitic elements namely, the drain-gate capacitance (C_{dg}), the gate-source capacitance (C_{gs}), and the drain-source capacitance (C_{ds}). The output current polarity is defined as positive when the current flows out from the half bridge's midpoint (A), as shown in Fig. 5.

Fig. 6 shows the detailed switching transitions when the output current is positive, where Figs. 6(a)-(c) elucidate the turn-ON commutation from the lower switch (S_L) to the upper switch (S_H), while the opposite case is shown in Figs. 6(d)-(f).

Referring to Fig. 6(a), when the lower switch S_L is ON, the current flows through its channel instead of the freewheeling diode, where the SiC MOSFET works in "synchronous rectification mode". At a time instant t_1 , a turn-OFF gate signal is applied to S_L where the current is diverted from the device channel to the antiparallel freewheeling diode, as shown in Fig.

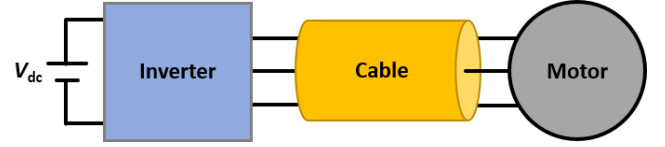


Fig. 4. Motor drive system with power cables.

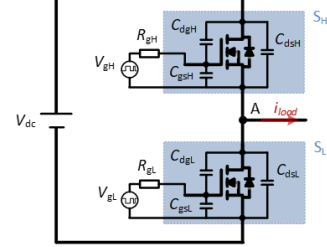


Fig. 5. A SiC-based half-bridge circuit.

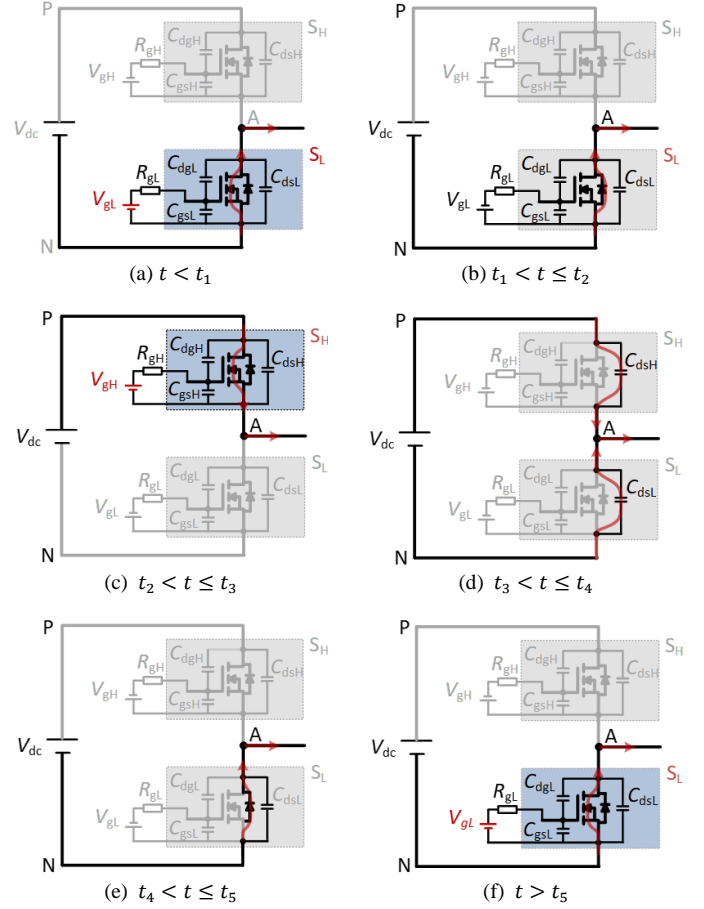


Fig. 6. Switching transitions of SiC half-bridge inverter.

6(b). In this case, the voltage V_{AN} across the lower switch keeps unchanged (i.e., $V_{AN} = 0$). After a dead time t_{dead} , a turn-ON gate signal is applied to the complementary device S_H allowing the current to flow through its channel, as shown in Fig. 6(c). Meanwhile, the lower switch blocks the entire dc-link voltage (i.e., $V_{AN} = V_{dc}$), as shown in Fig. 6(c). It should be noted that the switching time for V_{AN} to traverse from 0 to V_{dc} is only governed by the gate resistance of the adopted gate driver. Since

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the switching speed is extremely fast (the rise time is within 10–100 ns), the rising edge of V_{AN} is denoted as a step edge, as shown in Fig. 7(a).

Considering the opposite commutation case, when S_L is turned ON and S_H is turned OFF, Fig. 6(d) shows the current path when the turn-OFF gate signal is applied to S_H where the switch is instantly turned OFF. However, the voltage V_{AN} does not promptly decrease where the load current discharges the output capacitance of S_L while charges that of S_H . Thus, the voltage V_{AN} tardily decreases in a linear manner within a fall time t_{fall} , as given by:

$$t_{fall} = \frac{2C_{oss}V_{dc}}{i_{load}} \quad (1)$$

where, C_{oss} is the output capacitance of the SiC MOSFETs ($C_{oss} = C_{ds} + C_{dg}$), which can be considered as constant.

Therefore, according to (1), the fall time depends on the instantaneous load current i_{load} . When the current fully discharges the output capacitance of S_L (see Fig. 6(e)), the voltage V_{AN} declines to 0 V and the current flows through the antiparallel diode of S_L . After the deadtime t_{dead} , the turn-ON gate signal is applied to S_L , where the switch is turned ON and the current diverts from the antiparallel diode to the channel, maintaining V_{AN} at 0 V. Thus, during the turn-ON transition from S_H to S_L (interval $t_3 - t_5$), the voltage waveform V_{AN} can be illustrated as shown in Fig. 7(a), where the falling edge of V_{AN} is denoted as a ramp edge.

In a similar commutation mechanism, when the load current is negative, the switching transition can be obtained as shown in Fig. 7(b), where the rising edge is denoted as a ramp edge while the falling edge is denoted as a step edge.

Accordingly, when the output current is positive, the falling edge of the voltage V_{AN} is influenced by the load current and the parasitic capacitance. Oppositely, when the current is negative, the rising edge of V_{AN} is affected by the load current and the parasitic capacitance.

B. Switching Transitions of Line Voltages in a Three-Phase SiC Inverter

Fig. 8 shows a three-phase SiC inverter-fed motor drive with power cables. Only the line voltage V_{AB} is analyzed since the switching mechanism of the other line voltages is the same.

The line voltage V_{AB} is given by:

$$V_{AB} = V_{AN} - V_{BN} \quad (2)$$

Since V_{AB} is calculated as the difference between V_{AN} and V_{BN} , the switching transitions of V_{AB} depend on the relative polarities of the phase currents i_A and i_B . Within a fundamental cycle, these currents can be classified into four regions, depending on the polarity of alternation, as shown in Fig. 9. The theoretical phase- and line-voltage waveforms at different regions are accordingly depicted in Fig. 10.

In region I ($i_A > 0$ and $i_B < 0$), the voltage V_{AN} has a similar waveform with Fig. 7(a), the voltage V_{BN} has a similar waveform with Fig. 7(b), and the duty cycle of V_{AN} is larger than that of V_{BN} . Therefore, the line voltage V_{AB} is synthesized as shown in Fig. 10(a), where the voltage swings between 0 and

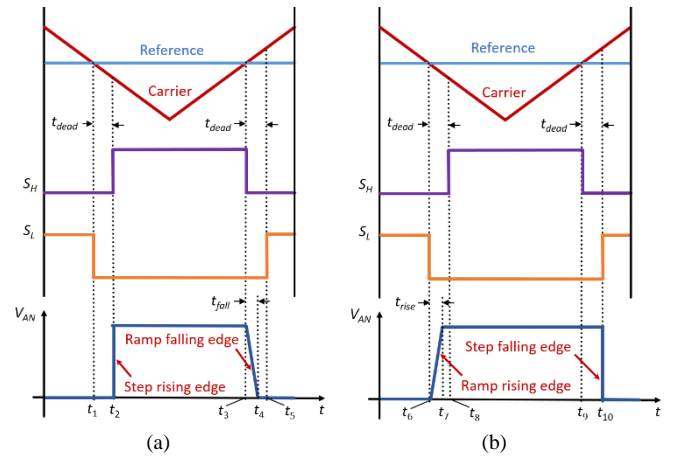


Fig. 7. The output voltage waveform of SiC half-bridge inverter when the phase current is (a) positive and (b) negative.

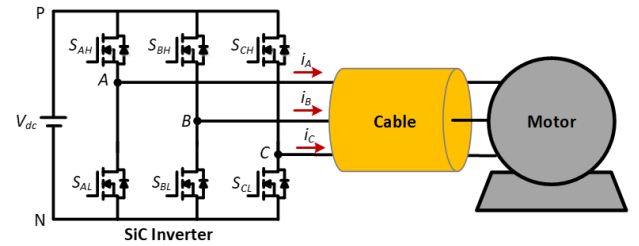


Fig. 8. Three-phase SiC cable-fed motor drive system.

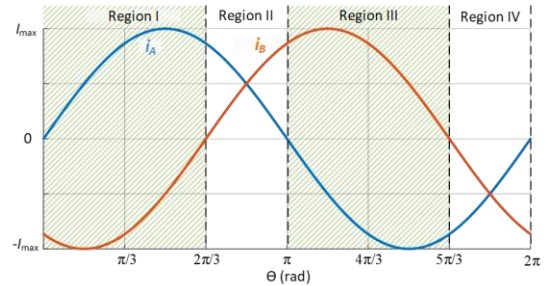


Fig. 9. Classification of phase currents based on their polarities.

V_{dc} . As can be noticed, the falling edges of the positive voltage pulses of V_{AB} are slower than the rising edges, being affected by the load current and the parasitic capacitance of SiC MOSFETs. For positive line voltage pulses, the rising edge results in ascending voltage transition from 0 to V_{dc} and the falling edge results in descending voltage transition from V_{dc} to 0. In this case, only the reflected voltages caused by the rising edges of V_{AB} matter since the resultant overvoltage can exceed the design voltage level of the motor winding insulation. Accordingly, in region I, the voltage reflections across the drive cables are only governed by the gate resistance.

In region III ($i_A < 0$ and $i_B > 0$), the voltage V_{AN} has a similar waveform with Fig. 7(b), the voltage V_{BN} has a similar waveform with Fig. 7(a), and the duty cycle of V_{AN} is smaller than that of V_{BN} . Therefore, the line voltage V_{AB} is synthesized as shown in Fig. 10(d), where the voltage swings between 0 and $-V_{dc}$. As can be noticed, the rising edges of V_{AB} are slower than

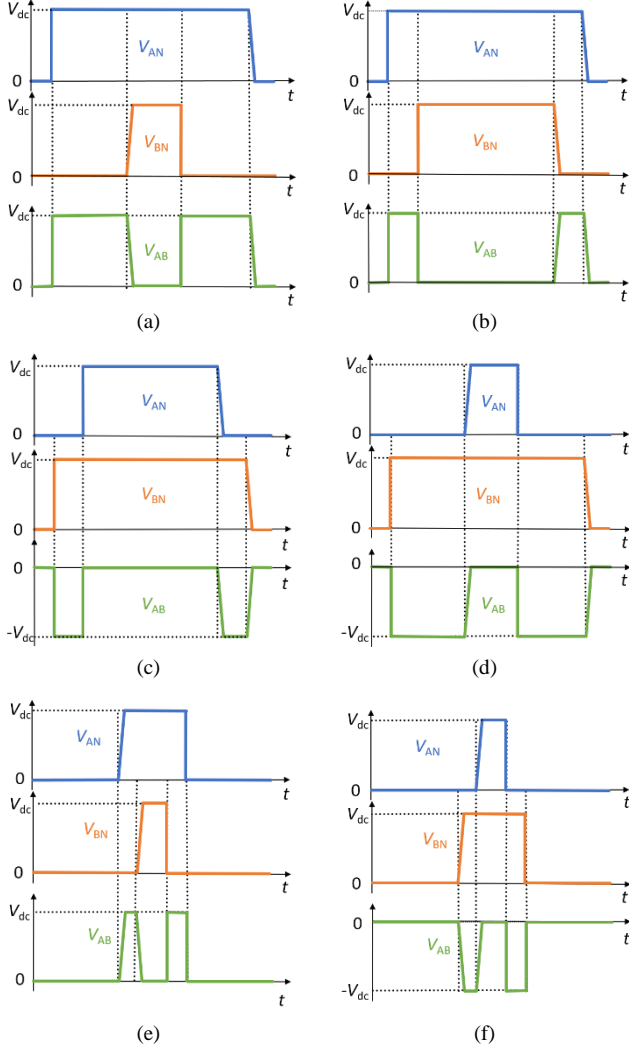


Fig. 10. Switching transitions of the line voltage V_{AB} in different regions: (a) region I (b) region II when $V_{AN} > V_{BN}$ (c) region II when $V_{AN} < V_{BN}$ (d) region III (e) region IV when $V_{AN} > V_{BN}$ (f) region IV when $V_{AN} < V_{BN}$.

the falling edges, being affected by the load current and the parasitic capacitance of SiC MOSFETs. For negative line voltage pulses, the rising edge results in ascending voltage transition from $-V_{dc}$ to 0 and the falling edge results in descending voltage transition from 0 to $-V_{dc}$. In this case, only the voltage reflections caused by the falling edges of V_{AB} matter since the associated overvoltage imposes higher stress across the motor windings. Thus, region III is similar to region I where the voltage reflections are only governed by the gate resistance.

In region II ($i_A > 0$ and $i_B > 0$), both V_{AN} and V_{BN} have similar waveforms with Fig. 7(a). When the duty cycle of phase A is larger than that of phase B, the line voltage V_{AB} is positive, as shown in Fig. 10(b), where the line voltage V_{AB} swings between 0 and V_{dc} . Oppositely, when the duty cycle of phase A is smaller than that of phase B, the line voltage V_{AB} is negative, as shown in Fig. 10(c), where the line voltage V_{AB} swings between 0 and $-V_{dc}$. Common to both figures, one voltage pulse of V_{AB} resembles a rectangle (i.e., step edges) and the

other pulse resembles a trapezoid (i.e., ramp edges). Thus, the rising/falling edges of V_{AB} pulses are occasionally affected either by the gate resistance or the load current and parasitic capacitance of SiC MOSFETs. In this case, the voltage reflections due to the incidence of rising/falling edges are governed either by the gate resistance or the load current and parasitic capacitance of SiC MOSFETs.

In region IV ($i_A < 0$ and $i_B < 0$), both V_{AN} and V_{BN} have similar waveforms with Fig. 7(b). When the duty cycle of phase A is larger than that of phase B, the line voltage V_{AB} is positive, as shown in Fig. 10(e), where the line voltage swings between 0 and V_{dc} . Oppositely, when the duty cycle of phase A is smaller than that of phase B, the line voltage V_{AB} is negative, as shown in Fig. 10(f), where the line voltage swings between 0 and $-V_{dc}$. Common to both figures, one voltage pulse of V_{AB} resembles a rectangle and the other pulse resembles a trapezoid. Therefore, the rising/falling edges of V_{AB} are affected either by the gate resistance or by the load current and parasitic capacitance of SiC MOSFETs. In this case, the RWP caused by the rising/falling edges can be either affected by the gate resistance or the load current and parasitic capacitance of SiC MOSFETs.

Accordingly, the output voltages of a three-phase SiC inverter have different rise and fall times depending on corresponding phase current polarities and phase-leg duty cycles. This results in a non-uniform overvoltage envelop at the motor terminals. For a given three-phase inverter-fed motor drive system, when the current polarity of phase A and phase B is different (region I and region IV), the RWP is only affected by the gate resistance. Whereas, when the current polarity of phase A and phase B is similar (region II and region III), the RWP can be affected either by the gate driver or the load current and parasitic capacitance of SiC MOSFETs. Therefore, the conventional DPT, which only focuses on the rising edge of the output voltage, cannot be effectively used to address the RWP in three-phase inverter-fed motor drives. The above theoretical analysis has been experimentally verified in the authors' earlier conference paper [19].

III. Q3L PWM OPERATION OF A T-TYPE CONVERTER FOR MOTOR OVERVOLTAGE MITIGATION

According to the analysis in Section II, the switching transitions are affected by the parasitic elements and load current, resulting in a non-uniform overvoltage envelop at the motor terminals. This also can affect the ability of some overvoltage mitigation methods that are fundamentally based on timing algorithms, where the inherent variation in switching rise/fall times can influence the accuracy of the applied mitigation strategy. Therefore, it is necessary to consider the conclusions drawn in Section II while assessing the effectiveness of some overvoltage mitigation approaches. Among existing overvoltage mitigation methods, the Q3L PWM is a filter-less approach which can mitigate the motor overvoltage without sacrificing the drive system efficiency. Being a time-based algorithm, the Q3L PWM performance in mitigating the motor overvoltage can be adversely affected by

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SiC parasitic. Thus, the Q3L PWM is addressed hereafter as an application example to extend the analysis of Section II.

The Q3L PWM was proposed in [16] for IGBT-based cable-fed motor drives. Its key idea is reshaping the PWM voltage transition pattern based on the observation that the voltage reflection can be cancelled by splitting the rising and falling transitions of the two-level PWM voltage pulses into two identical voltage steps with an appropriate separation time. Since the resultant voltage pulses have an interim voltage level in the transition between the two pole voltages, the modulation scheme is denoted as Q3L PWM. The delay time separating the two switched voltage steps is referred to as the dwell time t_{dwell} which depends on the wave propagation time t_p and the rise/fall time of the switching transitions t_r , as [15]:

$$t_{dwell} = 2t_p - t_r \quad (3)$$

The optimal setting of the dwell time, based on (3), allows the voltage reflections of the first voltage step to be significantly counterbalanced by the incidence of the second voltage step, as demonstrated in Fig. 11. Depending on the reflection coefficients at the inverter and motor sides, the motor overvoltage is 20% at most [15]. The Q3L PWM technique has been implemented using T-type converter-fed motor drives [16] and dual-converter-fed open-winding motor drives [17]. This article addresses the T-type converter, under Q3L PWM, as an application example to extend the parasitic/load current analysis from the two-level converter to the Q3L T-type converter.

As shown in Fig. 12, the T-type converter inherits the structure of standard two-level converters, however, with auxiliary branches connecting the dc-link midpoint to the output nodes of each phase leg. The auxiliary branches are realized using a bidirectional switch that is commonly implemented via a pair of switching devices in common source configuration [20]. Referring to Fig. 12, the output voltage V_{XN} , where $X = A, B$ or C , has three voltage states namely high, intermediate, and zero voltage levels (V_{dc} , $V_{dc}/2$, and 0). Considering phase A as an example, the high voltage level can be achieved by turning ON S_1 and S_2 , the intermediate voltage level is attained by turning ON S_2 and S_3 , and the zero-voltage level is attained by turning ON S_3 and S_4 . It should be noted that the switches in the auxiliary branch only conduct during the intermediate voltage level which lasts for a brief time (the dwell time). Thus, the current rating of these switches can be designed much lower than that of the main switches, unlike the case in a standard three-level T-type converter. Further, the switching devices in the auxiliary branches only block half of the dc-link voltage [20]. Therefore, the switching devices of the auxiliary branches can be implemented with lower voltage and current rating.

Fig. 13 illustrates the gate signals generation for the switching devices of phase A under Q3L PWM scheme, where t_{dead} is the deadtime between S_1 and S_3 or S_2 and S_4 , while $2t_p$ is the ON-time of S_2 or S_3 during the commutation process. Accordingly, Fig. 14 elucidates the ideal output voltage V_{AN} for different current polarities. When the phase current is positive,

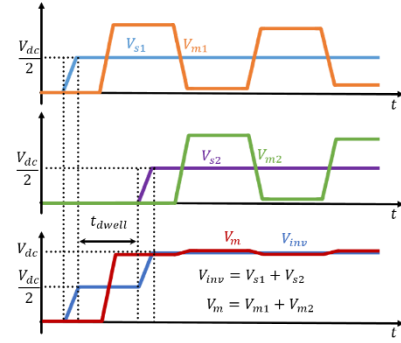


Fig. 11. Idealized inverter voltage V_{inv} and motor voltage V_m under Q3L PWM.

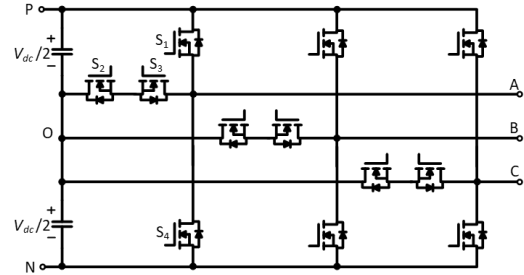


Fig. 12. A three-phase SiC T-type converter.

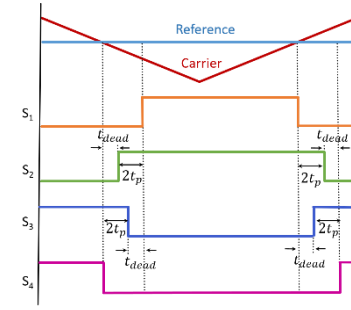


Fig. 13. Gate signal generation of Q3L PWM in T-type converters.

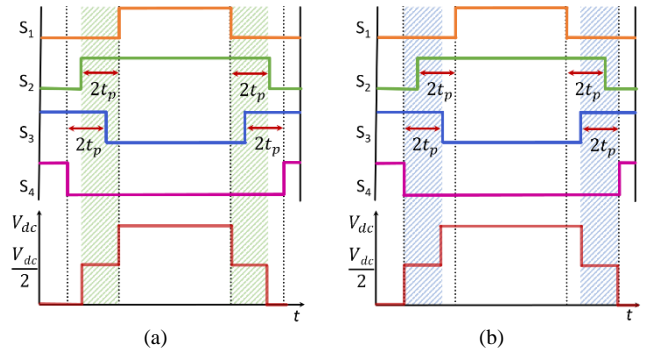


Fig. 14. The output voltage of Q3L T-type converter when the phase current is (a) positive and (b) negative.

i.e., the current flows out from the output node A, the dwell time of the intermediate voltage of V_{AN} is dominated by the ON-time of S_2 , as shown in Fig. 14(a). While the opposite case, i.e., when the phase current is negative, is shown in Fig. 14(b), where the intermediate voltage is dominated by S_3 . Since the ON-time of S_2 and S_3 are equal to $2t_p$, the intermediate voltage level

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duration is $2t_p$ regardless of the current polarity, i.e., the Q3L PWM scheme works independently of the current direction. It is worth noting that although the commanded dwell time is $2t_p$, the effective dwell time in the output voltage waveform is shortened by the rise time of the main switches, i.e., $t_{dwell} = 2t_p - t_r$.

IV. MODELLING OF SWITCHING TRANSITIONS IN Q3L T-TYPE CONVERTER

In the T-type converter, the effect of parasitic and load current on the switching rise/fall times of the output voltages can result in inaccurate dwell time setting which negatively impacts the effectiveness of the Q3L approach in overvoltage mitigation. Thus, the switching commutation process of the T-type converter under the Q3L PWM must be investigated in detail considering the effect of SiC parasitic. The analysis is conducted for a single-phase T-type converter, then extended for a three-phase system.

The commutation process can be divided into transition I, within which the output voltage V_{AN} ascends from 0 to V_{dc} , and transition II for the opposite case. Only the scenario for positive load current is analyzed in the following subsections where the negative load current scenario follows the same approach.

A. Switching Transition I

In this transition, the commutation process is divided into five intervals as elucidated in Fig. 15 with the corresponding output voltage waveform as shown in Fig. 16.

Referring to Figs. 15(a)-(c) and Fig. 16, the load current starts to divert from S_4 to the auxiliary branch when the turn-ON gate signal is applied to S_2 . Therefore, at a time instant t_2 , the output voltage V_{AN} starts to ascend from 0 to $V_{dc}/2$ within a rise time t_r . It should be noted that the rise time t_r is only governed by the gate driver resistance of S_2 . Likewise, referring to Figs. 15(d) and 15(e), the output voltage V_{AN} starts to ascend from $V_{dc}/2$ to V_{dc} when the turn-ON gate signal is applied to S_1 , where the rise time is only governed by the adopted gate driver resistance. Since the switching speed is extremely fast, the rising edges of V_{AN} are denoted as steep rising edges, as shown in Fig. 16.

In the above commutation process, the rising edges of the two voltage steps of V_{AN} have the same rise time t_r , which is governed by the gate resistance. Since the duration of the turn-ON signal of S_2 is $2t_p$, as mentioned in Section III, the effective dwell time is $t_{dwell} = 2t_p - t_r$, which is the optimal dwell time value for overvoltage mitigation.

B. Switching Transition II

Figs. 17 and 18 elucidate the commutation process and the corresponding output voltage waveform, respectively. The commutation process is affected by the parasitic of SiC MOSFETs and load current which can be divided into two regions depending on its value.

(a) High-current region

Referring to Figs. 17 (a)-(c) and Fig. 18 (a), at a time instant

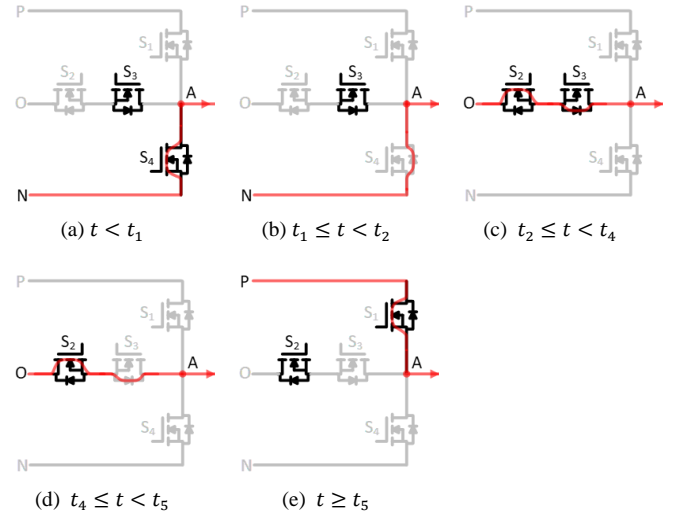


Fig. 15. The commutation processes for V_{AN} from 0 to V_{dc} when the load current is positive.

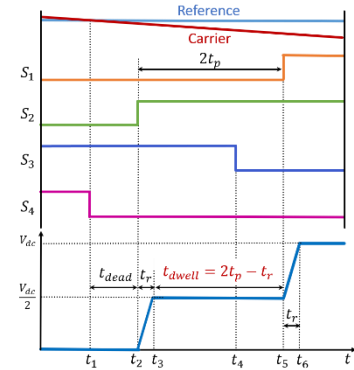


Fig. 16. The output voltage V_{AN} during the commutation process I when the phase current is positive.

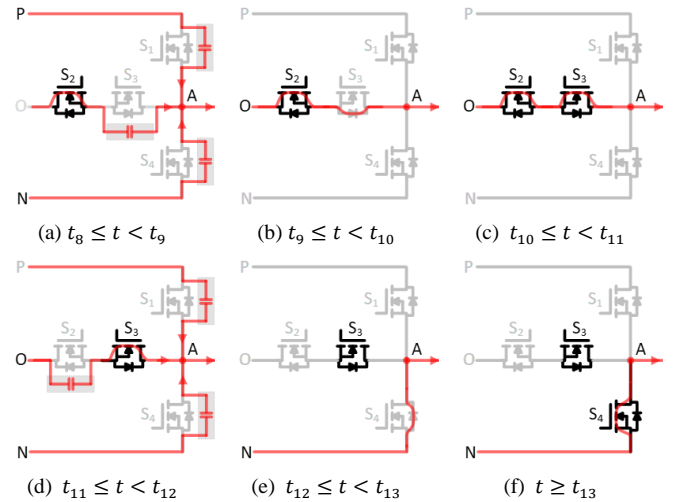


Fig. 17. The commutation processes for V_{AN} from V_{dc} to 0 when the load current is positive.

t_8 , S_1 is instantly turned OFF with the turn-OFF gate signal applied to it. However, the voltage V_{AN} does not promptly decrease where the load current discharges the output capacitance of S_3 and S_4 while charges that of S_1 . Thus, the fall

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time t_f of V_{AN} when declining from V_{dc} to $V_{dc}/2$ is given as:

$$t_f = \frac{3C_{\text{coss}}V_{dc}}{2i_{\text{load}}} \quad (3)$$

According to (3), the fall time depends on the instantaneous load current i_{load} .

Similarly, referring to Figs. 17 (d)-(f), the output voltage V_{AN} tardily decreases from $V_{dc}/2$ to 0 when the turn-OFF gate signal is applied to S_2 , where the load current discharges the output capacitance of S_4 while charges that of S_1 and S_2 . Thus, the fall time of V_{AN} is given by (3).

Referring to Fig. 18 (a), the time spent at the intermediate voltage level is $t_{\text{dwell}} = 2t_p - t_f$, which is the optimal dwell time for the Q3L PWM to mitigate the motor overvoltage.

(b) Low-current region

According to (3), when the inverter operates at the low-current region, the fall time t_f will be longer. Thus, the corresponding output voltage V_{AN} will be as shown in Fig. 18 (b). As seen, the output voltage V_{AN} is larger than $V_{dc}/2$ at t_{10} , where the energy stored in the output capacitance of S_3 has not been fully transferred to the load. This residual drain-source voltage is discharged through the channel of S_3 when the turn-ON gate signal is applied to it. It should be noted that the falling edge from V_{dc} to $V_{dc}/2$ has two segments with different slew rates. The first segment t_{f1} is controlled by the load current and devices' parasitic, while the second segment t_{f2} is controlled by the gate resistance. Similarly, the falling edge from $V_{dc}/2$ to 0 has two segments with different slew rates. As seen, when the turn-ON gate signal is applied to S_4 , the output voltage V_{AN} is larger than 0, resulting in the residual drain-source voltage being discharged through the channel of S_1 .

Referring to Fig. 18 (b) the effective dwell time is not equal to $2t_p - t_r$, where the Q3L approach cannot fully mitigate the voltage reflections when the load current is close to zero.

Accordingly, when the load current is positive, the output voltage waveform is shown in Fig. 19 (a), where the rising edge (blue line) is only governed by the adopted gate resistance while the falling edge (red line) is affected by the parasitic and load current. Oppositely, when the load current is negative, the output voltage waveform is shown in Fig. 19 (b), where the rising edge (red line) is affected by the parasitic and load current while falling edge is governed by the adopted gate resistance.

It should be noted that the red solid lines indicate the inverter operation at high-current region while the red dotted lines indicate the low-current region. Therefore, when the load current is close to zero, the Q3L does not fully mitigate the voltage reflections due to the impact of the parasitic and load current.

C. Switching Transitions of Line Voltages in Three-Phase Q3L T-type Converter

Comparing Fig. 19 to Fig. 7, the rising/falling edges of V_{AN} of the Q3L T-type converter inherit the same characteristics of the two-level converters, however the edges are split into two voltage steps with a dwell time. Therefore, the line voltage V_{AB} of the Q3L T-type converter is similar to that of the two-level

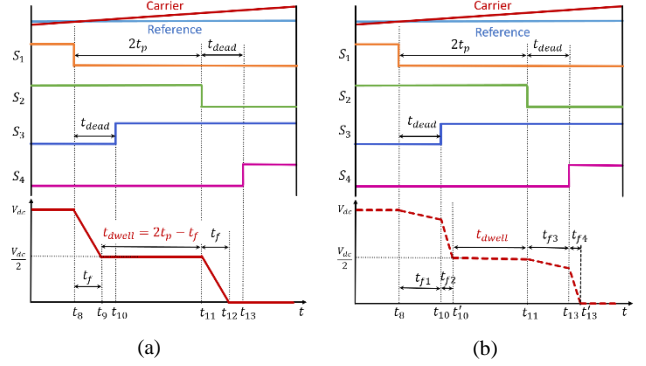


Fig. 18. The output voltage V_{AN} during the commutation process II when the inverter operates at (a) high load current region and (b) low load current region.

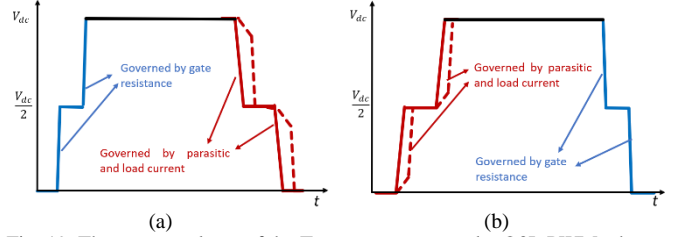


Fig. 19. The output voltage of the T-type converter under Q3L PWM when the load current is (a) positive and (b) negative.

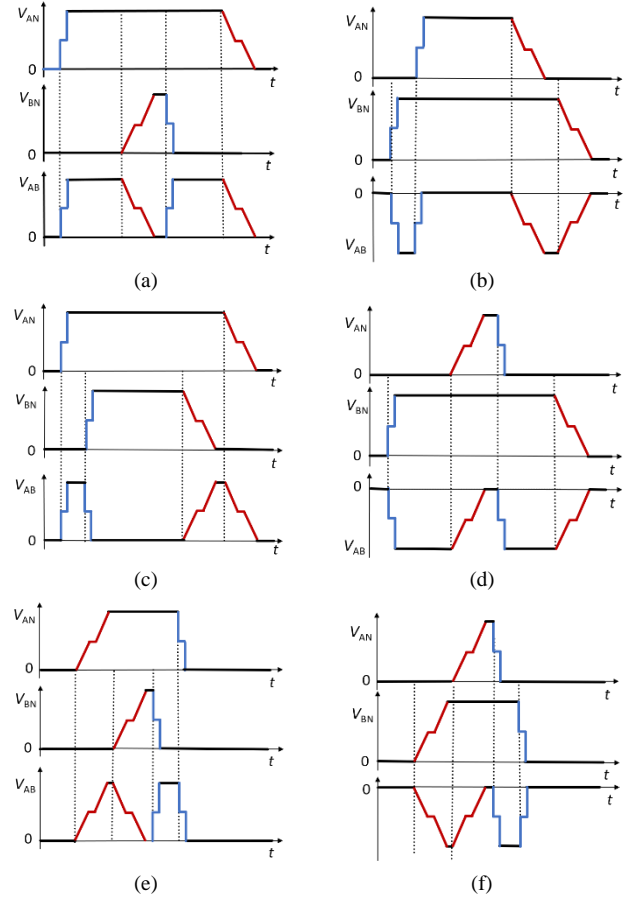


Fig. 20. Switching transitions of the line voltage V_{AB} of the Q3L T-Type converter in different current regions: (a) region I (b) region II when $V_{AN} > V_{BN}$ (c) region II when $V_{AN} < V_{BN}$ (d) region III (e) region IV when $V_{AN} > V_{BN}$ (f) region IV when $V_{AN} < V_{BN}$.

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converter. Fig. 20 depicts the phase- and line-voltage waveforms at different regions according to the phase current polarities. Accordingly, the characteristics of the line voltage V_{AB} can be summarized as follows:

- In region I (Fig. 20 (a)) and region III (Fig. 20 (d)), the Q3L PWM can completely mitigate the RWP since the effective dwell time is the optimal one as the switching transitions are governed by the gate resistance.
- In regions II and IV, the overvoltage mitigation ability of the Q3L PWM will be affected as the dwell time might deviate from the optimal value due to the load current and the parasitic elements. Specifically, in region II when $V_{AB} < 0$ (Fig. 20 (b)) and the load current i_A is close to zero, or when $V_{AB} > 0$ (Fig. 20 (c)) and the load current i_B is close to zero, the Q3L PWM cannot mitigate the RWP completely. Whereas, in region IV when $V_{AB} > 0$ (Fig. 20(e)) and the load current i_A is close to zero, or when the line $V_{AB} < 0$ (Fig. 20 (f)) and the load current i_B is close to zero, the Q3L PWM cannot mitigate the RWP completely.

V. EXPERIMENTAL VERIFICATION

To verify the theoretical analysis, a T-type converter is used to supply a three-phase four-pole 7.5kW induction motor through 12.5m long four-core unshielded 13 AWG PVC power cables, as shown in Fig. 21. The inverter is modulated by the Q3L PWM with 20 kHz switching frequency and 50 Hz fundamental frequency, and it is supplied from a 400 V dc power supply. The switching devices are based on Wolfspeed C2M0040120D SiC MOSFETs that are driven by gate drivers with 25 Ω gate resistance. The control algorithm is implemented using a DSP (TI TMS320F28335) and an FPGA (Xilinx XC3S400).

The inverter is first operated as a standard two-level converter, using the traditional SPWM, to assess the overvoltage due to the RWP. The two-level converter can be realized by deactivating the auxiliary branches of the T-type converter. Then, the Q3L PWM, shown in Fig. 13, is adopted where $2t_p = 220$ ns and $t_{dead} = 300$ ns.

Fig. 22 shows the voltage doubling effect due to the RWP when the inverter generates two-level voltage pulses. Fig. 22(a) shows the line voltage across the inverter and motor, with zoomed-in views in Figs. 22 (b) and (c) during the rising and falling voltage transitions, respectively. Referring to Fig. 22, the motor voltage oscillates with 2 p.u. magnitude in a damped manner due to the RWP. With the adoption of the Q3L PWM, Fig. 23(a) shows the inverter and motor line voltages within switching cycles. As shown, the Q3L PWM can effectively combat the overvoltage due to the RWP, where the maximum overvoltage is reduced to 1.15 p.u. Further zoomed views showing the load voltage propagation in response to the Q3L PWM during the rising and falling transitions are given in Figs. 23(b) and (c), respectively. It can be noticed that the voltage across the load terminal has a two-level waveform although the inverter voltage has a Q3L waveform.

It should be noted that the impact of parasitic and load current on the switching transitions and the RWP of SiC-based two-



Fig. 21. The experimental setup.

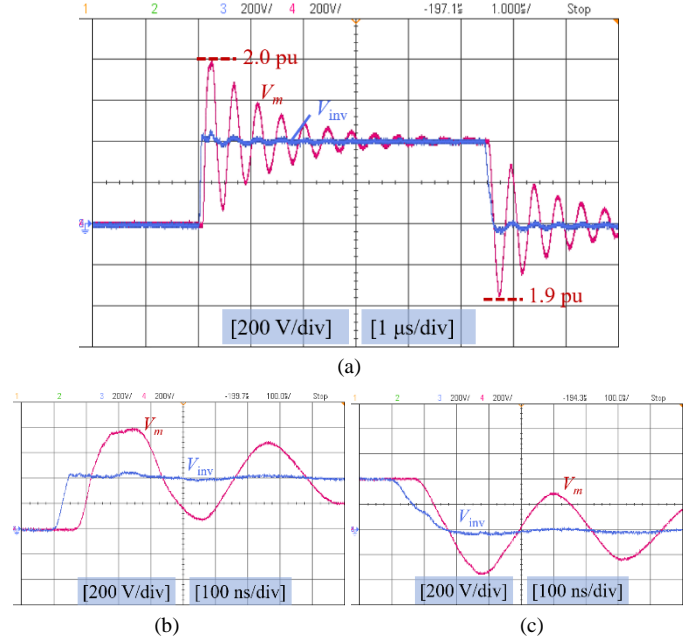


Fig. 22. Inverter and motor line voltages under the traditional two-level SPWM: (a) switching cycles view (b) a zoomed view at the rising transition and (c) a zoomed view at the falling transition.

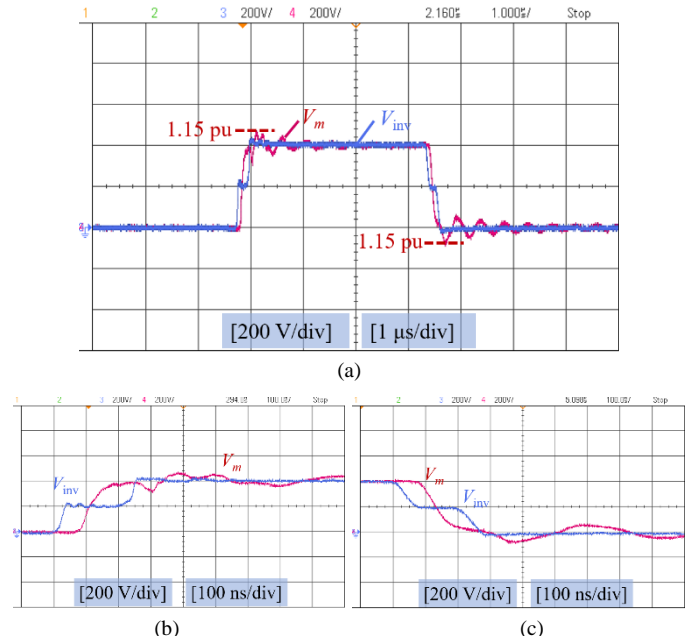


Fig. 23. Inverter and motor line voltages under the Q3L PWM: (a) switching cycles view (b) a zoomed view at the rising transition and (c) a zoomed view at the falling transition.

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level converters has been experimentally verified in the authors' conference paper [19]. For brevity, the following part only shows the experimental results that verify the impact of parasitic and load current on the attenuation of the RWP in the Q3L T-type converter cable-fed system.

Fig. 24 shows the phase currents i_A and i_B , the line voltage across the inverter V_{inv} , and the line voltage across the motor V_m of the T-type converter, when modulated by the Q3L PWM, for two fundamental cycles. As can be noticed, the load overvoltage is limited to 1.15 pu for the most of the fundamental cycle. However, the overvoltage is 1.37 pu when the load current is close to zero. This occurs since the dwell time is not the optimal value as a consequence of the parasitic, as previously analyzed. Fig. 25 further shows the motor overvoltage at different load current values when the inverter is controlled by the Q3L PWM.

Figs. 26-29 show zoomed views of the obtained results in Fig. 24, verifying the theoretical analysis of the line voltage waveform during different operation regions. In detail, Fig. 26 shows the results for region I, Fig. 27 for region III, Fig. 28 for region II, and Fig. 29 for region IV. It can be noticed that the experimental results show good agreement with the theoretical waveforms presented in Fig. 20.

Referring to Fig. 26, in region I, the inverter voltage $V_{inv} > 0$ and the rising time t_r is about 50 ns which is shorter than the falling time (100 ns). This is because the rising time is only affected by the gate driver while the falling time is affected by the load current and the parasitic capacitance of SiC MOSFETs. However, in region III (Fig. 27), the inverter line voltage V_{inv} shows the opposite trend. As can be noticed, the inverter voltage $V_{inv} < 0$ and the falling time (50 ns) is shorter than the rising time (60 ns). Common to Figs. 26 and 27, the peak load overvoltage is maintained within 1.15 pu since the dwell time is the optimal value where the rising and falling edges are governed by the gate resistance.

Fig. 28 shows the experimental results in region II when the inverter voltage $V_{inv} < 0$, where, the rising edge is shown in Fig. 28 (a) and the falling edge is shown in Fig. 28 (b). As can be noticed, both rising and falling times are longer than the switching time. Referring to Fig. 28 (a), the rising edges have different rise times resulting in a non-optimal dwell time setting. This results in an increased overvoltage across the load where the peak load voltage is 1.37 pu. This occurs since both rise time and fall time are affected by the load current and the parasitic capacitance of SiC MOSFETs when the line voltage, as analyzed in Section IV. It is noteworthy that compared with the theoretical analysis in Fig. 18 (b), t_{f4} does not show up in Fig. 28 (a). The main reason is that the theoretical analysis assumes the inverter output current keeps constant during commutation processes. However, in the experiment, the high dv/dt charges/discharges the parasitic capacitance of the cable resulting in a variable current during the switching transients, as evidenced in Fig. 28 (a). Referring to Fig. 28 (a), the current polarity of i_A changes from positive to negative, which means the converter operation region switches from region II ($i_A > 0$, $i_B > 0$) to region III ($i_A < 0$, $i_B > 0$). Therefore, t_{f4} does not

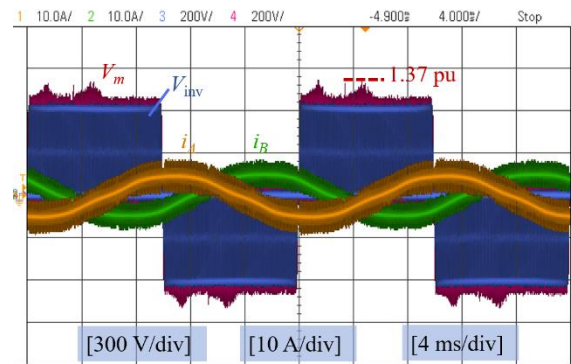


Fig. 24. Experimental results of the phase currents and the line voltages of the Q3L T-type converter-fed system at the inverter and motor sides.

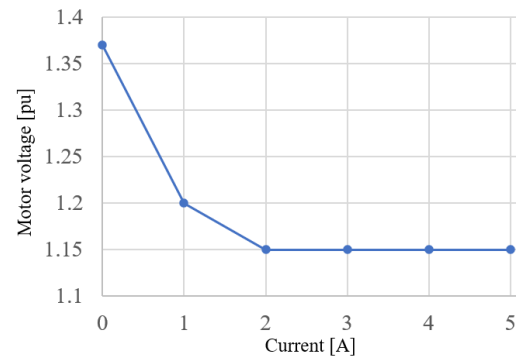
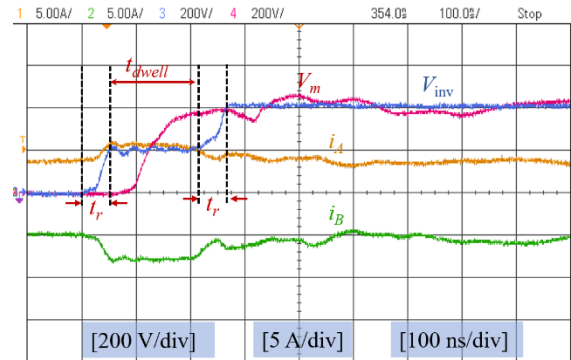
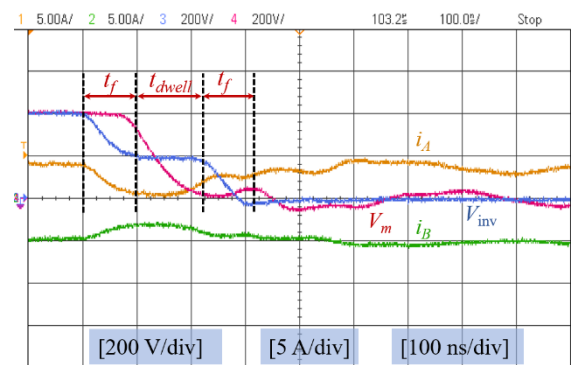


Fig. 25. Motor overvoltage at different current values.



(a)



(b)

Fig. 26. Phase currents and the line voltages at the inverter and motor sides under the Q3L PWM during the switching transitions in region I at (a) the rising transition and (b) the falling transition.

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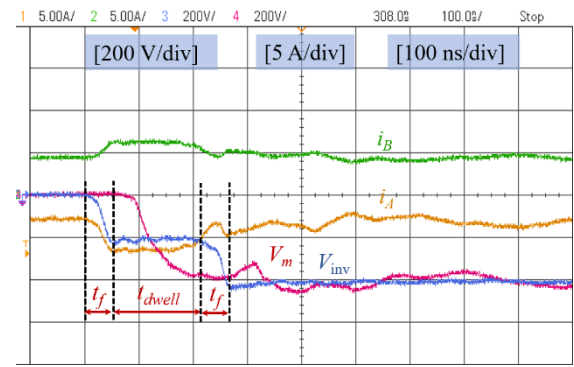
show up in the experiment, i.e., the falling edges (t_{f1} , t_{f2}) show a similar pattern with that in region II, and the falling edge (t_{f3}) shows a similar pattern with that in region III. Similar results can be observed in region IV, as depicted in Fig. 29.

In summary, the experimental results show that at low load current region, the motor overvoltage is attenuated to 1.37 pu which is still within the safe voltage limits of motor winding insulation. If further mitigation of overvoltage is needed under very low current, one possible mitigation approach is to change the inverter operation mode from the Q3L PWM to the standard two-level PWM when the load current is close to zero, while using a smart gate driver which can adaptively adjust the gate resistance to increase the switching rise time. With the prolonged rising transition, the motor overvoltage can be significantly attenuated when the load current is close to zero. Since only the rise time is prolonged when the load current is close to zero, this approach will not increase the switching power loss.

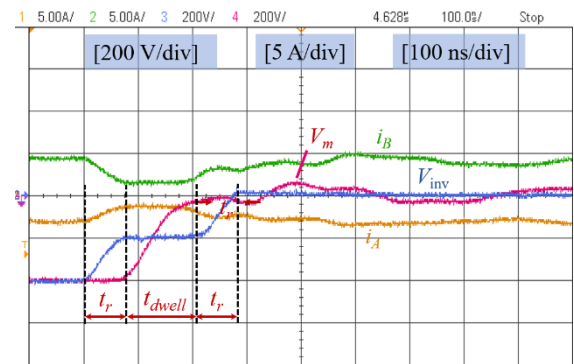
Another possible mitigation approach is adding a passive filter in cascade with the T-type converter to provide further overvoltage mitigation. Compared with the conventional system (two-level inverter + filter), the ‘Q3L inverter + filter’ system can reduce the filter size since the Q3L approach already features partial/full overvoltage mitigation. Since this article focuses on reporting the impact of the load current and switching device parasitic on the overvoltage mitigation, the aforementioned possible overvoltage mitigation methods at low current region will be investigated in future work.

VI. CONCLUSION

This article has analytically investigated the impact of load current and parasitic elements of SiC MOSFETs on the switching transitions of inverter-fed motor drives. The analysis has been presented for the two-level converters showing that the parasitic capacitance of SiC MOSFETs, along with the instantaneous load current value, critically affect the magnitude of motor overvoltage in cable-fed drives. As an application example, the analysis has been extended to the Q3L T-type converter being a candidate approach to mitigate the motor overvoltage in cable-fed drives. It has been shown that the SiC parasitic may adversely affect the ability of the Q3L T-type converter to fully mitigate the voltage reflections in certain cases, due to the consequent variation in the switching rise/fall times depending on the load current polarity and magnitude. The theoretical analysis has been experimentally verified. The results showed that the Q3L PWM approach can effectively mitigate the overvoltage between each two phases that have different current polarities, where the switching transitions of the associated line voltage are only governed by the gate resistance of the employed gate driver. Whereas, when the polarities of the phase currents are similar, the Q3L modulation scheme allows a full overvoltage mitigation only when the load current is high, and a partial overvoltage mitigation (i.e., increased overvoltage) when the load current is close to zero where the switching transitions are affected by the SiC parasitic capacitance.

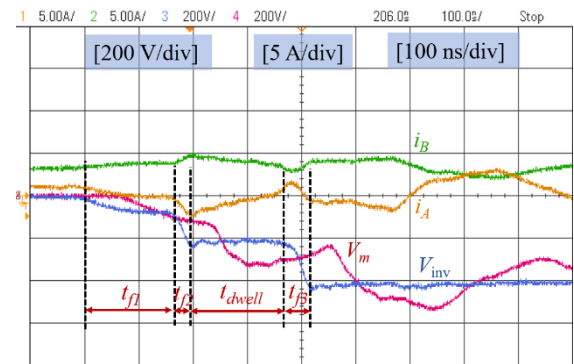


(a)

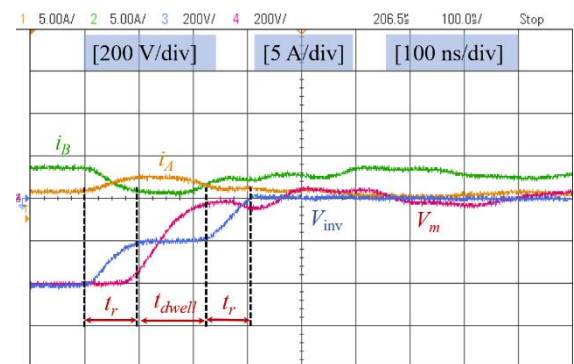


(b)

Fig. 27. Phase currents and the line voltages at the inverter and motor sides under the Q3L PWM during the switching transitions in region III at (a) the falling transition and (b) the rising transition.



(a)



(b)

Fig. 28. Phase currents and the line voltages at the inverter and motor sides under the Q3L PWM during the switching transitions in region II at (a) the rising transition and (b) the falling transition when $V_{inv} < 0$.

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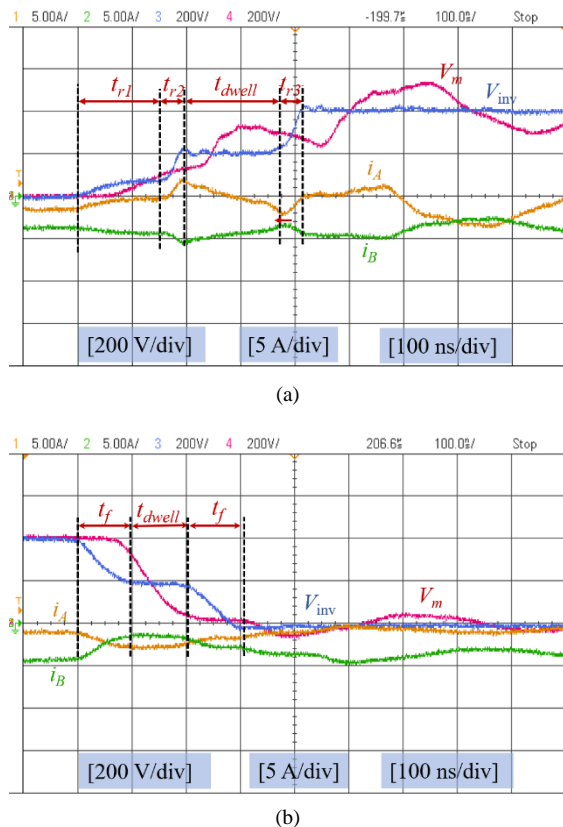


Fig. 29. Phase currents and the line voltages at the inverter and motor sides under the Q3L PWM during the switching transitions in region IV at (a) the rising transition and (b) the falling transition when $V_{inv} > 0$.

ACKNOWLEDGMENT

The authors would like to thank Dr. Mohammad H. Hedayati and Dr. Nick Simpson at the Electrical Energy Management Group, University of Bristol, Bristol, U.K., for their help in experimental setup preparation.

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