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Multi-Functional PV Inverter with Low voltage Ride-Through and Constant Power Output

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ABSTRACT Renewable photovoltaic (PV) energy is a primary contributor to sustainable power generation in microgrids. However, PV grid-tied generators remain functional as long as the grid voltage and the input PV source remain normal. Abnormal conditions like transient grid sags or solar irradiation flickering can make the grid-tied inverter go offline. Simultaneous shut down of PV generators residing in the distribution grid may lead to an overall grid instability or outage. Therefore, PV generators must be equipped with fault-ride-through mechanisms in order to remain connected and operational during faults. This paper presents a PV-inverter with low-voltage-ride-through (LVRT) and low-irradiation (LR) compensation to avoid grid flickers. The single-phase inverter rides through the voltage sags while injecting reactive power into the grid. The proposed control strategy ensures a steady DC-link voltage and remains connected to the grid during AC-side low voltage and DC-side low-irradiation faults. Unlike other PV inverters, the controller maintains the maximum-power-point-tracking (MPPT) in all conditions. LVRT, constant power output, and robust MPPT are the noticeable features of the proposed system. Frequency analysis, simulations, and a laboratory prototype validate the proposed control strategy.

INDEX TERMS Microgrid, PV inverter, LVRT, Constant power output, MPPT

I. INTRODUCTION

The recent rise of a low power distributed power generation (LPDG) into the grid network and its continuous growth will eventually make it a dominant power generation source in the future. Among the LPDG, photovoltaic (PV) sources are a noteworthy contributor to electricity. The PV power is interfaced to the grid via grid-tied inverters, which are inertia-less power electronic devices programmed to shut down if the grid parameters like voltage or frequency deviate from the standard values. However, grid voltage sags are commonplace in practical power systems, which may disrupt the grid-tied inverter's operation. The grid network, which is dominated by LPDG, is always at the risk of blackout or instability because an undue sag can make all the LPDG go offline for some time. In a conventional power grid, the sags are dealt with STATCOM techniques which connects a reactive element to the point-of-common-coupling (PCC) to fulfills the LVRT [1]. Since LPDGs are distributed all across the grid network, so a central grid operator cannot manage and control these low power generators. Therefore, STATCOM techniques are not effective for LPDGs of distribution grid. The LPDG must autonomously ride-through sags by intelligently detecting and countering the fault[2, 3]. The regulatory grid codes across the world recommend the LPDGs to reduce their active power and inject reactive power during sags[4]. However, the two-stage

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PV inverters are designed to extract the maximum available PV power in all conditions. The first stage boost converters keep operating at maximum power point tracking (MPPT) in sags, which surges the DC-link voltage [5, 6]. An unstable DC-link voltage is the cause of inverter shutdown. Therefore, many recently proposed LVRT control techniques for LPDGs disables the MPPT during sags to avoid DC-link surge[1, 7-9]. A comprehensive literature review suggests that all the existing LVRT techniques switches the first-stage boost converter from MPPT to a fixed duty cycle mode. However, the fixed duty cycle approach for attaining the LVRT is only effective if the sag is also of fixed intensity. Most of the solutions for single-phase LVRT inverters presented in the literature can only deal with pre-determined fixed sag intensity [1, 4, 6-13]. However, the actual grid scenario can have a sag of variable magnitude. More severe sag will have a severer effect on the operation of the PV inverter.

A. Existing LVRT Problem

The two-stage PV inverter consists of a first-stage DC-DC boost converter, and the second-stage DC-AC inverter is shown in Fig.1. The DC-link decouples the DC and AC sides. The DC-link voltage stability is critical to overall inverter operation. Therefore, AC and DC fault ride through is analyzed separately in terms of power balance at the DC-link. In PV systems, the total power (P_{Total}) available at the solar source is (P_{MPPT}). Therefore, for an efficient PV system, all the power must be consumed at all times, as shown in (1). Equation(2) expresses the power balance at the DC-link in normal operation just before faults, where P_{INV} is the output power of the inverter, $P_{DC\text{-}Link}$ is the power required to maintain the DC-link voltage, and P_{losses} is the power dissipated in losses.

$$P_{Total} = P_{MPPT} \tag{1}$$

$$P_{MPPT} = P_{INV} + P_{DC-Link} + P_{losses} \tag{2}$$

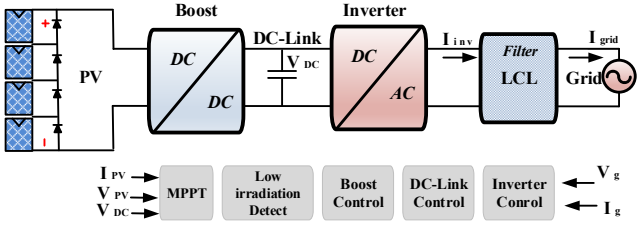

FIGURE 1. Operational block diagram of two stage PV inverter.

Consider the operating point of the inverter on the PV curve in Fig.2. In regular operation, the inverter is operating at MPPT. When the inverter experiences a 30% sag, the input power must be curtailed to ride through this sag. However, curtailing the input power can be achieved by shifting right or left on the PV curve. If the duty cycle of the boost is reduced, it will shift the boost converter at point A on the PV curve[13]. The same reduction in PV power can be achieved by increasing the duty cycle as shown at point A'. However, if a severer sag appears, the duty cycle of the boost stage must be adaptively selected to retain the power balance in the system. As depicted in Fig.2, when a 70% sag appears, the PV inverter again curtails the PV power by shifting more toward right or left on the PV curve. If the input power is reduced by further shifting left at point B' on the PV curve, the boost inductor core may saturate, leading to the collapse in the DC-link voltage[14, 15]. Since the maximum recommended duty cycle of a typical boost converter is 65-70% [16], it is advisable to keep the boost stage operation well below this value. Therefore, shifting the boost converter operation on the left of the PV curve must be avoided.

On the other hand, if the duty cycle is further reduced, the boost converter will be operating at point B and fall into an undesirable discontinuous-conduction mode (DCM). The boundary condition for transitioning from CCM to DCM is defined as k in (3) and (4); the derivation is available in the study [17]. The boundary condition depends on duty-cycle D, Boost inductance L_{boost}, switching frequency F_{sw}, and the load on the DC-link R, which is a function of injected grid-current I_{grid} and the power available at the PV panel P_{MPPT}, $R = V_{dc}/I_{dc}$, [17, 18].

$$k = 2F_{sw} L_{boost} R \tag{3}$$

$$k_{critical} = D(1-D)^2 \tag{4}$$

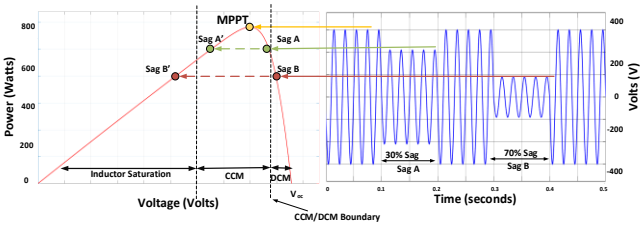

FIGURE 2. CCM to DCM in variable sag intensity

For reduced power operation during sags the first stage boost converter should be operated at a certain duty cycle to maintain the input/output power balance. However, the existing LVRT methods operate the boost stage at a predetermined fixed duty in both mild or severe sags. In a more severe sag, the fixed duty cycle operation cannot ensure the DC-link voltage stability and may still surge the DC-link voltage[13]. Therefore, the boost-stage duty cycle should be selected adaptively according to the sag intensity. However, for severe sag compensation a new duty cycle may be too-low which can make the boost converter falls from (CCM) to (DCM)[13, 19]. The boost converter may not provide adequate gain in DCM, thus failing to achieve the required DC-link voltage, resulting in inverter shutdown. If the LVRT strategy curtails the PV power by operating on the left side of PV curve, the duty cycle will exceed the maximum duty cycle of boost converter and saturates the boost inductor. Thus, resulting in a complete collapse in the DC-link voltage. Therefore, it is important to design an LVRT method independent of sag intensity without disrupting the boost stage operating point.

B. Flickers due to low irradiation

The intermittent nature of solar energy also affects the output of the PV generator. Even during fully illuminated solar hours, the solar irradiance can quickly fluctuate from 100% to 40% within a few seconds[20]. The irradiance fluctuation in PV systems may lead to power flickers, which can risk an overall grid stability [21]. The low-irradiance (LiR) directly affects the power quality of grid inverters in the form of AC flickers [22]. The input power variations also cause undue stress on the internal inverter components, thus reducing the inverter life and robustness Flicker problems are well-researched, and irradiance-generated flickers are observed in many parts of the world [23]. Most of the solutions to mitigate flicker is applied at the power system level in which the grid operator requires the load flow data at every bus in the power system. The busses load flow data enables the grid operator to take the actions such as PV-plants curtailments, reactive power injections, or targeted load shedding [24]. However, another solution to deal with flickers is by maintaining a constant power injection into the grid[25]. Many studies have proposed to utilize an energy storage device to mitigate the flickers generated due to renewable energy generators. The authors in [26] have proposed the BESS-based flicker compensator for small-scale hydel-inverters. Brinkel et al. [27] have proposed to utilize the battery energy of electric vehicles to reduce the power quality issues in the microgrid. The analysis for the fast variation in irradiance is reported in the study [20], which shows that the real-time irradiance fluctuations range from 10% to -90% within 10 seconds.

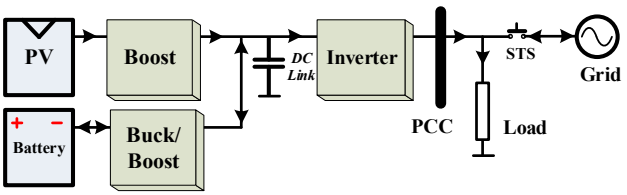

FIGURE 3. Two stage PV inverter.

C. Novel LVRT solution with constant power output strategy

The microgrid stability is mainly dependent on the resiliency of low-power PV generators; therefore, it is vital to provide a fault ride-through mechanism in PV inverters for grid sags and low-irradiation (LiR) faults [10]. This paper presents novel fault ride-through support for a two-stage PV inverter utilizing an intermediate energy storage buffer. The buffer can absorb the DC-link surplus energy during the grid sags. At the same time, it can deliver the energy deficit to DC-link in the event of low-irradiation conditions. Fig.3 shows a typical PV-Battery hybrid system. The first stage boost converter amplifies the low PV voltage to a high-voltage DC-link and tracks the maximum power point. Secondly, the DC-link voltage is converted to AC and coupled to the grid via a suitable filter. The novel features of the proposed system are listed as:

1. Unlike previous LVRT strategies for PV inverters, the proposed system can ride through variable intensity sags while maintaining the MPPT. This is accomplished by harvesting the surplus energy into storage buffer during sags.
2. The inverter provides the constant power output even during the transient low-irradiation. The energy deficit during LiR is acquired from a storage buffer.
3. The inverter remains connected to the grid in both AC and DC-side faults, thus fulfilling the grid code requirements. The multi-functional inverter uses a finite-state machine (FSM), which manages a seamless mode switching from normal-to-LVRT, normal-to-LiR, and faulty-to-normal modes.

The design approach uses a relative stability analysis via bode plots for each inverter stage. Section I of the paper introduces the effects of AC/DC faults on the PV inverters and proposes a novel fault-ride-through solution. Section II presents the mathematical analysis of power balance at the DC-link during the DC and AC-side faults. Section III presents the proposed hybrid PV-battery inverter along with its stability analysis. Section IV presents the experimental results, comparison, and validation. Finally, section V concludes the paper by highlighting the contribution and significance of the present work.

II. METHODOLOGY

A. POWER IMBALANCE DURING DC-SIDE FAULTS

The intermittent nature of PV sources results in varying output yield, leading to DC-side faults[28]. The irradiance can rapidly fluctuate within a few seconds, which causes power imbalance and flickering output[21]. The maximum power available at the input is P_{MPPT}. The inverter is feeding the grid with P_{INV}. The power consumed to maintain the DC link is $P_{DC\text{-}Link}$, and the losses are P_{Losses}. The reduced power yield due to DC-faults is denoted as P_{LP}. As the input current drops considerably in low irradiance, it causes a drip in the DC-link voltage, and the inverter becomes vulnerable to under-voltage shutdown. The reduced power can be related to a ratio of available power to nominal power denoted as k_{LP}. The reduced power during low-irradiation can be related as $P_{LP}=P_{MPPT}$ -$k_{LP}P_{MPPT}$. Therefore, (5-7) express the input to output power balance during low irradiation DC-faults.

$$P_{LP}=P_{INV}+P_{DC-Link}+P_{losses} \quad (5)$$

$$P_{MPPT}(1-k_{LP}) = P_{INV}+P_{DC-Link}+P_{losses} \quad (6)$$

$$P_{MPPT}=P_{INV}+P_{DC-Link}+P_{losses}+ k_{LP}P_{MPPT} \quad (7)$$

Comparing (2) and (7), we can say that, in order to maintain the DC-link power balance the inverter must also reduce its output power equivalent to ($P_c = k_{LP}P_{MPPT}$). The reduced output power injection into the grid is the cause of grid voltage flickers. The only way to avoid grid flickering is by maintaining the constant power output (CPO). The

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CPO is realizable when an additional energy source provides the compensating power ($P_c = k_{LP}P_{MPPT}$) during the low irradiation conditions[24].

B. POWER IMBALANCE DURING AC-SIDE FAULTS

The grid-voltage sag reduces the inverter output power, which also results in the DC-link power imbalance[29]. The grid sag-gain k_g is the ratio of instantaneous grid voltage V_g to the normal grid voltage V_n represented in (8).

$$k_g=\frac{V_g}{V_n} \tag{8}$$

The sag reduces the inverter power output, leading to a change in power balance at the DC-link, depicted in (9) and (10), where P'_{INV} is the reduced output power of the inverter during a sag.

$$P_{MPPT}=P_{INV}(1-\frac{V_g}{V_n})+P_{DC-Link}+P_{losses} \tag{9}$$

$$P_{MPPT}=P'_{INV}+P_{DC-Link}+P_{losses} \tag{10}$$

Equations 10 shows that the inverter can only consume limited power because of sagging grid voltage, even though the 1st stage of the boost converter has full PV power available. In this condition, if the input power is not reduced, the PV inverter will have extra energy, which will be dumped into its DC-link. The extra energy will surge the DC-link voltage and trigger the overvoltage protection. Therefore, the input power must be curtailed, equivalent to the reduced output power. The reduced harvesting of input PV power ensures the power balance and prevent the DC-link voltage surge, as depicted in (11).

$$P_{MPPT}-P_{INV}(\frac{V_g}{V_n})=P_{INV}(1-\frac{V_g}{V_n})+P_{DC-Link}+P_{losses} \tag{11}$$

Most of the LVRT capable PV inverters work in a non-MPPT mode during sags. The control algorithm operates the first stage boost at a pre-defined duty cycle, which can only ride through a particular severity sag. For severer sag, the duty cycle of the boost converter must further be decreased. However, while reducing the duty cycle in severer sag beyond a certain threshold, the boost converter may fall from continuous conduction mode (CCM) into a discontinuous conduction mode (DCM). The DCM cannot provide the necessary voltage boosting function, which may result in DC-link voltage collapse [30]. Eventually, the inverter will trigger the under-voltage shutdown.

CCM to DCM switching may result in unregulated DC-link voltage and ripples, disrupting the control operation[19]. Therefore, instead of disabling the MPPT in sag, it is beneficial to harvest the excess PV energy into a small energy buffer, thus always operating the boost stage in CCM. In this way, the inverter can seamlessly ride-through sag of any severity. The utilization of an energy buffer is even more beneficial when sag is more than 50% of the nominal grid voltage because the grid codes suggest injecting only reactive power in this condition. While injecting only reactive power, an insignificant amount of power is required to maintain the DC link voltage, and some power is dissipated in losses, as shown in (12).

$$P_{MPPT}=0+P_{DC-Link}+P_{losses} \tag{12}$$

Therefore, during severe sags, all the PV power P_{MPPT} is available to be harvested into the battery buffer without causing any instabilities in inverter control, as shown in (13), (14).

$$P_{MPPT}=0+P_{Buffer}+P_{DC-Link}+P_{losses} \tag{13}$$

$$P_{MPPT}\approx P_{Buffer}=P_{INV}(\frac{V_g}{V_n}). \tag{14}$$

In order to visualize the DC-link power imbalance during both AC and DC faults a simulation for a two-stage inverter is presented in Fig. 4. The 800W solar string is an input power source to the inverter. The first stage boost converter works in a CCM and charges the DC link. The duty cycle of the boost stage is directed by the perturb-and-observe (P&O) MPPT algorithm. The DC link is maintained at 380V when the inverter operates at the nominal power output. The inverter stage calculates the output current reference based on the DC-link voltage and the grid phase angle acquired by the phase-locked loop (PLL). In the simulation, a 50% grid-sag appears as an AC fault for 400ms, i.e., from 0.2-0.6s in Figure 4(a).

TABLE I
Simulation parameters.

Description	Symbol	Value
PV input Power	P_{pv}	800W
Boost inductor	L_{Boost}	1.2mH
Buffer inductor	L_{BB}	2mH
DC-Link capacitor	C_{DC}	3300µF
Grid side filter inductor	Lg	0.5mH
Inverter side inductor	L_{inv}	2mH
LCL filter capacitor	C_{LCL}	1.6µF
Nominal grid voltage	Vg	240 V (rms)
Inverter dc link	Vdc	380 V
Nominal grid frequency	fg	50Hz
Switching frequency	fsw	10kHz

Since the grid voltage is reduced, the inverter cannot inject the nominal current into the grid. Alternatively, it is programmed to inject the reactive current as recommended by the grid codes. The current waveform is fifty times (50x) amplified for intuitive visualization in the simulation results, as shown in the zoomed portion 'A' and' B' of Fig.4(a). Table I shows other parameters of the simulation.

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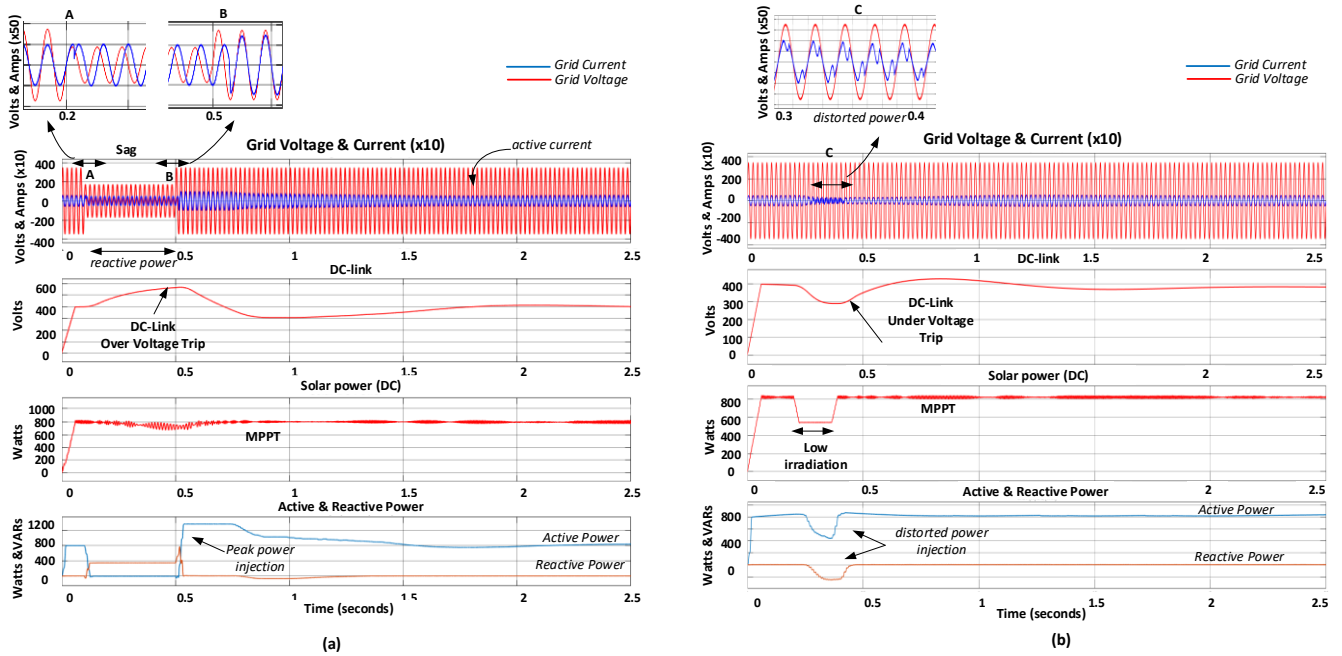

FIGURE 4. Simulation during AC/DC faults: (a) AC sag fault; (b) DC low irradiation fault

The simulation result in Figure 4(a) shows that the inverter output power is reduced during the AC-side fault. Since the MPPT mode is not disabled, the excess energy accumulation in the DC-link results in over-voltage, which can trigger the shutdown protection [7]. In contrast, Figure 4(b) shows the DC-link fault by applying low-irradiation for 100ms, i.e.,0.3-0.4 s in Fig.4(b). The PV power is reduced to 550W, while the DC-link falls below 300V. If the inverter keeps injecting power into the grid, voltage flickers and distorted grid current will be injected, as shown in the zoomed portion 'C' of Figure 4(b). The grid codes do not recommend flickers and distorted power injection into the grid. The low DC-link voltage may lead to shutdown protection as well.

Grid-tied inverters going offline or into shutdown because of AC or DC side faults is not desirable. The AC/DC faults can result in cascaded inverters shut down leading to an overall grid collapse or outage. In the age of renewable energy, grid-connected inverters need to ride through faults to ensure overall grid voltage and frequency regulation. The proposed control will provide nominal power to the grid in normal conditions and remain connected to the grid in faulty conditions while ensuring the inverter's safety and grid-codes regulations. Equation (15) relates the amount of reactive power that needs to be injected by individual power generating unit[1].

$$\begin{cases} I_q = 0 & 0.9 < v_{p.u.} < 1.0 \\ I_q = k\left(1 - v_{p.u.}\right) I_n & 0.5 < v_{p.u.} < 0.9 \\ I_q = I_n & 0.0 < v_{p.u.} < 0.5 \end{cases} \quad (15)$$

Where I_q is the reactive current to be injected, I_n is the nominal current, v_{pu} is the instantaneous per unit grid voltage, and k is the constant defined by the specific grid code, it is the measure of the grid weakness at the location of the generating unit. Many grid codes define $k=2p.u$.

III.PROPOSED PV-BATTERY HYBRID INVERTER

A. STRUCTURE

The proposed fault ride-through inverter topology and control loop is shown in Fig.5. Four 200W PV panels are connected in series to form a string configuration. The system comprises an input boost stage, an intermediate battery buffer stage, and the output inverter stage. During normal operation, the buffer stage remains idle, and the inverter injects the active power into the grid in proportion to the DC-link voltage. The boost converter tracks the PV string maximum power point and maintains the nominal DC-link (380V) to inject the nominal power (800W) into the grid. The boost inductance and output capacitor are selected for CCM as presented in [5, 19, 31]. A DC-link capacitor provides the decoupling between DC and AC stages. The second stage forms a simple H-bridge inverter topology, interfaced to the grid via an LCL filter.

B. OPERATION DURING SAG AND LOW IRRADIATION

The bidirectional buffer stage has two switches, an inductor, and a battery. The buffer charges or discharges the DC-link according to the relevant mode of operation. When the inverter detects the grid sag, the buffer stage buck mode is activated to absorb the excess energy by keeping the *Q3* Off while modulating only *Q2*. In contrast, boost mode is enabled when the input PV power is reduced significantly because of rapid low-irradiation. In this case, the buffer only modulates *Q3* and keeps *Q2* Off. The proposed PV inverter

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seamlessly ride-through AC sags and DC low-irradiation (LiR) effects. The inverter is programmed to inject reactive power during sags, which consume insignificant energy. Therefore, all the power from the PV source is available to charge the battery. Unlike other LVRT techniques, the proposed LVRT method does not disable the MPPT; rather, it harvests the PV energy into the battery. The main advantage of this method is that the inverter can ride through sags of any intensity. On the other hand, during rapid irradiance fluctuations, the battery buffer is utilized to provide the constant power output, which reduces the grid voltage flickering.

The system is controlled via a finite-state machine, where the AC sags and DC-low irradiation detectors are implemented. Grid-sags are detected by average grid voltage, while low-irradiation is detected by tracking a significant change in the input current from the PV source. Perturb and observe (P&O) MPPT algorithm keep working in the normal, low-irradiation, and grid sagging conditions. The control strategy also capped the output current during the sags to prevent the over-current shutdown. The output current is synchronized to the grid via SOGI phase-locked-loop (PLL). For sags $0.5< v_{p.u.}<0.9$, the phase angle Θ needs to be calculated so that both active and reactive power is injected simultaneously. The direct and quadrature component of the current (I_d *and* I_q) are used to calculate the phase angle Θ, as related by (16) [2, 4, 10].

$$I_d = I_n.\cos(\theta)$$
$$I_q = I_n.\sin(\theta)$$
$$\theta = \sin^{-1}\left(\frac{I_q}{I_n}\right) \quad (16)$$

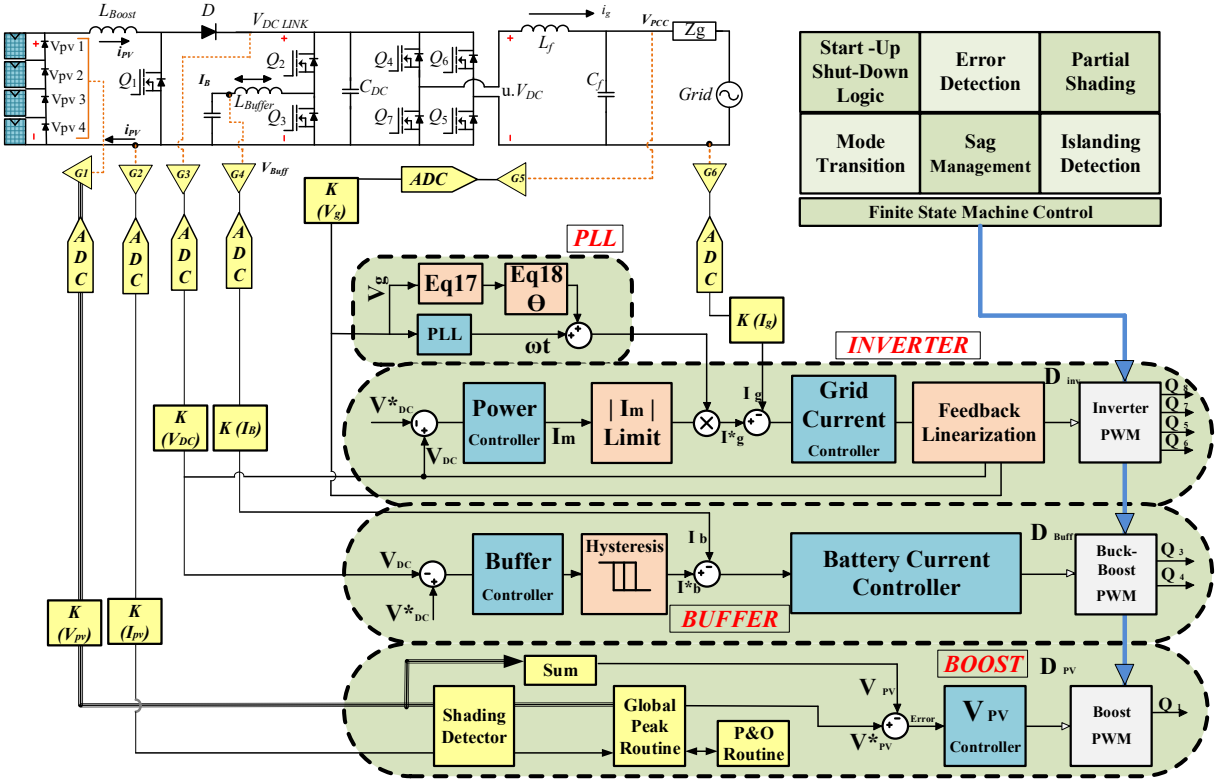

FIGURE 5. **Proposed fault ride-through control system**

The current controller comprises a Type-II (3-pole 3-zero (3P3Z)) control with feed-forward linearization. The developed PV-inverter distinct features are (1) The DC-link remains unaffected during grid sags of any intensity. At the same time, the intermediate energy buffer harvests the excess energy to enable a low-voltage ride-through with reactive power support. (2) As soon as the low irradiation is detected, the battery buffer ensures that the DC-link maintains its nominal voltage. Thus, the inverter keeps injecting the constant power output. (3) The MPPT remains enabled in normal, LVRT, and low irradiation conditions.

C. STABILITY ANALYSIS

The proposed strategy controls the PV-battery inverter in a modular fashion: The stability margins of every stage of the inverter are determined by the frequency analysis of the loop gain. Then, a suitable controller is selected to shape the loop gain and phase for attaining the desired performance. Finally, the design parameters of the phase-locked loop (PLL) are configured by the time-domain analysis.

1) BOOST CONTROL LOOP

The frequency analysis of the first stage boost converter is conducted by considering the inverter stage as a load [30]. A small-signal transfer function of output-voltage to duty-cycle $\frac{\hat{v}_o}{\hat{d}}$ of the boost-stage is derived as (19) [30].

$$\frac{\hat{v}_o}{\hat{d}} = G_{do}\frac{\left(1+\frac{s}{\omega_{esr}}\right)\left(1+\frac{s}{\omega_{rhp}}\right)}{\left(1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o{}^2}\right)} \quad (17)$$

Equation 17 shows the output voltage to the duty transfer function of a first-stage boost converter. Where $\hat{v}_o$ is the small-signal output voltage, $\hat{d}$ is the small-signal duty cycle, and $G_{do}$is the DC gain. $\omega_{esr}$is the frequency at which zero occurs due to equivalent series resistance (ESR) of the inductor, ω_{rhp} is the frequency at which right half plane zero occurs, $\omega_o$is the resonant frequency, and Q is the quality factor. Given the duty cycle D, $D' = D - 1$, the resistance of inductor L_{Boost} is rl and the on-resistance of switch $Q1$ is r_{on} . We can relate the total resistance to charge the inductor as $rl' = rl + r_{on}$. The DC gain can be derived as G_{do} in (18).

$$G_{do} = V_{in}\left[\frac{R(R(D'^2 - rl'))}{(RD'^2 + rl')(RD'^2 + rl + rcD')}\right] \quad (18)$$

With load "R", boost inductor "L" and output capacitor "C", the resonant frequency ω_o and quality factor Q are given in (19) and (20) respectively:

$$\omega_o = \sqrt{\frac{RD'^2 + D'rc + rl'}{C*L*R}} \quad (19)$$

$$Q = \frac{\omega_o}{\frac{1}{C*R} + \frac{rl + rcD'}{L}} \quad (20)$$

The frequency of right half plane zero and ESR zero are expressed in (21) and (22)

$$\omega_{rhp} = \frac{RD'^2 - rl}{L} \quad (21)$$

$$\omega_{ESR} = \frac{1}{C*rc} \quad (22)$$

The presence of the RHP zero in the boost transfer function poses a challenging task for controller design. During the output voltage control mode, a demand for more output will increase the duty cycle. Thus, the switch needs to turn on for longer time, so the output voltage drops initially before catching up to the demanded output[19]. Therefore, the close-loop control bandwidth should be less than RHP-zero. On the other hand, a voltage control loop with a high crossover frequency ensures a fast-dynamic response. A Type-II compensator with a pole-zero placement method attains the desired stability margins. The boost converter is designed to operate at the maximum power point in CCM mode using the procedure in references[19, 30]. Critical inductance, output capacitor, duty cycle, current ripple, and other boost controller parameters are shown in Table II.

TABLE II
Boost stage design parameters.

Description	Symbol	Value
Rated Power	P	800W
Load R	R	160 Ω
Critical Inductance	L	1mH
Duty cycle D	D	0.7
Inductor impedance	rl	1mΩ
Output Capacitor	C	3300.uF
Switch resistance	r_{on}	3mΩ
Capacitor impedance	rc	0.01mΩ
Output Voltage	Vout	380V

The open-loop frequency response of a boost converter (blue line) in Fig.6(a) shows a good DC gain at low frequencies, followed by a resonant peak because of complex poles. A -40dB/decade roll-off follows the resonant peak at 800Hz, which is due to a right-half-plane zero (RHP) at 2.3kHz. The phase plot shows a corresponding phase-lag and a 90° dip due to the RHP zero. An ESR zero also introduces the phase-lead after the gain cross-over frequency at 40 kHz. The compensator for this plant should have a high cross-over frequency and a minimum gain-margin and phase-margin of -20dB, 45°, respectively. A3P3Z controller can provide the desired gain and phase margins by considering three poles and two zeros. Equation (23) shows the structure of the 3P3Z controller:

$$H_c(s) = \frac{K_{DC}(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{\frac{s}{\omega_{p1}}(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})} \quad (23)$$

The zeros are placed at resonant frequency(800Hz), while the integrator is placed at the origin. The closed-loop system has a high gain and a bandwidth of 279Hz with an overdamped response. An underdamped system with a relatively higher bandwidth could also be achieved, but the resonant peak may still appear in the compensated system. Therefore, the achieved overdamped response is agreeable for the system. The second pole is placed precisely at RHP zero(2.3kHz). The remaining pole is placed at half of the switching frequency(10kHz) to have better noise immunity. Fig.6(b) shows the closed-loop step response of the designed boost converter with a rise time of 1ms and a settling time of 2.5ms.

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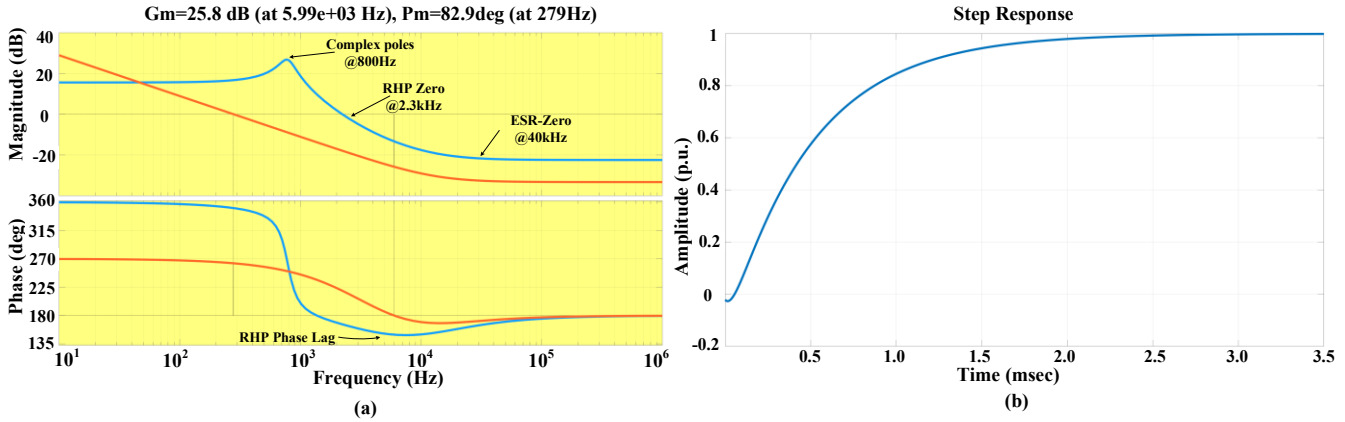

FIGURE 6. Controller design for boost stage: (a) Frequency response; (b) Step response

The PV string terminal voltage is 210V, and its MPP is at 160V. The designed boost provides the 380V DC-link voltage at MPP. The CCM mode is maintained by choosing the boost inductor greater than the critical inductance. The stability and rapid MPPT are ensured by verifying that the rise-time and settling-time are within 1ms. A classical perturb & observe(P&O) MPPT algorithm provides the reference PV voltage V^*_{pv}. The difference between the reference and feedback PV-voltage generates the boost converter's duty cycle, as depicted in Fig.7.

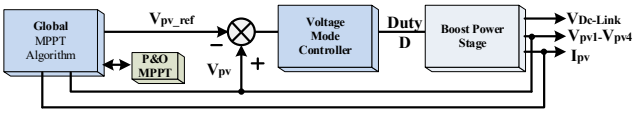

FIGURE 7. Integration of MPPT and boost-stage controller.

The PV inverter provides the nominal output current at a nominal DC-link voltage. The output current rises in proportion to the DC-link voltage and vice versa. The DC-link is designed to fluctuate in a very narrow range in normal operating conditions. The finite state machine continuously monitors the DC-link voltage and shut-down the inverter if the DC-link voltage exceeds the safety limits of 500V. Moreover, the inverter must limit the output current during a grid sag despite higher voltages at the DC-link. Therefore, the calculated reference current is capped at the maximum value in the current control loop.

2) PHASE LOCKED LOOP (PLL)

A phase-locked loop synchronizes the output voltage to the grid. A PLL consists of three parts indicated in Fig.8. First, a second-order generalized integrator (SOGI-PLL)[32] generates the orthogonal signals, which are transformed to direct and quadrature components to detect the phase error, as shown in Fig.8. After filtering the phase error, the nominal angular frequency *"ω_o"* is added and integrated to obtain the grid phase angle *"Θ"*.

Given the grid voltage V_g, the SOGI and DQ transformation provides the direct and quadrature components shown in (24) and (25):

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = V_g \begin{bmatrix} \cos\theta_{pll} & \sin\theta_{pll} \\ -\sin\theta_{pll} & \cos\theta_{pll} \end{bmatrix} \begin{bmatrix} cos\ \theta_g \\ sin\ \theta_g \end{bmatrix} \tag{24}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = V_g \begin{bmatrix} co\,s(\theta_{pll} - \theta_g) \\ sin\,(\theta_{pll} - \theta_{g)} \end{bmatrix} \tag{25}$$

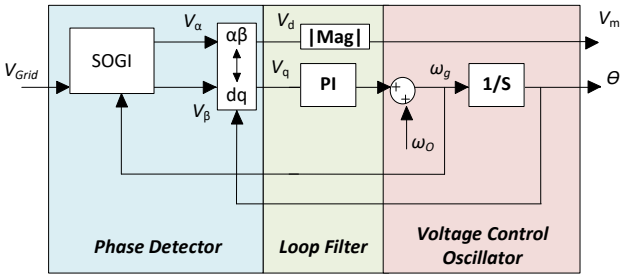

FIGURE 8. Operational Block diagram of PLL

Upon reaching a phase-locking condition, when $(\theta_{pll} - \theta_g)$ is very small the phase angle is passed to the loop filter (LP) made of a PI-controller given by (26).

$$LF = K_{p+}\frac{K_i}{s} \tag{26}$$

The PLL's output can be expressed as a second-order system and efficiently designed by defining the damping ratio δ, settling time t, and natural frequency ω_n. The output-phase angle (θ_{pll}) to input-phase angle(θ_g) transfer function of a PLL can be derived as in (27) and (28) [32], where T_s is the sampling time.

$$\frac{\theta_{pll}}{\theta_g} = \frac{LF*1/s}{1+LF*1/s} = \frac{sK_p + K_p/T_s}{s^2+sK_p+K_p/T_s} \tag{27}$$

$$\frac{\theta_{pll}}{\theta_g} = \frac{sK_{p+}K_i}{s^2+sK_p+K_i} \tag{28}$$

As shown in Fig.8, SOGI-PLL provides the grid voltage locked phase angle "θ_{pll}", which is used to generate the reference current for the inverter. However, during sag as additional phase angle "θ_{sag}" is added to "θ_{pll}" to provide the grid code compliant reactive power. To find the optimal PLL

gains "K_p" and "K_i", we compare (28) to the 2nd order transfer-function of (29).

$$T.F = \frac{2\delta\omega_n s+\omega_n^2}{s^2+2\delta\omega_n s+\omega_n^2} \tag{29}$$

The comparison provides "$\omega_n = \sqrt{\frac{K_p}{T_s}}$ "and damping ratio $\delta = \sqrt{\frac{T_s K_p}{4}}$. The time domain solution of (29) can be expressed in (30). Also, for compact mathematical representation we have defined $\sigma = \delta\omega_n$, $\omega_d = \sqrt{1-\delta^2\omega_n}$ and $c = \omega_n/\omega_d$

$$y(t) = 1 - c\, e^{-\sigma t}\sin(\omega_d t + \varphi) \tag{30}$$

where the error band is "Θ" and settling time "t.

$$t = \frac{1}{\sigma}\ln(\frac{c}{\theta}) \tag{31}$$

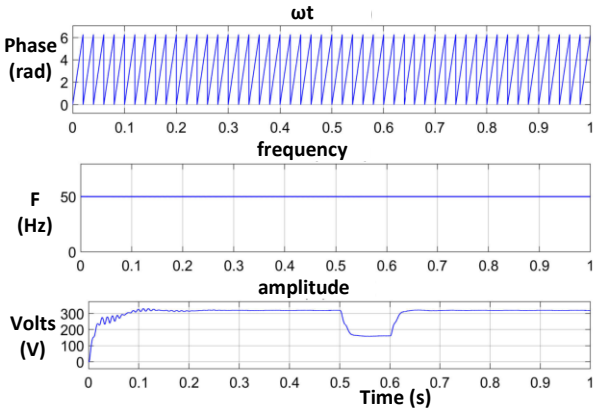

FIGURE 9. Simulation of PLL in sag

By setting the performance parameters in damping ratio δ, the settling time t, and the error-band "Θ", the PLL -gains *"K_p"* and *"K_i"* can be easily calculated. A simulation of SOGI-PLL with t=10ms settling time, damping ratio δ *=0.7*, and error-band *Θ=5%* is presented in Fig.9. A single-phase 50Hz sinusoidal signal with a peak value of 320V is the input signal for the PLL unit. Fig.9 shows the estimated phase, frequency, and amplitude. A 50% sag is generated from 0.5s to 0.6s. It is observed that the PLL remains stable during the sag and estimates the angular frequency accurately.

3) INVERTER CONTROL LOOP

The inverter stage is operated at high-frequency which produces higher-order harmonics in the output current. The higher-order harmonics are filtered by a low pass LCL filter to obtain a sinusoidal AC, as shown in Fig.10. The LCL filter designed in [33] is utilized for the proposed inverter. Where V_g is the grid voltage, V_{inv} shows high-frequency inverter output voltage, Z_{inv} is the inverter side impedance, Z_c is the capacitor branch impedance, and Z_g is the grid side impedance

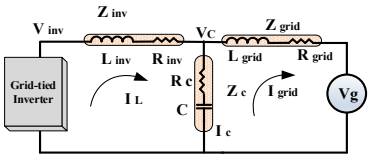

FIGURE 10. Inverter grid interface

A basic circuit analysis leads to (32). Now considering the inverter output voltage as a function of DC-link voltage and the duty cycle, we can write (33).

$$\frac{i_g}{v_{inv}} = \frac{Z_c+Z_g}{Z_{inv}(Z_c+Z_g)+Z_c Z_g} \tag{32}$$

$$G_{LCL} = \frac{i_g}{d} = \frac{V_{DC}(Z_c+Z_g)}{Z_{inv}(Z_c+Z_g)+Z_c Z_g} \tag{33}$$

Although (33) seems independent of grid voltage V_g. However, the studies [13, 34] show that the grid voltage Vg implicitly affects the current loop, creating a hidden impedance path. So, when the inverter is controlled by a classical integrator-based controller (PI, Type-I, or Type-II), it fails to attain the zero steady-state error. Therefore, the authors in the reference [13] have proposed a feed-forward grid voltage rejection method to avoid the effect of grid voltage V_g, by including a feed-forward compensator C_z in series with the current controller. The feed-forward linearization removes the steady-state error during sinusoidal reference tracking and improves the current control loop dynamics, as expressed in (34).

$$C_z = \frac{k}{V_{DC}} \tag{34}$$

Where k is the constant derived from the PWM gain of the H-bridge inverter for bipolar modulation scheme[13], we have integrated the feed forward block C_z of study[13] in the proposed inverter current control loop. Now defining the current sensor gain H_i, the loop gain for the current control loop is expressed as (35):

$$loopGain_i = C_i H_i G_{lcl} \tag{35}$$

An overall control diagram of a proposed two-stage inverter is shown in Fig.10[13]. Where the red trace shows the implicit addition of grid voltage disturbance and the blue trace shows the feed-forward compensation along with C_z block. The gain k_g represents the ratio of instantaneous grid voltage to the nominal grid voltage $k_g = V_g / V_n$. k_g is the measure of severity of the sag.

A pole-zero placement method is used for the current compensator C_i design. The desirable features are high gain at the fundamental frequency and a reasonable stability margin. Table III shows the frequency analysis parameters. Fig.12(a) blue trace shows the uncompensated bode-plots for a loop-gain of (35). A compensator is desired to shape the gain-plot with -40dB attenuation at the switching frequency in order to reduce the output current harmonics. The Type -II controller expressed in (36) is used for C_i design.

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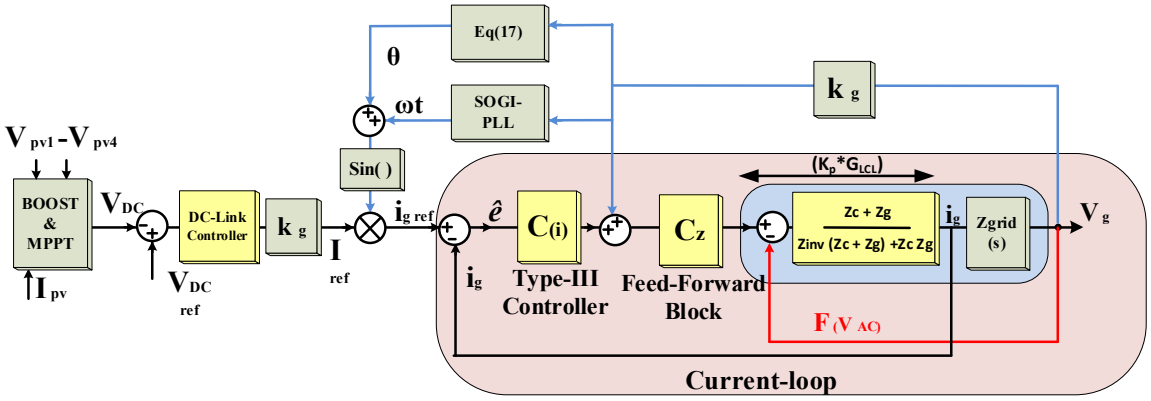

FIGURE 11. Current loop control with feed forward linearization[13]

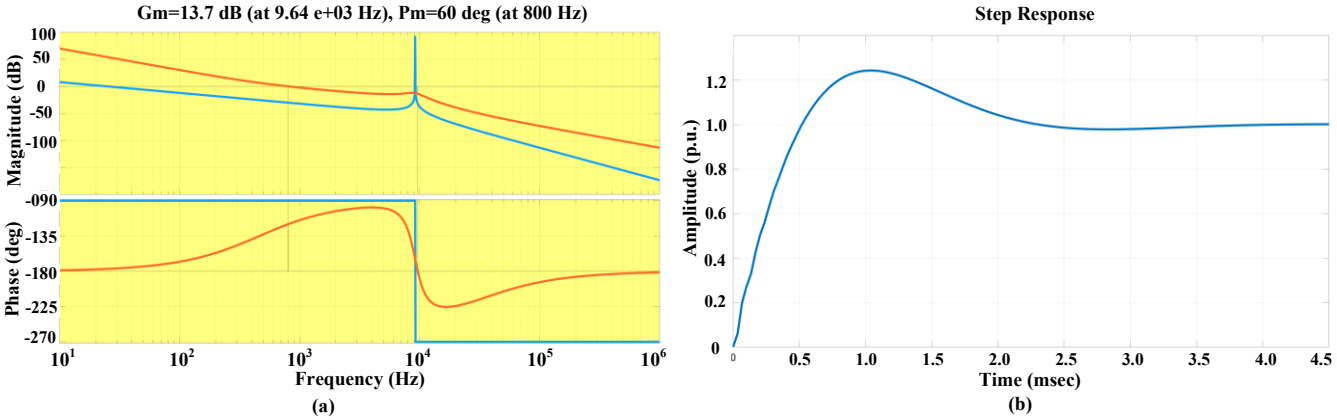

FIGURE 12. Controller design for inverter stage: (a) Frequency response; (b) Step response

TABLE III
Inverter stage design parameters

Description	Symbol	Value
Rated Power	P	800W
Inverter Impedance Zinv	Linv, Rinv,	3mH, 1mΩ
Grid Impedance Zg	Lg, Rg	0.5mH, 0.01mΩ
Capacitor Cc	C	1.2uF
Duty cycle d	d	0.5
DC Voltage	VDC	400V

$$H_{3P3Z}(s) = \frac{K_{DC}(1+\frac{s}{\omega_{Z1}})(1+\frac{s}{\omega_{Z2}})}{\frac{s}{\omega_{p1}}(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})} \quad (36)$$

An integrator compensates for the error at low frequencies and provides infinite gain at the DC. The complex zeros will dampen the resonant peak at 8kHz. Finally, the two-poles after the gain cross-over frequency reject the high-frequency noise. The bandwidth should be at least ten times the fundamental frequency, i.e., 10 * 50 ≥ 500Hz. A 3-pole 3-zero, Type II compensator can shape the desired frequency response. Figure 12(a) shows the compensated system (red-trace) with the 3P3Z compensator. A reasonable phase margin of 60 degrees a gain margin of 13.7 dB ensures stability. Fig.12(b) presents the step response of the close loop compensated plant. The overshoot due to the LCL filter's resonance is under 25% and a settling time of 3.5ms. The closed-loop systems show good transient response with 800Hz bandwidth.

4) BUFFER STAGE CONTROL LOOP

The bi-directional DC-DC converter is interfaced to the DC-link to absorb the excess power in sags and provide the energy deficit during low-irradiance conditions. Fig.13 shows the bidirectional converter with buck-boost topology attached to the DC-link. When the DC-link surges and exceeds the upper threshold voltage, the finite state machine (FSM) controller activates the battery charging during the grid sags. Buck operation of the buffer-stage accomplishes the charging mode, i.e., turning off Q3 and switching Q2. Alternatively, the FSM initiates the battery discharging during low irradiation (LiR) since the DC-link drops beneath the lower threshold voltage. Boost operation of the buffer-stage accomplishes the discharging mode, i.e., turning off Q2

and modulating Q3 as shown in circuit topology of Fig.13[31, 35].

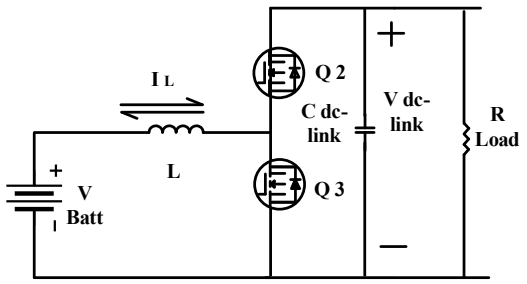

FIGURE 13. Buffer stage topology

The bi-directional buffer can work in both buck and boost modes. The average current of the battery buffer is controlled with dual cascade-control, the outer voltage loop and the inner current loop. A cascaded controller's outer voltage loop provides the reference current for the high bandwidth inner current-control loop. The current-loop derives the PWM block of the buck-boost stage, as shown in Fig.14. The small-signal transfer function of (37) relates the battery current i_b to the duty cycle d_b [31, 35].

$$G_{di} = \frac{i_b}{d_b} = V_{DC}\left[\frac{(sC+\frac{2}{R})}{(s^2LC+s\frac{L}{R}+D_b{}'^2)}\right] \quad (37)$$

Where L is the minimum inductance for CCM mode, C is the output capacitor, R is the nominal load, D_b is the duty cycle and $D_b{}'=(1-D_b)$. Considering the modulation gain K_{PWM}, the loop gain for the current-loop is expressed in (38):

$$Gain_i = C_i K_{pwm} G_{di} \quad (38)$$

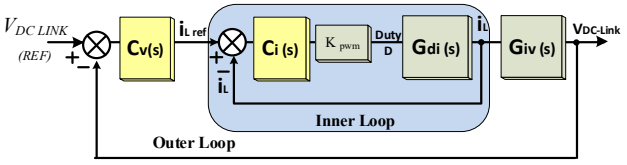

FIGURE 14. Dual loop buffer stage control

TABLE IV

Inverter stage design parameters

Description	Symbol	Value
Rated Power	P	800W
Buffer Inductor	L	3mH
Capacitor Cc	Cdc-link	3300uF
Duty cycle	Db	0.6
DC Voltage	VDC	400V
Load	R	160Ω

The current compensator regulates the battery current at the reference value (5A). The frequency-analysis parameters for the buffer stage are given in Table IV. The uncompensated open-loop bode plot (Blue) of the system is shown in Fig.15(a). A compensator is desired to shape the gain plot to have a -40dB attenuation at the switching frequency, thus reducing the output current harmonics. The compensator should subdue the resonant peak at 350Hz with complex zeros, and the two-poles should be placed after the gain cross-over frequency to reject the high-frequency noise. The bandwidth of the internal current loop should be at least 2.5kHz to ensure the inner loop's fast transient response.

A 3P3Z Type-II compensator is an excellent option to achieve the desired stability margins. The current-loop frequency response of compensated (red) and uncompensated (blue) trace is shown in Fig.15(a). The compensated response shows a bandwidth of 2.75KHz with a reasonable phase margin of 56.2 Degrees. The closed-loop gain of the internal current loop is expressed as $G_{CL,i}$ in (39). The step response of $G_{CL,i}$ has a rise time of 0.1ms and a settling time of 0.3ms, and less than 20% overshoot, as shown in Fig.15(b).

$$G_{CL,i} = \frac{C_i K_{pwm} G_{di}}{1+C_i K_{pwm} G_{di}} \quad (39)$$

The small-signal transfer function $G_{iv}(s)$ relating the DC-link voltage "v_{dc}" and the battery current "i_b" is presented in (40) [31, 35].

$$G_{iv}(s) = \frac{v_{dc}}{i_b} = D_b{}'\left[\frac{(1-\frac{sL}{RD_b{}'^2})}{sC+\frac{2}{R}}\right] \quad (40)$$

The inner current-loop influences the stability of the outer voltage loop. Therefore, the outer-loop (G_{iv}) plant dynamics must also account for the inner closed-loop dynamics $G_{CL,i}$. The loop gain and Bode analysis for the voltage-loop is conducted for $[G_{CL,i} * G_{iv}]$. The blue trace in Fig.16(a) shows the uncompensated loop gain of $[G_{CL,i} * G_{iv}]$. The frequency response shows that the system is inherently stable in terms of gain margin and phase margin; however, a compensator is required to reduce the bandwidth relative to the inner current control loop.

$$G_{CL,v} = \frac{C_v\left(\frac{C_i K_{pwm} G_{di}}{1+C_i K_{pwm} G_{di}}\right) G_{di}}{1+C_v\left(\frac{C_i K_{pwm} G_{di}}{1+C_i K_{pwm} G_{di}}\right) G_{di}} \quad (41)$$

A PID controller is suitable for achieving reasonable stability margins for the voltage loop. The compensated plant $\left[C_v * \left[G_{CL,i} * G_{iv}\right]\right]$ bode plot is shown in red trace in Fig. 16(a). The PID controller provides a reasonable GM of 36.6dB and a PM of 97 degrees. The controller also satisfies the design criteria for the outer voltage loop with a bandwidth around 218Hz. The closed-loop gain $G_{CL,v}$ of the overall dual loop system is expressed in (41), and the step response is plotted in Fig.16(b).

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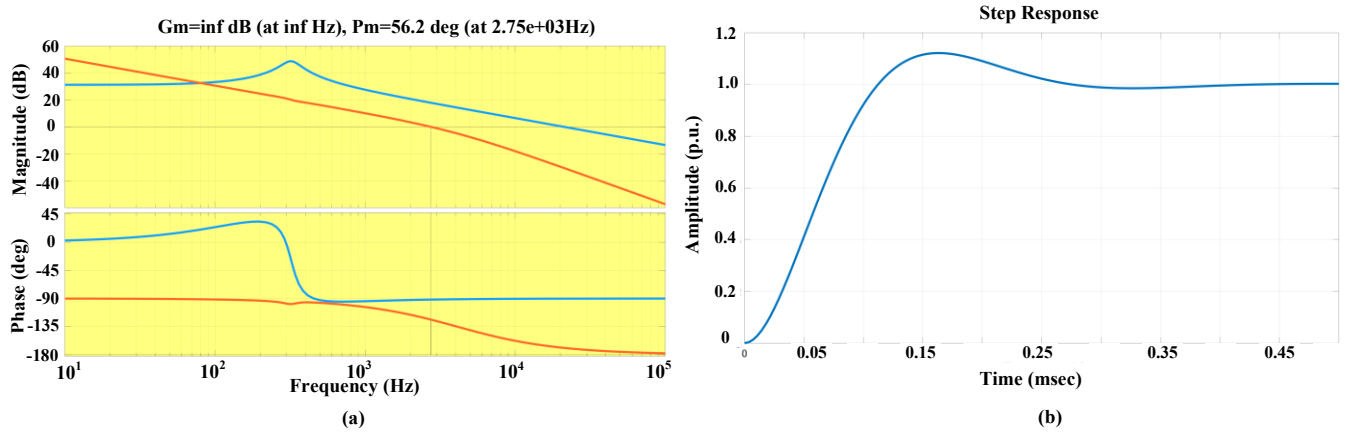

FIGURE 15. Controller design for buffer stage inner current loop: (a) Frequency response; (b) Step response

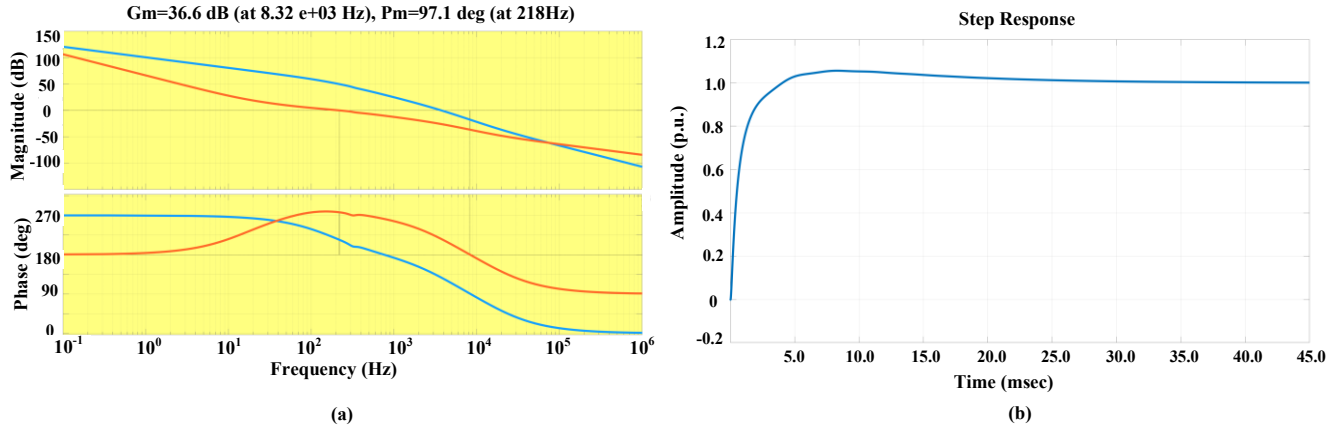

FIGURE 16. Controller design for buffer stage outer voltage loop: (a) Frequency response; (b) Step response

D. CONTROL ALGORITHM

Fig.17 shows the operational logic of the proposed control system, which requires simultaneous implementation of closed-loop controllers of all three stages. Mode transitioning is critical to the overall operation; therefore, the PWM switching frequency of all the stages is synchronized to execute the controller instances simultaneously. As soon as the inverter starts, the finite state machine selects the operating mode and checks the terminal conditions at the input PV and the output grid sides. In case of abnormal PV voltage or grid voltage, the inverter remains in the standby state and shows an error flag. It is crucial to detect abnormal conditions at every switching instant to prevent damage to the inverter. The DC-link voltage is initially built at a fixed duty cycle until it reaches the nominal value. At this instant, the MPPT algorithm provides the duty ratio of the boost stage. A Type II controller compensates for the difference between the reference PV and actual PV voltage, which drives the boost PWM. On attaining the nominal DC-link voltage, the state machine starts modulating the inverter stage. The output reference current amplitude is proportional to the DC-link voltage, while PLL generates the phase angle. The Type III compensator and the feed-forward linearization compensate for the difference between the reference current and the actual grid current to generate the PWM for the inverter stage.

The inverter continuously monitors the grid voltage RMS value to detect the sag. The RMS value is updated every 10ms. The inverter output current is calculated from DC-link voltage in normal conditions. However, if the grid sag is detected, the inverter stage reference current is calculated from (17-18). The phase angle is also appended with the LVRT phase calculated from (18). If the grid voltage drops more than 50% of its nominal value, the inverter only injects the reactive power, thus fulfilling the grid code. It is essential to prevent overvoltage in sags; therefore, the buffer stage is engaged in buck-charging mode to harvest the excess PV energy into the battery. The dual loop controller for the buffer stage explained in section (III.C.4), which regulates the DC-link voltage during the sagging event. When the input PV current drops more than 10% of its nominal value in low irradiation, the buffer mode operates in the boost configuration. Thus, the 1st stage boost converter and the buffer stage boost converter simultaneously charge the DC-link in LiR. Since the 1st-stage boost converter duty cycle is derived from the MPPT module, it does not regulate the DC-link; therefore, the buffer boost converter regulates the DC-link at a nominal value during LiR.

The flow chart in Fig.17 shows the sequence of operations. The firmware of the control system comprises urgent and non-urgent control routines. The analog data acquisition, PWM modules, and feedback controller instances are urgent tasks with the highest execution priority. Therefore, these tasks are implemented in a fast interrupt service routine. On the other hand, non-urgent tasks like MPPT, PLL, and fault detection are executed periodically in timer interrupt routines.

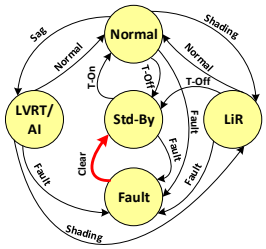

FIGURE 17. Buffer stage topology

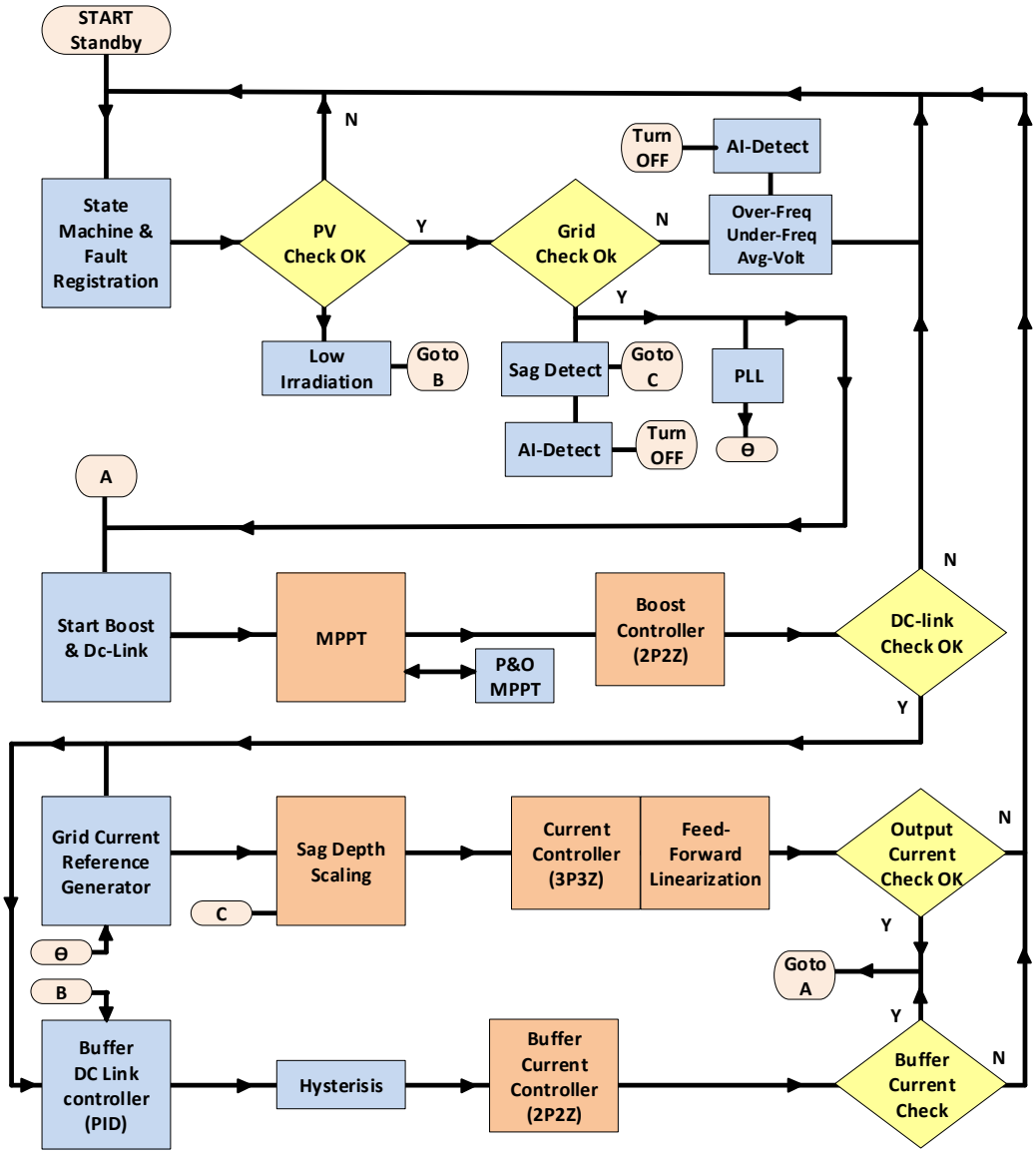

FIGURE 18. Controller logic Flow chart

The PV inverter has five modes Normal, LVRT, Low-irradiation, fault, and standby mode. A finite state machine shown in Fig.18 is implemented to execute the mode transition. Each state of the FSM consists of three subroutines (a) one-time execution subroutine, (b) continuous polling subroutine for fault detection, and (c) condition to switch/exit.

As soon as the inverter is powered up, the inverter detects the input/output terminal conditions, e.g., grid voltage frequency, PV voltage, etc., and the control resides in the "standby" state. The inverter continuously polls for the errors while staying in the "standby" state. When the user turn-on the inverter, the state is switched to a "normal" state, where the boost converter

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charges the DC-link while ensuring the MPPT. The reference current for the inverter stage is calculated from the DC-link voltage and the phase angle from the PLL unit. The "normal" state is terminated either with a sag or low irradiation detection. In the case of sag, the LVRT mode is activated for a maximum duration of 1.5s, the phase angle for inverter reference current is amended with respect to sag intensity. Overvoltage in the DC-link is prevented by diverting the excess energy to the buffer battery. When the inverter detects a drop-in input power, the FSM configures the buffer stage into boost mode to support the DC-link with additional energy. The current injection in LiR mode remains unaltered. The inverter is also equipped with protection in case of any abnormal terminal condition at input/output or the DC-link. An overcurrent/overvoltage at any terminals switches to the "Fault" mode, which disables the PWM, MPPT, and PLL modules and disconnects the inverter from the grid.

IV. RESULTS AND DISCUSSION

An experimental prototype shown in Fig.19 is developed in the laboratory to validate the proposed multi-functional PV grid-tied inverter rated at 800W. The solar string simulator from Chroma provides the 800W input power for the PV-inverter. The simulator emulates the low irradiance conditions via dynamic MPPT mode. The boost stage implements the MPPT and amplifies the PV low voltage to a high-voltage DC-link. The Chroma-6530 programmable grid simulator emulates the grid and generates the grid-sags of variable intensity. The bidirectional buffer stage connects the DC-link and the buffer battery (160V,7AH) to deliver or absorb the power during the faulty conditions. The second stage is a voltage source inverter which injects the AC into the grid via an LCL filter. The control algorithm efficacy is checked by observing the DC-link voltage stability, steady MPPT, DC-link charging during Sags, and flicker-free output in LiR mode. The grid/PV simulator initiates the one-shot measurement for Agilent Oscilloscope and Yokogawa WT500 power analyzer as soon as the AC/DC fault appears. The control algorithm is implemented in a TMS320F28335- digital signal processor. Table V summarizes some experimental parameters.

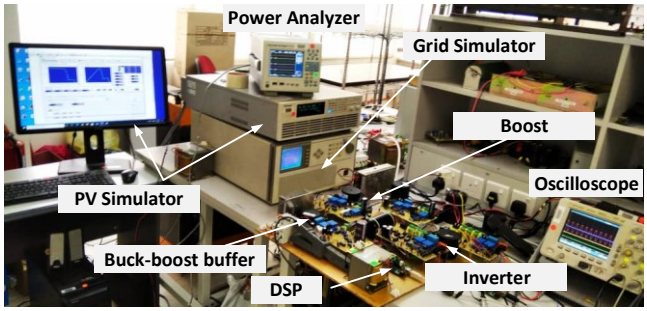

FIGURE 19. Buffer stage topology

TABLE V
Parameters for experimental setup.

Parameters	Values	Parameters	Values
L_{inv}, L_{grid}	3.0 mH	C_f	2.2 µF
$f_{switching}$	20 kHz	f_{grid}	50 Hz
$f_{sampling}$	50kHz	P_{MPP}	800W
$P_{LR,}$	600W	Q_{LVRT}	400 Vars
T_{LVRT} , T_{LR}	1.5s &1.0s	Sag	20%,50%,80%
K_P , K_I (PLL)	166.67, 27755	DC-Link	380 V
$V_{Battery}$	160 V , 7AH	$C_{DC\text{-}link}$	3300 µF

A. AC FAULTS

1) DC-LINK VOLTAGE STABILITY

The DC link is the most critical parameter for the PV inverter's stability in all conditions (Normal, LVRT, and low power modes). The low voltage sag creates an overvoltage at the DC-link while LiR causes Undervoltage. The proposed fault ride-through control manages both sag and LiR faults, as shown in Fig.20(a). In the first experiment, a sag equivalent 0.5 p.u of nominal grid voltage is applied while monitoring the corresponding DC-link voltage. When the sag arrives, the controller connects the buffer stage in buck mode to absorb extra power. A slight jitter in the DC-link voltage is observed on the buffer connection and disconnection as shown in, Fig.20(a-c). The inverter injects reactive power and remains connected with MPPT operation during sags. Once the normal grid voltage is resumed, the LVRT mode is disabled by switching off the buffer stage

2) PV AND BATTERY POWER IN LVRT

The inverter tracks the maximum power point in LVRT, as depicted in Fig.21(a). The inverter keep utilizing the full solar power during sags with (I_{pv}=5.0A, I_{pv}=800W), as shown in Fig.21(a), (b)& (c). The inverter either injects all the available power (800W) into the grid or stores solar energy in a battery buffer. During the sagging event, the boost stage continues its operation at MPP defined by the P&O method. Fig.21(d), (e) &(f) shows the battery buffer charging at 5A (800W) during the LVRT. Since the DC-link voltage is maintained during the AC-fault, the inverter seamlessly injects the reactive power during the sagging event.

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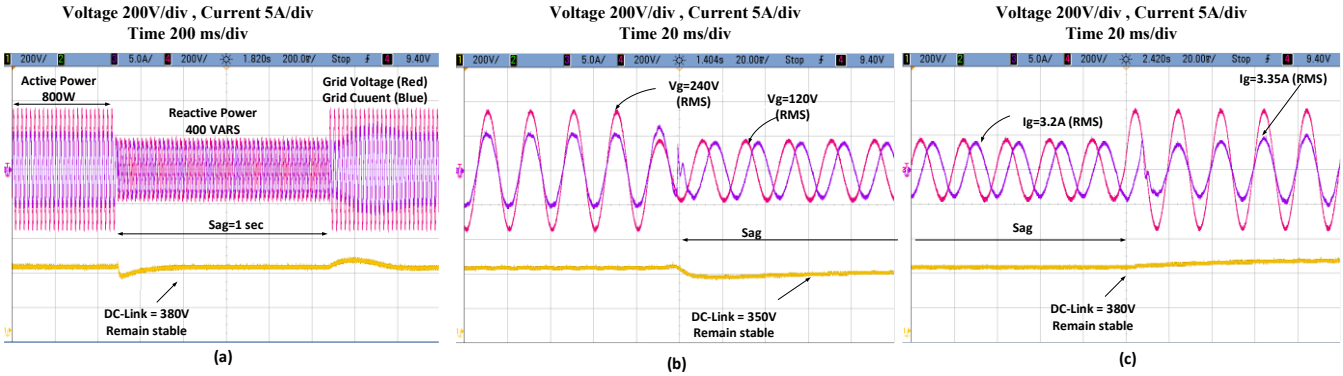

FIGURE 20. DC-link voltage in AC sag: (a) 1s, 50% AC sag ; (b) Sag arrival;(c) Sag departure

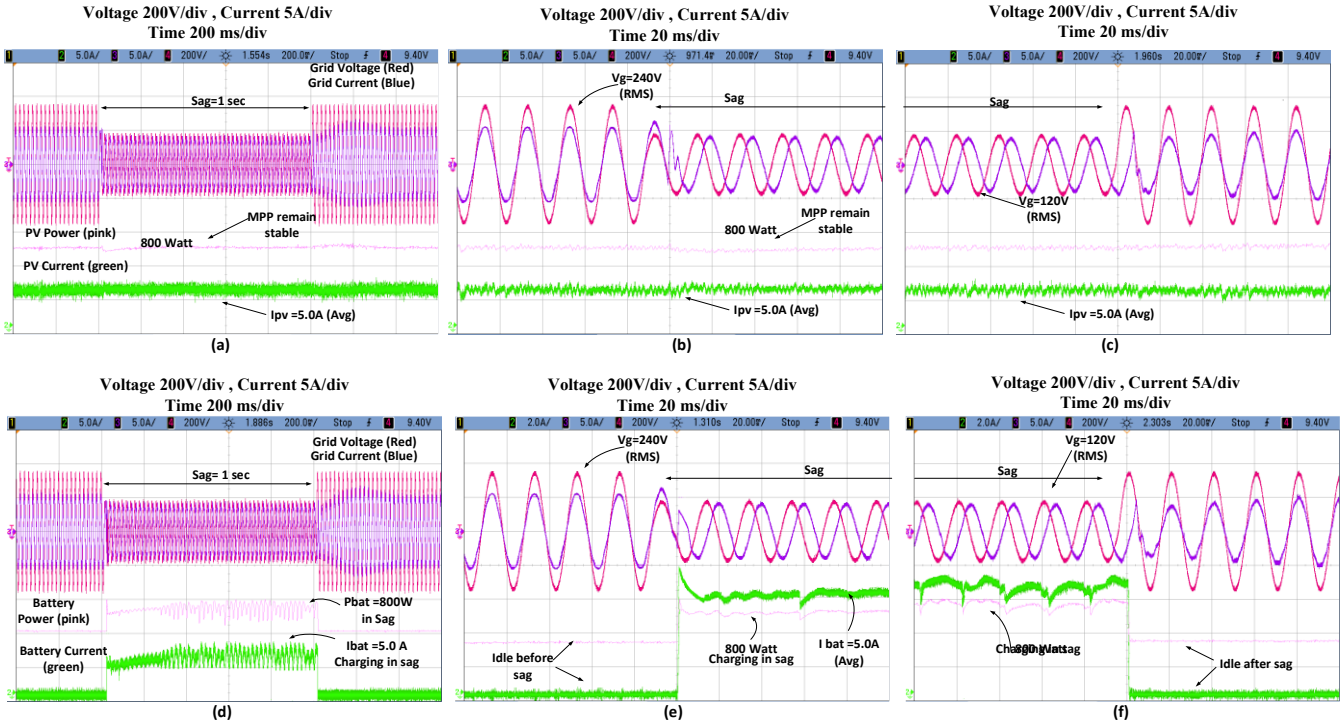

FIGURE 21. PV and battery current in AC sag: (a) 1s, 50% AC sag and PV current; (b) PV current during sag arrival;(c) PV current during sag departure; (d) 1s, 50% AC sag and battery current; (e) Battery current during sag arrival;(f) Battery current during sag departure

3) REACTIVE POWER INJECTION WITH SAGS OF VARIABLE STRENGTH

The proposed PV inverter is tested with sags of variable depths by subjecting it to three consecutive sags with intensities (0.20, 0.50, and 0.80) *p.u.* of the nominal grid voltage. The continuous trace of the power analyzer in Fig. 22(b) shows the grid voltage, current, active and reactive power (V_g , I_g ,P, Q). The reactive power during sags is a function of sag intensity, as calculated from (15-16). Each sag is of 1s duration separated by a normal grid voltage of 1s as well. The inverter worked normally for 5s and then three consecutive sag appears as shown in Fig 21(b).

The inverter harvests the excess DC energy into the battery during sags, as shown in Fig.22(a). At the same time grid code compliant reactive power is injected as shown in Fig.22(b) Some measurements for the multiple sags experiment are summarized in Table VI

TABLE VI
Measurement during sags of variable strength.

Parameters	Values	Parameters	Values
-	240	3.15	800W
20	192	3.15	550W
50	120	3.15	0W
80	50	3.15	0W

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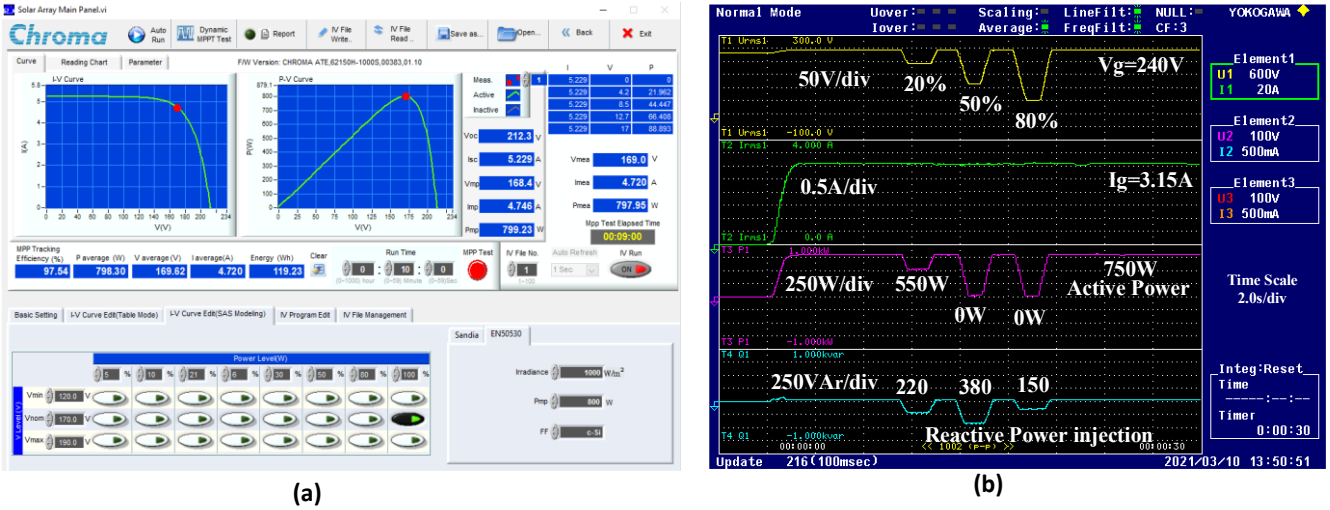

FIGURE 22. **(a)MPPT tracking during sags; (b) Active and reactive power control in sags**

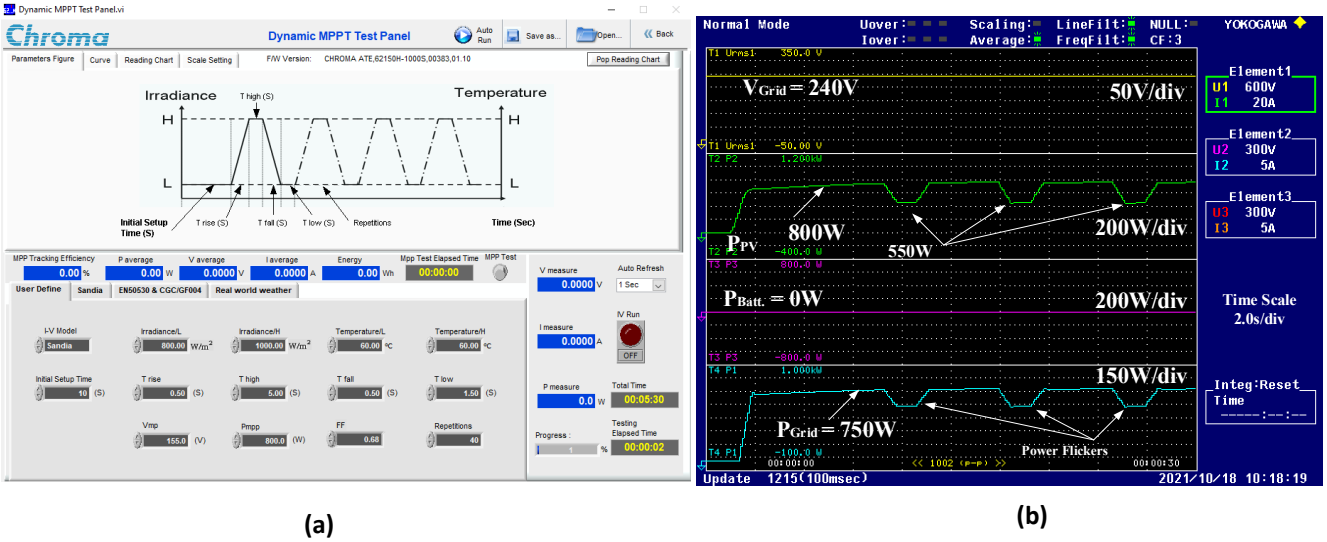

FIGURE 23. **(a) Dynamic MPPT programming ;(b) PV , battery and grid power during low irradiation faults**

B. DC LOW IRRADIATION FAULT RIDE-THROUGH

The natural solar irradiation can fluctuate significantly within seconds, which reduces the input PV power. The DC-link voltage may trigger a shutdown if the inverter keeps injecting nominal power in low irradiation. However, in the conventional two-stage PV inverter, the DC-link voltage must be regulated to generate sinusoidal current. So, when the input power is reduced, the inverter also reduces the output power injection. Although the DC-link voltage remains unchanged but the grid will receive flickering power. Therefore, power flickers must be avoided to attain inverter and grid stability[24]. The actual irradiation data shows that even in fully illuminated solar hours, the irradiation can rapidly fluctuate up to 50% within a few seconds[20, 21]. The dynamic MPPT testing feature of the PV simulator can easily mimic this scenario, as shown in Fig.23(a), where the nominal irradiance can be rapidly stepped down from a high level (H) to a low level (L). The transition times and time to stay in H or L levels can also be programmed. The proposed control strategy should keep the constant power output during low irradiation. In the experiment, the nominal irradiation of 1000W/m^2 is stepped down to 600W/m^2 for 1 s, after every 5s. Firstly, the system is operated without an energy buffer stage to observe the output power fluctuations. Fig.23(b) shows that, as the input PV fluctuates (green trace), the output power injection also fluctuates (blue trace). This kind of input DC disturbance is the cause of the grid voltage flickering.

The voltage flickering can be avoided by leveraging the energy storage buffer, which was previously utilized to absorb the DC-link energy during sags. The buffer is commanded to operate in the boost mode to charge the DC-link whenever the PV power drops beneath a certain threshold. For our experiment, if the input power drops below 10% of its nominal power, the buffer stage will

provide the energy deficit to maintain the constant power output.

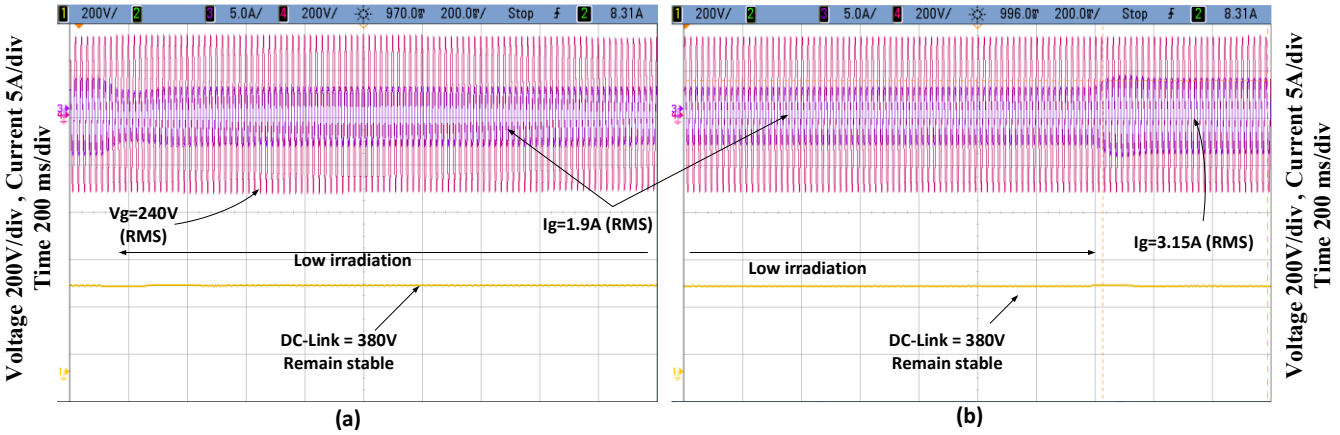

FIGURE 24. Inverter output without buffer stage during low irradiation (a) AC current reduction during low irradiation arrival ;(b) AC current reduction during low irradiation departure.

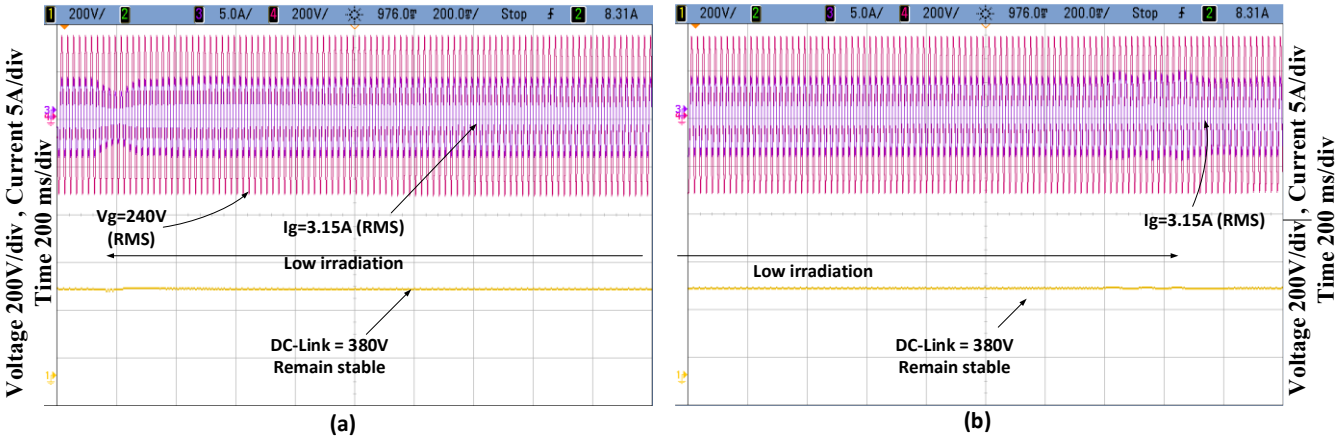

FIGURE 25. Inverter output with buffer stage during low irradiation (a) AC current reduction during low irradiation arrival ;(b) AC current reduction during low irradiation departure.

Fig.24(a) and 24(b) shows that the PV inverter reduces the output current from 3.15A to 1.19A without buffer stage, while the DC-link voltage remains constant. In the second experiment, the buffer stage is integrated with the control loop, as explained in section III(B). The buffer stage ensures that the output power injection remains constant during PV flickers. Fig.25(a) and 25(b) shows that the PV inverter maintains the output current at 3.15A with buffer stage, while the DC-link voltage remains constant. Fig.26(a) shows the grid voltage, PV power, Battery buffer power, and the output AC power when the inverter is subjected to periodic PV fluctuations of 1s, every 5s. As the PV power is reduced, the battery power provides the deficit, thus keeping the output AC power constant. Fig.26(b) shows the PV curves during dynamic PV fluctuations.

Table VII summarizes the measurements of the proposed system during AC/DC faults. The proposed control strategy keeps the inverter connected during AC-sags of variable magnitude. During the severer sags, only reactive power is injected into the grid. The amount of reactive power injection is programmed by the grid code standard presented in (15-16). The inverter is tested with variable intensity consecutive sags (0.20,0.50, and 0.80 p.u) and remains connected to the grid. As soon as the grid resumes standard voltage, the inverter seamlessly switches to regular MPPT operation. While injecting reactive power, the inverter harvests the available PV power (800W) into the battery instead of wasting it. In the case of DC side faults, when the drop in PV power falls below 10% of its nominal value (720W), the control algorithm triggers the additional DC-link charging from the buffer stage. The battery buffer provides an energy deficit to avoid flickering and maintains the constant power output. The system remained connected to the grid, and the DC-link voltage remained within the safe limits. The PV inverter maintains the MPPT and injects the maximum power into the grid or harvests it into the battery in AC/DC faults.

TABLE VII
Summary of experimental results.

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Fault type	Intensity %	DC-link (V)	PV Power (W)	Battery Power (W)	Reactive Power (VAR)	Active Power (W)
Single Sag	50%	380	800	+800	380	0
Multiple Sag	20%	380	800	+250	220	580
	50%	380	800	+800	380	0
	80%	380	800	+800	350	0
Low Irradiance	20%	380	550	-250	0	750
Normal	-	380	800	0	0	740

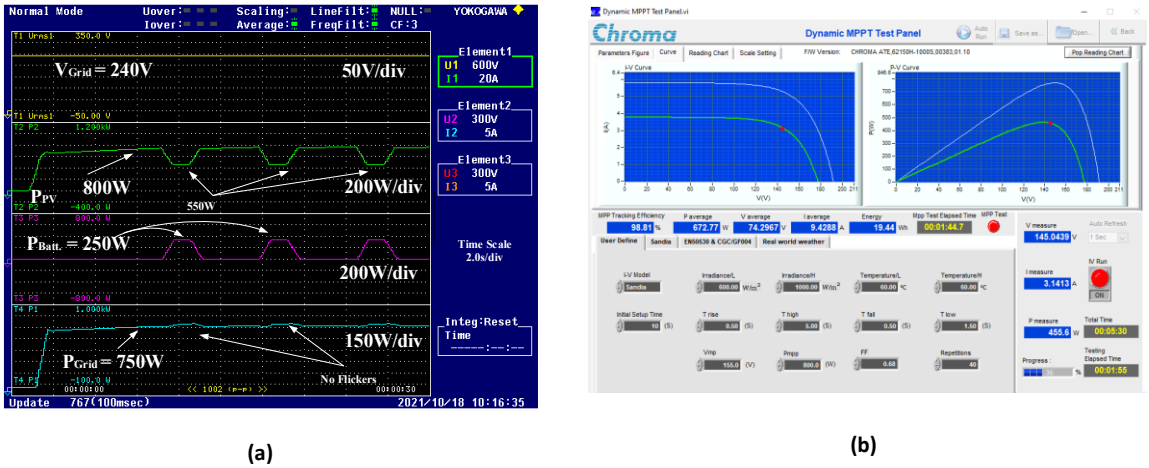

FIGURE 26. **Constant power output in low irradiation fault: (a) Dynamic MPPT (b) Dynamic irradiation change PV curve**

C. *Comparison with other inverters*

The single-phase grid-tied inverters are controlled either in the stationary reference frame (αβ) via PR controller or in the rotating reference frame (DQ) via PI controller. Both of these strategies provide acceptable inverter performance in terms of efficiency, output power quality, and controllability. Some studies have also explored both of these techniques to control the two-stage inverter during AC sags and DC input power fluctuations. Therefore, a simulation-based comparison of the proposed inverter with both DQ-PI and αβ-PR controlled inverters is presented to highlight the proposed system efficacy. The authors in the study [36] proposed single-phase rotating reference frame control (*DQ-PI*) to implement the LVRT in two stages inverter, while the authors in [37] have implemented a stationary reference frame control (*αβ-PR*) for sags compensation. These inverters closely matched the proposed two-stage system except for the battery-buffer stage. Therefore, the models of these inverters are simulated and compared with the proposed stationary reference frame control with the feed-forward linearization technique (PI-FFL).

All the inverters are rated at 800W nominal output in normal conditions, while LVRT strategy is implemented as described in their respective articles [36, 37]. The proposed buffer stage with small lead acid battery rated at 160V 7Ah is used in the simulation. The simulation is conducted for 7s, some other parameters of simulations are shown in Table I. Initially the inverters are started normally. Next, the three consecutive grid sag of 20% (0.5-1s), 50%(1.5-2s), and 80%(2.5-3s) are applied to the inverters. After sags, the two consecutive step changes in the input PV irradiance are tested (30% reduction from 4-4.5s and 50% reduction from 5-5.5s). The MATLAB simulation results in Fig. 27 shows the DC-link voltage, active/reactive power output, boost stage duty, and the PV operating point during the faults. The (*DQ-PI*) controlled inverter results are shown in Fig.27 in the left-most column, while the (*αβ-PR*) controlled inverter results are shown in the middle column. Finally, the proposed inverter (*PI-FFL*) results are shown in the rightmost column.

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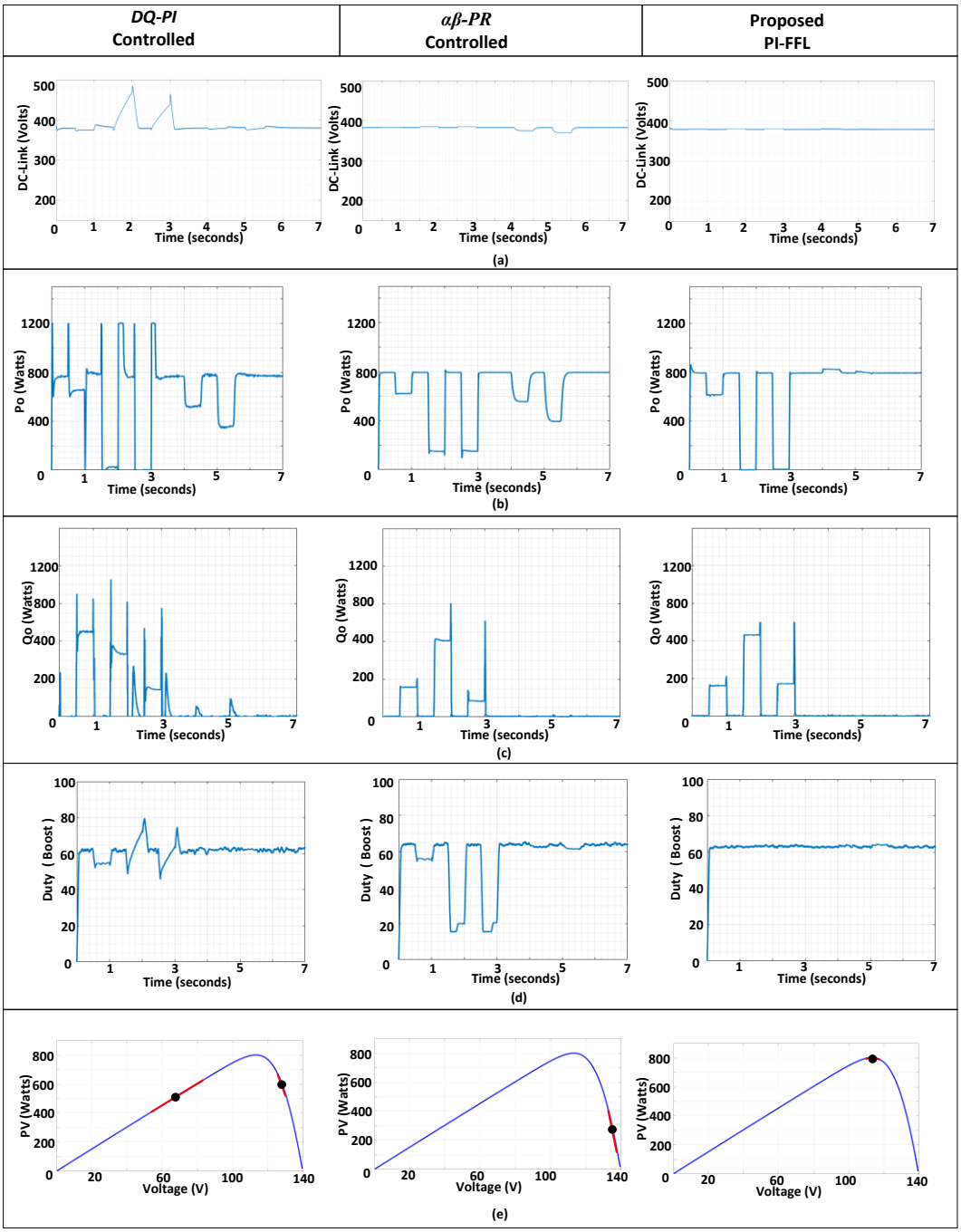

FIGURE 27. Comparison under faults: (a) DC-link voltage comparison, (b)active power comparison, (c) reactive power comparison, (d) boost duty ratio comparison, (e) PV operating point comparison

1) DC-LINK VOLTAGE COMPARISON

In Fig.27(a), the DC-link voltage is compared, and it can be seen that until the first 20% sag, the DC-link voltage remain stable for all the three inverters, but during 50% and 80% sags, the DC-link voltage has raised more than 500V for the *DQ* inverter. The DC-link voltage for *αβ* does remain stable but with some fluctuations. However, the DC-link voltage of the proposed control strategy is well regulated at 380V during the whole operation without any fluctuations

2) ACTIVE AND REACTIVE POWER COMPARISION

Similarly, Fig.27 (b) and 27 (c) show the output active and reactive power injection. The active power is reduced during the sags, while reactive power is injected as per grid codes. However, it is evident that the *DQ-PI-controlled* inverter often runs into peak power during transitions, which may trigger the shutdown protection.

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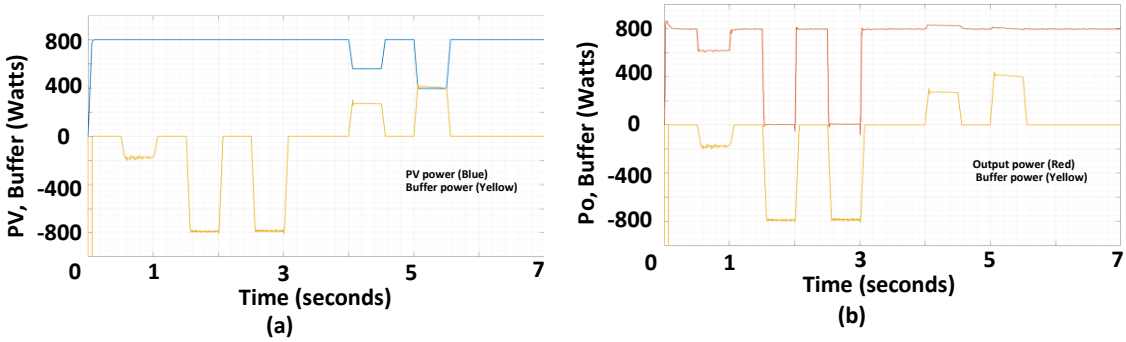

FIGURE 28. Power balance in sags and low irradiation with proposed control

TABLE VIII
Comparison with other inverters

	LVRT	Q-Support in LVRT	LiR Support	MPPT & LVRT	Multiple-intensity sags
[37]	✓	✓	×	×	×
[36]	✓	✓	×	×	×
[4]	✓	✓	×	×	×
[38]	✓	✓	×	×	×
[1]	✓	✓	×	×	×
[8]	✓	✓	×	×	×
[6]	✓	✓	×	×	×
[9]	✓	✓	×	×	×
[39]	✓	✓	×	×	×

The *αβ-PR* controlled inverter does inject the required active power during 20% sag. However, for 50% and 80% sags, the required power values could not be regulated. Moreover, both *DQ-PI* and *αβ-PR* strategies could not prevent the output power flicker during low-irradiation faults between (4-4.5)s and (5-5.5s). On the other hand, the proposed *PI-FFL* controllers successfully withstand variable intensity sags by diverting the PV power to buffer during sags and using the same buffer in case of low input power during low irradiation. As the operating point of the first stage boost converter remain undisturbed in the proposed LVRT control strategy, the PV inverter will not shut down in any intensity sag.

3) BOOST DUTY CYCLE COMPARISION

Figure 27(d) shows the duty cycle variation of 1st stage boost converter during the normal, LVRT, and PV flicker conditions. The *DQ-PI* inverter shows 45-80% variation, and *the αβ-PR* inverter show 15-65% variation in the boost duty cycle. These variations will shift the boost converter from CCM to DCM or saturate the boost induction, resulting in the DC-link voltage collapse.

On the other hand, the proposed *PI-FFL* control shows a continuous boost operation at 62-65% duty, ensuring the CCM mode during normal, LVRT, and PV flicker modes. Finally, the comparison of the operating point at the PV curves for all the three inverters is shown in Figure 27(e). During LVRT and PV flickers, the MPPT is disabled for both *DQ-PI* and *αβ-PR* inverters, forcing them to operate at low power at DCM or saturation. However, the proposed PI-FFL inverter keeps operating at MPPT.

4) POWER BALANCE IN SAGS AND LOW IRRADIATION

Figure 28(a) shows the PV power and the buffer power; as the sag arrives, the excess power is absorbed into the buffer, thus keeping the inverter stable. During the low DC-input from PV, the buffer stage provides the remaining power deficiency, thus keeping the flicker-free constant power output as shown in Figure 28(b).

D. Features comparison with other LVRT inverters

The features of the proposed system are compared with recently proposed PV inverters in Table VIII. The comparison shows that the proposed control strategy implements several ancillary features, including AC/DC fault ride-through, reactive power support, and MPPT during faults. Moreover, the proposed LVRT strategy is easily transferable to the available PV-battery hybrid systems of references [8, 40-48].

CONCLUSION

A robust fault ride through mechanisms in PV inverters would not only improve the effectiveness of PV grid-tied inverters but also improve grid stability. The proposed low-

power PV inverter has multifunctional features, tackling both AC sags and DC low irradiation faults. The presented simulations and experiments demonstrate the inverters capability to handle variable strength AC sag, reactive power injection, and low irradiation support. A small battery buffer is utilized to absorb the excess power during grid sags; thus, the inverter never disables the MPPT. The same battery buffer provides the PV inverter with additional power when the input PV power drops because of low irradiation. The proposed LVRT strategy with energy buffer can seamlessly fulfill LVRT grid codes.

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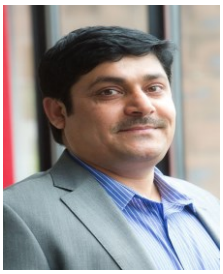

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