A High Step-Up Transformerless DC-DC Converter with New Voltage Multiplier Cell Topology and Coupled Inductor

A High Step-Up Transformerless DC-DC Converter with New Voltage Multiplier Cell Topology and Coupled Inductor

Pouria Sarvghadi, Ali Yazdian Varjani, *Member*, *IEEE*, Mahdi Shahparasti, *Member*, *IEEE*

Abstract— In this paper, a new high step-up transformerless DC-DC converter based on voltage multiplier and coupled inductor topology is presented. The proposed converter has two stages. In the first stage, a modified boost converter is designed by the coupled inductor and in the second stage, a new voltage multiplier by using a coupled inductor was illustrated. In this converter, high voltage gain can be achieved by adjusting the turn ratio of two coupled inductors and duty cycle which result in three degrees of design freedom. Using a single power switch with low on-resistance in the converter structure leads to simple control and low conduction loss. Also, total voltage stresses of active elements are decreased which cause to increase efficiency. Steady-state performance and theoretical achievements are confirmed by experimental test results on a test setup with one 200 W DC-DC prototype.

Keywords: coupled-inductor, high step-up, transformerless, dc-dc converter, high voltage gain

I. INTRODUCTION

Nowadays, with increasing energy consumption and environmental concerns, renewable energy sources such as wind and photovoltaic have become attractive topics in both academia and industry [1]. Photovoltaic systems need less periodic maintenance and they have no rotating elements. In addition, having a long life along with the above advantages leads to increase installation capacity continuously [2]-[3]. But it should be noted that the low output voltage of the photovoltaic (PV) panel is a challenge in their use. Series connection of the PV panels is the easiest way to increase voltage levels In this way, the existence of shadow and cloud effect or failure in any panel leads to reduced reliability as well as system efficiency [4], [5]. Using a transformer along with the converter topology is a simple solution to increase the output voltage of the PV panel [6].

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Full bridge, push-pull, flyback and forward are familiar topologies that using a transformer in their structure [7], [8]. In these topologies, high voltage gain can be achieved by increasing the turn ratio of the transformer [9]. As a result, leakage inductance will increase by high turn ratio of the transformer that leads to reverse recovery problem and switching loss [10], [11].

In recent years, high step-up transformerless (HSUT) DC-DC topologies have been proposed to solve the above problems [4]. Hence, low switching loss, volume and cost are some advantages of the transformerless converter. Moreover, high efficiency and high power density complete the above benefits [10], [12]. HSUT DC-DC converters can be categorized as, boost, cascade boost, Z-Source, switch capacitor, coupled inductor, multilevel and voltage multiplier [13], [14]. Boost topology is a basic HSUT DC-DC converter. Although this topology has an infinite gain in theory, the high voltage stress and parasitic problem limit the gain of this converter in real application [1]. The poor efficiency and reverse recovery problem are other drawbacks of the boost converter [15]. Cascade boost converters have a high gain but control of these are complicated due to the high number of conversion stages [16]. Usually, two high gain converters are connected in a back to back way. The first stage works with a higher switching frequency and for lossless operation, the second stage works with a lower frequency [17]. The high number of required components and low reliability are some drawbacks of the cascade converter [18].

The DC/DC Z-source converters, as another family of HSUT converters, operate based on the shoot through among DC link and then charging inductor and capacitor in their circuit [19], [20]. After the shoot through, the saved energy of the passive element is accumulated by the dc-link and then voltage boosting is occur. Due to the use of many passive elements, the cost and volume are high in Z-source converters [21]. Further, high voltage stress and current spike in this topology lead to switching loss and consequently low efficiency [22].

Using switch capacitor converters is another way to attain high voltage gain. These topologies adopt an uncomplicated circuit but they need to use many capacitors for reaching high voltage gain which results in reducing the lifetime of the converter [23]. Moreover, the high number of switches in these converters leads to poor efficiency and high complexity in control [24]. Further, the dependence of voltage gain on the arrangement of capacitors is another disadvantage of switch capacitor converters [25].

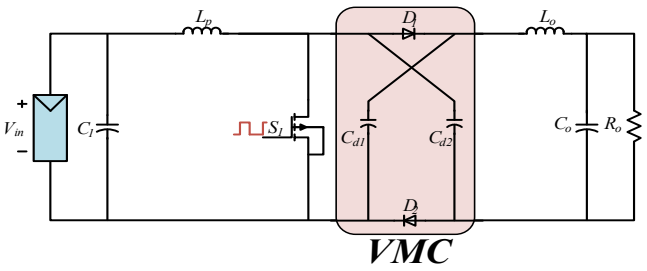

Fig. 1. Arranged VMC in conventional boost converter [14]

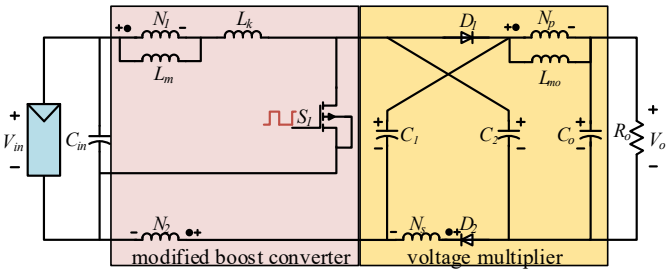

Fig. 2. Proposed converter based on voltage multiplier and coupled inductors

HSUT DC-DC converters with coupled inductors have been presented in [5], [26]. In these topologies, windings wrap around one core that leads to low weight and volume and also high power density and efficiency [27]. High gain can be achieved by increasing the number of turn ratios in the coupled inductor [25], [28].

Similarly, voltage multiplier (VM) is a simple, efficient and low cost that consists of diodes, capacitors and inductors [29]. Basic VM is shown in Fig. 1, which consists of two diodes and two capacitors.

As shown in Fig. 1, a high voltage gain can be achieved by inserting VM after the active switch in the boost topology [14]. From Fig. 1, capacitors will be charged and discharged by turning off and on the active switch respectively. VMs are suitable for high output voltage and low output current converters [29]. Despite the mentioned benefits, but the main weakness of VM is a fixed gain [29]. This means that adjusting the gain of this converter is done by changing the duty cycle of the active switch and the VM stage has a fixed gain that, multiplies in boost gain.

Considering the above description and deficiency of high step-up converters, a new HSUT DC-DC converter with voltage multiplier and coupled inductors will be proposed in this paper. High voltage gain can be achieved by a new voltage multiplier and coupled inductors structure which solved the fixed gain problem. The proposed converter includes a single switch that simplifies converter control and it is suitable for PV applications. Besides, the proposed topology gives three degrees of design freedom. This means that voltage gain can be adjusted by the duty cycle as well as the turn ratio of coupled inductance in the first stage and turn ratio of coupled inductance in the second stage. Also, the proposed topology can work in the low duty cycle. With a lower duty ratio, voltage and current stresses on the components are decreased which results to reduce conduction loss. In the next sections, operation mode and steady-state analysis of the proposed converter is investigated in section II. Then, related equations will be discussed in section III. Next, comparison study and experimental results were investigated in sections IV and V respectively. Finally, section VI concludes the paper.

II. Steady-State Analysis

The proposed topology is shown in Fig. 2 which has two high step-up stages. In the first stage, a modified boost converter is designed by the coupled inductor and in the second stage, a new voltage multiplier by using a coupled inductor is implemented.

The proposed converter consists of one active switch S_1, two coupled inductor L_m & L_{mo}, two diode D_1 & D_2 and two capacitors C_1 & C_2. For increasing voltage gain, a new voltage multiplier and a coupled inductor topology are combined with a modified boost topology.

This proposed topology has three operation modes as shown in Fig. 3. In order to simplify, the following assumptions are considered:

1) *All semiconductor components are ideal without any loss.*
2) *All capacitors are large enough, so their ripple can be ignored.*
3) *The proposed converter operates in CCM conditions.*
4) *Ignore leakage inductance of the coupled inductors in the operation condition*

MODE I (t_0-t_1): In this mode, active switch S_1 is turned on by gating pulse signal, and magnetizing inductance L_m is charged by input dc voltage source. D_1 and D_2 are in blocking mode and magnetizing current of L_{mo} is increased by energy stored at VM stage capacitors C_1 and C_2. Based on Fig. 3(a), the load current is supplied by capacitor C_o. This mode is finished when the switch is turned off. The key waveform of this mode is represented in Fig. 3(a).

MODE II (t_1-t_2)(intermediate mode): This intermediate time interval is shown in Fig. 3(b) where S_1 goes to the off state. Due to the inductor current is kept in continuous conduction mode, D_2 is working in conduction mode and its current is greater than zero. The diode D_1 is in forward bias but its current is zero. This causes an intermediate interval but has no effect on the voltage equations of the proposed topology. In this intermediate mode, D_1 is in the forward bias, but due to the discharge of the output magnetizing current in the capacitor C_1, its current is zero. Therefore, C_2 is charged by the input current. Output inductance current ILmo decreases linearly and also C_1 charges by this current. A detailed visual representation is shown in Fig. 3.

MODE III (t_2-t_3): In this time interval, S_1 is still at the off state and D_1 goes to conduction mode (see Fig. 3(c)). Primary (VN1, VNp) and secondary (V_{N2}, V_{Ns}) windings of input and output coupled inductance act as a voltage source and make a voltage loop with input dc source. As a result, these series voltage sources transfer energy to the load. Hence, the high voltage gain can be achieved by increasing of turn ratio of the coupled inductor. C_1, C_2 continues to store energy and then discharges this energy into the output inductance V_{Lmo} at the beginning of mode I. The presence of a secondary winding in the VM path increases the voltage across capacitor C_2 and transfers more energy to the output inductor when the switch is turned on.

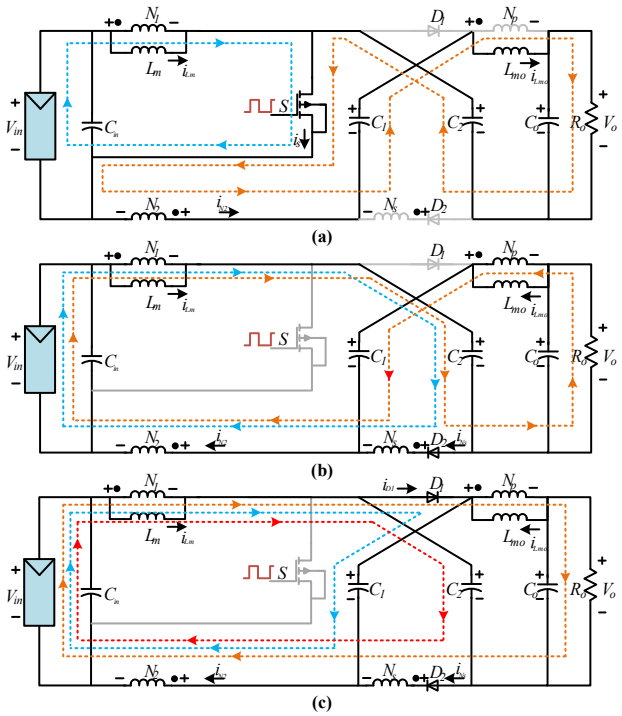

Fig. 3. Operational mode of the proposed converter a) Mode I [t_0-t_1] b) Mode II(intermediate) [t_1-t_2] c) Mode III [t_2-t_3]

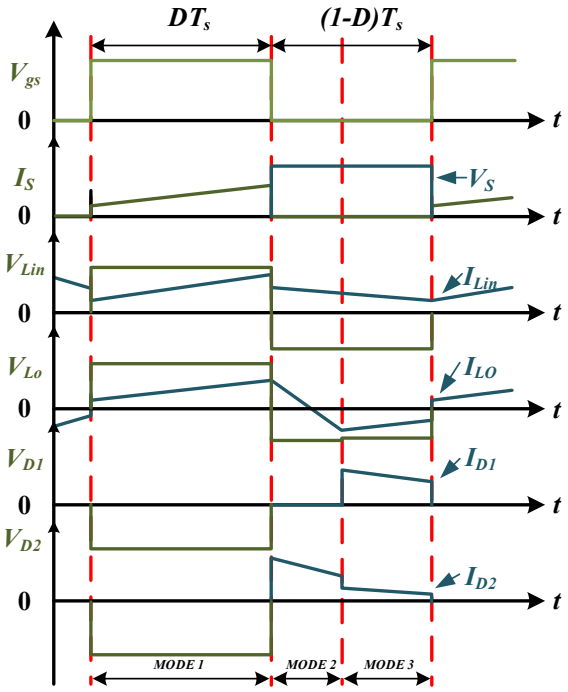

Fig. 4. Typical waveforms of the proposed converter

III. Equivalent Equations

For optimizing the operation of the proposed topology, the converter design procedure is very important. Hence, the analysis of the proposed topology is discussed below.

A. Calculation of the proposed converter voltage gain

According to Fig. 3, the proposed converter has three modes in CCM condition. First, the below assumptions are considered.

$$V_{N_1} = V_{Lm} = \frac{N_1}{N_2} V_{N_2}$$
$$V_{Np} = V_{Lmo} = \frac{N_p}{N_s} V_{N_s} \qquad (1)$$
$$n_i = \frac{N_2}{N_1} \qquad n_o = \frac{N_s}{N_p}$$

where V_{Lm} and V_{Lmo} are the voltages of magnetizing inductances of primary and secondary coupled inductors. n_i and n_o are turn ratios of input and output coupled inductors respectively. By applying KVL law for mode I in Fig. 3(a), the following relations can be extracted :

$$V_{Lm} = V_{in} \qquad (2)$$
$$V_{c2} - V_o - V_{Lmo} + V_{c1} + n_i V_{Lm} = 0 \qquad (3)$$

where V_{c1}, V_{c2} are voltages of C_1 and C_2 capacitors, respectively. When the first time interval is completed, the main switch goes to the turn-off state and diodes D_1 and D_2 is being to the conduction mode. However, it should be noted that the current of D_1 (MODE II) is equal to zero. KVL law for Fig. 3(b) and Fig. 3(c) are as follows:

$$-V_{in} + V_{Lm} + V_{Lmo} + V_o + n_o V_{Lmo} + n_i V_{Lm} = 0 \qquad (4)$$
$$-V_{in} + V_{Lm} + V_{c1} + n_i V_{Lm} = 0 \qquad (5)$$
$$-V_{in} + V_{Lm} + V_{c2} + n_o V_{Lmo} + n_i V_{Lm} = 0 \qquad (6)$$
$$-V_{c2} + V_{Lmo} + V_o = 0 \qquad (7)$$
$$-V_{c1} + V_{c2} + n_o V_{Lmo} = 0 \qquad (8)$$
$$-V_{c1} + V_{Lmo} + V_o + n_o V_{Lmo} = 0 \qquad (9)$$
$$-V_{in} + V_{Lm} + V_{c2} - V_o - V_{Lmo} + V_{c1} + n_i V_{Lm} = 0 \qquad (10)$$

In the $(1\text{-}D)T_s$ time interval, energy from the source as well as the energies stored in the windings of the coupled inductor are transferred to the load.

The V_{c1} and V_{c2} voltages of the proposed converter can be calculated according to the volt-second law of input inductor L_m and output inductor L_{mo} and respect to input and output voltages. Hence, considering equations (2) and (5):

$$\begin{cases} (2) \rightarrow V_{Lm} = V_{in} \\ (5) \rightarrow V_{Lm} = \dfrac{(1-D)}{1+n_i}(V_{in} - V_{c1}) \end{cases} \qquad (11)$$
$$DV_{in} + \frac{(1-D)}{1+n_i}(V_{in} - V_{c1}) = 0$$

In (11), D is the duty cycle of the active switch. As a result, V_{c1} can be calculated as follows.

$$V_{c1} = \left(\frac{1+Dn_i}{1-D}\right) V_{in} \qquad (12)$$

By applying the volt-second law for output inductor L_{mo} and based on (3) and (7), the below equation can be extracted.

$$\begin{cases}(3)\rightarrow V_{Lmo}=V_{c2}-V_o+V_{c1}+n_iV_{in}\\(7)\rightarrow V_{Lmo}=V_{c2}-V_o\end{cases}$$
$$D(V_{c2}-V_o+V_{c1}+n_iV_{in})+(1-D)(V_{c2}-V_o)=0 \quad (13)$$

The voltage of C_2 can be described from (13) as follows:

$$V_{c2}=V_o-DV_{c1}-Dn_iV_{in} \quad (14)$$

Finally, the output voltage gain can be calculated by applying volt-second law for the output inductor by using (3), (9), (12) and (14) as:

$$\begin{cases}(3)\rightarrow V_{Lmo}=V_{c2}-V_o+V_{c1}+n_iV_{Lm}\\(9)\rightarrow V_{Lmo}=\dfrac{V_{c1}-V_o}{1+n_o}\end{cases}$$
$$D(V_{c2}-V_o+V_{c1}+n_iV_{Lm})+(1-D)(\frac{V_{c1}-V_o}{1+n_o})=0 \quad (15)$$

As a result, the output voltage gain of the proposed converter is calculated based on the below equation:

$$M_{ccm}=\frac{V_o}{V_{in}}=\frac{1+D+2Dn_i+Dn_o+Dn_in_o}{1-D} \quad (16)$$

Also, the output voltage gain by considering the leakage inductance is obtained from the following equation.

$$M=\frac{V_o}{V_{in}}=\frac{1+D+2Dn_ik_1+n_ok_2D+n_in_ok_1k_2D}{1-D} \quad (17)$$

where k_1 and k_2 are magnetic coupling coefficients and calculated as follows.

$$k_1=\frac{L_m}{L_m+L_{k1}} \quad (18)$$

$$k_2=\frac{L_{mo}}{L_{mo}+L_{k2}} \quad (19)$$

where L_m, L_{k1}, L_{mo} and L_{k2} are input magnetizing and leakage inductance and output magnetizing and leakage inductance respectively.

From (16), output voltage gain depends on three parameters n_i, n_o and D. Hence, the output voltage of the proposed converter can be changed by adjusting any of the above parameters. This means that it has three degrees of design freedom for increasing output voltage gain.

Output voltage gain in terms of duty cycle and turn ratio of input coupled inductor $n_i=N_2/N_1$ is shown in Fig. 5. According to this figure, the proposed converter can achieve high voltage gain by increasing of n_i turn ratio.

Output voltage gain versus of duty cycle and turn ratio of output coupled inductor $n_o=N_s/N_p$ is shown in Fig. 6. Similarly high voltage gain attains with increasing at output coupled inductor turn ratio. In the high step-up DC-DC converters, the output current is lower than the input current. Hence, increasing the number of turn ratio in the output coupled inductor effects less on reducing efficiency. By assuming that constant duty cycle (D=0.5), the variation of output voltage gain concerning changing turn ratio at input and output coupled inductor is shown in Fig. 7.

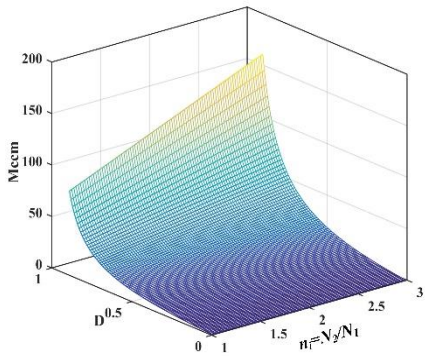

Fig. 5. Output voltage gain in terms of duty cycle and secondary winding of input inductor

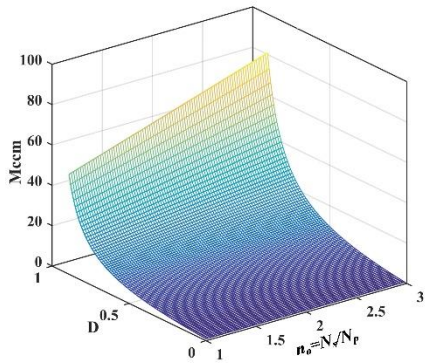

Fig. 6. Output voltage gain in terms of duty cycle and secondary winding of output inductor

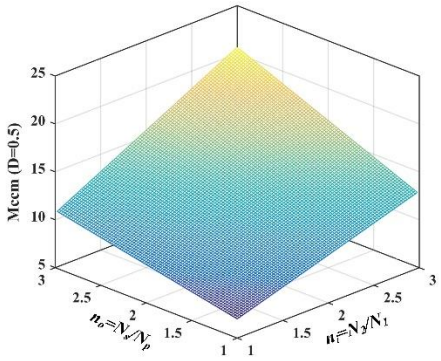

Fig. 7. Output voltage gain in terms of duty cycle and secondary winding of output inductor

B. Voltage stresses of the semiconductors

The proposed converter has one main switch and two diodes. The voltage across the semiconductor in the off state is used for stress calculation. Hence, the voltage at off state for the main active switch is equal to:

$$V_s=V_{in}-V_{Lm} \quad (20)$$

where V_s is the voltage stress of the main active switch. Based on (2), when the active switch is turned on voltage of magnetizing inductance at the input coupled inductor is equal to the input voltage source. So, with applying volt-second law for input inductor and according to (2) and (20) the voltage stress of the main active switch can be obtained by:

$$DV_{in} + (1-D)(V_{in} - V_s) = 0 \Rightarrow$$
$$V_s = \frac{V_{in}}{1-D} \quad (21)$$

Diodes, D_1 and D_2, are in blocking mode when the active switch is on. In DT_s time interval, voltages of D_1 and D_2 can be calculated by the below equations.

$$V_{D1} + V_{c1} + V_{Lm} + n_i V_{Lm} - V_{in} = 0 \quad (22)$$

$$V_{D2} + V_o + V_{Lmo} + n_o V_{Lmo} - V_{c1} = 0 \quad (23)$$

Using V_{c1} and V_{Lm} from (5), the voltage of D_1 with accordance to (22) can be described as follows:

$$V_{D1} = -\frac{1+n_i}{1-D} V_{in} \quad (24)$$

Likewise, using V_{c1} and V_{Lmo} from (9) and substitution in (23) voltage of D_2 is calculated as:

$$V_{D2} = \frac{\frac{1+n_o D}{1-D} - M_{ccm}}{D} V_{in} \quad (25)$$

C. Magnetizing inductances and core volume calculation

First, magnetizing calculation of the proposed converter is investigated as follows. Based on [30] and [31], the magnetizing current of the coupled inductor is calculated as:

$$I_{Lm} = I_1 + \frac{N_2}{N_1} I_2 \quad (26)$$

where I_{Lm}, I_1 and I_2 are magnetizing currents, current of first winding and current of second winding respectively. According to (26) the average magnetizing current of input coupled inductor obtained as:

$$I_{Lm} = I_{in} + \frac{N_2}{N_1} I_o = (M_{ccm} + n_i) I_o \quad (27)$$

Also, the magnetizing current ripple for the input coupled inductor is calculated as follows:

$$\Delta I_{Lm} = I_{Lm-\max} - I_{Lm-\min} = \frac{DV_{in}}{L_m f_s} \quad (28)$$

In the continuous conduction mode, the minimum current of the magnetizing inductor must be greater than zero. As a result, according to (27) and (28), the minimum required inductance for the input coupled inductor is derived from the below equation.

$$L_m > \frac{R_L D}{2M_{ccm}(n_i + M_{ccm}) f_s} \quad (29)$$

Similarly, the average and ripple current of the magnetizing output inductance can be calculated as follows:

$$I_{Lmo} = I_o + \frac{N_s}{N_p} I_o = (1+n_o) I_o \quad (30)$$

$$\Delta I_{Lmo} = I_{Lmo-\max} - I_{Lmo-\min} = \frac{D(1+ni)V_{in}}{L_{mo} f_s} \quad (31)$$

Considering equations (30) and (31), the minimum magnetizing inductance for the output coupled inductor can be described as follows.

$$L_{mo} > \frac{R_L D(1+n_i)}{2M_{ccm}(1+n_o) f_s} \quad (32)$$

The area product (AP) parameter will be calculated as an indicator of the required core volume in the converters. This parameter is the product of the window area, W_a, and the core cross-section, A_c. For the coupled inductor AP is formulated as:

$$A_{p\_coupled} = \frac{L_{11} I_{11}^{\max} \pm M_{12} I_{22}^{\max}}{B_{\max} k_u J} I_{rms}.10^4 \quad \text{cm}^4 \quad (33)$$

where L_{11}, M_{12}, I_{11max}, I_{22max}, B_{max}, k_u , J and I_{rms} are self-inductance, mutual inductance, the maximum current of first winding, the maximum current of second winding, the maximum flux density of the core, winding fill factor, current density and RMS current of winding respectively. Mutual inductance can be obtained as:

$$M_{12} = k\sqrt{L_{11} L_{22}} \quad (34)$$

where k is the coupling coefficient.

D. Efficiency Analysis

In this section, the detailed loss analysis among components of the proposed converter is investigated. Losses in DC-DC converters are divided into different parts including switching losses, diode losses, magnetic losses and capacitive losses. Hence, the loss distribution among components of the proposed converters is studied using the analytical method presented in [31]-[35].

1) Mosfet Switch loss

The conduction loss of the Mosfet is obtained as follows:

$$P_{mosfet\_cond} = R_{DS\_on} I_{rms}^2 \quad (35)$$

where R_{DS_on} and I_{rms} are the on-resistance of the Mosfet during its on-state and RMS of Mosfet current respectively.

The switching loss of the Mosfet is obtained as:

$$P_{mosfet\_switching} = \frac{1}{2} C_s f_{sw} {V_S}^2 \quad (36)$$

where C_s is the output capacitance of the active power switch which is derived from the Mosfet datasheet. Also, f_{sw} and V_s are the switching frequency and the off-state voltage across the power switch.

2) Diode loss

The conduction loss of diodes is calculated from (37), where, V_{D_on}, R_{D_on}, I_{D_avg} and I_{D_rms} are the diode on-state voltage drop, on-resistance of the diode, average and RMS diode currents, respectively.

$$P_{D\_con} = V_{D\_on} I_{D\_avg} + R_{D\_on} I_{D\_rms}^2 \quad (37)$$

3) Magnetic core and copper loss

According to [32], magnetic core loss per kg is obtained as,

$$P_{core\_loss} = K_c \left(\frac{\Delta B}{2}\right)^{\beta} f_{sw}^{\alpha} \quad (\frac{w}{m^3}) \quad (38)$$

where K_c, α and β are constants relating to the magnetic core material, which are given in [32] for the selected core material. Also, ΔB is peak to peak flux density ripple. In addition, the copper loss of the windings of the coupled-inductors are formulated in [34] as,

$$P_{copper\_loss} = \rho \frac{MLT}{K_u W_a} (N_1 I_1 + N_2 I_2)^2 \quad (39)$$

where, ρ, MLT, Wa, Ku are the copper wire resistivity, the mean length per turn of windings, the winding area of the core and the winding fill factor, respectively. Also, N_1 and N_2 (or N_p, N_s) are windings turns, and I_{N1}, I_{N2} (or I_{Np}, I_{Ns}) are RMS currents of windings.

4) Capacitor ESR loss

The capacitor loss is associated with the equivalent series resistance (ESR) of the capacitor, which can be experimentally measured. This power loss is obtained as,

$$P_{capacitor\_loss} = R_{ESR} I_c^2 \quad (40)$$

where, R_{ESR} and I_c are the equivalent series resistance and the RMS current of the capacitor, respectively. All capacitors losses are calculated using (40) and summed together as the total loss of the capacitors.

IV. Comparison Study

In this part, a brief comparison is done between the proposed converter and other high step-up DC-DC converters. The focus of this comparison is around the number of components such as switches, diodes, inductors and capacitors and also voltage stresses of semiconductors and voltage gain. This comparison is collected in Table. I, in which, the number of capacitors regardless of the output capacitor is calculated. The proposed converter has lower components with respect to all HSUT DC-DC topologies in Table. I.

In order to explore the voltage gain variation versus duty cycle, in three different modes by changing the turn ratio of coupled inductor is shown in Fig. 8. Both [16], [36] use a VMC circuit but they have a fixed gain as shown in Fig. 8. Moreover, in [36] utilizing two active switches leads to increase complexity and conduction loss. From Fig. 8 (a) with a duty cycle below 0.5, the converters in [18], [27], [37] have a higher gain than the proposed topology. It should be mentioned that these converters contain more diodes and capacitors which leads to decrease efficiency and lifetime respectively.

Based on Fig. 8 (b), (c), if the turn ratio of the coupled inductor increases, the voltage gain of the proposed converter becomes more distant from other converters. It should be noted that, contrary to [18], [25], [27] and [38], the ratio of the coupled inductor is equal to the primary to the secondary ratio in the proposed converter. Therefore, the turn ratio of the coupled inductor must be raised for increasing the voltage gain. As a result, the turn ratio of the primary winding is greater than the turn ratio of the secondary winding in those converters that leads to high magnetizing inductance, and consequently higher size and losses in the coupled inductor.

In another comparison, total voltage stresses (TVS) for the active switch and diode with respect to changing the turn ratio of the coupled inductor is investigated. The voltage gain is considered fixed and equal to 12 (g=12). Based on Fig. 9 and Fig. 10, the TVS for the active switch and diodes are grid shape and other topologies are single line. From Fig. 9, it can be seen that there are many choices for ni and no in order to achieve low TVS for the active switch in the proposed topology.

Moreover, the TVS for the active switch is less than [16], [18], [25], [27], [36] and [37] which leads to the size and cost reduction of the active switch. In some points of Fig. 9, with the increasing turn ratio of the coupled inductor, the TVS of the active switch of [38] is below than proposed topology.

However, in [38] increasing the turn ratio leads to a high magnetizing current and more core size. Another comparison is related to the TVS of diodes, which is shown in Fig. 10. In this figure, the TVS for the diode in the proposed topology is mainly lower than other HSUT converters. Also, g=12 can be achieved with different values of n_i and n_o to reduce TVS for diodes. As a result, high step-up gain along with low switch stress is accessible in the proposed converter.

Table. I. Comparison between the proposed topology and other high step-up topologies

	Voltage Gain(M)	Switch Voltage Stress $\sum V_s$	Diode Voltage Stress $\sum V_d$	Number of components				Total of Components
				SW	D	C	Core	
Converter in [27]	$\frac{2+n+D}{1-D}$ $n:N_p/N_s$	$\frac{1+M}{3+n}V_I$	$\frac{(2n+4)(1+M)}{3+n}V_I$	1	4	4	2	9
Converter in [37]	$\frac{2+n+D(n+1)}{1-D}$ $n:N_s/N_p$	$\frac{1+M+n}{3+2n}V_I$	$\frac{(3n+4)(1+M+n)}{3+2n}V_I$	1	4	4	2	9
Converter in [38]	$\frac{(n+1)D+1}{1-D}+2n$ $n:N_p/N_s$	$\frac{M-n+1}{n+2}V_I$	$\frac{(3n+1)(M+1-n)}{n+2}V_I$	1	4	4	2	9
Converter in [16]	$\frac{3+D}{2(1-D)}$	$\frac{1+2M}{4}V_I$	$\frac{(3+6M)}{4}V_I$	1	4	3	2	8
Converter in [36]	$\frac{3+D}{1-D}$	$\frac{2(1+M)}{3}V_I$	$1.5(M+1)V_I$	2	3	2	3	6
Converter in [18]	$\frac{2(n+1)}{1-D}$ $n:N_p/N_s$	$\frac{M}{1+n}V_I$	$\frac{7M}{1+n}V_I$	2	7	6	2	15
Converter in [25]	$\frac{(n+1)}{1-D}$ $n:N_p/N_s$	$\frac{M}{n+1}V_I$	$\frac{(2n+1)M}{n+1}V_I$	1	3	3	2	7
Proposed converter	$\frac{1+D+2Dn_i+Dn_o+Dn_in_o}{1-D}$ $n_i:N_2/N_1$ $n_o:N_s/N_p$ $A=\frac{M+1+2ni+no+nino}{2+2ni+no+noni}$	AV_I	$A(2+3n_i+n_in_o)V_I$	1	2	2	2	5

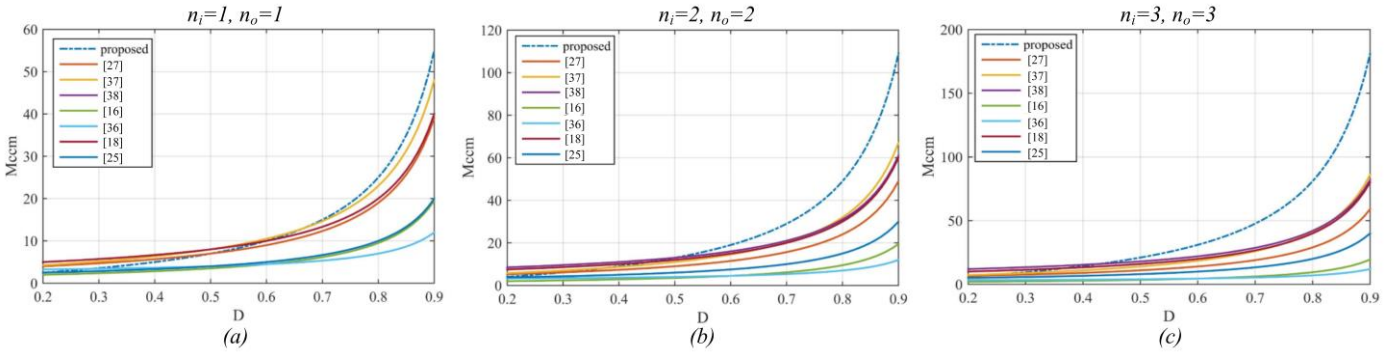

Fig. 8. Gain versus *d* in the proposed converter and other high step-up converters a) n_i=n_o=1 b) n_i=n_o=2 c) n_i=n_o=3

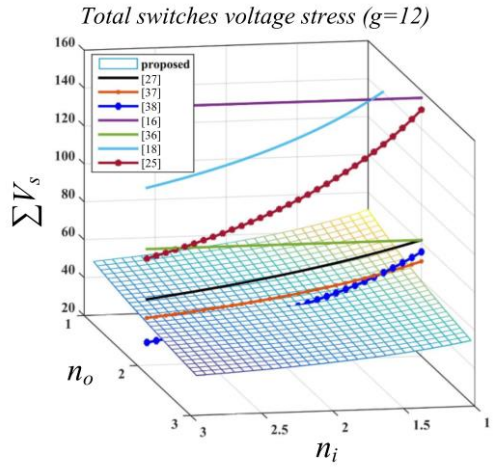

Fig. 9. Switch stress versus gain for the proposed converter and other high step-up converters

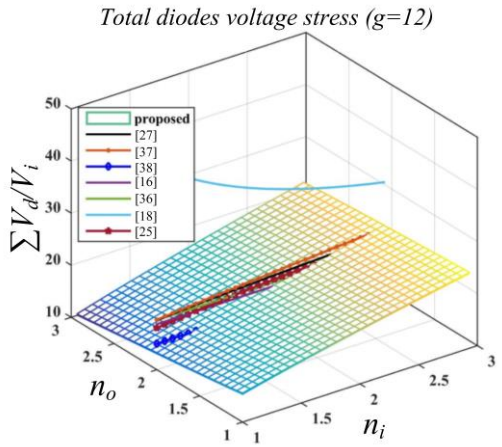

Fig. 10. Diodes stress versus gain the proposed converter and other high step-up converters

V. Experimental Results

A 200-watt prototype of the proposed converter was built and several tests have been done to evaluate its performance. The experimental setup of the proposed converter is shown in Fig. 11. The parameters of the experimental setup have been designed in accordance with the aforementioned equations and are stated in Table. II. For this evaluation, the duty cycle is considered around 0.65 and coupled inductors turn ratio is equal to 1:1. Total loss in the proposed topology with 4 different turn ratios of the coupled inductor is shown in Fig. 12. It can be seen that using a greater turn ratio of the coupled inductors leads to higher output voltage gain. On the other hand, the losses are increased as well as the efficiency is decreased in the proposed converter with higher turn ratios. Output voltage along with input voltage and current are shown in Fig. 13. The output voltage is equal to 300 V with 25 V input voltage, and the voltage gain corresponds to 12.

From Fig. 13, it can be seen that high output voltage is achieved with a middle duty cycle. In the theoretical analysis with the D=0.65, voltage gain equals 12.14 which has an acceptable difference with the experimental gain due to the voltage drop of the semiconductors and winding resistance.

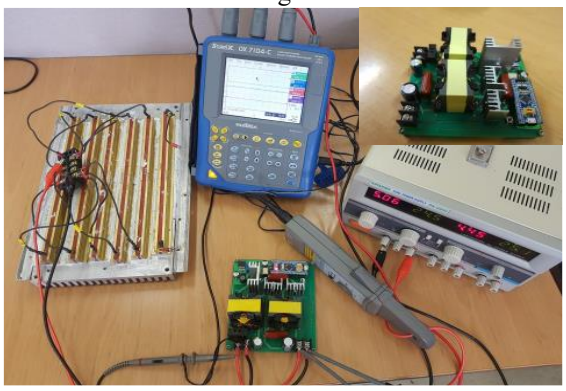

Fig. 11. The experimental setup of the proposed high step-up DC-DC converter

Table. II. Parameters of the proposed converter

Parameters	Value
Input Voltage (V_{in})	25 V
Output Voltage (V_o)	300 V
Output Power (P_{out})	200 W
Output Capacitor (C_o)	56 µF
Magnetizing Inductance of L_m	30 µH
Magnetizing Inductance of L_{mo}	400 µH
Turn Ratio for n_i and n_o	N_2/N_1=N_s/N_p=1
Power Switch	IRFP260
Diodes (D_1, D_2)	MUR2040, MBR20200
VMC Capacitors (C_1, C_2)	2.2 µF
Load Resistance (R_o)	450 Ω
Switching Frequency (f_{sw})	75 kHz

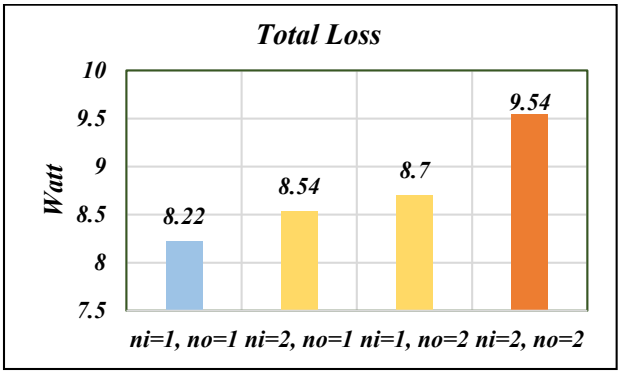

Fig. 12. Total power loss of the proposed topology with various winding turn ratios of the coupled-inductor

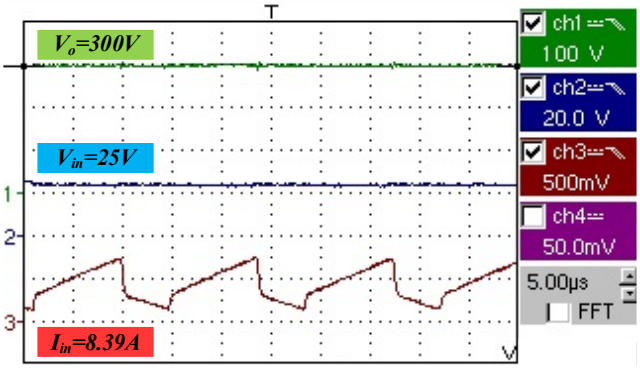

Fig. 13. Experimental result of the proposed converter 1:Output voltage 2: Input voltage 3:Input current

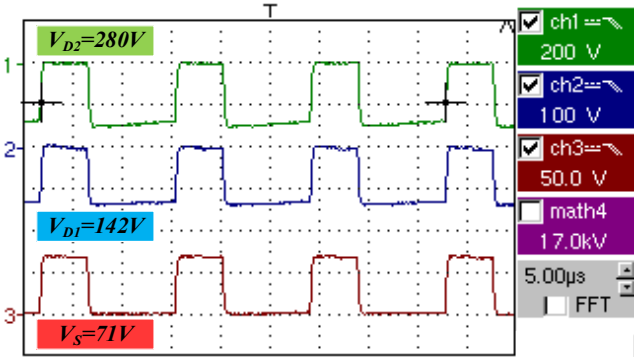

Fig. 14. Experimental result of the proposed converter 1: D_2 voltage 2: D_1 voltage 3: Switch voltage

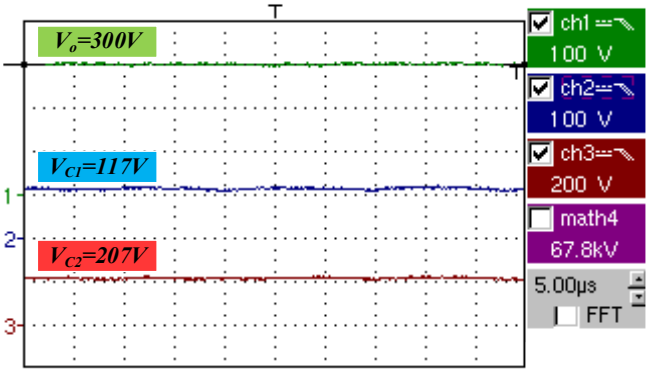

Fig. 15. Experimental result of the proposed converter 1: Output voltage 2: C_1 voltage 3: C_2 voltage

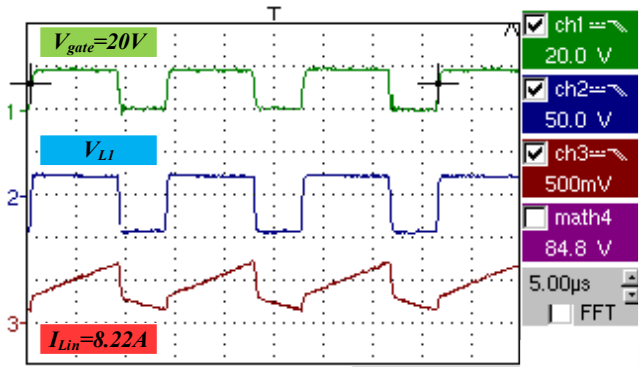

Fig. 16. Experimental result of the proposed converter 1: Gate signal 2: Output inductor voltage 3: Output inductor current

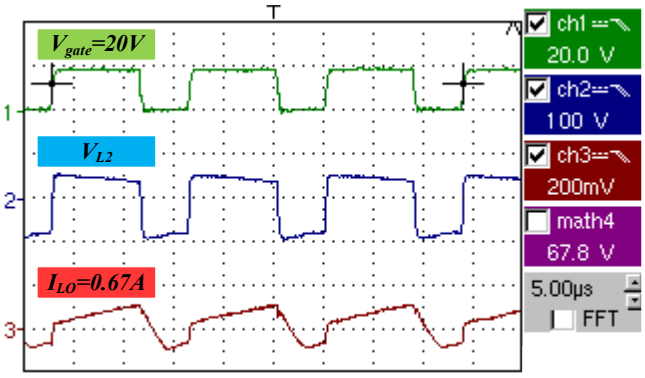

Fig. 17. Experimental result of the proposed converter: 1) Gate signal, 2) Input inductor voltage, 3) Input inductor current.

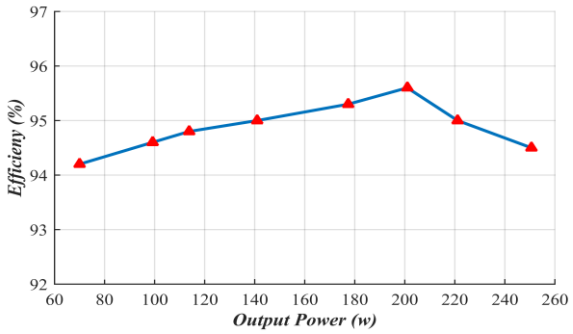

Fig. 18. Efficiency versus output power

The output power of the proposed converter is equal to 200W and the efficiency corresponds to 95.6%. for 8.3A input current. The voltage stress of the power switch and VM diodes are shown in Fig. 14. According to this figure, the voltage stress of the switch is around 71V which is considerably low compared to the output voltage. Hence, a switch with low voltage can be used that has a low on-resistance ($R_{DS\text{-}on}$). As a result, the conduction loss of the switch is low that leads to an increase in the efficiency of the proposed topology. Also, the voltage stresses of the VM diodes D_1 and D_2 are shown in Fig. 14. The voltage stress of diode D_1 is 142V and the voltage stress of diode D2 is 280 V which are closed to equations (24) and (25), respectively. As can be seen from Fig. 15, the voltages of capacitors C_1 and C_2 along with output voltage are depicted. The voltage ripples of these capacitors are low. Moreover, the value

of V_{c1} is 117 V and the value of V_{c2} is 207 V which correspond to equations (12) and (14), respectively.

Finally, the gate pulse along with magnetizing voltage and current of the input and output coupled inductors are shown i Fig. 16 and Fig. 17, respectively. In the turn-on state of the active switch, the current is increased among both coupled inductors. Also, the magnetizing inductance current is decreasing and discharging its saved energy into the circuit elements at the off state.

The efficiency while power increases from 70w to 250w is shown in Fig. 18. In the beginning, when the output power changes between 70w to 200w, the efficiency of the proposed converter is increased. The peak efficiency occurs at the 200W output power and its value is equal to 95.6%. Then, the efficiency is decreased due to the domination of copper and switching loss. However, in the proposed topology efficiency always is higher than 94% at all output power from70W to 250W. The breakdown loss of the proposed converter is shown in Fig. 19, and it can be seen that the prevailing power loss is related to the power switch.

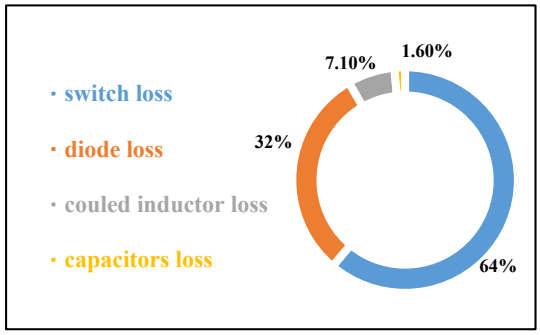

Fig. 19. Breakdown loss of the proposed converter

VI. Conclusion

In this paper, a new topology of a high step-up transformerless DC-DC converter with a voltage multiplier coupled inductor was introduced. The proposed converter consists of one modified boost converter and a new voltage multiplier structure. Voltage gain can be increased with an appropriate turn ratio of the CLs. The steady-state performance under the CCM condition has been presented. The total voltage stress of the active switches is decreased compared to other high step-up DC-DC converters. High voltage gain, low switching stress, three degrees of design freedom and uses of a single power switch are the significant advantages of the proposed topology. The experimental results were performed to evaluate theoretical analysis wherein high voltage gain 12 was obtained under 95.6% efficiency. Experimental results show high voltage gain along with low switching stress for the proposed topology.

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