THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

On-chip electrochemical capacitors and piezoelectric energy harvesters for self-powering sensor nodes

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Cover: On-chip electrochemical capacitors and piezoelectric energy harvesters as self-powering sensor nodes for applications of the world.

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“One can never have enough socks," said Dumbledore. "Another Christmas has come and gone and I didn’t get a single pair. People will insist on giving me books."

- J. K. Rowling, *Harry Potter and the Sorcerer’s Stone*

Abstract

On-chip sensing and communications in the Internet of things platform have benefited from the miniaturization of faster and low power complementary-metal-oxide semiconductor (CMOS) microelectronics. Micro-electromechanical systems technology (MEMS) and development of novel nanomaterials have further improved the performance of sensors and transducers while also demonstrating reduction in size and power consumption. Integration of such technologies can enable miniaturized nodes to be deployed to construct wireless sensor networks for autonomous data acquisition. Their longevity, however, is determined by the lifetime of the power supply. Traditional batteries cannot fully fulfill the demands of sensor nodes that require long operational duration. Thus, we require solutions that produce their own electricity from the surroundings and store them for future utility. Furthermore, manufacturing of such a power supply must be compatible with CMOS and MEMS technology. In this thesis, we will describe on-chip electrochemical capacitors and piezoelectric energy harvesters as components of such a self-powered sensor node. Our piezoelectric microcantilevers confirm the feasibility of fabricating micro electro-mechanical-systems (MEMS) size two-degree-of-freedom systems which can address the major issue of small bandwidth of piezoelectric micro-energy harvesters. These devices use a cut-out trapezoidal cantilever beam, limited by its footprint area i.e. a 1 cm^2 silicon die, to enhance the stress on the cantilever's free end while reducing the gap remarkably between its first two eigenfrequencies in the 400 - 500 Hz and in the 1 - 2 kHz range. The energy from the M-shaped harvesters could be stored in rGO based on-chip electrochemical capacitors. The electrochemical capacitors are manufactured through CMOS compatible, reproducible, and reliable micromachining processes such as chemical vapor deposition of carbon nanofibers (CNF) and spin coating of graphene oxide based (GO) solutions. The impact of electrode geometry and electrode thickness is studied for CNF based electrodes. Furthermore, we have also demonstrated an improvement in their electrochemical performance and yield of spin coated electrochemical capacitors through surface roughening from iron and chromium nanoparticles. The CVD grown CNF and spin coated rGO based devices are evaluated for their respective trade-offs. Finally, to improve the energy density and demonstrate the versatility of the spin coating process, we manufactured electrochemical capacitors from various GO based composites with functional groups heptadecan-9-amine and octadecanamine. The materials were used as a stack to demonstrate high energy density for spin coated electrochemical capacitors. We have also examined the possibility of integrating these devices into a power management unit to fully realize a self-powering on-chip power supply through survey of package fabrication, choice of electrolyte, and device assembly.

Keywords: Energy harvesting, Energy storage, MEMS, piezoelectric energy harvesters, 2DOF, Microsupercapacitors, graphene oxide, spin coating, sensor node

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Agin Vyas
Göteborg, March 2022

List of Publications

This thesis is based on the following appended papers:

Paper 1. **Agin Vyas**, H. Staaf, C. Rusu, T. Ebefors, J. Liljeholm, A. D. Smith, P. Lundgren and P. Enoksson. *A Micromachined Coupled Cantilever for Piezoelectric Energy Harvesters.* Micromachines (ISSN 2072-6669), no. 5 (2018): 252.

Paper 2. **Agin Vyas**, K. Wang, A. Anderson, A. Velasco, R. van den Eeckhoudt, M. Haque, Q. Li, A. Smith, P. Lundgren, and Peter Enoksson. *Enhanced electrode deposition for on-chip integrated micro-supercapacitors by controlled surface roughening.* ACS Omega 2020, 5 (10), 5219-5228

Paper 3. **Agin Vyas**, K. Wang, Q. Li, A. M. Saleem, M. Bylund, R. Andersson, V. Desmaris, A. Smith, P. Lundgren and P. Enoksson. Impact of electrode geometry and thickness on planar on-chip microsupercapacitors. In *RSC Adv., 2020, 10, 31435*

Paper 4. **Agin Vyas**, S. Z. Hajibagher, Q. Li, M. Haque, A. Smith, P. Lundgren, and P. Enoksson. Comparison of Thermally Grown Carbon Nanofiber-Based and Reduced Graphene Oxide-Based CMOS-Compatible Microsupercapacitors. In *Phys. Status Solidi B2021,258, 2000358*

Paper 5. **Agin Vyas**, S. Z. Hajibagher,U. A. Méndez-Romero, S. Thurakkal, Q. Li, M. Haque, R. K. Azega, E. Wang, X. Zhang, P. Lundgren, P. Enoksson, and A. Smith. Spin-coated Heterogenous Stacked Electrodes for Performance Enhancement in CMOS compatible On-chip Micro-supercapacitors. In *ACS Appl. Energy Mater. 2022*

Other relevant contributions co-authored by Agin Vyas:

B. Pamfil, R. Palm, **Agin Vyas**, H. Staaf, C. Rusu, and P. D. Folkow. *Multi-Objective Design Optimization of Fractal-based Piezoelectric Energy Harvester.* In 2021 IEEE 20th International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS), pp. 96-99. IEEE, 2021.

Agin Vyas, S. Z. Hajibagher, U. M. Romero, R. K. Azega, E. Wang, P. Lundgren, P. Enoksson, and A. D. Smith. *Alkyl-Amino Functionalized Reduced-Graphene-Oxide–heptadecan-9-amine-Based Spin-Coated Microsupercapacitors for On-Chip Low Power Electronics.* Physica status solidi (b) (2021): 2100304.

A. Velasco, **Agin Vyas**, K. Wang, Q. Li, A. D. Smith, P. Lundgren, and P. Enoksson. *Investigation of vertical carbon nanosheet growth and its potential for microsupercapacitors.* In Journal of Physics: Conference Series, vol. 1837, no. 1, p. 012006. IOP Publishing, 2021.

Q. Li, A. D. Smith, **Agin Vyas**, F. Cornaglia, A. Anderson, M. Haque, P. Lundgren, and P. Enoksson. *Finger Number and Device Performance: A Case Study of Reduced Graphene Oxide Microsupercapacitors.* Physica status solidi (b) 258, no. 2 (2021): 2000354.

Agin Vyas, Q. Li, R. van den Eeckhoudt, G. Geréb, A. Smith, C. Rusu, P. Lundgren, and P. Enoksson. *Towards Integrated Flexible Energy Harvester and Supercapacitor for Self-powered Wearable Sensors.* In 2019 19th International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS), pp. 1-6. IEEE, 2019.

A. D. Smith, Q. Li, **Agin Vyas**, M. Haque, K. Wang, A. Velasco, X. Zhang, S. Thurakkal, A. Quellmalz, F. Niklaus, K. Gylfason, P. Lundgren, P. Enoksson. *Carbon-Based Electrode Materials for Microsupercapacitors in Self-Powering Sensor Networks: Present and Future Development*, Sensors 19.19 (2019): 4231.

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Q. Li, A. D. Smith, M. Haque, **Agin Vyas**, V. Kuzmenko, P. Lundgren, P. Enoksson. *Graphite paper/carbon nanotube composite: A potential supercapacitor electrode for powering microsystem technology*, Journal of Physics: Conference Series, 922 (2017) 012014

List of Acronyms

CMOS	–	Complementary metal–oxide–semiconductor
IoT	–	Internet of things
AIoT	–	Artificial Internet of things
MEMS	–	Micro-electromechanical systems
SoC	–	System on chip
FPGA	–	Field Programmable Gate Arrays
ADC	–	Analog-to-digital converter
EDL	–	Electric double layer
RF	–	Radio frequency
PV	–	Photovoltaic
RFID	–	Radio frequency identification
DC	–	Direct current
PEH	–	Piezoelectric energy harvester
MPEH	–	Micro piezoelectric energy harvester
PZT	–	Lead zirconate titanate
MB	–	Micro-battery
MSC	–	Micro-supercapacitor
EDLC	–	Electric double layer capacitor
FEOL	–	Front-end-of-line
BEOL	–	Back-end-of-line
IC	–	Integrated circuit
VLSI	–	Very large scale integration
MOSFET	–	Metal oxide semiconductor field effect transistor
UV	–	Ultraviolet
2DOF	–	Two degrees of freedom
1DOF	–	One degree of freedom
nDOF	–	Multiple degrees of freedom
CNC	–	Computerized Numerical Control
FOM	–	Figure-of-merit
PDMS	–	Poly(dimethylsiloxane)
PVDF	–	Polyvinylidene fluoride
MKS	–	Mass spring damper
FUC	–	Frequency up-conversion
DRIE	–	Deep reactive ion etching
SOI	–	Silicon on insulator

SiP	–	System-in-package
PCB	–	Printed circuit board
EMIMAc	–	1-Ethyl-3-methylimidazolium acetate
CV	–	Cyclic voltammetry
GCD	–	Galvanostatic charge-discharge
EIS	–	Equivalent impedance spectroscopy
CVD	–	Chemical vapor deposition
MPCVD	–	Microwave Plasma-enhanced Chemical Vapor Deposition
SiNW	–	Silicon nanowire
CNT	–	Carbon nanotubes
VACNT	–	Vertically aligned carbon nanotubes
rGO	–	Reduced graphene oxide
GO	–	Graphene oxide
PET	–	Polyethylene terephthalate
PANI	–	Polyaniline
CAD	–	Computer aided design
PEDOT:PSS	–	poly(3,4-ethylenedioxythiophene) polystyrene sulfonate
CNF	–	Carbon nanofibers
EPD	–	Electrophoretic deposition
ZIF	–	Zeolitic imidazolate framework
MOF	–	Metal organic frameworks
DVD	–	Digital Video Disc
LSG	–	Laser scribed graphene
CMEMS	–	Carbon micro-electromechanical systems
PPy	–	Polypyrrole
EMIM-TFSI	–	1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide
PVD	–	Physical vapor deposition
PVA	–	Poly(vinyl alcohol)
HMDS	–	Hexamethyldisiloxane
HD9A	–	Heptadecan-9-amine
ODA	–	Octadecanamine
TMP	–	Trimethylolpropane
PEGMA	–	Polyethylene glycol monomethacrylate
BEMA	–	Behenyl Methacrylate
TMOS	–	Tetramethyl orthosilicate

Contents

Chapter 1

A self-reliant on-chip power supply

1.1 Introduction

The advancements in microelectronics with the miniaturization of transistors through complementary metal-oxide-semiconductor (CMOS) technology have enabled the innovation of intelligent sensors and microprocessors as in mobiles, computers, cameras, and vehicles. These sensors can potentially communicate with each other forming a hive-like grid. Such a grid could constitute a part of the Internet of things (IoT) [1]. IoT can influence all sectors of life with application areas ranging from home, health, industry, transport, energy and construction (Figure 1.1). With the advent of fifth-generation wireless systems and artificial intelligence, IoT can make a combination of sensor networks into an artificial intelligence of things (AIoT) to collect, process, analyze, store, and control data [2].

Sensor networks are central to making decisions in complex systems that are designed to be intelligent [3]. These decisions are based on active measurement methods that are used in sensors. Such a procedure could be determining the change in electrical current based on the changes in physical conditions such as position, length, mass, resistance, and vibrations [4]. These physical conditions are manifestations of the environment surrounding the sensor. At home, our entertainment systems are using microsystems for communicating with our phones or controls that are powered (directly or indirectly) by our household electricity supplies [5].

Similarly, alarm systems and cameras are connected to phones and tablets of homeowners [6]. In healthcare, these networks can improve assisting patients in critical conditions in a more efficient manner [7]. Biological functions of the body can be measured during invasive surgeries in medicine [8]. Industries have already started adopting the IoT technology within the frames of another acronym called 'Industry 4.0'. Several reports address the importance of non-stop communication between automation, processes, and distribution while avoiding subjecting humans to the risks that such environments pose [9]. The sustainability of factories can be enhanced by measuring real-time environmental factors such as temperature, humidity, factory output, thereby potentially minimizing maintenance costs. Transportation is another area where IoT applications range from vehicles train condition monitoring to track and road sensing [10].

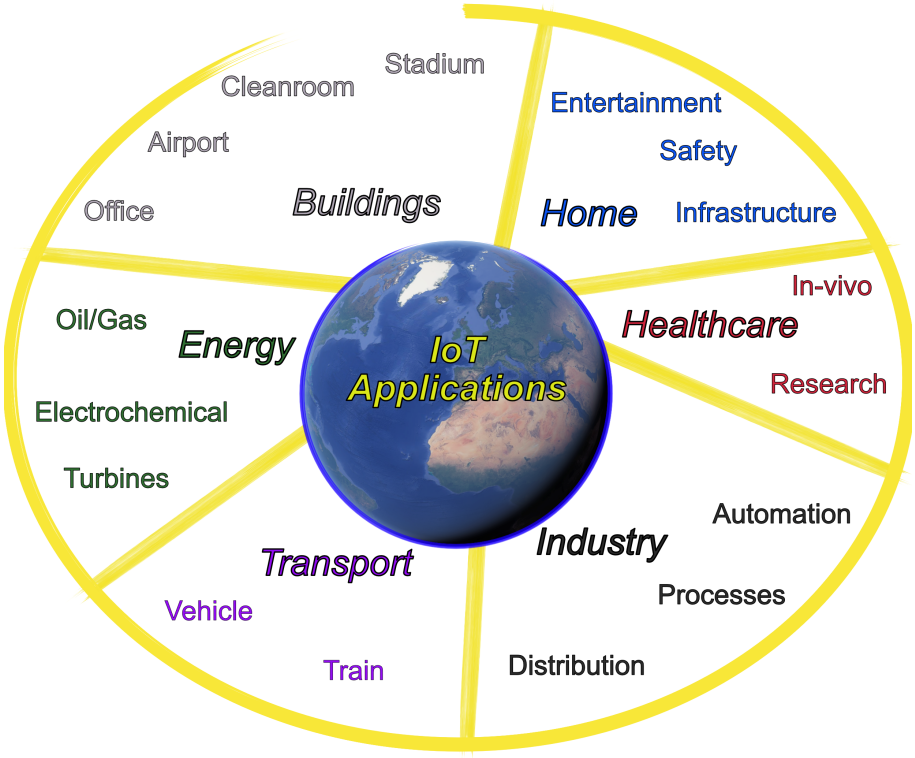


Figure 1.1: IoT applications that encompass our every day life.

The hardware implementation for these IoT applications varies depending on the application in question. It can vary from a circuit board implementation with a battery as power supply connected to a sensor and a micro-controller unit [11] to 3D stacking or chip-level integration of devices to complete system-on-a-chip hardware implementation [12]. As the trend of demands in technologies communicating with each other increases with wearable, smart-home, health, and manufacturing devices, the projected number is about 500 billion IoT devices by 2030 [13]. Wireless sensor networks will be pervasive with continued fast progress in developing miniaturized devices such as portable electronics, micro-electro-mechanical systems (MEMS), CMOS technology in nearly all aspects of our lives. The usefulness of these devices is, however, limited depending on their supply of power [14]. Devices powered by batteries require the replacement of the power supply if they are to continue operating beyond the battery's lifetime. Therefore, there is an increasing interest in self-powered sensors and communication devices with a lifetime that is not limited by their power supply. A review of capabilities of sensors and actuators designed through MEMS technology is presented in Wilson et al.[15].

1.2 Wireless sensor nodes

This section will describe the components of a wireless sensor node and their power requirements for autonomous sensing and data transfer. A sensor node is a composition of four units, as shown in Figure 1.2. These units can be categorized as follows -

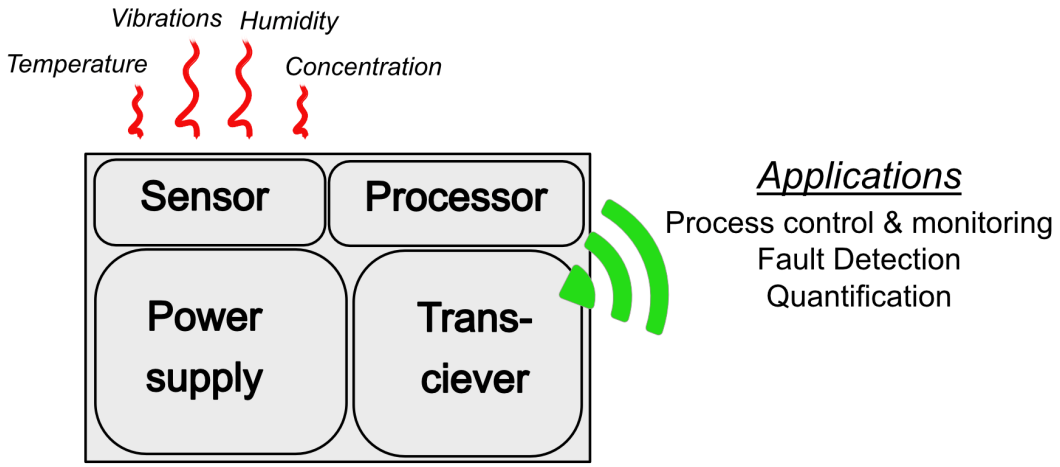


Figure 1.2: Schematic of a wireless sensor node.

transceiver, processor, sensor, and power unit.

The transceiver combines a transmitter and a receiver that can send and receive signals. It is typically a high power consuming component of the sensor system. The transceiver is connected to a processing unit that comprises a system on chip (SoC) and storage. A processor performs the basic arithmetic, I/O operations, and logic operations alongside allocating commands for the different components running in the system. It is in charge of signal processing such as modulation, demodulation, compression and controls memory access, communication and power management. The processor unit is also connected to the sensing unit. The sensing unit is typically made up of a sensor and a unit that converts analog signals into digital called the analog-to-digital-converter (ADC). The sensor senses the physical information of its surrounding manifesting as an analog electrical signal. The digital information representation provided by the ADC is stored and processed in the processing unit. There can be other subunits, too, depending on the type of application. Through CMOS technology, the power consumption of sensor systems can be kept low while also enabling miniaturized devices.

The final unit in the sensor node is the power unit. The power unit must be able to provide power to the sensor node subsystems during passive and active working hours. The utilization of batteries is often deterred by their short lifetimes. Therefore, there is a need for self-sustaining power supplies that harvest their energy from the surroundings and store it in electrochemical capacitors. This would ensure an independent maintenance-free, autonomous and continuously operating sensor node. Some configurations of a power supply can be combinations of various ambient energy harvesting and energy storage devices with a PMU connecting their respective output or input. Such a schematic can be seen in Figure 1.3.

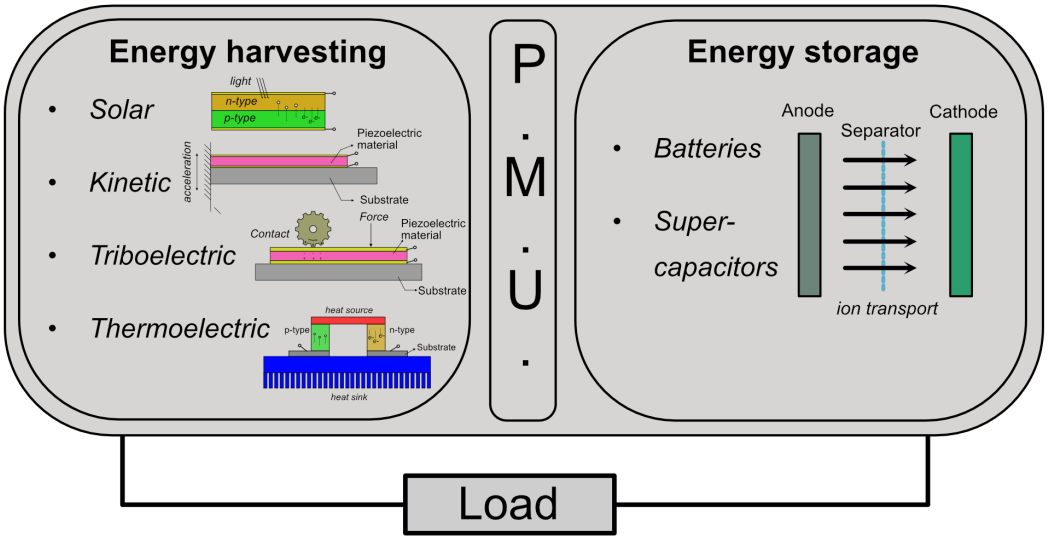


Figure 1.3: Schematic of a power supply with various energy harvesting and energy storage technologies combined through a power management unit.

1.2.1 Power requirements for on-chip sensors and transducers

This section discusses the power requirements of various micro-controller and communication units presented in the literature for on-chip sensor nodes. According to the overview of the field presented by Mayer [16], the power requirements for communication technologies to transmit information is 10 mW. With recent advancements in micro-controller technology, microelectronic circuits can operate at minimum power requirements of 100 μW to 10 mW [17]. To further reduce the power requirements of the sensor nodes, various on-chip processors can be implemented to transfer the outcome of processing data collected rather than transmitting all of the raw data for analysis [16].

Traditionally, a sensor node requires power at all stages of operation - sensing, data processing, and data transfer mode. The fraction of total time required for sensing, processing, and delivery comprises the duty cycle of the sensor node. The sensor node is awakened intermittently to transmit information during the duty cycle while sleeping on other occasions. However, to capture real-time changes in the environment, an Always-ON fourth stage is suggested for the sensor node with an automatic surge in power input to the processing and transceiver units to notify the network of the detection of changes immediately. This requirement would require the sensor node to be self-powered with the challenge of delivering nW to mW power at all times.

Batteries are currently being used as power supplies in many different applications. These devices are desirable for their relatively high energy densities. More recently, work in microbatteries has resulted in significant advancements in their rate capability and power density. Electrochemical capacitors or supercapacitors, on the other hand, are governed by two differing mechanisms - electric double layer (EDL) or redox (pseudocapacitive) behavior [18]. These devices have very high power densities and extremely long lifetimes due to their non-reactive nature of storing charge. Supercapacitors, however, need an energy harvesting source to store electrical energy.

Based on the properties of the energy storage device, the energy harvesting system can be chosen based on the following key metrics - size, operation lifetime, frequency (in case of vibrational harvesters) and power. The self-sustaining power supply can function on two mechanisms - harvest environmental surplus energy and use directly or harvest, store and use later. In the former mechanism, the energy harvester powers the sensor units directly. This requires a harvester to function continuously and generate an electrical output resembling a direct current. Thus, with the latter, the harvested energy can be stored in electrochemical capacitors or charge a battery and then the stored energy is supplied to the sensor node for operation. The energy stored in the electrochemical capacitors can also be used in later cycles as per application requirements.

Energy harvesting can make use of energy present in the environment in the form of solar, wind, thermal, or vibrational energy and convert it into usable electrical energy [19]. These energy sources will never deplete as long as the earth is rotating and revolving around the sun. Energy storage units are any devices that can store this electrical energy in the form of charge and then supply it to the system when needed [20]. Since most common microelectronic devices used to construct a sensor node are fabricated through CMOS technology, it would be an advantage for prospects of integration, cost reduction and miniaturization if the power unit's fabrication process would be compatible with this technology.

Integration of such energy harvesting based power supplies into an IoT platform would be fully in line with the ambitions of providing a sustainable development [21, 22]. For energy harvesters and supercapacitors to be implemented in wireless sensor nodes, they must fulfill size, power density, performance, and lifetime requirements. First, they must be small enough, sometimes as small as a cubic centimeter [23] (and be light enough at the same time). Secondly, the supercapacitor should present low losses in power. Thirdly, they require sufficiently low production costs, and finally, as these sensor nodes are to be used in often inaccessible places, the lifetime of these devices must be prolonged.

1.3 Energy harvesting

Let us consider the energy harvesting unit as the first component of the on-chip power supply. This unit converts forms of energy present in their environment into usable electrical energy through various physical mechanisms. These mechanisms can be, for example, photovoltaic (PV), piezoelectric, thermoelectric, triboelectric, or radio frequency (RF) [19]. This section will provide a concise summary of various energy harvesting technologies that are compatible with CMOS-MEMS technology. Based on their bendability, output power, conversion efficiency, ON/OFF times, size, and challenges, the harvesters will be compared.

1.3.1 Solar energy harvesting

Solar energy is one of the most abundant forms of energy in our solar system. The conversion of light to electrical energy can be clean, non-destructive, and practically

infinitely replenishing. When light is incident on a solar cell, electrical energy is released as an output from the absorption of a photon in the semiconductor lattice. This effect is called the photovoltaic effect. The efficiency of the solar cell is determined by the ratio of total output to input energy. Solar based energy harvesting has emerged as the most viable solution for ambient energy harvesting to supplement batteries and supercapacitors. There are three significant devices used for solar energy harvesting - silicon-based solar cells, dye-sensitized solar cells, and organic solar cells, as shown in Figure 1.4.

Silicon solar cells are the most produced and commercialized devices efficiencies reported in research. The highest conversion factor is 25 %, while commercial devices report 15 - 18 % efficiency. These devices are fabricated in large-scale CMOS compatible processing labs. Their process plan uses photolithography, doping, and various other technologies to develop components with a high wafer yield on a silicon substrate. Figure 1.4(a) shows different silicon solar cells. Dye-sensitized solar cells are another form of solar harvesting device that has attracted some attention as promising candidates for alternates to silicon PVs. These devices are semi-flexible and semi-transparent, properties most suited for flexible electronics as shown in Figure 1.4(b). In practical applications, they have reported a maximum conversion efficiency of 15 %. Due to their flexible nature, the encapsulation of an aqueous electrolyte becomes a challenge that requires engineered solutions for further improvement. Organic solar cells are relatively new PV device which utilize polymeric chains of molecules in the light to electricity conversion to obtain low-cost photovoltaics, in Figure 1.4(c). They are rather easy to manufacture as they require vacuum evaporation or filtration as their methods of electrode deposition. They are also unstable, i.e. the organic photovoltaic material can degrade [24]. They are considered inefficient compared to PVs of hard materials, with their overall efficiency up to 10 %.

1.3.2 Thermoelectric energy harvesting

Thermoelectric energy harvesting can use the waste thermal energy present in the surroundings of machines, mines, industries, and even the human body. There are two main principles of thermal energy harvesting. The first principle of harvesting involves the thermoelectric effect [28]. In this principle, the device utilizes the Seeback effect that drives the diffusion of electrons over a temperature gradient. The thermoelectric energy harvesters have been developed to produce energy from temperature gradients on human body. The harvester can reliably operate at ambient conditions while indicating 20 μW cm^{-2} [29]. The prototype could also demonstrate energy harvesting during nighttime conditions. This is a significant advantage over solar PVs.

Thermoelectric generators are easily fabricable, robust, compact, and fatigue proof as they do not involve any moving parts. These devices are desirable in areas where the thermal gradient is large. The second method of thermal harvesting involves the pyroelectric effect. This effect is a combination of charge generation due to polarization through temperature leading to a piezoelectric effect induced in the material [30].

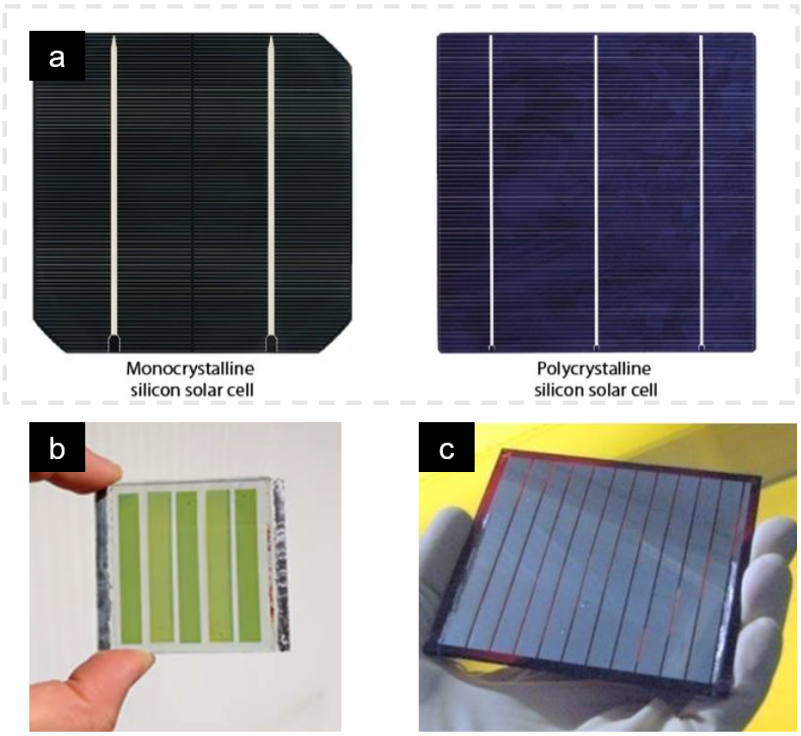


Figure 1.4: (a) Silicon solar cells fabricated on mono and poly crystalline silicon, reproduced from Saga et al. [25], (b) Dye sensitized solar cell fabricated by Huaulme et al. [26], (c) Organic photovoltaic cell manufactured at Solarmer [27]. Images reproduced after permission from the respective authors or publishing agencies.

1.3.3 RF energy harvesting

RF energy harvesting is yet another form of energy harvesting through RF waves present in the environment. The idea of limitless extraction of power from RF interactions has been quite widely adopted in radio frequency identification (RFID) badges. The same principle can be applied in the case of energy harvesting devices for IoT sensor nodes. [31]

The RF harvester is a circuit consisting of an antenna that receives the signal, followed by an impedance matching circuit and rectifier connected to an energy storage unit or sensor load. The antenna captures the RF signal propagating in a wireless transmission medium. Maximum power is extracted from the antenna through the impedance matching circuit and converted to direct current (DC) via the rectifier. If the voltage from the rectifier is lower than required, then the circuit can have a voltage multiplier as a component as well. The output from the rectifier is led to the storage unit of the sensor node. The largest RF harvested power of 62 μW was verified through a ten capacitor circuit with a voltage multiplier [32]. The prototype could power a portable calculator at a low charging speed.

The RF harvesters can be used for short burst of power applications. Like the principle of RFID tag, the harvesters can be combined with various flexible electronics that can be used for smart skin health applications. Similarly, such devices can be used

in weather monitoring stations, or lighting LEDs.

1.3.4 Triboelectric energy harvesting

Triboelectric energy harvesting is based on the contact electrification effect in which electrical energy is generated from mechanical contact of material surfaces. The material surface becomes electrically charged after coming in contact with another material surface. The charge transfer between the two materials is facilitated by friction between the surfaces. The transferred charge can then be collected at the current collectors through the induced potential difference. The electricity is generated by frequent contact between the two material surfaces [33].

There are four different operation modes for triboelectric harvesters based on their electrode configuration - vertical contact, lateral sliding, single electrode, and free-standing. In vertical contact mode, the two material surfaces interact with each other in-plane, normal to the direction of motion. Figure 1.5(a) shows one such triboelectric nanogenerator fabricated by Zhang et al. [34]. The device can produce up to 53 mW cm^{-3}. One material interface moves in the plane direction parallel to the surface in lateral sliding mode. Pang et al. [35] designed a lateral triboelectric generator that was an acceleration sensor as well. Figure 1.5(b) shows the schematic image of the designed harvester/sensor. The single electrode method is similar to the contact mode method. However, it is applicable in certain areas where there is a requirement of only one electrode. Figure 1.5(c) shows a device demonstrated by Yang et al. [36] which can deliver up to 500 mW/m^2 from a force input of human touch. The free-standing mode, finally, is based on the principle of potential difference formed between the top and bottom material interface [37].

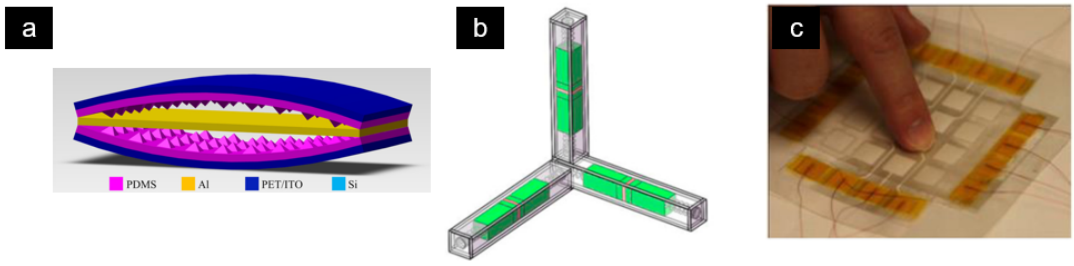


Figure 1.5: Various types of triboelectric energy harvesters (a) Vertical contact electrodes developed by Zhang [34], (b) lateral design from Pang et al. [35], (c) single electrode device by Yang et al. [36]. Images reproduced after permission from the respective authors or publishing agencies.

1.3.5 Piezoelectric energy harvesting

Kinetic energy harvesting of mechanical energy to electrical energy can be implemented through the piezoelectric effect. The piezoelectric effect is present in many materials with a crystalline structure. The deformation of crystalline structure in the presence of stress or strain causes the electric charge propagation through changes in the charge

distribution of the piezoelectric material. The material is layered on a stressed structure. Therefore, piezoelectric vibrational harvesters are potential candidates for devices that can provide electrical energy for IoT sensor nodes.

While piezoelectricity is not the only conversion mechanism for mechanical to electrical energy, piezoelectric energy harvesters (PEH) have the maximum energy density and a high energy conversion efficiency [38] compared to other kinetic energy harvesting mechanisms such as electrostatic and electromagnetic transduction. They have a simple configuration that can utilize MEMS technology for their fabrication. PEHs also do not require any input voltage for starting up compared to the electrostatic and electromagnetic harvester [39, 40]. Thus, they can be considered potential candidates for powering miniature devices and wireless sensors.

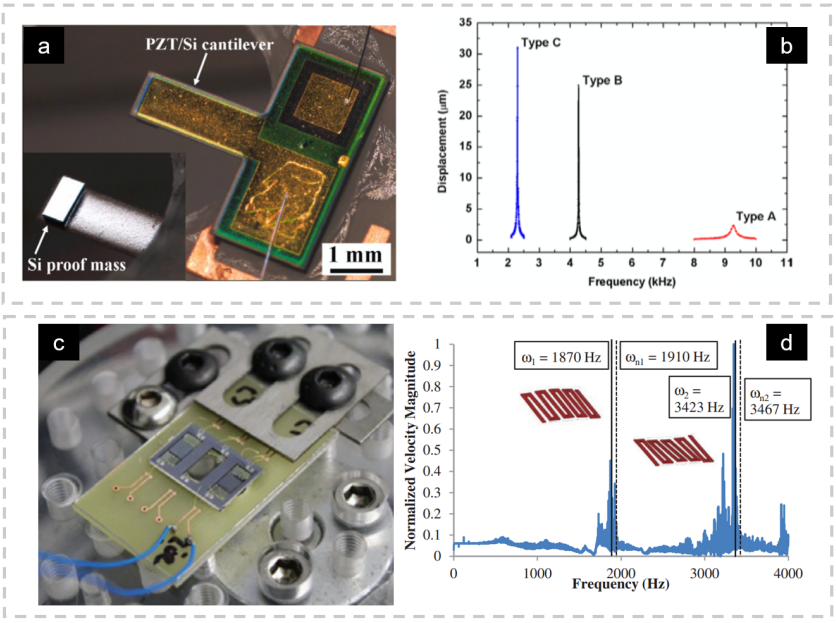


Figure 1.6: MEMS on-chip vibrational energy harvesters: (a) Single cantilever beam produced by Isarakorn et al. [41], (b) output of cantilever beams with 0.5 μm epitaxial PZT layer. (c) Folded spring energy harvesters fabricated by Lueke et al. [42] (d) The harvester has the potential to generate energy over a wide range of vibrational frequencies. Images reproduced after permission from the respective authors or publishing agencies.

Micromachined piezoelectric energy harvesters (MPEH) can provide the necessary power to the sensor node in the presence of vibrations at its resonant frequency. PEHs usually consist of a free-standing cantilever beam fixed to one end. The beam surface is covered by piezoelectric material, either on both sides. Isarakorn et al. [41] fabricated and experimentally characterized a cantilever beam with a-Si proof-mass to generate an output of 13 μW g^{-2} at an output current of 48 μA g^{-1} at a resonant frequency of 2.3 kHz (Figure 1.6(a)) where g is the gravitational acceleration. The output of the energy harvester fabricated is shown in Figure 1.6(b). Although the energy harvester can provide the necessary output for charging sensor nodes, the q-factor of the output is too high. Any deviations from the natural frequency of the design would lead to a significant loss of output. Several solutions for solving this issue have been presented in the literature.

Among them, multi-degree-of-freedom cantilevers provide the necessary improvement in power bandwidth of the energy harvesters of the significant stress present on its surface over a range of frequencies, determined by the complex vibrational response of a system with many eigenmodes [42]. Folded spring harvester shown in Figure 1.6(c, d) can harvest electricity at frequencies from 45 Hz to 3.6 kHz. However, due to a thin lead zirconate titanate (PZT) layer, their maximum output could reach up to 0.6 μW at 226 Hz.

1.4 Energy storage

The second principal component of an on-chip power supply is the energy storage unit. The energy harvesters gather the energy from ambient sources in the surroundings and deliver it to the power conditioning unit. The energy storage unit is then connected to the output of the power conditioning circuit, which provides a steady DC output. First chosen as primary energy storage systems were rechargeable batteries such as NiMH [43] and Li-ion [44]. While rechargeable batteries show high capacity and low leakage, the wireless sensor life is limited by the cycle life of rechargeable batteries [45]. The cycle life of a battery is the number of charge-discharge cycles it can go through before its capacity drops below 80 % of its maximum capacity. The residues from the electrode-electrolyte reaction age the device by increasing the internal resistance over a period of time. However, in reality, at the end of its cycle life, the battery's capacity can reach up to 50 % or even 20 % in some cases. Potential solutions to increase the lifetime, such as increased mass loading of the electrodes [46], reducing the reaction rate between the electrode and electrolyte [47] lead to an undue increase in the size of the device and also leads to potential trade-offs in various other sectors such as safety. Due to this, a WSN would require replacement after not even 1-2 years. Batteries also contain harmful chemicals resulting in environmental pollution [48]. However, various measures are being undertaken to mitigate these ill effects. Supercapacitors have emerged to be successful technological tools in storing charge. They have a higher cycle life than batteries, and in recent years, their energy storage performance has been confirmed to be equivalent to the low-end commercial batteries [49][50]. Supercapacitors can reduce the load on batteries by acting as a smoothing capacitor.

Batteries and supercapacitors, despite their trade-offs, can hold a sufficient application charge from the incoming power from energy harvesting sources. As there is a specific constraint on the size of the power supply intended for IoT sensor nodes, miniaturized devices called micro-batteries (MBs) and microsupercapacitors (MSCs) have the potential to be integrated into such systems. As the miniaturization concept of these devices is still in an exploratory phase, generally, these devices have a total footprint area from anywhere between 1 mm^2 to 10 mm^2. The same definition can be applied for flexible MBs and MSCs. However, to limit our deliberation, we will be focusing on solid-state solutions to manufacturing these devices. There are two main configurations of MBs and MSCs - stacked and planar. The electrolyte and separator are sandwiched between two electrodes deposited on the same footprint geometry in a stacked configuration. All the components lie on the substrate plane in the planar devices, and no separator is required, thanks to separation between the electrodes. The

following sections will describe MBs and MSCs that can be potentially integrated into an on-chip power supply with an energy harvesting unit.

1.4.1 Microbatteries

MBs generally provide energy through reversible redox reactions, typically slow. The redox reactions can further be categorized into insertion, alloy, and conversion types reactions. MBs typically establish very high energy densities ranging from 20 to 200 mWh cm^{-3} with a low self-discharge current.

Among the architectures, stacked and planar MBs, stack MBs were developed in the initial stages of technology development. The electrodes, electrolytes and separator are stacked over the same footprint area. The anodes typically require metal oxides such as V_2O_5 or lithium transition metal-oxides ($LiCoO_2$, $LiMn_2O_4$, $LiNiCoO_2$), but polyanion compounds and olivine electrodes can also be considered as anodes. For the electrode that undergoes reduction when the battery delivers power (cathode), typical materials involve graphite or porous carbon like carbon-based materials. Silicon, lithium and titanium compounds such as TiO_2, $Li_4Ti_5O_{12}$ are also applied as cathodes. Stacked MBs require solid-state or gel electrolytes for ion-conduction as liquid electrolytes run the risk of short circuits in an on-chip circuitry. Solid-state electrolytes for stacked MBs include lithium lanthanum titanium oxide compounds such as $Li_{3x}La_{2/3-x}TiO_3$, lithium niobium silicon oxides ($LiNbO_3-SiO_2$,$Li_2-P_2S_5$), lithium phosphates, lithium phosphorus oxynitrile (LiPON) and certain polymers as electrolytes [51]. Typically, the electrolytes have low ion conductivity, which is detrimental to power density. The materials for electrodes and electrolytes are traditionally deposited through micromachining processes such as sputtering [52], electron beam evaporation [53], chemical vapor deposition [54], sol-gel method [55] and atomic layer deposition [56].

Planar MBs have the electrodes parallel to each other on a substrate with a liquid or solid electrolyte for ion transportation. Typically, the electrodes are interdigitated patterns of metal current collectors on which the anode or cathode is deposited. This kind of electrode geometry allows for faster ion transportation related to redox reactions, thereby increasing the power density of the device. However, as the design is planar, the footprint area of the MBs is halved for a single electrode which leads to a reduction in energy density compared to stacked MBs. Typically the anodes and cathodes of planar MBs are deposited through electrodeposition [57] and electroplating [58]. Typical materials used for anodes involve nickel-tin alloys, nickel scaffolds, $Li_4Ti_5O_{12}$, or graphene while cathodes utilize, manganese oxide, $LiFePO_4$, MoS_2 as cathodes.

Some examples of MBs are shown in Figure 1.7. Nakano et al. [59] designed interdigitated cells for MBs using $LiMn_2O_4$ and $Li_{3/4}Ti_{5/3}O_4$ for the cathode and anode respectively. The MBs demonstrated an operational voltage of 2.45 V. The device is shown in Figure 1.7(a). An example of a stacked MB is shown in Figure 1.7(b). The authors in this work [60] deposited the materials bottom-up using a direct-write printing method. The discharge capacity was measured at 0.98 mAh cm^{-2}. The energy density of the device was 1.2 mWh cm^{-2}. 3D printed MBs using lithium tantalum oxide and LFP as electrodes were indicated by Sun et al. [61] using a 30 μm printing nozzle.

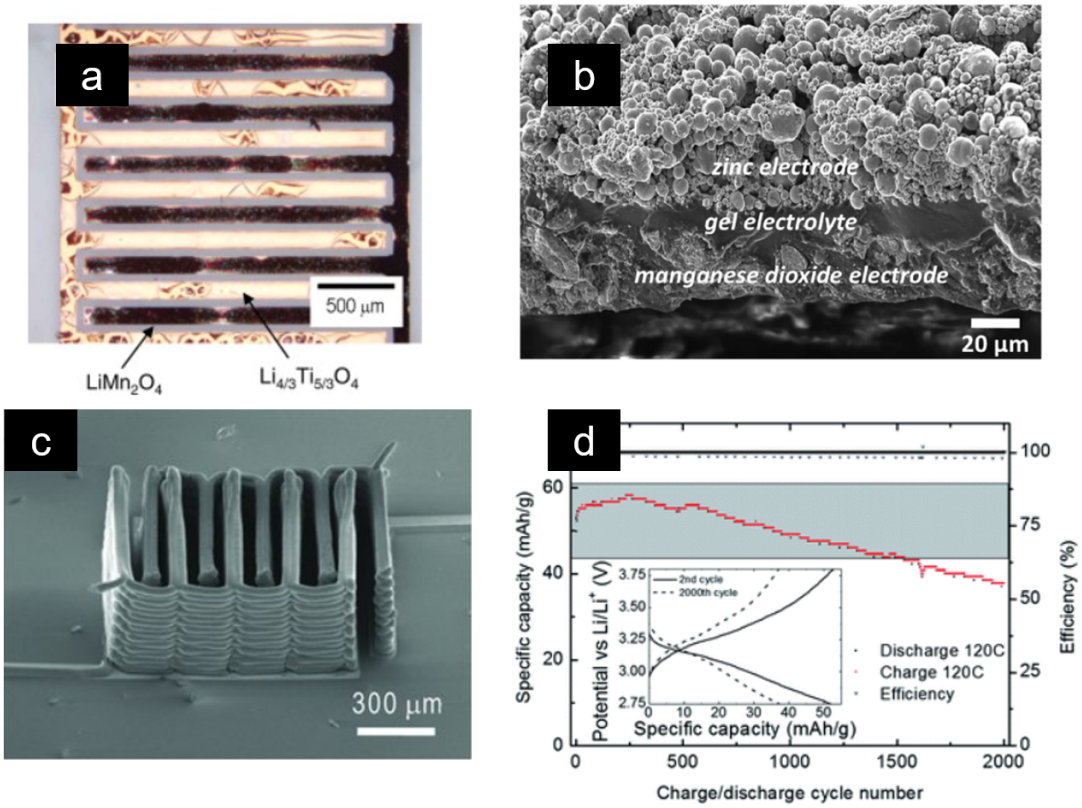


Figure 1.7: Examples of MBs present in literature: (a) planar MB fabricated by Nakano et al [59] using solution based deposition of electrodes, (b) stacked MBs fabriceted by Ho et al. [60] using screen printing, (c) 3D printed MB by Sun et al.[61]. (d) Example of poor cyclic capability of MBs with V_2O_5 as electrodes. Images reproduced after permission from the respective authors or publishing agencies.

Although there have been significant advancements in MBs, several challenges require considerable attention for improvement in their power density and cyclic stability before being a viable solution for a self-reliant power supply. An example of the cyclic lifetime of a battery is shown in Figure 1.7(d). The V_2O_5 MB electrodes fabricated by Nilsen et al. [62] lose the specific capacity by 33 % by 1500 cycles. Suppression of redox reaction by-products such as the dendritic formation of lithium and zinc is also an issue that needs to be tackled [63]. Optimization of solid-state electrolyte ion conductivity, stability, and non-flammability are a few problems with current electrolytes applied in MBs. Thus, we require more sustainable and stable solutions for energy storage.

1.4.2 Microsupercapacitors

MSCs are another form of supercapacitors that store or generate charge through electrical double layer capacitance (EDLC) or redox mechanism (pseudocapacitance) at the electrode-electrolyte interface. In the EDLC mechanism, the electrolyte ions are attracted to the positive and negative electrodes of the device, where they form nano-capacitors at the electrode interface with the electrode surface. During EDL behavior, the electrodes and electrolytes interact non-invasive to form nano-capacitors at their

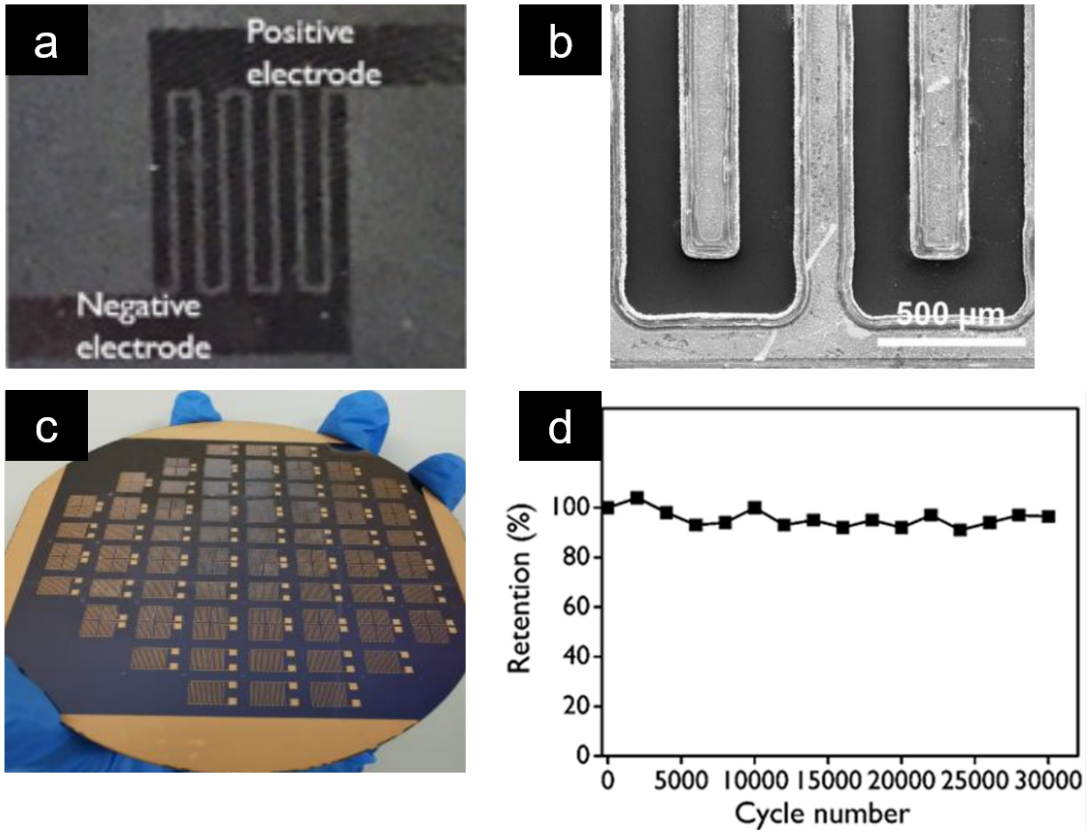


Figure 1.8: (a) Laser scribed graphene based MSC fabricated by Kim et al. [64] , (scale = 1 μm) (b - c) 3D mesoporous gold fabricated by electrodepostion by Wang et al. [65], (d) Example of cyclic stability of a MSC using C/MnO_2 as electrodes by Wang et al. [65]. Images reproduced after permission from the respective authors or publishing agencies.

interface. This allows the supercapacitor to store more charge per unit area than conventional capacitors. In pseudocapacitance, the electrode and electrolyte interact in the form of a redox reaction to store the input charge acquired from an energy harvesting/power conditioning output. MSCs are considered an alternative to MBs due to their extremely long cycle life (over 10^6 cycles) and high power density.

The architecture of MSCs is also similar to MBs, as discussed in the earlier section, categorized into the stack and planar structures. Stacked MSCs suffer from the problems encountered in stacked MBs, such as low ionic conductivity inability to utilize ionic or aqueous electrolytes. Similarly, issues with short-circuiting of electrodes are more evident in MSCs than MBs due to the porous nature of the electrodes. Several articles reveal the performance of pseudocapacitive material, such as RuO_2 as stacked electrodes with solid-state electrolytes such as LiPON [66]. More recently, 2D materials with high electrical conductivity enable ultrathin films to be used as stacked MSCs [50]. They can also be used as separators on their own after modulating their conductivity. Stacked MSCs are often utilized for flexible electronics with a smaller restriction on size. Stacked devices, however, are limited to ultrathin films as the thickness increases the resistance

of ion-transportation paths. Thus, there needs to be a trade-off between footprint area and thickness.

Planar MSCs, on the other hand, can exhibit short ion transportation channels between the positive and negative terminals due to the geometric patterns of micrometer resolutions. Compared to stacked MSCs, planar devices demonstrate a drastically improved power and rate capability. The fabrication of planar devices on solid-state substrate reduces the issue of high resistance in thicker electrodes as the electrolyte is in contact with a larger surface area of electrodes. Planar MSCs are often fabricated using carbon, 2D material, pseudocapacitive, and polymer-based electrodes while using a gel, aqueous, or solid-state electrolyte. They are fabricated through a range of fabrication processes such as electrodeposition [67], photolithography [68], chemical vapor deposition [69], layer-by-layer [70], Inkjet printing [71], and laser scribing [72]. Among various viable techniques for fabrication, photolithography and chemical vapor deposition are some of the standard CMOS processes. Some examples of MSCs are shown in Figure 1.8.

Both planar and stacked MSC configurations have advantages and disadvantages, making them suitable for specific applications. Although MSCs have large power density, short charge-discharge cycles, and high cyclic stability, these devices also require attention on low energy density, high serial resistance, poor high-frequency behavior, and non-standardized front-end-of-line (FEOL) and back-end-of-line (BEOL) CMOS compatibility.

1.5 Challenges

There are several challenges in implementing an on-chip self-sustaining power supply for IoT sensor nodes. The main challenge is the loss of power or energy due to a temporary lack of the expected or required physical conditions such as available sunlight or vibrations at the appropriate frequencies. A directly related challenge is the efficient storage of harvested energy in the energy storage system. Batteries typically have low leakage. However, the main concern with them is their cyclic stability. Therefore, they require to be swapped after short term usage. The high cost of manufacturing and disposal of batteries has become another critical issue. Therefore, they must be replaced entirely or complemented by electrochemical capacitors to improve upon their short lifetimes.

One main challenge currently presented for vibrational energy harvesters in their deployment is the lack of sufficient bandwidth in MEMS designs. Impedance mismatch is also an issue with vibrational harvesters as it can significantly impact the magnitude of the output harvested power. Although the fabrication methodology of these harvesters is well defined, there are several severe problems in their wafer-level fabrication that increase the total cost of manufacturing a single device, such as electrode retention, wafer-scale piezoelectric poling, and dicing, to name a few. A more comprehensive review addressing fabrication challenges of MPEHs is given by Rezaei et al. [73].

On the other hand, electrochemical capacitors suffer primarily from low energy density, high leakage current, and lack of proper CMOS compatible fabrication methodology. Most of the fabrication processes examined in literature for manufacturing MSCs

utilize different methodologies for various electrodes. In order to design the properties of energy storage devices, there must be a cohesive fabrication process that can incorporate any material essential for improving the device performance. Such a process should have high resolution and establish a high wafer yield comparable to the state-of-the-art sensor or CMOS technology.

1.5.1 Manufacturing for microelectronic compatibility

To understand the challenge of fabrication of on-chip vibrational energy harvester and CMOS compatible MSCs, we will review the standard processes used in microelectronic integrated circuits (IC) compatible fabrication processes. The standard process technology for ICs and very large scale integrated (VLSI) circuits is shown in Figure 1.9. The fabrication of these components starts on a wafer, a polished semiconductor substrate. The next step usually involves deposition or growth of thin films such as SiO_2, Si_3N_4, polySi or dielectric films, and even metalized oxides. After the growth of thin films, the substrate undergoes doping through diffusion or ion implantation. This process is used in IC technology to fabricate pn junction diodes which can later be used in MOSFET (metal-oxide-semiconductor field-effect transistor) fabrication. Then, the substrate is subjected to photolithography, where a polymeric photoresist is spin-coated on it and then exposed in UV light through a special mask with a specific design. The photoresist is sensitive to UV light depending on its chemical structure. It is generally of two types - positive and negative. In the case of the positive photoresist, the UV light breaks the linkages of the polymer exposed, while in the negative, the exposure strengthens the bonds of the polymer. During the development of the photoresist step, the weaker linkage polymers are etched out of the substrate while leaving the photoresist in the desired pattern. Depending on the process's requirement, the exposed surface is then used for further doping, film formation, or etching. The process is then repeated in several cycles depending on the total number of photolithographic masks [74].

However, there are several constraints in the IC fabrication process regarding the choice of material and equipment. The first significant constraint is the material for the wafer. An IC wafer should be mechanically robust with the required hardness to survive both automated and manual handling in all process steps. The second constraint comes in the form of radiation required for photolithography: optical and UV light, X-ray, and electron beam. The third constraint is in the form of metals used in IC fabrication. This list is restricted to Al, Au, Ag, Cr, Mo, W, Pt, Pd, Ta, and Ti [74]. Furthermore, the process is also dependent on the melting point of these metals. Among the used metals, Al has the lowest melting point at 660 °C. So, the fabrication of energy harvesters, supercapacitors, and subsequent integration should be conducted with the techniques within these constraints.

Fabrication of on-chip MPEHs requires photolithography, etching, metallization, doping, and deposition techniques. These processes are standard in micromachining techniques too. Furthermore, with improving MEMS technology, these processes have become highly developed in improved reliability, mass production, and cost reduction while achieving a high wafer yield. Therefore, energy harvesters that are fabricated

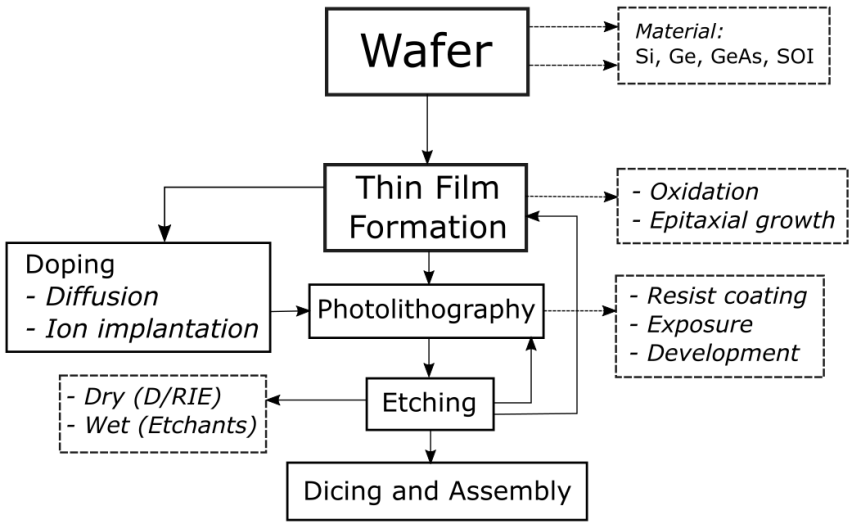


Figure 1.9: Main fabrication steps for a IC fabrication process. The dotted square boxes show the constrained variety of processes possible in a CMOS compatible fabrication facility.

through MEMS techniques can be easily integrated into a CMOS compatible fabrication process.

However, for the energy storage element, supercapacitors generally require a large physical size and specialized manufacturing techniques that make them hard to be integrable in microsystem electronics technology that requires semiconductor micromachining. Therefore, developing CMOS compatible fabrication processes has attracted much attention over the past few years [75, 76, 77, 64, 71].

Compared to other techniques to manufacture MSCs such as screen printing [78], inkjet printing [71], laser scribing [64], electrostatic spray deposition [77], electrophoretic deposition [79], chemical exfoliation [80] and doctor blade coating [81], the use of spin coating has the advantage of already being an established conventional part of standard CMOS processing, implying that it is as such inherently CMOS/MEMS compatible. Techniques that are not compatible with semiconductor device processing prohibit cost-effective integration and fabrication of on-chip harvesters and MSCs. Processes like inkjet printing and screen printing do not have an effective scaling down technique, while its raster-scanning process inhibits laser scribing. Thus, in view of the expected further automation in IC manufacturing [82], its compatibility advantage makes spin coating a strong candidate for being a preferred MSC manufacturing technique, provided it can validate that it can fabricate devices of sufficient quality and yield.

1.6 Scope of the thesis

In this thesis, we will discuss vibrational energy harvesters and electrochemical capacitors that can be fabricated through MEMS and CMOS compatible technology to develop an on-chip power supply for sensor nodes with an aim of extended lifetime. Chapter 1 introduced the concept behind a self-reliant on-chip power supply through

an evaluation of requirements necessitated by IoT applications. A concise summary of energy harvesting, micro-energy storage, and IC-compatible manufacturing process is presented.

Chapter 2 discusses the current status of piezoelectric energy harvesting technology. A formal theory is presented to motivate the choice of device design intended for on-chip energy harvesting. The energy harvesters are categorized for various bandwidth improvement strategies and their performance metrics are examined with a state-of-the-art comparison of micro-electro-mechanical-systems (MEMS) piezoelectric micro-energy harvesters based on them. The two-degree-of-freedom (2DOF) structures are investigated further in Paper 1 through design and fabrication of cut-out cantilevers. The challenges of fabrication are summarized and the second and third generation of vibrational energy harvesters are presented and explained. A section on discussion of future of vibrational energy harvesters is presented.

In chapter 3, we focus on the energy storage component of a wireless sensor node, with MSC in focus. The chapter summarizes different figures of merit determining the charge storage and delivery capacity of the MSCs. The fabrication methodologies for manufacturing MSCs for on-chip electronics is considered in more detail with a comprehensive literature survey of electrode deposition processes such as chemical vapor deposition, photolithography, inkjet printing, electrodeposition, and electrode conversion. The impact of electrode geometry and thickness is investigated in Paper 3 through fabrication of CVD based carbon nanofiber (CNF) electrodes. Based on the results of electrode geometries, the spin coating process is explored as the viable option for CMOS technology integration of MSCs using graphene oxide (GO) based aqueous solution. The fabrication process and its shortcomings are examined in more detail. We introduce an enhanced spin coating process in Paper 2 and review the impact of surface roughening on the spin coating of electrodes. The CNF and rGO based devices are compared in Paper 4. Finally, we will discuss the results to improve the energy density of the MSCs using a variety of rGO based electrodes deposited through enhanced spin coating process described in detail in Paper 5.

Chapter 4 examines the challenges of on-chip integration of vibrational micro-energy harvesters and MSCs for a self-reliant on-chip power supply. The packaging of both devices – harvesting and storage are examined. The experimental aspects of package fabrication, choice of electrolyte, and device assembly are considered. The strategies for on-chip integration are analyzed with a description of proposed experimental integration of on-chip power supply. In chapter 5, we will highlight the summary of the thesis and take up the aspects that can be explored in future work. Finally, a summary of appended papers is presented.

Chapter 2

Piezoelectric vibrational energy harvesters

2.1 Introduction

Piezoelectric energy harvesting is a type of energy scavenging that uses the vibrations present in the environment as their source. Vibrations are ubiquitous in our body and surroundings ranging from heartbeats, traffic on roads and railway tracks, and industrial equipment in use. The mechanical energy is converted to electrical energy by a piezoelectric material layered on a cantilever. When the cantilever vibrates at a certain frequency, the vibrations produce a mechanical stress in its structure. The stress in the beams is transferred to the piezoelectric material present on the cantilever structure. This leads to accumulation of charge in the domains of the piezoelectric material. When the device is connected to a load, the circuit is complete and the output electrical energy is delivered in the form of an alternating current.

In comparison to various energy harvesters discussed in the introduction, MPEHs demonstrate considerable potential in charging energy storage devices for wireless sensor nodes owing to relatively high energy densities and possibilities for integration in MEMS and IC technologies. The presence of vibrations in harsh environments such as industries, mines, and deep-sea exploration are specially suitable for the application of vibrational energy harvesters. A model of an energy harvesting devices for the collection of vibrational energy from the surroundings was developed in 2000 [83]. This model was designed for the transfer of power to sensors in sensing networks. An analytical solution and experimental design of a bimorph, i.e., a cantilever containing piezoelectric material on both sides, was developed by Inman et al. [84], both with series and parallel connections of the piezoelectric layers. Since then, the PEH has been studied for ambient vibrations such as traffic [85], bridges [86], motors [87], air turbulence [88, 89], and human motion [90, 91, 92]. PEHs are also present as fabric composites that can be woven in e-textiles [93]. They can also be used to produce electrical energy from water flows [94], rain drops [95, 96, 97], and rotation- and flow- induced vibrations [98, 99, 100] that are present as outcomes of impact [101], friction [102] and random excitations [103]. There is additional benefit in miniaturizing the designs so they can be fitted in extremely narrow or small spaces. Such MPEHs can be integrated alongside

energy storage units such as electrochemical capacitors through compact, high power miniaturized mechanical designs that can be integrated with sensors, transceiver, and IC processing units, on a 1 cm^2 die footprint.

There are, however, two important challenges that restrict a scalable integration of MPEHs. Firstly, they must be able to produce enough energy to charge an electrochemical capacitor through either steady state- or intermittent charging. Steady state charging can be achieved by placing the MPEH in an environment that has vibrations in a certain frequency range with semi-infinite duration. Intermittent charging is more applicable where the MPEH transforms energy during a specific action in the environment, such as train passing over the sensor node fitted on a railway track, or the opening of heavy doors in shopping areas. In real life situations, the vibrations in both cases occur over a range of frequencies that should be compatible with the bandwidth of operation for the harvester. Typical vibrations in systems present in the environment such as traffic can range from 1 - 100 Hz. Similarly, ground borne vibrations, machinery, and acoustic vibrations can range from 1 to 500 Hz [104]. Thus, it is necessary for the MPEH to produce sufficient electricity over a large bandwidth of operation. If these devices can provide μW to mW power, they can be integrated to power sensor nodes in areas with access to high waste mechanical energy.

There are several mechanisms in the literature that improve the bandwidth of the MPEH. They can be broadly categorized in four categories - monostable or one-degree-of-freedom (1DOF) structures, multi-stable structures, frequency up-conversion mechanisms, and multiple-degrees-of-freedom (nDOF). These mechanisms are used extensively in macro-energy harvesters. We categorize macro-energy harvesters as structures that have been manufactured through conventional machining techniques such as high-precision lasers, lathe machines, computerized numerical controls (CNCs) and toolboxes. We shall review the MEMS compatibility of these mechanisms in this chapter followed by a comprehensive review of PZT based MPEHs using piezoelectric micro-cantilevers.

The mechanisms for vibrational energy harvesting utilize a variety of piezoelectric materials. Piezoelectric materials can be categorized into three different categories - inorganic piezoelectric materials, piezocomposites, and voided charged polymers. Inorganic piezoelectric materials include PZT, ZnO, and AlN based materials. They generally possess a high figure-of-merit (FOM), a quantity used to characterize the piezoelectric response of a material. The FOM of piezoelectric materials can be defined as the ratio between the total electrical energy harvested over the total mechanical energy applied. It is denoted as $k^2 = \frac{d^2}{s \times \epsilon}$ where $d_{31,33}$ is the strain induced in the material normal (31) or parallel (33) to the applied force vector, $s_{31,33}$ is the material compliance, and ϵ is the relative permittivity. The inorganic piezoelectrics also have a high Curie temperature, the point at which the material loses its piezoelectric property. Piezocomposites are another category of piezoelectric materials that use materials such as multifunctional cellulose, ZnO with cellulose, Pt nanowires with polydimethysiloxane (PDMS) composites. They are similar in terms of FOM with the inorganic piezoelectrics however they possess a lower Curie temperature. Voided charged polymers are newly developed highly porous piezoelectric materials that use parlyene, PDMS, polyvinlydiflouride (PVDF) polymers. They generally possess quite low FOMs compared to the other piezo-

electric material however their availability and ease of manufacturing bulk films makes them a competitive solution for use in energy harvesting.

The second challenge in integrating MPEH in wireless sensor nodes is the scalability of the fabrication process. Piezoelectric micro-cantilevers are already used in scanning tunneling microscopy to characterize the surface properties of devices and materials through electrical excitation at a particular resonating frequency [105]. However, these structures are designed for narrow bandwidths with a large quality factor. In order to fabricate devices with large bandwidths, there are several fabrication challenges that can impede the manufacturing process. We shall discuss these challenges in this chapter through experimental evaluation of the MEMS fabrication process performed in a state-of-the-art cleanroom facility.

2.1.1 Challenges in power density

In order to understand the working mechanism of MPEHs, the device can be visualized as a mass-spring-damper (MKS) system, as seen in Figure 2.1. The mass of the device is m, y is the amplitude of displacement, k is the stiffness of the beam, $y(t)$ is the displacement of the beam, $z(t)$ is the relative position of the center of mass of the beam with respect to its displacement and b_m and b_e are the damping coefficients and $b = b_m + b_e$, where m and e are the mechanical and electrical indices respectively.

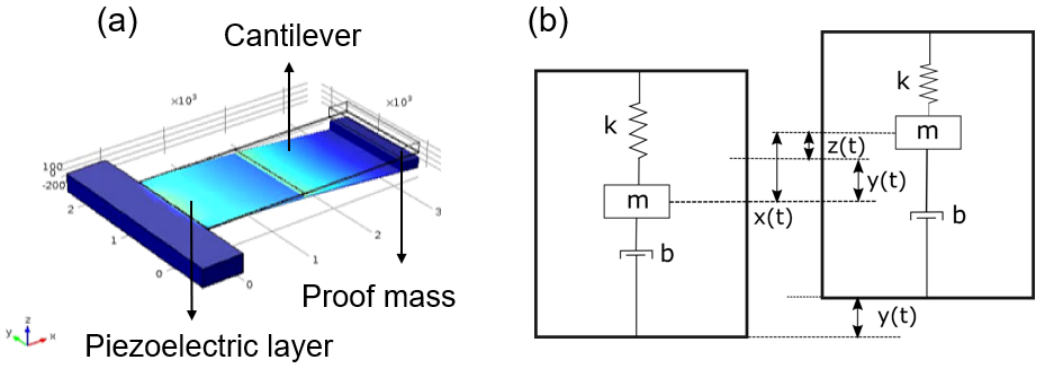


Figure 2.1: (a) Schematic of a typical single cantilever vibrational energy harvester. The gradient - light to dark blue represents descending order of stress on the beams, (b) Typical schematic of the MKS 1DOF system.

Let the displacement of the system $y(t) = Y sin(\omega t)$. With that we get the transfer function as a second order differential equation

$$mz"(t) + bz'(t) + kz(t) = -my"(t) \tag{2.1}$$

Now in a standard form,

$$z"(t) + \frac{b}{m}z'(t) + \frac{k}{m}z(t) = -y"(t) \tag{2.2}$$

From the solutions of the second order differential equation, we know that

$$\frac{b}{m} = 2\zeta\omega_n \qquad\qquad \frac{k}{m} = \omega_n^2$$

where ω_n is the natural frequency of the undamped system, and ζ is the damping ratio. So, from this, we get

$$\omega_n = \sqrt{\frac{k}{m}} \qquad \zeta = \frac{b}{2\sqrt{km}}$$

We can also derive a notation called the quality factor (Q) as

$$Q = \frac{\sqrt{km}}{b}$$

which can also written in terms of ω_n as

$$Q \approx \frac{\omega_n}{\Delta\omega} \tag{2.3}$$

where $\Delta\omega$ is the bandwidth of frequencies that have a power output of at least half the magnitude at the resonant frequency ω_n. It is also denoted as the 3 dB bandwidth of any harvesting system. Considering our input signal $y(t)$, the solution for average power related to mechanical losses and electrical output is

$$P(\omega) = \frac{m(\zeta_m + \zeta_e) Y^2 (\frac{\omega}{\omega_r})^3 \omega^3}{[1 - (\frac{\omega}{\omega_r})^2]^2 + (2(\zeta_m + \zeta_e)\frac{\omega}{\omega_r})^2} \tag{2.4}$$

When the frequency of the system ω is equal to the resonant freqency ω_r, the power reaches its maximum which is

$$P = \frac{mY^2\omega_r^3}{4(\zeta_m + \zeta_e)} \tag{2.5}$$

On further analysis of equation 2.8, we figure out one main issue that needs to be optimized with the utilization of MPEHs in on-chip power units, i.e. narrow bandwidth.

Considering $\frac{\omega}{\omega_r} = x$ and keeping m, Y and ζ_m, ω_r, and ζ_e as arbitrary constants $C_{1,2}$, we get the equation 2.8 as

$$P = \frac{C_1 x^6}{(1 - x^2)^2 + C_2 x^2} \tag{2.6}$$

When we plot this equation in Figure 2.2(a), we see the reduction of output power at either side of ω_r. Therefore, we need to find solutions for improving its bandwidth of frequencies by reviewing some of the pre-existing solutions in macro-energy harvesters. Such a desirable output is shown in Figure 2.2(b). These solutions must also be feasible for realization in a MEMS structure which can then further be integrated with an on-chip power supply.

Thus the development of MPEHs requires improvements in the design compared to a single cantilever to achieve a maximum power density. Even a slight variation in the vibrational frequency of the environment would result in the dramatic reduction of power output from MPEHs resulting in severe transduction inefficiency. Thus, there is a need to survey the existing literature for macro-energy harvesting mechanisms for improving bandwidth and design of an MPEH that can be fabricated in a scalable way through MEMS fabrication technology. In the next section, we shall discuss various mechanisms reported in the literature to improve the bandwidth of operation.

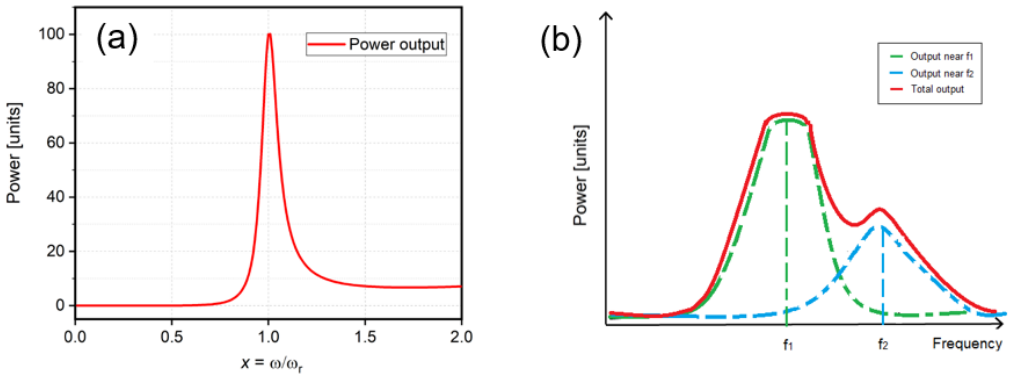


Figure 2.2: (a) Simulated power output of a generic single cantilever based energy harvester with respect to $x = \frac{\omega}{\omega_r}$, (d) Desirable wide bandwidth output power required from the energy harvester.

2.1.2 Bandwidth improvement designs

PEHs can generally be divided into four categories. The following section examines these categories and discusses the aspects of bandwidth improvements in these designs.

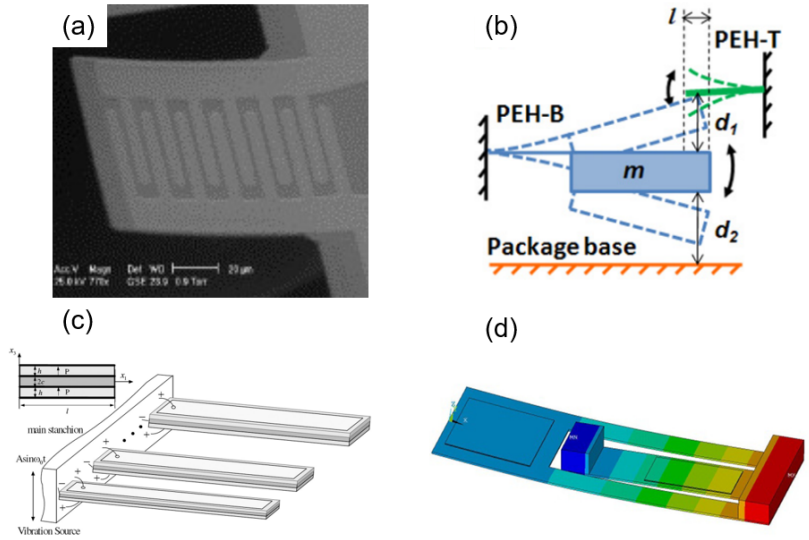


Figure 2.3: Techniques in macro-energy harvesting that are used for improving the device's bandwidth of frequencies: (a) A stress induced structure by Blystad et al. [106], (b) amplitude limiter, (c) array configuration by Xue [107], (d) 2DOF freedom structure by Wu et al. [108]. Images are reproduced after permission from the publishers.

Mono-stable or 1DOF structures

The first energy harvesting mechanism in MPEHs pertains to monostable or 1DOF oscillations. They require an external stimulus at their resonant frequency. After the

input stimulus is switched off, they return to their equilibrium position. The power output of these designs depends on the amplitude of vibration, their natural frequency, and young's modulus E of the structure. Generally, cantilever beams with a proof-mass are used to produce high power output at their first natural frequencies. Figure 2.1(a) shows a typical cantilever design. Due to movement of the beams in only one direction, these designs are often referred to as 1DOF structures.

Surface micro-machining fabrication techniques have been used in manufacturing several 1DOF energy harvesters at a large scale [109]. They presented a single rectangular cantilever with a hanging proof-mass. The proof-mass is usually quite thick compared to the cantilever beam. The large proof-mass acts as a hanging mass to the spring system, thereby reducing its natural frequency. The proof-mass can be made during the micromachining process, or it can be added onto the fabricated structure. Jeon and Choi [110], [111] fabricated a d_{33}, PZT-based vibrational harvester. The cantilever beam was composed of a thin SiO_2/SiN_x layer with a diffusion barrier of ZrO_2 separating PZT from the structure. The proof-mass was made up of SU-8 thick resist. Fang et al. [112] similarly created microcantilevers through micromachining techniques and added a Ni proof-mass post-processing. Due to Ni's higher density over Si (8.9 g/cm^3 vs. 2.3 g/cm^3), it reduces the resonance frequency of the device. We have examined several micro-energy harvesters in a more concise format in Paper 1. Also, the list of device performances can be found in Table 2.1.

While 1DOF designs have the narrow bandwidth issue that was discussed extensively previously, their stress distribution on the beams leaves excessive dead space on the cantilever structure for developing sufficient stress in the PZT layer. To improve the distribution of stress on the cantilever beams, several structures such as trapezoidal beams [113, 114] have been reported. The trapezoidal designed cantilevers experimentally revealed 30 % improvement in stress distribution across the beam. Similar studies in the literature have been achieved with quadrilateral beams [115], inverse trapezoidal beams, u-shaped cantilever ends [116], planar, holed, rounded and coupled ends [117].

However, for monostable structures, the problem of high Q-factor still exists due to the simplicity of the mechanism[118]. However, these designs can be arranged in an array-like configuration to generate power at various resonant frequencies. Another idea of improving bandwidth is to create a generator array consisting of cantilever beams of different lengths and proof-masses operating at different frequencies. Studies conducted by Shahruz et al. [119], Ferrari [120], Xue [107], and Liu [121], Qi et al. [122] expounded upon this concept with more cantilevers in a single array. Figure 2.3(c) shows a schematic representation of array-based MPEHs. Similarly, Feng et al. [123] developed a four cantilever based MPEH fabricated and electrically connected in parallel. They achieved a wide frequency range of 300 - 800 Hz. Liu et al. [124] could achieve a bandwidth of 18 Hz between 30 - 48 Hz with an power output of 30 - 100 nW. Although favorable results are obtained, the requirement of integrating particular electrical circuitry for each cantilever and the device's limited volume efficiency, make multi-frequency generator arrays more complicated to design and fabricate as a MEMS design.

With the above energy harvesters, most of the designs comprise of a beam that has an active piezoelectric area along the fixed end while the free end is left unused as it ex-

periences minimal stress, which can be considered as a "dead area". When the material is stressed, its molecular orientation exhibits an increased dipole moment. This dipole moment gives rise to an electric field that leads to the redistribution of charge in the a circuit containing the piezoelectric material. If there is no stress on the piezoelectric material, the total dipole moment of the piezoelectric material reduces, thus giving less charge redistribution. This is an issue when we discuss the performance of 1DOF harvesters. The MEMS devices should utilize highest fill factor for the piezoelectric material area on the cantilevers for efficient performance. Therefore, we require novel solutions from the macroscopic MPEHs to test them on a MEMS scale.

Frequency up-conversion structures

Frequency up-conversion (FUC) mechanisms constitute another technique used in vibrational energy harvesters. The FUC mechanism improves the power density of the devices by adding non-linearity in the MPEH vibration through either geometric restriction or stoppers.

Studies by Blystad [106] and Liu [124] suggest amplitude limiters as a way to increase the bandwidth. A metal plate is used as a mechanical stopper to limit the displacement of the cantilevers. This design is illustrated in Figure 2.3(b). Soliman et al. [125] experimented on such a structure with a single stopper and showed an improvement in the power output bandwidth of the device. Even with the improved bandwidth, in practicality, lower maximum output power and fatigue-induced failures in such designs make their incorporation harder in microstructural harvesters. The drawbacks such as complex method of assembly in MEMS scale design of the FUC mechanism restricts its application in miniaturized on-chip sensor nodes.

Multi-stable structures

One of the potential solutions to the bandwidth and power problem is a nonlinear generator with multi-stable structures. A multi-stable structure provides the cantilever design with multiple stable equilibrium positions that allows it to have multiple frequencies where the stress distribution on the beams is optimal. These positions are isolated by potential barriers with amplitudes depending on the direction of vibration. Generally, in multi-stable structures, a magnetic force is applied on the cantilever through an external magnet.

Besides applying a magnet, non-linearity can also be introduced in the device structure by using a Duffing-type oscillator that can change its stiffness based on the amplitude of vibration. Integration of multi-stable MPEHs has not been observed till date. There are a few bi-stable MPEHs.

Stanton et al. [126] incorporated a magnetic nonlinearity with the help of two magnets strategically placed in a linear system. Wu et al. [127] and Erturk et al. [84] also arrived at the same conclusion of obtaining a broad bandwidth. The stability of response can be monitored easily through adjusting the number of magnets or changing their geometric size, or position. Hajati et al. [128] developed a four fixed-fixed beams structure, with a Si proof-mass with a bandwidth of 450 Hz. Marinkovic et al. [129]

devised a similar harvester with a bandwidth of 160–400 Hz. Rezaeisaray et al. [130] showed Duffing-type harvester vibrating at 100 Hz with nW of produced power.

Having a multi-stable structure with magnetic attachments is a promising idea; however, it is usually large and requires an auxiliary support structure that cannot currently be placed in a MEMS design. Although, the frequency broadening mechanism of multi-stable devices has enormous potential, the stability of silicon cantilevers at non-equilibrium positions is low and can lead to device breakage and failure. Thus, the multi-stable mechanism is generally not suitable for MEMS fabrication and application in powering on-chip sensor nodes.

Table 2.1: List of macro- and micro-MPEHs ordered according to year of publication from oldest to newest.

Ref.	**Vol. (mm^3)**	**Res. Freq. (Hz)**	**V**$_{pp}$ (V)	**Power** (W)	**Geometry**
[112]	0.6	608	0.89	2.16 μ	Cantilever
[111]	0.05304	13900	2.4	1 μ	Cantilever
[131]	0.48	1580	-	10 n	Cantilever
[132]	0.75	1800	-	40 μ	Cantilever
[123]	45	300 - 800	-	40 μ	Dual-cantilever
[121]	0.045	610	3.9	3.98 μ	Array
[133]	0.069	461	-	2.15 m	Cantilever
[120]	13.5	113	-	89 μ	Array
[84]	620	46.4	-	-	Dynamic magnifier
[134]	0.48	875	-	1.4 μ	Thinned cantilever
[11]	0.17	572	-	60 μ	Cantilever
[135]	0.05	255	2.6	2.7 μ	Cantilever
[136]	480	39.8	-	13.54 m	Right angle
[137]	3640	26	-	-	2DOF no cutout
[122]	6800	14-30	18	-	Array
[138]	800	11	60 V/g		2DOF two cantilevers
[139]	1650	21	4.7	5.68 μ	2DOF no cutout
[124]	0.075	30-48	100 m	100 n	Dynamic magnifier
[140]	3	115	16 m	1 n	Quasi bendable cantilever
[127]	2640	18	22 V	1.25 m	2DOF "cut-out" rectangular
[141]	0.36	234.5	1.62 - 5	66.75 μ	Rectangular
[142]		45 - 3667	-	690 n	Folded Spring
[143]	48	330-410	11.7 V		S-shaped coupled cantilever
[144]	0.05	300 - 700	3 - 10 m	1.4 μ	Spiral cantilever array
[116]		20-30	-	29.8 μ	U-shaped single cantilever
Paper 1	0.05	1258 - 1783	-	-	M-shaped
[145]	100	68-200	45 m	23 n	Spiral
[146]	150000	10	110 m	127 μ	Flexible single cantilever

Multiple degrees of freedom

The fourth mechanism used to obtain more efficient conversion of mechanical energy to electrical energy is to apply multiple degree of freedom (nDOF) structures for closening

the gap between the first two natural frequencies. If the eigenfrequencies are close enough, the confluence of two resonance peaks can establish a power output shape similar to the one discussed in Figure 2.2(b).

In recent literature, Scornec et al. [146] developed a flexible tunable length meandering MPEH with a frequency range of 7 Hz. Liu et al. [147] developed a novel S-shaped cantilever, while Wen[148] and Song et al.[145] developed spiral cantilevers using PVDF and PZT respectively, operating at wide bandwidths of 20 Hz and 68 Hz respectively.

In recent years, the focus of the vibrational micro-energy harvester research has shifted to the fabrication of specialized designs to improve the bandwidth of the energy-providing frequencies. Park et al. [140] designed an intrinsically stress-induced bent Si cantilever of 3 mm × 2 mm × 18 μm. The harvester had two directions of oscillation, vertical and radial. When the cantilever is released, it undergoes bending deformation through the presence of a low temperature oxide (SiO_2) and a low stress nitride (SiN_x) on top of the Si substrate. They designed the study on the principle of proportional dependence of the output power on the bending moment. They also shaped the cantilevers in a trapezoidal form to improve the distribution of stress on the beam. The device gave 1 μW power output at a resonance frequency of 115 Hz with a Q-factor of 51. Leuke et al. [142] fabricated a set of folded spring structures for reduction of the operating frequency of the microstructures. The folded beam shape reduces the overall stiffness of the design and thus brings the natural frequency of the system to 30 - 300 Hz. Also, the next natural frequencies of the structure are brought closer to one another. They achieved a maximum power output of 690.5 nW at 226 Hz in one of the designs which had four folded Si springs attached to a central hanging proof-mass. Yu et al. [141] designed a five cantilever system with a single large proof-mass. The fabricated generator had plates of size 3 mm × 2.4 mm × 50 μm and a Si proof-mass of 8 mm × 12.4 mm × 0.5 mm. The power output at its resonant frequency of 234 Hz was 66.75 μW. A similar concept was also employed by Zhang et al. [149] where instead of rectangular folded springs, they used circular annular rings, each attached to the central proof-mass. The device die is 6 mm × 6 mm in size and demonstrated resonance frequencies lower than 11 Hz with a voltage output 7.5 mV at less than 0.2g acceleration.

To devise natural frequencies closer, Jang et al. [150] developed a 2DOF piezoelectric energy harvesting device which exploited the structure's translation and rotation vibration modes. The device showed a two-peak power output and displayed bandwidth improvement at high power levels compared to the conventional one-degree-of-freedom (1DOF) device. Kim et al. [138] (2011) displayed the performance comparison between a 2DOF and conventional SDOF device. Wu et al.[108] proposed a "cut-out" 2DOF harvester with a secondary beam enclosed within the main beam, which achieves two close resonances with significantly large amplitudes. Although, even with close resonance peaks, the bandwidth of the system included an anti-resonance frequency which led to a significant drop of the output voltage.

Currently, known solutions use 2DOF structures to improve the bandwidth in micro-cantilever designs. Roundy et al. [113] initially proposed the idea of incorporating multiple proof-masses to create a multiple-DOF with at least one structure resonating in the desired frequency range. Ou et al. [137] then derived a theoretical model of a dual-mass beam structure for bandwidth broadening. Aldraihem and Baz [151] and

Arafa et al. [139] studied a 2DOF device acting as a dynamic magnifier. Although close resonances could be achieved, the magnifier required a huge weight, which proved counterproductive to miniature harvesters. Later, Erturk et al. [152] and Xu et al. [136] considered innovative L-shaped designs for cantilevers to bridge the gap of natural frequencies.

While several studies show significant improvement of bandwidth through 2DOF structures, not much research on it focuses on the distribution of stress on the cantilever beams as discussed in the monostable structures. Studies by Staaf et al. [153, 143] provide an assessment of using parallel cantilevers coupled to one another at one end. This improves the stress distribution patterns and the bandwidth through coupled resonances. The details of the MPEHs can be found in Table 2.1.

2.2 Two-degrees of freedom (2DOF) design

A piezoelectric energy harvester is normally designed as a MKS system for analytical modeling. In this model, m_1 and m_2 are the masses of the primary and secondary structures respectively, k_1, k_2, and b_m, b_e are their respective spring constants and damping. When the system is in an excited base configuration, the initial displacements of the base, primary, and secondary proof-masses are y_0, y_1 and y_2. $-V\theta$ is the force induced by mechanical coupling, where V is the potential formed in the piezoelectric film, θ is electromechanical coupling coefficient, and C is the capacitance.

The equations of motions and the current equations are derived from the free-body-diagram shown in Paper 1. Solving the equations, we get the equation for the difference between two dimensionless natural frequencies as [154]

$$\Omega_{1,2} = \sqrt{\frac{(1+\mu)\lambda^2 + (1+k_e^2)}{2} \pm \frac{\sqrt{((1+\mu)\lambda^2 + (1+k_e^2))^2 - 4\lambda^2(1+k_e^2)}}{2}} \tag{2.7}$$

where we have $\mu = \frac{m_2}{m_1}$, $k_e^2 = \frac{\theta^2}{Ck_1}$, and $\lambda = \frac{\omega_2}{\omega_1}$. ω_1 and ω_2 are the two natural frequencies of the primary and secondary structures respectively. They are calculated as $\omega_{1,2} = \sqrt{\frac{k_{1,2}}{m_{1,2}}}$.

It can be seen from equation 2.7, that the closening of the first two natural frequencies depends on the parameters μ and λ. Figure 2.4 shows the contour plot of $\Delta\Omega$ vs μ and λ. The next section describes the simulation results in COMSOL for three designs that provided different values of λ and μ and extends the hypothesis generated by equation 2.7.

2.2.1 Operational bandwidth

The 2DOF micro-energy harvester is numerically simulated in COMSOL to acquire the optimal dimensions for the realization of enhanced stress distribution and narrowing of natural frequencies. Three different topologies of designs were investigated, named, M-shape, M-long, and M-big. Figure 2.5 shows the schematic of the generalized harvester in COMSOL. The big-block is taken as the fixed support in the simulation. For modeling

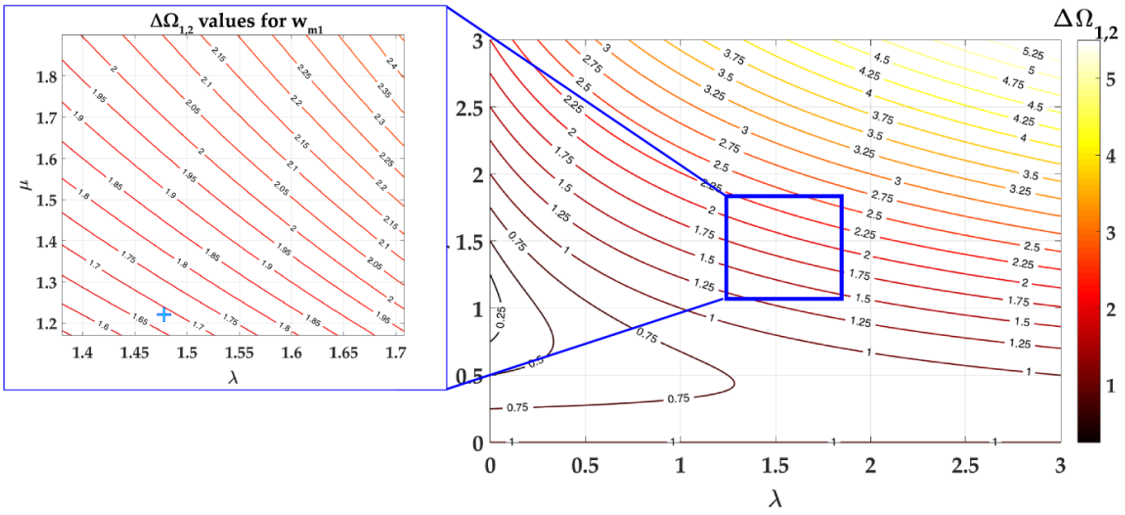


Figure 2.4: Contour plot of difference in the first two dimensionless eigenfrequencies ($\Delta\Omega$) with respect to ratio of beam masses (μ) and their respective first eigenfrequencies (λ)

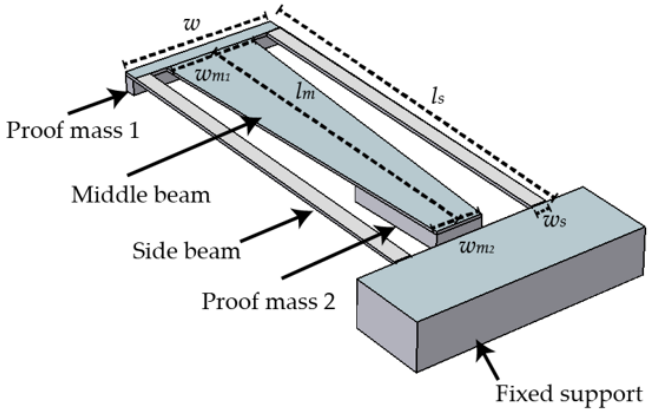


Figure 2.5: Schematic image of the M-design harvester setup in COMSOL. Table 2.3 outlines the dimensions of each design.

a MEMS PEH, the design structure consists of Si and the piezoelectric material is chosen to be PZT-5A, the one with the closest elasticity matrix with the PZT that we could accrue from Silex Microsystems on our wafers. The five main dimensional parameters that play an important role in determining natural frequencies are the length and width of the side beams, l_s and w respectively; the length of the middle beam, l_m, and the widths of the middle beam at the attached and free ends, w_{m1} and w_{m2} respectively. The thickness of the device is decided by the SOI wafer used, i.e. 20 μm. The thickness of the proof-mass is 100 μm for each design so that they could be fabricated within a single fabrication process plan. A detailed presentation of the cantilever design in relation to μ and λ parameters is discussed in Paper 1, section 2.2.

Dimensions l_s and w govern the natural frequencies of the system. They were chosen

such that the first resonance occurs at 1.2 - 1.5 kHz. If M-shape is taken as a reference, then M-long has a longer and narrower middle beam, while M-big is approximately double the size of M-shape to test the scaling of characteristics. Table 2.3 provides the detailed differentiation of dimensions on each design. The designs employed for the M-shape, M-long, and M-big were chosen to bring the first two natural frequencies as close to each other as possible. Therefore, each of these designs is an ideal representation of its particular features. Further description of the dimensional analysis relating to μ and λ is given in Paper 1.

Table 2.2: Dimensions of M-shape, M-long, and M-big used in COMSOL simulations, in μm.

Dimensions	M-shape	M-long	M-big
l_s	2500	2900	5000
w	1000	1000	2000
l_m	2288	2700	4576
w_{m1}	560	500	1000
w_{m2}	300	100	400
w_s	100	100	200

2.2.2 Fabrication

Process plan

After modeling and simulations for various cantilever designs, the fabrication of all three energy harvesters is performed through the following process scheme on a 6" Si-on-Insulator (SOI) wafer. The enumeration below follows the process plan illustrated in Figure 2.6 that shows the fabrication scheme.

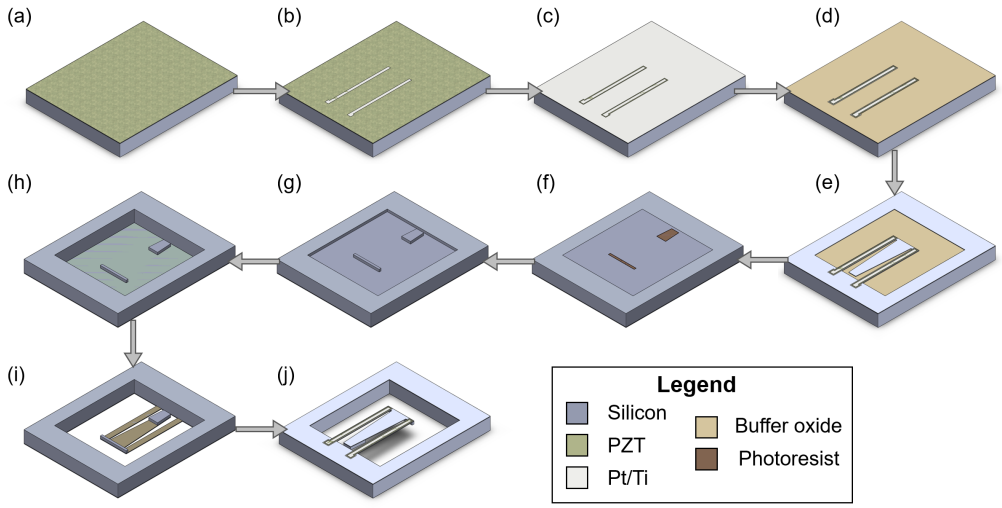


Figure 2.6: Process scheme for the micro-energy harvester fabrication.

(a) A 6" SOI wafer is cleaned (Figure 2.6(a)). The deposition processes of the bottom electrodes, PZT, and top electrodes were performed by Silex Microsystems AB, Sweden. A 20 nm layer of Ti is sputtered onto the substrate. Ti acts as an adhesion layer for Pt and also provides epitaxial uniformity to the metal current collector. The Pt layer of 100 nm is sputtered, keeping the texture template uniform for the subsequent PZT deposition. A buffer layer of LaNiO (20 nm) is added on top of the surface. Then, a PZT layer of 1.1 μm is deposited by a sol-gel process on the buffer layer. The PZT layer has previously displayed an electromechanical coupling coefficient, e_{31} = -18 C/m^2.

(b) For the lift-off process of top electrodes, a photoresist pattern of S1813 and LOR-3A is spin-coated on the SOI substrate. The LOR-3A is spin-coated at 4000 rpm with 2000 rpm/s acceleration. The photoresist is soft baked at 180 °C for 5 min. S1813 is spin-coated at the same speed on top of LOR-3A for 60 s and then soft-baked at 120 °C for 1 min and 20 s. The photoresist stack is exposed in the UV-mask aligner and later developed in MF-319 developer for 60 to 90 s. The substrate is descummed through 1 min of O_2 ashing at 100 W. The top electrode Pt/Ti (100/20 nm) layers are evaporated in the e-beam evaporator (Lesker Evaporator 252) at deposition rate of 2 nm/s. The photoresist is then lifted-off from the substrate surface using mr-REM400 in 55 min at 100 % ultrasound sonication.

(c) The layers are etched one-by-one through separately patterned resist masks. For each layer, an AZ4562 thick resist pattern is spin-coated at 3000 rpm/s for 30 s, and then soft-baked at 100 °C for 3 min. The resist is exposed through an Ultra Violet (UV) enabled mask aligner for 50 s. The exposed pattern is then developed in MF319. The resist deposited on top of the surface protects the required layouts on the wafer. The 1.1 μm PZT layer is etched through a solution of HF:HNO_3:H_2O in 1 min 20 s.

(d) The buffer oxide and the bottom Pt/Ti layers are etched by the same Argon plasma exposing the bottom most SiO_2 layer.

(e) A resist mask is deposited over the electrodes, and the device Si layer of the SOI wafer is etched down to the buried oxide through SF_6 and C_4F_8 deep reactive ion etching (DRIE) process in Centura II (DPS & MxP). The etch process is performed by the tool in three steps, 1.2 s of C_4F_8 passivation layer deposition, followed by the passivation breakthrough step of 1.3 s and Si etching step of 1.5 s. More information on the recipe is provided in Paper 1. The DRIE process lasted for 21 min for a 20 μm Si etch.

(f) The wafer is then processed from the backside. The SOI wafer is bonded onto a carrier wafer by a thermal tape (120 °C release temperature), and an Al hard mask is etched; firstly a 500 nm Al layer is sputtered at the back; it is then patterned via ma-N1410 negative resist – the wafer is heated at 100 °C for 5 min, the resist is spin-coated at 4000 rpm and then patterned through backside enabled UV mask aligner; finally an 85 % H_3PO_4 solution is used for etching Al in 3 min and 30 s. Later, AZ4562 resist mask is deposited and patterned to protect the proof-mass

structures. Since the etch rates for AZ resist:Si is 1:66, the 7 μm resist mask is thick enough to sustain the 100 μm Si etching.

(g) Si is then DRIE etched using SF_6 and C_4F_8 in STS-ICP plasma etcher in two cycles – etching for 12 s and passivation for 7 s.

(h) The resist mask is then removed, and the bare wafer is etched from the backside for 280 μm until the buried oxide is reached.

(i) The remaining buried oxide SiO_2 layer between the device and bulk layer of the SOI wafer is etched in HF solution for 45 min to release the cantilevers.

(j) The device is cleaned in acetone, IPA and DI water for 5 min each without sonication and then dried in the oven at 100 °C. For further cleaning of the surface, O_2 ashing was employed.

Once the required structures are obtained, the wafer is diced into smaller chips.

2.2.3 Results

The results for the eigenfrequency simulations are shown in Figure 2.7(c). The M-long design has its first two resonating frequencies at 1232 Hz and 1456 Hz.

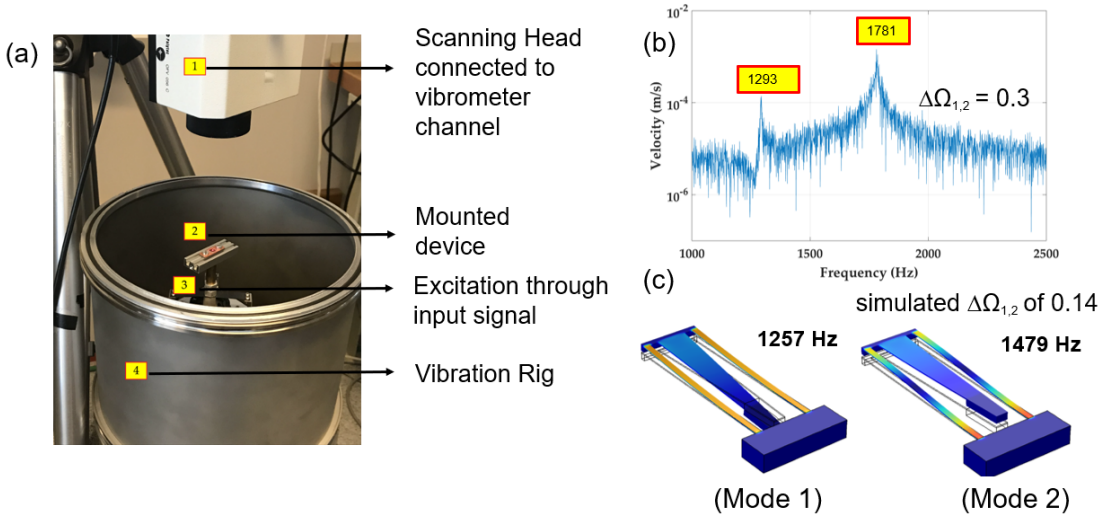


Figure 2.7: (a) LDV setup for the vibration measurement experiments. (b) Characterization of *M-long* in a LDV setup for a periodic chirp pulse with a voltage signal of 0.1 V. The $\Delta\Omega = \frac{\Delta f_{1,2}}{\omega_1}$, where f_1 and f_2 are the first two natural frequencies observed. (c) Simulated first two natural frequencies for the M-long shape.

The von-Mises stress, scalar quantity of the stress vectors, gradient suggests that the vibration of the middle beam enhances the distribution of stress on the cantilever beams on each of the three designs. The middle beam does not act as a dormant proof-mass; it has its own characteristic vibrational mode. The presence of stress on the middle

beam is coupled with the side beam's stress, which leads to a larger area acting under stress. M-long displays a characteristic curve where the stress at the free and fixed ends is nearly constant.

A setup of instruments is designed to record the vibrational characteristics of the device, shown in Figure 2.7(a). It consisted of a laser interferometer and reference, shaker table, photodetector, and a vibrometer. The object is placed on the excitation table. The laser beam from the scanning head is positioned to a scan point on the object through mirrors fitted into the system. The scattered light from the device is received correspondingly. The backscattered light interferes with the reference beam at the scanning head and the photodetector records this interference. The decoder in the vibrometer provides a voltage which is proportional to the velocity of the vibration parallel to the measurement beam. This voltage output is digitized and processed as a vibrometer signal. There are various kinds of excitations possible in the measurement setup. They can be periodic with rectangular or sinusoidal vibrations, transient, i.e., with a pulse or an impact blow, and random noise generated signals.

Figure 2.7(b) shows velocity response in the measured frequency domain for the free end of M-long device when investigated under an electrical signal. M-long device is subjected to a periodic chirp signal of 0.1 V across 3.5 kHz. The first two eigenfrequencies are measured at 1294 Hz and 1781 Hz. The shift in resonance peaks can be attributed to over-etching of the proof-masses. An interesting phenomenon in the graph is the presence of substantial oscillations between the two resonance peaks. This is the effect of using a 2DOF design that the device is stressed even at frequencies away from its eigenfrequencies due to its coupling mechanism.

2.3 Issues in fabrication

While the cantilevers for the energy harvester could be fabricated using MEMS technology, we encountered several issues that resulted in the destruction of several devices on the 6" SOI wafer. We will review these issues and steps taken to mitigate them in the following section.

The first major issue arises in depositing PZT using a sol-gel process on a substrate. The thickness of the PZT layer could not be increased to more than 1.1 μm without noticing severe cracking in the deposited layer. This can be attributed to a large epitaxial stress introduced in the layers due to subsequent spin-castings. As the thickness increases, the number of amorphous domains in the stack increases. The domains can agglomerate with domains in their vicinity to form a structure with lowest entropy. This leads to cracking in the PZT layer. Since the layer thickness cannot exceed 1.1 μm, the expectation of high power density performance remained unreachable.

The second major issue that we encountered during the fabrication of the first version of harvester related to DRIE processing. The frontside etching is to be performed on a resist patterned, 20 μm thick device layer. Centura II (DPS & MxP) is used for this process step. There were several bubbles trapped at the adhesive during the bonding of the SOI wafer to the 8" carrier after thermal taping. This led to uneven heating during DRIE. If the heating on the substrate is compromised during etching, then there is a risk

of photoresist evaporation due to high temperatures. This issue occurred during the backside etching of the proof-masses leading to uneven etching on the back-side (which is the top-side in the wafer/thermal tape/carrier package) and undesired etching at the top-side (the backside attached to the tape). The thermal taping was also compromised during this fabrication step.

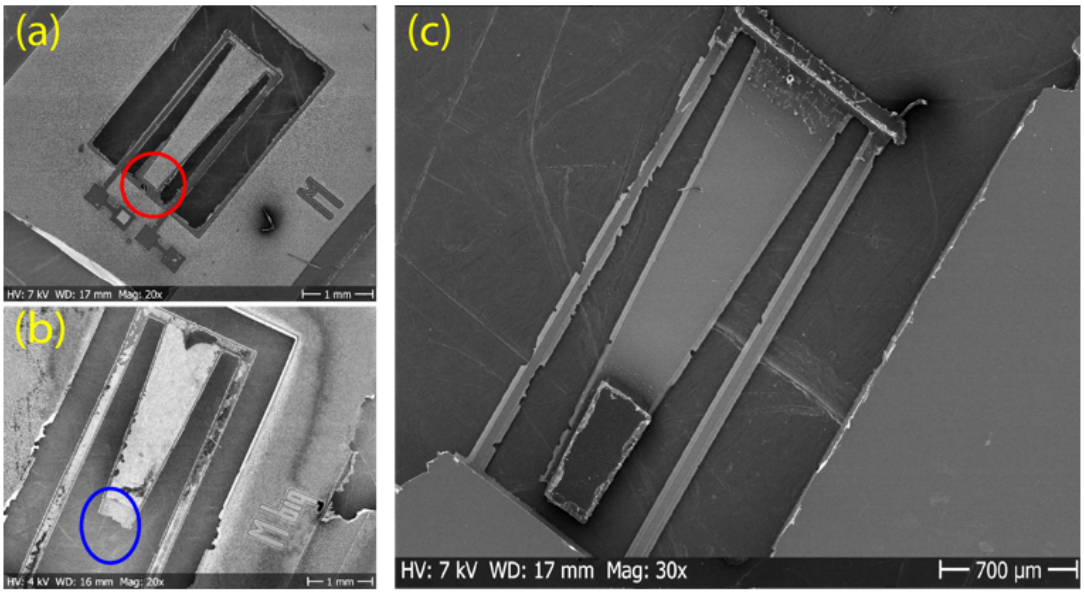


Figure 2.8: SEM micrographs of the fabricated energy harvesters. (a) *M-shape*. The red circle shows the partially etched Si device layer. The results for the fabricated structure are shown in Paper 1 (b) *M-big* after fabrication process. The secondary proof-mass is snapped off during thermal release, its intended place denoted through the blue circle. (c) *M-long*. One of the only devices that could be fabricated on a 6" SOI wafer that contained 189 devices.

Thermal taping was the third major issue we encountered during the fabrication. After we had successfully etched the back-side through to the buried oxide layer of the SOI, we performed the thermal release step at 120 °C. While releasing the tape, devices with uneven and unetched proof-masses stayed on the thermal tape adhesive. Furthermore, we saw that the cantilevers that had released with considerable difficultly from the tape had their top electrodes ripped off from the structure due to the thermal tape adhesive. Thus, it is highly recommended to not use thermal taping for through-wafer etches. Figure 2.8 shows the cantilever structures in scanning electron microscope (SEM). As is visible in the images, the silicon wafer is unevenly etched with some designs remaining unetched due to poor thermal taping, while some devices are broken at the proof-mass end due to the thermal tape adhesive. During the fabrication process, the challenges in frontside etching and the final thermal tape release led to the failure of nearly 90 % of the devices on the wafer.

To overcome the challenges in fabrication, we carried out the fabrication of the first generation energy harvesters on two wafers. Both the wafers broke down due to excessive stress in the substrate during the first lithography step. While we did not carry out further fabrication steps on the first wafer, we completed all the process steps for

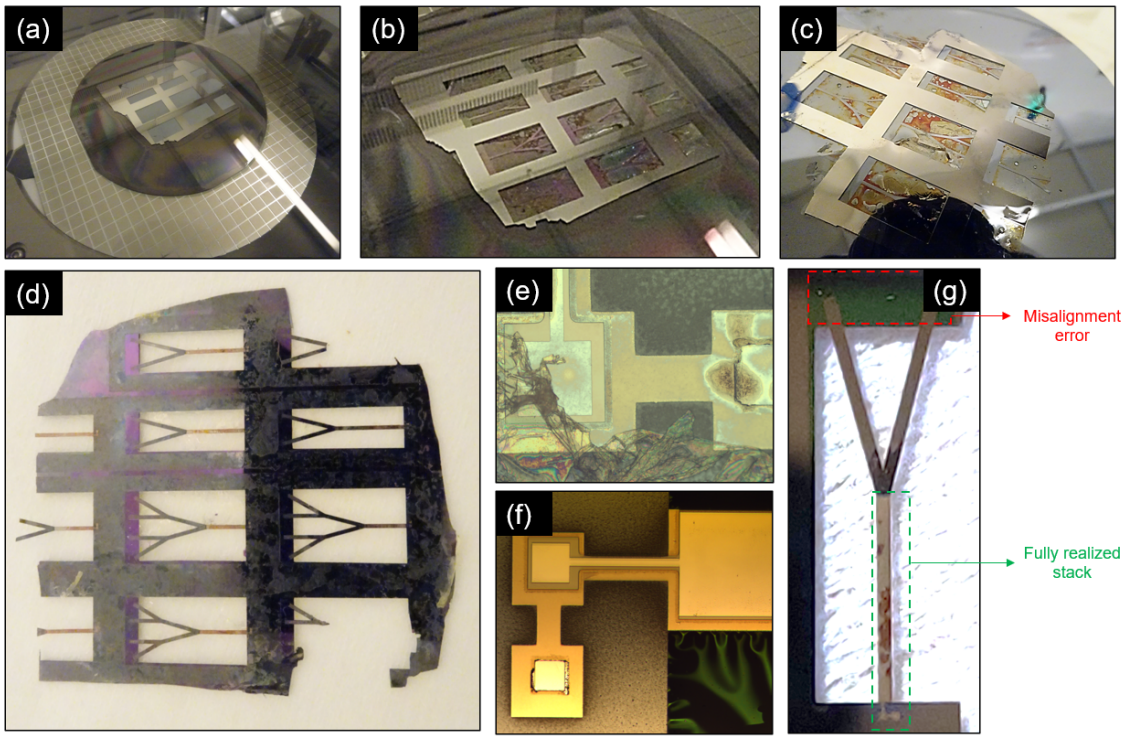


Figure 2.9: Second round of fabrication of the energy harvesters. (a) DRIE process of the broken substrate after photoresist packaging. (b) Optical micrograph of the substrate after DRIE processing. (c) Immersion of wafer package in acetone. (d) Released devices after removing the photoresist packaging. (e) Electrical contacts before O_2 ashing at 300 W and (f) after ashing. (g) Optical micrograph of a single device after dicing.

the second wafer despite various challenges of patterning 3 layers on one side and 1 layer on the backside without proper alignment marks. The main purpose of carrying out the fabrication was to devise a process plan for a backside etch that would establish a high wafer yield.

The process plan for backside etching was considerably improved with the use of a photoresist instead of a thermal tape. In order to make a bond between the aluminum carrier wafer and the chip substrate, the chip substrate backside (the one in contact with the carrier) is coated with thick photoresist AZ4562. The photoresist laden substrate was stuck to a 4" Si carrier wafer. The same photoresist process is applied to the 4" substrate when packing it on top of the aluminum carrier plate. The entire stack was soft-baked at 100 °C for 3 min and then hard baked at 120 °C for 1 hour. The stack is visible in the optical micrograph shown in Figure 2.9(a). The results after through wafer etch can be seen in Figure 2.9(b). The DRIE recipe was kept the same as the previous process plan. The wafer package was then retrieved from the DRIE chamber and placed in acetone for overnight removal of the photoresist. This process step can be seen in Figure 2.9(c). The released cantilevers can be seen in Figure 2.9(d). The cantilever contacts can be seen in Figure 2.9(e). The dirt on the contacts is the dried photoresist after acetone release. The dry photoresist is an indication of the heat that is present in the DRIE chamber. The contacts are cleaned completely through harsh O_2 ashing at 300 W for 15 min. The results from the cleaning can be seen in Figure 2.9(f). These devices, however, are also

not similar to the designs developed. The main issue with these devices was due to the poor alignment between the top- and back-side footprint area. As visible in green in Figure 2.9(g), the free end of the cantilever is still fixed to buried oxide layer.

Therefore, in order to fabricate improved micro-energy harvesters, we devised second and third generations of devices. The second generation of harvesters removes the use of proof-masses as eigenfrequency reducers, while increasing the lengths of side and middle cantilever beams to compensate for their absence. The third generation of energy harvesters is developed after devising a convenient fabrication process explained above. This generation of harvester included a proof-mass as thick as the silicon substrate with a thicker piezoelectric layer (bulk-PZT).

2.4 Improving power density

In this section, we aim to describe the second and third generation of energy harvesters designed to power on-chip sensor nodes on a miniaturized footprint area. The design and fabrication of the energy harvesters require a synergy that as the fabrication can pose certain restrictions on the design. While the design simulated and fabricated in the first generation of harvester was novel and state-of-the-art in terms of the bandwidth of working frequencies in the cantilever performance, the design could not be fabricated due to the issues we discussed earlier. On comparison with the simulations and subsequent power density simulations, we found that the piezoelectric material area was too small to generate even a μW power output. Thus, we required solutions for not only reducing the fabrication complexity, but also improving the power density of the devices.

The second generation harvester addresses the issue of reducing complexity of back-side etching. It is based on 20 μm silicon cantilevers that are prescribed through the SOI device layer thickness. The PZT layer area needs to be increased for tangible energy harvesting on the silicon substrate as the wet etch process etches away as significant amount of PZT during the etch step. Similarly, the PZT on the middle beam also needs to be utilized for the 2DOF mechanism. It addresses the issue of small piezoelectric area through increasing the widths of the side beams in the cantilever design.

The third generation harvester was based on a more free form design only limited by its footprint area i.e. 1 cm^2 silicon die and M-shaped 2DOF structure. It addresses the issue of power density primarily by utilizing a thicker cantilever beam to increase the stress amplitude on the cantilevers and bulk-PZT (120 μm) to demonstrate over 100 mV output between its first two to three natural frequencies.

2.4.1 Second generation harvesters

The aim of the second generation of energy harvester is to develop a design that exhibits a large bandwidth by employing the 2DOF principle and which generates a significant voltage of over 100 mV for a sufficiently wide range of frequencies. The design is developed from the first generation energy harvester by varying the factors that affect the natural frequencies of the system namely - length, width, spacing between the middle and side beams, and thickness. The thickness of the silicon cantilever beams is kept

at 20 μm and the PZT thickness is also constant at 1.1 μm as the wafers acquired from Silex Microsystems. The designs for the second generation are shown in Figure 2.10(a - c) at the first two natural frequencies.

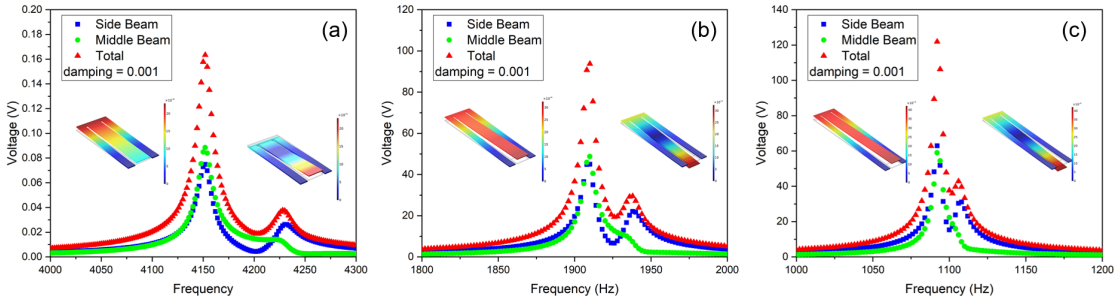


Figure 2.10: Voltage outputs of the second generation of piezoelectric micro-energy harvesters with cantilever beams of (a) 2 mm, (b) 3 mm, and (c) 4 mm lengths. For more information, the reader is referred to [155]

Another important aspect of design is the presence of piezoelectric material on the middle cantilever beam. Although, the piezoelectric patch was also present on the middle cantilever beam in the first generation of harvesters, the electrical contacts to the middle beam were linked to the piezoelectric patches on the side beams. The second generation harvester is designed for separate connections between the side beams and the middle beam. As the middle beam is fixed to the free end of the side beams, its electrical contacts are formed from pathways on the side beams. Thus, we also needed to increase the widths of side beams without reducing the bandwidth of electrochemical response.

The results from the eigenfrequency and frequency sweep simulations can be seen in Figure 2.10. The second generation harvester includes three main designs each of different lengths with a governing ratio between the side beam and middle beam lengths. The simulation was conducted in the Shell Beam module of COMSOL Multiphysics, with a damping ratio suggested by the experiments on the first generation cantilever beams. The designs, at the first eigenfrequency, the structure undergoes pure tension or compression and at the second eigenfrequency, the structure generates stress due to a mix of tension and compression along the beam. The figures show the individual and added contributions of the inner beam and outer beam. More information on the design can be accessed in Johan Andersson's masters thesis [155].

This design used a 1.1 μm PZT film that cannot establish high power densities between the inter-peak valleys of the eigenfrequencies. As we found that we could not bring the natural frequencies closer, we require a thicker piezoelectric material to improve the output voltage from the harvesters.

2.4.2 Third generation harvesters

In the third generation of energy harvester design, the main attention is focused towards improving the voltage output between the lowest eigenfrequencies. One method to increase the output of the harvester is to increase the amount of piezoelectric material layered on the cantilever beams. Another method to obtain a high voltage is by

Table 2.3: Dimensions of second generation energy harvesters used in COMSOL simulations, in μm.

Dimensions	**2 mm**	**3 mm**	**4 mm**
l_s	2000	3000	4000
w	900	900	900
l_m	2000	2990	3980
w_{m1}	400	400	400
w_{m2}	300	100	400
w_s	200	200	200

increasing the stress on the beams by making the cantilevers thicker. Thus, in the third generation energy harvester, we designed a single and double fold M-shape harvester in an iterative process, starting out from Johan's work [155].

The total footprint area of the energy harvester is kept at 1 cm^2 as a realistic representative size for a self-powering on-chip sensor node. The thickness of the cantilever beams were limited to 100 μm and bulk-PZT (Precision Acoustics) was chosen for a thickness of 120 μm. As the cantilever beams were thicker, the natural frequencies scale up proportional to the square-root thickness of the beam. To negate the high frequency design, we included a proof-mass once again to bring the natural frequencies of the system to a range that we had previously worked on in the first and second generation harvesters. The schematics of the single- and double fold harvesters are shown in Figure 2.11(a - b).

The dimensions of the two designs studied in this generation are listed in the Viktor's thesis [156]. The double-fold harvester has an extra fold within the middle cantilever to exploit closening of more than two natural frequencies of the system. The proof-masses of the system are designed to be of the same thickness as the bulk Si layer of the substrate, i.e. 500 μm. The single fold generator results in an operating bandwidth (V > 0.1 V) of of approximately 1400 Hz from 1100 Hz to 2500 Hz as can be seen in Figure 2.11(c). The differently colored peaks for voltages over a range of frequencies show the change in eignefrequencies for by changing its proof mass weights. The proof mass length l_{po}, is simulated beyond the 1 cm^2 bounded area in the Shell beam module to get the estimate of the total weight required for the silicon proof-mass. The silicon proof mass is to be etched through DRIE or wet etching of substrate backside. The thickness of the PZT layer improves the amplitude of the inter-peak valley trend that was visible in the second generation harvester. The design for the double-fold generator results in a bandwidth of about 800 Hz operating between 800 Hz and 1600 Hz Figure 2.11(d). The single fold generator is superior in terms of tolerance in the inter peak valleys referring to the voltage output margin to the threshold of 0.1 V in the valley. On the other hand, the bandwidth of the double fold generator is larger than the single fold generator with respect to the minimum threshold of 0.1 V. With such a large range of frequencies providing a useful voltage output, these devices provide a potential solution to the problem of output beyond a small range around specific eigenfrequencies in piezoelectric microgenerators.

The fabrication of the third generation harvester follows a different process than the

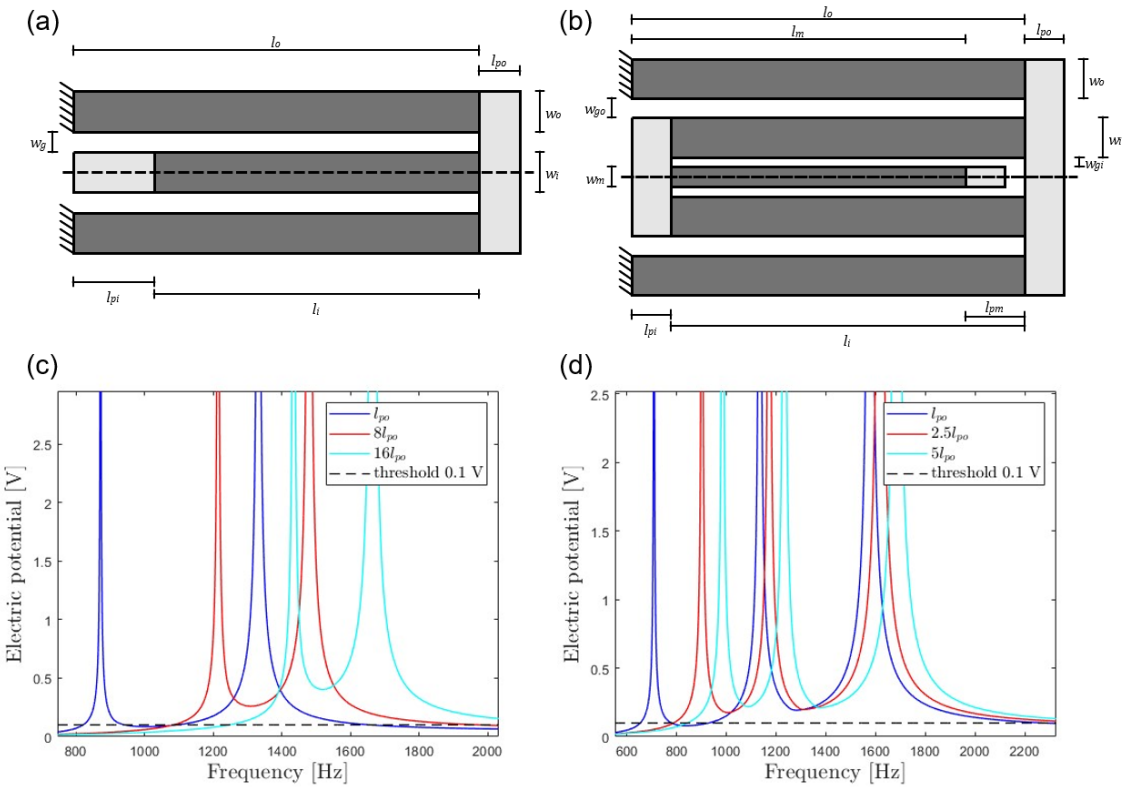


Figure 2.11: Schematic designs for third generation of piezoelectric micro-energy harvesters. (a) Single-fold M-shape structure with proof-masses, (b) Double-fold M-shape structure with proof-masses. (c) Simulated electrical voltage from single-fold M-shape cantilever beams. Beams of varying l_{po} signify the proof-mass weight required to achieve the same convergence of eigenfrequencies, (d) Simulated electrical voltage from double-fold M-shape harvester.

generations discussed earlier. In this process, the bulk PZT requires to be attached to the wafer substrate using bonding techniques. We have previously reviewed one form of bonding, i.e., photoresist bonding for the attachment of the harvester substrate to the carrier wafer. The bulk-PZT bonding follows a similar process applying an epoxy glue in place of the photoresist. Another method of substrate to PZT bonding involves evaporation of an Au thin film on the connecting substrates of the PZT and substrate and then annealing the package under generation of high electric field (200 - 1000 V) and temperature (150 ° C) [157]. This form of anodic bonding is prevalent in bulk-PZT fabrication. The remaining process steps from Figure 2.6 (a-g) are the same with added precaution necessary due to bulk-PZT thickness during backside etching. More information on the device design and fabrication is listed in the master's thesis of Viktor Sjöstrom [156].

2.5 Discussion and conclusion

Among the various harvesting techniques, piezoelectric energy harvesting can convert the ambient vibrational energy into electrical signals using piezoelectric mate-

rials through various compliant mechanisms. These mechanisms generally include monostable, multi-stable, frequency-up conversion, and multiple-degree-of-freedom structures. The nDOF structures, due to their in-plane designs and ease of conversion to a MEMS integrable process, have the highest potential to be investigated for on-chip energy harvesting for a self-powering miniaturized sensor node.

We have shown three versions of nDOF energy harvesting structures and have attempted fabrication of the former two designs. The first nDOF harvester (M-long) was fabricated using MEMS technology and was characterized for its eigenfrequencies and displacement at various frequencies of operation. The design was optimized for improvement of stress distribution on the cantilever beams using the combined principles of cut-out vibrating proof-mass and trapezoidal beam design. Thinner proof-mass is also one of the characteristic features of the design. Although the designs could achieve a closening of eigenfrequencies, it had several issues - mainly related to the fabrication of the structures and the thickness of the piezoelectric materials. The fabrication issues arose from the implementation of complex back side processing that involved three hard-mask etching steps and its subsequent release of the top side from the thermal tape. The cantilever design was fabricated but the top electrodes were ripped off due to the thermal release. Using thinner proof-masses added greater complexity to the fabrication process as we required an extra cleaning step for the photoresist after etching the proof-mass to 100 μm. Using aluminum as a hard mask for through wafer etching is also not a good technique as it leads to re-deposition of micro Al masks on the etched surface. This leads to formation of silicon grass on the substrate which is detrimental to the etch-rate and uniformity of etching across the wafer [158].

Another issue, we realized after the fabrication of the M-long harvesters, was the poor current response from the energy harvesters. Although the voltages that can be acquired range from 10 mV to 10 V, but the current response from the PZT beams is limited to nA. This leads to a poor power density of the harvesters. As the response from literature studies suggest that the power is limited for vibrational energy harvesters, it is necessary to invest further research in piezoelectric materials that can exhibit a higher power conversion efficiency and can facilitate MEMS compatible fabrication.

We have addressed both the issue of complex backside fabrication and low output power density in the next versions of the nDOF MEMS harvesters. The fabrication process was improved in the second round in which we fabricated a fractal-based planar nDOF design without proof-masses. In this process, we removed the thermal taping process and replaced it with a photoresist attachment between the carrier plate and wafer substrate. The wafer yield was significantly better in this process compared to thermal taping.

Still, we encountered other challenges such as wafer breakage during a lithography step, masking mismatch between the top-side and back-side, and cantilever breakage during dicing. The breakdown of the wafer during the top-electrode lift-off process was surprising. This can possibly be attributed to mismatched stresses on the two sides of the substrates with a Pt/Buffer/PZT layer on the top-side. Even after wafer breakdown, we continued the fabrication process on one of the substrate pieces. The mismatch between the top and back side alignment was due to the wafer breakage as we had no in-line alignment marks to work with. Finally the fabricated structures could not

sustain the dicing process due to the high frequency vibrations of the blade and the high pressure water flow from the coolant nozzle.

These issues can be mitigated by using smaller substrates compared to 6" SOI wafers. Dicing is a hard challenge for PEHs. We applied a diamond blade technique to dice the devices post-fabrication. Although the process is less destructive, it still has various inconveniences. Firstly, the vacuum suction in the diamond scriber was not appropriate for free standing structures. Secondly, the scriber has to be extremely sharp if it has to make appropriate dents for wafer breakage points. In the absence of such a blade, the user is compelled to scribe the lines multiple times on the wafer. This leads to unwanted defects in the crystalline structure of the wafer, which eventually leads to breakage over undesired areas. Finally, there are health issues pertaining to breaking wafers using a diamond scriber. The minuscule Si nanoparticles can easily enter our lungs and contaminate the biological environment. This can lead to severe pulmonary health issues. In order to reduce the complexity of the fabrication process, we designed the second version of energy harvesters without proof-masses. The middle cantilever beam was extended beyond the side beam lengths to negate the absence of proof-masses. We could achieve similar results in terms of bandwidth improvement in the cantilever design through a 2DOF design. These designs are currently being fabricated on 1 cm^2 SOI chips. This footprint area can house up to 4 designs. Since we have incorporated all three designs on a single chip, we expect a wide coverage of operational bandwidth ranging from 1100 Hz to 4150 Hz.

In the third round of harvester design, we focused on the aspect of increasing the power density of the energy harvester through utilizing a proof-mass with a thickness equivalent to the wafer thickness to avoid the Al process step. As explained earlier, the proof-mass is essential to lower the working frequencies and to increase the stress on the cantilever beams to produce a larger output. We also increased the thickness of the piezoelectric layer by using commercialized bulk-PZT of 120 μm. The design was similar to the previous 2DOF harvesters in the aspect of 1 cm^2 footprint and having cut-out beams for the middle cantilever. The cut-off of output voltage between the first few eigenfrequencies was set to 100 mV as well. The intended design is also designed to be fabricated using a MEMS process with a PZT to wafer bonding step in the beginning.

In conclusion, we have demonstrated three generations of 2DOF MPEHs for powering on-chip wireless sensor nodes within a 1 cm^2 footprint area. The first generation of harvesters showed an outstanding expected improved bandwidth of 1293 - 1791 Hz. The fabrication issues in the manufacturing process for the first version of harvesters were removed by fabrication of fractal-based cantilevers by using a photoresist attachment. The second generation MPEH simulations employed increasing lengths of the cantilever beams to negate the absence of proof-mass. The third generation MPEHs focused on the aspect of getting an above cut-off output between the vibrational eigenfrequencies. Although there are several remaining challenges in incorporating PEHs starting from fabrication to power output, these designs can be used to power wireless sensors in areas where vibrations range from 100 Hz to 5000 Hz, a range typical for heavy machinery used in manufacturing, industry, and mining [159]. With the employment of efficient power conditioning circuitry and MSCs, MPEHs can be integrated for on-chip harvesting of ambient energy to power wireless sensor nodes.

Chapter 3

Microsupercapacitors

With electronic device miniaturization following Moore's law, SoC and system in package (SiP) technologies can show high processing capabilities within the same footprint area. As their functionalities increase, there is an increase in power consumption in microelectronic devices. These devices will benefit from having access to an on-chip energy storage unit. Traditionally, batteries have been the primary power source in electronic packages due to their high energy density. Batteries, however, suffer from poor charging/discharging rates and low lifetimes. On the other hand, supercapacitors offer an excellent contrast to batteries with very high power densities, short charging/discharging times and a long lifetime of charge storage capability.

Supercapacitors generally utilize formation of capacitors at an electrode-electrolyte interface in the presence of a potential difference. The electrode material is a conductive film, sheet, or a group of particles that possess a large surface area for the interaction with the electrolyte. The electrolyte is a solution with ionic charges that can be separated when a potential difference gives rise to an induced electric field. In the presence of a potential difference, the electrode material interacts with the electrolyte ions. This electrostatic interaction leads to the formation of nano-capacitors with $d \approx nm$ [18]. These capacitors in parallel configuration result in a large capacitance at the electrode-electrolyte interface. It is generally considered in the literature that interaction can be described as forming an EDL at the electrode-electrolyte interface. Helmholtz discovered this phenomenon for the first time in 1853 [160]. The studies by Guoy-Chapman in 1910 and 1913 [161] and later by Stern in 1924 [162], improved the theory of EDL charge storage further. The stored charge can then be used to power a sensor node or the electronic unit connected to the output of the on-chip power storage unit.

A supercapacitor has three main principles of storing charge - in the EDL, pseudocapacitively, by a hybrid of the two. In EDLCs, charge storage takes place electrostatically (non-Faradaic) i.e., no shifting of matter takes place between electrode and electrolyte (which makes them highly reversible along with high cycling stability). Pseudocapacitance is another form of charge delivery in supercapacitors. In this case, the electrode stores charge through electrosorption, intercalation, and oxidation/reduction reactions between the electrode and electrolyte. Both these forms require a high surface area of interaction between the electrode and electrolyte. Thus, we can say that the choice of electrode material is mainly dependent on its specific surface area. Also, for a better

capacitor formation at the interface, the electrolyte ion size should be equivalent to the pore size in the electrodes [18].

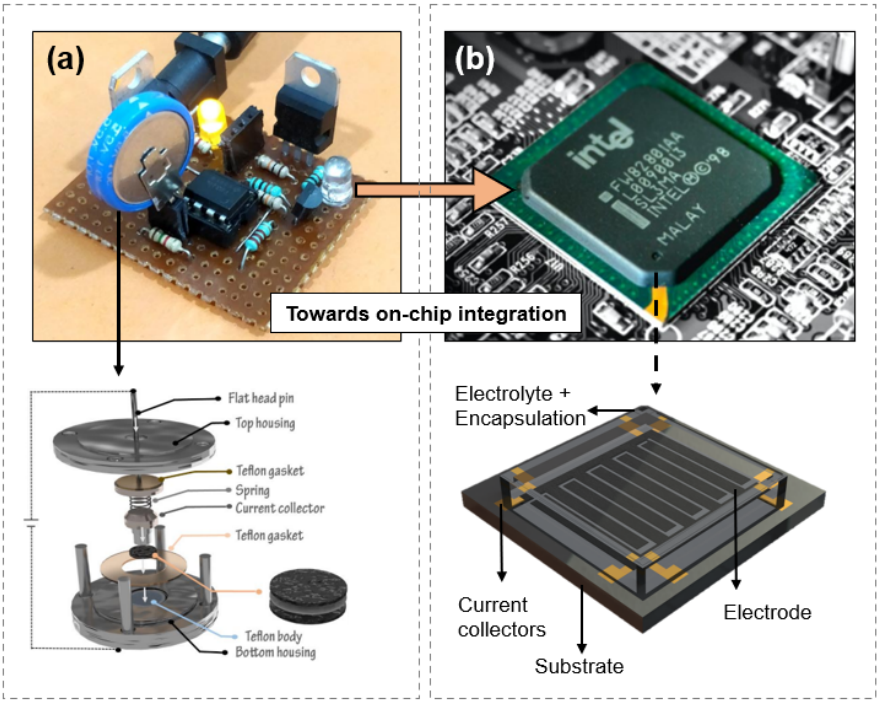


Figure 3.1: (a) Various SiP components assembled on a PCB including a supercapacitor in a coin cell assembly. The assembly includes various subcomponents fitted to encapsulate the electrode-electrolyte-separator assembly. (Image reproduced from Li et al. [163], and circuit digest, [164]), (b) Example of a SoC IC unit. The MSC unit such as a planar designs with electrode-electrolyte-package can be included in a FEOL or BEOL processing step with the IC. Image acquired from Intel Inc. [165]. Other images reproduced after permission from the respective authors or publishing agencies.

Supercapacitors are generally manufactured in the form of coin cells or in box-like configurations. Coin cells are circular coin-shaped current collectors that also form the casing of the electrodes and electrolytes in the form of a cylindrical shell. The electrodes are cut out in the form of circular films to fit into each end of the coin cell. The electrolyte is then introduced in the system through a separator, a porous non-conducting film that allows the transportation of ionic charges across its interface. There are several commercial methods of manufacturing the electrode-electrolyte-separator composition of energy storage. Among them, coin cells, pouch cells, rectangular lids with screwing mechanism, or battery like cylindrical cells are currently widely used for packaging. An integrated SiP configuration is demonstrated on a PCB in Figure 3.1(a) which uses a coin cell packaging for the supercapacitor application. The coin cell in the printed circuit board (PCB) takes up a large fraction of space on the circuit board, leaving little space for other SiP components that could have improved the functionality of the sensor node. A custom coin cell is displayed that incorporates activated carbon as its electrodes and a polymer electrolyte 1-ethyl-3-methylimidazolium acetate (EMIMAc) as the electrolyte. Another configuration of supercapacitors is the box-type assembly, where a rectangular box is used instead of the circular shaped current collector [166]. Both these designs

have been commercially manufactured and are being used in high power applications in conjunction with batteries [167].

MSCs have emerged as potential solutions to replace or complement batteries in electronic systems that steadily decrease in size. Therefore, developing CMOS compatible fabrication processes has attracted much attention over the past few years [75, 76, 77, 64, 71]. These devices can be integrated either as self-powering systems with charging through energy harvesters or enhanced micro battery systems where they act as hybrid devices with batteries to improve the lifetime of a device. Ideal incorporation of MSC in the SoC package is symbolically represented in Figure 3.1(b), where an Intel microprocessor unit is shown. The ideal MSC, packaged and encapsulated, should fit in the processing of the semiconductor chip shown above in a FEOL or BEOL processing technology.

In order to be integrated with CMOS circuits, these MSCs need to be fabricated through similarly compatible fabrication techniques. In this chapter, we shall first delineate the MSC figures-of-merits that form the basis of the electrochemical evaluation of the device, followed by various fabrication technologies that can manufacture MSCs on a wafer-scale level. The advantages and disadvantages of these technologies are examined in detail after an extensive literature survey. The impacts of electrode geometry and electrode thickness are also examined, followed by suggestions for an improved design. We will explain the fabrication of MSCs through a scalable spin-coating method. We present fabrication and device performance challenges and methods utilized to overcome them. We shall also discuss the fabrication and performance of the spin-coating method for various graphene-based electrodes. Finally, we shall validate the application of spin-coating in stacking different materials on the same substrate to improve the device's performance.

3.1 Supercapacitor figures-of-merit

An MSC can be considered to be a capacitor with very high charge storage capability owing to its electrode geometry that gives high specific surface areas. The relationship between capacitance, C, charge and voltage is as follows:

$$C = \frac{Q}{V} \tag{3.1}$$

where Q is the total stored charge, V is the is the voltage between the two electrodes of the capacitor. Experimentally, the capacitance of a device is calculated through cyclic voltammetry (CV) experiments. CV measurements are a set of experiments in which the electrode potential between the electrodes is ramped up with a scan-rate, ν. The cyclic voltammetric capacitance, $C_{A,V}$ is normalized over a surface area (A) or volume (V).

CV measurements are used to determine the system properties such as potential window for the electrolyte functioning, contributions from faradaic reactions, and the effects of scan rate of device capacitance. An in-depth explanation of CV measurements is provided at Conway et al. [168].

The MSC can also be evaluated by charging at various current densities. The MSC is experimentally charged and discharged at different current densities and the capacitance is calculated by taking the effect of series resistance into account through the voltage drop ΔV it induces when switching from charging to discharging current. We determine the $R_{esr} = \Delta V/(2I)$, equivalent series resistance of the MSC. The capacitance is then calculated as

$$C = \frac{I \times t_d}{V - \Delta V} \tag{3.2}$$

where t_d is the discharging time for the MSC, and I is the current density. The charging/discharging measurements are called galvanostatic charge discharge (GCD) measurements. They are typically used to measure the electrochemical properties of the MSC over time at different input currents and capacitance retention. They are also useful to evaluate the lifetime of charging discharging cycles that an MSC can withstand before deteriorating to < 80 % of its initial capacitance.

The energy density of the MSC is calculated from the CV and GCD measurements as

$$E_x = \frac{1}{2} C \times V^2 \tag{3.3}$$

The power density is calculated as

$$P_x = \frac{V^2}{4 \times R_{esr}} \tag{3.4}$$

Electrochemical impedance spectroscopy (EIS) is another important measurement technique for MSCs that represents the impedance behavior of the MSC as a unit. We can analyze the capacitance of the device over a range of frequencies ($f = \omega/2\pi$). A small ac input signal is introduced to the MSC over a range of frequencies. The impedance Z represents the complex impedance of the device. The real and imaginary capacitances for a given frequency, C_{real} and C_{imag} are then calculated as

$$C_{real}(\omega) = \frac{-Z_{imag}(\omega)}{\omega \times |Z(\omega)|^2} \tag{3.5}$$

and

$$C_{imag}(\omega) = \frac{Z_{real}(\omega)}{(\omega \times |Z(\omega)|^2)} \tag{3.6}$$

The real and imaginary impedances are plotted in the Bode and Nyquist plots to analyze the EIS of the devices. The Bode plot represents the C_{real} vs frequency plot while the Nyquist plot shows information of the EIS when the data is plotted as Z_{real} and $-Z_{imag}$ in the x and y co-ordinates respectively. The equivalent series resistance R_{esr} of the MSC values from the EIS measurements are calculated by measuring the intercept the intercept extrapolated for a frequency approaching infinity at the Z_{real} axis. The R_{ct}, charge transfer resistance is acquired from measuring the radius of the semi-circle region in the Nyquist plot. The dielectric time constant, τ is calculated

from the peak C_{imag} for a frequency f_0 , also known as the characteristic or knee-point frequency as

$$\tau = \frac{1}{f_0} \tag{3.7}$$

from the Bode plot where τ is the dielectric relaxation time constant for the whole system.

The phase of the device (ϕ) is calculated as

$$\phi = tan^{-1} \frac{Z_{imag}}{Z_{real}} \tag{3.8}$$

3.2 Fabrication methodologies

There are two main configurations for MSC fabrication – stacked and planar. Stacked MSCs are sandwich-type structures with an electrolyte between two electrodes, while planar MSCs are devices with two in-plane electrodes separated by a specific distance. A planar MSC design holds several advantages over the stacked structure. Firstly, since the planar electrodes are on the same substrate, the lateral distance between electrodes can be defined to be much smaller than the distance defined by a separator. Secondly, the stack of electrodes, electrolytes, and current collectors would require specific masking techniques in the fabrication process, leading to a challenging list of process steps. Thus, for high-performance planar MSCs, it is imperative to have an electrode deposition technique that results in robust electrodes and ensures that the deposited film can sustain and withstand post-processing lithography and device integration steps. A variety of methods can be used to fabricate thin films of these materials [169].

EDLC MSCs generally utilize graphene as their primary electrode material. A typical graphene-based single layer film can demonstrate a theoretical capacitance of 21 μF cm^{-2} [170] owing to its large specific surface area of 2630 m^2 g^{-1}. Furthermore, graphene as a material displays several excellent characteristics such as high electron mobility, high conductance, doping feasibility, non-toxic nature, and low material decomposition. The material owing to its feasible tunability of application-based electrical characteristics has the potential to be utilized in a FEOL process for the fabrication of on-chip sensors and storage on the same planar footprint.

Applications requiring the integration of supercapacitors with CMOS technology require coating and patterning methods compatible with CMOS processes, chemistry and temperatures. MSCs can be fabricated depending on their target application and process limitations [35]. Manufacturing approaches include electrophoretic deposition, electrospinning, chemical vapor deposition (CVD), spin coating, laser scribing, inkjet printing, 3D printing, shadow masking, spray coating, electrodeposition, and electrode conversion have been used to coat electrode materials onto a wide variety of target substrates. The processing technology of MSC fabrication defines the resolution of the electrode geometry. Based on the necessities and budget of the application, we can determine the fabrication methodology suitable for graphene-based electrode deposition. Among various techniques examined above, only a handful of techniques can be deemed CMOS compatible in the current state of IC manufacturing - CVD, spin

coating, inkjet printing, laser scribing, electrodeposition and electrode conversion. The working mechanisms for the selected techniques are shown in Figure 3.2.

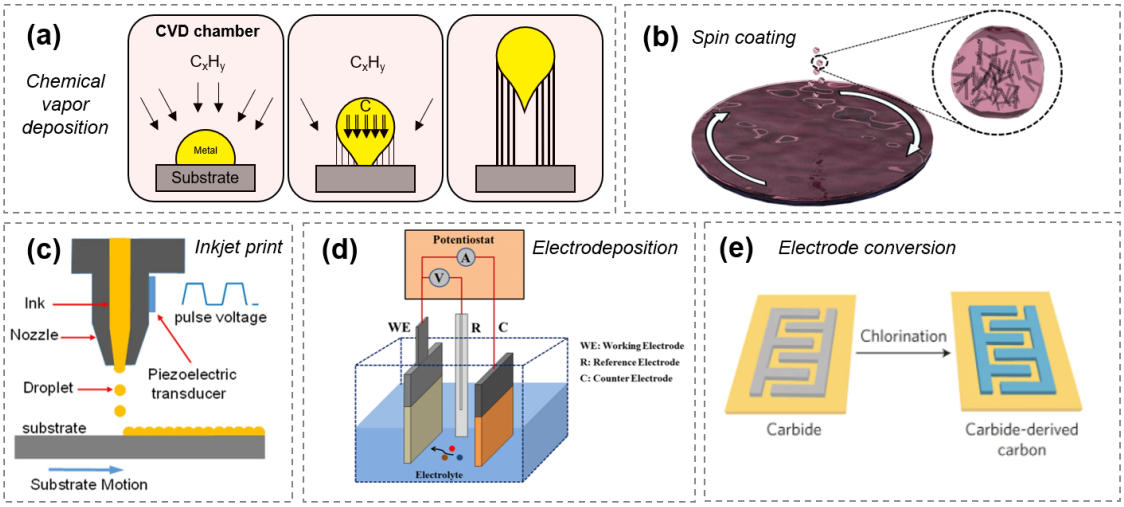


Figure 3.2: Working mechanism of fabrication methodologies deemed compatible for CMOS scale device integration of MSCs. (a) Chemical vapor deposition. (b) Spin coating, (c) Inkjet printing from Lin et al. [171]. (d) Electrodeposition by Ho. et al [172]. (e) Electrode conversion by Pech et al. [173]. Images reproduced after permission from the respective authors or publishing agencies.

3.2.1 Chemical vapor deposition

Chemical vapour deposition (CVD) is an attractive electrode fabrication process as it is pre-existing in the semiconductor industry for thin film deposition. CVD growth on a particular substrate starts with a metal precursor as shown in Figure 3.2(a). The substrate is held at a very high temperature (300 - 700 ° C) in a glass chamber. Later a carbonized gas is introduced in the system that dissociates at high temperature into its constituent carbon element and other molecules such as nitrogen or hydrogen. The form that carbon materials develop is dependent on both deposition and etching dynamics/kinetics. This technique has been used to grow various graphene and carbon-based electrodes for on-chip MSCs. Since this process also allows a one-step growth process of MSCs, CVD grown electrodes for MSCs can drastically change the energy storage architecture in CMOS circuits.

Several carbon-based materials have found a way among MSC electrodes through this growth process. Among these, graphitic petals or graphene nanosheets directly synthesized on Ni foil and carbon cloth using microwave plasma chemical vapour deposition (MPCVD) exhibit promising potential for MSC applications [174]. Xiong et al. fabricated high-power MSCs based on micrometres-thick graphitic petal electrodes [175]. The electrodes were prepared using microwave plasma CVD and patterned by optical lithography and reactive ion etching. Similarly, multilayer graphene and monolithic 3D graphene have also been fabricated by Ye [176], and Zhang [177], respectively. A wide variety of materials, such as diamond-coated Si nanowires, has also been grown through the CVD technique. These were used to fabricate asymmetric MSCs [178].

Similarly, Zhang et al. [179] developed a facile vapour deposition and sewing sequence to create rugged textile MSCs. Some reported performances of the CVD process are given in Table 3.1.

Among on-chip solid-state MSCs fabricated through CVD growth, graphene MSCs showed by Wuttke et al. [180]. They showed a capacitance of 66 μF cm^{-2}. Carbon-based materials have been combined with electrophoretic methods to introduce pseudocapacitive materials in CVD grown electrodes. CVD grown graphene with SiC and silicon nanowires (SiNWs) show an areal capacitance of 3.2 mF cm^{-2} [181]. CVD grown vertically aligned carbon nanotubes (VACNTs) with TiO_2 and TiN layers show a capacitance of 5.2 mF cm^{-2} by Zhang et al. [182]. Graphene with PANI and silicon nanowires demonstrated a very high capacitance of 85 mF cm^{-2} in work reported by Tuon et al. [183]. Later Li et al. [184] showed a capacitance of 185 mF cm^{-2} using the same material. With the exhibition of such high areal capacitances and a one-step growth process, MSCs fabricated through CVD have the potential for integration with on-chip sensor nodes. The process is already used for the fabrication of MBs as well. However, to be integrated with CMOS technology, CVD growth of carbon materials requires to be conducted at lower temperatures, preferably approaching 350 °C. Also, the non-ideal thermal gradient across the wafer substrate in the growth chamber needs to be improved for the proper growth of materials in the CVD process.

3.2.2 Photolithography

Among the list of different fabrication processes described, with photolithography, MSCs can be fabricated easily and cheaply with an extremely high resolution that depends only on the lithography tool available. A schematic of the deposition process is shown in Figure 3.2(b).

Several strategies can be used to fabricate MSCs using photolithography. One is spray coating, where an electrode material is spray-coated on a substrate. Then either metal can be evaporated on the substrate and then etched using reactive ion etching, or a resist can be deposited on the electrode layer, followed by developing trenches for electrode evaporation and lift-off [185]. Another technique variation can be a double lift-off of the electrode and the current collector using a single photoresist mask on the substrate [186]. This process can be called the inverted current collector process as the current collector is on top instead of being at the bottom as in conventional MEMS processes. The main advantage of this technique is that it requires only one photomask. However, there are disadvantages that inhibit the utilization of this process in integration with CMOS circuitry. Inaccessibility of the electrolyte on the top and bottom ends of the electrodes would severely restrict its performance. Secondly, during the development process for electrode or current collector lift-off, the tendency of the electrode material to dissociate from the substrate is quite high.

Pech et al. [187] fabricated a pair of interdigitated electrodes from onion-like carbon that operated as a single MSC. The MSC showed a discharge rate three orders higher than conventional supercapacitors because of how easily ions could diffuse between the electrodes. After that, the research of interdigitated electrodes has expanded to include other materials, such as carbon nanotubes (CNTs), graphene, reduced graphene oxide

(rGO), and hydrated graphene oxide (GO). Laszcyzk et al. [188] demonstrated an MSC fabrication technique where they deposited CNT as an electrode material through a doctor blade technique. Pan et al. [189] followed a new protocol mimicking the spider's spinning process developed to create highly oriented microfibers from graphene-based composites via a purpose-designed microfluidic chip. Similarly, Kim [64] fabricated an electrode based on a boron-doped 3D porous carbon pattern by lithographic processes. The electrode layer is obtained by carbonization and doping a polymer pattern fabricated by interference lithography. Lithography can also be performed on flexible substrates such as PET. Hu et al. [190] fabricated Au/polyaniline (PANI) electrodes involving laser printing technology and in situ anodic electropolymerization while exhibiting remarkably high mechanical flexibility and showing excellent cycling stability (73 % after 10000 cycles). Spin coating of rGO can develop MSCs with 30 μF cm^{-2} [179] and 220 μF cm^{-2} [191] more recently.

Considering the needs of an automated CMOS process, out of the three deposition techniques, spray coating, doctor blade layering, and spin coating, the former is can be easily automated for increasing device yield. Spray coating is a process in which a solution is designed to be used in a jet that sprays the ink across the whole substrate. It is different from inkjet printing in terms of the manner of the coating. An electrode solution is poured on the substrate in a doctor blading process. Then, a blade with a specific distance from the substrate is swiped over the electrode film. In the spin coating process, the electrode solution is analogous to a photoresist, following the same fabrication process used for polymeric resists such as AZ4562 or S1813. Among these, only spin coating emerges out to be a viable option. We want to stress that spin-coating and photolithography is a viable route to use existing standard tools in IC manufacturing, hence it is advantageous, regardless of the various difficulties other techniques need to face before possibly being implemented in manufacturing.

3.2.3 Inkjet printing

Inkjet printing is another promising electrode fabrication technique that can be easily explored in CMOS integration strategies shown in Figure 3.2(c). It is a typical technique used to deposit electrode films at precise places defined by a computer automated design (CAD). With inkjet printing, various electrode films can be deposited, which are not limited to carbon materials. In this process, a liquid ink of an electrode is prepared and deposited on a substrate with a jet nozzle similar to 3D-printing equipment. The process is as scalable as the size of the jet nozzle allows, i.e., it can go up to 2 μm of resolution [192]. The main advantage of inkjet printing is similar to laser scribing as it requires only one fabrication step for electrode deposition. Another significant advantage of inkjet printing over laser scribing and photolithography is the minimum use of ink while fabrication takes place. With laser scribing and photolithography, there is a substantial waste of electrode material, which is either not utilized in the former and wasted during a spin coating or doctor blading process as in the latter. Moreover, the direct phase transformation of the liquid ink into a solid-state active electrode nanomaterial adds to its merits.

These devices have demonstrated high flexibility, excellent rate/mechanical stabil-

ity and high cycling stability with an excellent electrochemical performance holding great promise for applications in flexible all-solid-state MSCs. The process has been used to deposit inks on solid-state substrates as well. Li et al. have demonstrated the development of MSCs that use poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) mixed with graphene quantum dots to show a capacitance of 2 mF cm^{-2} with a high power density of 0.7 mW cm^{-2}. They also showed printing of graphene ink to show a capacitance of 313 μF cm^{-2} and rGO revealing a capacity of 99 μF cm^{-2} and 441 μF cm^{-2}. Inkjet printing can also be used for deposition of MXenes, pseudocapacitive material mixed rGO, and carbon structures such as CNTs, carbon nanofibers (CNF), rGO with PANI composites [193], and lamellar $K_2Co_3(P_2O_7)_2.2H_2O$ nanocrystal whiskers [194] with tunable geometry and thickness. More examples of the inkjet process are given in Table 3.1.

The main issue with inkjet printing, as with laser scribing, is introducing new equipment in a CMOS processing framework. Clogging of inks in the nozzles and slow throughput are a few disadvantages that inkjet printing faces. This is a recurring issue in 3D printing as the nozzle needs to be cleaned out entirely or replaced after a certain number of cycles. Thus, this process will be fully capable of being introduced in an automated IC fabrication process only after such challenges are addressed.

3.2.4 Electrodeposition

Electroplating or electrophoretic deposition (EPD) are subcategories of the electrodeposition of MSC electrodes. It is a process of depositing ions, molecules or complexes when a substrate is immersed in a solution as shown in the setup schematic in Figure 3.2(d). The characteristic feature of electrophoretic deposition is the immersion of the target substrate in a colloidal solution containing the desired electrode molecules. The molecules or ions in the solution migrate to the current collectors in the presence of an electric field.

Electrodeposition is used for depositing a variety of electrodes for MSCs. Sharma et al. [195] deposited TiO_2 material on carbon nanofibers that results in a high capacitance of 9.4 mW cm^{-2}. Similarly, Li et al. fabricated MSCs using zeolitic imidazolate frameworks (ZIF) molecular organic framework (MOF) molecules showed an energy density of 2.9 mWh·cm^{-2}. The capacitance of the device roughly translates to 18 μF cm^{-2} in a voltage window of 1 V. Electrophoresis has also been used to deposit MnO_x of rGO to yield a capacitance of 1.6 mF cm^{-2} [196]. The process is also applied by Dusane et al. [195] to show 240 μF cm^{-2} capacitance with silicon nanowires decorated with rGO as electrodes for on-chip MSCs. High capacitance with wideband frequency response MSC device was exhibited by Wang et al. [197]. Their group fabricated mesoporous gold electrodes through Au/Ag co-sputtering followed by selective etching of Ag. The mesopores in the current collector surface establish a high-frequency response. Later they deposited MXene quantum dots through electrophoretic deposition with a capacitance yield of 14 mF cm^{-2}. More examples of the EPD process are given in Table 3.1.

There are some advantages of electrodeposition, such as them being lower in cost than other fabrication processes with simple control requirements. The electric field only influences the deposited material, so the process is transferable to any substrate.

Among some notable disadvantages, the EPD process solution is often determined by the material deposited on the substrate surface. The processing conditions, temperatures, and equipment are determined based on the solution. The coating process involves submerging the substrate in a coating bath or solution with a typical voltage of 25 to 400 V DC. Immersion in a solution bath or high potential on the substrate can lead to unwanted reactions between the substrate and solution in typical cases. The evolution of H_2 gas during the coating process is another factor that can be detrimental to on-chip circuitry. Thus, electrodeposition is a feasible technique for post-fabrication integration of devices; however, from FEOL or BEOL processing, it will require further extensive investigation on the impact of electrodeposition of new materials.

3.2.5 Laser scribing

Laser scribing is a method to develop MSCs in a simple, cost-effective, and scalable way. Its concept is to irradiate graphite oxide with a laser beam to convert it into graphene through a photothermal effect. This reduction ability makes it feasible for direct patterning of electrodes on any form of substrates. It is also possible to fabricate both planar and stacked MSCs through this process.

In some cases, direct laser reduction of GO to graphene sheets can be performed by a LightScribe Digital Video Disc (DVD) optical drive [198, 199, 200]. The films that were produced were mechanically robust. They also showed a high electrical conductivity. The authors claimed that these films could be used directly on a substrate without requiring binders or current collectors. These electrodes were fabricated on flexible substrates such as nitrocellulose membrane, photocopy paper, or conductive Al foil. The devices confirmed a high power density and excellent cyclic stability. Later, Wen et al. [148] improved the performance of laser scribed graphene (LSG) by combining it with coated layers of GO/CNTs hybrid powders on flexible PET sheets. In the presence of CNTs with a smaller diameter, the laser-scribed CNT combination of electrodes yields better electrochemical performance. These devices were integrated with solar cells to demonstrate the feasibility of using MSCs as energy storage units for an on-chip power supply [201].

Laser scribing is a process that can be integrated into CMOS compatible machinery but despite its excellent electrochemical performance, this process is also severely restricted to materials that can be reduced by laser irradiation. Moreover, the thermal effects on the substrate lead to remarkably high parasitic resistance, which can lead to very high leakage currents. Despite the disadvantages, the simplicity, reproducible nature, and substrate independence of laser scribing make it a perfect candidate for flexible and wearable electronics where pre-existing irreplaceable technologies do not severally constrain the throughput and use of equipment.

3.2.6 Electrode conversion

Electrode conversion is another fabrication technique compatible with processing technologies used for on-chip integration of sensors and actuators. In this process, the electrode material is either deposited on the substrate in the form of a photoresist,

template, or a precursor, which is later converted to an EDLC based material that exhibit high conductivity and large specific surface area for the application of storing charge as in Figure 3.2(e). This process is also categorized as carbon MEMS or CMEMS based on the one-step lithography process and one step photoresist pyrolysis to carbon-based electrodes. Several articles in the literature have used pyrolysis of polymeric photoresists at over 700 °C to manufacture MSCs. The polymeric photoresist chains break at high temperatures, and the impurities in the carbon structure are removed from the chemical composition through products of the chemical reaction with the high-temperature annealing gas such as N_2 or H_2. The process is like the standard lithography process beginning with evaporation and lift-off of current collector electrodes. This step is followed by forming desired patterns on the spin-coated photoresist through UV-lithography or laser writing. Once the photoresist is developed and etched at exposed or unexposed areas on the substrate based on their chemical nature, it is pyrolyzed, giving rise to carbon-based electrodes suitable for energy storage. The photoresist can be thick through the application of different photoresists, such as AZ4562, which can demonstrate a thickness of 8 μm when spun on a silicon substrate at 2000 rpm with an acceleration of 2000 rpm s^{-1}. The photoresist can also be mixed with different materials such as MnO_2 or CNTs to improve the energy and power density of the device.

While electrode conversion or CMEMS is a highly fascinating one-step process that can show very high energy and power densities, the pyrolysis step of the MSC fabrication is a deterring aspect to the integration of this technology in semiconductor fabrication. Application of temperatures above 350 °C is detrimental to the metallic layers in CMOS circuits as the metals start melting and diffusing in the substrates that can lead to severe device breakdown consequences such as electromigration, dielectric breakdown, short-circuiting, and high package failure.

Among these different techniques, only spin-coating and CVD emerge as fabrication processes that are utilizable in the near-immediate future to fabricate on-chip MSCs for integration with ICs and MEMS energy harvesting devices. An in-depth analysis of on-chip MSCs with electrodes grown through the CVD process is explained in Paper 3. In Paper 2 we analyze the photolithographic MSCs developed at our group through advancing the spin coating technology for electrode deposition. In Paper 4, we compare the two fabrication methodologies. Finally, in Paper 5, we use the optimized spin coating method in Paper 2 to stack several rGO composites to improve the areal capacitance and energy density of the spin-coated MSCs. In the following sections, we will highlight the significant findings from these reports.

3.3 Impact of electrode geometry

While several fabrication processes can be used to manufacture planar MSCs, it is essential to understand the role of electrode geometry and thickness in terms of the device's electrochemical performance. This section will discuss the impact electrode geometry of current collectors on the capacitance, energy, power, and resistance of the MSCs through fabrication and evaluation of CVD grown CNFs on Au/Ti contacts. We shall also examine the role of electrode thickness on the total capacitance of power delivering capacity of the MSCs, followed by a short discussion on total capacitance as

Table 3.1: Summary of most recent MSCs reported through different fabrication methodologies. The reported maximum capacitance, energy and power density are based on voltage sweeps and current densities that demonstrate the highest values.

Fabrication	Material	Capacitance	Energy density	Power density	Ref.
CVD	CNT/MnO_x	37 mF cm^{-2}	0.3 μWh cm^{-2}	81.8 mW cm^{-2}	[202]
CVD	PANI/G/SiNW	85 mF cm^{-2}	11.9 μWh cm^{-2}	0.78 mW cm^{-2}	[183]
CVD	Armchair GNR	100 F cm^{-3}	1 mWh cm^{-3}	1000 W cm^{-3}	[203]
CVD	3D-Si/C/MnO_2	223 mF cm^{-2}	5 μWh cm^{-2}	117 μW cm^{-2}	[204]
CVD	VACNT/TiO_2/TiN	5.18 mF cm^{-2}	2.5 mJ cm^{-2}	1.4 mW cm^{-2}	[182]
CVD	Graphene film	66 μF cm^{-2}	-	-	[180]
CVD	G/SiC/SiNWs	3.2 mF cm^{-2}	-	-	[181]
CVD	G/$Ni(OH)_2$/NiOOH	0.75 mF cm^{-2}	1.04 mWh cm^{-3}	54 mW cm^{-3}	[205]
CVD	G/SiNW/PANI	185 mF cm^{-2}	-	-	[184]
CVD	Graphene	30 μF cm^{-2}	34.48 mWh cm^{-3}	2.21 W cm^{-3}	[206]
Electrodeposition	TiO_2/NF	9.4 mF cm^{-2}	0.64 μWh cm^{-2}	307.2 μW cm^{-2}	[195]
Electrodeposition	ZIF-8	-	2.87 mWh cm^{-2}	687 mW cm^{-3}	[207]
Electrodeposition	SiNW with MnO_2	2.1 mF cm^{-2}	0.12mJ cm^{-2}	0.14 mW cm^{-2}	[208]
Electrodeposition	Nanoporous gold with nanocarbon onions	1.16 mF cm^{-2}	0.16 μWh cm^{-2}	29.87 μW cm^{-2}	[209]
Electrodeposition	rGO/MnO_x	1.6 mF cm^{-2}	1.02 mWh cm^{-3}	3.44 W cm^{-3}	[196]
Electrodeposition	rGO/SiNW	240 μF cm^{-2}	-	-	[210]
Electrodeposition	-	1.8 mF cm^{-2}	0.8mJ cm^{-2}	1.28 W cm^{-2}	[211]
Electrodeposition	Mesoporous gold	2 mF cm^{-2}	-	-	[212]
Focussed ion beam	rGO	472 μF cm^{-2}	1.1 mWh cm^{-3}	21.4 F cm^{-3}	[213]
Inkjet	PEDOT:PSS/GQD	2 mF cm^{-2}	0.39 μWh cm^{-2}	0.7 mW cm^{-2}	[71]
Inkjet	$Ti_3C_2T_x$	754 F cm^{-3}	9.4 mWh cm^{-3}	150 mW cm^{-3}	[214]
Inkjet	Pyrolysed carbon	3.9 mF cm^{-2}	0.9 mWh cm^{-3}	0.4 W cm^{-3}	[215]
Inkjet	Fe_2O_3/MnO_2/ G	0.8 mF cm^{-2}	39 mWh cm^{-3}	259 mW cm^{-3}	[216]
Inkjet	Graphene	313 μF cm^{-2}	-	4 mW cm^{-3}	[217]
Inkjet	rGO/Bi_2O_3	-	13.28 mWh cm^{-2}	4.5 W cm^{-3}	[218]
Inkjet	rGO	441 μF cm^{-2}	-	-	[219]
Inkjet	rGO	99 μF cm^{-2}	-	-	[220]
Laser scribing	CNT/MnO_2	10 mF cm^{-2}	6.83 mWh cm^{-3}	154.3 mW cm^{-3}	[221]
Laser scribing	Lignin/Graphene	25 mF cm^{-2}	1 mWh cm^{-3}	2 W cm^{-3}	[222]
Laser scribing	Nitrogen doped graphene/MnO_2	13 mF cm^{-2}	4 μWh cm^{-2}	1 mW cm^{-2}	[223]
Laser scribing	Benzene bridged PPY	0.95 mF cm^{-2}	50.7 mWh cm^{-3}	9.6 kW cm^{-3}	[224]
Laser scribing	GO-Zn	3.9 F cm^{-3}	0.43 mWh cm^{-3}	0.40 W cm^{-3}	[225]
Laser scribing	GO-CNT-AC	10 mF cm^{-2}	2 μWh cm^{-3}	0.2 mW cm^{-2}	[226]
Laser scribing	Graphene/flourinated polyimides	110 mF cm^{-2}	0.01 mWh cm^{-2}	0.58 mW cm^{-2}	[227]
Laser scribing	B/N enriched polymers	20.9 F cm^{-3}	2.9 mWh cm^{-3}	1461 W cm^{-3}	[228]
Laser scribing	MOF-199/ZIF-67	8.1 mF cm^{-2}	1 μWh cm^{-2}	10 mW cm^{-2}	[229]
Laser scribing	Graphene/MoO_2	81 mF cm^{-2}	113.7 μWh cm^{-2}	2.5 mW cm^{-2}	[230]
Laser scribing	V_8C_7/rGO	49.5 mF cm^{-2}	3.4 mWh cm^{-2}	0.4 W cm^{-3}	[231]
Laser scribing	Sulphur doped G	55.4 mF cm^{-2}	4.93 μWh cm^{-2}	-	[232]
Laser scribing	G-Co doped	110 mF cm^{-2}	9.79 μWh cm^{-2}	-	[233]
Laser-scribing	Co/rGO	2.27 F cm^{-3}	1.06 mWh cm^{-3}	0.97 W cm^{-3}	[234]
Spin coating	Sulphur-doped G	80 μF cm^{-2}	-	0.7 mW cm^{-2}	[235]
Spin coating	Graphene	2 μF cm^{-2}	89.5 mF cm^{-2}	17.9 W cm^{-3}	[68]
Spin coating	MoS_2/rGO/PR	13.7 mF cm^{-2}	1.9 μWh cm^{-2}	1 mW cm^{-2}	[236]
Spin coating	Horizontal array CNT	0.22 mF cm^{-2}	54 mWh cm^{-3}	44.7 W cm^{-3}	[191]
Treating-cutting-coating	$Ti_3C_2T_x$	0.7 mF cm^{-2}	4 μWh cm^{-2}	0.015 mW cm^{-2}	[237]

a function of total active electrode area. For a more in-depth analysis of the geometry and thickness for different materials, the reader is referred to Paper 3 and article by Li et al. [238].

Previous studies conducted for understanding the influence of geometry on electrochemical performance analyzed pseudocapacitive materials such as MnO_2, PANI, layer-by-layer assembled rGO, and multiwalled CNTs. The results establish an increase in power density by increasing the number of fingers. However, effects on device resistance, capacitance, and cut-off frequency were under-reported. Similarly, the effect of electrode thickness on the areal and volumetric capacitance of MSCs was also not adequately analyzed. In Paper 3, we discussed the impact of electrode geometry based on interdigitated planar fingers on the device capacitance, R_{esr}, power density, and device cut-off frequency. Multiple MSCs with one finger (1F), five fingers (5F), ten fingers (10F) and twenty fingers (20F), all with fixed device lengths (4.7 mm) are fabricated.

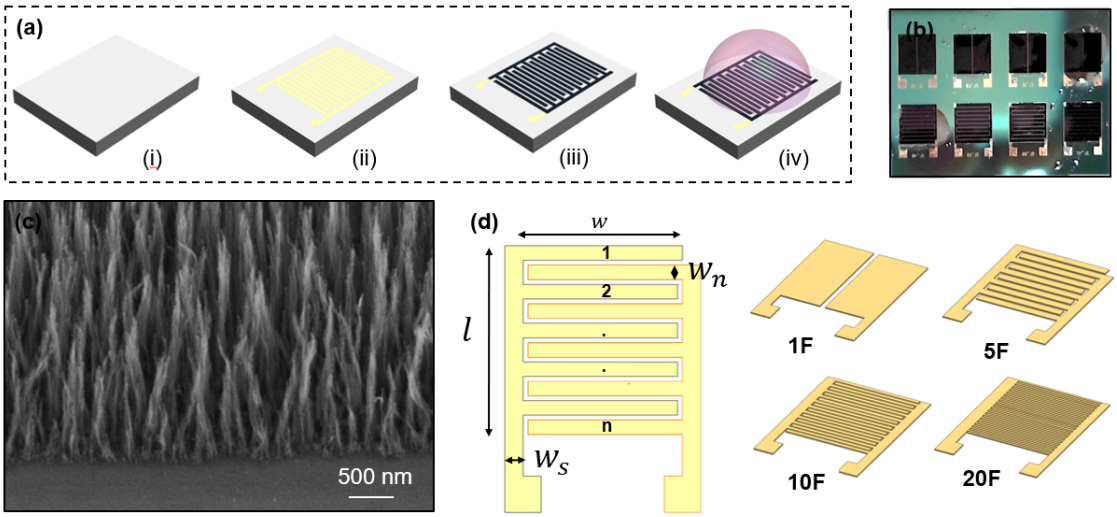


Figure 3.3: (a) CVD fabrication of MSCs: (i) substrate cleaning, (ii) current collector and catalyst lift-off, (iii) CNF growth, (iv) electrolyte deposition. (b) Optical micrograph of the fabricated MSC structures. (c) Growth of CNF visible in SEM optical micrography. Image acquired after permission from Saleem et al. [239]. (d) Schematic illustration of the top view of MSC cell and isometric view of the MSCs with different finger geometries. The dimension of the devices are shown in Table 3.2.

Figure 3.3(d) shows the different schematics of the MSCs evaluated. The dimensions of the tested devices are shown in Table 3.2. The article also analyses the trade-off of increasing electrode thickness by evaluating CNFs grown at various lengths of 3 μm, 5 μm, 8 μm and 14 μm on Pd current collectors.

The fabrication process for CVD growth of MSCs on Pd/Ti current collectors is shown in Figure 3.3(a). The process starts with cleaning a standard silicon wafer and then growing a 400 nm SiO_2 insulating layer on the surface through thermal oxidation at 1050 °C for 4 hours. The Pd/Ti current collectors of 100/20 nm respectively are evaporated using an e-beam evaporator on the developed photoresist patterns. The photoresist is then lifted off, and a catalyst layer is deposited using the same process. The CNF is grown on the catalyst using Black Magic Aixtron at 390 °C and 550 °C in the presence of acetylene and hydrogen gas. The fabricated devices on a Si/SiO_2 chip are shown in Figure 3.3(b). The electrolyte EMIM-TFSI poured on top of electrodes is also visible in the image. The CNF growth through the CVD process can be seen in Figure 3.3(c), which shows the scanning electron micrograph of the grown electrodes.

Table 3.2: Dimensions of various finger geometries with 40 μm interspacing for MSC fabricated through CVD process

Device/Dimension	Area (cm^{-2})	Finger length (μm)	Finger width (μm)
1F	0.21	2200	4750
5F	0.20	4180	440
10F	0.15	4180	200
20F	0.14	4180	80

A summary of electrochemical results for the fabricated and tested CNF-MSCs can be seen in Figure 3.4. The Radar plot summary of the MSCs with different finger geometries is shown in Figure 3.4(a). The MSC with the maximum quadrilateral area is the best performing device, 10F-MSC. The 5F-MSC surprisingly shows the highest volumetric capacitance among all the fabricated MSCs despite the expectation of a constant C_V for the devices. As expected, the power density and cut-off frequency of the 20F device is the highest, while the 10F-MSC shows the highest conductance. Intuitive to the finger geometry, the 1F-MSC demonstrates the highest resistance, R_{esr} (mentioned R_D in the article) among the devices with the lowest cut-off frequency and least power density due to a poor phase response in the electrode geometry. It was expected that the 1F-MSC would exhibit the highest capacitance, based on the results by Li et al. [238], based on the total active material. However, the Radar plot in Figure 3.4(a) results indicate a lower CNF growth in 1F devices compared to the other interdigitated geometries. This can be due to the high surface area of condensation for the carbon gas on the catalysts at the edges of the interdigitated structure. An in-depth comparison of the areal capacitance of the 1F- and 5F-MSC is shown in Figure 3.4(b). Both the devices follow a similar scaling trend over a range of current density inputs. Thus, based on the necessity of the intended application, the number of fingers can be tuned to give priority to conductivity, power density, or cut-off frequency for the CVD fabricated MSCs.

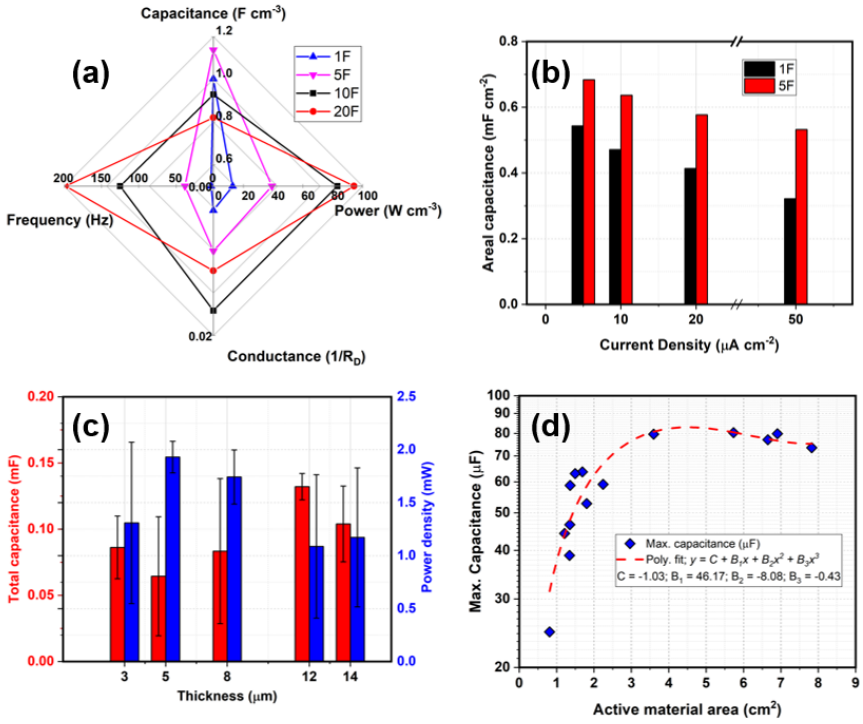


Figure 3.4: Evaluation of the impact of electrode geometry and thickness on the electrochemical performance of CVD grown CNF MSCs: (a) Radar plot of MSCs with varying finger geometry, (b) Comparison of areal capacitance between the 1F and 5F geometry, (c) Impact of electrode thickness on the total capacitance, (d) Capacitance scaling over total CNF active area.

The total device capacitance of electrodes with different thicknesses alongside their exhibited maximum power density evaluated from the EIS spectrum is shown in Figure 3.4(c). As visible, the total capacitance of the device with 12 μm thick electrodes reach a maximum capacitance of 0.14 mF, which is larger than the capacitance of 14 μm thick electrodes. The non-intuitive result can be attributed to poor electrolyte penetration in electrodes with higher thicknesses. The theory is further evaluated in Figure 3.4(d), where the maximum capacitance is plotted against the total active material area. The active material area is calculated by counting the number of CNF strands present in a given area in Figure 3.3(c) and then calculating the circumferential surface area of the nanofibers by using $A = \pi r^2 l$ where r is the radius of the CNF, and l is the length. It is evident from the trend that the electrolyte penetration in the CNF fibers initially increases at first until 4 cm^2 where it starts saturating at 80 μF. The impact of electrode thickness is evaluated for the CNF grown devices by an in-depth analysis of cut-off frequencies and R_{esr} (or R_D) in Paper 3.

3.4 Spin coating technology for microsupercapacitors

Application of spin coating for deposition of electrode inks for MSC fabrication can remove the necessity of using advanced machines for electrode deposition. Several works in the literature have focused on developing graphene-based MSCs. Since the properties of graphene can be tuned to various functionalities through relatively easy doping [240], it is highly sought to develop a wafer-scale fabrication process that can manufacture several graphene-based MSCs in a single batch of processing. The following sections examine the fabrication process developed by Smith et al. [76], the electrochemical performance of MSCs and then challenges in wafer-scale fabrication. The fabrication process is also transferable to different electrode materials such as vertically aligned carbon nanosheets (VACNS) grown in CVD chamber as discussed more in-depth in our previous publication [241].

3.4.1 Fabrication

The developed spin coating process is a top down process that uses two masks for MSC fabrication. The schematic of the fabrication process is shown in Figure 3.5. The first mask is applied for the current collector layer fabrication and the second mask is used to develop electrodes over the current collectors. The steps for fabrication are outlined below:

- A 2" Si wafer is used as a substrate (Figure 3.5(a)). Its surface is oxidized to SiO_2 in the oxidation furnace Centrotherm at 1050 °C for 45 min. (Figure 3.5(b)).
- Gold and titanium (Au/Ti) current collectors are deposited using the lift-off technique. This is a clean process that does not involve a substrate being subjected to highly reactive chemical etchants. Generally, the process employs a resist with a higher process thickness than the desired metal thickness. This allows for the metal layer to break off the resist wall during an evaporation procedure. The

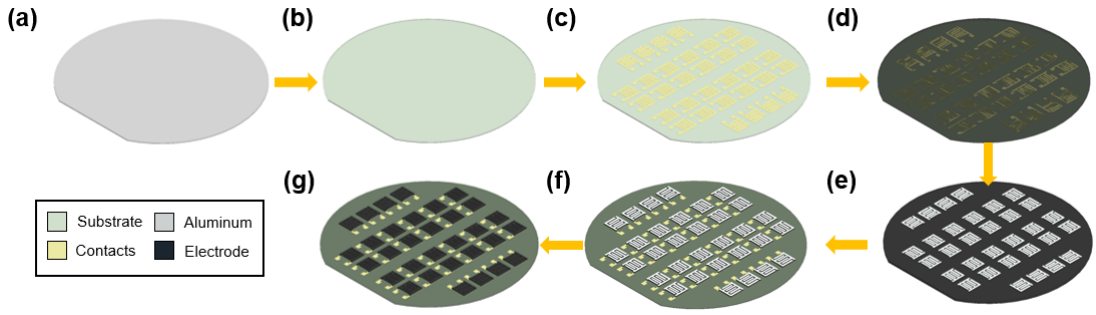


Figure 3.5: Schematic fabrication process of the spin coating process followed for manufacturing MSCs on a wafer scale.

resist is then developed, and the freestanding metal layer on top is lifted off. Thus, S1813 lift-off resist with a thickness of 1.3 μm is spin-coated for 60 s at 4000 pm with 2000 rpm/s acceleration. After soft baking for 5 min at 180 °C, the resist is exposed in the mask aligner using a contact layer photomask. When the wafer is in hard contact with the photomask with a helium cushioning of 20 μm, UV light is radiated on the setup. The light breaks the polymer linkages of the exposed positive resist, which is then developed in MF319 developer for 60 s and transferred to the water. A post bake for 1 min at 120 °C is essential for resist hardening. Once the pattern is ready, Au/Ti (100 nm/10 nm) metal layers are evaporated onto the substrate in Lesker Physical vapor deposition (PVD). PVD is a process in which the bombardment of electrons heats a metal in condensed form in an ultra vacuum chamber. The vapor phase produced by the e-gun travels in a vertical electric field toward the target wafer where it reverts to a condensed phase as a thin film. After the deposition of Au/Ti layers, the lift-off process is completed by submerging the wafer into mrREM 400 bath while being ultrasonically treated for 55 min. Although gold is used for proof of concept, it can be replaced with CMOS compatible metals such as Pt, Pd, or Mo. (Figure 3.5(c))

- Electrode deposition through spin coating and CVD growth

  1. The GO solution used for spin coating was purchased from Graphene Supermarket. The solution was diluted in DI-water to 3g/l and then sonicated for 15 min at 80 °C in 35 kHz sonication. The sonication before spin-coating dissociated the graphene platelets from stacking and aggregation. Next, GO is spin-coated five times on the substrate. Each iteration comprises of pouring the GO solution on more than four-fifths of the wafer, spinning it for 60 s at 1000 rpm with 1000 rpms acceleration and soft baking it at 100 °C after every spin. Post-spin-coating, the wafer is baked at 100 °C overnight to remove the water concentration from the coated films. (Figure 3.5(d))
  2. VACNS were grown on the prepared substrates in a cold-wall low-pressure PECVD reactor (Black Magic, Aixtron). The ordinary recipe is that the substrate was heated to 775 °C with the ramp rate of 300 °C min and annealed for 1 min with the mixing of 20 sccm H_2 gas and 1000 sccm Ar gas flow. The

plasma was then turned on with a DC bias with the power of 75 W. The plasma voltage is 800 V with the current limit of 0.5 A. The actual growth was initiated by introducing acetylene gas (C_2H_2) which was maintained for 10 min. After the growth, the system was evacuated to be at less than 0.2 mbar and cooled down to room temperature. Growth time and C_2H_2 flow rate used in this process can be changed to control the size of VACNS.

- An Al hard mask is fabricated on the solvent-free GO surface. This enables etching of carbon material in areas outside the interdigitated pattern. A thin film of Al, 70 nm, is evaporated on the substrate. S1813 resist is spin-coated on it for 60 s at 4000 rpm with 2000 rpm/s acceleration. It is soft baked for 2 min and dried overnight at 110 °C. The Al film area which is not covered by the resist is dry-etched in Oxford Plasmalab using a standard recipe mixture of Cl_2 and $SiCl_4$ in the presence of Ar. When Cl_2 reacts with Al, it produces $AlCl_3$ that is volatile enough to get removed during the gas exchange in the plasma chamber. $SiCl_4$ is generally used to protect the Al layer from an undercut. (Figure 3.5(e))

- With the hard mask on top, GO is dry-etched in Plasmatherm using O_2 plasma at 100 W in a 100 mTorr pressure chamber for 4 h, shown in Figure 3.5(f). During this step, the resist on top of Al hard mask is also ashed away. Once the GO is completely etched from uncovered areas, Al is completely etched away using the dry etch recipe discussed in the previous step. Figure 3.5(g) shows the result after the final fabrication step.

- This step is required only for GO electrodes. The reduction of GO to rGO can be performed chemically or thermally. In this work, we have used thermal annealing of GO substrates for the material reduction. Conductivity and surface area are highest for GO solutions annealed at 500 °C [242]. The annealing process commences at 150 °C, ramping up every minute by 10 °C until 500 °C. The temperature is held for 5 min at that instance and then ramped down 10 °C/min till the substrate is cooled down to room temperature. The Raman micrographs for the rGO can be seen in the manuscript by Smith et al. [76].

3.4.2 Results

The results for MSCs fabricated by deposition of electrodes through spin-coated rGO and CVD grown VACNS followed by photolithographic etching in the presence of KOH and H_2SO_4/poly(vinyl alcohol) (PVA) respectively are shown in Figure 3.6. The cyclic voltammogram of rGO-MSC show an areal capacitance of 0.2 mF cm^{-2} over a 0.8 V voltage window. The galvanostatic charge discharge measurements in Figure 3.6(b) show that the MSC can be charged and discharged at current densities ranging from 10 μA to 50 μA without significant voltage drop due to R_{esr} during the current polarity switch.

The cyclic voltammograms of VACNS-MSC on Au/Ti and Pd/Ti current collectors is shown in Figure 3.6(c-d) respectively. Integrating the area under the current curves for both the voltammograms we acquire the capacitances of Au/Ti-VACNS-MSC and

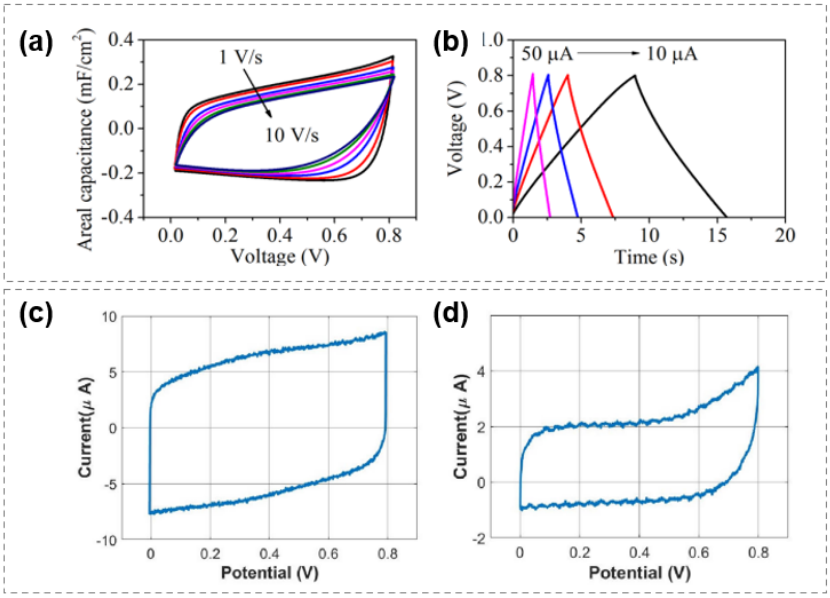


Figure 3.6: Electrochemical performance of rGO and VACNS based MSCs (a) Cyclic voltammograms of rGO-MSCs for various scan rates. (b) GCD evaluation of rGO-MSCs. Cyclic voltammogram of VACNS-MSCs fabricated on (c) Au/Ti, (d) Pd/Ti current collectors.

Pd/Ti/VACNS MSC as 5.5 μF cm^{-2} and 1.3 μF cm^{-2}. The total energy density of the two devices is calculated at 1.76 μJ cm^{-2} and 0.42 μJ cm^{-2}. The VACNS exhibit a relativity low capacitance compared to the rGO MSCs. However, the growth of VACNS across the substrate is uniform but the CVD process does not lead to uniform properties while occurring on a 2" Si/SiO_2 wafer. The results indicated that there is a non-uniform temperature gradient in the growth chamber which leads to uneven electrode heights. In some cases, the MSCs were found to be highly resistive. These results could be easily mitigated when the growth was performed on individual chips of 1 cm^2 area. Thus, as of now, we cannot consider the CVD of CNFs and VACNS a viable option of CMOS compatible process.

3.4.3 Issues in fabrication

Although the fabrication process is reproducible, there were several issues that still existed in the process that are required to be mitigated to yield a high number a functional devices on a single substrate. Figure 3.7 shows the different issues that existed in the described process plan.

Poor deposition

Uniform spin coating of rGO based inks on the silicon substrate is perhaps the most challenging aspect of fabricating several MSCs on a substrate. Figure 3.7(a) shows the optical micrograph of an entirely fabricated MSC using rGO in dimethylfluoride solution. The issue is due to the smooth SiO_2 surface on the silicon substrate. As the graphene

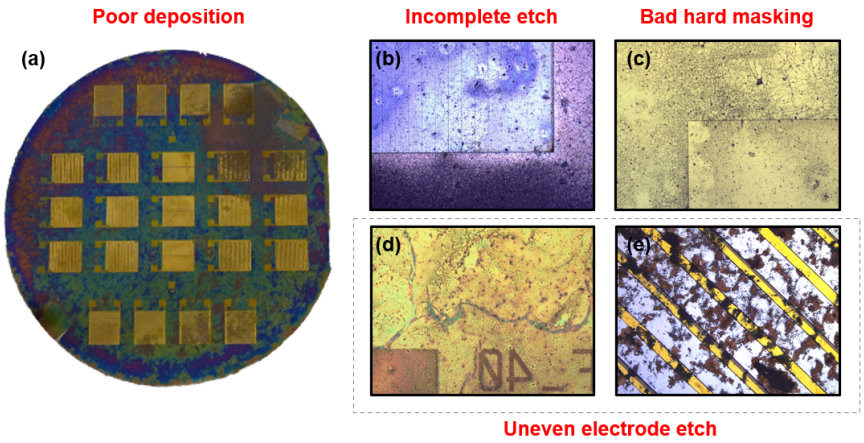


Figure 3.7: (a) Optical micrograph of the MSCs fabricated through spin coating on Si/SiO_2 substrate. (b) Incomplete etching of the electrode material post Al hard mask etching, (c) Uneven hard mask thickness across the Si wafer due to poor uniformity in thickness. (d) Uneven rGO etch after 8 hours of etching in O_2 plasma. (e) Short-circuiting among interdigitated electrodes due to uneven electrode etching.

flakes are large than 1 nm, the surface roughness of 0.71 nm is not enough to act as anchors to the deposited material. The electrode ink randomly tends to agglomerate across the substrate after the spin coating process. Such an electrode layer does not exhibit sufficient uniformity or coverage on the wafer surface. Moreover, during the subsequent processing steps that involved photolithography and development, the electrode material tends to dissociate itself from the current collectors, thus lacking sufficient adhesion to sustain the fabrication process conditions such as immersion in aqueous solutions sonication and etching in low-pressure chambers.

Bad hard masking

The poor uniformity and coverage of the spin-coated rGO ink directly led to problematic Al deposition on the electrode. The electrode thickness differed by over 70 nm across 1 mm of the surface. Since the optimum thickness supported by the GO layers was 70 nm of Al, several cracks developed across the surface. Thus, it is essential to deposit a thicker hard mask for etching electrodes. When the photoresist is spin-coated on the Al surface, it seeps through the cracks developed in the layers. During the soft baking and lithography steps, the photoresist polymers act as independent lift-off areas and get removed during the development process. This often leads to aluminum flaking in the solution. Some failed devices due to insufficient hard masking are shown in Figure 3.7(b-c).

Incomplete etch

Later, when the Al hard mask is applied for plasma etching of GO, the unwanted exposed and unexposed areas lead to device failure by revealing extremely low capacitance or short-circuiting. In the worst cases, a significant section of the substrate is not applicable. Also, the poor uniformity of GO leads to the same effect on the Al layer, which later

transfers it to the photoresist layer. Furthermore, when the substrate is immersed in a developer solution, the GO material gets dissociated from the current collector surface and gets redeposited on the substrate surface. Subsequently, in the soft baking step, when the water content is evaporated from the GO/Al/photoresist stack. The bubbling of the photoresist with water can sometimes lead to a failed batch of processing. However, such failures in the processing are less frequent and are not commonly known across cleanroom users as the processing of 2D materials has started to take shape over a few recent years only. An example of a bad photoresist Al patch on the device can be seen in Figure 3.7(d). Figure 3.7(e) shows the example of short-circuiting in a device on the wafer. Thus, there was an urgent need for optimization in the process plan, which would provide a higher yield standard in a CMOS process. We shall discuss the optimization of the spin coating process in the next section.

3.5 Improving electrode deposition and device performance

After the review on the first version of spin-coated MSCs, there was an urgent need to improve the electrode inks' adhesion, uniformity, and coverage. The fabrication group followed a factorial design of experiments for improving the adhesion of rGO on the substrate by increasing the surface roughness through argon plasma embedding, applying Fe nanoparticles, applying an adhesion layer such as hexamethyldisulfide (HMDS) polymer, and annealing. In the following sections, we will discuss the summary of the fabrication results from experiments with improving surface roughening through annealing of a thin Fe layer for increased uniformity, thickness, coverage, and adhesion of the rGO ink to the silicon substrate. The impact of surface roughening on a silicon substrate is initially examined based on these parameters. Later, a section is dedicated to comparing MSCs fabricated after surface roughening with the ones on non-roughened substrates. The results of the experiments are explained more in detail in Vyas et al. [75] and Paper 2.

The surface roughened devices are then compared with the CNF-MSCs with the exact dimensions (20F) in the following section based on Paper 4. The processes are categorized for their trade-offs of fabrication ease, energy density, power density, and rate capability. We will examine the fabrication of different graphene-based composites using the optimized spin coating fabrication process and analyze numerous devices based on their volumetric capacitance. The fabrication process will be analyzed for its wafer yield. Finally, we will discuss the experiments with stacking different materials through the spin coating to enhance the areal energy density of MSCs in the section based on Paper 5.

3.5.1 Enhanced spin coating

Following the optimizations examined in our report [75] and Paper 2, the spin coating of 3 g/l GO ink is performed on a thin layer of Fe nanoparticles annealed at 500 °C. For the GO-ink to be coated uniformly on a substrate, we investigated the surface's wettability when it comes in contact with the GO-ink. The effect of surface structure on liquid wettability was established by Wenzel and Baxter [243]. They verified that

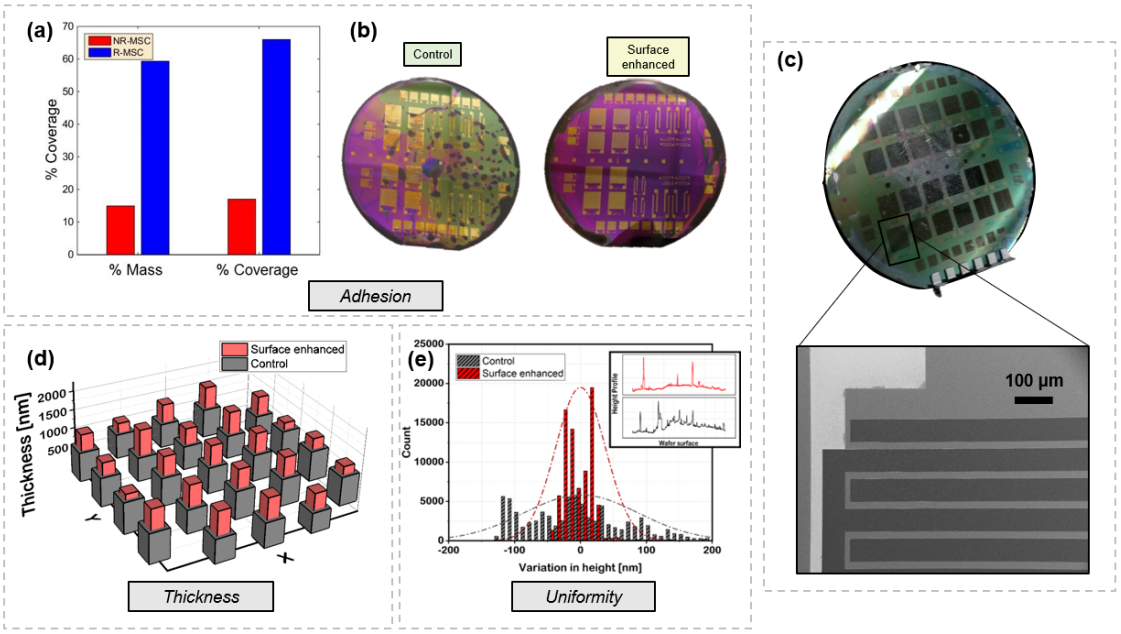


Figure 3.8: (a) Improvement in adhesion of rGO after application of surface roughening through Fe nanoparticles, (b) Optical micrographs of the spin-coated rGO on non roughened and roughed substrate. (c) Camera captured image of the fabricated MSC wafer after all processing steps, inset shows the scanning electron micrograph of the intedigitated electrode structure. (d) Improvements in thickness of electrodes after surface roughening. (e) Increased uniformity displayed in the histogram analysis of the thicknesses measured through surface profiler.

increasing the surface roughness of a surface leads to increased wettability. Hsieh et al. [244] also established an increased coverage of oil like surfaces for surfaces with high roughness. Si and Au nanoparticles have been used recently to increase surface roughness. Si etching can be performed in fluorine-based plasma recipes, while the Al etching occurs in a chlorine plasma environment. Application of Si nanoparticles as surface roughening agents leads to challenges in the etching of nanoparticles in the later stages of fabrication. After etching the Al layer in the final step, if we require another reactive ion etching process, there is a risk of electrode etching during the same process step. Thus, we required a metal layer compatible with the etching of Al while also being unreactive during the device characterization in an aqueous, ionic, or gel electrolyte environment. Conversely, for Au nanoparticles, the etching recipes for Au require wet etching in aqua regia solution or a high power argon bombardment plasma process, which are detrimental to the device yield.

The thin Fe (4 nm) layer was evaporated on the Si/SiO_2 surface. The substrate was then annealed at 500 °C for 5 min. The temperature of the furnace increases the kinetic energy in the Fe surface molecules, which leads to nanoparticles coalescing. This results in an increase in the surface roughness of the substrate. The surface roughness of Au/Ti metals on SiO_2 is 0.71 nm, while Au/Ti on Fe nanoparticles gives a roughness of 1.4 nm.

The improved surface roughness through Fe nanoparticles can be seen in Figure 3.8(a). The total mass coverage on the rough MSCs (Control) is more than 50 % higher than the non roughened MSC (Surface-enhanced). Similarly, the total coverage of the

surface-enhanced substrate is higher than that of the control substrate. The improved adhesion can also be optically evaluated in the pictures of the wafers shown in Figure 3.8(b). The control substrate shows the agglomeration of GO-ink, while the surface-enhanced substrate shows a fully covered area with GO. The devices are fabricated based on the fabrication process examined earlier. The uniqueness of Fe nanoparticles is that they do not disrupt the processing steps of MSCs. The Fe layer is etched alongside the Al layer etch step shown in Figure 3.5(f). The substrate after complete processing is shown in Figure 3.8(c). The improvement in thickness due to surface roughening can be seen in Figure 3.8(d). The increase in electrode thickness directly impacts the charge storage capability of the MSCs. The thickness across the wafer surface is also uniform when comparing the electrodes' maximum thickness in a 1 μm^2 area. The results of the comparison are shown in Figure 3.8(e). The inset shows the rGO thickness across one interdigitated finger. Thus, using a nanoparticle layer increases the surface roughness of a silicon substrate, leading to increased adhesion, thickness, uniformity, and coverage of the GO-ink, which leads to improved performance in the Control-MSCs compared to Surface-enhanced-MSCs.

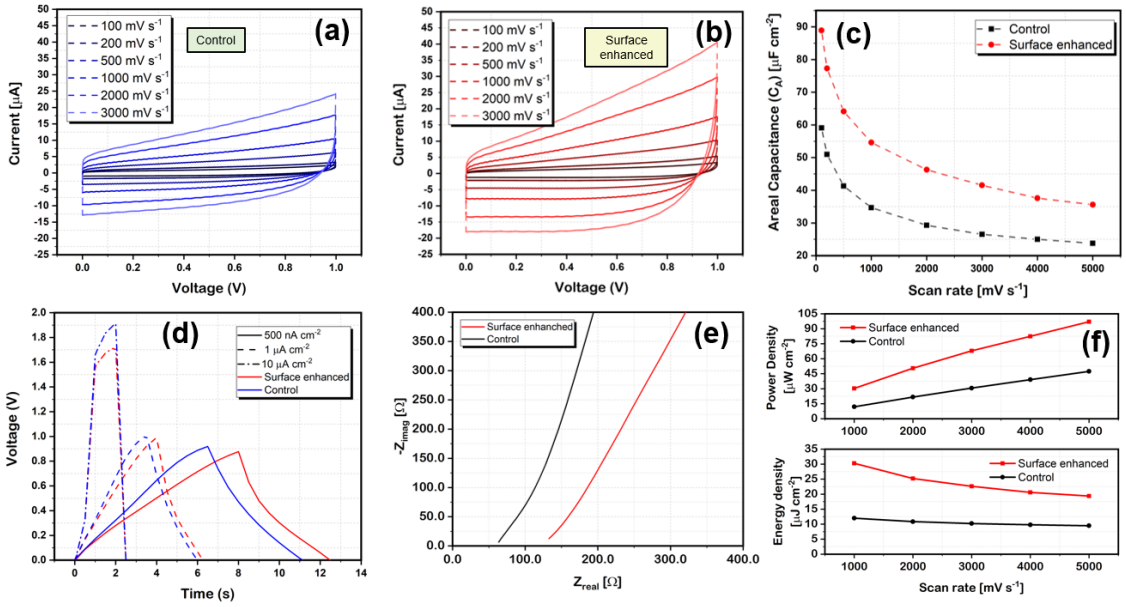


Figure 3.9: Electrochemical performance of the control and Surface-enhanced MSCs. (a) Cyclic voltammograms of the control MSC, (b) Surface-enhanced MSC. (c) Comparison of areal capacitance for the two MSCs fabricated, (d) GCD curves for control and Surface-enhanced MSC at different current densities, (e) Nyquist spectrum comparison. (f) Delineation of energy and power densities of the fabricated Surface-enhanced and Control-MSCs at different scan rates.

The results of their electrochemical evaluation are displayed in Figure 3.9. The cyclic voltammograms of the Surface-enhanced-MSC and Control-MSC show that the MSC fabricated on the surface roughened surface has a higher capacitance, as can be seen in Figure 3.9(a-b). Analyzing the cyclic voltammograms of the R- and Surface-enhaced-MSC, we see that the parasitic resistance extracted from the slope of the CV curve for Control-MSC is higher. This is a negative consequence of the surface roughness. Also, the contact resistance of the current collector increases due to the parasitic reaction

between the Fe nanoparticles and the electrolyte, EMIM-TFSI in this case. The rate capability of the R- and Surface-enhanced-MSCs can be evaluated from the change in areal capacitance of the device over a range of scan rates. Rate capability was measured by the high scan rate capacitance ratio to low scan rate capacitance. The maximum areal capacitance of the rGO-MSCs in Surface-enhanced-MSC was 58 μF cm^{-2} and 90 μF cm^{-2} for the Control-MSC in an ionic liquid electrolyte. These results are state of the art performances in spin-coated GO-based solid-state MSCs reported in the literature. The Control-MSC shows a 3.3 % lower rate capability than Surface-enhanced-MSC in Figure 3.9(c). The GCD comparison of the MSCs also reveals Control-MSC's higher resistance than Surface-enhanced-MSC in Figure 3.9(d). The charging and discharging of the MSCs is carried out at several current densities. At 500 nA cm^{-2}, the Control-MSC displays a higher R_{esr} calculated from the abrupt voltage drop after switching the current polarity after the charging cycle. The device also shows a high leakage current as it discharges faster than Surface-enhanced-MSC. Similar results are extracted from the other current density trends. The R_{esr} values acquired from the GCD characterization match the series resistance of the devices shown in the Nyquist plot in Figure 3.9(e). The low-frequency behavior of Warburg impedance suggests a higher dimension of porosity for the Control-MSC compared to Surface-enhanced-MSC. Also, the semicircle shown at the onset of the Warburg impedance in Control-MSCs shows a high charge transfer resistance in the device. In-depth analysis of CV, GCD, and EIS spectra are given in Paper 2.

Despite several trade-offs relating to increased serial, leakage, and charge transfer resistance in the Control-MSC, the primary advantage of the optimized fabrication process is the exhibition of high electrode thickness that yields a high capacitance, energy and power density in the electrochemical characterization of the device. The energy and power densities of the MSCs are shown in Figure 3.9(f). The Control-MSC has a high power density of 96 μW cm^{-2} compared to 47 μW cm^{-2} for Surface-enhanced-MSC. Similarly, the Control-MSC also shows a higher energy density than its counterpart. The volumetric capacitance of the MSCs was measured at 0.90 F cm^{-3}, which means that the increase in surface roughness does not lead to deterioration of capacitor performance of the electrode material.

3.5.2 Comparison with CVD

Spin coating and CVD processes are two electrode deposition techniques accessible for the fabrication of MSCs geared towards on-chip integration with MPEHs. This section will illustrate the key advantages of the two processes through comparison in fabrication methodology, rate capability, impedance behavior, and total device capacitance at various charging currents.

Regarding the fabrication methods, electrodes grown through the CVD process require a one-step process, while the spin-coated electrodes need a hard mask needed for the etch step after deposition of its current collectors. The CVD yield across small silicon chips is uniform and demonstrates high controllability. The thickness of the electrodes can reach up to several cms of CNTs, as studied in Rao's report [245]. The spin coating process is still in its maturing stage, in which we have recently shown good

adhesion, uniformity, and coverage for rGO based inks on 2" silicon wafers. The thermal budget of CVD growth is, however, an area of concern as the temperatures in CNF growth can reach up to 390 °C and 550 °C. In the case of spin coating, while the GO is annealed at 500 °C, the utilization of different inks that can be preconditioned as electrodes can negate that factor. The CVD process is at a mature stage where it can yield singular MSC chips that can be used for BEOL integration for on-chip sensor nodes after proper encapsulation. However, due to a non-uniformity in the thermal gradients in Black Magic chambers, the growth of carbon-based materials is not entirely uniform across all the surfaces. This is also an issue deposition for spin-coated electrodes. However, the process can be optimized and repeated several times to achieve further uniformity.

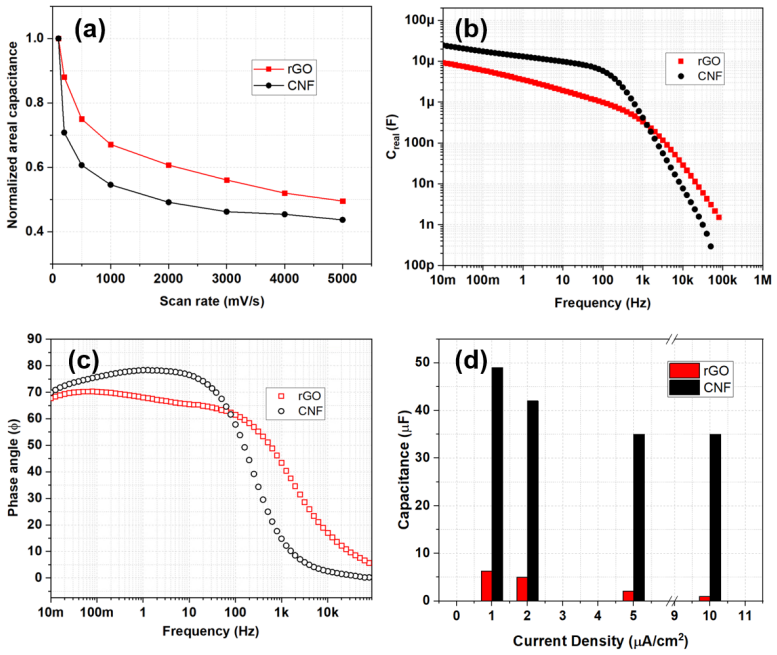


Figure 3.10: Comparison of electrochemical performance of rGO and CNF-MSCs through (a) rate capability over various scan rates, (b) Bode spectrum, (c) phase demonstration, and (d) total capacitance on the chip footprint ready for integration.

The electrochemical performance comparison of the two fabricated devices, rGO-MSC and CNF-MSC, is shown in Figure 3.10. The area of both devices is 0.13 cm^{-2} with 20 interdigitated fingers with the lengths and widths presented in Table 3.2. The CNF-MSC shows an areal capacitance of 270 μF cm^{-2}, approximately more than two times higher than rGO-MSC's 112 μF cm^{-2}. The rGO-MSC shows a higher rate capacity compared to CNF-MSC. This can be related to the interstitial spacing between the rGO flakes compared to fibers in the CNF forests. The small-signal behavior of the MSCs can be seen in Figure 3.10(b), which shows the Bode plot comparison of the devices. The CNF-MSC exhibits a behavior closer towards applicability in ac-line filtering where the frequency response of the reactive component of impedance should be close to 120 Hz while showing a phase close to 90°. The rGO-MSC, in comparison, shows a parasitic resistance in its C_{real} trend even at low frequencies. The phase of rGO-MSC shown in Figure 3.10(c) also exhibits a resistive response as the trends are much lower than the

purely capacitive 90°phase. The total capacitance on the chip footprint is compared in Figure 3.10(d), where we see that the capacitance of 3 μm CNFs is much higher than 1 μm rGO material. Paper 4 entails further discussions on the performance of the two MSCs.

Thus, these results demonstrate that CVD grown CNFs have a significantly better performance than spin-coated rGO. Despite the possibility of fabrication of several devices in a single run, there is an urgent need to improve the energy density of the MSCs if they are to be comparable to the performance of CVD grown MSCs. In the following sections, we will review the applicability of the enhanced spin coating process for a variety of rGO based composites to illustrate the high wafer yield of the fabrication process and find materials that can deliver high enough energy densities in order to be comparable to other electrode deposition standards.

3.6 Improving spin-coated electrode thickness

In this section, we will examine the selected results from Paper 5 which describe the utilization of the enhanced spin coating process to fabricate batches of MSCs using different composites of graphene synthesized for improving deposition of graphene through spin coating.

We have used GO functionalized with functional groups heptadecan-9-amine (HD9A), a branched alkane chain and octadecanamine (ODA), a linear alkane chain synthesized by Mendez et al. [246] to improve the dispersibility of rGO in aqueous inks for spin-coated energy storage electrodes. The alkane chains connect GO and rGO flakes through a covalent bond. The functional group terminates with an amine group for increased Van der waals interactions between the flakes. The spin coating process was conducted for several energy storage materials such as GO, GO-HD9A, rGO-HD9A, rGO-ODA, $MoSe_2$, MoS_2, WS_2, and exfoliated graphene. However, the discussion in this thesis will only be limited to electrochemical performance of the first four materials in the list, namely - GO, GO-HD9A, rGO-HD9A, and rGO-ODA. The devices are fabricated using the processing scheme shown in Figure 3.5 with enhanced surface roughening technique analyzed in Paper 2 except this time using Cr (2 nm) layer as a roughening surface instead of Fe (4 nm).

The effects of surface roughening on spin-coating and performance of individual MSCs, GO, GO-HD9A, rGO-ODA, and rGO-HD9A are shown in Figure 3.11. Figure 3.11(a) outlines the molecular structures of the different materials. The GO layer is a layer of graphene with various oxidation sites, marked as red. GO-HD9A similarly is graphene functionalized with a branched alkane with amine functional group, heptadecane-9-amine and specific binding sites. rGO-ODA is a similar functionalization with a linear alkane group instead of branched with amine ends. rGO-HD9A is pre-reduced GO-HD9A with similar properties as its precursor. The effects of surface roughening on the electrode solutions can be observed in Figure 3.11(b-c), more specifically for functionalized GO solutions where we see an extremely high change in surface coverage compared to non-roughened substrates. The volumetric capacitance of various devices fabricated through the enhanced spin coating process is shown in Figure 3.11(d). The

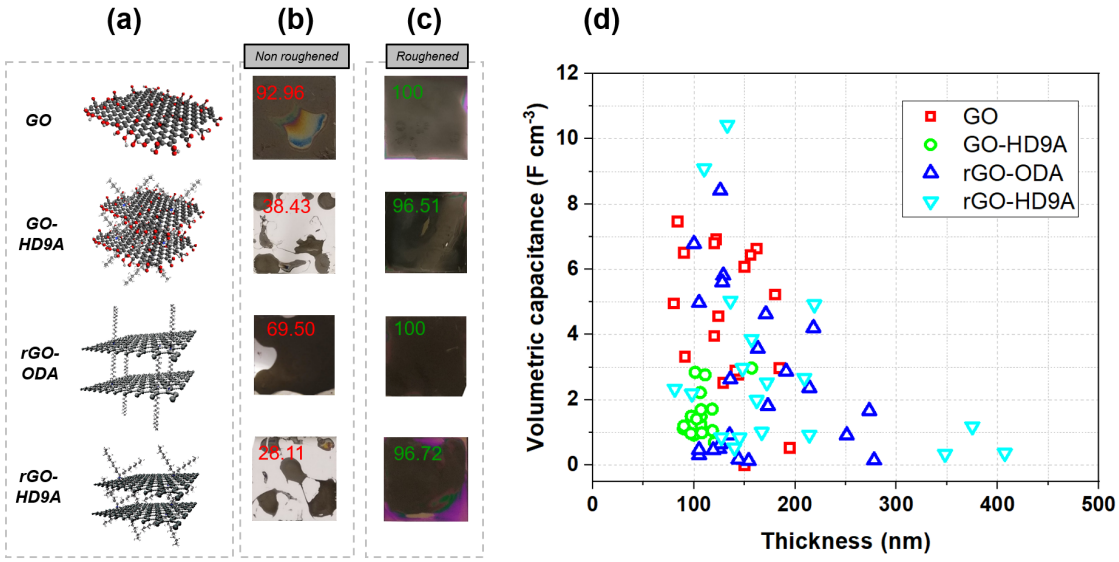


Figure 3.11: (a) Chemical structure of various composites of rGO synthesized to improve MSC's electrochemical performance. Application of surface roughening to improve the adhesion, uniformity, and coverage of electrodes on fabrication substrate which is (b) non roughened , (c) roughened, (d) Volumetric capacitance of the devices fabricated through spin-coating, color-coded for different electrode materials.

plot represents the volumetric capacitance of the MSCs fabricated through spin coating using GO, GO-HD9A, rGO-ODA, and rGO-HD9A. As visible from the thickness trends, GO-HD9A shows the highest uniformity in electrode thickness ranging from 90 nm to 150 nm. The volumetric capacitance of GO-HD9A is also more stable compared to other materials. rGO-HD9A and rGO-ODA both display very high volumetric capacitances of 10.5 F cm^{-3} and 8.5 F cm^{-3}. However, their spectrum of volumetric capacitance displays lower values at electrodes thicker than 200 nm. It can be inferred from these results, and the impact of electrode thickness in Paper 3 that improving the thickness of electrodes does not necessarily have a positive influence on the charge storage capacity of the deposited electrodes.

For the in-depth analysis of the properties of various rGO based composites for energy storage, the reader is referred to Paper 5. The chosen four materials display distinctly different features as electrodes: GO for assertive EDL performance, GO-HD9A for uniformity, rGO-ODA for capacitance improvement, and rGO-HD9A for improved thickness. GO-HD9A, rGO-ODA and rGO-HD9A improve the frequency behavior of the MSC substantially through their modulated structural van der Waals bonding in the alkane chains. GO-HD9A does not store a large amount of charge. However, it shows the lowest R_{esr} among the fabricated MSCs while demonstrating the highest uniformity in performance over many tested MSCs in the same batch.

3.7 Stacking materials

We have previously established a spin coating process to fabricate MSCs in a CMOS compatible spin-coating process by fabricating graphene-based rGO electrodes through an

aluminum hard mask. These devices, however, suffered from issues with electrode adhesion, wafer coverage of material, and uniformity in thickness of spin-coated electrodes. The spin coating process was improved by utilizing surface roughening through Fe nanoparticles for enhanced coverage, adhesion, and uniformity. However, this process has not been tested for stacking a variety of electrode materials to yield modular properties such as optimizing for energy density while demonstrating good power density. Thus, Paper 5 validates the fabrication of a modular composite stack of functionalized rGO based on four different materials. The MSC stack constituted a layer of GO-HD9A at the bottom to improve uniformity, followed by GO for strong EDL behavior, rGO-ODA for vertical conductivity and rGO-HD9A for higher electrode deposition and adhesion improvement during post-processing steps. The schematic of the stack can be seen in Figure 3.12(a). The functional groups can also allow rGO to be combined with several different materials to modulate the MSC characteristics. This stack of individual rGO based materials has an additive response to the capacitance characteristics of the Stack-MSC.

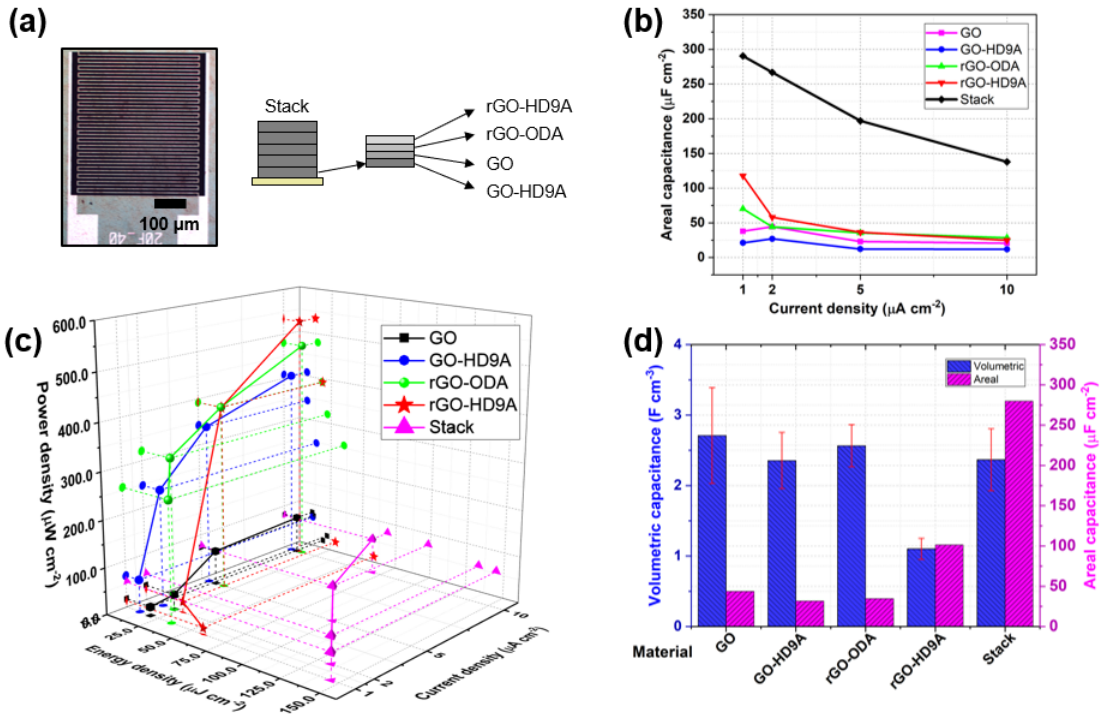


Figure 3.12: (a) Optical micrograph of the stack-MSC, inset contains the composition of the stack of electrodes, (b) Comparison of areal capacitance of the Stack MSC with individual MSCs of its constituent electrodes, (c) 3D plot of energy and power density of MSCs over a range of charging-discharging current densities, (d) Comparison of areal and volumetric capacitance of the electrodes and stack MSC at a single current density.

The stack-MSC is tested for its areal capacitance at various scan rates and current densities. The improved areal capacitance for the stack-MSC compared to MSCs from individual materials can be seen in Figure 3.12(b). The devices compared on all the wafers are based on the 20F geometry listed in Table 3.2. As visible, the capacitance

of the stack at lower current densities is higher than the combined capacitance of the individual materials. The same trend is followed at other current densities as well. The rate capability of Stack-MSC is about 50 % when the current density is scaled from 1 to 10 μA cm^{-2}, while the rate capability of other individual MSCs is lower than the Stack-MSC's retention capacity. This improvement can be due to the spin coating of multiple materials in a single stack unit, as shown in Figure 3.12(a). As discussed previously, the structure of rGO-ODA and rGO-HD9A through functionalization of alkane chains can show more significant free regions of ion transport between their interlayers. The cage-like matrix that the rGO-ODA and rGO-HD9A flakes assemble into can also be used to trap pseudocapacitive materials to improve the energy density of the MSCs as well. Despite an increase in energy density in the Stack-MSC, the power density of the device scales along with the power performance of the worst performing material in the stack, i.e. GO in our case. The results for energy and power density plotted against a range of current densities is shown in Figure 3.12(c). Finally, looking at the volumetric and areal capacitance of the stack with the other individual materials, we see that the stacking of materials does not influence the materials' capacitive properties. A more detailed comparison of the five MSCs fabricated through the enhanced spin coating is covered in Paper 5.

3.8 Discussion and conclusion

The role of MSCs as on-chip energy storage units have become more prominent with the latest achievements of high energy and power density reported. In this chapter, we have examined miniaturized ultracapacitors or MSCs in detail through a literature survey of devices reported in the literature and then fabricating and characterizing CNF and rGO based MSCs for on-chip integration with MPEHs for a self-powered sensor node. Despite achieving high energy densities in the fabricated MSCs sufficient for some application requirements, the energy density (per unit area) is far from matching the energy density (per unit area) provided by sunlight during one day. Thus, in this section, we will discuss the challenges and future perspectives of MSCs for moving further towards the goal of a self-powering on-chip sensor node.

MSCs as standalone devices currently are close to demonstrating rectifying electrical circuit outputs. Alongside capacitance, the cut-off frequency becomes a critical factor in establishing high power delivery. We have reported interdigitated structures as electrode geometries as in several other reports. The interelectrode distance can be reduced even further with advancements in photolithographic resolution. However, these geometries will touch a fundamental saturation point. Thus, in order to move beyond-interdigitated structures, several fractal-based geometries have been investigated in the literature [248]. A choice of examples are shown in Figure 3.13(a). These geometries on further evaluation of active electrode area, energy, power, and R_{esr} show improved performance in all the characteristics. In future iterations of spin-coated and CVD fabrication of MSCs, these designs can be considered as viable alternatives on Si/SiO_2 substrates after conducting essential simulations.

It is also possible to increase the energy density of the MSCs by using engineering materials for energy storage. Layered 2D and 3D framework molecules such as

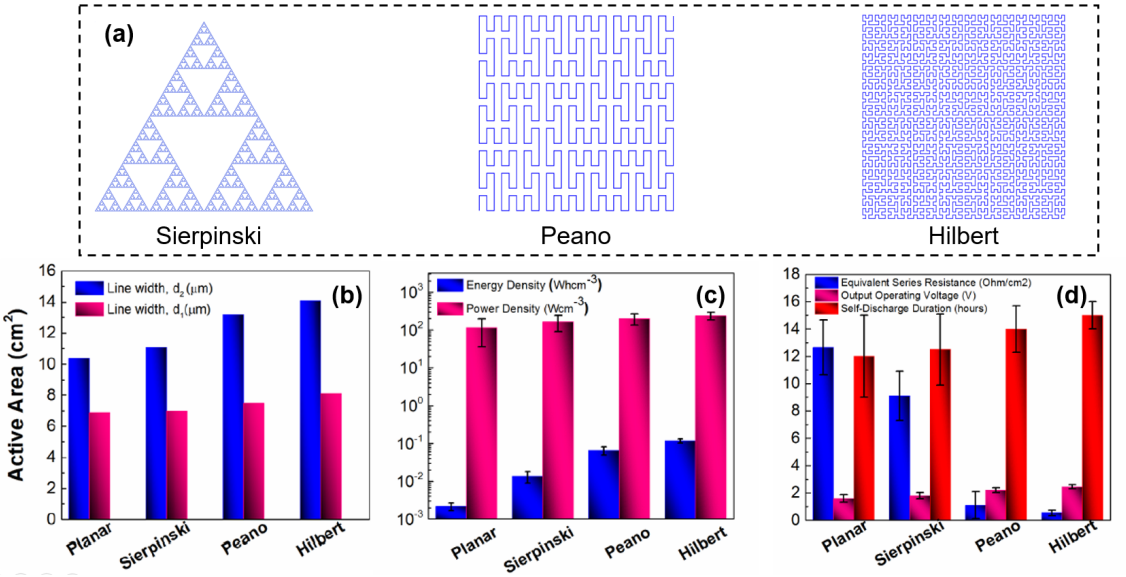


Figure 3.13: Impact of various electrode geometries on MSC performance over the same footprint area. (a) Various fractal based design geometries assessed by Thekkerara [247]. Scaling of (b) Active area, (c) Energy and power density, (d) Equivalent series resistance, operating voltage and self-discharge. Images reproduced after permission from the respective authors or publishing agencies.

metal-organic and covalent organic frameworks exhibit very high specific surface areas. Combining COFs [249] and MOFs [250] with transition metal dichalcogenides such as MXenes [251], perovskites [252], and black phosphorous [253] can result in high ion and sheet conductivity electrodes. In recent use, application of MnO_2 [254], TiO_2 [255], Ni and Co composites [256], V based oxides [257] and several other pseudocapacitive materials have led to extremely high capacitances of 400 F g^{-1} to 900 F g^{-1} (compared to graphene oxide, 123 F g^{-1} [258]) while retaining a similar power density to the state-of-the-art supercapacitors. Thus, pseudocapacitors can viably support applications requiring short-term high currents with their already high capacitance. These materials can be combined with rGO-inks for spin coating electrodes. The use of polymeric battery electrodes such as PANI [183, 259], PPY [260], and PEDOT:PSS [261] can also lead to increased energy densities and reduce the device's self-discharging behavior. We will also discuss the storage of even higher energy densities through novel electrode materials for enhanced ion conductivity, electron transport, and self-discharge reduction.

For the MSC fabrication process to be compatible with CMOS fabrication, MSCs need a process plan that can be incorporated within a MEMS or CMOS process scheme without affecting the material or design quality for the other devices. The issue of material loss during typical cleanroom processes such as photoresist development and ultrasonication has been mitigated by applying surface roughened Cr NPs, as explained in the previous sections regarding the enhanced spin coating process. Some CMOS compatibility issues in the MSC fabrication process still need to be addressed before the process can be implemented for integrated systems-on-chip. For example, the standardization of graphene-based materials in a semiconductor cleanroom environment

is challenging. Another challenge of using Au as current collectors can be mitigated by using other metals such as Pd, Pt, Mo, Cr, or W, which are CMOS compatible. However, as discussed before, the capacitance of Au/Ti collector VACNS is four times higher than Pd/Ti VACNS MSCs. Finally, using aqueous or gel electrolytes with CMOS circuit fabrication requires further studies on proper packaging solutions such as epoxy glues, poly-di-methyl-siloxane molding, or micromachined package fabrication. The next chapter will review these issues and issues relating to the on-chip integration of micro energy harvesters with MSCs.

Chapter 4

On-chip integration

IoT platforms such as Industry 4.0 and AIoT are envisioned on a platform of wireless sensor networks that can accumulate and transfer information about the surroundings without replacing them at regular intervals. The power supply of a wireless sensor node is arguably a major bottleneck in the miniaturization and lifelong implementation of wireless sensor networks [262]. Integration of energy harvesters and energy storage units will play a vital role in utilizing energy present in the environment and supplying it to the sensor while demonstrating an extended lifetime. They can eventually replace or reduce the reliance on pollution inducing power supplies such as lead-acid and lithium batteries.

In the previous chapters, we have discussed the design and fabrication of MPEHs and MSCs as potential candidates for on-chip integration for self-powering sensor nodes. An M-shaped MPEH is designed and fabricated to display the principle of the broad bandwidth of working frequencies that can potentially harvest approximately 20 nW in a 4 mm^2 piezoelectric area structure according to simulations of the fabricated cantilevers. The fabrication of the device was performed through conventional micromachining techniques. Similarly, the MSCs were designed for high power density and CMOS compatibility by using graphene-based composites for a high areal capacitance of 280 $\mu F\ cm^{-2}$. In this chapter, we will examine various possible integration methods through a survey of existing integrated devices reported in the literature. Next, we will argue potential integration strategies for MPEHs and MSCs designed in this work with separate discussions on the packaging of MPEHs and MSCs. We will describe an optimal FEOL and BEOL integration of the two units. Finally, we will conclude the thesis by looking at the future aspects of MSCs and energy harvesters geared towards further miniaturizing on-chip self-powered sensor nodes.

4.1 Existing designs

There has been considerable work done to demonstrate an on-chip sensor node equipped with an energy harvesting and storage unit and sensors, power conditioning circuits, and RF units. Several devices have been fabricated for flexible electronics that perhaps show the roadmap for developing an integrated harvester storage sensor unit. Jeong et al. [266] developed a triboelectric energy harvester using silica nanostructures and

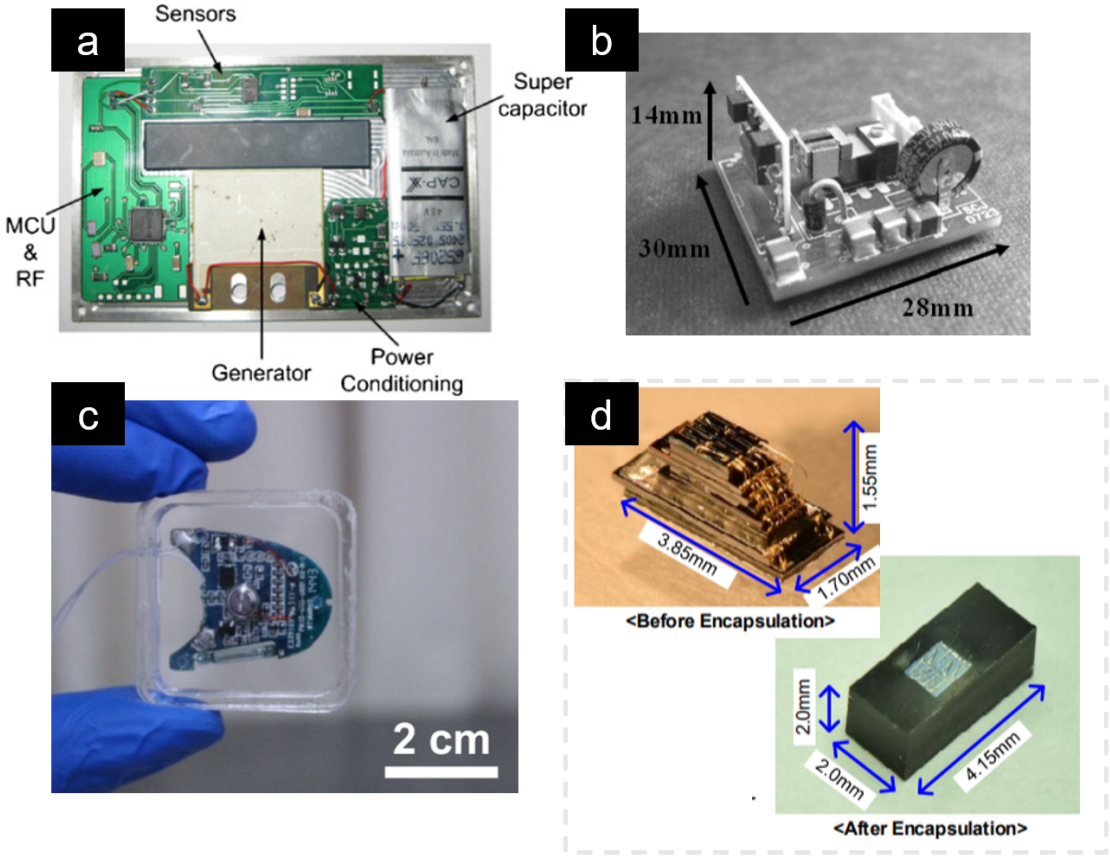


Figure 4.1: Various sensor node architectures using energy harvesters and energy storage units as on-chip power supply. (a) Piezoelectric harvester and pouch cell supercapacitor based sensor node by Roundy et al. [12]. (b) Electromagnetic harvester and coin cell supercapacitor combination by Beeby et al. [263]. (c) Triboelectric energy powering a temperature sensor with a caapcitor shown by Zhao et al. [264]. (d) Solar energy harvester with temperature sensor powered by a MB by Lee et al. [265]. Images reproduced after permission from the respective authors or publishing agencies.

successfully charged a 22 μF capacitor at 1 V s^{-1}. Similarly, a flexible harvester and capacitor were fabricated by Tong et al. [267] using polymer composite films. The capacitor was charged through finger motion and bending that induced electric charge redistribution harvested by the PVDF used as the piezoelectric material. Triboelectric nanogenerators have also been used by Wang et al. [268] to charge a Li/ion battery in 11 hours. The solid-state battery could provide a power of 0.3 μW cm^{-2} while the system is subjected to mechanical agitation or motion. Dennler et al. [269] report a hybrid organic, inorganic solar cell using a Li-polymer battery (66 mm × 35 mm × 4.2 mm) connected through custom interconnects. The solar cell is designed in such a way that the battery is always fully charged by providing a voltage of 3.8 V. The battery can deliver power in a range of μW to mW at 1 V to 20 V. Mao et al. [270] could deliver an instantaneous power of 15 mW cm^{-3} by scavenging energy from a single electrode triboelectric flexible generator that could light up to 6 commercial LEDs.

Graphene-based energy harvesting and energy storage devices have been integrated on a single substrate by Chien et al. [271]. They used CVD grown graphene with

P3HT based OPVs to show an open circuit voltage of 0.55 V. The capacitor could be charged to 2.5 mF cm^{-2} within 40 s under illumination conditions. Supercapacitors have also directly been integrated with silicon PVs by Westover et al. [272]. Beeby et al. [263] demonstrated an electromagnetic energy harvester coupled with a supercapacitor shown in Figure 4.1(a). The harvester produced 58 μW at a frequency of 52 Hz while the coin cell supercapacitor had a capacity of 0.22 F. To compensate for the low harvester output voltage, they used a voltage multiplier circuit, which also charged by the supercapacitor. The processing unit was Microchip PIC16F676 which could operate at 8.6 μA at 2 V. The total size on the sensor node is 28 × 30 × 14 mm^3.

Roundy et al. [12] developed a 'smart-tag' self-power sensor node using a vibrational energy harvester and pouch supercapacitor from Cap-xx shown in Figure 4.1(b). The overall dimensions of the sensor node were 85 × 55 × 3 mm^3. The energy harvester generated an output power of 240 μW at 67 Hz, delivered to the 0.55 F supercapacitor. The supercapacitor had a voltage limit of 4.5 V with maximum energy storage of 5.6 J. A 3-axis accelerometer, AD converter, Texas Instruments micro-controller CC2430 and a cold-start circuit were used as sensor node units. The typical current consumption of these devices ranges from 15 μA for the cold-start circuit to 27 mA for the micro-controller. The supercapacitor was supplied a constant voltage of 1-2 V through the rectifier output. The generated power in the vibrational harvester and stored power in the Cap-xx supercapacitor was deemed sufficient for periodic sensing and charging.

Wireless temperature sensors can also be powered by triboelectric nanogenerators, as revealed by Zhao et al. [264]. They showed a compact, 40 mm × 40 mm × 7 mm sensor node that used polyamide films as wind-induced vibrational harvesters as can be seen in Figure 4.1(c). The device could continuously work for 14 h at a wind speed of 12 m s^{-1}. They can even be operated from a distance of 26 m. A power management unit delivered a constant output voltage of 3.3 V to a 10 mF capacitor. The sensor node transmitted the temperature of the environment to a smartphone.

A genuinely wireless miniaturized sensor node was presented by Lee et al. [265] (Figure 4.1(d)). They showed a fully encapsulated 17 mm^3 temperature sensor powered by a lithium battery with a solar harvester used to charge it. The sensor node components are integrated into a BEOL process with chips' 3D stacking, followed by wire bonding to a micro-PCB. The device was encapsulated in black epoxy, making the senor node a complete black box for temperature sensing. However, their inherent nature of generating energy through faradaic reactions reduces the cathode, which cannot be replenished indefinitely.

4.2 Packaging and encapsulation of MPEH and MSC

MPEH encapsulation

The MPEH can be encapsulated in a variety of ways. Elfrink et al. [11] fabricated encapsulation packages using a glass substrate. The substrate was immersed in HF solution and etched. The contacts to the glass package were enabled through powder blasting. The encapsulation was bonded to the MPEH using the SU-8 layer and a wafer-scale roller coating process. Under vacuum conditions, the glass substrates were bonded

to the Si devices in two consequent wafer-scale steps. A description of the fabrication process and the subsequent sensor node is shown in Figure 4.2(a). Another method of encapsulation has been devised by the Jia and Seshia group [117] where they developed deep silicon cavities to make a leadless chip carrier. The MPEH is then bonded to the contact pads of the carrier, and a plate is sealed on top using a gettering material. An example of such a package is shown in Figure 4.2(b).

MSC encapsulation

Another important consideration for devising on-chip integration of MSCs involves the utilization of a solid or gel electrolyte that does not flow across the substrate surface. This requires either a form of encapsulation barrier that stops the flow of electrolytes or a solid electrolyte derived from polymer technology. One example of a solid electrolyte is shown in Figure 4.2(c). It shows a thick ionogel synthesized by mixing SU-8 and EMIM-TFSI. The ionogel layer is spin-coated on the silicon substrate and then exposed to UV-lithography [273]. The cell voltage from the photo patternable electrolyte could reach up to 2.5 V, which results in a significant increase in the energy density of the MSC. As a solid gel electrolyte, the ionogel alleviates the issue of reflowing in on-chip circuitry.

The same process has also been used by Asbani et al. [274] using EMIM-TFSI and PVDF polymer. The gelation of this mixture could be completed in vacuum at 60 °C for 18 hours. Thiol-ene monomer with trimethylolpropane tris(3-mercapto propionate) (TMPTMP, thiol monomer) and trimethylolpropane triacrylate (TMPTA, ene monomer) with EMIM-TFSI is yet another electrolyte used in hydrodynamic jet printing for high areal energy density MSCs by Lee et al. [275]. Solid electrolytes, apart from MSCs, are also used in microactuators and transistors. The electrolytes for these applications are chosen for their voltage window and high ionic mobility. Demonstration of good performance in these properties is highly desirable for MSCs. Zhong et al. [276] developed a solid polymer electrolyte from bisphenol A ethoxylate dimethacrylate (BEMA) and poly(ethylene glycol) methyl ether methacrylate (PEGMA) monomers through photopolymerization and mixed them with $NaClO_4$. The polymer mixture was spin-coated on a silicon substrate and illuminated in UV lithography. The polymer was developed using acetone. Weissbach et al. [277] also showed a photo patternable electrolyte using EMIM-$EtSO_4$, N-isopropylacrylamide, N, N'-methylenebisacrylamide, 2-hydroxy-4'-(2-hydroxy-ethoxy)-2-methylpropiophenone, 1-ethyl-3-methylimidazolium ethyl sulfate, and deionized water. The solution was stirred overnight and developed in acetone through a photomask. Finally, EMIM-TFSI has also been mixed with tetramethoxysilane (TMOS), and formic acid by Hsia et al. [278]. The gelation process is carried out for over 12 hours before testing [279].

4.3 Potential integration strategies

We will describe three potential ways to integrate energy harvesters and energy storage units. The first integration method involves the connection of MPEH and MSC dies post-fabrication using wire bonds on a custom PCB. The second method is FEOL integration, in which the two devices are fabricated on a single substrate, an example of SoC. The

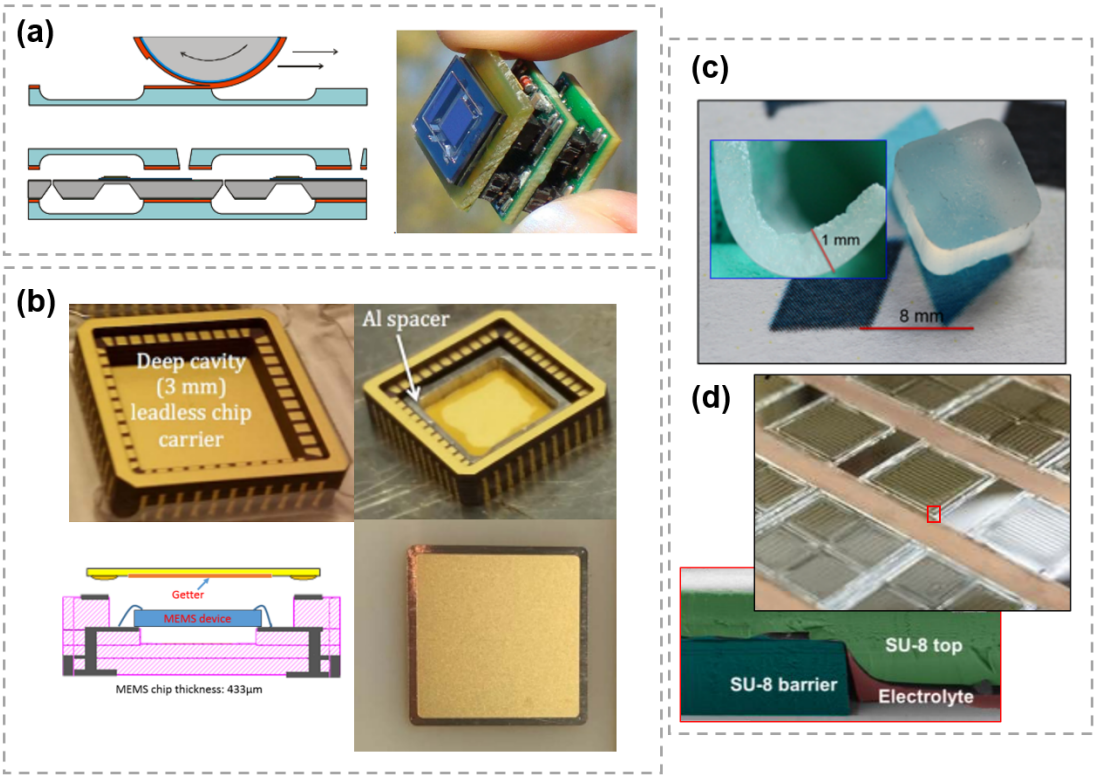


Figure 4.2: Strategies for packaging MPEH and MSC devices for on-chip integration. (a) Glass packaging demonstrated by Elfrink et al. [11]. (b) Deep cavity space bonding methodology shown by Jia et al. [117]. (c) Solid electrolyte ionogels for on chip integration purposes by Asbani et al. [274]. (d) Wafer scale integration of MSCs through SU-8 area enclosement technique by Wang et al. [279]. Images reproduced after permission from the respective authors or publishing agencies.

silicon substrate used for processing can also include sensors and ICs fabricated in the same process plan. This method aims for a genuinely monolithic device where no wire bonds would be required. Finally, the third method is BEOL integration, in which the energy harvester, storage, and ICs are manufactured through 3D integration using Cu or CNT vias for connections between different levels. The last two methods are highly challenging as several factors such as temperature or etching gases severely limit the prospect of seamless integration. However, finding a solution for pure FEOL of BEOL fabrication can enable a seamless technology integration with sensors and CMOS electronics. In this section, we will discuss the three methodologies for integration, propose a fabrication sequence, and consider the assembly's challenging aspects.

4.3.1 Component assembly

The component assembly method of assembling the on-chip devices on a PCB alongside an integrated black-box sensor node that can contain sensors, transceivers, and power conditioning circuits is quite common commercially [262]. This process involves the demonstration of four main objectives to achieve an on-chip sensor node. The fabrication of the MPEH and MSC can take place separately, including encapsulation

steps using different techniques discussed in the previous section. In this method, the issue for standard processing for fabrication of MPEH and MSC is generally trivial as the components are usually assembled outside a cleanroom facility. Since the MSC fabrication has various routes, the option that shows the highest energy or power density can be utilized, for example, spin-coated MSCs shown in Paper 2 and Paper 3, both of the devices are suitable for component assembly with MPEH.

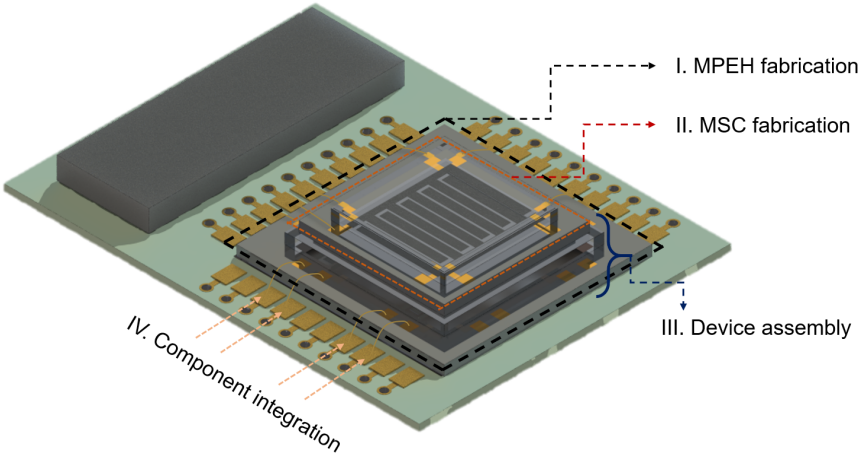


Figure 4.3: Proposed manufacturing of the packaged MSC and MPEH integrated with wireless sensor node.

On the other hand, the MPEH packaging should consider the bonding on PCB. One way the PCB can be designed such that it has an opening for the energy harvester to vibrate. Also, in a way, the opening can be used to bond the MPEH die directly to the vibrating surface to reduce the damping induced by PCB to chip bounding. But, the impact of the PCB on the mechanical behavior and transduction of vibrations from the environment can be a cause of concern regarding the power output. Thus, if the MPEH can be encapsulated with a freedom to display internal vibrations, it would be a better solution. Once the MPEH is attached to the PCB, it can be wire-bonded to the PCB contacts using aluminum or gold wire bonds. The MSC can be bonded on top of the MPEH using the same epoxy glue used for bonding the MPEH in the previous level. The MSC is to be wire bonded separately from the MPEH as the conditions for wire-bonding will change based on the level of integration from the PCB. The wire bonds on the PCB contact pads are to be arranged to complete the circuit on the PCB. The sensor can be soldered to the PCB surface.

While the component assembly method allows for a higher degree of freedom for the fabrication of MPEHs and MSCs, some issues can still impact the performance and size of the on-chip sensor node. Firstly, the size of the sensor node would be dependent on the PCB size and thickness. Secondly, there is a risk of glue or epoxy used for bonding to reflow, which can cause the assembled sensor node to detach or cause an open or short circuit. Thirdly, the wire bonding failures such as voiding, looping, contaminant, and calibration issues can severely affect the yield of the fabricated devices [280]. Finally, a very significant problem during applications can be attributed to using vibrations as a source of energy. If not appropriately transferred to the energy harvester, the vibrations

on the PCB can lead to breakage of wirebonds, detachment of bonded dies, and in some cases, delamination of MSC electrodes. Thus, experiments relating to the die's and PCB's vibrational stability must be carried out before assembling the components. Similarly, an experimental or simulation level evaluation of the wire bonds must also be conducted to analyze the structural integrity of the wires and electrical losses in the on-chip sensor system.

4.3.2 FEOL integration

The FEOL process generally refers to the IC fabrication of transistors, resistors, and capacitors patterned on the semiconductor substrate. The process aims to fabricate all the devices on a single level of the silicon substrate. Such a monolithic integration is highly desirable as it reduces the cost of integrating different technologies on a wafer scale level. Integration of MEMS devices such as MPEH and energy storage fabricated FEOL is the final goal of an on-chip power supply, albeit challenging. A representation of the proposed fabrication process is shown in Figure 4.4.

The fabrication processes for the MPEH and MSC are based on lithography and etching of silicon substrate and carbon material, respectively. As both the devices require current collectors to function, the collector metals can be evaporated for them within the same process. As the MPEH processing steps are elaborate and span several masks, the MPEH fabrication is a first-hand priority. The MPEH can be fabricated with the final device release step before carrying out the MSC fabrication processing.

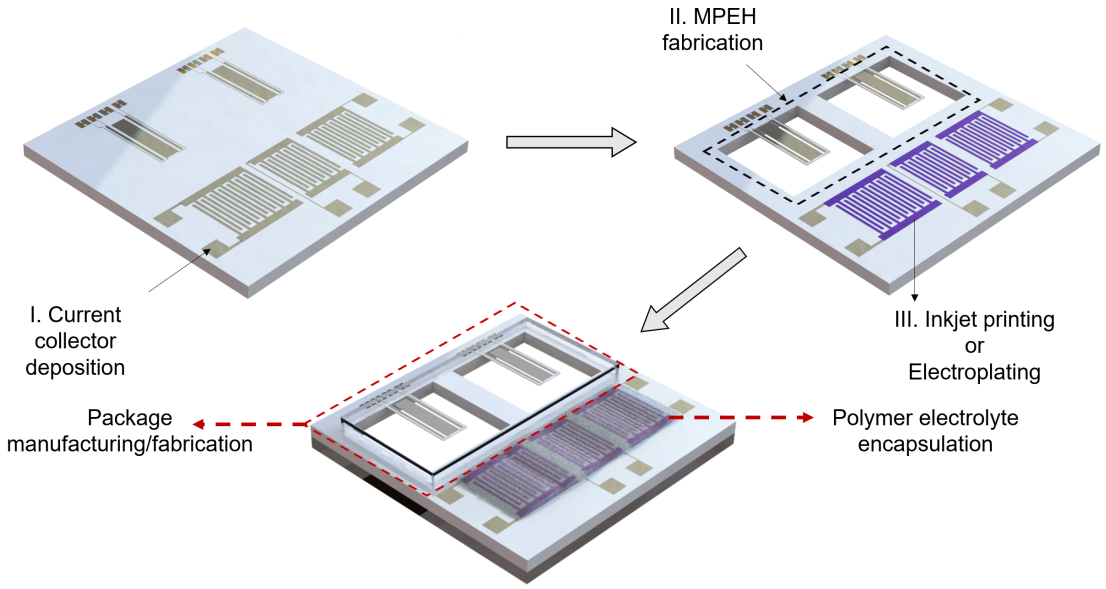


Figure 4.4: Representation of proposed FEOL methodology for integration of MPEH and MSC including packaging and encapsulation.

MSC fabrication follows the MPEH processing in step III of Figure 4.4. For the proposed FEOL integration, we recommend two CMOS compatible processes other than the spin coating of electrodes. While the spin coating is ubiquitous in terms of materials, this electrode deposition process is not suitable for integration with MPEHs

due to several reasons. The first processing issue relates to the spin coating process itself. During spin coating, as discussed before, the substrate is held under vacuum on the spinner chuck, and then the electrode material is spin-coated on it. As the MPEH device contains fully etched silicon cavities and fragile silicon cantilevers, any form of spinning is not advised. One can argue for the processing of MSC before the MPEH fabrication. However, due to the utilization of carbon material and SU-8 packaging, both the material and package can run into the risk of detachment or being washed off from the substrate during the front or backside etching of the MPEH. Thus, spin-coated MSCs cannot be advised unless a revolutionary processing method is discovered or invented in the meantime.

Similarly, the CVD process is also not utilizable due to its high-temperature processing. The Curie temperature of a piezoelectric material can range up to 245 °C [281] and the CVD process requires processing temperatures over 300 °C, in our case 390 °C and 550 °C. Thus, we are restricted to other options such as inkjet printing and electroplating. Both the methods can be used after MPEH processing. They can be very selective of the places for electrode deposition as inkjet printing uses the raster scanning method, while electroplating uses the electric potential developed on the current collectors of the MSC. After the harvester fabrication, materials such as mesoporous gold [65], Prussian blue [282], or carbon inks [216] can be deposited on the MSC current collectors. The final steps for FEOL integration involve packaging the MPEH and MSC as examined in the previous section.

The fabricated die must eventually be heterogeneously assembled with the sensor and IC devices on a PCB or integrated with these devices through BEOL processing. Also, the fabrication of MSCs reduces the fill factor of the MPEH. Instead of four devices that could be manufactured on a 1 cm^2 die, the FEOL process can integrate only two, thus reducing the fill factor to one half. This issue can become more severe for solar energy harvesters as they require as high fill factor as possible to extract maximum energy from the incident solar radiation. Finally, removing photoresists from the etched MPEH structures is a challenging aspect of device fabrication. Any residual photoresist on the MSC current collectors can lead to device performance degradation.

4.3.3 BEOL integration

The final method of integration involves BEOL processing. This step is usually followed in IC fabrication for connecting individual devices fabricated across different levels of the fabrication sequence through silicon vias. The most commonly used metal for through-silicon vias are copper[283]. However, more recently, CNTs have also been used for such applications [284]. The BEOL processing can be categorized into two formats - pure BEOL and a more realistic FEOL + BEOL integration. A representation of the proposed device is shown in Figure 4.5.

While fabricating a pure BEOL package, the packaging of the MSC can be intertwined with the substrate used for capping the energy harvester [163]. If the processing of devices is conducted on thin substrates, it would be more beneficial for integration with TSVs in later fabrication steps.

The first level of fabrication relates to manufacturing power management circuitry with the sensor and transceiver units. Current 0.18 μm CMOS technology can produce a solar PV with PMU in a 1.5 mm^2 area [285]. While the fill-factor of the PV suffers, the system can self-start while using an off-the-shelf supercapacitor. for larger amount of energy harvesting, it is desirable for the solar harvesting device to be on the top level such that it is exposed to maximum light intensity. The BEOL fabrication can be processed for making a dual in-line chip package with the sensor, and IC units forming the first level of substrate. The second layer of substrate can be insulated from the first level using thin film insulators. The insulators can be etched for TSV contacts followed by spin coating of carbon electrodes on metal current collectors. The MSC packaging on level three is designed to accomplish three purposes: (1) housing the MSC electrolyte, (2) interconnect formation from level one and two to level three, and (3) acting as a substrate for an energy harvester (such as solar PV fabrication). The substrate for level three of BEOL fabrication may be processed separately for isotropically etched backsides. This can be followed by bonding of the two substrates and energy harvester fabrication. If such a BEOL process can be demonstrated, we can produce a large yield of devices within a single batch of processing. The devices can be diced and bonded on dual in-line IC leads. Finally, the packaging can be a further improved by using epoxy to bond to on-chip circuitry with direct SoC leads such as Figure 4.5.

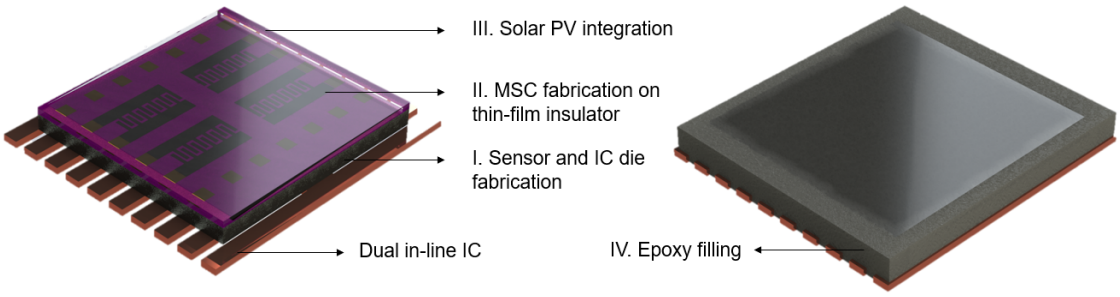


Figure 4.5: Representation of proposed BEOL methodology for integration of an energy harvester and MSC.

However, there are several challenges that can restrict the vision of such BEOL fabrication. One significant issue is dealing with high tensile stress and curling structures after the bonding of substrates [157]. Another issue can arise from the detachment of vias due to material or structural stress. Packaging of MEMS devices or MSCs can sometimes lead to the formation of high pressure in the packing. This can lead to an increase in residual stress and device failure. Furthermore, there is a risk of low wafer yield compared to component integration and FEOL processing. This issue can be due to adding levels of the substrate above the fully processed level. With a single stack of PMU, sensor, MSC, harvester and TSVs, breakdown of any one device will lead to the total failure of that die. In component integration, if one of the devices does not function, it is possible to change it after fabrication. Similarly, for FEOL processing, the yield mainly depends on the adeptness of the lithography based fabrication process as it rules out several challenging processing steps such as die to die bonding.

Chapter 5

Conclusion and summary of appended papers

Conclusion

Miniaturization of devices is essential for the design and fabrication of IoT applications. As microsystems shrink to form components of complex IoT networks, their power demands cannot be met entirely through conventional batteries with a limited life span. Having a miniaturized power supply that recharges itself based on the energy present in the surroundings will give the future IoT access to several relevant and challenging locations. On-chip electrochemical capacitors with PEHs can serve as a platform for on-chip energy storage for a self-powering sensor node for IoT wireless sensor networks. Micro-machining fabrication techniques have been used in manufacturing energy harvesters at a large scale. Similarly, for energy storage, MSCs are miniaturized energy storage devices that can be combined in an on-chip platform as a component of a power supply for IoT sensors. Integration of these on-chip devices requires them to be fabricated through CMOS compatible fabrication techniques.

This thesis reports work on an M-shaped 2DOF micro-cantilever for energy harvesting. It was designed to reduce the gaps between the first two natural frequencies to achieve a broad bandwidth and improved stress distribution. The design was fabricated using micromachining techniques and was examined for dimensional and mechanical characteristics. The dimensional analysis showed the feasibility of the fabrication process. The mechanical evaluation further demonstrated that the device behavior is close to the intended simulation design. Also, the fabricated M-shape micro-cantilever design shows harvesting capabilities in beam vibrations associated with the coupling mechanism in a single structure. The fabrication process of PEHs was further developed and optimized to improve the manufacturing yield of the devices. Based on the performance of the fabricated devices, designs were developed for a more feasible fabrication process for improved wafer yield. Based on a 2DOF cantilever design, the devices were simulated to find ways to improve the power density and bandwidth of working frequencies.

MSC fabrication for CMOS compatible processes requires a feasible and facile technique pre-existing in IC industries. We have shown spin-coating and CVD as CMOS

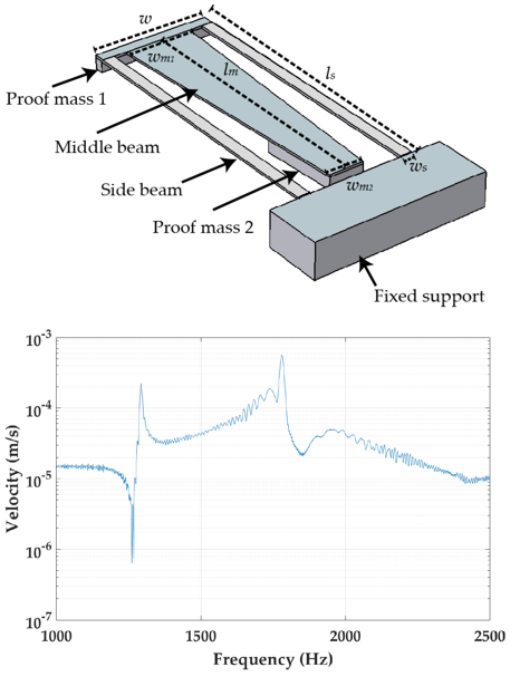
compatible processes. The use of spin-coating of carbon materials can further be optimized by improving the surface adhesion of the substrate using Fe nanoparticles through evaporation and annealing. The enhanced surface roughness improves thickness, mass retention and uniformity of the electrode material coverage on a Si substrate. The fabricated devices were compared to state-of-the-art CVD grown CNF based MSCs. The performance of rGO based MSCs was further improved by employing a stack of spin-coated rGO based composites.

The fabricated devices can be integrated with an on-chip PMU and other application-specific ICs to realize an integrated power supply. For such realization, substantial work still needs to be performed. Making the right type of power supply is highly dependent on requirements from applications. For example, for MSC and MPEHs, these application areas can be broadly based on pulsed power requirement, or low duty ratio, rapid cycling, or buffering batteries during peaky loads. Similarly, some other considerations for a power supply can include investigating the total cycle life of the combined harvesting and storage unit, calendar lifetime for product evaluation, temperature range of useful application, fatigue shock and vibration testing for autonomous deployment, pressure, humidity, and safety.

Applicability of energy harvesters and energy storage devices for powering micro or nano systems for sensing and monitoring can lead to a paradigm shift in energy conversion and utilization. The approach is further promising due to its an applicability as subsidiary units in battery management systems that can harvest the ambient energy in the surrounding. The integration of technologies, in the short run, will aim for improving the battery lifetimes. In the long run, such power management systems can reduce fossil fuel consumption and power supply costs. The produced and stored energy will also be clean and emission free which will result in a positive environmental impact. If the processing for manufacturing such devices is scalable, then the industry and consumers can also benefit from cheaper power supplies with unlimited lifetimes. Such endless possibilities can build a foundation for a better life on this planet for all living organism alike who will benefit from clean and sustainable energy not only in this generation, but for the time earth revolves around the sun.

Summary of appended papers

Paper 1: A Micromachined Coupled Cantilever for Piezoelectric Energy Harvesters



This paper presents a demonstration of the feasibility of fabricating micro-cantilever harvesters with extended stress distribution and enhanced bandwidth by exploiting an M-shaped two-degrees-of-freedom design. The measured mechanical response of the fabricated device displays the predicted dual resonance peak behavior with the fundamental peak at the intended frequency.

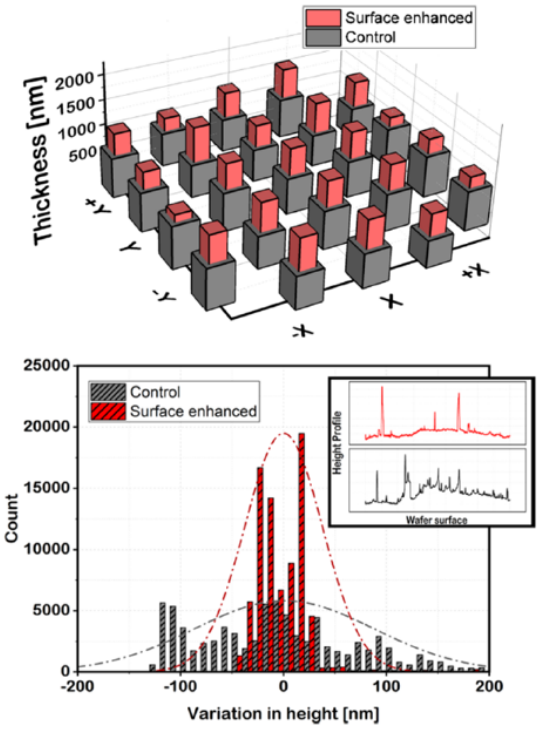
The M-shaped 2DOF cantilever design has the features of high energy conversion efficiency in a miniaturized environment where the available vibrational energy varies in frequency. The cantilever was designed based on the principle of closing the gaps between the first two natural frequencies to achieve a broad bandwidth and improved stress distribution. The design was fabricated using micromachining techniques and was investigated for dimensional and mechanical characteristics. Dimensional analysis showed the feasibility of the fabrication process.

Mechanical evaluation further demonstrated that the device behavior is close to what was intended in the design. In addition, the demonstrated M-shape micro-cantilever design shows harvesting capabilities in beam vibrations ranging from 1293 Hz to 1781 Hz, which can be attributed to the coupling mechanism in a single structure. It makes such a design suitable for future large volume production of integrated self-powered sensors nodes for the Internet of Things.

Paper 2: Enhanced electrode deposition for on-chip integrated micro-supercapacitors by controlled surface roughening

On-chip microsupercapacitors, integrated with energy harvesters, hold substantial promise for developing self-powered wireless sensor systems. However, MSCs have conventionally been manufactured through techniques incompatible with semiconductor fabrication technology, the most significant bottleneck being the electrode deposition technique.

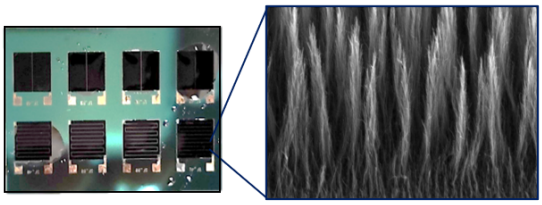
Utilization of spin-coating for electrode deposition has shown promise to deliver several CMOS compatible MSCs on a silicon substrate. Yet, their limited electrochemical performance and yield over the substrate have remained challenges obstructing their subsequent integration. We report a facile surface roughening technique for improving the wafer-yield and the electrochemical performance of complementary metal-oxide-semiconductor (CMOS) compatible MSCs, specifically for reduced graphene oxide (rGO) as an electrode material.

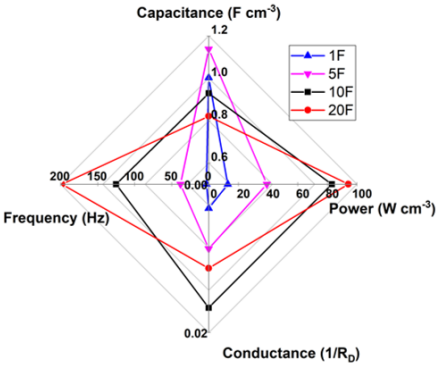


A 4 nm iron layer is deposited and annealed on the wafer substrate to increase the roughness of the surface. In comparison to standard non-roughened MSCs, the increase in surface roughness leads to a 78% increased electrode thickness, 21% improvement in mass retention, 57% improvement in the uniformity of the spin coated electrodes and a high yield of 87% working devices on a 2" silicon substrate. Furthermore, these improvements directly translate to higher capacitive performance with enhanced rate capability, energy, and power density. This technique brings us one step closer to fully integrable CMOS compatible MSCs in self powered systems for on-chip wireless sensor electronics.

Paper 3: Impact of electrode geometry and thickness on planar on-chip microsupercapacitors

We report an assessment of the influence of both finger geometry and vertically-oriented carbon nanofiber lengths in planar microsupercapacitors. Increasing the finger number leads to an up-scaling in areal power densities, which increases with scan rate owing to lower device resistance.

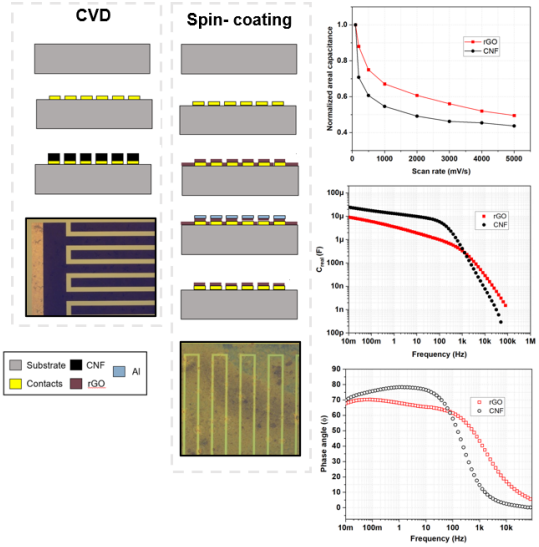




Growing the nanofibers longer, however, does not lead to a proportional growth in capacitance, proposedly related to limited ion penetration of the electrode. Among all the devices, the devices with more than one finger on each current collector demonstrated a decrease in areal capacitance due to reduced active electrode footprint during the low frequency response.

Overall, while including the effects of device resistance, the MSC with 10 fingers displays the best overall performance while incurring the lowest trade-off costs. The thickness of the electrode has a very small impact on the capacitance, characteristic frequency, and resistance.

Paper 4: Comparison of Thermally Grown Carbon Nanofiber-Based and Reduced Graphene Oxide-Based CMOS-Compatible Microsupercapacitors

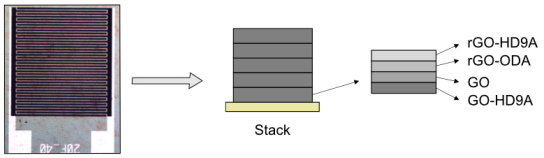


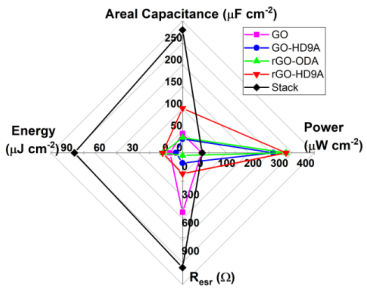
Microsupercapacitors as miniatured energy storage devices require complementary metal oxide semiconductor (CMOS) compatible techniques for electrode deposition in order to be integrated in wireless sensor network sensor systems. Among several processing techniques, chemical vapor deposition (CVD) and spin coating, present in almost all CMOS manufacturing facilities, are the two most viable processes in terms of electrode growth and deposition respectively.

In order to make a well reasoned argument for choosing either of these techniques to fabricate MSCs utilizable for an on-chip power supply, we need a comparative assessment of their electrochemical performance. This paper reports the evaluation of MSCs with CVD grown carbon nanofibers (CNF) and spin coated reduced graphene oxide (rGO) based electrodes. The devices are compared for their capacitance, energy and power density, charge retention, characteristic frequencies, and ease of fabrication over a large sweep of scan rates, current densities and frequencies.

The rGO based MSCs demonstrated 112 μF cm^{-2} at 100 mV s^{-1} and a power density of 12.8 mW cm^{-2}. The CNF based MSCs show 269.7 μF cm^{-2} and 30.8 mW cm−2 at the same inputs. For the impedance spectroscopy results, CVD grown CNF outperforms spin coated rGO in capacitive storage at low frequencies, while the latter is better in terms of charge retention and high frequency capacitance response.

Paper 5: Spin-coated Heterogenous Stacked Electrodes for Performance Enhancement in CMOS compatible On-chip Microsupercapacitors





Integration of microsupercapacitors (MSCs) with on-chip sensors and actuators with nano-energy harvesters can improve the lifetime of wireless sensor nodes in an Internet-of-Things (IoT) architecture. However, to be easy to integrate with such harvester technology, MSCs should be fabricated through a complementary-metal-oxide-semiconductor (CMOS) compatible technology, ubiquitous in electrode choice with the capability of heterogeneous stacking of electrodes for modulation in properties driven by application requirements.

In this article, we address both these issues through fabrication of multi-electrode modular, high energy density micro-supercapacitor (MSC) containing reduced graphene oxide (GO), GO-heptadecane-9-amine (GO-HD9A), rGO-octadecylamine (rGO-ODA), and rGO-heptadecane-9-amine (rGO-HD9A) stack through a scalable, CMOS compatible, high wafer-yield spin coating process. Furthermore, we compare the performance of the stack with individual electrode MSCs fabricated through the same process.

The individual electrodes, in presence of 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfony)imide (EMIM-TFSI), demonstrate a capacitance of 38, 30, 36, and 105 μF cm^{-2} at 20 mV s^{-1} whereas the fabricated stack of electrodes demonstrates a high capacitance of 280 μF cm^{-2} at 20 mV s^{-1} while retaining and enhancing the material dependent capacitance, charge retention, and power density.

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