

THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Modulation, efficiency and lifetime of two-level
and multilevel converters for a hydropower
application

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Technical Report No. 1111-111X
ISSN 3.1415-9265
This thesis has been prepared using L^AT_EX.

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Printed by Chalmers Reproservice
Gothenburg, Sweden, May 2022

Abstract

Along with the integration of the renewable energy in the electrical grid, the pumped-storage hydropower has gained more and more attention due to its fast response and energy storage ability. To have a higher overall efficiency and more flexibility of the system, variable speed is preferred in the operation of the pumped-storage hydropower applications. The key component for the variable speed pumped-storage hydropower application is the full-size power converter, which is the main study object in this work.

Different converter topologies, such as the two-level converter, the neutral point clamped converter, and the modular multilevel converter, have been investigated in this study. The simulation and experimental results verify the feasibility of the studied modulation and control methods for different converter topologies. The nine-level modular multilevel converter needs four times the amount of the power modules compared with the two-level converter, not to mention the extra submodule capacitors and arm inductors in the nine-level modular multilevel converter. However, the nine-level modular multilevel converter shows the best efficiency of 99.37% at nominal power in the loss study, while the classical two-level converter shows an efficiency of 98.44%. At the end, a lifetime study is conducted for power switches inside a modular multilevel converter, and it is found that with the used semiconductors design, i.e., the semiconductors have an RMS current value that of half of its stated maximum value, the lifetime requirement of 30 years can always be fulfilled.

Keywords: Pumped-storage hydropower, variable speed, converter, neutral point clamped converter, modular multilevel converter, pulse width modulation, space vector modulation, efficiency, losses, thermal modelling, lifetime.

List of Publications

This thesis is based on the following publications:

[I] **C. Tang** and T. Thiringer, “Thermal modelling of a multichip IGBT power module,” *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1-P.8, doi: 10.23919/EPE.2019.8914769.

[II] B. Khanzadeh, **C. Tang** and T. Thiringer, “A Study on the Lifetime of Q2L-MMC-DAB’s Switches for Wind Turbine Applications,” *2020 Fifteenth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, 2020, pp. 1-6, doi: 10.1109/EVER48776.2020.9243073.

[III] **C. Tang** and T. Thiringer, “Performance comparison of five-level NPC and ANPC converters in medium voltage drives for hydro power application,” *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021, pp. P.1-P.7.

[IV] **C. Tang** and T. Thiringer, “Lifetime Analysis of Power Switches in a Back-to-back MMC for Variable Speed Hydropower Application”, *The 31st IEEE International Symposium on Industrial Electronics (ISIE)*, 2022. (Accepted)

[V] **C. Tang** and T. Thiringer, “Modular multilevel converter control with using a general space vector PWM method in medium voltage hydro power application”, *2022 24rd European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, 2022. (Accepted)

[VI] **C. Tang**, J. Zhao and T. Thiringer, “Circulating Currents and Losses Analysis of a MMC with using SVM-based Common Mode Voltage Reduction Strategy for Wind Turbine Application”, *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022. (Accepted)

Acknowledgments

First of all, I would like to express my sincere thanks to Professor Torbjörn Thiringer, my supervisor and examiner, who showed great patience and support to me along this path. It is always a pleasure to have conversations with you regarding different topics. You have been such a nice teacher for showing me the spirit of being curious about everything.

I would also like to thank Professor Massimo Bongiorno, Dr. Mebtu Bihonegn Beza for the discussions about the modelling of the MMC converter. Thank Associate Professor Peiyuan Chen for the discussions about the back-to-back converter control and hydro power generation.

Thank Dr. Junfei Tang, Dr. Douglas Jutsell Nilsson, Dr. Zeyang Geng, and Babak Alikhanzadehalmadari for all the discussions about the measurements and the help with the experimental set-up.

Finally, I would like to thank European Union's Horizon 2020 research and innovation programme, this thesis has received funding under grant agreement No. 764011.

Acronyms

AC:	Alternating Current
ANPC:	Active Neutral Point Clamped
B2B:	Back to Back
CFSM:	Converter Fed Synchronous Machine
DBC:	Direct Bond Copper
DC:	Direct Current
DFIM:	Double Fed Induction Machine
FEM:	Finite Element Method
FFT:	Fast Fourier Transform
HVDC:	High Voltage Direct Current
IEA:	International Energy Agency
IGBT:	Insulated Gate Bipolar Transistor
IM:	Induction Machine
MMC:	Modular Multilevel Converter
MV:	Medium Voltage
NPC:	Neutral Point Clamped Converter
PWM:	Pulse Width Modulation
RMS:	Root Mean Square
SM:	Synchronous Machine
SVM:	Space Vector Modulation
THD:	Total Harmonics Distortion
VSC:	Voltage Source Converter

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CHAPTER 1

Introduction

1.1 Background

Renewable energy, such as wind power and solar power, plays an important role in reducing greenhouse gas emissions. Unfortunately, renewable energy also brings fluctuations in power production due to its intrinsic characteristics. Therefore, to facilitate the integration of renewable energy into the grid, flexible energy storage methods are needed. One of the solutions for energy storage is to employ the century-old pumped-storage hydropower technology. Fig. 1.1 illustrates the layout and components of a typical pumped-storage facility.

By utilizing the variable speed operation in the pumped-storage hydropower technology, the flexibility of the system can be increased [1]. The key component in the variable speed operation is a power electronic converter, which is the interface between the hydro generator/motor and the grid. Due to the frequent changes in the weather conditions, the power generation from

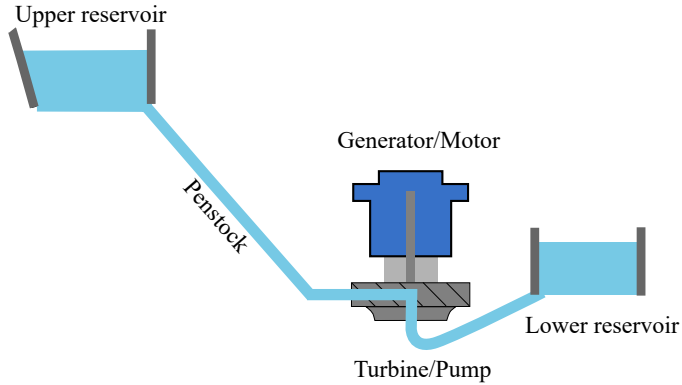


Figure 1.1: The layout of the pumped-storage hydropower facility

the wind varies rapidly, and frequent start-stops need to be implemented in the pumped-storage hydropower unit to cope with this variation to keep the electrical grid balanced.

One of the most commonly used converter topologies in industrial applications is the two-level converter. However, for the medium voltage (MV) application, in which the nominal system voltages are greater than 1 kV and less than 100 kV [2], it is a challenge to use the two-level converter due to the constraints of voltage and current ability of the power switches. Besides, the current and voltage total harmonic distortions (THDs) are quite high in the two-level converter system, which means the increased cost for additional filters in the set-up. Therefore, a multi-level converter is preferable in such MV applications.

In this study, different multilevel topologies, such as the neutral-point-clamped (NPC) converter topology and the modular multilevel converter (MMC) topology, are investigated. The NPC converter was introduced in [3] in the year 1981, and since then, it has been more and more applied in high-power medium voltage applications [4]. The modular multilevel converter (MMC) topology was introduced in [5] in year 2003, and it has been successfully applied in voltage source converter high-voltage direct current (VSC-HVDC) transmission systems, and now it is being used in medium voltage variable speed drives as well [4]. Various researchers have conducted researches about these con-

verters from different aspects, however, it is hard to find one research that contains the comparison with different converter topologies with considering the modulation, efficiency, and lifetime aspects for the variable speed pumped-storage hydropower application. For example, Yazdani *et al.* [6] studied the back-to-back connected NPC converter with variable speed operation, however, the application is for a wind power unit. Phil and Colin [7] calculated the power losses inside an MMC, yet the lifetime of the power switches was not determined, and the application is for an HVDC application. Lv *et al.* [8] analyzed the reliability and lifetime of an MMC in a hydropower application, however, the back-to-back configuration of the converter is not included, and the variable speed operation of the system is not considered.

1.2 Aim of the study

The aim of the study is to investigate the modulation, efficiency, and lifetime between two-level and multilevel converters for a hydropower application. Within this target, simulations and experiments are conducted to verify the operation of the selected converters.

1.3 Contributions of the study

- Demonstrating the usefulness of using a lumped parameter thermal model when considerations of the heat spreading and the thermal coupling effect are accounted for.
- Determination of the lifetime of the power switches inside a back-to-back MMC in a hydropower application.
- Quantifying the switching loss and conduction loss of various converters at various power levels.
- Verifying the usefulness of using a general space vector modulation method for the MMC, along with the circulating current control and the submodule voltage balancing.

2.1 General introduction to hydropower generation

Hydropower is one of the oldest and largest renewable energy sources. Based on the International Energy Agency (IEA), hydropower generation reached 4418 TWh by the end of the year 2020, and the amount of generation is more than all other renewable technologies combined [9]. In addition to that, hydropower shows great potential in the future. The average annual generation growth rate of hydropower between 2020 and 2030 is expected to be 3%, according to the Net Zero Emission by 2050 Scenario [10]. To meet the target generation growth rate, an average new capacity of 48 GW of hydropower should be installed in the aforementioned period.

Hydropower technologies generate power by using the elevation difference of the water, and a general expression for the generated power P is

$$P = \eta\rho gQH \tag{2.1}$$

where η is the overall efficiency of the system, ρ is the density of the water, Q is the flow rate of the water, and H is the net head of the system.

The hydropower facilities are usually divided into three categories: impoundment, diversion, and pumped-storage. An impoundment facility employs a dam to store water in a reservoir, and the electricity is generated by releasing the water from the reservoir through a turbine to spin the generator. The diversion facility channels a portion of a river through a penstock to generate the electricity with the hydro turbine and generator. The pumped-storage facility works like a giant “battery” with using two reservoirs, and the electricity can be stored when the water is being pumped from a lower reservoir to an upper reservoir.

The pumped-storage hydropower is the main focus of this study, due to its flexibility to integrate the other renewable energy sources, like solar and wind power. As described in the introduction part, to cope with the fluctuations of the electricity generation of the other renewable energy sources, the pumped-storage hydropower facility needs to be switched frequently between generation mode and pumping mode.

2.2 Variable speed operation

Traditionally, under generation mode, pumped storage hydropower operates with a fixed speed; however, it is found that variable speed operation can bring several advantages to the system over fixed speed operation [1], and one of the important advantages of variable speed operation is the higher overall efficiency of the system [11][12], particularly for the cases with the varying flow or head. The benefit of using variable rotor speed for a Francis turbine is illustrated in Fig. 2.1, in which the efficiency hill chart of a normalized reaction Francis turbine is presented.

If the turbine is operated at a fixed speed, when the normalized flow rate Q'_1 decreases, the operation point of the turbine shifts from point A to point B, and the efficiency of the turbine decreases. However, if the turbine is operated in variable speed mode, then, instead of shifting to point B, the turbine can shift to point C, which gives higher efficiency than in point A. Higher efficiency means lower losses in the system, and it brings more profit to the stakeholders

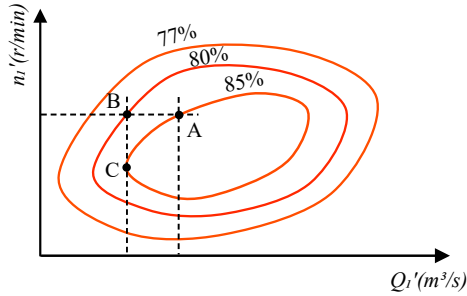


Figure 2.1: Efficiency hill chart of a normalized Francis type reaction hydro turbine

in return.

To achieve variable speed operation of a pumped-storage hydropower facility, modern power electronic converters are needed, and there are two dominating configurations. The first one is the double-feed induction machine (DFIM) configuration, and the second one is the converter feed synchronous machine (CFSM) configuration.

2.2.1 DFIM configuration

The DFIM configuration uses an induction machine (IM) as the generator or motor, and the stator of the IM is connected with the grid directly, while the rotor of the IM is connected to a power electronic converter via slip rings. The layout of the DFIM configuration is shown in Fig. 2.2, in which the transformer on the grid side is omitted. The DFIM configuration has been widely used in hydropower applications to achieve variable speed operation.

The variable speed operation of the DFIM configuration is achieved through the frequency control of the rotor current, and the operation principle of the DFIM is described in detail in [13]. Typically, for a $\pm 10\%$ speed variation, a power electronic converter with a rating that does not exceed 30% of the nominal power is needed [1]. The drawback of the DFIM configuration is the limitation in the rotor power makes the accessible speed range and starting torque of the system rather low [14].

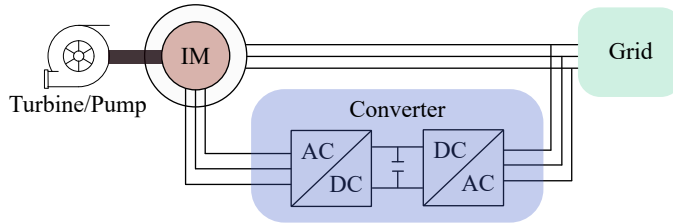


Figure 2.2: DFIM configuration

2.2.2 CFM configuration

The CFM configuration uses a synchronous machine (SM) as the generator/motor, and the layout of the CFM configuration is shown in Fig. 2.3, in which the transformer at the grid side is not shown. The first CFM with a rated power of 100 MVA was installed in Grimsel 2 in Switzerland [15].

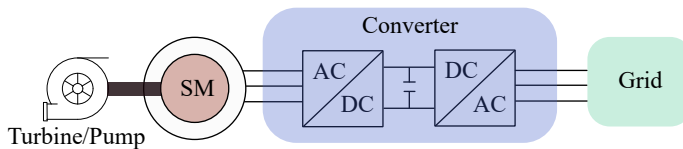


Figure 2.3: CFM configuration

In the CFM configuration, the stator of the SM is connected to the grid via a power electronic converter. The power electronic converter has two voltage source converters (VSC) which are back-to-back (B2B) connected. As depicted in Fig. 2.3, the synchronous machine is decoupled with the grid, and with the control of the two VSCs, a wide range of variable speed operations is achieved. In contrast to the DFIM configuration, the CFM configuration needs full-size converters, and when considering the size and investment of the converter, it is more suitable for the hydropower application with low power ratings. A typical value of the power rating is 100 MVA [12], and with the

development of the power semiconductors and converter topology, this power rating can be pushed to a higher value.

In [14], the benefits of the CFM configuration over the DFIM configuration have been introduced, such as the rapid start-up and large variable speed range. However, the utilization of the full-size converter introduces more losses into the system. The focus of this study is to investigate the losses of the converter when using the CFM configuration, with potential methods to lower the losses. Furthermore, by using the multilevel converter topology, the voltage rating of the system can be increased by using the available power switches, showing the possibility of making the system transformerless, thus, lowering the total investment.

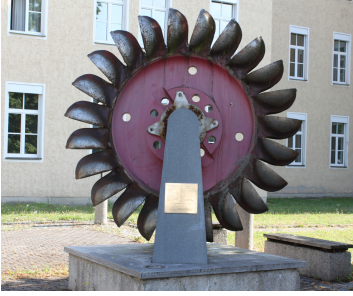
2.3 Hydro turbine and pump

In hydropower applications, based on the energy at the inlet, the hydro turbines are usually classified into two categories: impulse turbines and reaction turbines [16]. For the impulse turbine, the energy is generated by using the velocity of the water to move the runner, and the water is being discharged at atmospheric pressure. A typical type of impulse turbine is the Pelton turbine, and it is shown in Fig. 2.4a. For the reaction turbine, the energy is generated from the combined force of pressure and moving water. One of the most common types of reaction turbine is the Francis turbine in Fig. 2.4b. In pumped-storage hydropower applications, reversible Francis turbine-pumps are commonly used [17].

One of the main parts inside the Francis turbine is the runner, and the function of the runner is to transform the available hydraulic power into rotating mechanical power. The Euler equation

$$\rho Q(u_1 c_{u1} - u_2 c_{u2}) = T\omega \quad (2.2)$$

can be used to describe this power transformation [20], where u_1 and u_2 are the turbine runner's peripheral speeds at the inlet and outlet respectively, c_{u1} and c_{u2} are the water's absolute velocity component in the peripheral speed's direction, T is the shaft torque of the turbine, and ω is the angular speed of the turbine. Considering the guide vane opening, pressure, water flow,



(a) A Pelton turbine [18]



(b) A Francis turbine [19]

Figure 2.4: Two types of hydro turbines: Pelton and Francis

and rational speed, the dimensionless turbine equations are derived in [20]. Fig. 2.5 depicts the model based on the dimensionless turbine equations [21]. The inputs to the model are the turbine opening κ , turbine speed ω , and water head H . H is assumed to be a constant value of 1 in this study. The output of the model is the mechanical output power of the turbine P_m .

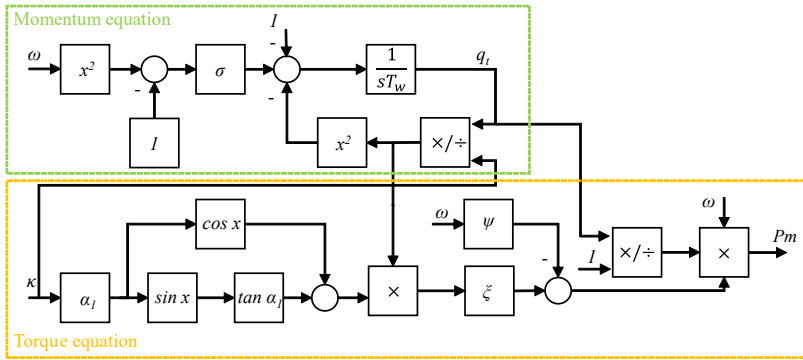
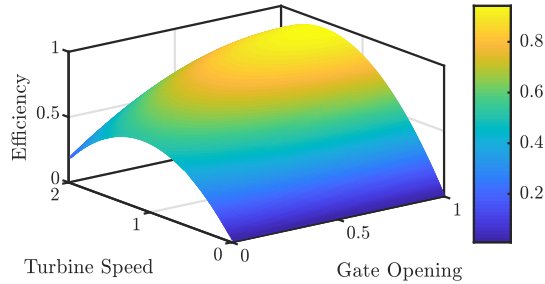


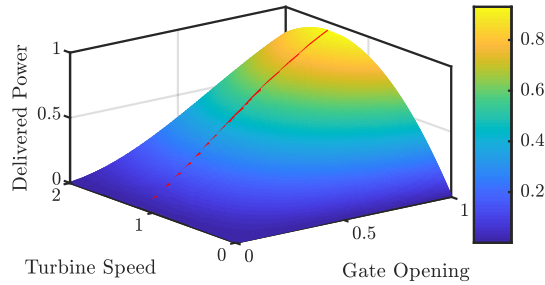
Figure 2.5: Turbine model based on Euler equations with a constant water head $H = 1$ [21]

Based on the turbine model in Fig. 2.5, an efficiency map and a power delivery map of the turbine model are shown in Fig. 2.6. The red line in Fig. 2.6b represents the maximum efficiency operating points of the turbine. In general,

these two maps can be used to determine the reference speed and torque for the electric machine control. When a certain amount of power delivery is commanded from the grid, the corresponding turbine speed and gate opening is acquired from Fig. 2.6b based on the maximum efficiency points. Then, the reference speed and torque are calculated and fed into the controller of the electric machine.



(a) Efficiency map of the variable speed Francis turbine model



(b) Power map of the variable speed Francis turbine model

Figure 2.6: The 3D map of the used variable speed turbine model: (a) Efficiency map. (b) Delivered power map, the red line denotes the path for maximum efficiency under the same power level.

With reverse rotating, the Francis turbine can work as a centrifugal pump,

and it obeys the following pump laws

$$\left\{ \begin{array}{l} Q \propto n \end{array} \right. \quad (2.3)$$

$$\left\{ \begin{array}{l} H \propto n^2 \end{array} \right. \quad (2.4)$$

$$\left\{ \begin{array}{l} P \propto n^3 \end{array} \right. \quad (2.5)$$

where n is the rotation speed of the pump, Q is the flow rate of the pump, H is the head developed by the pump, and P is the pump power. For the pumping mode operation, the pump should work around the best efficiency point for different speeds, then, the corresponding power can be calculated based on the equation (2.5).

Converter topology, modulation, and control

3.1 Converter topologies

Voltage source converters are commonly used in the studied hydropower application with a CFMS configuration. The VSC can convert a fixed DC voltage to a three-phase voltage with variable magnitude and frequency, by switching on and off of the power switches. The back-to-back connection of two VSCs with one common DC-link forms the essential part of the converter in Fig. 2.3 of the studied application.

The medium voltage VSC plays an important role in the market due to its high power density, good efficiency, and high reliability [22]. Typical medium voltage converter topologies are the two-level converter, the neutral point clamped (NPC) converter, and the modular multilevel converter (MMC). The latter two converter topologies belong to the multilevel converter family.

3.1.1 Two-level converter

The electric schematic diagram of the two-level converter is shown in Fig. 3.1. If the neutral point of the DC-link capacitors is connected to the ground, then the output voltage of each phase is either $V_{dc}/2$ or $-V_{dc}/2$, and that means the output phase voltage has two levels.

For each switch position in the two-level converter, several power switches may be connected in series and parallel to meet the power and current requirements of the system. For example, if the DC-link voltage is 13 kV, and the rated blocking voltage of used power switch is 3.3 kV, then, the switch S_1 in Fig. 3.1 needs 8 of these power switches being connected in series to withstand the blocking voltage. This number is acquired by using the DC-link voltage 13 kV divided by the recommend blocking voltage 1.7 kV of the switch. For the 3.3 kV power switch, when considering the safety margins, usually 1.7 kV is recommended as the usage of the blocking voltage.

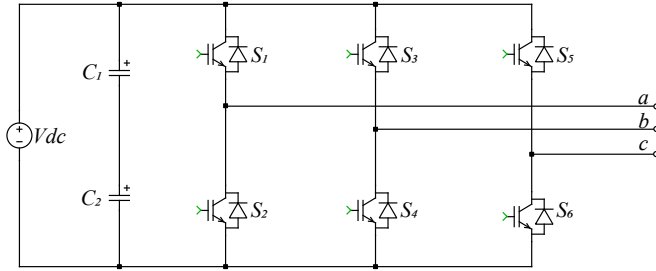


Figure 3.1: Schematic diagram of a two-level converter

3.1.2 Neutral point clamped converter

Neutral point clamped converter topology is the multilevel converter topology that has been firstly studied in this work, and both the three-level and five-level NPC have been investigated. The electric schematic diagram of the three-level and the five-level NPC converter with using the clamping diodes are shown in Fig. 3.2. It can be seen that the structure of the five-level converter is similar to that of the three-level converter.

The benefits of using a multilevel converter include reduced dv/dt and THD in the ac outputs. More importantly, the lower blocking voltage rating power switch could be used directly in one switching position without several in series [4]. However, compared with the two-level converter in Fig. 3.1, the NPC converters need extra clamping diodes.

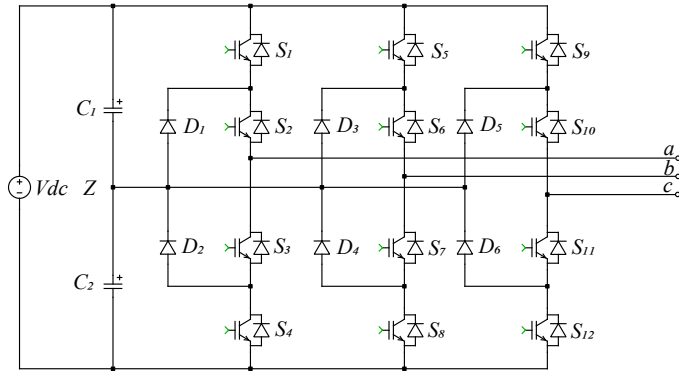
The three-level NPC converter has been practically used in different high-power medium voltage applications, such as in [23] and [24]. The aforementioned pumped-storage hydropower unit installed in Grimsel 2 in Switzerland employs the three-level NPC converter as well [15]. In terms of the five-level NPC converter, the research in [25] shows the feasibility of using it in a medium voltage drive of a kite tidal power application.

3.1.3 Modular multilevel converter

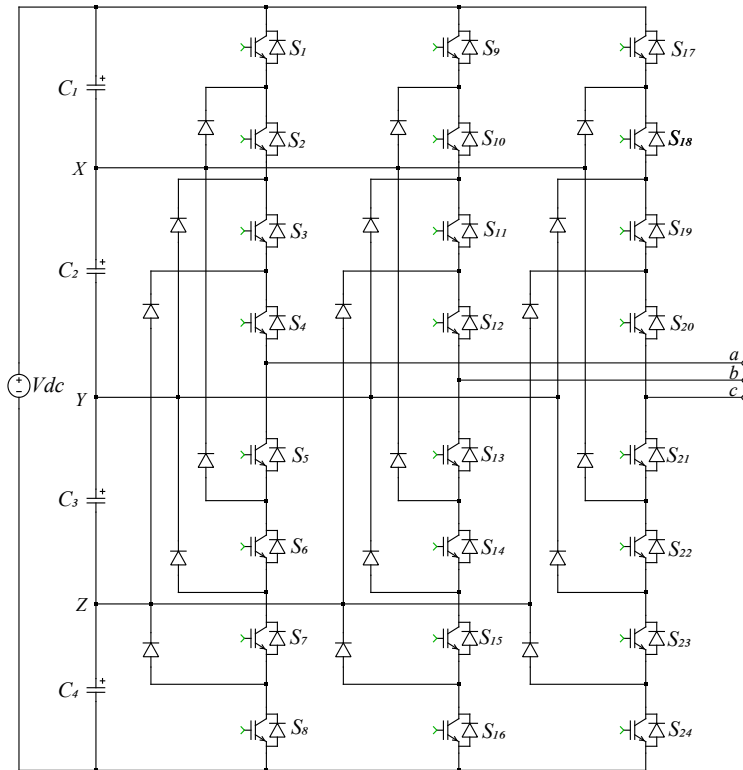
The other multilevel converter topology that has been studied in this work is the MMC topology. The schematic diagram of the MMC is shown in Fig. 3.3, and it is similar to that of the two-level converter with 6 arms. For a $n + 1$ level MMC, each arm of the MMC consists of a n number of submodules and one arm inductor L_0 . The presence of the arm inductor in the circuit can prevent inrush current [4], and it can limit the circulating current as well.

The studied submodule is a half-bridge IGBT submodule, which has shown the lowest losses and the lowest cost in HVDC applications [26]. The half-bridge submodule consists of two IGBT-diode switch pairs and one capacitor, and the two IGBTs in the half-bridge SM are being switched in complementary mode. The submodule can be inserted into or bypassed from the circuit, depending on the switching states of the two IGBTs. In Fig. 3.4, these two states of the submodule are shown.

When the upper IGBT1 is being turned on, and the current is flowing in the direction shown in Fig. 3.4a, the submodule will be inserted into the circuit, and thus, the submodule capacitor will be discharged. If the current direction is opposite to that in Fig. 3.4a, the submodule can still be inserted into the circuit with the current flowing through the freewheeling diode Diode1, and the submodule capacitor will be charged instead. When the lower IGBT2 is being turned on, the submodule is bypassed from the circuit, and the submod-



(a) Schematic diagram of a three-level NPC converter



(b) Schematic diagram of a five-level NPC converter

Figure 3.2: Schematic diagrams of the NPC converter

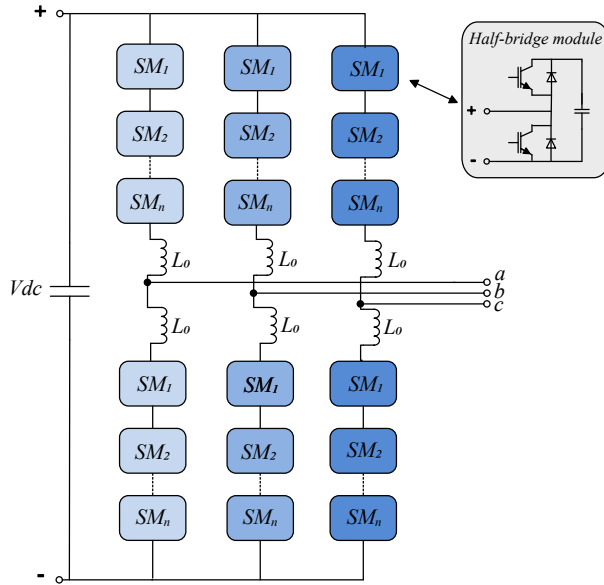
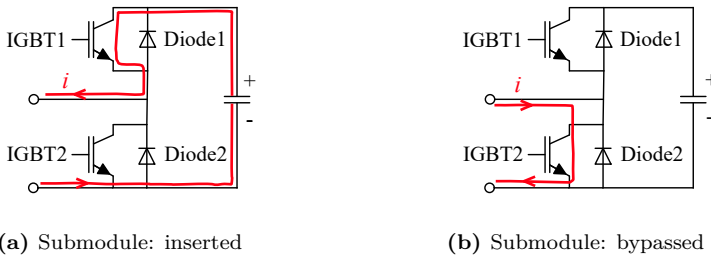


Figure 3.3: Schematic diagram of the MMC topology



(a) Submodule: inserted

(b) Submodule: bypassed

Figure 3.4: PWM carrier wave and modulating waves

ule capacitor voltage will not be affected. The current can flow either through IGBT2 or Diode2 in the bypass state. Prior to the operation of the MMC, the submodule capacitor voltage is usually precharged to V_{dc}/n . The other type of submodules, like the full-bridge submodule or three-level submodule, can be used in the MMC topology as well.

As mentioned in the introduction chapter, the MMC topology has been successfully used in HVDC applications, and it is now being used in drives applications as well. In [27], the control and operating of using the MMC for a medium voltage motor drive are investigated. In [28], the MMC topology was studied in a wind energy conversion system.

3.2 Converter modulation

3.2.1 Modulation for the two-level converter

Pulse width modulation

One of the most commonly used modulation techniques in digital control of VSCs is the pulse width modulation (PWM), in which sinusoidal modulating waves are compared with the triangular carrier waves to generate the gate switching signals for the power switches of the converter. A zero-sequence signal can be injected into the modulating waves in order to increase the amplitude of the fundamental component of the output voltage without causing over-modulation for a given available DC-link. The carrier wave and modulating waves for the normal PWM and the zero-sequence signal injection PWM are shown in Fig. 3.5.

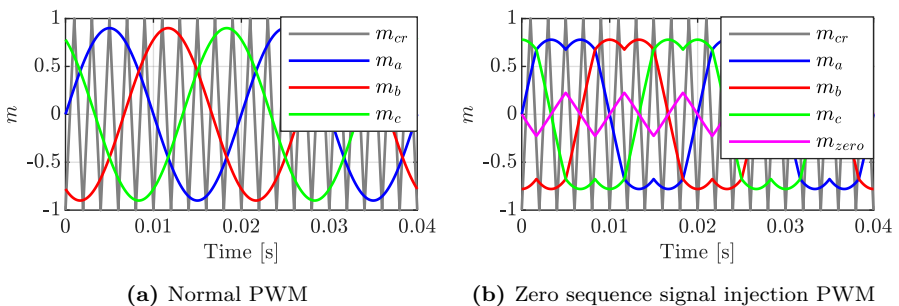


Figure 3.5: PWM carrier wave and modulating waves

Space vector modulation

Space vector modulation (SVM) is another commonly used modulation technique in the digital control of VSCs. The operating status of the switches in the three-phase two-level converter in Fig. 3.1 can be represented by the voltage vectors \vec{V}_0 to \vec{V}_7 states which are shown in Fig. 3.6.

For example, the voltage vector \vec{V}_1 has the switching states [100], which means the upper switch in phase a is ON while the upper switch of the other two phases are OFF. The zero voltage vector \vec{V}_0 has two switching states, [000] and [111].

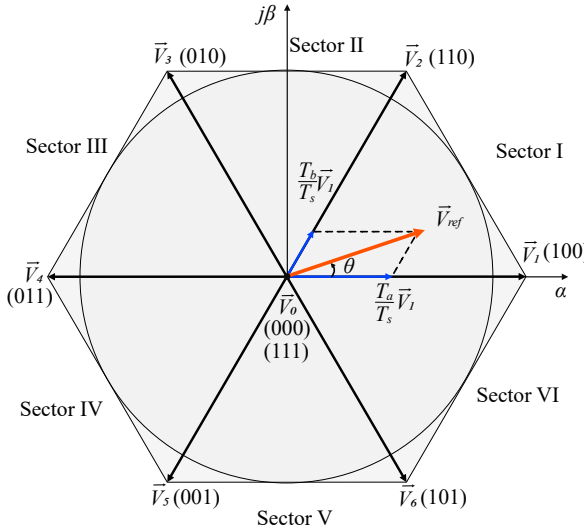


Figure 3.6: Space vector plane for a two-level converter

The space vector plane is in the $\alpha\beta$ coordinates, and it is being divided into six sectors. The three-phase voltage reference signals are firstly being converted to a rotating voltage vector \vec{V}_{ref} in the $\alpha\beta$ coordinates, and then based on the angle θ , the sector number and the small voltage vectors that are used to synthesize the reference voltage vector \vec{V}_{ref} can be determined. For example, the \vec{V}_{ref} in Fig. 3.6 falls in the Sector I, and the three nearest voltage vectors

are \vec{V}_0 , \vec{V}_1 and \vec{V}_2 . The dwell time of each voltage vector are determined by the “voltage-second balancing” principle

$$\begin{cases} \vec{V}_{ref}T_s = \vec{V}_1T_a + \vec{V}_2T_b + \vec{V}_0T_0 & (3.1) \\ T_s = T_a + T_b + T_0 & (3.2) \end{cases}$$

where T_0 , T_a and T_b are the dwell times for the vectors \vec{V}_0 , \vec{V}_1 , and \vec{V}_2 , respectively. In contrast to the PWM modulation, the duty cycle of each switch can be directly calculated based on the dwell times.

When the reference voltage vector falls in the other sectors, by converting the θ to θ' , the reference voltage vector can be treated as in the first sector, and the above process can be applied to get the dwell time of each small voltage vector. The transformation from θ to θ' is shown in Table. 3.1.

Table 3.1: Reference voltage angle transformation

Sector	Angle θ	Angle θ'
1	$(0, \pi/3]$	$\theta' = \theta$
2	$(\pi/3, 2\pi/3]$	$\theta' = -\theta + 2\pi/3$
3	$(2\pi/3, \pi]$	$\theta' = \theta - 2\pi/3$
4	$(\pi, 4\pi/3]$	$\theta' = -\theta - 2\pi/3$
5	$(4\pi/3, 5\pi/3]$	$\theta' = \theta + 2\pi/3$
6	$(5\pi/3, 2\pi]$	$\theta' = -\theta$

3.2.2 Modulation for the multilevel converter

Level-shifted and phase-shifted PWM

PWM modulation can be used for multilevel converters as well, however, usually more than one carrier wave is needed, and the number of the needed carrier waves is determined by the voltage level. Typically, n number of carrier waves can be used to modulate a $n + 1$ level converter. Based on the placement of the carrier waves, the multilevel PWM can be divided into two types, the level-shifted PWM and phase-shifted PWM. In Fig. 3.7, these two PWM types for a five-level converter are shown.

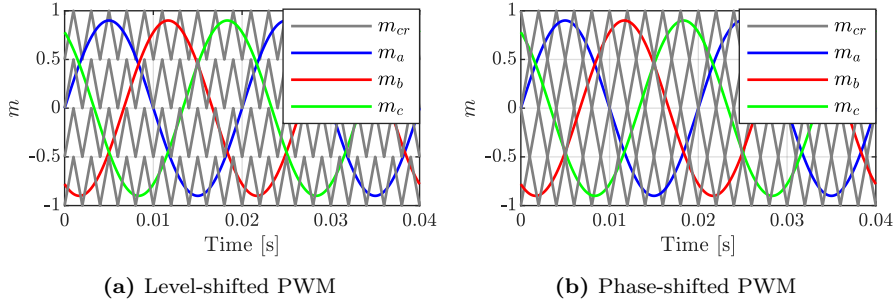


Figure 3.7: Multi-carrier PWM for a five-level converter

The carrier waves in the level-shifted PWM are re-scaled with respect to the n level of the converter, and all the carriers are placed vertically with an offset of $2/n$. The carrier waves in the phase-shifted PWM are still in the range of $[-1, 1]$, however, a phase offset of T_s/n is needed between each carrier wave. For the same multilevel converter, the frequency of the carrier waves in the level-shifted PWM is f_{sw} , while in the phase-shifted PWM is f_{sw}/n .

SVM

SVM can be used for modulating the multilevel converter as well, however, with the increase of the voltage level, the vectors increased drastically. For a $n + 1$ level converter, the SVM has $(n + 1)^3 - n^3$ voltage vectors [29], and Fig. 3.8 shows the space vector plane for a five-level converter.

As can be seen in Fig. 3.8, the SVM for a multilevel converter contains multiple hexagon layers, and for some of the small voltage vectors, more than one switching state can be used to get the same line-to-line output voltage. For example, the small voltage vector \vec{V}_D in Fig. 3.8 contains three switching states: [210], [321], and [432]; and these switching states in one small voltage vector are called redundant states.

The challenge of using SVM for a multilevel converter is to select the suitable switching states to synthesize the reference voltage vector. One way to tackle this issue is to use predefined look-up tables for the switching states in the controller, however, the complex lookup table for storing the switching states

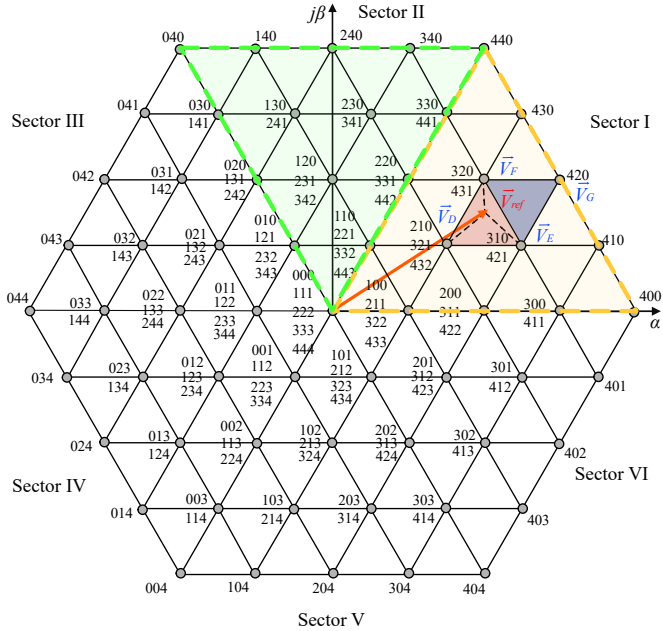


Figure 3.8: Space vector plane for a five-level converter

results in a large burden on the controller memory. In [29], a generalized SVM method for the multilevel converter is proposed, and in [25], this method is being successfully utilized for modulating a five-level NPC converter. The same as for the two-level SVM, this generalized method uses the nearest three voltage vectors in the space vector plane to synthesize the reference voltage vector. The reference voltage \vec{V}_{ref} in Fig. 3.8 can be synthesized by small voltage vectors \vec{V}_D , \vec{V}_E , and \vec{V}_F . The same angle conversion in Table. 3.1 can be used to convert the reference voltage vector which locates in the other sectors to the sector I.

One extra step in the generalized SVM method is the coordinate transformation. The reference voltage vector \vec{V}_{ref} is firstly being normalized with respect to $2V_{dc}/3$ to get v^* , then v^* is being transferred from $\alpha\beta$ coordinates to a 60° coordinates $(\alpha'\beta')$ according to

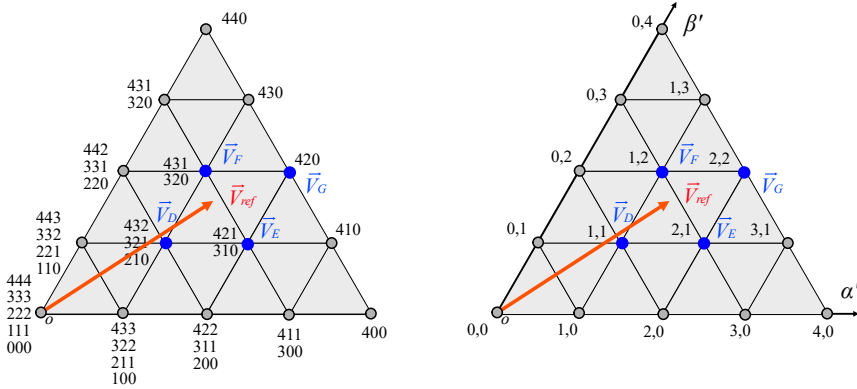
$$\begin{cases} v_{\alpha'} = v^* \cos\theta - \hat{V} \sin\theta / \sqrt{3} \\ v_{\beta'} = v^* \sin\theta \cdot 2 / \sqrt{3} \end{cases} \quad (3.3)$$

$$\begin{cases} v_{\alpha'} = v^* \cos\theta - \hat{V} \sin\theta / \sqrt{3} \\ v_{\beta'} = v^* \sin\theta \cdot 2 / \sqrt{3} \end{cases} \quad (3.4)$$

where v^* is the normalized voltage vector and θ is the vector angle. Once $v_{\alpha'}$ and $v_{\beta'}$ are calculated, the following vectors of the parallelogram $DEFG$ which contains the reference vector in the space vector plane can be calculated,

$$\begin{bmatrix} V_D \\ V_E \\ V_F \\ V_G \end{bmatrix} = \begin{bmatrix} \text{floor}(v_{\alpha'}) & \text{floor}(v_{\beta'}) \\ \text{ceil}(v_{\alpha'}) & \text{floor}(v_{\beta'}) \\ \text{floor}(v_{\alpha'}) & \text{ceil}(v_{\beta'}) \\ \text{ceil}(v_{\alpha'}) & \text{ceil}(v_{\beta'}) \end{bmatrix} \quad (3.5)$$

Fig. 3.9 shows one-sixth of the five-level SVM plane when mapping from $\alpha\beta$ coordinates to $\alpha'\beta'$ coordinates. The next step is to find the three nearest small voltage vectors in $\alpha'\beta'$ coordinates that can be used to form the reference voltage vector. Later, these new small voltage vectors need to be converted back from the $\alpha'\beta'$ coordinates back to the $\alpha\beta$ coordinates based on some transformations. The detailed process is described in [25].



(a) One-sixth of the space vector plane of a five-level MMC (b) Space vector plane converted to 60° $\alpha'\beta'$ coordinates

Figure 3.9: SVM vectors converting from $\alpha\beta$ coordinates to $\alpha'\beta'$ coordinates

For the multilevel NPC converter, the above SVM method can be used directly, whereas, for the MMC, a modification of the SVM is needed due to the need of a “dual-modulator” for both the upper arm and the lower arm of the MMC. Fig. 3.10 shows the two voltage references for the upper arm (\vec{V}_{ref}) and lower arm (\vec{V}'_{ref}) of the MMC when using the SVM modulation. The two voltage references rotate in the same direction with a phase-shift of 180° .

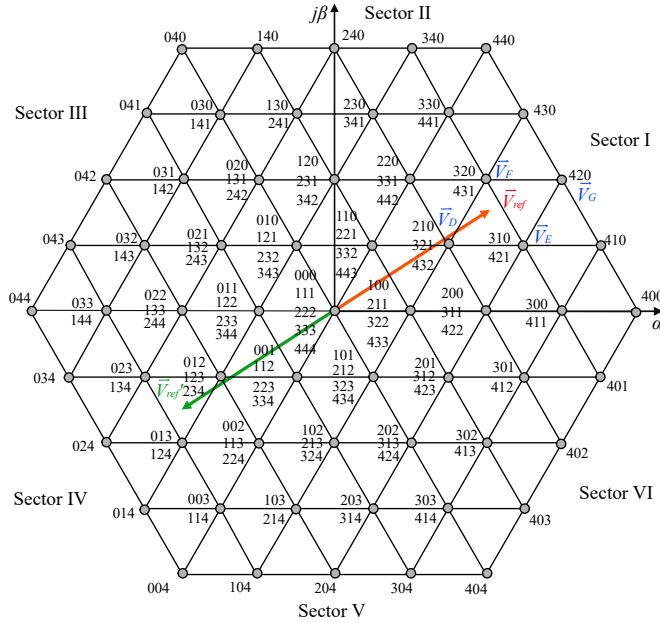


Figure 3.10: Dual voltage reference of SVM for MMC

By using the aforementioned generalized SVM method, the small voltage vectors for synthesizing the upper arm reference voltage can be determined. For the lower arm, there are two ways to determine the small voltage vectors. The first way is to use the voltage vector $[nnn]$ minus the corresponding upper arm small voltage vectors, where n is the number of submodules in each arm. For example, for the five-level MMC with 4 submodules in each arm in Fig. 3.10, if the small voltage vectors for \vec{V}_{ref} are $[310] \rightarrow [320] \rightarrow [321] \rightarrow [421]$, then the corresponding small voltage vectors for \vec{V}'_{ref} would be $[134] \rightarrow [124] \rightarrow [123] \rightarrow [023]$ in sector IV. However, the drawback of this method

is the output phase voltage level would be limited to $n + 1$ level, thus, the THD in the output current and voltage would be higher. The second way is to use the redundant switching states of the lower arm small voltage vectors. For example, for the same upper arm \vec{V}_{ref} , instead of using vectors [134] -> [124] -> [123] -> [023], the lower arm small voltage vectors can be [023] -> [123] -> [124] -> [134]. It can be seen that the average number of the total inserted submodules in one phase during one switching period T_{sw} would be equal to n , which is 4 for the five-level MMC.

Compared with the SVM modulation for the NPC converter, the SVM method for the MMC takes into account two voltage references and the total number of inserted submodules in one phase. Thus, some modifications to the generalized SVM method need to be done, and the detailed process of using SVM for MMC will be presented in **Paper V**.

3.3 Converter control

3.3.1 Control for CFM configuration

The overall control scheme for the CFM configuration of the pumped-storage power unit is shown in Fig. 3.11, and the controller can be divided into two parts, the upper part in Fig. 3.11 is the machine-side controller, and the lower part in Fig. 3.11 is the grid-side controller. Both the machine-side and grid-side controllers use cascaded PI controllers. In this study, a permanent magnet synchronous machine is used as the generator/motor.

Machine side converter control

The machine-side control contains an outer speed controller and an inner current controller. The output of the speed controller is the q current reference, and the input is the mechanical speed reference which can be acquired from the optimal speed calculation process.

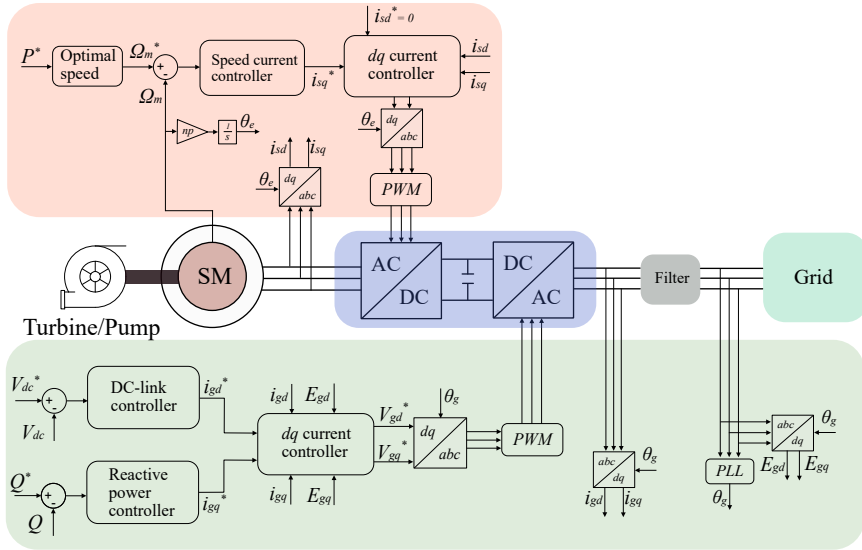


Figure 3.11: The control scheme for CFSM configuration

Grid side converter control

The grid-side control contains the outer DC-link voltage controller and reactive power controller to get the d and q current respectively. An inner current controller generates the reference voltage that is sent to the PWM modulator to get the gate signals for the converter.

3.3.2 NPC control aspects

Neutral point voltage deviation

One of the issues for the NPC converter is the neutral point voltage deviation in the common DC-link. As shown in Fig. 3.2a, the potential of the neutral point Z increases when the current flows into it and vice versa. This can be more intuitively illustrated with the help of Fig. 3.12. When phase a is connected to positive DC-link voltage and phase b and c are connected to

the neutral point of Z , according to the current path in Fig. 3.12, it can be seen that the current will flow from the positive side of C_1 into Z , thus, increasing the potential of the neutral point. A similar analysis can be applied when phase a is connected to positive DC-link voltage and phase b and c are connected to the neutral point of Z , the current will flow out of the neutral point, making the neutral point potential decrease.

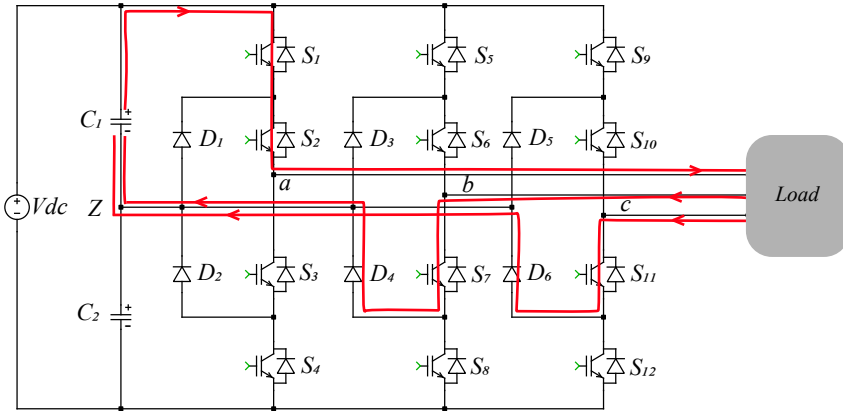


Figure 3.12: Neutral point potential increase due to flow-in current

For the five-level NPC in Fig. 3.2b, the neutral points of X, Y , and Z face a similar issue of voltage deviation.

To deal with the neutral point voltage deviation, different methods have been developed based on different modulations. Fig. 3.13 shows the general solutions for NPC converters that can be used to balance the neutral point voltage [30]. The solutions can be divided into two categories, software-based solutions and hardware-based solutions. For the software-based solutions, by using open-loop or closed-loop control, the modulation signal is being modified to balance the neutral point voltage. For the hardware-based solution, usually, the back-to-back configuration is needed [31], or additional external circuits which work as independent DC-DC converters are needed in the DC-link.

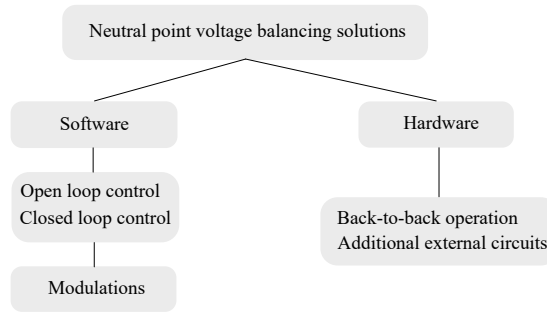


Figure 3.13: Solutions for neutral point voltage balancing in NPC converters

Uneven temperature distribution of NPC

Another issue with the NPC converter is the uneven temperature distribution among the power semiconductors. Fig. 3.14 shows the temperature inside the switches in the upper arm of phase a of a three-level NPC, and it can be seen that the IGBT of the outer switch S_1 has the highest temperature while the diode of the inner switch S_2 has the lowest temperature. This uneven temperature distribution means that some switches inside the NPC converter experience harsher conditions and can deteriorate faster than the other switches.

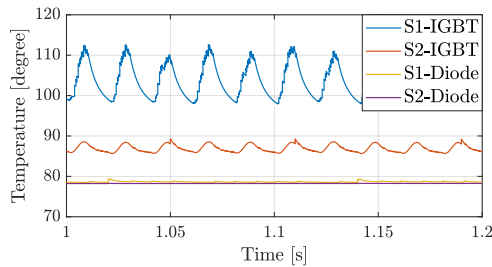


Figure 3.14: The temperature inside the power semiconductors of the NPC converter

To deal with this issue, the active NPC (ANPC) converter was developed [32]. By using active power switches to clamp the neutral point, losses of the switches can be redistributed, and the temperature will be more evenly

arranged among the power switches [4]. However, for the high-level ANPC converter, the modulation gets complicated, while the uneven temperature distribution among the switches is not greatly improved. Furthermore, some of the control methods of the ANPC converter can increase the total loss of the converter, and the results are presented in **Paper III**.

3.3.3 MMC control aspects

Circulating currents

One of the challenges in the MMC control is the circulating currents, and Fig. 3.15 shows the path of circulating currents $i_{circ,j}$ of phase- j in the MMC, where $j = a, b, c$.

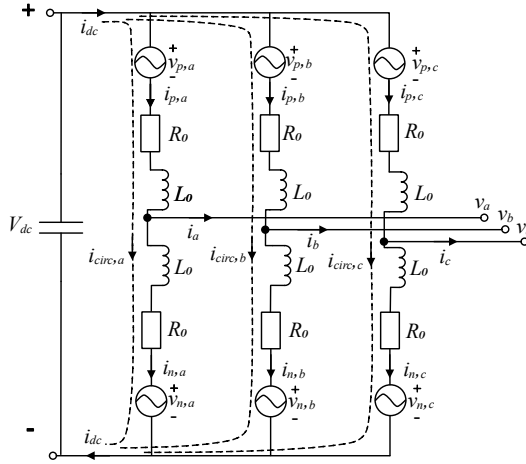


Figure 3.15: Circulating currents path in the MMC

According to the circuit diagram in Fig. 3.15, the upper arm and lower arm currents of phase- j can be written as

$$i_{p,j} = i_{circ,j} + \frac{i_j}{2} \quad (3.6)$$

$$i_{n,j} = i_{circ,j} - \frac{i_j}{2} \quad (3.7)$$

By combining (3.6) and (3.7), the expression of the circulating currents can be derived

$$i_{circ,j} = \frac{i_{p,j} + i_{n,j}}{2} \quad (3.8)$$

For the upper arm and lower arm voltages of each phase, the following equations can be applied

$$\frac{V_{dc}}{2} - v_{p,j} = L_o \frac{di_{p,j}}{dt} + R_o i_{p,j} + v_j \quad (3.9)$$

$$\frac{V_{dc}}{2} - v_{n,j} = L_o \frac{di_{n,j}}{dt} + R_o i_{n,j} - v_j \quad (3.10)$$

where $v_{p,j}$ and $v_{n,j}$ are the total voltages of the inserted submodule in each arm. Combining (3.8), (3.9) and (3.10), the internal dynamics of the MMC circulating currents are expressed by

$$L_o \frac{di_{circ,j}}{dt} + R_o i_{circ,j} = \frac{V_{dc}}{2} - \frac{v_{p,j} + v_{n,j}}{2} \quad (3.11)$$

The circulating currents flow internally among the converter legs, thus, the converter output voltage and current are not being affected [4]. However, the presence of the circulating currents increases the losses of the power switches in each arm, and that reduces the efficiency of the converter. Fig. 3.16 shows the losses comparison between the cases with and without circulating currents for a five-level MMC.

It can be seen from Fig. 3.16 that if the circulating currents are not minimized, the converter would have 40% more total losses. Once the circulating currents are minimized, both the conduction loss and the switching loss can be reduced, and the switching loss reduction accounts for the majority of the total loss reduction.

Equation (3.11) can be used to design the controller for minimizing the amplitude of the circulating currents. In this study, the method of suppressing the circulating current is called double-line frequency circulating current con-

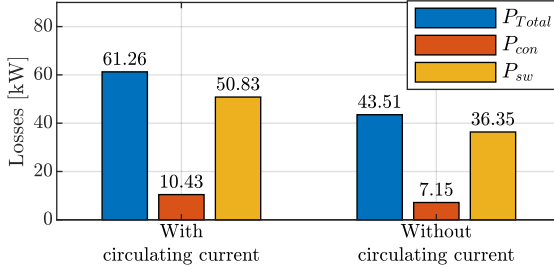


Figure 3.16: Losses for the cases with and without circulating currents

troller [33], and the structure of the controller is shown in Fig. 3.17.

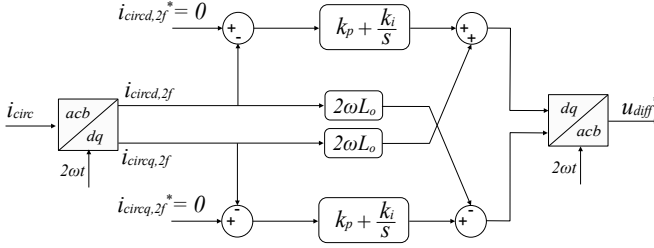


Figure 3.17: The double line frequency circulating current controller

The circulating currents in the MMC are in the form of a negative sequence with the frequency of twice the fundamental frequency, and the circulating currents are firstly transformed from abc to dq coordinates. The PI controller is designed in dq coordinates, and the parameters of k_p and k_i are acquired by using the loop shaping method to have a first-order response of the closed-loop system.

Capacitor voltages in the submodule

The other challenge in the MMC control is the unbalanced capacitor voltages in the submodules. For each submodule capacitor, the voltage of it is alternating around the nominal value V_{dc}/n , which is caused by the charging

and discharging processes due to the energy exchange. However, the submodule capacitor voltages can be unbalanced and deviate from the nominal value during the operation if no active balancing strategy is applied.

Various submodule voltage balancing methods have been proposed by different researchers, such as in [34], [35] and [36]. In this study, the classical sorting and balancing algorithm, which is based on the submodule capacitor voltages comparison and the polarity of the arm currents, is employed at the modulation stage [37],[38]. The balancing principle is, if the arm current is positive, the arm submodule capacitor voltages are firstly sorted in ascending order, then, from the submodule with the lowest capacitor voltage, a certain amount of submodules are inserted into the circuit; the inserted number of the submodule is based on the modulation signal. If the arm current is negative, a similar process is applied, while the order of the sorting for the submodule capacitor voltages is descending. Consequently, the inserted submodule capacitor will be charged or discharged based on the polarity of the arm currents, and the voltage of the corresponding submodule will be increased or decreased, thus, all the submodule capacitor voltages are balanced.

The voltage ripple of each submodule capacitor voltage is another issue in the MMC. The limitation of the voltage ripple impacts the size of the submodule capacitor. For the variable speed hydropower application, the low-speed operation of the machine will increase the voltage ripple, due to the longer charge and discharge process in the submodule capacitor [39]. In this study, the submodule capacitors are assumed to be big enough to limit the voltage ripple, furthermore, the control of circulating currents can help to limit this voltage ripple as well.

Thermal and lifetime modelling

4.1 Thermal modelling

Thermal modelling of the power switches inside the converter contains two parts, the first part is evaluating the losses of the power switch, and the second part is using the thermal network to evaluate the junction temperature T_j inside the power switch. The process for the thermal modelling is shown in Fig. 4.1.

Based on the electrical modelling, the current and voltage of the power switch can be acquired and fed into the thermal model. The junction temperature is thus calculated and being fed back into the loss evaluation process, due to the fact that losses of the power switch depend on the junction temperature. With several iteration processes, the junction can finally reach the steady-state value, and the losses of the power switch are determined.

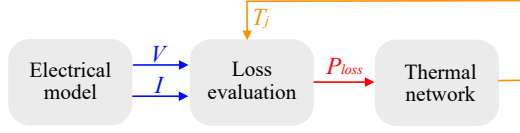


Figure 4.1: The process for thermal modelling

4.1.1 Loss evaluation

It is well known that the total losses inside a power switch consist of two parts: the switching loss and the conduction loss. As described in [40] and [41], the following equations can be used to quantitatively estimate the average conduction losses in the power switch

$$P_{cond,IGBT} = \left(\frac{1}{2\pi} + \frac{m \cos(\varphi)}{8} \right) V_{th} \hat{I}_1 + \left(\frac{1}{8} + \frac{m \cos(\varphi)}{3\pi} \right) R_{on} \hat{I}_1^2 \quad (4.1)$$

$$P_{cond,D} = \left(\frac{1}{2\pi} - \frac{m \cos(\varphi)}{8} \right) V_{th} \hat{I}_1 + \left(\frac{1}{8} - \frac{m \cos(\varphi)}{3\pi} \right) R_{on} \hat{I}_1^2 \quad (4.2)$$

where m is the modulation index, φ is the load angle, V_{th} is the on-state threshold voltage of IGBT and diode, R_{on} is the on-state resistance, and \hat{I}_1 is the fundamental part of the output current. The average IGBT switching loss and the diode reverse recovery loss, per switching period, can be estimated with

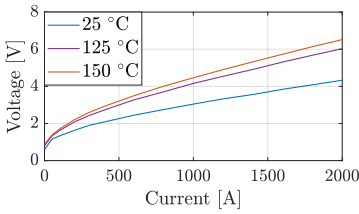
$$P_{sw} = \frac{f_{sw}}{\pi} E_{sw} \left(\frac{\hat{I}_1}{I_{ref}} \right)^{K_i} \left(\frac{V_{cc}}{V_{ref}} \right)^{K_v} \quad (4.3)$$

where f_{sw} is the switching frequency, E_{sw} is the energy dissipated during the switching process, I_{ref} and V_{ref} are the reference current and voltage correlated to the switching losses, V_{cc} is the blocking voltage of the power

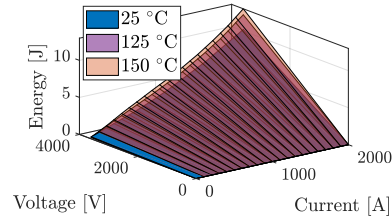
switch, K_i and K_v are the current and voltage dependency of the switching losses.

The parameters used in (4.1) to (4.3) can be determined from the datasheet of the power switches. It is worth pointing out that some of the parameters are temperature dependent, like V_{th} and R_{on} , thus, using the above equations to estimate the losses of the switches may bring some errors when the temperature inside the power switch varies.

Apart from the mathematical equations, the other possibility to estimate the losses inside the power switch is using the loss lookup tables from the datasheet. For the conduction loss, the lookup table contains information about the current and voltage of the power switch under different temperatures. For the switching losses, the lookup table contains the information of the switching energy with different voltage, current, and temperatures. An example of the IGBT turn-on loss and conduction loss lookup tables are shown in Fig. 4.2.



(a) IGBT conduction loss lookup table



(b) IGBT turn-on loss lookup table

Figure 4.2: IGBT turn-on and conduction losses lookup table example in PLECS

4.1.2 Thermal network model

A thermal network model is used to get the junction temperature in the power switch with the feed-in of losses, thus, it is important to have a thermal network model which can represent the reality. In Fig. 4.3, the cross-section view of an IGBT power module is shown, and it can be seen that the power module contains several layers with different materials.

The lumped parameter thermal network model with a heat source is com-

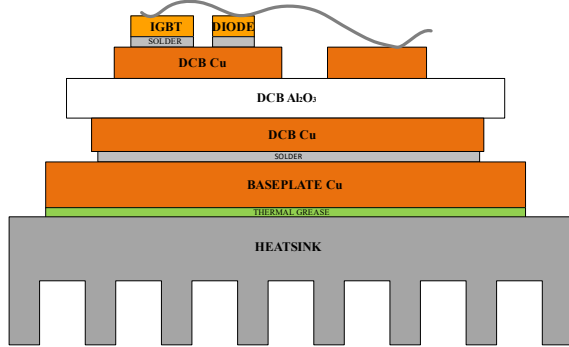


Figure 4.3: Cross-section view of a commercial IGBT power module

only used to model the transient thermal behavior of the power switch. The transient thermal impedance Z_{th} can be quantified with different thermal resistances and capacitances, and is determined by

$$Z_{th} = \frac{T_j - T_c}{P}, \quad (4.4)$$

where T_j is the junction temperature of power semiconductors, T_c is the temperature of the case, P is the losses dissipated from semiconductor chips. There are two types of lumped parameters thermal model network model, the Cauer model, and the Foster model, which are shown in Fig. 4.4a and Fig. 4.4b respectively.

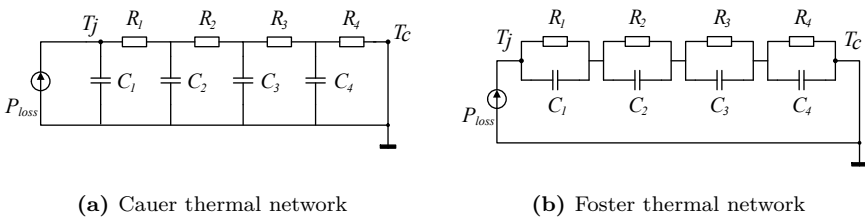


Figure 4.4: Different equivalent circuit thermal models

The Cauer model contains several RC ladders, and each RC ladder represents one layer of the stacked power semiconductors module. The RC parameters in

the Cauer model can be roughly estimated based on the material and geometry of the power switch. The foster model consists of several RC links, while they have no physical meaning. The RC parameters of the Foster network can usually be found in the datasheet of the power switches.

The case temperature T_c in Fig. 4.4 can be assigned with a fixed temperature value that is equal to the ambient temperature, and then the steady-state junction temperature of the power switch T_j under different operating points can be determined with an iterative procedure. In order to have a more accurate T_j , the full set of the thermal parameters from the power switch junction to the coolant is needed. In the datasheet, the thermal parameters from the case to coolant are usually missing, and the finite element method (FEM) can be used to determine these parameters, as long as the geometry of the power switch is known. Fig. 4.5 shows the 3D model of a commercial IGBT power module with a heatsink mounted in COMSOL.

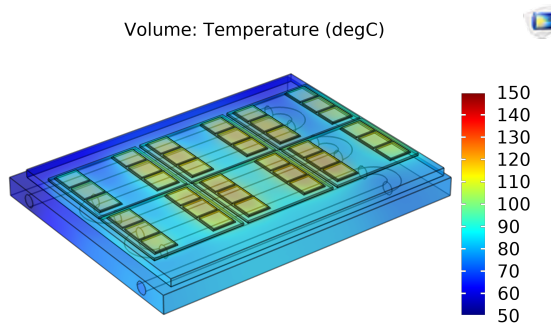


Figure 4.5: Temperature response of the COMSOL 3D simulation

By using multiphysics simulation in COMSOL, the temperature response in the case of the power switch can be acquired; and the thermal parameters from the case to the coolant are thus determined.

4.2 Lifetime modelling

Lifetime estimation is important for the reliability improvement and cost reduction of the power switches, and it has been studied in different applications, for instance, in [42], [43], and [44]. For the power electronic converter built with power semiconductors, it is found that the two major failure mechanisms inside the power devices are bond wire degradation and solder fatigue. According to the study in [45], the thermal cycling stresses in the range of seconds are mainly responsible for the former failure mechanism; while the slow thermal cycling stresses caused by ambient temperature variations are more related to the latter one.

Both the fast and slow thermal cycling stresses can be interpreted from the junction temperature profile of the power switches, and the junction temperature profile can be generated based on the previous thermal modelling process for different operating points. Fig. 4.6 shows the overall process of evaluating the lifetime of the power switches in this study.

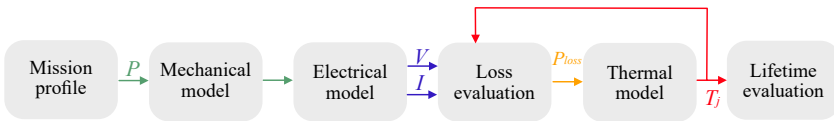


Figure 4.6: Lifetime estimation process

The input to the lifetime estimation process is the mission profile, and an example is shown in Fig. 4.7.

The mission profile defines the operating points of the system for a certain period, thus, the cyclic temperature swings of the power switches which are acquired when feeding the operating points into the previous thermal modelling steps. Fig. 4.7 is the power deployment plan for a 21 MW hydropower unit from [46] with a data sampling rate of 15 mins, and it defines all the operating points of the system for a one-year period. The distribution of the mission profile is shown in the histogram in Fig. 4.8.

It can be seen that for one year period, the studied power unit operates 6233

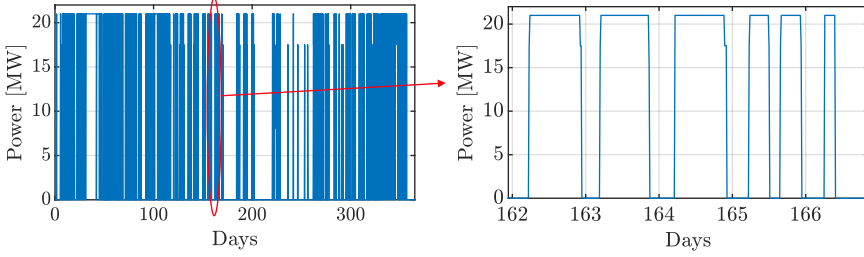


Figure 4.7: Power dispatch plan of the studied hydropower unit

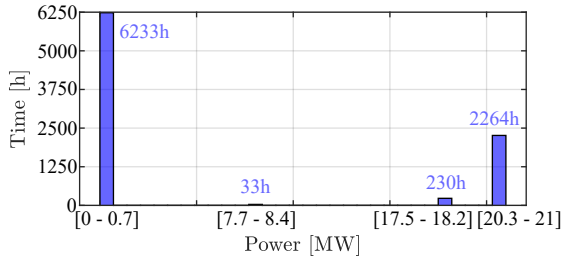


Figure 4.8: Distribution of the mission profile

hours within the range of $[0 - 0.7]$ MW, and 2494 hours within the range of $[17.5 - 21]$ MW.

The mechanical model, electrical model, loss evaluation, and thermal model in Fig. 4.6 have been introduced in previous chapters or sections. The last step in the process is the lifetime evaluation, and it relies on the junction temperature profile of the estimated power switch. What can be interpreted from the junction temperature profile is the thermal stress cycles that have been imposed on the power switch, and the number of different thermal cycles (based on ΔT_j) needs to be counted.

The rainflow counting method [47], which was originally used for fatigue analysis, has become the tool for analyzing and counting the thermal stress cycles for the semiconductors. The cycle counting process is being handled in MATLAB, and once the cycle counts of each thermal cycle are acquired, the next step is to use a lifetime model to find the accumulated damage when running

the corresponding mission profile.

The lifetime model used in this study is introduced in [48], which is developed by Semikron, and is called the SKiM63 lifetime model [49]. The life cycles, N_f , of the switches with respect to the temperature swing, ΔT_j , and the mean junction temperature, T_{jm} , is given by

$$N_f = A \times (\Delta T_j)^\alpha \times (ar)^{\beta_1 \Delta T_j + \beta_0} \times \left[\frac{C + (t_{on})^\gamma}{C + 1} \right] \times \exp\left(\frac{E_a}{k_b \times T_{jm}}\right) \times f_{diode} \quad (4.5)$$

where the parameters are given in Table 4.1.

Table 4.1: Lifetime model parameters

Parameter	Value	Parameter	Value
A	3.4368×10^{14}	α	-4.923
β_1	$-9.012 \times 10^{-3} \text{ 1/K}$	ar	0.31
β_0	1.942	C	1.434
E_a	$6.606 \times 10^{-2} \text{ eV}$	γ	-1.208
k_b	$8.62 \times 10^{-5} \text{ eV/K}$	f_{diode}	0.6204

The accumulated damage D of the switch for one repetition of the mission profile can be determined by Miner's rule,

$$D = \sum_{i=1}^n \frac{N_i}{N_{fi}} \quad (4.6)$$

where N_i can be acquired from the rainflow counting algorithm [47] and N_{fi} can be calculated from (4.5). The inverse of D times the period time of the mission profile gives the lifetime of the power switches. For example, if N_r equals 1, then the switch can only withstand a single run of the considered mission profile, which is 365 days.

Results - converter modulation and control

5.1 Case set-up

This chapter shows the modulation and control results for different converter topologies. MATLAB Simulink simulations have been done for all the converter topologies, and the general boundary conditions of the simulation model are listed in Table 5.1.

Due to the similarity between the machine-side converter and grid-side converter, the simulations of different converter topologies for modulation were conducted on the grid-side converter. The common DC-link voltage was assumed to have a fixed value in the simulation, and a closed-loop controller for the grid-side converter control which has been introduced in Chapter 3 were implemented. For the system-level control of the CFM configuration, the simulation was only conducted in a two-level converter to demonstrate the control concept, and both the machine-side and grid-side control were implemented.

Table 5.1: Boundary conditions for the converter simulation

Parameters	Value	Unit
Power S	6	MVA
Power factor $\cos(\varphi)$	1	/
DC-link voltage V_{dc}	12	kV
Grid phase peak voltage $V_{g,peak}$	5.5	kV
Grid frequency f	50	Hz
PWM frequency modulation ratio m_f	23	/
RL filter Resistance R_f	1.5	m Ω
RL filter inductance L_f	10	mF

Apart from simulation, experimental waveform verification was conducted for a five-level MMC, and the parameters of the experimental set-up will be introduced in Section 5.3.2.

5.2 NPC converter modulation and control

5.2.1 Three-level NPC

The simulation results of a three-level NPC with using the level-shifted PWM and the SVM are shown in Fig. 5.1 and Fig. 5.2 respectively. The results indicate that both the PWM and the SVM work for the three-level NPC converter.

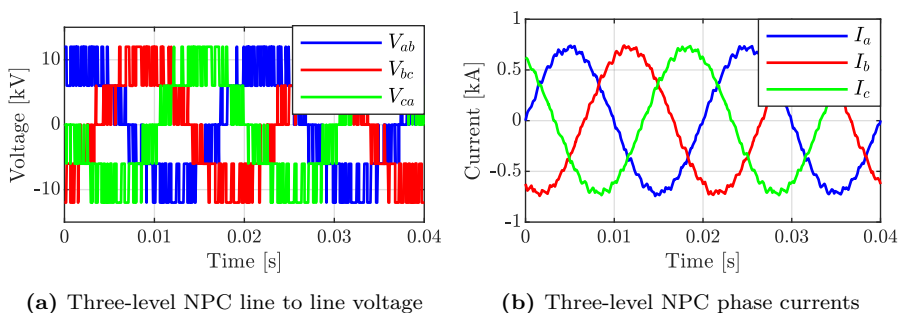


Figure 5.1: Three-level NPC converter with PWM modulation, 100% power

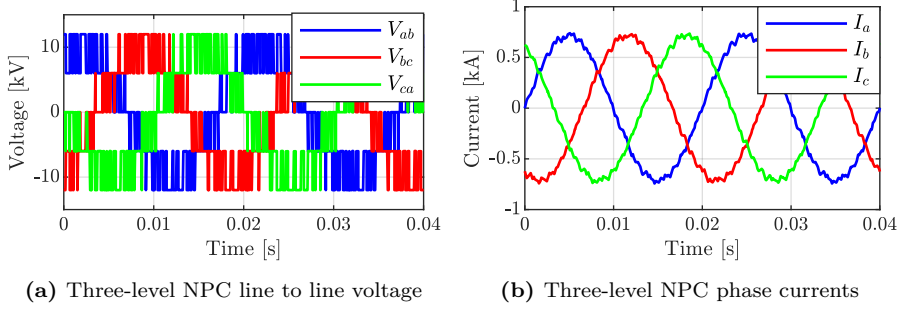


Figure 5.2: Three-level NPC converter with SVM modulation, 100% power

When applying the fast Fourier transform (FFT) analysis on the voltage and current waveforms in Fig. 5.1 and Fig. 5.2, the results of THDs (maximum frequency 10 kHz) are shown in Table 5.2.

Table 5.2: THD results based on FFT analysis - Three-level NPC

THD	PWM	SVM
V_{LL}	36.74%	36.64%
I_{phase}	3.25%	3.23%

It can be seen that the THD results of the PWM and the SVM modulation for the three-level NPC are quite close, and the phase currents THD are less than 5% with the defined boundary conditions.

5.2.1.1 Neutral point voltage control

To illustrate the function of the neutral point voltage control in the three-level NPC, a simulation with activating the neutral point voltage controller at a certain time is conducted. Fig. 5.3 shows the two DC-link capacitors voltage inside the three-level NPC converter, and the neutral point voltage controller is activated at $t = 0.6$ s.

Before $t = 0.6$ s, the upper capacitor is being discharged while the lower one is being charged, which means the neutral point voltage is deviating from the nominal value. After $t = 0.6$ s, with using the software-based neutral point

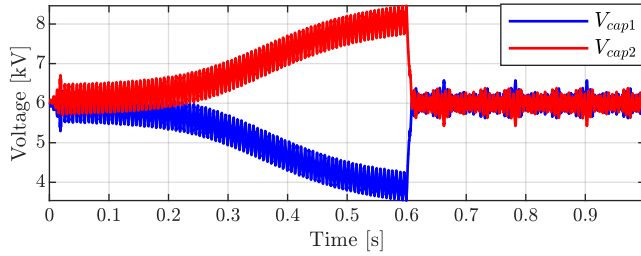


Figure 5.3: Three-level NPC capacitor voltage, neutral point voltage balancing activated at $t = 0.6$ s

voltage balancing method, the capacitor voltages are controlled to the nominal value, and the neutral point voltage is balanced.

5.2.2 Five-level NPC

For the five-level NPC, the simulation results of PWM and SVM are shown in Fig. 5.4 and Fig. 5.5 respectively.

The line-to-line voltages and the phase currents indicate that both the PWM and SVM modulation are applicable for the five-level NPC converter. The same as for the three-level NPC converter, an FFT analysis was applied for the voltage and current waveforms in Fig. 5.4 and Fig. 5.5, the results of THDs (maximum frequency 10 kHz) are shown in Table 5.3.

Table 5.3: THD results based on FFT analysis - Five-level NPC

THD	PWM	SVM
V_{LL}	19.15%	19.02%
I_{phase}	1.41%	1.21%

It can be seen that the THD results of the five-level NPC are greatly improved when compared with the results of the three-level NPC. As shown in voltage waveforms, the line to line voltage of the five-level NPC has more levels, thus, the lower voltages THD are achieved for both the PWM and the SVM modulation. The phase currents THD of the five-level NPC are less than

1.5%, which means the ripple in the phase currents are decreased compared with the three-level NPC. The higher voltage levels mean a lower dv/dt can be seen from the machine winding perspective, and it benefits the machine winding insulation design. The lower current ripple means a smaller filter is needed between the converter and the grid, thus, decreasing part of the total cost. In addition to that, it can be seen the SVM modulation for the five-level NPC can have a slightly better current THD result for the defined boundary conditions.

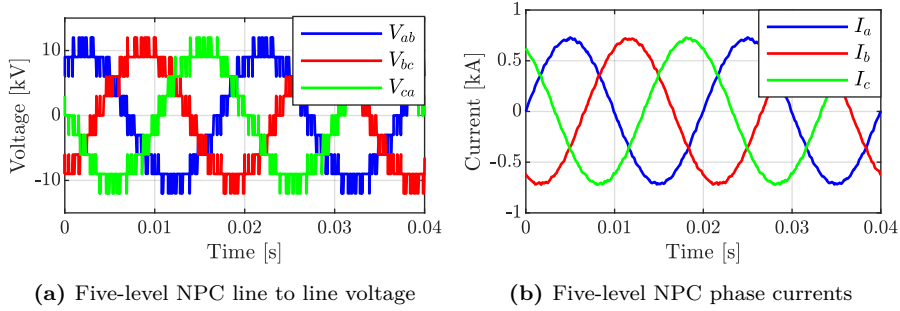


Figure 5.4: Five-level NPC converter with PWM modulation, 100% power

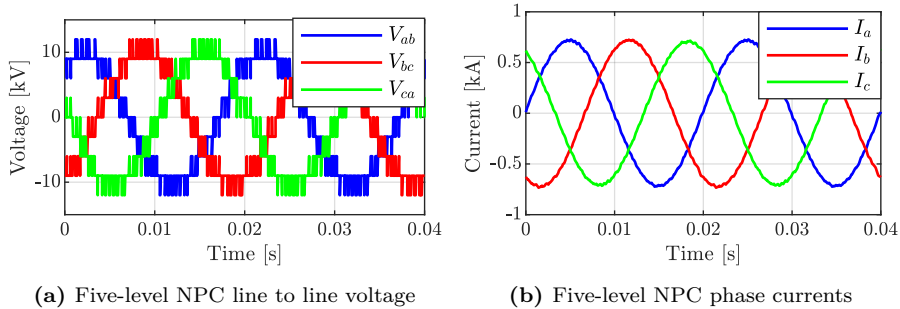


Figure 5.5: Five-level NPC converter with SVM modulation, 100% power

The neutral point voltage balancing in the five-level NPC is based on the hardware method, which means a DC-DC converter is used for each of the DC-link capacitors, and thus, a fixed DC-source is used to represent each capacitor in the simulation.

5.3 MMC modulation and control

5.3.1 Simulation

A five-level MMC was simulated, and the parameters of the submodule and arm inductors are listed in Table 5.4.

Table 5.4: Submodule and arm parameters of the simulated five-level MMC

Parameters	Value	Unit
Number of submodules in each arm N_{SM}	4	/
Submodule voltage E_{SM}	3	kV
Submodule capacitance C_{SM}	1.41	mF
Arm inductance L_{arm}	5	mH

As in the case for the NPC converter simulation, the grid-side MMC using a closed-loop control was modelled. Moreover, the circulating current control and submodule capacitor voltage balancing control were studied as well. The simulation results of the five-level MMC with using the phase-shift PWM and the SVM are shown in Fig. 5.6 and Fig. 5.7 respectively.

It can be seen that the voltages and currents of the MMC follow the reference according to the given power, and both the PWM and the SVM work for the modulation of the five-level MMC. The same as for the NPC converter, an FFT analysis was conducted for the voltages and currents in Fig. 5.6 and Fig. 5.7, and the results of the THDs (maximum frequency 10 kHz) are shown in Table 5.5.

Table 5.5: THD results based on FFT analysis - Five-level MMC

THD	PWM	SVM
V_{LL}	11.74%	12.36%
I_{phase}	1.53%	2.41%

Based on the THD results, when comparing the five-level MMC and the five-level NPC converter, it can be seen that the MMC has a better result of the line-to-line voltage THD, while the phase current THD is slightly worse (PWM modulation). The better result of the voltage THD is due to the $2n+1$

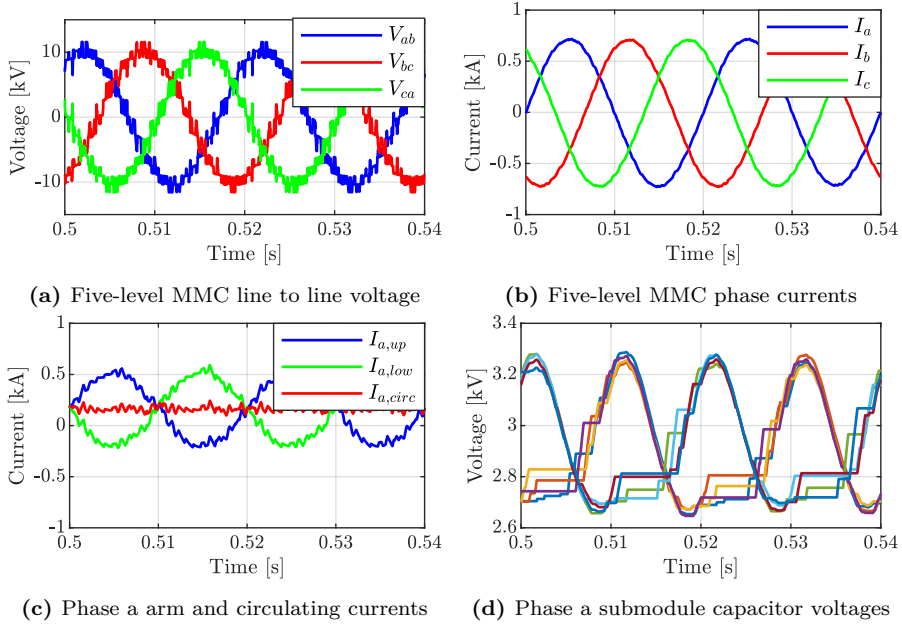


Figure 5.6: Five-level MMC converter with PWM modulation, 100% power

level modulation in the MMC, and this can be clearly seen from the voltage levels in Fig. 5.6a and Fig. 5.4a. The slightly worse current THD is due to the fact that the five-level NPC converter is simulated with a fixed voltage DC source in the common DC-link, while the MMC is not. It can also be seen from Table 5.5 that the simulation results of the MMC for the case of PWM modulation are better than the case of SVM modulation, especially for the phase currents. Nevertheless, for both modulation techniques, the current THDs are less than 2.5%. The waveforms of the circulating currents and the submodule capacitor voltages in Fig. 5.6 and Fig. 5.7 also show that the PWM modulation gives better results than the used SVM modulation. However, the freedom of designing the switching sequence in one switching period in the SVM gives more freedom to the control of the MMC to achieve certain goals. For example, the discontinuous SVM with the five-segment switching states can be utilized to decrease the switching losses in the MMC (will be presented in **Paper V**); the common-mode voltage can be reduced

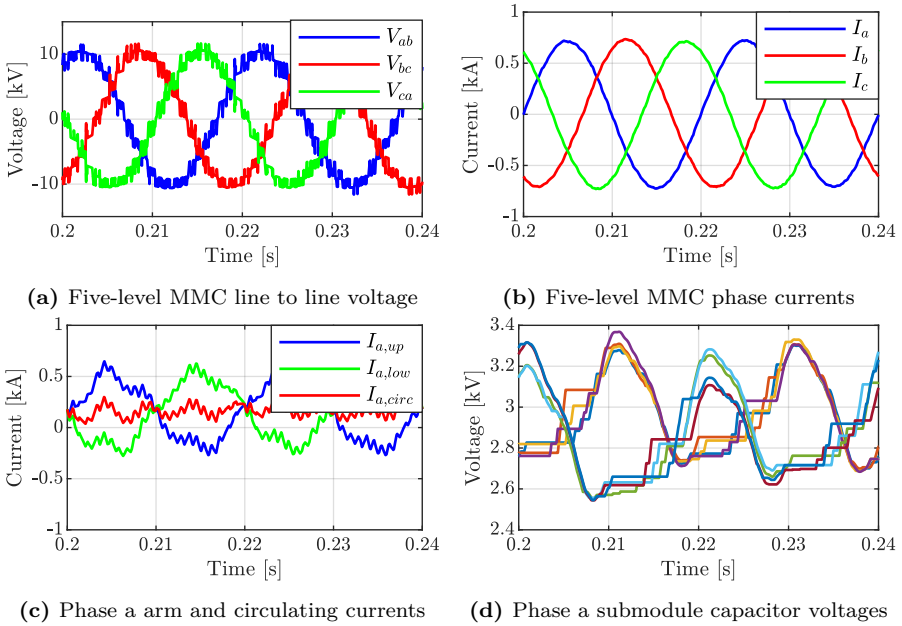


Figure 5.7: Five-level MMC converter with SVM modulation, 100% power

with a well-designed switching pattern (will be presented in **Paper VI**).

The circulating currents in Fig. 5.6c and Fig. 5.7c are controlled with the objective to have a minimum oscillation. It can also be seen that there is a DC component inside the $I_{a,circ}$ based on Equation (3.8), and the amplitude of the DC component is $I_{dc}/3$. This DC current component is used to deliver active power from DC-link to the grid. Fig. 5.8 illustrates the function of the circulating current controller, which is activated at $t = 0.3$ s. The circulating can be successfully suppressed to a minimum oscillation with the defined simulation conditions.

Apart from the circulating currents, another control target in the MMC is the submodule capacitor voltage balancing, and from Fig. 5.6d and Fig. 5.7d, it can be seen that the submodule capacitor voltages are balanced around 3 kV with using the sorting and balancing algorithm.

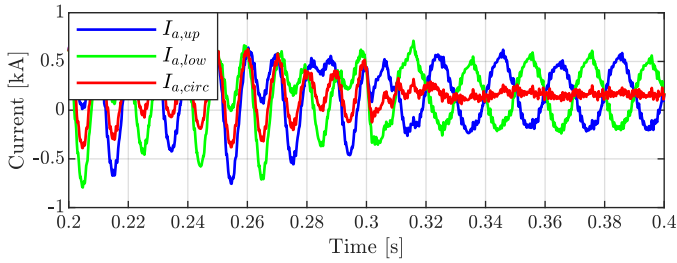


Figure 5.8: Phase a arm and circulating currents, circulating current controller activated at $t = 0.3$ s

5.3.2 Experiment

5.3.2.1 Introduction to the experimental set-up

The experiment focuses on the waveform verification of the MMC converter, and the MMC experimental setup is shown in Fig 5.9.



Figure 5.9: Lab set-up of the MMC: 1) DC power supply 2) MMC 3) Three-phase RL load

The set-up contains three main sections:

1. The DC power supply is from DELTA ELEKTRONIKA, and the model is SM 1500-CP-30. The supply voltage and current range of the DC

power supply are $0 \sim 1500 \text{ V}$ and $-30 \sim 30 \text{ A}$ respectively. In the experiment setup, the DC power supply is used as a 400 V DC voltage source.

2. The five-level MMC cabinet is from Imperix power electronics. More details about the five-level MMC are described in 5.3.2.2.
3. The three-phase RL load, and the parameters are $R = 50 \Omega$ and $L = 28 \text{ mH}$. The three-phase load is being “star” connected.

5.3.2.2 Components of the five-level MMC

The inner part of the five-level MMC cabinet is shown in Fig. 5.10, and the MMC consists of 5 main parts, which can be divided into two main groups.

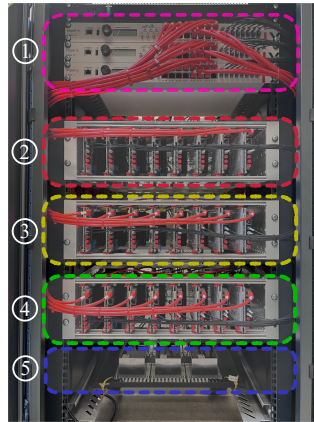


Figure 5.10: Imperix converter cabinet: 1) Controllers 2)Phase a submodules 3) Phase b submodules 4) Phase c submodules 5) Arm inductors

The first group is the controller unit, and the model of the controller is called B-Box RCP. There are three controllers in total in the five-level MMC, and each controller contains 16 channels of PWM outputs. By feeding in the analog inputs to the controller, the PWM outputs can be generated at each sampling time, and in this way, the IGBT submodules are controlled. All the three BB-BOX RCP controllers are synchronized together to control the total 24 IGBT submodules in the five-level the MMC.

The second group is the electrical circuitry, and it contains 24 IGBT submodules and 6 arm inductors. The used IGBT submodule is shown in Fig. 5.11.

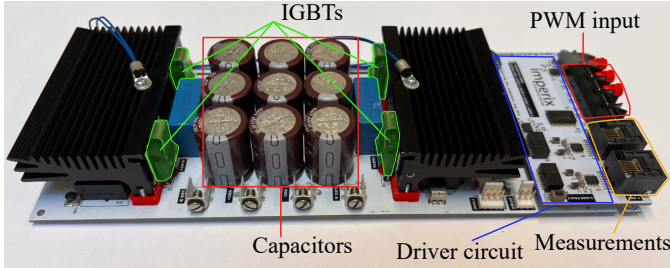


Figure 5.11: The IGBT submodule inside the converter cabinet

The submodule includes $4 \times$ IGBT power switches on the board, forming a “H-bridge”, while only two of the switches are used in the five-level MMC to form the half-bridge submodule. Apart from the power switches, the submodule also includes $9 \times$ *PanasonicEET* capacitors to form the submodule capacitor with a capacitance of 5 mF. The driver circuit, the optical PWM input, and the onboard measurements of the submodule are shown in Fig. 5.11 as well.

In addition to the IGBT submodules, there are 6 arm inductors in the electrical circuitry, which are placed at the bottom side of the converter cabinet, and the inductance is 2.3 mH for each arm.

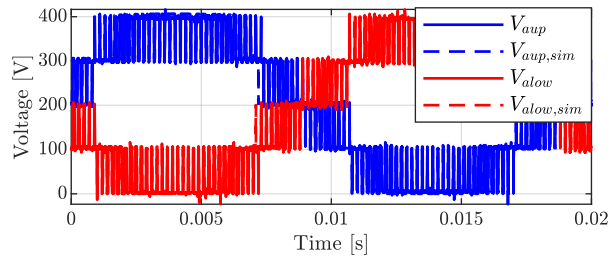
5.3.3 Experimental results of the open-loop control

To demonstrate the working principle of the five-level MMC, an open-loop operation with using PWM modulation is first conducted.

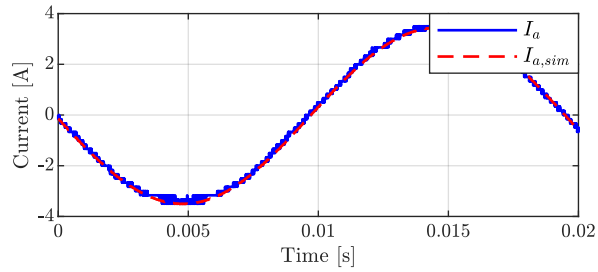
The experimental and simulated results of the arm voltages and current of phase a of the five-level MMC with modulation index $m_a = 0.95$ are shown in Fig. 5.12. The switching frequency of each submodule is 5 kHz.

In Fig. 5.12, it is shown that the experimental results are close to the simulation results, and for $m_a = 0.95$, all the four submodules in each arm are being operated.

The sampled submodule capacitor voltages ($f_{sampling} = 5$ kHz) which are sent



(a) Phase a up and low arm voltages



(b) Phase a current

Figure 5.12: Phase a arm voltages and current, $m_a = 0.95$

to the controller of phase a are shown in Fig. 5.13, and with the implemented sorting and balancing algorithm, all the 8 submodule capacitor voltages are balanced and controlled at the desired voltage level.

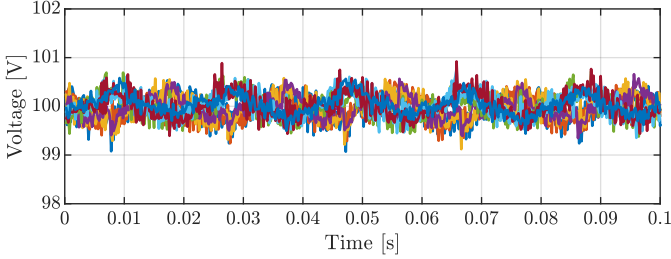


Figure 5.13: Phase a submodule capacitor voltages

The arm currents and circulating current of phase a are shown in Fig. 5.14. The circulating current controller is activated at $t = 0.1$ s, and it can be seen that the oscillations of the circulating current are greatly suppressed with the aforementioned circulating current controller.

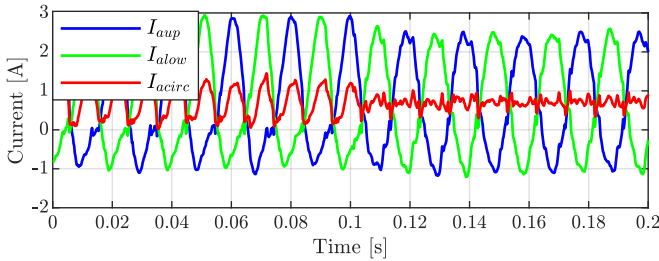


Figure 5.14: Phase a arm currents and circulating currents

5.3.4 Experimental results of the closed-loop control

The following sections show the experimental results when using the closed-loop current control for both the PWM and the SVM modulations. The closed-loop current controller is the classical PI controller which is implemented under dq coordinates. The DC-link voltage is set to be 400 V, which

means each submodule is charged to 100 V. The nominal frequency of the system is set to be 50 Hz.

5.3.4.1 PWM modulation

Fig. 5.15 shows the experimental results when a d current step from 3.5 A to -1.5 A is activated at 0.5 s, and q current reference is set to be zero in the simulation.

In Fig. 5.15a, the magenta curve is the amplitude of the reference current, and it can be seen that the amplitude of the three-phase currents can follow the reference value before and after the reference step. In addition to that, the current response is fast, and this is as expected since the bandwidth of the closed-loop current controller is designed as 1000 rad/s.

In Fig. 5.15b, the circulating current oscillations are minimized both before and after the current step. The DC component inside the circulating current decreases when the amplitude of the reference current is decreased, and this is as expected since the total delivered active power is decreased.

In Fig. 5.15c, the submodule voltages are balanced both before and after the current step. During the current step, the average submodule voltage is increased, and this is due to the higher oscillation inside the circulating current during the transient. Eventually, the average submodule voltage will go back to the reference value, which is 100 V.

5.3.4.2 SVM modulation

Figure. 5.16 shows the experimental results when the SVM modulation is implemented for the five-level MMC. As for the PWM modulation, it can be seen that for both of the current steps, the phase current amplitude can follow its reference value, the circulating currents are minimized, and the submodule capacitor voltages are balanced.

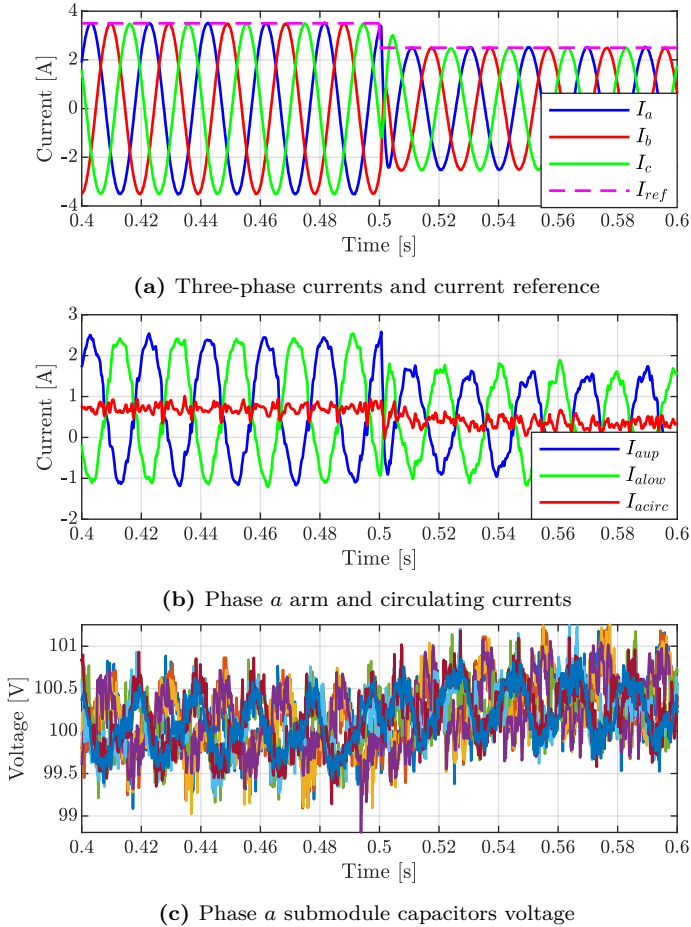


Figure 5.15: Experimental results of PWM modulation with current step: 3.5 A to -2.5 A

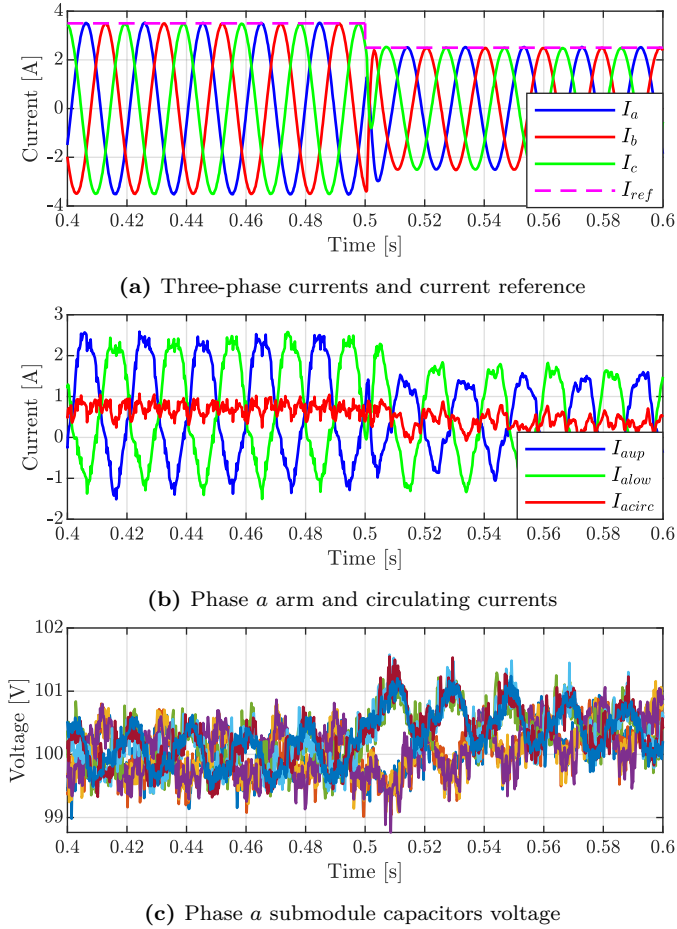


Figure 5.16: Experimental results of SVM operation with current step: 3.5 A to -2.5 A

5.4 Converter control with CFSM configuration

The converter control for the CFSM configuration was simulated in a two-level converter to demonstrate the functionality of the grid-side and machine-side control. PWM modulation was used in the control of the CFSM setup. Both the machine-side controller and grid-side controller were implemented in MATLAB Simulink based on the control theory in Chapter 3.

The synchronous machine, the filter, and the grid model were built using PLECS Blockset. The synchronous machine used in the simulation is a 30 pole-pairs PMSG, and the parameters of the PMSG, along with the parameters of the filter and the grid are shown in Table 5.6.

Table 5.6: The PMSG model parameters

Parameters	Value	Unit
Rated power P_n	2	MW
Rated voltage V_n	690	V
Rated frequency f_n	9	Hz
Rated electrical speed w_n	56.550	rad/s
Pole pairs n_p	30	/
Flux constant Ψ_m	9.962	Wb
Stator resistance R_s	7	m Ω
d-axis inductance L_d	0.806	mH
q-axis inductance L_q	1.5	mH
DC-link voltage V_{dc}	1.5	kV
Filter R_f	0.1	m Ω
Filter L_f	0.1	mH
Rated grid frequency f_g	50	Hz

The control target is to make sure that the CFSM configuration can deliver or absorb the reference power from the grid, and the response of the system should be fast in order to cope with the reference power steps. Furthermore, the DC-link voltage should be kept as the reference value during all the transients. The simulation results are shown in Fig. 5.17.

The input to the simulation model is the machine mechanical reference speed which is acquired from the optimal speed process. As shown in Fig. 5.17a, the speed can follow the reference quite well in the simulation. At $t = 0$ s, the

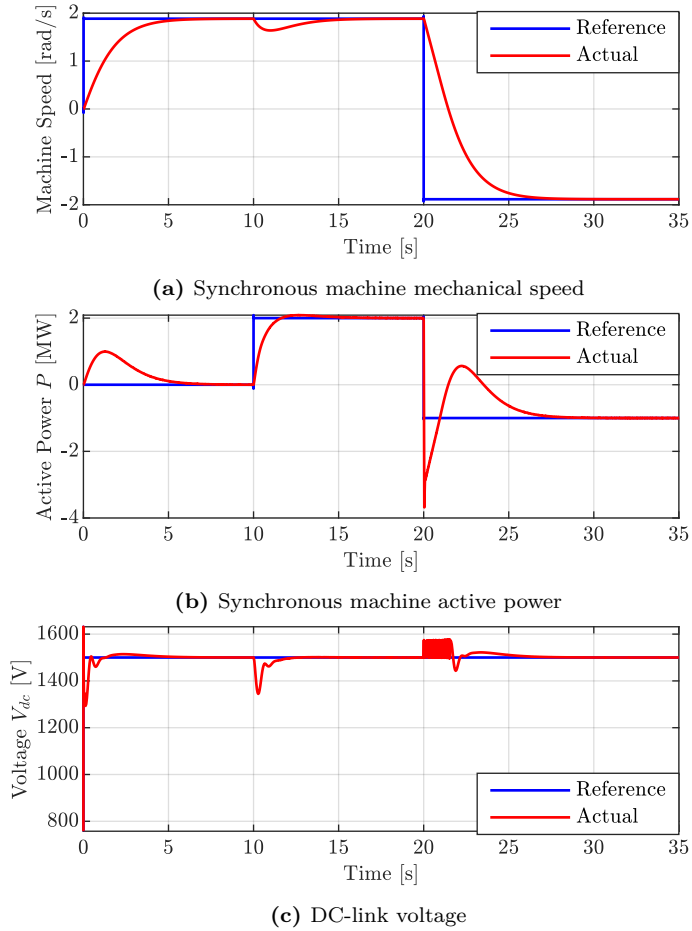


Figure 5.17: Simulation results of a 2 MW two-level converter with the CFM configuration

reference speed is applied, and the machine starts to rotate. However, there is no load applied to the set-up, thus, the active power P delivered from the machine in Fig. 5.17b is 0 when the machine reaches the reference speed. At $t = 10$ s, a load of 2 MW is applied, and it can be seen that the machine speed drops first, then it follows the reference speed again, and the delivered power reaches 2 MW.

At $t = 20$ s, the set-up shifts to pumping mode, and the reference speed changes from the positive nominal speed to the negative nominal speed. In the meantime, the load power changes from 2 MW to -1 MW. The simulation results in Fig. 5.17a and Fig. 5.17b show that the CFSM set-up can handle the transition from “generating” mode to “pumping” mode quite well.

Furthermore, it can also be seen that the DC-link voltage is being controlled at 1.5 kV during all the transitions, and in the time interval of 20 s to 22 s, the DC-link voltage is maintained within the limit by using a DC brake chopper.

In general, the results shown in Fig. 5.17 imply that the control methods introduced in Chapter 4 can be successfully used for the pumped-storage hydropower application.

CHAPTER 6

Results - thermal modelling, losses, and lifetime

6.1 Thermal modelling

Thermal modelling is one important part of this study. To reduce the time and computation burden of the thermal simulation, a Cauer thermal model with considering the heat spreading effect and the thermal coupling effect was developed through FEM simulations. The detailed process is presented in **Paper I**.

6.1.1 Thermal modelling - heat spreading effect

The COMSOL simulation result of a small IGBT chip block is shown in Fig. 6.1a. Interesting to note is that the heat flux (red arrows in Fig. 6.1a) has a spreading effect when flowing from the IGBT chip to the direct bond copper (DBC) substrate. This phenomenon can be illustrated by a simple model in

Fig. 6.1b, where the angle φ is the effective heat spreading angle [50]. Thus, a heat spreading angle need to be considered when using the Cauer impedance network in the PLECS simulation to get the temperature response.

In practice, a heat spreading angle of 40° from [51] can be added to the Cauer model in order to represent the heat spreading effect. In this simulation, in order to match the PLECS simulation result with the FEM simulation result, an angle of 32.5° was selected; the simulation results between the COMSOL FEM model and the PLECS Cauer model are compared in Fig. 6.2. It can be seen that the PLECS Cauer model simulation results are really close to COMSOL results, when a 32.5° heat spreading angle is added.

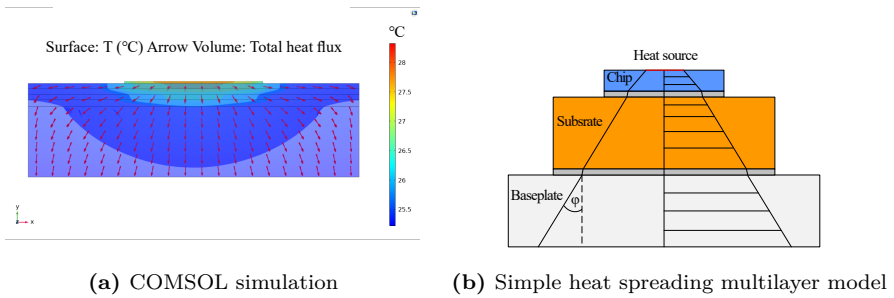


Figure 6.1: Heat spreading effect modelling

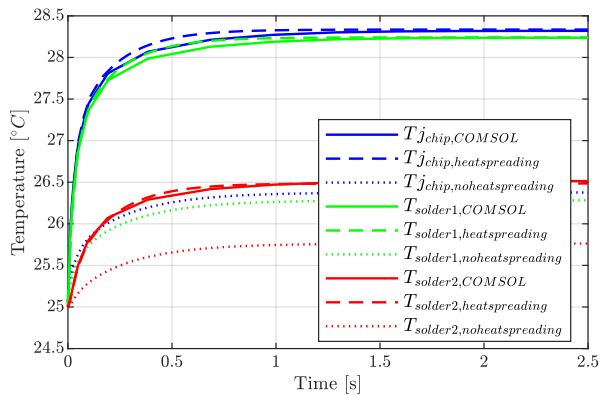


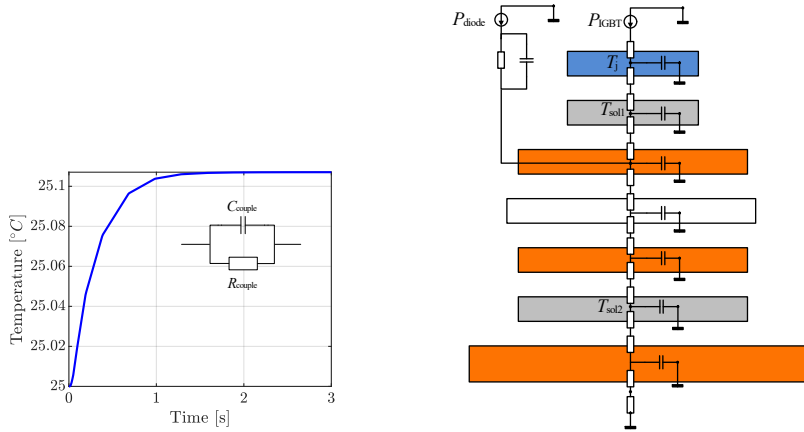
Figure 6.2: Thermal modelling results with considering the heat spreading effect

6.1.2 Thermal modelling - thermal coupling effect

In addition to the heat spreading effect, the thermal coupling effect between two closely placed semiconductor chips needs to be considered, due to the fact that the device can be heated up to a higher temperature. One important factor for including the thermal coupling effect or not is the distance between the IGBT chip and diode chip. According to [52], when the distance between two chips is less than 3 mm, the thermal coupling effect should be considered. For the power module with a compact size in this study, the distance between the IGBT chip and the diode chip is around 1.87 mm, thus, in order to have good accuracy of thermal modelling, this thermal coupling effect should be considered.

Similar to in the previous section, a small block with only considering one IGBT chip and one diode chip was built in COMSOL. The coupling thermal impedance from the diode to the IGBT can be acquired by using the thermal impedance equation. When a heat source is applied to the diode chip, the temperature inside the IGBT chip will rise with time, and the temperature response can be observed in COMSOL, which is shown in Fig. 6.3a. It can be seen that the temperature response seems to have the characteristic as an exponential curve, which means that Foster RC links can represent the dynamic behavior of this curve. By using the curve fitting tool in MATLAB, the values of R and C in the Foster RC link were acquired, and it was found that one RC link was fine for representing the response. The modified Cauer model with adding this thermal coupling RC link is shown in Fig. 6.3b.

The simulation result of temperatures in different layers when considering both the thermal spreading effect and the thermal coupling effect is shown in Fig. 6.4. It can be seen that by adding the thermal coupling effect, the FEM simulation result and PLECS simulation result have a small difference from each other. This is due to that the thermal coupling term changes the heat flux distribution inside the substrate layers, and the previous fixed 32.5° heat spreading angle does not completely represent the current condition. However, the difference between these two simulation results is acceptable, which means that this modified thermal model can be used for future long-term analysis.



(a) Temperature response on the IGBT with the heat source on the diode (b) Cauer thermal model with adding thermal coupling effect

Figure 6.3: Thermal coupling effect modelling

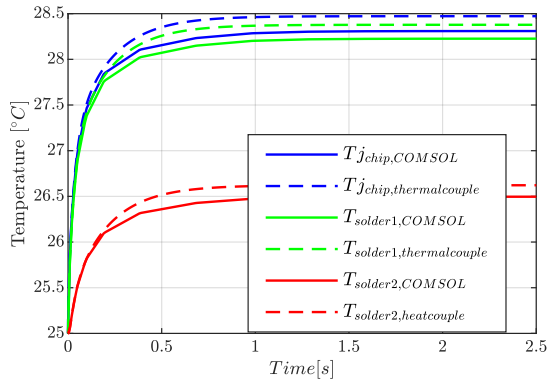


Figure 6.4: Thermal modelling results with considering the thermal coupling effect

6.2 Losses evaluation

The overall process of evaluating the total losses of the converter is shown in Fig. 6.5, and it can be seen that there are three different domains. The controllers and the modulators for both grid-side and machine-side converters are being simulated in the Matlab Simulink domain. The electrical behaviors of the converters are simulated in PLECS electrical domain, and the switching signals are passed from the control process. The third domain is the PLECS thermal domain, and the losses of the power switches inside the converter are evaluated in it. The aforementioned loss lookup tables are used in this loss evaluation process.

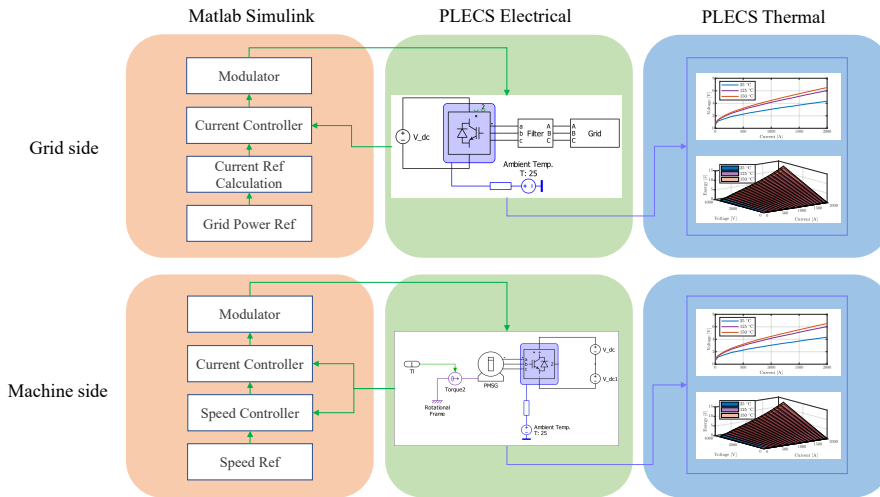


Figure 6.5: The process to evaluate the losses inside the converter

The boundary conditions used for the simulation are listed in Table 5.1. From the power and voltage ratings of the studied unit, it is concluded that the RMS current in one phase is around 500 A, and the peak current is around 700 A. When selecting the power switch to handle such a peak current, a certain amount of safety margin should be considered, and thus, in this study, the current rating of the used power switches is set to be 1000 A, i.e. twice the RMS value of the rated current. The DC-link voltage is 13 kV, and in order to have the lowest number of series connected power switches in one switch

position, a commercial IGBT power switch with 6.5 kV blocking voltage is selected. As mentioned earlier, 6.5 kV is the maximum blocking voltage, and some safety margins need to be considered, thus, this 6.5 kV power switch is used for 3.3 kV DC voltage operation. The model of the selected power switch is 5SNA1000G650300 from Hitachi Energy. For some of the multilevel converter topologies, when the voltage level is high, that means another lower voltage rating power switch 5SNA1000N330300 can be used.

The losses of various converter topologies under different power levels are shown in Fig. 6.6, and all the loss values in Fig. 6.6 are normalized with respect to the rated power.

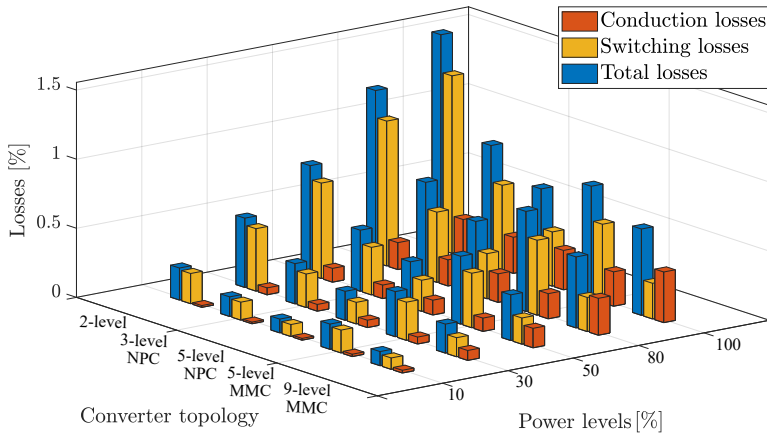
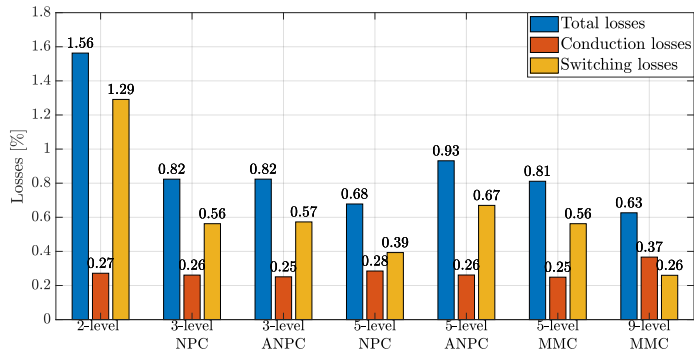


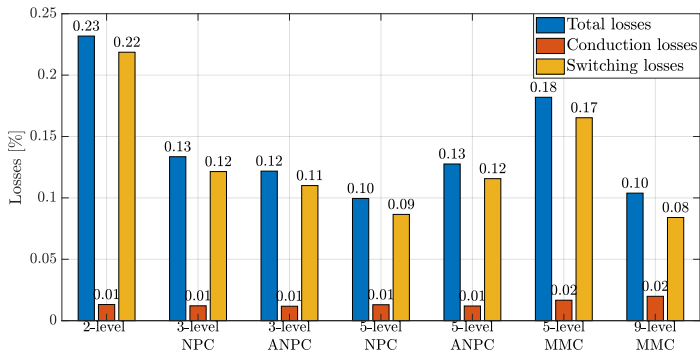
Figure 6.6: Converter losses with various power levels

In general, it can be seen that the loss of the converter in absolute terms increases when the power level is increasing, and the two-level converter has the highest losses, while the 9-level MMC has the lowest losses. For the converters with less than five voltage levels, the switching loss accounts for the majority of the losses for all levels. For the 9-level MMC, the conduction loss is higher than the switching loss at the high power level.

In Fig. 6.7, the losses of the converter at 10% and 100% power are presented. In addition to adding the values of the losses in the figure, the losses of the ANPC converters are shown as well.



(a) Converter losses with 100% Power



(b) Converter losses with 10% Power

Figure 6.7: Converter losses at 100% and 10% power level

Apart from the losses, the component count of different converter configurations is shown in Table 6.1, in which module Type I is 5SNA1000G650300 and module Type II is 5SNA1000N330300.

Table 6.1: Components count of different converter topologies

Converter type	Components number count				Module type
	Module	Clamping diode	Submodule capacitor	Arm inductor	
2L	24	/	/	/	Type I
3L NPC	24	12	/	/	Type I
5L NPC	24	36	/	/	Type I
5L MMC	48	/	48	6	Type I
9L MMC	96	/	96	6	Type II

Based on the above results, it is shown that of all the converter configurations, the nine-level MMC shows the lowest losses. However, the nine-level MMC needs the highest number of components, including 96 IGBT modules, 96 submodule capacitors, and 6 arm inductors for the defined boundary conditions. It should be mentioned that the nine-level MMC uses a smaller power switch 5SNA-1000N330300 compared with the other converter configurations. The price of 5SNA-1000N330300 [53] is almost half of the other power switch 5SNA-1000G650300 [54], thus the investment in the IGBT module in the nine-level MMC is almost the same when compared with the five-level MMC. Worth mentioning is that extra investment is needed for the driver circuits and submodule capacitors in the converter. This means that the total cost of the 9-level MMC would be the highest while the losses would be the lowest. Therefore, if the main target for designing the converter for the application is to have the lowest loss in the converter, the nine-level MMC would be the best option.

On the other hand, if the yearly power dispatch plan of the power unit is known, another analysis from the perspective of the total saved energy in one year can be conducted. Based on the mission profile for a 21 MW unit in Fig. 4.7, the mission profile for the simulated 6 MW unit can be derived by scaling down the power, and the calculated annual electricity generation of this 6 MW unit is around 14.8 GWh. According to the losses percentage values in Fig. 6.6, the annual converter energy losses of different converter

topologies with the unit of [MWh] and [%] (with respect to the total annual energy production) are shown in Table 6.2.

Table 6.2: Annual converter energy losses of different converter topologies

Converter topology	Total losses [MWh]	Total losses [%]
2L	320.934	2.17
3L NPC	184.474	1.25
5L NPC	139.351	0.94
5L MMC	191.258	1.29
9L MMC	132.419	0.89

From Table 6.2, it can be seen that the nine-level MMC has the lowest annual energy losses, and this matches with the previous analysis. The converter that generates the second lowest annual losses is the five-level NPC, and the loss difference between the nine-level MMC and the five-level NPC converter is 6.932 MWh. If the average price of 1 kWh electricity is 1 SEK, then the profit difference between the nine-level MMC and the five-level NPC converter would be 6932 SEK/year. Considering the power switch price in [53], it can be calculated that it takes the nine-level MMC to be running for 98.5 years to accumulate the amount of money that is invested in the extra power switches compared with the five-level NPC. This 98.5 years can be decreased to some extent when considering the investment in the clamping power diodes in the five-level NPC converter. On the other hand, the reference mission profile in Fig. 4.7 shows that the power unit is not operating with full power all over the year, thus, this 98.5 years can be further decreased if the power unit is scheduled for delivering more annual energy.

If the target in the design of the converter is not only to maximize the efficiency of the converter but also to have the least complexity, then, the five-level NPC could be a good option for such an application. When using the same power switches, the five-level NPC shows the lowest losses inside the converter, and the total number of IGBT modules is only half of the five-level MMC. However, the five-level NPC needs some extra clamping diodes, and the neutral point voltage control and uneven distribution of the temperatures in different switch positions make the five-level NPC not that attractive.

The three-level NPC converter shows the third best performance among all the five converter topologies. However, when considering the extra investment

on the clamping diodes and the external filter due to the higher voltage and current THDs, the five-level MMC can outperform the three-level NPC converter if the losses can be decreased. As shown in Fig. 6.7a, the switching loss is almost two times of that of the conduction loss in the five-level MMC at 100% power, thus, it is natural to think about how the switching losses can be decreased. One way of reducing the switching loss is to cut down the frequency of the sorting events for balancing the submodule capacitor in the MMC, while the voltage ripples in the MMC half-bridge modules will increase, which means a larger capacitor is needed for each of the submodules. Another way of decreasing the switching losses is to utilize the discontinuous SVM. By using the five-segment operation in the converter, the switching events in each PWM cycle can be decreased, thus lowering the switching loss.

6.3 Lifetime evaluation

The following parts show the results of evaluating the lifetime of the power switches inside an MMC with the CFM configuration under turbine mode, and the detailed process is presented in **Paper IV**.

6.3.1 Power switches junction temperature estimation

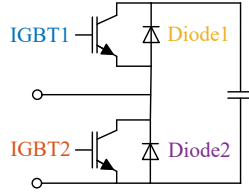
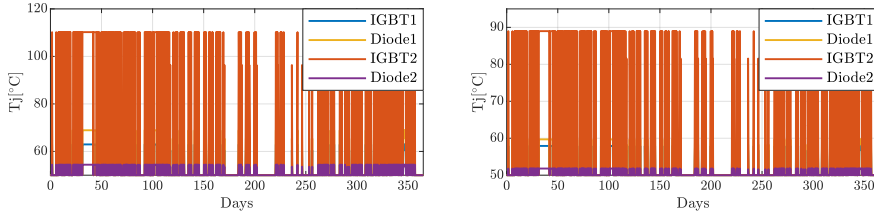
The junction temperature estimation of the power switches inside a back-to-back MMC configuration was conducted with the converter parameters listed in Table 6.3, and the power switch type is Hitachi Energy 5SNA1000G650300.

The structure of the half-bridge submodule is reviewed in Fig. 6.8. By feeding in the mission profile in Fig. 4.7, the junction temperature variations inside one half-bridge module of the MMCs are shown in Fig. 6.9.

It can be seen that IGBT2 in the half-bridge module experiences the highest temperature variation both in the grid-side and the machine-side MMC, and the situation in the grid-side MMC is worse than in the machine-side MMC. It can also be seen that the highest junction temperature inside the MMC is around 110 °C, which is below the datasheet recommended temperature limit of 150 °C for the selected power switches. These temperature profiles can be used to estimate the lifetime of the switches inside the MMC based on the

Table 6.3: The MMC parameters used for lifetime estimation

Parameters	Value	Unit
Power S	21	MVA
DC-link voltage V_{dc}	24	kV
Number of submodules in each arm N_{SM}	8	/
Submodule voltage E_{SM}	3	kV
Submodule capacitance C_{SM}	20	mF
Submodule capacitor ESR R_{SM}	26.8	m Ω
Arm inductance L_{arm}	2.5	mH
Arm resistance R_{arm}	64.3	m Ω
PWM carrier frequency $f_{carrier}$	750	Hz

**Figure 6.8:** Half-bridge submodule structure

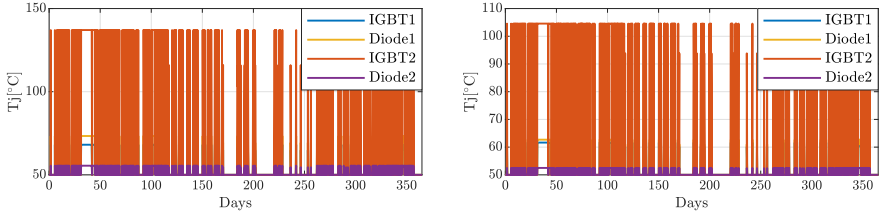
(a) Junction temperature variation in grid-side MMC, 5SNA1000G650300 (b) Junction temperature variation in machine-side MMC, 5SNA1000G650300

Figure 6.9: Junction temperature variations with 5SNA1000G650300

lifetime model in section 4.2. This indicates that the 5SNA1000G650300 is slightly over-dimensioned for this application in terms of the junction temperature limit.

Another power switch 5SNA0750G650300 which has a lower current rating is

selected to quantify the junction temperature for the same application, and the results are shown in Fig. 6.10. It can be seen that the highest temperature inside the converter is around 137 °C, which is still below its upper thermal limit.



(a) Junction temperature variation in grid-side MMC, 5SNA0750G650300 (b) Junction temperature variation in machine-side MMC, 5SNA0750G650300

Figure 6.10: Junction temperature variations with 5SNA0750G650300

6.3.2 Lifetime results

Based on the junction cyclic temperature swings in Fig. 6.9 and Fig. 6.10, a rainflow counting method is utilized to count the thermal stress cycles of the power switches to evaluate the lifetime, and the results are shown in Table 6.4, and a bar plot of the results is shown in Fig. 6.11.

Table 6.4: Lifetime analysis results

Lifetime/year	IGBT1	Diode1	IGBT2	Diode2
Grid-side				
5SNA1000G650300	3.2e6	5.1e5	2.3e3	6.0e8
Grid-side				
5SNA0750G650300	6.3e5	1.9e5	462	2.0e8
Machine-side				
5SNA1000G650300	3.4e7	1.7e4	1.3e7	4.7e10
Machine-side				
5SNA0750G650300	5.2e6	3.6e3	3.4e6	9.2e9

From Table 6.4 and Fig. 6.11, it can be seen that IGBT2 in the grid-side converter when using the 5SNA0750G650300 power switch has the shortest

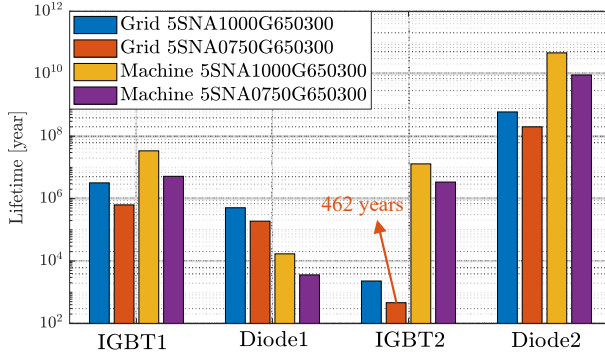


Figure 6.11: Lifetime results with bar plot

lifetime during the operation, which is 462 years. This is as expected since the power switch in this position experiences the highest temperature variations inside the converter. When using the 5SNA1000G650300 power switch, the IGBT2 lifetime is still the shortest in the power module, however, the value of it is five times longer than the value when using the 5SNA0750G650300 power switch. This indicates that when using the MMC in the turbine operation of the hydropower application, the two IGBT and diode anti-parallel pairs in the half-bridge module can be arranged with different ratings. This hybrid power switch configuration in the half-bridge module can make the temperature distribution more even in the module, thus increasing the lifetime of the power switches. If switches with the same power ratings are used in the half-bridge module, then the coolant path design should focus more on the IGBT2 area to prolong the lifetime of the power switches.

On the other hand, considering the shortest lifetime of 462 years of the power switches inside the converter, it can be found that it is longer than the designed lifetime of the converter (30 years). However, it should be mentioned that this is the component lifetime, and the full system (converter) utilize many components, which means the full system lifetime depends on the individual components lifetime distribution. So, in order to have a 90% probability of 30 years of full system lifetime, this 462 years maybe fine. Anyway, if we return to this 462 years lifetime of the power switch, it means that the installed power switches in the converter can be used to handle higher thermal stress. The

mission profile in Fig. 4.7 shows that the start-stop operation of the studied power unit is not that frequent, thus, a more intense mission profile can be utilized to analyze the lifetime of the power switches.

Assuming that the studied power unit will start and go up to full power and stop to zero power every hour in one day to cope with the renewable energy fluctuations, and this will occur everyday all over one year, then a new mission profile can be created. Fig. 6.12 shows the newly created mission profile for one day period.

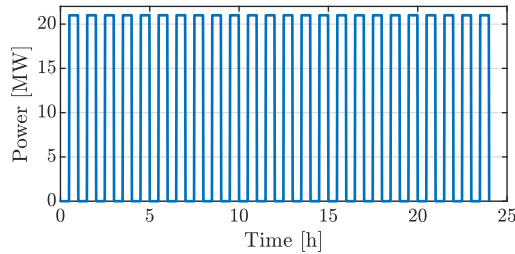


Figure 6.12: The new designed mission profile for one day period

Since the grid-side IGBT2 shows the shortest lifetime in the previous analysis, the new lifetime analysis will only be conducted on this switch position. By using the same lifetime analysis process, the new lifetime results of the grid-side IGBT2 are shown in Table 6.5.

Table 6.5: Lifetime analysis results with the new mission profile

Power switch type	Lifetime [year]
5SNA1000G650300	72
5SNA0750G650300	14

It can be seen that when using the lower voltage rating power switch 5SNA075-0G650300, with the new designed 24 start-stops operations per day, the lifetime of the grid-side IGBT2 will reduce to 14 years, which is less than the designed lifetime of the converter. However, for the other power switch 5SNA1000G650300, this frequent operation is not a problem, and the 72 years of a lifetime shows the ability that the power switch can withstand an even more intense mission profile.

Conclusions and future work

7.1 Conclusions

In this study, various converter topologies have been investigated for a variable speed pumped-storage hydropower application from the aspects of modulation, efficiency, and lifetime.

PWM and SVM are used for the modulation of different converter topologies. According to the simulation results, even though the SVM shows slightly worse results compared with PWM, the freedom of designing the switching sequence to decrease the switching loss or reduce the common-mode voltage shows more flexibility when using SVM compared to PWM.

The simulation results also show that the studied control methods, such as the current control and the DC-link voltage control, are feasible for the converter control in the application. However, for the NPC converter and the MMC, additional control aspects need to be taken into account to fulfill different

targets. The three-level NPC converter uses the injection of a zero-sequence signal into the modulation signal to keep the neutral point voltage balanced while the five-level NPC uses external hardware to keep the neutral point voltage balanced. The MMC uses a closed-loop circulating current controller to suppress the current oscillations to reduce the conduction losses in the power switch. Besides, a sorting algorithm is implemented in the MMC to balance the submodule voltages. The experimental results in a five-level MMC verify that the circulating current control and submodule balancing algorithm are feasible for the studied applications.

Thermal modelling when considering the heat spreading effect and thermal coupling effect was conducted in the study as well. A fixed thermal spreading angle of 32.5° along with a thermal coupling RC link was added to a Cauer thermal model and the simulation results were compared with the FEM simulation to show that the proposed modified Cauer thermal model can be used for a long term analysis while the computation burden is greatly decreased.

A loss evaluation process was conducted for different converter topologies, and the 9-level modular multilevel converter shows the best efficiency of 99.37% for the defined conditions in the loss study, while the classical two-level converter shows efficiency of 98.44%. The five-level NPC shows the second best efficiency of 99.32%, but the extra components and neutral point voltage balancing circuit make this topology less attractive. On the other hand, the 9-level modular multilevel converter has the most component count when compared with the other converter topologies.

A lifetime study was conducted for power switches inside a modular multilevel converter, and it is found that with the used semiconductors design, i.e., the semiconductors have an RMS current value that of half of its stated maximum value, the lifetime requirement of 30 years can always be fulfilled.

7.2 Future work

Some examples of the future work are

- Experimental verification on the thermal modelling. The thermal modelling has been a vital part of this work, and it would be of great interest

to verify some of the ideas, such as the loss value evaluation.

- Lifetime modelling with various lifetime models. As different researchers have developed various lifetime models based on different failure mechanisms, it would be beneficial to compare the results of using different lifetime models to see the impact of different failure mechanisms on the lifetime.
- System-level lifetime analysis. It would also be interesting if a system-level lifetime study can be conducted by considering all the components inside the converter, not merely the power switches.
- Other modulation and control methods to reduce the losses or increase the performance of the converter for a general medium voltage variable speed application.

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