Thesis for the Degree of Doctor of Philosophy

Wideband CMOS Data Converters for Linear and Efficient mmWave Transmitters

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Cover: Chip photo of the 2×10 bit RF-IQ modulator presented in paper B.

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Abstract

With continuously increasing demands for wireless connectivity, higher carrier frequencies and wider bandwidths are explored. To overcome a limited transmit power at these higher carrier frequencies, multiple input multiple output (MIMO) systems, with a large number of transmitters and antennas, are used to direct the transmitted power towards the user. With a large transmitter count, each individual transmitter needs to be small and allow for tight integration with digital circuits. In addition, modern communication standards require linear transmitters, making linearity an important factor in the transmitter design.

In this thesis, radio frequency digital-to-analog converter (RF-DAC)-based transmitters are explored. They shift the transition from digital to analog closer to the antennas, performing both digital-to-analog conversion and up-conversion in a single block. To reduce the need for computationally costly digital predistortion (DPD), a linear and well-behaved RF-DAC transfer characteristic is desirable. The combination of non-overlapping local oscillator (LO) signals and an expanding segmented non-linear RF-DAC scaling is evaluated as a way to linearize the transmitter. This linearization concept has been studied both for the linearization of the RF-DAC itself and for the joint linearization of the cascaded RF-DAC-based modulator and power amplifier (PA) combination. To adapt the linearization, observation receivers are needed. In these, high-speed analog-to-digital converters (ADCs) have a central role. A high-speed ADC has been designed and evaluated to understand how concepts used to increase the sample rate affect the dynamic performance.

Keywords: CMOS, Efficient, Linear, Linearization, MIMO, mmWave, Predistortion, RF-DAC, SAR ADC, Wideband.

Publications

This thesis is based on the work contained in the following papers:

[A] **Victor Åberg**, Christian Fager, and Lars Svensson. "A 2×6 b 8 GS/s 17–24 GHz I/Q RF-DAC-Based Transmitter in 22 nm FDSOI CMOS", in *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 8, pp. 929-932, Aug. 2021.

[B] **Victor Åberg**, Christian Fager, Rui Hou, and Lars Svensson. "An 11 GS/s 2×10 b 20–26 GHz Modulator using Segmented Non-Linear RF-DACs and Non-Overlapping LO signals", *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2022, pp. 1-4.

[C] **Victor Åberg**, Han Zhou, Christian Fager, and Lars Svensson. "RF PA Predistortion using Non-Linear RF-DACs", submitted to *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, 2022, pp. 1-5.

[D] **Victor Åberg**, Christian Fager, and Lars Svensson. "Design Considerations and Evaluation of a High-Speed SAR ADC", *2018 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*, 2018, pp. 1-6.

Parts of the contributions also resulted in inventions:

[I] **Victor Åberg** and Lars Svensson, Radio Frequency Digital to Analog Converter (RF-DAC) Unit Cell, PCT/SE2020/050372, filed on April 8$^{\text{th}}$, 2020.

[II] **Victor Åberg**, Christian Fager, and Lars Svensson, Digital to Analog Conversion and Power Amplification, filed on February 4$^{\text{th}}$, 2022.

Contents

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Pursuing a Ph.D. is a journey with a clear goal. However, the path, from start to finish, is far from straight. It is like walking through a maze without a map, and when you think you figured it out, the maze changes. Thankfully, I had people both guiding and supporting me along the way.

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Victor Åberg
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Acronyms

5G	fifth generation mobile network
ACPR	adjacent channel power ratio
ADC	analog-to-digital converter
AMAM	amplitude modulation to amplitude modulation
AMPM	amplitude modulation to phase modulation
APD	analog predistortion
ASIC	application-specific integrated circuit
AWGN	additive white Gaussian noise
BB	baseband
BER	bit-error rate
BiCMOS	bipolar complimentary metal oxide semiconductor
BJT	bipolar junction transistor
CA	carrier aggregation
CML	current-mode logic
CMOS	complimentary metal oxide semiconductor
DAC	digital-to-analog converter
DC	direct current
DE	drain efficiency
DFT	discrete Fourier transform
DNL	differential non-linearity
DPD	digital predistortion
DR	dynamic range
DSP	digital signal processing
ENOB	effective number of bits
EVM	error vector magnitude
FDSOI	fully-depleted silicon-on-insulator
FET	field-effect transistor
FF	flip-flop
FoM	figure of merit
FoMS	Schreier figure of merit
FoMW	Walden figure of merit
FPGA	field-programmable gate array
HD	harmonic distortion

INL	integral non-linearity
IQ	in-phase/quadrature
IRR	image rejection ratio
ISI	inter-symbol interference
LO	local oscillator
LSB	least significant bit
LUT	lookup table
MIMO	multiple input multiple output
mm-Wave	millimeter wave
MSB	most significant bit
NMOS	n-type metal-oxide-semiconductor
OFDM	orthogonal frequency division multiplexing
OSR	oversampling ratio
OTA	over-the-air
PA	power amplifier
PAE	power-added efficiency
PAPR	peak-to-average power ratio
PMOS	p-type metal-oxide-semiconductor
PPF	poly-phase filter
QAM	quadrature-amplitude modulation
RF	radio frequency
RF-DAC	radio frequency digital-to-analog converter
RF-IQ modulator	radio frequency in-phase/quadrature modulator
RMS	root-mean-square
RRC	root-raised cosine
SAR	successive-approximation register
SC	single carrier
SFDR	spurious free dynamic range
SNDR	signal-to-noise-and-distortion ratio
SNR	signal-to-noise ratio
TI	time-interleaved
TIA	transimpedance amplifier
ZOH	zero-order hold

Chapter 1

Introduction

In the 3rd quarter of 2021, the total global data traffic in mobile networks reached 78 EB per month [1]. During the last decade, the compound annual growth has exceeded 50 % without signs of slowing down. It is predicted that in five years, the global mobile traffic will exceed 350 EB per month [1]. To cope with this rapid increase, and to overcome the bandwidth limitations in the crowded frequency bands below 6 GHz, wireless networks increasingly make use of millimeter wave (mm-Wave) frequencies, where a large amount of continuous spectrum is available. For example, the fifth generation mobile network (5G) standard introduces several frequency bands in the 24.25–52.6 GHz frequency range, most having a bandwidth of around 3 GHz [2], thereby putting unprecedented requirements on transmitter implementation.

1.1 The MIMO transmitter

At mm-Wave frequencies, the transmission losses are larger than at lower frequencies, making it hard to cover large areas. With massive multiple input multiple output (MIMO) transmitters, it is possible to focus the energy towards the user, extending the reach, while allowing for the use of a lower transmit power [3]. In addition, at mm-Wave frequencies, a large number of antennas may be placed within a small physical space. Hence, we need transmitters that provide sufficient output power while having a size small enough to fit within the footprint of a single antenna. To handle the wide bandwidth, the transmitters must also allow for tight integration with the digital signal processing (DSP).

All transmitters suffer from imperfections and non-linearities. At high carrier frequencies, approaching a *perfect* transmitter is even more challenging. For a single transmitter, the device's non-linearities will have the greatest impact on the performance. In a system with multiple transmitters, the variations among them further degrade performance. These imperfections and non-linearities will affect the spectral properties of the signal, and some radio frequency (RF) power

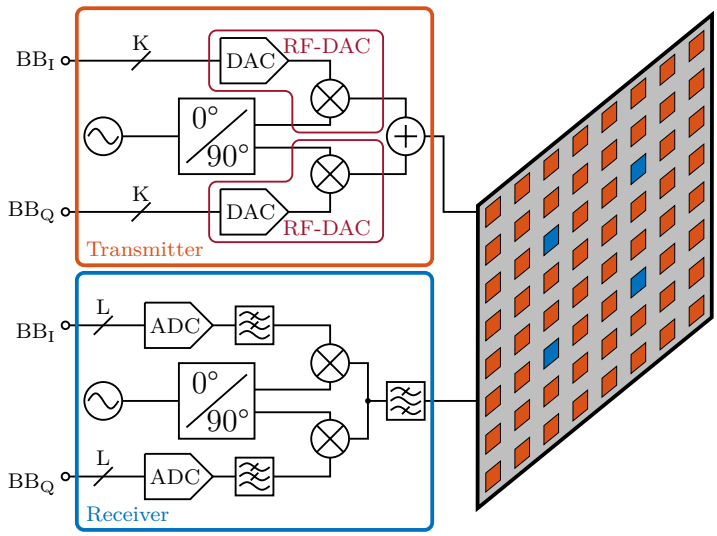


Figure 1.1: Illustration of a MIMO array with transmitters and over-the-air (OTA) observation receivers. Orange rectangles represent transmit antennas while blue rectangles represent receive antennas. Each antenna is connected either its own transmitter or receiver.

might be emitted outside the intended channels, potentially disturbing other channels. To mitigate the problem, in a system with one or a few transmitters, each transmitter may be fitted with an observation receiver that monitors the transmitted signal [4]. This observation signal is then fed to an algorithm that will alter the transmitted signal, resulting in a transmitted signal with reduced non-linearity.

In a massive MIMO system, up to several hundred sub-signals may be combined to form the transmitted signal. Each of these is radiated by an antenna fed by its own transmitter, which makes it unrealistic to locate an observation receiver along with each transmitter. In addition to the large power consumption and area that these receivers would require, there is also a large computational cost for processing their output. Rather, it is desirable to share the observation receiver among multiple transmitters. This can either be done through switches [5], or by combining all the different sub-signals, overcoming the limited isolation between the switches [6]. However, combining all sub-signals through routing is problematic as it might result in additional cross-talk not visible in the transmitted signal. Rather than combining the sub-signals through routing, it is also possible to combine them in air, just like the signal reaching the user. It has been shown that with only a few observation receivers, replacing some of the transmitters, it is possible to measure the transmitted signal over-the-air (OTA) [4]. A massive MIMO array with a few observation receivers is illustrated in figure 1.1. The distance between the antennas is

related to the signal wavelength. In addition, this figure also shows simplistic schematics for the transmitters and receivers and the DSP block.

1.2 Technology options

With potentially several hundred transmitters in a single MIMO array, each transmitter must not only be compact and cheap, it must also be both power efficient and enable tight integration with the DSP. The modulator in a single transmitter may require a data-stream in excess of 100 Gb/s while the data delivered to the users only make up <10 % of this data-stream. Similar digital bandwidths are also delivered by the analog-to-digital converters (ADCs) located in the observation receivers, further exposing the need for tight integration between the transmitters, observation receivers, and DSP.

Given the aspects presented above, there is no existing technology that is optimal for all the required components. Silicon-based complimentary metal oxide semiconductor (CMOS) and Silicon-Germanium (SiGe)-based bipolar complimentary metal oxide semiconductor (BiCMOS) are the most suitable alternatives. In CMOS technologies, transistors are realized using the field-effect transistor (FET) topology. Modern CMOS processes can be divided into two categories; FIN-FETs, where the gate wraps around the channel, and fully-depleted silicon-on-insulator (FDSOI) which is closely related to the traditional FET topology, except for a buried oxide layer that separates the channel from the bulk, while introducing a back gate. These processes bring exceptional computational performance and the transistors are fast enough for mm-Wave applications, although their large input capacitance and poor transconductance sometimes become problematic. BiCMOS extends regular CMOS technologies with bipolar junction transistors (BJTs), thus combining high computational efficiency with excellent analog performance brought by the BJTs. While BiCMOS takes advantage of the reduced feature size in modern CMOS processes, the technology still lies several process-nodes behind the latest CMOS processes in terms of scaling, delivering significantly lower digital performance.

With reduced feature sizes, the supply voltages are also reduced. This is beneficial when considering the power consumption but from an analog perspective, the reduced supply voltages reduce the circuit dynamic range. It also becomes problematic to deliver high output power levels.

When considering the integration and computational requirements for a mm-Wave transmitter, a modern CMOS process is currently the only viable option even though the analog performance is slightly lower than the performance of the BJTs in a BiCMOS process. All circuits presented in this thesis are implemented using modern FDSOI CMOS processes.

1.3 Problem statement

Transmitters intended for user equipment only use a channel for shorter periods of time. Base station transmitters, on the other hand, must cover the entire band all the time. With the large number of transmitters required in mm-Wave massive MIMO arrays, each individual transmitter must not only support a wide bandwidth, it must also be linear, efficient, and allow for tight integration with digital logic. The same goes for the observation receivers required for linearizing the transmitter.

Wideband, linear, and efficient data converters with sufficient dynamic range for modern communication signals are fundamental for the realization of these transmitters and observation receivers. To fit a transmitter within the footprint of a single antenna and allow space for some DSP close to the transmitter while fulfilling a tight energy budget, innovative topologies that reduces the footprint of the transmitter are needed. In addition to the digital-to-analog converters (DACs) required in the transmitters, wideband and efficient ADCs are required in the observation receivers to enable adaptive transmitter linearization. With a large number of transmitters and very wideband signals, the cost of linearization grows very rapidly. For an efficient transmitter, the linearization must be implemented with care to keep both the hardware cost and power consumption small.

To push the boundaries in circuit design, in addition to making innovative circuits, one must also understand what limits their performance. In this thesis, I study the use of radio frequency digital-to-analog converter (RF-DAC)-based modulators as a way of reducing the transmitter footprint, combining the digital-to-analog conversion with up-conversion in a single block. I explore the use of an expanding non-linear DAC scaling to linearize not only the DAC itself but also a power amplifier (PA) driven by a RF-DACs-based modulator. The linearization is achieved without any additional hardware cost other than somewhat increased transistor widths in the RF-DACs. I also analyze the impact of comparator offset voltage in an alternating comparator successive-approximation register (SAR) ADC. To better understand what limits the performance in the fabricated circuits, measurement results are compared to simulation results, to identify the cause.

1.4 Thesis outline

The remainder of the thesis is organized as follows. Chapter 2 briefly introduces concepts related to wireless communication and data conversion. In chapter 3, concepts and theory related radio frequency in-phase/quadrature modulator (RF-IQ modulator) are introduced. Chapter 4 introduces the concept of predistortion. In chapter 5, theory and concepts related to ADCs are introduced. These four chapters are intended to form a theoretical base for the remainder of the thesis. Related work on RF-IQ modulators, linearization and ADCs are presented in

chapter 6. Chapter 7 extends the discussion started in the included papers A and B with focus on the quadrature local oscillator (LO) generation, effects that limit performance, and extended measurement results. In chapter 8, the linearization concept is further explained and simulations results for modulated signals (not included in paper C) are presented together with the static properties. Chapter 9 extends the discussion on the impact of offset voltage in an alternating comparator SAR ADC. Chapter 10 concludes the thesis with a summary of the contributions presented in the included papers and an outlook on future research topics. Finally, the included papers (papers A to D) are presented.

Chapter 2

Introduction to wireless communication and data conversion

This chapter will introduce important concepts and theories behind wireless communication and data conversion, forming the base for both the theoretical and the design-oriented chapters that will follow. Concepts and theories with a clear connection to one of the three cornerstones in this thesis will be presented in their respective chapters (chapters 3 to 5).

2.1 Modulation

A continuous wave (CW) signal cannot transmit any information as all its properties (amplitude, phase, and frequency) are static over time. For the signal to carry information, at least one of these properties needs to be altered over time. Modulation is the process of encoding information onto the carrier signal by altering one or several of its properties in a predefined way.

In the early days of wireless communication (in the telegraph era), operators manually encoded information onto the carrier signal using pulses of different lengths. The Morse alphabet was used as the key for encoding and decoding the information. The same simple principles are still in use today by amateur radio operations around the world.

Although modern communication systems rely on the same fundamental principles, the resources must be used more efficiently. With limited spectral resources, a modern communication system must maximize the amount of information that may be transmitted in a reliable way using the smallest amount of resources. There is however a fundamental limit to the information that may be transmitted. The Shannon theorem, equation (2.1), describes

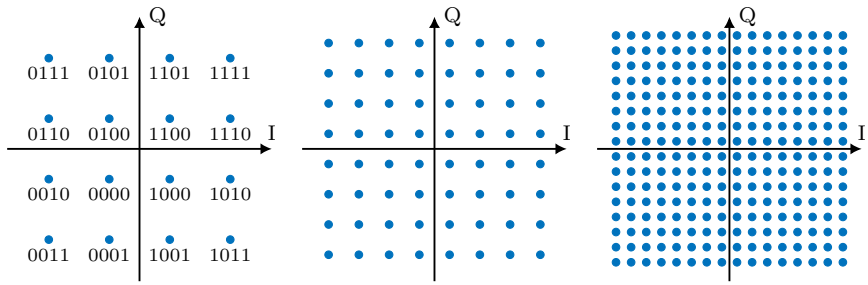


Figure 2.1: Illustration of complex modulation formats, (a) 16-QAM, (b) 64-QAM, and (c) 256-QAM, commonly used in modern cellular systems. In (a), the mapping of digital bits onto the constellation points is illustrated.

this limit for a channel with additive white Gaussian noise (AWGN) where the channel capacity C is given by the channel bandwidth B and the signal-to-noise ratio (SNR) [7].

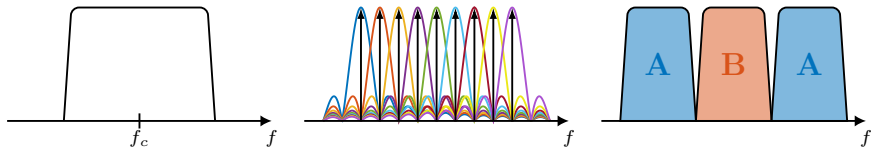
$$C = B \log_{10}(1 + \text{SNR}) \quad [\text{b/s}] \tag{2.1}$$

2.1.1 Modulation formats

Modulation formats are the key used for relating digital information to analog signal properties. In the general case, each symbol value is represented by a unique combination of the carrier signal amplitude and phase. In simple modulation formats, either the amplitude or phase is kept constant. The collection of all unique combinations then gives the *constellation diagram*, often illustrated using a complex coordinate system, although the signal properties (amplitude and phase) would be better represented by a polar coordinate system. Thus, the constellation diagram is used to illustrate the mapping between digital information and analog signal properties.

Spectral efficiency is a metric of the amount of information that may be transmitted using a given bandwidth. In the simplest case, using a single channel, the spectral efficiency equals $\log_2$ of the number of unique points in the constellation diagram. For MIMO systems where multiple streams reuse the same frequency resources, a higher spectral efficiency may be achieved. From Shannon's theorem, a high channel capacity, which for a given bandwidth translates into a high spectral efficiency, requires a high channel SNR. Hence, a modulation format with high spectral efficiency implies a tougher SNR requirement.

The principle behind the quadrature-amplitude modulation (QAM) formats commonly used in modern communication systems originate from 1960 [8] and the square QAM format appeared a few years later [9]. A few QAM formats of varying complexity are shown in figure 2.1. To minimize the impact of



(a) SC **(b)** OFDM **(c)** CA

Figure 2.2: Illustration of different wireless channel options, (a) SC located at f_c, (b) orthogonal frequency division multiplexing (OFDM) with the sub-carriers represented by the arrows, and (c) carrier aggregation (CA) where user **A** gets 2 aggregated channels while used **B** gets one channel.

erroneously decoding a symbol, the bits representing each constellation point are typically Gray-coded [10, Ch. 3]. That is, the digital code-words for the closest neighbouring constellation points only differ by a single bit, as illustrated in figure 2.1a. This also reduces the bit-error rate (BER) as it is most likely that a symbol is erroneously detected at a neighbouring constellation point, given a channel limited by AWGN.

2.1.2 Channel configuration

Several methods are possible for mapping symbol streams to RF signal values. In the single carrier (SC) case, a single stream of symbols is transmitted, one symbol after another. In this configuration, a symbol is represented by the carrier properties of a constellation point at a specific point in time. While the same signal properties (amplitude and phase) are used multiple times, a unique symbol is formed when these properties are used at a specific point in time. This method is the simplest, from the modulator's perspective, as only a single symbol is transmitted at any given time. However, with a very short symbol duration, the fading experienced in a cellular system will be problematic, potentially causing multiple symbols to be lost [10, Ch. 15]. With the SC configuration, the single modulated signal will cover the entire channel bandwidth, centered around the carrier, as illustrated in figure 2.2a.

To reduce the impact of fading, longer symbols are desired. In the SC case, however, longer symbols directly result in reduced throughput. One solution is to use orthogonal frequency division multiplexing (OFDM) where N symbols are modulated in parallel on different sub-carriers, sharing a common channel. As a result, the OFDM-symbol becomes N times as long as the symbol in the SC case, giving the sub-carrier spacing $F_{sym,SC}/N$. With the significantly longer symbol duration, fading no longer is a problem given that it only occurs during a short period of time [10, Ch. 15]. Another benefit of the longer symbol duration is that the inter-symbol interference (ISI) is reduced in comparison to the SC case. On the other hand, a major disadvantage with OFDM is that a single modulator is needed for each of the N individual sub-carriers. This is however impractical already for a small N. Thankfully, the multiple parallel tones are

conceptually very similar to the basis functions of a discrete Fourier transform (DFT) [10, Ch. 15]. The DFT is often realized using a fast Fourier transform (FFT) and with the symbols in the frequency domain, an inverse fast Fourier transform (IFFT) can be used to generate a time-domain signal that is similar to the one in the SC case, albeit with a larger computational cost compared to the SC case. An illustration of an OFDM signal with 9 sub-carriers is shown in figure 2.2b. In contrast to a single symbol in the SC case, an OFDM-symbol carries significantly more information and can be seen as a small package of information. In addition to resilience against fading, OFDM inherently supports division of the frequency resources into several smaller channels.

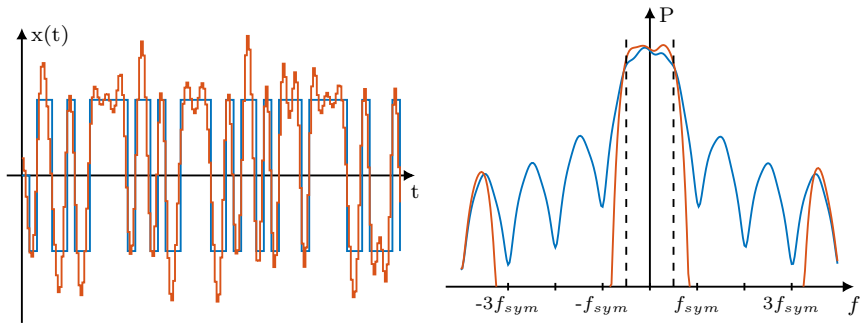
Another impact of the different channel configurations is the signal dynamic range, often illustrated by the peak-to-average power ratio (PAPR). For both cases, PAPR is related to the complexity of the modulation format. However, OFDM comes with significantly higher PAPR as a result of the interaction of the different tones in the time-domain, which results in higher amplitude peaks and deeper valleys and therefore large variations in instantaneous power. From a hardware perspective, a high PAPR is problematic as the resulting low average power significantly degrades the transmitter's efficiency.

To simultaneously support multiple users, a typical communication band is divided into multiple channels serving different users. For the 5G frequency range 2 (FR2) bands, the following channel configurations are available: 50 MHz, 100 MHz, 200 MHz, and 400 MHz [2]. In some cases, it can however be desirable to achieve a bandwidth higher than what is available in a single channel. The solution to this is carrier aggregation (CA) where multiple channels are combined. These channels do not have to be located next to each other; they can even span multiple bands if that is necessary. The principle of CA is illustrated in figure 2.2c.

2.1.3 Pulse shaping

A DAC is typically modelled using two blocks, one generating an analog value based on the digital input code and another one for holding this analog value for the duration of the sample. A zero-order hold (ZOH) function can be used to model this second block. A time-domain modulated signal passed through a ZOH DAC is shown in figure 2.3a. The frequency-domain representation of ZOH is a sinc with zeros at every multiple of the symbol rate f_{sym}, illustrated in figure 2.3b. The desired signal is located in the range $-\frac{f_{sym}}{2}$ to $\frac{f_{sym}}{2}$, and frequencies outside this range contain images of this signal.

In a communication system where channels are tightly packed, requirements on the signal quality are not only strict within the channel but also on the power emitted outside the channel. Thus, it is important to suppress emissions outside the transmitted channel caused by ZOH, non-linear distortion, and ISI. A digital filter may be used to make the signal band-limited and to prevent ISI. Typically, a root-raised cosine (RRC) filter is used in communication systems as it allows for the same filter to be implemented in both the transmitter and



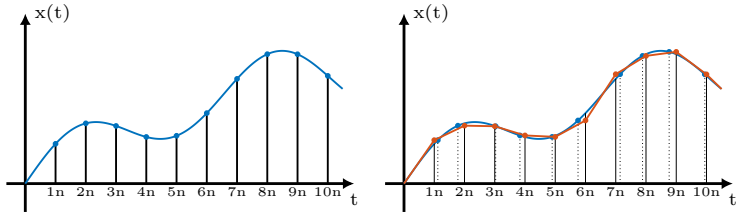
(a) Time-domain **(b)** Frequency-domain

Figure 2.3: Illustration of the combined benefits with pulse-shaping and oversampling in (a) time-domain, and (b) frequency-domain. The signal is shown without pulse-shaping and oversampling in blue and with pulse-shaping and oversampling in orange. The dashed lines mark the desired signal. An oversampling ratio (OSR) of 4 has been used in this example.

receiver while minimizing the ISI in the received signal [10, Ch. 4].

The images caused by the ZOH on the other hand cannot be addressed in this way as the effect is generated when entering the analog domain. Filtering in the analog domain is needed, but the tightly packed channels present a problem as analog filters cannot be made sharp enough to filter out a single channel. A solution to this problem is to combine the RRC filter with oversampling. This smooths out the sharp signal transitions, as can be seen for the time-domain signal in figure 2.3a. In the frequency domain, the smoother transitions result in the images being shifted further away from the desired signal, as illustrated in figure 2.3b, allowing for a wider analog-filter transition band. From this figure, it can also be observed that the signal occupies a slightly wider range than $-\frac{f_{sym}}{2}$ to $\frac{f_{sym}}{2}$, indicated by the dashed lines. The amount of additionally occupied frequency resources is controlled through the filter roll-off factor. With a reduced roll-off factor, a narrower transition band is achieved. The oversampling ratio (OSR) is the ratio between the sample rate at which the DAC operates and the symbol rate used by the system.

To benefit from oversampling, the DAC needs a higher resolution compared to the resolution needed for generating the constellation points, since intermediate signal levels are needed to provide the smooth signal transitions. Also, the resolution will set the noise floor for both in-band and out-of-band emissions. While oversampling is very useful when shifting images, the required sample rate grows rapidly with an increased OSR, especially in a wideband system. The combination of high resolution and high sample rate makes the design of the required DACs challenging.



(a) **(b)**

Figure 2.4: (a) A uniformly sampled signal and (b) the sampling instances affected by jitter. Here the blue points indicates the sampled signal while the resulting signal is shown in orange, assuming uniform sampling.

2.2 Sampling and quantization

Both ADCs and DACs work with signals that are both sampled and quantized. An ADC takes a continuous signal and converts it into a sampled and quantized representation. A DAC uses the sampled and quantized signal to reconstruct an analog signal. A reconstruction filter typically follows the DAC, smoothing the transitions from one sample to the next.

2.2.1 Sampling

In an ADC, a continuous signal is converted into a discrete representation. From a mathematical perspective, uniform sampling can be seen as multiplication with uniformly distributed Dirac pulses [11, Ch. 2]. The sampled signal is then given by equation (2.2), with an inter-sample spacing $T_s = 1/f_s$ [12, Ch. 2]. A uniformly sampled signal is shown in figure 2.4a. However, in practice, it is not possible to achieve fully uniform sampling [13, Ch. 1]. Undesired variations, caused by systematic errors (skew) or random variations (jitter) cause the exact sampling instance to vary. Even small variations may have a large impact on the accuracy of the sampled signal. Figure 2.4b illustrates the effect of variations in the sampling instance and the resulting signal when assuming uniform sampling.

$$x_s(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\,\delta(t - nT_s) \tag{2.2}$$

Sampling is a linear operation, which is indicated by equation (2.2). The sampled signal will suffer from bandwidth expansion with images of the sampled signal appearing around every multiple of the sampling frequency f_s [13, Ch. 1]. To avoid images from overlapping each other, a band-limited signal is required [11, Ch. 2]. This issue was first recognized by Nyquist [14] who indicated a requirement for the relationship between the signal and the sample rate. The relationship was then formulated into the expression, known as the Nyquist criterion, equation (2.3), by Shannon [7], although he formulated it in words.

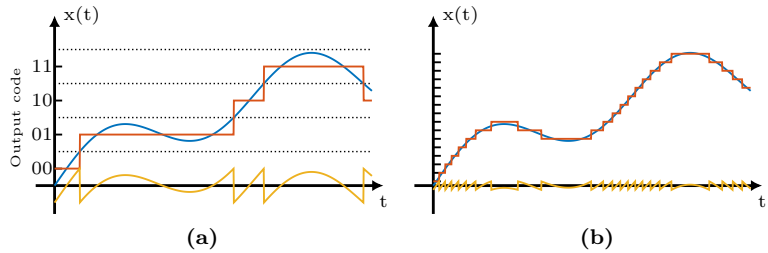


Figure 2.5: Signal, quantized signal, and resulting quantization error (a) for a 2 bit resolution and (b) for a 4 bit resolution. The boarders and output code for each quantization level are show in (a).

The equation implies that for a signal to be reconstructible based on the sampled representation, it must be band-limited. This requirement must not only be fulfilled by the desired signal but also by the noise. Hence, to guarantee a band-limited signal, an anti-aliasing filter is needed to suppress signals outside the desired band.

$$BW < \frac{f_s}{2} \tag{2.3}$$

In its basic form, the Nyquist criterion assumes signals in the range $[0, f_s/2)$. However, equation (2.3) can be extended into equation (2.4) allowing for other bands to be covered. It is assumed that the entire signal falls within the same Nyquist band; thus the freedom when selecting a sample rate becomes reduced, in order to avoid folding [13, Ch. 1].

$$f_H - f_L < \frac{f_s}{2} \tag{2.4}$$

The Nyquist criterion, not only applies when sampling a signal, it also applies to the reconstruction of the signal. Thus, the sample rate in a DAC is governed by the same principles as an ADC. There is however one difference regarding what the sample represents. In a DAC, a sample is represented at the output during its entire duration. This is in contrast to an ADC, where a sample only represents the signal at a specific point in time. This guarantees a one-to-one mapping between the discrete-time and continuous-time representation.

2.2.2 Quantization

Quantization is similar to sampling in the sense that we take a continuous signal and generate a discrete representation. In an ADC, quantization is performed by rounding the input signal to the closest level, making each quantization level correspond to a range of continuous values. Hence, information gets lost and errors are introduced. A DAC on the other hand uses the discrete voltage levels when generating an output signal, having a one-to-one mapping between the

input code and the output value. To smoothen the signal, a reconstruction filter is needed, suppressing the artefacts introduced by the ZOH.

The number of quantization levels not only sets the accuracy of the signal representation, it also defines the achievable dynamic range (DR); the ratio between the largest signal level the converter can handle and the noise level [13, Ch. 1]. For a data converter with a low resolution, resulting in few quantization levels, a limited DR can be achieved. With an increased resolution, the number of quantization levels increases and thus also the DR. The quantization step size Δ in equation (2.5) is given by the full-scale range of the signal X_{FS} and the converter resolution N. In figure 2.5, a signal is quantized using two different resolutions. From the figure, we can see how the resolution affects the accuracy of the discrete representation and the size of the error being made while quantizing the signal.

$$\Delta = \frac{X_{FS}}{2^N} \tag{2.5}$$

2.3 Limits for high-speed data converters

The achievable performance in high-speed data converters is limited by a combination of theoretical and implementation-related limitations. Some are directly related to the converter resolution while other effects may be reduced at a cost, typically in terms of area and/or power.

2.3.1 Quantization noise

Quantization is the process of turning a continuous signal into a discrete representation with a limited set of levels resulting in the introduction of errors. The error can only be zero when an infinite number of quantization levels are used, which is impossible to realize in practice. For a quantizer with the output represented by the mid-point of the quantization interval, the maximum error is half the size of the quantization step ($\Delta/2$). The average error on the other hand is highly dependent on the signal [13, Ch. 1]. Given the three following circumstances, the quantization error can be treated as white noise [13, Ch. 1]: The probability of reaching any quantization level should be equal; the quantization errors should be uncorrelated with the input signal; and a large number of equally sized quantization levels are required. Hence, the signal must be changing over time and have an amplitude large enough to occupy a large portion of the input range.

Given the assumption of a uniform distribution of the quantization error $p(\epsilon_Q) = 1/\Delta$ in the range $[-\Delta/2, \Delta/2]$, equation (2.6) gives the average quantization noise.

$$P_Q = \int_{-\infty}^{\infty} \epsilon_Q^2 p(\epsilon_Q)\, \mathrm{d}\epsilon_Q = \int_{-\Delta/2}^{\Delta/2} \frac{\epsilon_Q^2}{\Delta} \mathrm{d}\epsilon_Q = \frac{\Delta^2}{12} \tag{2.6}$$

The power for a full-scale sine wave is given by equation (2.7). The ratio between this signal power and the noise power in equation (2.6) gives the SNR in equation (2.8). This expression gives the highest theoretically achievable SNR for a given resolution, assuming uniform quantization.

$$\mathrm{P}_{sig} = \frac{1}{T}\int_0^T \left(\frac{\mathrm{X}_{FS}}{2}\sin(\omega t)\right)^2 \mathrm{d}t = \frac{\mathrm{X}_{FS}^2}{8} = \frac{\left(2^N\Delta\right)^2}{8} \tag{2.7}$$

$$\mathrm{SNR}_Q = 10\log_{10}\left(\frac{2^{2N}\Delta^2}{8}\frac{12}{\Delta^2}\right) = 6.02N + 1.76 \quad [\mathrm{dB}] \tag{2.8}$$

2.3.2 Component matching

Due to process variations, no device is identical to another one. All devices: capacitors, resistors, and transistors all experience the effect of variations [11, Ch. 5]. On-chip process variations can be divided into two categories: local variations between devices located close to each other on the chip, and global variations among chips from the same wafer or in between wafers. However, not all contributions to inaccuracies come from process variations. Asymmetries in the placement and routing of devices may also affect the matching. With high-speed signals, even a small asymmetry in the routing might have a large impact on the overall matching.

There are however methods that can be used to reduce the impact of variations. Designing circuits that rely on ratios rather than using absolute values makes it possible to reduce the effects of global variations. Still, even with only local variations, device mismatch is an issue. In some cases, calibration can be adopted to tune out the effects of component mismatch [15]. Other effects of mismatch can be compensated for in the digital domain. However, calibration in analog and/or digital form cannot do magic. The device placement and routing still largely impact the achievable matching accuracy. Component dimensions, i.e. length and width, also affect the achievable accuracy [16]. The influence of length and/or width effects reduces with increased device sizes as the dimension error is relatively independent of the absolute dimension, thus making the relative error smaller for larger components [17, Ch. 7].

A matching problem often present in ADCs is the large component ratios required for the binary-weighted cells used when generating the decision levels. Large component ratios are hard to accurately match as device properties are not linear with respect to length and/or width. This problem can however be managed by connecting several smaller devices, often referred to as unit cells, in series and/or parallel depending on needs. Distributing groups with a large number of unit cells and locating those with a smaller number in the middle allows for gradient variation effects to be averaged in the large groups thus further improving the achievable matching.

Above, all discussions have targeted static mismatch effects. However, dynamic properties might also affect the resulting matching accuracy. This can

include local IR drops in the supply network and variations in the edge rates for control signals to mention a few. For example, in an array of distributed unit cells, the number of *active* cells will impact the currents in that row or column and as a result, affect the accuracy of their contribution. Effects of dynamic mismatch might sometimes be harder to estimate and also harder to consider as they to some extent are signal-dependent.

The most important thing about matching is however to identify the devices within the circuit where the impact of mismatch has the greatest effect on the performance.

2.3.3 Jitter

In general, when processing a sampled signal one assumes a uniform distribution of the samples over time. This greatly simplifies DSP as the time-stepping will be equal. In real circuit implementations, there is always a small variation in the arrival of the edges, known as jitter, for example, due to finite rise- and fall-times of the control signals. Jitter is also known as the time-domain equivalent of phase noise. In a sampled system, the time instance for sampling or updating the signal will be sensitive to variations in the clock arrival.

When sampling a signal at a slightly wrong time, a small error will be introduced due to our assumption of uniform sampling [11, Ch. 2]. Assuming the time error $\Delta T\,(t)$ to be small, the sampled magnitude error will depend not only on $\Delta T\,(t)$ but also on the slope of the signal at this point [13, Ch. 1]. For a sine wave signal, the noise power due to jitter is given by equation (2.9). For more complex signals, the expression can be calculated using the signal derivative. The resulting SNR degradation due to jitter is then given by equation (2.10).

$$x_j^2\,(t) = A^2\omega_{in}^2\cos^2\left(\omega_{in}t\right)\Delta T\,(t) \tag{2.9}$$

$$\mathrm{SNR}_{ji} = 20\cdot\log_{10}\left(\omega_{in}\Delta T_{rms}\right) \quad [\mathrm{dB}] \tag{2.10}$$

Jitter can also be related to the quantization noise and thus also to the resolution, assuming a full-scale input signal. In equation (2.11), the allowable jitter for a noise contribution equal to the quantization noise is given as a function of the signal frequency and the quantizer's resolution.

$$\Delta T_{rms} = \sqrt{\frac{2}{3}}\frac{1}{2^N\omega_{in}} \quad [\mathrm{s}] \tag{2.11}$$

As can be seen from the equations above, the tolerable jitter is tightly connected to both the signal frequency and the resolution of the quantizer. Hence, in high-speed, high-resolution data converters, jitter can be a serious problem that is hard to overcome. In digital circuits, jitter in the order of tens of picoseconds root-mean-square (RMS) is commonly seen [11, Ch. 2]. In high-speed, high-resolution data converters on the other hand, jitter $<1\,\mathrm{ps}_{rms}$

may be required. However, reaching below $100\,\mathrm{fs}_{rms}$ becomes very challenging with only a few demonstrated implementations [18].

Jitter will behave slightly different in a DAC compared to an ADC as a result of it discrete-time representation [19]. Just as for an ADC, the impact of jitter in a DAC is dependent on the signal derivative. However, the discrete-time derivative is dependent on architectural properties, such as resolution and OSR [19]. One can however only take advantage of over-sampling if the resolution is sufficiently high, such that new signal values can be realized between the previous ones, reducing the signal's slope.

In addition to clock jitter, RF-DAC-based transmitters also suffer from LO signal phase noise. The presence of significant phase noise is indicated by a rotational effect on the transmitted constellation. This is however an impairment from which other transmitter topologies also suffer.

Chapter 3

RF-IQ modulator: Concepts and principles

In this chapter, I present design concepts and performance metrics used for comparing implementations of RF-DAC-based in-phase/quadrature (IQ)-modulators. This not only includes RF-DACs, but also the quadrature LO generation. This chapter is intended as a base for the presentation of the related work in section 6.1, and the implementations presented in papers A and B with an extended discussion in chapter 7.

3.1 Architectures

Traditionally, direct-conversion or superheterodyne transmitters are typically chosen for mm-Wave transmitter realizations. However, with the increased performance brought by modern CMOS processes, alternative topologies, where the cross-over between digital and analog is shifted closer towards the antenna, receive increased interest. Three such topologies are the Cartesian modulator, the polar modulator, and the outphasing modulator. All these three topologies are based on the direct-conversion principle, but combine digital-to-analog conversion and up-conversion in a single component. The operational principles for all these three topologies will be described below.

3.1.1 Cartesian modulator

The Cartesian RF-DAC-based modulator is the topology that has the most similarities with the direct-converting modulator. It uses two RF-DACs fed with quadrature LO signals; thus, each DAC produces one of the quadrature components. These components are then summed to form the output signal. A generic Cartesian modulator is illustrated in figure 3.1a, and the vector summation forming the output is shown figure 3.1b. Here we can see that this

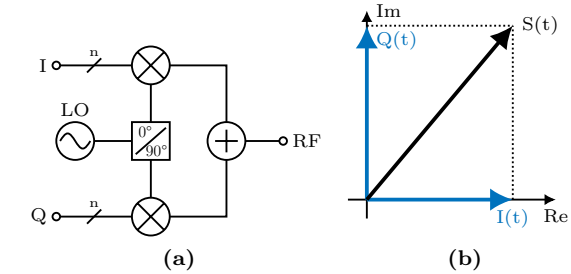


Figure 3.1: (a) Illustration of a generic Cartesian modulator and (b) the vector summation that forms the output signal.

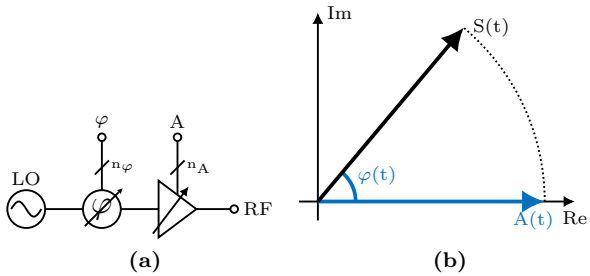


Figure 3.2: (a) Illustration of a generic polar modulator and (b) the vector summation that forms the output signal.

topology fully relies on amplitude modulation and that the phase modulation is realized through the summation of the quadrature components.

3.1.2 Polar modulator

In a polar modulator, the modulation is divided into two steps, first modulating the signal phase and then modulating its amplitude. Hence, this topology only requires a single RF-DAC [20], in contrast to the Cartesian topology where two RF-DACs are required. On the other hand, a phase modulator is needed. In figure 3.2a, a generic polar modulator is visualized and in figure 3.2b the vector summation of the phase φ and amplitude A gives the desired output signal.

3.1.3 Outphasing modulator

The outphasing modulator differs from the other two topologies in the sense that it uses a fixed amplitude and then just tune the phases to modulate the output amplitude [21]. The amplitude modulation is realized by changing the outphasing angle θ and then summing the channels. With an increased outphasing angle, the vector summation brings a lower amplitude, thereby realizing amplitude modulation. An outphasing modulator does not require any

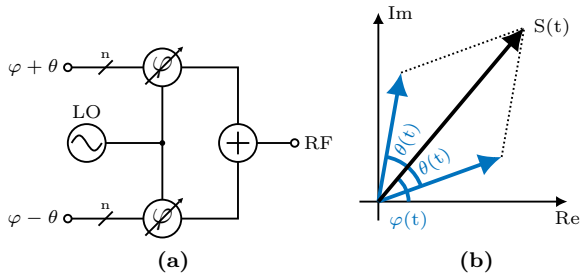


Figure 3.3: (a) Illustration of an outphasing modulator and (b) the vector summation that forms the output signal.

RF-DAC but requires two phase modulators. A generic outphasing modulator is illustrated in figure 3.3a, and the vector summing that forms the output is illustrated in figure 3.3b.

3.2 Quadrature LO generation

As may be seen in figure 3.1, the quadrature LO generation is an essential part of a Cartesian modulator. It combines the generation of accurate quadrature LO signals with the buffering required to drive the RF-DACs.

3.2.1 Architectures

Quadrature LO signals can be generated in different ways. A quadrature oscillator can combine frequency generation with the generation of quadrature LO signals [22, Ch. 8]. However, for greater flexibility when evaluating the chip, it is desirable to feed a single-phase LO to the chip and generate the quadrature phases from this signal. Both passive and active circuits, including 90° hybrids, dividers, and poly-phase filters (PPFs) may be used.

A 90° hybrid is a passive circuit that uses $\lambda/4$ microstrip lines to output signals with 90° phase difference. As illustrated in figure 3.4, the 4-port circuit has one input, two outputs with 90° phase offset, and an isolated port [23, Ch. 7]. To create all four phases, baluns are required on each output (not included in the figure) to convert the single-ended signals into differential signals, thus giving us all four quadrature phases. Although it is desirable that the quadrature LO signals have equal amplitude, and thereby the same power, hybrids can be designed for unequal power split and different impedances at the input and output ports [24, Ch. 4].

As a result of the $\lambda/4$ length requirement, hybrids have a limited operational bandwidth of around 10–20 %; that limitation however may be relaxed by cascading multiple hybrids [23, Ch. 7]. However, at mm-Wave frequencies, the physical dimensions are too large for a practical on-chip implementation [24,

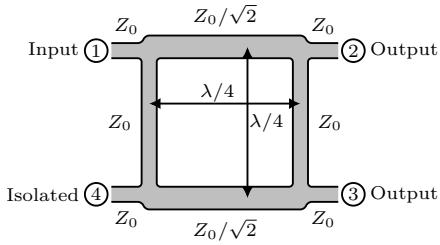


Figure 3.4: Illustration of a 90° hybrid with the lengths and characteristic impedances of the transmission lines. Z_0 is often assumed to be 50 Ω.

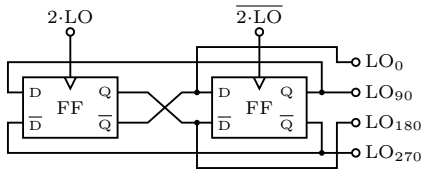


Figure 3.5: Schematic of a divide-by-two circuit used to generate quadrature LO signals.

Ch. 4]. Thankfully, there are techniques for reducing the required transmission line length, at the cost of a slight bandwidth reduction. Lumped LC networks can further reduce the footprint while providing increased design space. However, the limited inductor quality factor will result in amplitude and phase imbalance, limiting the achievable performance [24, Ch. 4].

Through a divide-by-two circuit, quadrature LO signals can be generated from a differential input signal at twice the frequency. The accuracy of this differential input signal is directly connected to the achievable phase imbalance. In figure 3.5, the schematic of a divide-by-two circuit is shown. With the divider approach, quadrature signals can, in principle, be realized from direct current (DC) up to half of the highest clocking rate for the flip-flop (FF)'s [22, Ch. 4]. With no passive elements needed when realizing the divide-by-two circuit, its footprint becomes very small, making it an attractive choice within its operating range.

Poly-phase filters traditionally use a combination of resistors and capacitors to shift the phases of the incoming signal while providing 90° phase offset between the output signals. At the RC pole frequency $\omega_\mathrm{i} = 1/(R_i C_i)$, there is no amplitude or phase imbalance. However, away from this pole frequency, amplitude or phase imbalance increases. By cascading multiple filters, the bandwidth can be increased, especially if the segments come with different pole frequencies [25]. The number of segments required may be derived based on the desired bandwidth and required amplitude/phase imbalance [25]. However, cascading multiple segments will introduce a loss of 3 dB per stage [25]. In

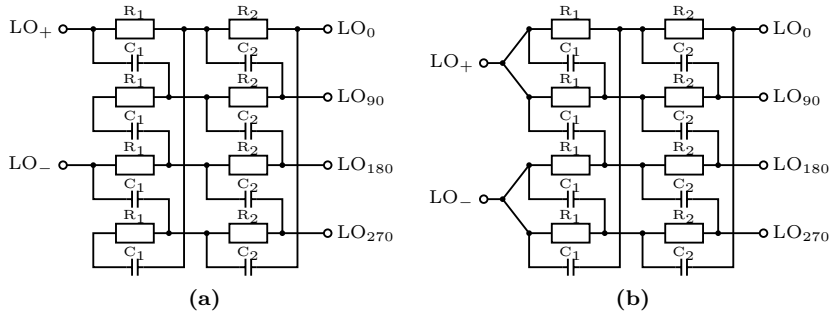


Figure 3.6: Schematic of 2-stage PPFs with resulting (a) amplitude imbalance and (b) phase imbalance caused by the feeding principle.

figure 3.6, two different ways of driving the PPF using a single input pair are presented. The feeding illustrated in figure 3.6a will result in amplitude imbalance, while perfect 90° phase offsets are achieved over all frequencies [25]. In contrast, using the approach in figure 3.6b, we will see phase imbalance but no amplitude imbalance. Active versions of the PPF can be realized using the transistor's transconductance g_m [26, 27]. However, the phase order is reversed in an active PPF compared to the passive realizations shown in figure 3.6.

3.2.2 Impact of load

A quadrature LO generator is a block that typically drives another circuit, either an IQ mixer or an RF-DAC-based modulator. However, these two circuits present very different loads. A mixer often uses smaller transistors and comes with a compact layout, presenting a small load on the LO buffers. A RF-DAC-based implementation on the other hand may be seen as a distributed mixer, but with a significantly larger total transistor size spread over a larger area. In addition, the routing needed to connect all unit cells further increases the load seen by the LO buffers. With an increased load, the cost of driving that load also increases. Typically, one or several buffer stages are needed when the load increases, causing an increased power consumption and footprint together with reduced bandwidth.

For both mixers and RF-DACs, it is desirable to have a high-power LO signal at the input [23, Ch. 13], which for metal-oxide-semiconductor field-effect transistors (MOSFETs) translates into a large voltage swing at the gate. However, with the limited supply voltage in modern CMOS processes, a large swing is hard to come by.

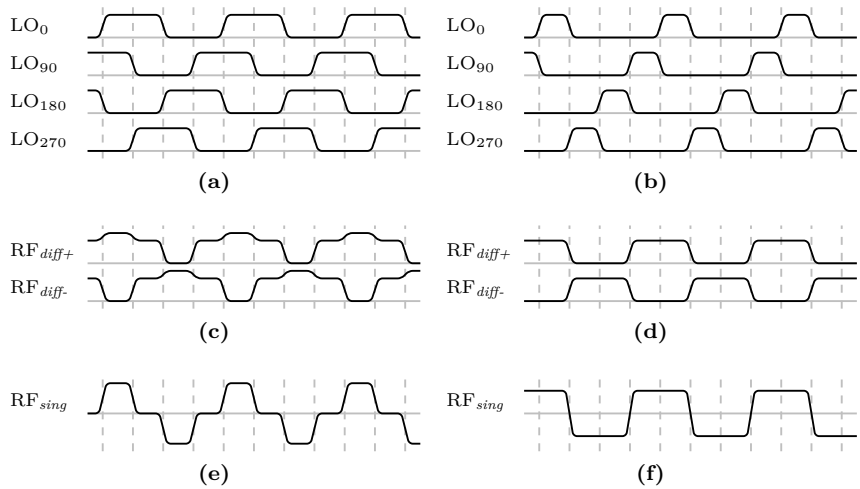


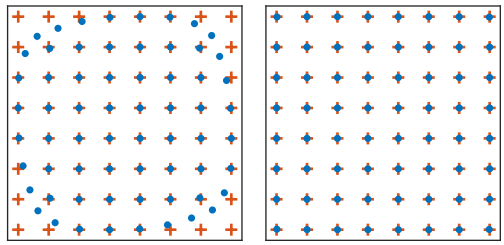
Figure 3.7: Quadrature LO signals with (a) 50 % duty-cycle and (b) 25 % duty-cycle. LO_0 and LO_{90} (LO_{180} and LO_{270}) are then combined into RF_{diff+} (RF_{diff-}) in (c) and (d) for the two duty-cycles. The resulting RF signal is then shown for the 50 % and 25 % cases in (e) and (f) respectively.

3.2.3 Duty cycle

The signal duty cycle is rarely considered in analog circuit design. Sine-wave signals are not only considered for the LO generation but they are also the carrier in modulated signals. By definition, a pure sine-wave has no harmonics and is symmetrical around its DC-level. These are in most cases desirable properties; however, for mixers where a high-power LO signal is desirable, a compressed sine-wave signal might be of interest. The more the sine-wave signal is compressed, the more it resembles a square wave. The duty cycle is one of the properties that describe the shape of a square-wave signal. It is defined as the ratio between the duration where the pulse is above the average signal value and its period. With this definition, a symmetrically compressed sine-wave signal approaches a 50 % duty-cycle square-wave signal.

In most cases, using a 50 % duty-cycle signal is not a problem. However, in summed RF-DAC-based topologies such as the Cartesian, a 50 % duty-cycle may cause the individual branches to interact, causing cross-modulation distortion. This interaction between the RF-DACs may be eliminated using fully orthogonal LO signals, a requirement not fulfilled by 50 % duty cycle signals [28].

The undesired interaction may be avoided by using lower-duty-cycle signals. As an example, we take four LO signals, for both the 25 % and 50 % duty-cycle cases, and combine them as they would be combined at the output of a Cartesian modulator. The differential signal RF_{diff+} is generated by combining LO_0 and LO_{90} as defined in equation (3.1). Similarly, LO_{180} and LO_{270} are used to generate RF_{diff-}. The single-ended signal is then given by combining the two



(a) (b)

Figure 3.8: Effects of cross-modulation distortion caused by directly summing the RF-DACs outputs in a Cartesian modulator using (a) LO signals with 50 % duty cycle and (b) LO signals with 25 % duty cycle. The reference grid is shown in orange.

differential components, as in equation (3.2). The waveforms are illustrated in figure 3.7 for both duty-cycles. From the figure, we can observe how the LO signals overlap with each other when a 50 % duty cycle is used while there is no overlap for LO signals with 25 % duty cycle. The resulting large overlap of the differential signals also results in the cancellation of significant portions of the signals when generating the single-ended signal, bringing a significant efficiency reduction.

$$\mathrm{RF}_{diff+} = \mathrm{LO}_0 + \mathrm{LO}_{90} \tag{3.1}$$

$$\mathrm{RF}_{sing} = \mathrm{RF}_{diff+} - \mathrm{RF}_{diff-} \tag{3.2}$$

The effect of duty-cycle-related cross-modulation can also be seen in the transmitted constellation. In figure 3.8, it can be observed how the cross-modulation distortion affects the constellation points located in the corners when a 50 % duty cycle is used while a perfectly square constellation is achieved with 25 % duty cycle. This assumes LO signals with rise- and fall-times significantly shorter than the period, and direct summation of the quadrature components.

While *perfect* 25 % duty-cycle signals are possible to approach at low frequencies, they becomes significantly harder to realize at mm-Wave frequencies. This is due to the limited gain provided by the transistors at high frequencies, limiting the number of usable harmonics. In figure 3.9, a 25 % duty-cycle signal is approached using a limited number of harmonics. With exactly 25 % duty cycle, the fourth harmonic becomes a zero, thus making this realization identical to the case when only the third harmonic is used.

3.3 Effects of component matching in RF-DACs

As indicated in section 2.3.2, devices with large footprints are typically less sensitive to manufacturing variations than components with a small footprint.

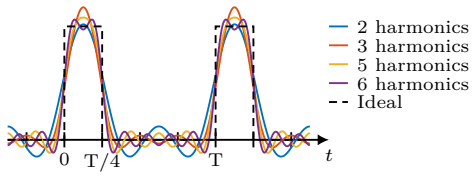


Figure 3.9: Two periods of a 25 % duty-cycle signal realized using a limited number of harmonics. One should observe that the forth harmonic is zero for a 25 % duty cycle.

For a given converter resolution, the required output level accuracy can be derived. This then translates into a requirement for the minimum device size needed to achieve this accuracy. In RF-DAC-based circuits, the maximum output power scales with the number of unit cells and with their size. Clearly, with increased resolution, the minimum full-scale output power increases not only due to an increased number of unit cells but also as a result of the increased device size required for sufficient matching accuracy.

The maximum achievable output power for a RF-DAC on the other hand is limited by the driving capabilities of the LO-chain. As the RF-DAC input load is proportional to the delivered output power, the maximum achievable output power thus is independent of the RF-DAC resolution.

As both these points need to be considered in an actual implementation, we can observe that the design space for selecting a full-scale output power reduces with increased resolution. For each additional bit of resolution, the design space will shrink by 6 dB. This does however not include the required device scaling needed to achieve a good device matching, thus, in reality, the design space will shrink even faster.

3.4 Non-linear scaling

Traditionally, DACs have a uniform quantization step across the entire range. That is, the effect of toggling the least significant bit (LSB) will be the same for all input codes. The uniform quantization step is realized using either binary scaled stages or through thermometer-coded unit cells, both realizing a linear mapping between the input code and the enabled transistor width which is proportional to the output magnitude. This however assumes that no compression effects are present. With compression, the smallest output step will reduce with increased output code.

To compensate for the compression, an expanding non-linear input-output relation is needed. This may be achieved by using DSP at the cost of a reduced effective resolution, or by using thermometer encoding and non-uniform unit cell sizes. Through careful selection of the unit cell sizes, a linear transfer from input code to output magnitude can be achieved even when compression is present.

In practice, it is however not realistic to make unit cells with unique sizes. With a segmented scaling, it is possible to realize an approximate expanding non-linear function using only a small number of segments and thereby also a small number of unit cells having a unique size [29].

3.5 Testability

Evaluating a fabricated design is just as important as the actual implementation. However, testing is rarely as easy as connecting some power supplies and monitoring the output. With increased circuit complexity the number of biasing and supply signals may rapidly increase, becoming problematic not only from a measurement perspective but also from a design perspective as a large number of connection points make the circuit large. To simplify the measurement setup and avoid problematic interconnect problems, it is important to think through the testing already at design time.

When measuring multi-stage RF circuits, it is often desirable to be able to tune the bias in the different stages to change properties or find the last bit of performance. With a potentially large number of biasing signals, it soon becomes impractical to externally feed these onto the chip. Typically, a biasing signal only draws a small current, in contrast to the larger currents drawn from the supply nets. This makes the biasing signals highly suitable for an on-chip generation with digital control. The digital control signals can then be set using a compact serial interface with a small footprint.

Another consideration when evaluating RF-DAC-based circuits is their high sample rate and for controlling them, digital control words need to be delivered at a high speed. Already at moderate resolutions and sample rates, a Cartesian modulator using two RF-DACs may require data at a rate exceeding 100 Gb/s. These high data rates are impractical if not even impossible to externally feed into the chip. Either, a high-speed digital interface is used, potentially limiting the performance, or the data is sourced on-chip, keeping the high-speed signals within the chip boundaries. As performance evaluations typically involve several different tests requiring different input signals, it is important to have flexible data generation. An on-chip static random-access memory (SRAM) programmed using a low-speed serial interface, allows for both flexible waveforms and a simplified measurement setup thanks to the low-speed interface. With a limited chip area, the memory depth needs to be carefully selected. A shallow memory will be compact but may limit the test signals that may be used. A deep memory on the other hand will occupy a larger area, but might not bring additional benefits from a testing perspective.

3.6 Figures of merit

In contrast to ADCs, there are no generally accepted comparison metrics for RF-DAC-based modulators that account for complexity, and thus fairly comparing

different implementations is challenging. Also, as it is highly beneficial to co-integrate multiple functions into the modulator block, it is problematic to isolate the parts that should be included in a comparison metric. In addition to this, the large span of output power levels and carrier frequencies further complicates the comparison. The selected modulation formats must also be compared with the modulator resolution, as higher resolution ideally should bring a more accurate constellation.

Traditional comparison metrics used for DACs, such as linearity and signal-to-noise-and-distortion ratio (SNDR), are also problematic to use. The static linearity does not give any indication of the linearity for wideband signals. The narrow-band signal used when characterizing the SNDR also poorly matches the behaviour with wideband signals.

In addition to the carrier frequency, output power, DC power consumption, and resolution, there are few metrics commonly used when comparing different RF-DAC-based modulator implementations. These include LO leakage, error vector magnitude (EVM), adjacent channel power ratio (ACPR), and image rejection ratio (IRR). As some comparison metrics are highly affected by the carrier frequency, the output power, and the modulator resolution, it is important to keep these values in mind.

3.6.1 LO leakage

In direct-converting transmitters, leakage from the LO signals to the transmitter output is problematic. RF-DAC-based implementations require special attention due to their distributed layout and significant amount of routing. The LO tone will appear centered in the transmitted band, thus, when down-converting the signal in a receiver, it will be translated into a DC offset. This offset is complex to filter out and might be significantly amplified in the receiver's baseband path.

In some cases, it is possible to digitally compensate for LO leakage on the transmitter side. This however requires a relatively small leakage to start with as digital resolution is sacrificed in proportion to the compensated leakage. Also, in general, digital compensation can at most suppress the LO leakage to 3 dB below the output level of the LSB. Hence, the achievable compensated LO leakage becomes dependent on the modulator's resolution.

3.6.2 Error vector magnitude

The EVM is a measure of the accuracy of the transmitted constellation compared with the intended one. It is typically measured either as the RMS error normalised to the average constellation power $\mathrm{EVM}_{\mathrm{RMS}}$, or to the highest constellation power $\mathrm{EVM}_{\mathrm{RMS,peak}}$.

Figure 3.10 illustrates the EVM definition for a single point. With the error given by equation (3.3), the EVM for a single point is given by equation (3.4). However, when analysing performance, the EVM for a single point is not of interest, but rather the average behaviour for many points. Thus, we can

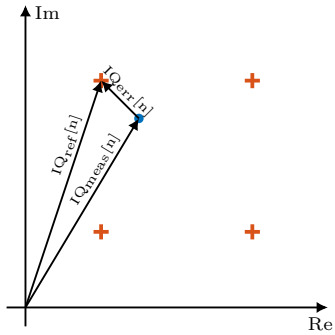


Figure 3.10: Illustration of the EVM definition for a single point.

extend equation (3.4) into equation (3.5) for an EVM normalized to the average constellation power, and to equation (3.6) for an EVM normalized to the peak constellation power. With an RMS-based EVM, comparisons between modulation formats become possible [12, Ch. 5].

$$\mathrm{IQ}_{err} = \mathrm{IQ}_{meas} - \mathrm{IQ}_{ref} \tag{3.3}$$

$$\mathrm{EVM}\,[n] = \frac{|\mathrm{IQ}_{err}\,[n]|}{\left|\mathrm{IQ}_{ref}\,[n]\right|} \tag{3.4}$$

$$\mathrm{EVM}_{RMS} = \frac{\mathrm{rms}\left(|\mathrm{IQ}_{err}|\right)}{\mathrm{rms}\left(\left|\mathrm{IQ}_{ref}\right|\right)} \tag{3.5}$$

$$\mathrm{EVM}_{RMS,peak} = \frac{\mathrm{rms}\left(|\mathrm{IQ}_{err}|\right)}{\max\left(\left|\mathrm{IQ}_{ref}\right|\right)} \tag{3.6}$$

In an actual communication system, the received constellation is contaminated with noise coming from three sources: the transmitter, the channel, and the receiver. With noise, errors will be introduced in the transmitted data stream. The BER is a measure of the probability that an erroneous bit is received. As both EVM and BER are related to the SNR of the received signal, one may connect them. Assuming an AWGN channel, the bit-error probability for a QAM constellation is given by equation (3.7), substituting $P_{e\sqrt{M}}$ with equation (3.8) [12, Ch. 2]. In these equations, M is the constellation size, BW is the bandwidth of the system, and BR is the bit rate. $Q\,(x)$ is the Q-function, often seen in error-probability expressions [12, Ch. 2].

$$P_b\,(M) = \frac{2P_{e\sqrt{M}}}{\log_2 M}\left(1 - \frac{1}{2}P_{e\sqrt{M}}\right) \tag{3.7}$$

$$P_{e\sqrt{M}} \cong \frac{2\left(\sqrt{M}-1\right)}{\sqrt{M}}Q\left(\sqrt{3\frac{\log_2 M}{M-1}\frac{\mathrm{BW}}{\mathrm{BR}}\mathrm{SNR}}\right) \tag{3.8}$$

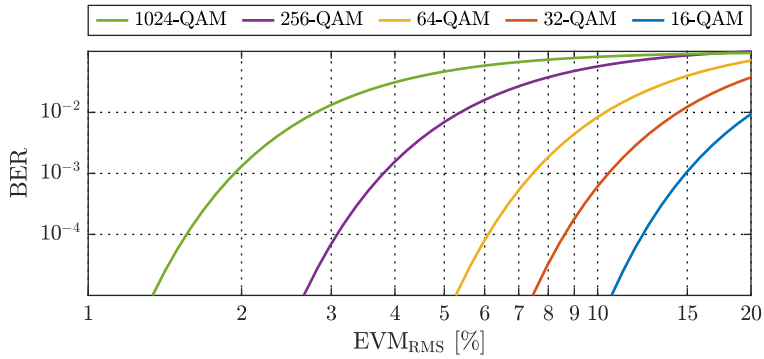


Figure 3.11: BER versus $\mathrm{EVM_{RMS}}$ for various modulation formats

For an AWGN channel where bit-errors are caused by the additive noise [30], the SNR is given as the average signal over the average noise, thus, $\mathrm{EVM_{RMS}}$ is related to SNR as in equation (3.9).

$$\mathrm{EVM_{RMS}} = \frac{1}{\sqrt{\mathrm{SNR}}} \tag{3.9}$$

With the crest factor c, the relationship between maximum and average constellation magnitude is defined, while PAPR gives the corresponding power ratio. The expression for the modulation-format-dependent ratio is given by equation (3.10), where M is the modulation size [31–33]. With EVM being inversely proportional to the signal power, equation (3.11) relates $\mathrm{EVM_{RMS,peak}}$ and $\mathrm{EVM_{RMS}}$.

$$c = \sqrt{\mathrm{PAPR}} = \sqrt{3\frac{\sqrt{M}-1}{\sqrt{M}+1}} \tag{3.10}$$

$$\mathrm{EVM_{RMS,peak}} = \frac{1}{c}\mathrm{EVM_{RMS}} \tag{3.11}$$

In figure 3.11, the relationship between $\mathrm{EVM_{RMS}}$ and BER is plotted for several modulation formats with varying complexity. Typically, in high-capacity wireless systems an input BER of 10^{-3} is targeted. DSP including error-correcting capabilities then further reduces the BER [30]. From the figure, we can observe that with a quadrupled number of constellation points, the required EVM must be halved for a constant BER.

As EVM is such an important comparison metric, it becomes important to know what sources that likely limit the performance already at design time [34, 35]. Equation (3.12) shows a few different sources that are dominant in mm-Wave transmitters [34]. With the assumption that these sources are uncorrelated, their effect will be combined. In reality, numerous other sources also influence the EVM.

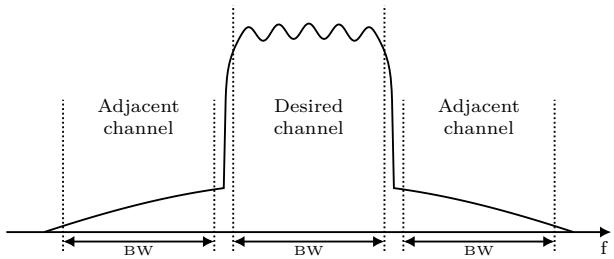


Figure 3.12: Illustration of the channels used when calculating ACPR.

$$\mathrm{EVM_{tot}} \approx \sqrt{\frac{1}{\mathrm{SNDR}^2} + \varphi_{\mathrm{RMS}}^2 + \mathrm{EVM_{IRR}^2} + \mathrm{EVM_{LOFT}^2} + \mathrm{EVM_{GF}^2}} \tag{3.12}$$

3.6.3 Adjacent channel power ratio

In addition to an accurate in-band signal, it is also important that the transmitter does not radiate in neighbouring channels. ACPR, also known as adjacent channel leakage ratio (ACLR), is a measure of the amount of radiated power in the neighbouring channel relative to the power in the desired channel, see equation (3.13) [12, Ch. 5]. Non-linearities and imbalances in the transmitter cause power to be radiated at undesired frequencies making ACPR a measure of the transmitter's linearity. Figure 3.12 illustrates the channels considered when computing the ACPR.

$$\mathrm{ACPR} = \max_{c=1,2} \left(\frac{P_{adj,c}}{P_{ch}} \right) \tag{3.13}$$

3.6.4 Image rejection ratio

For a receiver, the IRR is defined as the ratio between the desired sideband and its image sideband. Although originating as a metric to evaluate receivers, the metric is also suitable for evaluating the accuracy of the quadrature LO signals driving a Cartesian modulator. The concept was first introduced by Norgaard [36] and is defined in equation (3.14). Here, A_{bal} is the amplitude ratio between the I and Q components, and $\Delta\theta$ is the deviation from the ideal 90° phase difference between the I and Q components.

$$\mathrm{IRR} = \frac{1 + 2A_{bal}\cos(\Delta\theta) + A_{bal}^2}{1 - 2A_{bal}\cos(\Delta\theta) + A_{bal}^2} \tag{3.14}$$

Assuming an perfect amplitude balance or zero phase difference allows the IRR to separately defined for the amplitude imbalance $\mathrm{IRR_{gain}}$ and phase deviation $\mathrm{IRR_{phase}}$ using equations (3.15) and (3.16) [25]. With these equations, we

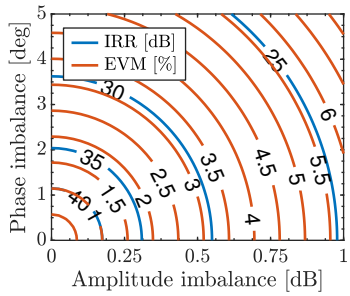


Figure 3.13: IRR and resulting EVM for different amplitude and phase imbalances.

can now relate amplitude and phase imbalance provided by a circuit generating quadrature LO signals to an IRR, and thus understand the severity of the imbalance.

$$\mathrm{IRR_{gain}} = \mathrm{IRR}_{\Delta\theta=0} = \left(\frac{1 + A_{bal}^2}{1 - A_{bal}^2}\right) \tag{3.15}$$

$$\mathrm{IRR_{phase}} = \mathrm{IRR}_{\mathrm{A_{bal}}=1} = \cot^2\left(\frac{\Delta\theta}{2}\right) \tag{3.16}$$

Amplitude and/or phase imbalance is one component that will degrade the achievable EVM in a mm-Wave transmitter [34, 35]. In figure 3.13, the IRR is plotted for some amplitude and phase imbalances. In addition, the figure also shows the EVM reduction related to these imbalances.

3.6.5 Efficiency metrics

Different efficiency metrics are of interest when comparing building blocks in a larger integrated system. For power amplifiers, both drain efficiency (DE) and power-added efficiency (PAE) are commonly used to evaluate the efficiency of an implementation. While DE only considers the power consumption in the output stage, equation (3.17), PAE accounts for all the power consumption in the analog path, equation (3.18). However, it is unclear how the power consumption for digital components in a RF-DAC are counted.

$$\mathrm{DE} = \frac{P_{RF,out}}{P_{DC}} \tag{3.17}$$

$$\mathrm{PAE} = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}} \tag{3.18}$$

An alternative comparison approach is to use the energy required to transmit a single bit. This becomes highly useful when comparing the performance not only for entire systems but also for smaller subsystems [37].

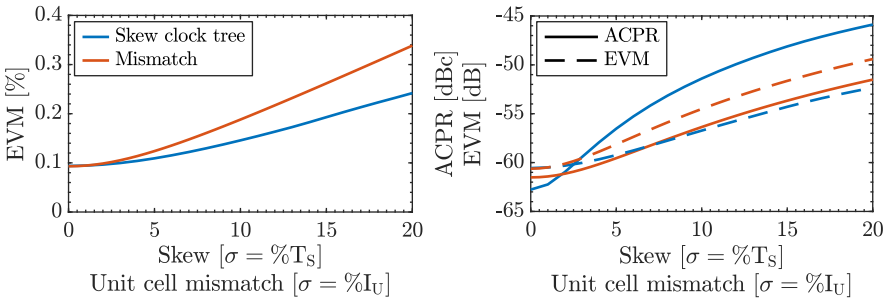


Figure 3.14: (a) EVM and (b) ACPR and EVM in dB, for different amounts of simulated skew in the clock network, and for unit cell mismatch.

None of these efficiency metrics are ideal for evaluating RF-IQ modulators. While DE and PAE to some extent account for variations in the output power, they neither account for the transmitter's bandwidth nor its carrier frequency. With the metric energy per bit, the transmitter's bandwidth is accounted for but neither the output power nor the carrier frequency. Due to the vast design space, making a comparison metric that accounts for both the circuit complexity and its performance in a fair way is extremely challenging. Hence, fair comparisons are elusive.

3.7 EVM and/or ACPR degradation

As mentioned above, EVM and ACPR are important metrics used to evaluate the accuracy of the transmitted signal. There are numerous sources causing a degraded transmitter performance, resulting in EVM and/or ACPR degradation. In addition to compression effects, two static sources are present in RF-DACs and DACs in general: random variations in the output levels caused by mismatch, and skew in the arrival of the control signals. If present, both these effects will degrade the transmitter performance resulting in reduced EVM and/or ACPR.

To better understand the impact of these effects, simulations has been performed using 256-QAM SC signals oversampled a factor of 4 and a modulator resolution of 2×10 b. By varying the mismatch or clock skew in these simulations, the EVM and ACPR presented in figure 3.14 are retrieved. Since mismatch will have a direct effect on levels outputted by the RF-DAC, and since the error is present during the full duration of the sample, it is clear that the error introduced will appear as noise both within the channel and in the adjacent channels. As expected, both EVM and ACPR are degraded roughly the same amount with increased mismatch, clearly visible in figure 3.14b. Skew, on the other hand, will only have a marginal impact on the levels outputted, thus it is expected to have a small impact on the EVM. With skew, in addition

to extending the time required for the transition from one level to the next, several intermediate levels will also be visited during short time periods, mostly resulting in high-frequency noise appearing in the adjacent channels. This explains why we can observe a large degradation in ACPR while the EVM only is degraded slightly.

In short, magnitude effects will degrade both EVM and ACPR with similar amounts. Timing misalignments, on the other hand, will have a greater impact on the ACPR than on the EVM.

Chapter 4

Predistortion: Theory and concepts

In this chapter, the concept behind predistortion will be introduced followed by an introduction of the three commonly adopted predistortion concepts. This chapter is intended as a base for the related work in section 6.2 and the linearization concept presented in paper C, which is extended in chapter 8.

4.1 Why and how?

The PA is the component within the transmitter that typically is responsible for a majority of the transmitter power consumption. For the highest PA efficiency, it is desirable to operate close to saturation. However, in saturation, the PA will suffer from its inherent non-linearities, introducing both in-band and out-of-band distortion [38]. For more linear operation, the PA can be operated with reduced output power, at the cost of compromising the power efficiency [38]. To operate the PA close to saturation while outputting a signal with little distortion, its non-linearities may be compensated for, before the signal reaches the PA. The inverse of the PA transfer characteristic must be applied to the signal to pre-distort it.

In figure 4.1, a conceptual predistorter-PA combination is showed together with the amplitude modulation to amplitude modulation (AMAM) transfer characteristic for the predistorter, the PA, and the cascaded pair. In figure 4.1c, the PA's AMAM transfer characteristic shows a significant compression for high input levels. For a linear output from the cascaded predistorter and PA, the predistorter transfer function must implement the inverse of the PA transfer characteristic. Figure 4.1b shows the expanding transfer function required by the predistorter to linearize the PA. Combining the two transfer functions in figure 4.1b and figure 4.1c gives the linear transfer characteristic shown in figure 4.1d. This example only considers the magnitude, but in the real case,

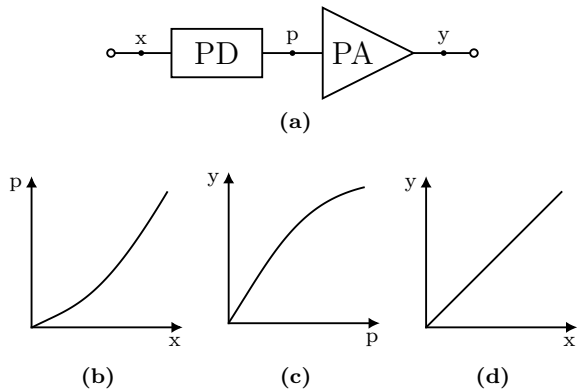


Figure 4.1: (a) Schematic of a combined predistorter and PA. Transfer function for the (b) predistorter, (c) PA, and (d) the cascaded predistorter and PA.

the phase behaviour is also important.

4.2 Predistortion techniques

The expanding transfer function needed to linearize a PA can be realized both in the analog and in the digital domain, filling different needs.

4.2.1 Analog predistortion

With analog predistortion (APD), the predistortion is realized using an additional circuit placed before the PA. This circuit often acts as a non-linear load, adjusting the attenuation of the input signal depending on the power level, to generate the desired expanding characteristic [39, Ch. 14]. In addition to significant signal power losses, APDs typically come with a limited range of compensation. They are however more suitable for wide bandwidths as the linearization is not dependent on the transmitter sample rate.

4.2.2 Digital predistortion

With digital predistortion (DPD), the predistortion is applied in the digital domain before the digital-to-analog conversion. This is the most commonly adopted predistortion technique [39, Ch. 14]. Here implementations are realized using lookup tables (LUTs) or using polynomial or Volterra-based functions. Thanks to the flexibility provided by DSP, DPD can be designed to handle a broader range of non-linear effects such as memory effects. In contrast to APDs, DPDs can also easily be updated with different parameters, thus making it possible to adapt the linearization to changing conditions. However, the computational cost rapidly increases when more complex models of the non-linearity are used [40]. Another drawback with DPD is that the sample rate

needs to be increased to also cover the non-linear components generated. This quickly becomes challenging in wideband systems [40].

4.2.3 Hybrid predistortion

Hybrid predistortion relies on a combination of APD and DPD. By combining both APD and DPD, the APD can compensate for static non-linearities, allowing for reduced DPD complexity, while still taking advantage of the adaptability brought by DPD.

Chapter 5

High-speed ADCs: Theory and concepts

This chapter covers theoretical background, design concepts, and performance metrics used for comparing different ADC implementations. The chapter is intended as a base for the presentation of the related work in section 6.3 and for the implementation of a high-speed ADC presented in paper D, with extended discussion in chapter 9.

5.1 Thermal noise

With quantization noise setting the theoretically lowest noise floor for data converters, the contribution from other noise sources must be smaller for a low overall noise level. Thermal noise is one of these other noise sources. It is present in all types of electronics and may limit the achievable performance in an ADC [13, Ch. 1]. In an ADC, the primary sensitivity to thermal noise lies in the sampling network consisting of a sample switch followed by a sampling capacitor storing the sampled voltage. Ideally, the switch should have no on-resistance but in practice, there will be a small on-resistance present, leading to noise. The noise is introduced by the random movement of electrons in the switch and it is connected to the device temperature and internal resistance [23, Ch. 10]. The noise is in nature white, spanning the entire frequency spectrum with an average power given by equation (5.1).

$$\overline{v_{n,R_s}^2} = \overline{4kTR_s} \tag{5.1}$$

The combined sampling switch and capacitor form a low-pass filter that band-limits the thermal noise, thereby reducing the sampled noise power [11, Ch. 2]. The band-limited noise power is given by equation (5.2) and the resulting total sampled thermal noise power is given by equation (5.3).

$$v_{n,C_s}^2(\omega) = \frac{\overline{4kTR_s}}{1 + (\omega R_s C_s)^2} \tag{5.2}$$

$$P_{n,C_s} = \int_0^\infty \frac{\overline{4kTR_s}}{1 + (2\pi f R_s C_s)^2} \mathrm{d}f = \frac{kT}{C_s} \quad [\mathrm{W}] \tag{5.3}$$

From equation (5.3), it is clear that the size of the sampling capacitor sets the sampled thermal noise power. By setting the thermal noise power equal to the quantization noise power, we can calculate the required sampling capacitance needed for a SNR reduction of 3 dB. Equation (5.4) then gives the desired capacitance as a function of the resolution. For a reduced thermal noise contribution, a larger sampling capacitor is needed.

$$C_s = \frac{kT}{v_{n,C_s}^2} = \frac{12 \cdot 2^{2N} kT}{V_{FS}^2} \quad [\mathrm{F}] \tag{5.4}$$

All these calculations assume a single-ended sampling circuit. What happens if the sampling circuit is differential? Assume that each of the two parallel channels is identical to the single-ended one, and that the same signal magnitude applied to the single-ended input is applied to both the differential inputs. This will result in a doubling of the sampled thermal noise power and a quadrupling of the signal power in the differential case [41, Ch. 6]. Hence, the SNR is improved by 3 dB. For a constant SNR, twice the amount of thermal noise can be tolerated in each channel, giving room for a 50 % reduction of the sampling capacitance in each channel. In the end, the same total sampling capacitance is required in both the single-ended and differential cases.

5.2 High-speed ADC architectures

For the implementation of high-speed ADCs, several architectures are of interest. These include the flash converter, the pipelined converter, and the SAR converter. Their operational principles will be described below.

5.2.1 Flash ADC

The flash converter is designed not only for high throughput but also for low latency [11, Ch. 8]. With one comparator per reference level, all levels are evaluated simultaneously providing a thermometer-encoded result [13, Ch. 4], as illustrated in figure 5.1. For a binary result, a decoder is required as illustrated in the figure. However, the $2^N - 1$ comparators required for an N-bit resolution, bring a high power consumption. In addition, with a large number of comparators, matching becomes problematic and individual comparator calibration is unrealistic. The S&H must also drive all the comparator inputs, a load that increases by a factor of two for each additional bit of resolution. Hence,

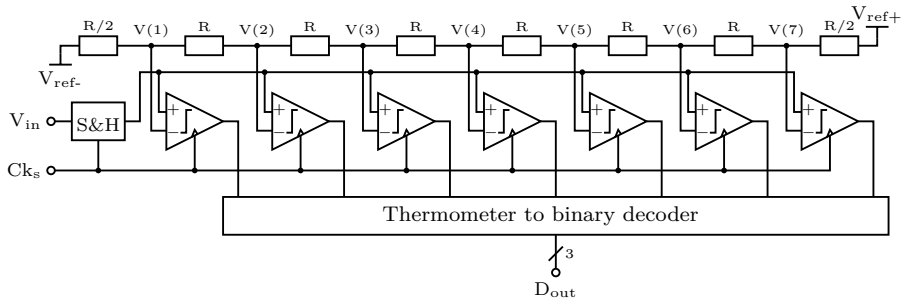


Figure 5.1: A generic 3 bit flash ADC.

the flash converter topology is most suitable for high-speed and low-resolution converters, where only a small number of comparators are needed.

5.2.2 Pipeline ADC

A pipelined converter uses several cascaded low-resolution converters that distribute the conversion over multiple cycles, re-sampling the signal between each stage [13, Ch. 4]. These cascaded stages are illustrated in figure 5.2a, together with a timing diagram showing when the conversion result is ready for each stage, in figure 5.2b. A conceptual pipeline stage is illustrated in figure 5.2c. Here, a complete low-resolution ADC is used to quantize the sampled signal, the DAC outputs an analog signal representing the converted result which is then subtracted from the sampled signal, giving a residual signal which is amplified before the next stage. In implementations of pipeline converters, the DAC might be co-integrated with the reference level generation, directly giving the residual signal. The use of multiple smaller converters allows for the realization of high-speed and high-resolution ADCs.

The amplifiers re-scale the residual signal to use the full range in each stage. However, due to component variations, the gain accuracy typically limits the performance in pipeline converters [11, Ch. 8]. A gain of 2 may be achieved with high accuracy, but higher gains are increasingly harder to achieve with high accuracy due to component variations.

5.2.3 SAR ADC

In contrast to flash and pipeline converters which build on parallelism in hardware, SAR converters use compact hardware and multiple iterations over time [11, Ch. 8]. An illustration of a generic N-bit SAR converter is given in figure 5.3a. A timing diagram, figure 5.3b, illustrates the different clocks and when the different bits are generated. With a small set of analog components and no amplifiers, SAR converters show great potential for achieving a low power consumption [11, Ch. 8]. Their performance is limited by the accuracy in

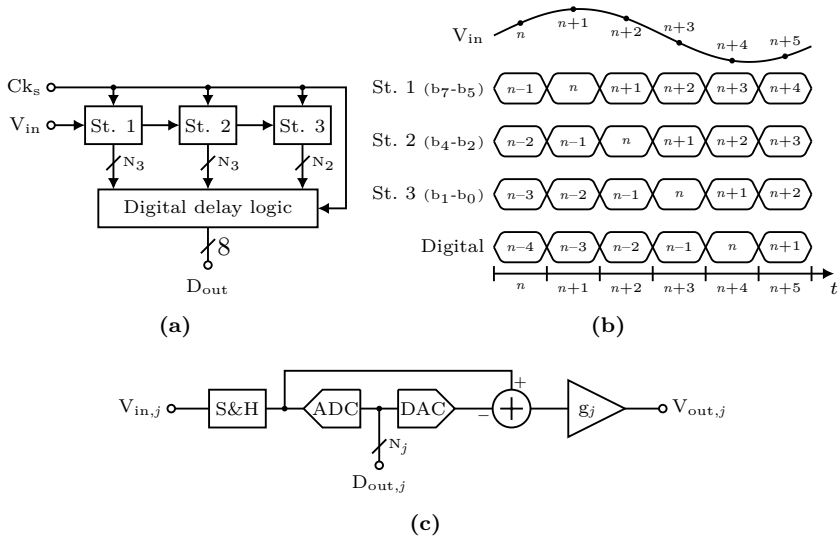


Figure 5.2: (a) An 8 bit, 3-stage pipeline converter. (b) Timing diagram illustrating when data is ready, both for each specific stage and for the entire converter. (c) A generic pipeline stage.

the reference voltage generation, and by comparator offset voltage [11, Ch. 8].

The conversion cycle starts with sampling the voltage and then comparing it with the reference voltage. The comparison result is then used to update the reference voltage before a new comparison is performed. The process is completed when the total number of comparisons performed matches the intended converter resolution.

5.3 Charge redistribution

The DAC required for generating decision levels in a SAR ADC can in principle be based on any topology [11, Ch. 8]. Traditionally, resistive structures have been the preferred choice, but in modern low-power converters, capacitor-based, so-called charge-redistribution networks have become popular, taking advantage of the good switching properties provided by modern CMOS processes [11, Ch. 8].

In a charge-redistribution network, a binary scaled capacitor array is used, both as the sampling capacitor and as the DAC. A simple 3-bit charge-redistribution network is illustrated together with a simple SAR ADC in figure 5.4. Before sampling a voltage onto the array, all capacitor back-plates are connected to the reference voltage. The voltage is then sampled onto the top-plates of the capacitor array before the most significant bit (MSB) switch is toggled to ground, reducing the voltage on the top-plate according to equation (5.5). The comparator then compares the input signal V_{in} with a scaled version of V_{ref}

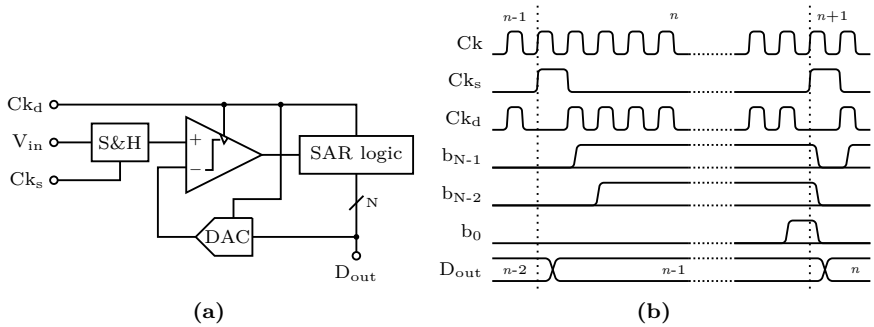


Figure 5.3: (a) Topology for a N-bit SAR converter. (b) Timing diagram indicating when the different bits are generated.

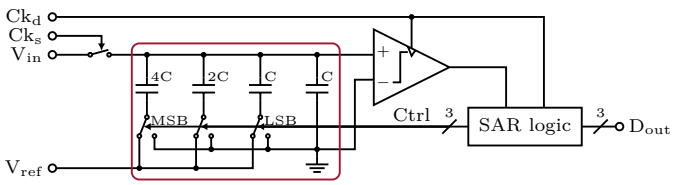


Figure 5.4: A 3 bit charge-redistribution network integrated with a SAR converter. The charge-redistribution network is encircled.

which gives the MSB, and keeps the switch grounded if the comparator did not toggle. The process is then repeated until all bits are resolved. In a differential charge-redistribution network, there is no need to toggle any switch before the first comparison as this level is inherent from the differential topology [11, Ch. 8].

$$V_{top} = V_{in} - \frac{4C}{4C + 2C + C + C} V_{ref} = V_{in} - \frac{C_{stage}}{C_{array}} V_{ref} \quad [\text{V}] \tag{5.5}$$

When implementing a charge-redistribution network, not all capacitance connected to the top plate will be switchable. The routing required to connect all the individual capacitors in the array contribute to the parasitic capacitance, reducing the achievable DR. As the parasitic load is constant, it can be compensated for with an increased reference voltage as indicated by equation (5.6), restoring the desired DR [42].

$$V_{ref} = V_{FS} \frac{C_{sw} + C_p}{C_{sw}} \quad [\text{V}] \tag{5.6}$$

5.4 Redundant scaling

The smallest number of required comparisons for a given resolution is achieved with a binary scaled charge-redistribution network. However, there will be no redundancy against erroneous decisions [43]. In principle, assuming correct decisions is not a problem; however, in a high-speed converter, it becomes costly to guarantee fully settled decision levels. The settling time for the DAC is related to the RC time-constant τ for the switch and capacitor combination in the array and to the required settling accuracy. Reducing C is typically not possible due to thermal noise. Reducing R using a large switch is also not desirable as it will load the charge-redistribution network with additional parasitic capacitance, and be costly to drive.

With a binary scaling, the absolute tolerable settling error is given by the resolution and it is thereby fixed in an implementation. The relative settling error and thus the required settling time is on the other hand dependent on the stage as they have different contributions to the result. As the first decision has the largest impact on the voltage when the DAC switches, it will also require the longest settling time. The required time is then reduced for each of the following stages.

With redundant scaling, it is possible to reduce the required settling time, thereby increasing the converter speed [11, Ch. 8]. However, with a redundant scaling, additional comparisons are needed, resulting in additional iterations of the SAR operation. With a redundant scaling, the absolute tolerable error is increased for stages covered by the redundancy, making it possible to use a shorter settling time [44]. In actual implementations, a constant settling time is typically used for all stages, making it highly beneficial to reduce the settling time. However, to reduce conversion speed, the time spent on additional comparisons must be re-gained through the reduced settling time, which limits the redundancy options.

To simplify the presentation of the different scaling principles, the following definitions will be used: A *stage* corresponds to one iteration in the SAR algorithm. A *level* is one of the outputs from the reference generator against which the signal is compared. A *decision* is a comparison result. A *path* is a sequence of decisions and the corresponding levels that have been visited during the previous stages. With redundant scaling, several paths might result in the same level. A *step* is the separation between decision levels at two successive stages. In addition to this, we also assume that control bits have a binary representation, either 0 or 1.

5.4.1 Binary scaling

With a binary scaling and error-free operation, the overall ADC conversion error will never be larger than 0.5 LSB [42]. However, an erroneous decision along the way will result in a larger error. An example with a 5 bit decision tree is shown in figure 5.5a, showing the effects of both correct and incorrect

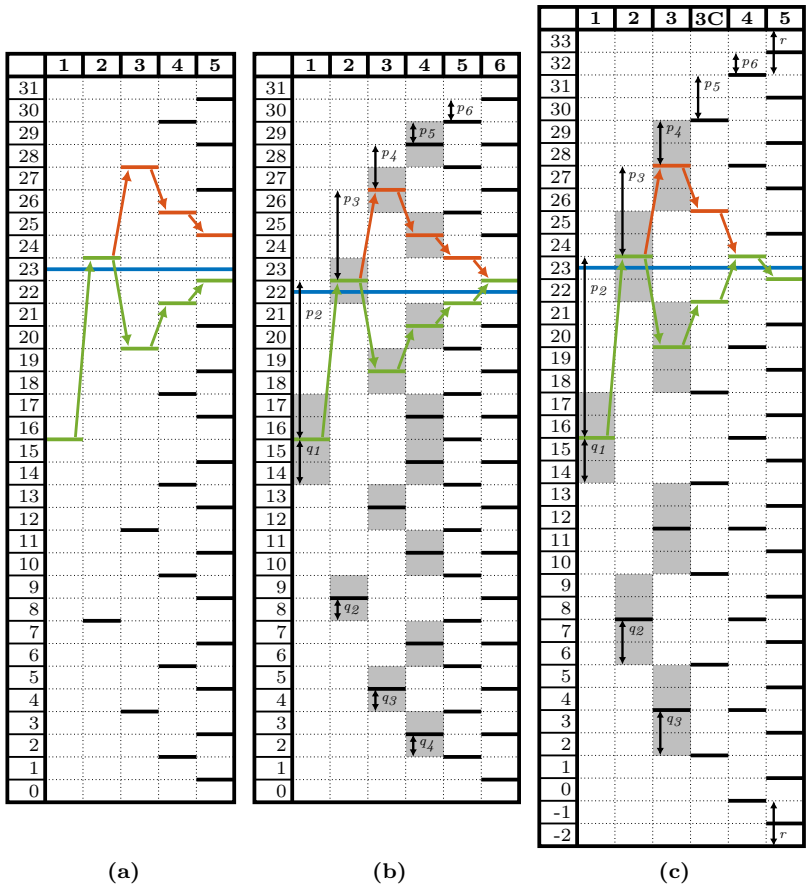


Figure 5.5: Examples of (a) binary scaled reference levels, (b) reference levels scaled according to the generalized non-binary algorithm, and (c) the compensating scaling. For the generalized non-binary scaling, the following properties are used: $p = [16, 7, 4, 2, 1, 1]$ and $q = [2, 1, 1, 1, 0, 0]$. For all three cases, the effects of both, fully correct decisions, and an erroneous decision in the second stage are demonstrated. In both (b) and (c), the effect of an erroneous decision is masked by the redundancy giving a correct output result. Decision levels are indicated by black lines and gray filled boxes shows the redundancy. The input is shown in blue, the path for correct decisions is shown in green, and the path with an erroneous decision is shown in orange.

decisions. The levels are calculated using equation (5.7). The resulting output code, given as an integer in the range 0 to $2^N - 1$, is given by equation (5.8) using the decisions $d(i)$.

$$V_{ref}(k) = 2^N \left(2^{-1} + \sum_{i=1}^{k} -1^{d(i-1)+1} 2^{-1} \right) \quad [\mathrm{V}], \quad (k = 1, 2, \ldots, N) \tag{5.7}$$

$$D_{out} = d(1)\, 2^{N-1} + d(2)\, 2^{N-2} + \cdots + d(N) = \sum_{i=1}^{N} d(i)\, 2^{N-i} \tag{5.8}$$

5.4.2 Generalized non-binary scaling

The redundant non-binary scaling is the simplest realization of a redundant scaling with a fixed radix $\gamma = 2^{N/M}$, with $N \leq M$, where N is the resolution and M is the number of stages [43]. This gives a radix in the range $1 < \gamma \leq 2$, which most likely not will result in integer-sized steps. With a lower radix, increased redundancy is achieved at the cost of additional stages.

The generalized non-binary scaling extends the radix definition, allowing an individual radix in each stage [43]. This gives additional freedom in the redundancy placement and provides the option for using integer-sized steps.

The requirements for the generalized non-binary scaling are governed by two propositions. First, equation (5.9) states the range covered by the redundancy of stage k [43]. Second, equation (5.10) defines the number of redundant paths, given a redundancy $q(i)$ at stage i and an over-range r. The cost of adding redundancy at a stage is dependent on the number of decision levels provided by that stage. As the number of decision levels increases for each stage, the cost of adding redundancy at later stages in the conversion cycle will also increase.

$$|V_{in} - V_{ref}(k)| < q(k) \tag{5.9}$$

$$2^M - 2^N = \sum_{i=1}^{M-1} 2^i q(i) + 2r \tag{5.10}$$

When calculating the steps for an output range $\left[-r, 2^N - 1 + r\right]$, the level in the first stage is assumed to be located in the middle of the range [43], defined by equation (5.11). The relationship between the step sizes and the total number of decision levels is given by equation (5.12). The step $p(k+1)$ is then given by equation (5.13), for a chosen redundancy q starting at stage k.

$$p(1) = 2^{N-1} \tag{5.11}$$

$$\sum_{i=1}^{M} p(i) = 2^N - 1 + 2r \tag{5.12}$$

$$p\left(k+1\right) = 2^{M-k-1} - q\left(k\right) - \sum_{i=k+1}^{M-1} s^{i-k-1} q\left(i\right) \tag{5.13}$$

For stage k, the decision levels are given by equation (5.14) [43]. The redundant output vector is converted into an integer representation in the range $\left[-r, 2^N - 1 + r\right]$ using equation (5.15). Note that in contrast to a binary scaling which can be referred to, both from 0 and from the mid-range, a redundant scaling is only symmetric around its mid-point.

$$V_{ref}\left(k\right) = p\left(1\right) + \sum_{i=2}^{k} -1^{d(i-1)+1} p\left(i\right) \quad \left[\mathrm{V}\right], \quad \left(k = 1, 2, \ldots, M\right) \tag{5.14}$$

$$D_{out} = p\left(1\right) + \sum_{i=2}^{M} -1^{d(i-1)+1} p\left(i\right) + 0.5 \cdot -1^{d(M)+1} - 0.5 \tag{5.15}$$

In figure 5.5b, an example for a generalized non-binary scaling using $M = 6$, $p = [16, 7, 4, 2, 1, 1]$, $q = [2, 1, 1, 1, 0, 0]$, and no over-range is presented. The figure shows the paths both for fully correct decisions and for the case when one erroneous decision is made. In the example, we can see how the erroneous decision is corrected by the redundancy, providing the same result although different paths have been taken to reach it.

5.4.3 Compensating scaling

The compensating scaling uses binary scaled stages and is a special case of the generic non-binary scaling [42]. Redundancy is provided through the introduction of compensation stages having the same size as the previous stage. The compensation stage will introduce a level shift equal to half the size of the compensation step, thereby introducing an over-range. A larger redundancy will result in a larger over-range and thus a reduced DR [42].

An example of a 5 bit compensating scaling is presented in figure 5.5c, where the compensating stage is located after the third stage. Here, we can observe the alternative path taken in the case of an erroneous decision in the second stage.

5.5 Figures of merit

Comparing different circuit implementations with each other in a fair way is always complex, independent of the type of circuit being evaluated. For ADCs, this process is simplified thanks to the somewhat standardized interfaces, with a sampling capacitor at the input, and a digital interface at the output. In addition to design-specific parameters such as resolution, sample rate, and

architecture, and generic properties such as power consumption, there are a few specific metrics commonly used to evaluate different ADC implementations.

An ideal ADC should only show quantization errors. However, in practice, additional errors related to the circuit topology, process variations, converter resolution, and sample rate, all further reduce the achievable performance for a converter [11, Ch. 4]. Although some of the above error sources have a purely static origin, they impact both the static and dynamic converter performance.

5.5.1 Static metrics

An ADC is typically assumed to have equally sized quantization steps, resulting in a linear relationship between the analog input signal and the resulting digital representation. However, due to variations, the quantization steps will be unequally sized, resulting in a non-linear mapping.

A converter's linearity is often assumed to be static and independent of the input signal [13, Ch. 2; 41, Ch. 1], although, in some implementations, it might be signal-dependent. The non-linearity resulting from non-uniform quantization is categorized using two metrics, the differential non-linearity (DNL) and the integral non-linearity (INL). Both these metrics are typically reported in LSBs although volts and fractions of the DR might be used [13, Ch. 2].

DNL is the deviation from the ideal quantization step Δ and for uniform quantization it will be 0 LSB. In order to avoid missing codes, that is digital output codes that cannot be produced by any analog signal, a DNL grater than -1 LSB is required [11, Ch. 4]. For a step size $\Delta_r(k) = X_{k+1} - X_k$, equation (5.16) gives the resulting DNL [13, Ch. 2].

$$\mathrm{DNL}(k) = \frac{\Delta_r(k) - \Delta}{\Delta} \tag{5.16}$$

The total deviation from the ideal transfer function, that is the INL, is given by equation (5.17), using the already calculated DNL. This gives the true interpolated INL. In some cases, this is considered to be a bit pessimistic as it also includes potential offset and linear gain errors. The end-point fit is often used as it eliminates such errors, giving an INL of 0 LSB at the end-points [11, Ch. 4; 13, Ch. 2]. Equation (5.18) shows the INL when a gain error is present. Assuming an INL without gain and offset errors is not problematic as these are linear effects that easily can be compensated for in the DSP typically following the converter.

$$\mathrm{INL}(k) = \sum_{i=1}^{k} \mathrm{DNL}(k) \tag{5.17}$$

$$\mathrm{INL}(k) = (1+G) \sum_{i=1}^{k} \mathrm{DNL}(k) \tag{5.18}$$

Typically, the worst-case value is reported for each respective metric, although a plot with respect to the output code often gives a better illustration of the non-linear behaviour. Although both DNL and INL are considered to be static, they will impact the dynamic performance. A high uncorrelated DNL will appear like additional quantization noise, while a large INL will distort the signal, causing harmonic distortion (HD) [13, Ch. 2].

5.5.2 Dynamic metrics

The dynamic converter performance is characterized by its noise behaviour using two metrics, the SNDR and the spurious free dynamic range (SFDR) [41, Ch. 1]. Effective number of bits (ENOB) is in some cases used as substitute for the SNDR [13, Ch. 2].

Both these metrics are calculated from the spectrum of the converted signal. They are typically measured using a single sine-wave signal for a clear distinctness between signal and noise. The SNDR is the ratio between the signal power and the total noise power including distortion, as defined in equation (5.19). The SFDR, on the other hand, is the ratio between the signal and the largest spurious tone. In contrast to HD, which only considers harmonics, SFDR considers all spurious tones, giving a more accurate indication of the usable DR.

$$\text{SNDR} = 10\log_{10}\left(\frac{P_{signal}}{P_{noise+distortion}}\right) \quad [\text{dB}] \tag{5.19}$$

The highest achievable SNDR is set by the quantization noise and thus by the converter's resolution. In reality, additional noise is introduced, reducing the achievable SNDR. Converting the SNDR into ENOB, using equation (5.20), allows for a quick comparison with the designed resolution.

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02} \quad [b] \tag{5.20}$$

5.5.3 Comparison metrics

All the above metrics are suitable for evaluating and comparing the performance of ADCs with similar specifications. The power consumption, on the other hand, is more complex to compare. The energy per conversion is a metric that normalizes the power consumption to the sample rate, giving the energy cost for a single conversion. However, as the power consumption is dependent on the converter resolution and sample rate, this metric will not give a fair comparison of the energy consumption at different converter resolutions and/or sample rates. Hence, metrics that account for the increased complexity and power consumption resulting from an increased converter resolution are needed.

A number of weighted figures of merit (FoMs) have been presented in literature [11, Ch. 4; 13, Ch. 2]. Two such metrics, the Walden figure of merit (FoMW) and the Schreier figure of merit (FoMS), are broadly accepted to account

for the cost of the increased complexity brought by an increased resolution. They are both based on empirical analysis of the measured performance for a large number of ADC implementations.

The FoMW normalizes the energy consumption to the converter effective resolution, as seen in equation (5.21) [11, Ch. 4; 13, Ch. 2; 45]. Originally, the inverted definition was used, but it proved to be unintuitive [46, 47]. This FoM is most suitable for low and moderate resolution converters, as the increased complexity in noise-limited designs is not accounted for [18, 48].

$$\text{FoMW} = \frac{P_{DC}}{2^{\text{ENOB}} f_s} \quad [\text{fJ/conv} - \text{step}] \tag{5.21}$$

The FoMS is the other popular comparison metric [11, Ch. 4; 13, Ch. 2], equation (5.22), which is commonly used for high-resolution ADCs. The reduction in energy per conversion is too optimistic for low-resolution converters [18]. This metric has also been adapted from its original definition to better cover the converter noise performance [49, Ch. 9; 50, Ch. 1].

$$\text{FoMS} = \text{SNDR} + 10 \log_{10} \left(\frac{f_s}{2 P_{\text{DC}}} \right) \quad [\text{dB}] \tag{5.22}$$

Chapter 6

Related work

This chapter presents an overview of the field for each of the three building blocks, RF-IQ modulators, predistorters, and high-speed ADCs, presented in this thesis. Each block is given one section presenting the history, current status, and trends.

6.1 RF-IQ modulators

The first RF-DAC-based modulator was demonstrated by Luschas et al. [51] in 2004. This implementation relied on a sample clock derived from the LO signal, thus the sample rate was fixed with respect to the carrier frequency. In 2005, Eloranta et al. [52] demonstrated the first RF-DAC-based modulator using fully independent LO and sample clock frequencies. Following these early realizations, RF-DAC-based transmitters have been demonstrated using carrier frequencies from a few gigahertz [28, 29, 53–66], to 30 GHz [37, 67–70], 60 GHz [20, 71–80], and >100 GHz [30, 81–85]. These include both Cartesian and polar modulators with vastly different resolutions and sample rate. The large improvements in carrier frequency and sample rate taken since the first realizations are enabled by the increased performance brought by modern CMOS processes. In figure 6.1, RF-DAC-based transmitters are arranged according to their resolution and center frequency. For those realized using a polar topology, the resolution refers to their magnitude resolution. In the figure, there appear to be only two groups, however, considering the logarithmic frequency axis, the rightmost group represents the three groups with the highest frequencies above. One can also observe that for lower carrier frequencies, a resolution >8 b is often used. This is in contrast to the higher carrier frequencies where most realizations use a resolution <7 b, with several using a 2–3 b resolution.

Essentially all RF-DAC-based transmitters are based on current steering, although switched-capacitor-based topologies also have been demonstrated [64, 70]. For current-steering RF-DACs, the unit cells is in most cases realized

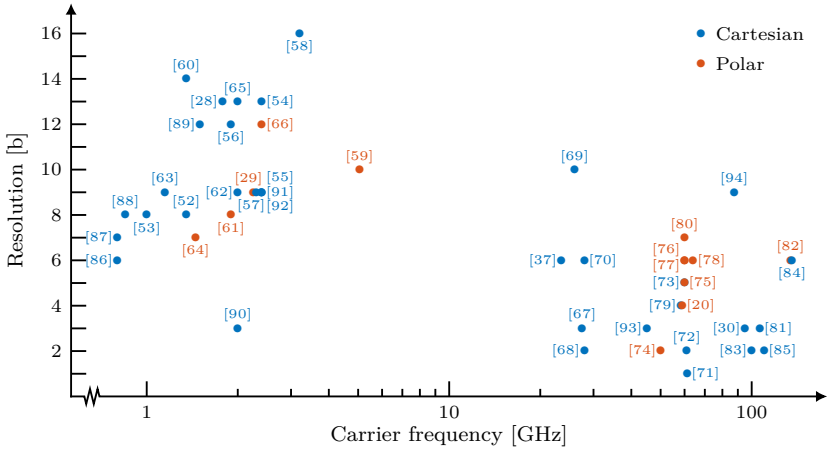


Figure 6.1: A collection of RF-DAC-based transmitters arranged according to their carrier frequency and resolution.

using two stacked transistors, one driven by the LO signal and the other by the digital data signal. In some cases, especially at lower frequencies, the LO and data signals are combined using an AND-gate before driving a single transistor [29,54–56,59–61,63,66]. This improves efficiency, but it is problematic to realize at high carrier frequencies. There are realizations using a large LO-transistor shared among multiple data-switches [30,93,95]. This minimizes the LO routing but increases the load on the node connecting the data-switches to the LO-transistor.

To achieve a high output power, some implementations use cascodes to enable the use of high voltages rather than large currents [37,67,81–84,94]. To keep an even voltage split across the transistors in the cascode, the current must be kept constant, independent of the output level. This results in constant power consumption, independent of the output level.

In Cartesian modulators, the sign may either be applied within the unit cell, increasing the load on the LO driver, or it may be set before the RF-DAC [28,54,56,60,69,90]. In the latter case, sign and magnitude need to be aligned with sub-sample precision, just as the phase and magnitude must be in a polar transmitter [20]. This is however problematic at high sample rates. Another problem with Cartesian transmitters is combining the quadrature components. Directly summing the nodes will result in cross-modulation distortion. At very high carrier frequencies, OTA combining may be used as a substitute for an on-chip combiner [73,83,84]. At low carrier frequencies, non-overlapping LO signals may be used to reduce the impact of the cross-modulation distortion [28,55,60,63,90].

In a polar transmitter, the magnitude and phase modulation are divided into two cascaded blocks. While the RF-DAC used for the magnitude modulation is

similar to the RF-DACs used in the Cartesian topology, the phase modulation is more complex to realize. Polar transmitters are in some cases demonstrated using a phase-modulated LO signal that is externally generated, thus only realizing the amplitude modulation [29, 66, 74, 76]. Others use IQ-mixers driven by external baseband (BB) IQ signals for the phase modulation. When the phase modulation is realized entirely on-chip, Cartesian-based modulators are most commonly adopted [59, 61, 78, 80]. The use of both an oscillator [77], and a digital-to-time converter [64] have been demonstrated.

The performance of a circuit should be evaluated as close to the targeted operating conditions as possible. For a transmitter, the modulated signal must represent a realistic communication signal, using a signal with limited and well-defined bandwidth. Implementations at lower carrier frequencies are typically evaluated in this way, considering both the in-band and the out-of-band performance. Target applications with clear requirements are here most likely a driving factor. For implementations at higher carrier frequencies, on the other hand, only a few use band-limited signals. In addition to reporting the wideband performance, these also report the out-of-band performance, either in the form of ACPR [69, 70] or as a comparison with a spectral mask [20, 78].

With increased carrier frequency and sample rate, it is not only more challenging to perform the measurements; generating the wideband digital BB signals to drive the RF-DACs is also challenging, which may be one reason why some implementations are not evaluated using realistic communication signals. Comparing the performance for implementations using proper pulse-shaped and bandwidth-limited signals with those just stepping from one symbol to the next with a resulting sinc-shaped spectrum is problematic. Although the EVM requirements are fulfilled, the use of non-bandwidth-limited signals results in reported data rates that are not achievable if proper pulse-shaped signals were used. This is since oversampling would be required to shift the images away from the channel such that an analog filter could suppress them.

A high sample rate is central to enabling wideband signals. Most RF-DAC-based transmitters with both high resolution and high carrier frequency have a sample rate of 2–6.5 GS/s [37, 67–70, 73, 80], although 10 GS/s has been demonstrated for the magnitude part of a polar modulator [20]. However, this circuit does not demonstrate a complete on-chip realization of the phase modulation. With interpolation, pulse shaping can be realized in hardware, potentially reducing the required sample rate [78, 80].

6.1.1 Quadrature LO generation

Dividers are very popular to use for the quadrature LO generation at low frequencies [28, 56, 59–61], but they are also used at higher frequencies [37, 78]. In [96], the upper-frequency limit is pushed thanks to the elimination of the cross-coupled regeneration stage. The dynamic latch here relies on the parasitic capacitance for state retention. In [78], a divider is followed by frequency triplers to overcome the upper-frequency limit for the divider.

Although PPFs are not commonly used together with RF-DACs, they receive an increased interest, filling the gap between dividers and hybrids. With a single-stage PPF, the quadrature LO signals may only be generated over a narrow bandwidth. To extend the frequency range, either a multi-stage filter may be used [35, 97, 98], with an increased loss, or a single tunable filter stage can be used [99, 100]. Active PPFs have been demonstrated at lower frequencies, overcoming the inherent loss present in a loaded passive PPF [27, 101, 102].

At higher frequencies, above the range for dividers and PPFs, hybrids are commonly used for the quadrature LO generation [35,97–100]. Although physical dimensions are small at high frequencies, lumped realizations are sometimes used to further reduce the hybrid footprint [20, 84, 94].

The use of non-overlapping LO signals is a popular method to reduce the impact of cross-modulation distortion in Cartesian transmitters at low carrier frequencies. To accurately generate the non-overlapping pulses, divide-by-two circuits are typically combined with AND-gates [28, 60]. Non-overlapping LO signals has also been demonstrated in receiver applications up to 30 GHz [103, 104]. There, the pulses are generated using transmission-gate-based AND-gates located between the buffers and mixers, eliminating the need for buffering of the non-overlapping signals. This is possible thanks to the small load presented by the mixers. In BiCMOS, the generation of non-overlapping LO signals has been demonstrated up to 62 GHz, although with increased duty cycle at higher frequencies [105].

To drive the RF-DACs, buffering of the quadrature LO signals is needed. Transimpedance amplifier (TIA)-buffers are often located between the quadrature LO generation and the RF-DACs [30, 37, 67, 78, 84]. With high carrier frequencies and large capacitive loads presented by the RF-DACs, the buffering of the LO signals has a large impact on the total power consumption for the transmitter [37]. In [69], the final LO buffering stage is distributed throughout the unit cells. To reduce LO leakage, these buffers are deactivated when the cell is not in use, thus also reducing the power consumption for the LO buffering. In [70], edge-combining-based frequency-tripling delay-locked-loops are placed within all unit cells to reduce the frequency of the LO signals distributed throughout the RF-DACs. As the modulation is performed before the last edge-combining stage, the highest sample rate is limited to one-third of the carrier frequency. With another frequency multiplication factor, the highest sample rate may be further reduced.

6.2 Predistorter implementations

For a long time, DPD has been the most common solution to handle the inherent trade-off between PA linearity and power efficiency [106]. A vast number of DPD algorithms have been presented in literature, targeting different transmitter non-linearities [40]. In some cases, a hardware implementation is demonstrated, either using a field-programmable gate array (FPGA) [107–116], or in the form

of a custom application-specific integrated circuit (ASIC) [117, 118], thus not only showing the algorithm performance, but also its hardware cost. These hardware realizations are either based on LUTs or use non-linear models such as polynomial or Volterra basis functions [40]. Although being both flexible and powerful, the predistorter linearization accuracy must be traded off against the implementation complexity and power consumption. For feedback loops running at single gigasample-per-second rates, the predistorter might have a Watt-level power consumption [40].

Conventional DPDs typically requires a sample rate five times lower than the signal bandwidth to ensure proper linearization [106, 112, 116]. For narrow bandwidths, this is not an issue as FPGAs may be clocked at the full sample rate used in the observation receiver [112, 113]. With bandwidths potentially reaching beyond 1 GHz, in wideband systems, neither FPGAs nor ASICs can easily operate at the required clock frequency [106]. Efforts has been put, both into reducing the sample rate used in the observation path [116, 119, 120], and into parallelizing the DPD implementation [115]. Still, these implementations are demonstrated for bandwidths <1 GHz, leaving room for further development.

In APDs, the expanding gain characteristic is realized using a non-linear circuit [121–127]. Different topologies commonly in use include cold-mode FETs [121, 122], reflection-based circuits [124, 125], and Class-C amplifiers [123]. The cold-mode FET predistorter relies on the expanding behaviour of the FET drain-source resistance with increased RF power [121]. The reflection-based predistorter uses a power-dependent matching network and a non-linear load that alters the amount of power reflected back to the PA [124]. In [123], a Class-C amplifier is used to generate third-order intermodulation products before a delay line shifts their phase such that they are cancelling those generated by the PA. Analog predistorters often introduce a significant power loss [122, 123], potentially resulting in the need for additional buffer amplifiers [121]. This is problematic, especially at mm-Wave frequencies where gain is costly.

Clearly, APDs and DPDs each have their advantages and disadvantages. The hybrid predistorter combines DPD with APD, reducing the complexity of the DPD implementation while still taking advantage of the flexibility it brings [128–130]. The hybrid approach becomes highly interesting in a MIMO transmitter, where the APD can be used to align the spread in the PA non-linearity, letting the DPD linearize the average non-linearity [130].

6.3 High-speed ADCs

There is a long tradition of research on ADCs for various applications. With the vast number of designs presented in literature, comparisons can be challenging to perform. In 2007, Boris Murmann started collecting all ADCs presented at the International Solid-State Circuits Conference (ISSCC) and the VLSI Symposium in a single document [18], together with some illustrations showing how the latest designs compare them-self with previously presented ones. In

addition to trends, this collection also enables other types of comparisons and studies.

In figure 6.2, a comparison of different high-speed ADCs with a resolution in the range 7–12 b are shown. These ADCs have a single-channel sample rate exceeding 500 MS/s. The collection is based on the Murmann survey and extended with designs presented at the Asian Solid-State Circuits Conference (A-SSCC), the Custom Integrated Circuits Conference (CICC), and the European Solid-State Circuits Conference (ESSCIRC).

In figure 6.2a, the ENOB is plotted versus the single-channel sample rate. From this figure, it is possible to observe that only a few realizations show a channel sample rate above 1.5 GS/s. It is also possible to note that SAR converters are the most common choice for lower resolution realizations. For higher resolutions, pipeline converters and pipelined SAR converters are more popular.

From figure 6.2a, it is possible to compare the achieved ENOB with the converter designed resolution. For the converters presented in the figure, those with a lower resolution, in general, show an ENOB around 1–1.5 b lower than their resolution. For the converters with a higher resolution, the difference is slightly larger, around 1.5–2.5 b. Time-interleaved (TI) converters generally show a 1 b ENOB reduction compared to their single-channel counterparts. One should here keep in mind that these TI converters have a very large bandwidth and often experience a significant signal attenuation, especially at higher frequencies [194], partly explaining the difference.

With all these converters targeting a high single-channel sample rate, it is likely that many designs trade off accuracy for speed. There are however a few designs that demonstrate a high relative ENOB. These include a few different pipeline topologies [132, 157, 158, 161, 187, 188, 193]. Some use SAR stages [157, 158] while others are assisted by flash stages [161, 193]. These, there are also some pure SAR converters [142, 145, 164], out of which two use a multi-bit per stage topology [142, 164]. Although being based on highly different topologies, all achieve their high relative ENOB through a relaxed comparator timing requirement. Other topologies relax the timing requirement on the comparators without achieving a high relative ENOB. The alternating comparator SAR converter is one topology that successfully demonstrates a very high single-channel sample rate [143, 144, 170, 181]. Of these, only [143] show a good relative ENOB. Then there is the unfolded SAR topology where a dedicated comparator is used for each comparison. This topology further relaxes the timing requirement on the comparator, at the cost of more hardware. Multiple implementations demonstrate good relative ENOB and a high sample rate [151, 155, 156, 158, 177, 180].

In figure 6.2b, the FoMW is plotted versus the energy per conversion, for the same implementations as in figure 6.2a. In the figure, one can note that for each additional bit of resolution, the energy required per conversion increases with roughly 2 to 3 times. Looking at the FoMW, one can also notice that the implementations with a low FoMW, all have a high relative ENOB. This

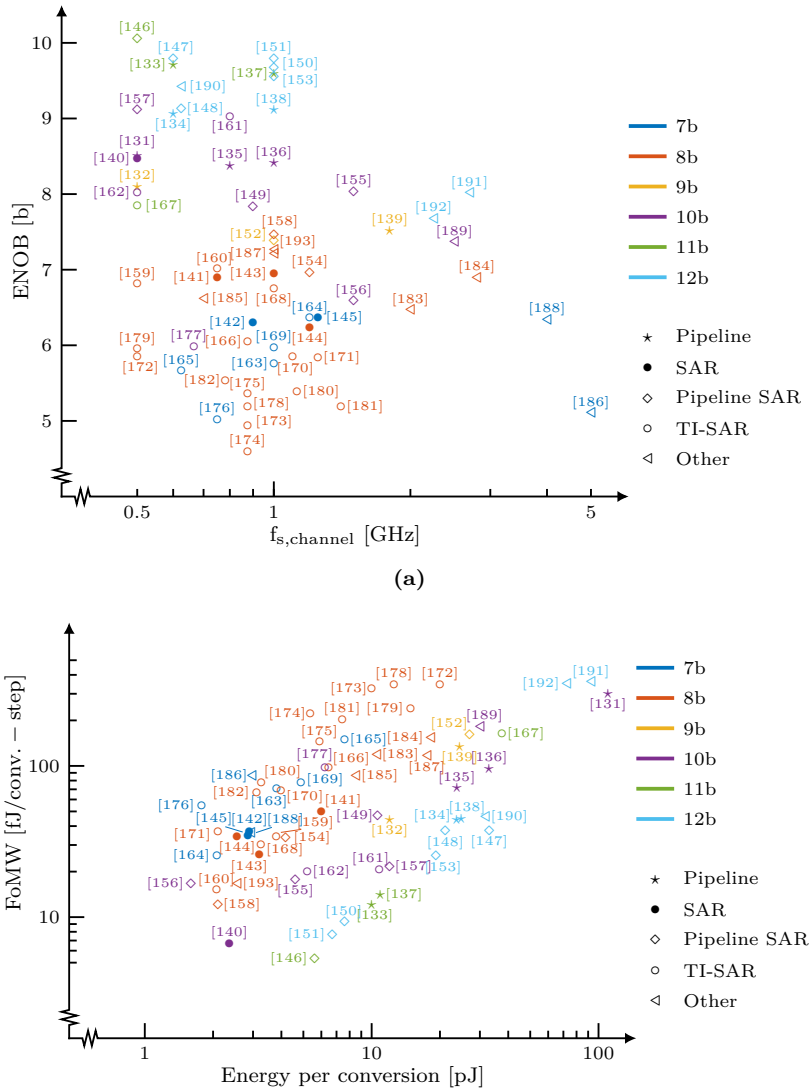


Figure 6.2: Different ADC implementations with a channel sample rate exceeding 500 MS/s and a resolution in the range 7–12 b. These designs are presented in one of the top-ranked solid-state circuits conferences (A-SSCC, CICC, ESSCIRC, ISSCC, and VLSI symposium). (a) The ENOB versus the channel sample rate, and (b) the FoMW versus the energy per conversion. In these plots, the color represents the converter's designed resolution and the symbol represent its architecture.

also becomes clear from equation (5.21). Hence, for overall effective utilization of the hardware and power budget, it is clear that a balance between a high sample rate and a high relative ENOB is needed.

To further push the boundaries, it is important to understand what limits the performance in current implementations. Central in the realization of many SAR ADCs are capacitor-based DACs. To minimize their power consumption, unit cells with a capacitance $<1\,\mathrm{fF}$ are being used [195, 196]. The matching of these small capacitors is evaluated in [197] using measurements. The impact of capacitor mismatch on the achievable ENOB has also been studied, connecting ENOB and capacitance mismatch with yield [198]. Another critical component in SAR ADCs is the comparator, where the offset voltage and noise are considered most critical. From the perspective of the traditional SAR ADC with a single comparator, offset voltage is not critical as the effect is static [199]. In multi-comparator topologies, such as loop-unrolled SAR ADCs [200–203], and alternating comparator SAR ADCs [44, 143, 194, 204], multiple comparators are used to boost the conversion speed. Using different comparators for different parts of the conversion may however result in reduced ENOB [203]. The effect of comparator offset voltage is analyzed for a loop-unrolled SAR topology in [203] and the trade-off between comparator noise and power is studied in [204]. Although multiple comparators are used in the loop-unrolled SAR topology, they are only reset at the end of the conversion cycle. This is in contrast to the alternating comparator topology where the reset is performed while a comparison is performed by the other comparator, making the reset accuracy a factor.

Chapter 7

Wideband modulation using RF-IQ modulators

In papers A and B, two different RF-IQ modulators are presented. This chapter will present concepts and discuss design choices and limitations with the designs, in order to bring a deeper understanding of the circuit implementations. Topics touched include the quadrature LO generation, effects of skew in the control signals, clock jitter, and switching induced supply noise. Some extended results using OFDM signals will also be presented.

7.1 Quadrature LO generation

Generating and buffering quadrature LO signals for a large load at mm-Wave frequencies is challenging. The large load presented by the RF-DACs often results in large power consumption and footprint for the quadrature LO generation and buffering. Moreover, the accuracy of the quadrature LO signals limits the achievable modulator performance. Studying implementations in literature, one can observe that the overall modulator topology greatly impacts the quadrature LO generation topology.

From the RF-DAC perspective, the use of non-overlapping LO signals is highly beneficial. The cross-modulation distortion is significantly reduced even if the RF-DAC outputs are directly summed. With sine wave LO signals, a complex combiner would be required for this summation in order to avoid cross-modulation distortion. However, non-overlapping LO signals bring different signal properties compared to pure sine wave signals, further complicating the LO buffering. In papers A and B, two different approaches have been used for the generation and buffering of non-overlapping LO signals.

In paper A, a divider-based approach was used to generate the quadrature LO signals, from an input signal at twice the desired frequency. These signals were then buffered through 17 inverter stages. The width of each inverter stage is

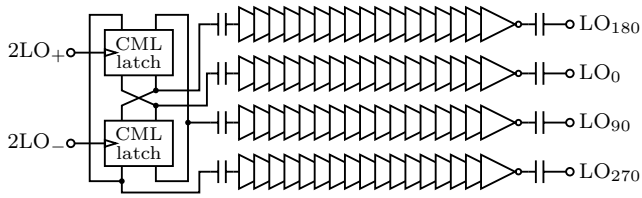


Figure 7.1: Schematic of the divider-based quadrature LO generation used in paper A.

increased by roughly 1.5 times. To sharpen the edge rates, the last two inverters have the same width. The same also goes for the first two inverters in the buffer. Through the DC-bias at the buffer inputs, the LO-signal duty cycle may be controlled. A schematic of the entire quadrature LO generation is shown in figure 7.1. In absence of inductors within the buffers, a size similar to the size of the two RF-DACs is achieved. The inverter approach is flexible in the sense that it can support a range of duty cycles. However, with a large load and mm-Wave frequencies, the gate and parasitic capacitances are problematic. Four parallel buffers are required, resulting in a large power consumption. The high frequency and the large capacitive loads make the implementation challenging, forcing a small transistor width increase for each buffer stage. This indicates that we are close to the upper-frequency limit for this approach given the selected technology, a 22 nm FDSOI CMOS process. In addition to device mismatch, the accuracy of the differential LO signal driving the latches and the circuit symmetry at the latch outputs all affect the achievable IRR. An imperfect differential input, with a non-180° phase difference, will directly translate into a phase imbalance between the 0° and 90° phases. Asymmetries in the latch output loads will individually skew both the amplitude and phase of each phase, further degrading the accuracy of the quadrature LO signals.

In paper B, a three-stage active PPF is combined with current-mode logic (CML) NOR-gates and four-stage asymmetrical TIA-buffers, shown in figure 7.2a. With an active PPF, it is possible to overcome the significant loss resulting in a loaded a passive PPF. The gain will however depend on the bias settings controlling the frequency response. In addition to generating the non-overlapping LO signals, the CML NOR-gates, shown in figure 7.2b, also bring the possibility to control the LO magnitude. The top-placed p-type metal-oxide-semiconductor (PMOS) transistor both provides bias control for the gate and control of the output magnitude.

To maximize the voltage swing for symmetrical signals, such as a pure sine wave, it is desirable to have the TIA's switching point located at half the supply voltage. That is the point where the highest large-signal voltage gain is achieved. As stated in section 3.2.3, the DC-level for non-overlapping signals depends on their duty cycle, increasing with increased duty cycle. As a result of the TIA inverting characteristic, the duty cycle, and thus the DC-level will shift from one buffer stage to the next. To achieve a large LO magnitude, this varying

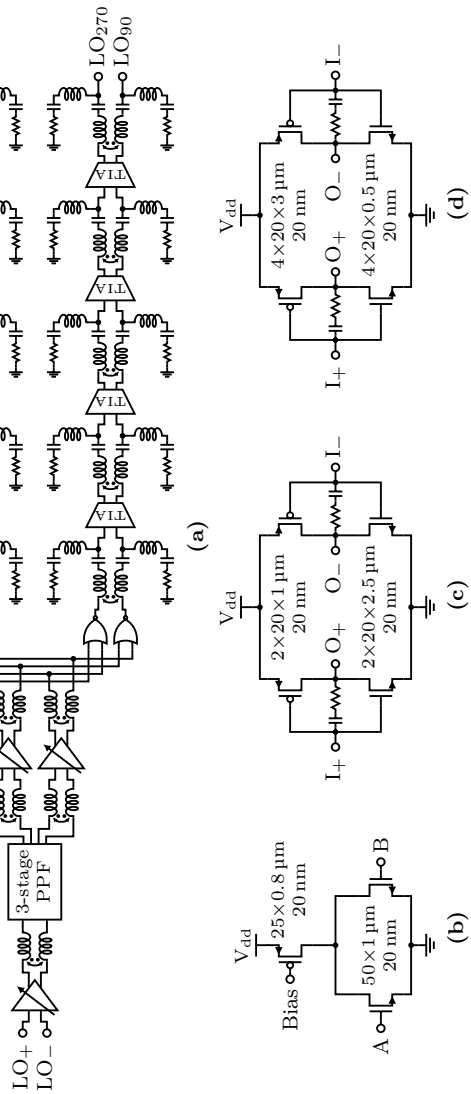


Figure 7.2: (a) Schematic of the quadrature LO generation used in paper B. (b) Schematic of the current-mode logic (CML) NOR-gate used to create the non-overlapping pulses. Schematic of the TIAs used in (c) the third and (d) the fourth buffer stage, including the transistor dimensions used. The TIAs used in the first and second stage have the same topology but the transistor widths are one quarter of the widths used the third and fourth stage respectively.

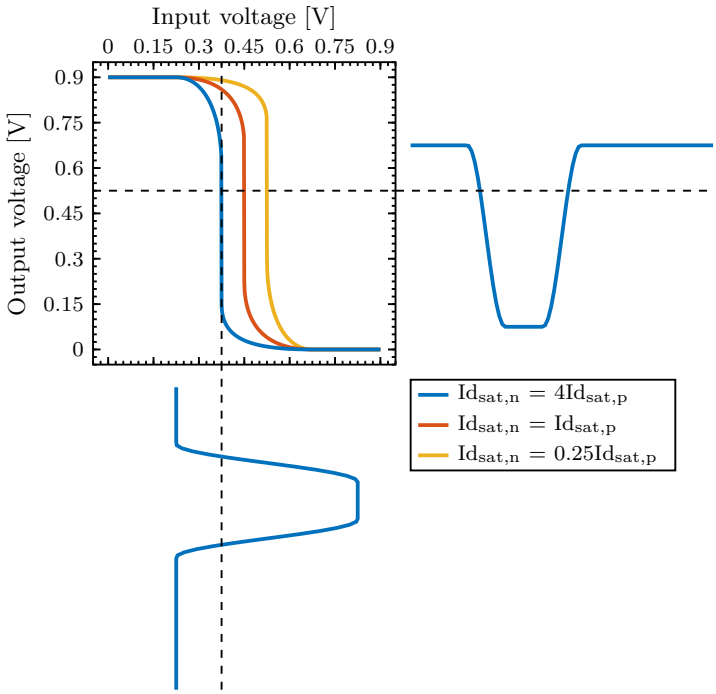


Figure 7.3: Transfer characteristics for different TIA saturation current ratios. In addition, the operating point for a non-overlapping waveform is shown, illustrating the need for the shifted switching point.

duty cycle must be accounted for. To prevent the TIAs from compressing the output signal, the DC-level of the input signal should be located at the switching voltage. Due to the inverting TIA characteristic, the DC-level at the output will be shifted in the other direction, increasing the usable range. In figure 7.3, the transfer characteristics for three different saturation current ratios are shown, demonstrating how the switching point and large-signal gain in the TIA may be shifted. This figure also shows the operating point for a non-overlapping signal at both the TIA input and output. By aligning the signal DC-level with the switching voltage, we can maximize the use of the TIA large-signal gain.

The ratio in saturated drain current required for the n-type metal-oxide-semiconductor (NMOS) and PMOS transistor to achieve the shifted switching voltage is realized through the transistor width ratio of the two transistors. The widths, shown in figures 7.2c and 7.2d, that are used for the implementation of the TIAs in paper B, realize a current ratio of roughly 4 and 1/4 for the two TIAs shown. Since the normalized saturation current is different for the NMOS and PMOS, the required ratio for the transistor widths need to be different, as can be seen in figures 7.2c and 7.2d.

With non-overlapping signals, multiple harmonics are required to maintain

the signal shape. At mm-Wave frequencies, already the third harmonic is very challenging. In addition, with several tones forming the signal, all tones must be amplified by the same amount, making the buffer bandwidth important and challenging. The TIA-buffers used here have been designed to achieve a flat gain between 20–90 GHz, allowing the non-overlapping signal to include the third harmonic up to a fundamental frequency of 30 GHz. To achieve this wide bandwidth, inductive peaking is used to increase the gain at the higher frequencies. The shunt placed series inductor-capacitor-resistor-based resonators, see figure 7.2a, are used to flatten the gain response by loading the circuit at desired frequencies.

The divider and inverter based quadrature LO generation used in paper A consumes 355 mW at 23 GHz. With the PPF and TIA based approach used in paper B, the power consumption is reduced to 260 mW at 23 GHz. However, the inductors used for the inductive peaking significantly increase the footprint, making it around 20 times larger than the LO generation used in paper A and around 13 times larger than the RF-DACs used in paper B. Still, the quadrature LO generation has a significant contribution to the overall power consumption. Hence, it would be desirable to share some parts of the quadrature LO generation among multiple transmitters. For the quadrature LO generation used in paper B, the PPF and the two variable gain amplifiers (VGAs) occupy roughly 30 % of the area used by the LO generation and are responsible for roughly 30 % of its power consumption. Thereby, it is highly beneficial to share these blocks among multiple transmitters, reducing per-transmitter cost. In principle, the same may also be done for the divider used in paper A. However, the divider only occupy around 1 % of the LO generator area and consumes around 1 % of its power, thereby not showing the same potential gain.

7.2 Control signal skew and jitter

Ideally, all control signals driving the data switches in the unit cells should switch simultaneously, independently of the signal value. However, in practice, this is not the case due to different types of variations causing different delays for different signals. Examples of variations causing these types of effects include: device mismatch, asymmetries in clock distribution, data-dependent delay variations, and load imbalances. Device mismatch is always present but its effects may be reduced by careful layout. The same goes for the clock network where an H-tree topology and buffers can be used to minimize skew and isolate the effects of asymmetries. The effect of data-dependent delay is mainly related to the characteristics of the selected FFs. Due to the large RF-DAC footprint, all control signals will present different loads on the drivers, resulting in different delays for different control signals. For thermometer-coded RF-DACs, the variation is mainly caused by parasitic load on the routing. For binary scaled RF-DACs, independently of their organization, the variation is mainly caused by the bit-position-dependent width of the driven data switches.

In addition to these, there is also clock jitter.

To analyze how the main sources of skew and jitter present in my RF-IQ modulator implementations degrade the performance for modulated signals, a behavioural RF-DAC model is used. With this model, random skew in the clock distribution and FFs clock-to-Q propagation delay, the static data-dependent propagation delays in the FFs, and cycle-to-cycle jitter, are modelled. The effect that these skew sources have on modulated signals is presented in figure 7.4, where the X-axis is relative to the sample duration, for each source separately. This figure also shows the impact of cycle-to-cycle clock jitter. The simulations use a 256-QAM SC signal, pulse-shaped using an RRC filter with factor 0.1 and up-sampled 4 and 6 times.

First, taking the random skew variation in the clock tree, and in the clock-to-Q delay, we can observe that the clock tree has a greater impact on the performance for the same skew variance. This is explained by the difference between the number of FFs and the number of leaves in the clock tree. As each unit cell contains two FFs, the clock skew will affect both signs, while the internal skew in the FF will affect the different signs individually, thus reducing the likelihood of a large skew affecting the signal.

Second, the effects of a static difference in the FF's clock-to-Q rising and falling delay are shown in figure 7.4; one can observe that this effect has a significantly larger impact on the performance, although not as large as the clock jitter. This is expected, as all FFs are affected in the same way, in contrast to the case with skew; thus even a small difference between the rising and falling delay will have a large impact on the performance.

Finally, the effects of cycle-to-cycle clock jitter. As shown in figure 7.4, jitter will have a great impact on the achievable performance. From figure 7.4b, it can be noted that the ACPR and EVM curves are located on top of each other, showing that both in-band and out-of-band performance is equally affected by jitter. This is expected as both the sample duration and the symbol duration (N samples) are varying as a result of the clock jitter.

To minimize the effect of skew in the switching of the control signals, the unit cells used in both papers A and B include FFs directly driving the data switches. This also relaxes the routing, making the clock the only signal which requires careful distribution throughout the entire DAC core. Montecarlo simulations (mismatch only) have been performed on both the FF and complete clock distribution used in paper B, with full parasitic extraction (resistance, capacitance, and inductance). For the FF, using 100 000 Montecarlo simulations, the skew variance from clock to output is 0.6 ps for rising output and 0.7 ps for falling output. In addition, a static data-dependent delay difference of 13 ps is observed, where a falling output results in a longer delay than a rising output. For the clock distribution, using 1000 Montecarlo simulations, the skew variance is 1.53 ps for rising clock and 1.55 ps for falling clock. This skew variance is calculated based on the individual skew in each of the 136 leafs present in the RF-DAC. To put these results in contrast to the relative values presented above, we here assume a peak sample rate of 10 GS/s, giving a sample period

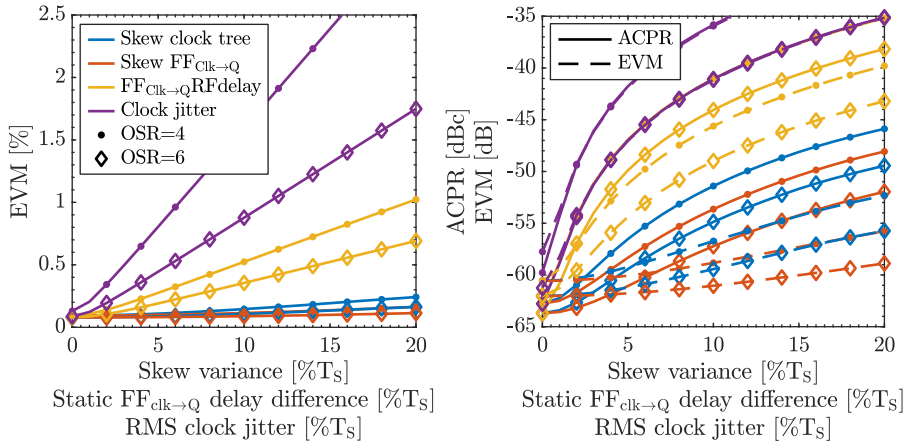


Figure 7.4: (a) EVM and (b) ACPR and EVM in dB, for different amounts of simulated skew in the clock network, for the FFs clock-to-Q propagation delay, for a static FF data-dependent delay, and for clock jitter.

of 100 ps, allowing us to directly convert the variance into percent. Applying the properties gathered for the FFs and clock distribution to the model, we get an EVM of 0.67 % and an ACPR of −38.8 dBc. Connecting the different contributions with the results in figure 7.4, we can observe that the difference between the rising and falling delay has the largest impact on the achievable performance. The impact of jitter is not considered here, but it is assumed to be smaller than the impact brought by the difference in rising and falling delay.

Placing FFs in each unit cell not only simplifies the layout, it also makes the skew more predictive. In addition, with fewer critical signals, it becomes easier to minimize the total skew. Although the power consumption for each individual FF is not that large, even at high a sample rate, with around a thousand FFs, the resulting power consumption is significant. From the results presented here, it should be noted that in addition to being optimized for power, the FFs must also have a small difference between the rising and falling delay. Note that a large difference between the rising and falling delays will be as problematic when the FFs are located within the unit cells, as if they are located along with the driving logic.

7.3 Switching induced supply noise

In addition to the effects presented above, it is expected that the RF-DACs will be affected by noise caused by variations in the supply current that is dependent on the control code-word. Up-sampling and pulse-shaping are used to provide band-limited signals at the modulator output. A low OSR is desirable as a

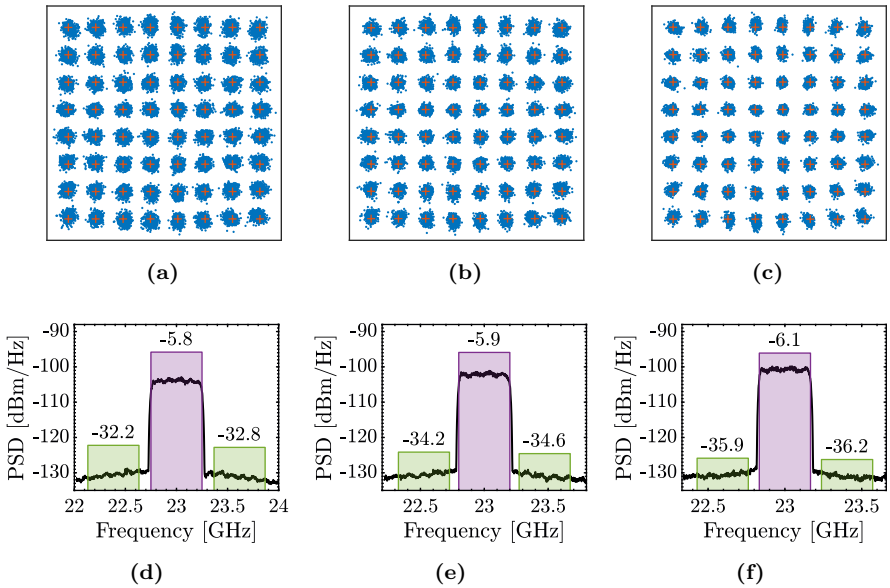


Figure 7.5: (a) Constellation diagram and (d) output spectrum for an OSR of 4. (b) Constellation diagram and (e) output spectrum for an OSR of 5. (c) Constellation diagram and (f) output spectrum for an OSR of 6. Results are measured using the modulator presented in paper B using 64-QAM SC signals sampled at 2 GS/s.

larger portion of the sample rate may be used for transmitting information. With oversampling, the step taken from one symbol to the next is split into several smaller steps taken by each sample. With increased oversampling, the per-sample step is reduced, bringing smaller changes in the RF-DACs supply current.

To evaluate if supply noise is responsible for the degraded performance observed in the measurements, measurement results are compared with simulations. Measurements have been performed using the 2×10 b RF-IQ modulator from paper B. 64-QAM SC signals with an OSR in the range 4–6, sampled at 2 GS/s are used. A low sample rate is here selected to reduce the impact of the limited bandwidth in the output matching network. In figure 7.5, constellation diagrams and output spectrums are presented for these three cases. In table 7.1, the corresponding EVM and ACPR are listed. The table also presents the average number of active unit cells and the average per-sample change in the number of active unit cells. These two are proportional to the average supply current and the average change in the supply current respectively. With a fixed sample rate, the varying OSR will result in changing channel bandwidths. Hence, with a flat noise floor, a small change in the ACPR, proportional to the changed channel bandwidth, is expected. However, the observed ACPR change cannot be fully explained by the changed channel bandwidth, although a fairly

Table 7.1: Measured EVM and ACPR at different OSR using the RF-IQ modulator is paper B generating a 64-QAM SC signal at a sample rate of 2 GS/s. In addition, the table also shows the average number of active unit cells and the per-sample change in the number of active unit cells.

OSR	4	5	6
EVM [%]	5.36	4.79	4.30
EVM [dB]	−25.4	−26.4	−27.3
ACPR [dBc]	−26.4	−28.3	−29.8
Average number of active unit cells (I+Q)	275	270	270
Average per-sample change in number of active unit cells (I+Q)	106	86	73

flat noise floor is observed. Excluding this expected ACPR change gives similar changes in both the EVM and ACPR with respect to a changes OSR.

In the spectrum shown in figures 7.5d to 7.5f, a small change in the power spectral density (PSD) is observed when comparing the three different OSR settings. This indicates a connection between the per-sample change in the number of active unit cells and the observed noise level. To confirm the cause of the noise, simulations were set up using simplified RF-DACs, the output matching network, and bond wires. The simulations were performed both by stepping the number of the active unit cells with the average per-sample change in the number of active unit cells and by using proper modulated signals. When stepping the number of active unit cells, an increased noise floor was observed. The noise-floor level was related to the number of unit cells toggling. With modulated signals, a small improvement in the EVM and ACPR was observed when increasing the OSR. However, the observed performance changes were not large enough to explain the changes observed in measurements. Thus, the simulations cannot give conclusive results on if supply noise caused by large changes in the supply current limits the measured performance.

In RF-DACs with constant biasing current [37], this effect is not present. On the other hand, these RF-DACs suffer from a poor efficiency at lower input codes, which is problematic considering the distribution of input codes for modern communication signals.

7.4 Extended OFDM results

To better understand what limits the performance for wideband OFDM signals, I here present additional measurement results for the RF-IQ modulator presented in paper B. In figure 7.6, constellation diagrams and output spectra are shown for 3 to 5 simultaneous 400 MHz 64-QAM OFDM channels having a tone-spacing of 120 kHz. All these results are gathered using a sample rate of 9 GS/s and achieve a BER better than 10^{-3}. Taking a careful look at the constellation

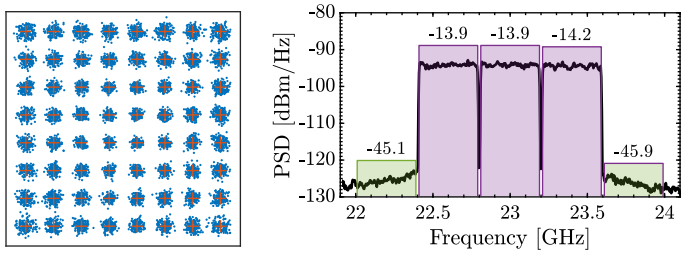
diagrams in figures 7.6a, 7.6c and 7.6e, we can observe an increased spread around each constellation point, indicating an increased noise level. In the output spectra in figures 7.6b, 7.6d and 7.6f, an increased noise level is also observed in the adjacent channels. This is expected as the effective OSR is reduced when the number of simultaneous channels is increased.

With additional channels, the transmitted power per channel is reduced, resulting in an expected ACPR reduction. The ACPR reduction is however not only caused by the reduced signal power. From the spectra shown in figures 7.6b, 7.6d and 7.6f, one can observe that the channel power is reduced further away from the center, further reducing the ACPR. This is a result of the limited bandwidth in the output matching network. One can here also observe that the power in the adjacent channels increases slightly when additional channels are used. This additional noise is also expected to appear within the channels, degrading the EVM. When excluding the ACPR reduction caused by the reduced channel power and limited bandwidth of the output matching network; a similar degradation of both the EVM and ACPR is observed. This confirms that the increased noise is present both in-band and in the adjacent channels. Since the effective OSR is reduced when increasing the number of adjacent channels, given a fixed sample rate; the per-sample change in the number of active unit cells will increase. Hence, the performance is limited by the same effect discussed in the previous section.

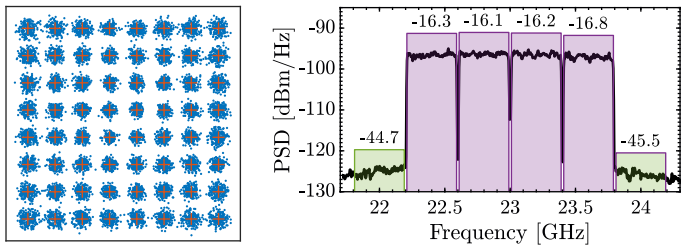
Comparing these results to the EVM (8 %) and ACPR (−28 dBc) requirements for 5G mm-Wave channels [2], one can observe that the EVM requirement is fulfilled with five simultaneous channels while the ACPR requirement is not.

7.5 Summary

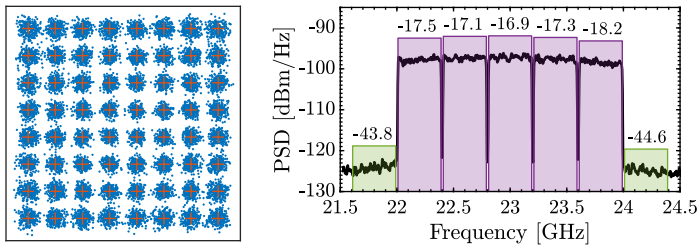
In this chapter, I have studied the different quadrature LO generation circuits used in papers A and B in more detail. In addition, I have also analyzed how skew, the difference in the propagation delay, and clock jitter affect the performance. I have also studied the impact of noise introduced by changes in the RF-DACs supply current, using a combination of simulations and measurement results. Finally, additional measurement results for aggregated OFDM channels are presented.



(a) 6.39 Gb/s, EVM 5.72 % **(b)** ACPR −31.24 dBc



(c) 8.52 Gb/s, EVM 6.43 % **(d)** ACPR −28.42 dBc



(e) 10.64 Gb/s, EVM 7.12 % **(f)** ACPR −26.34 dBc

Figure 7.6: Constellation diagram and output spectrum for (a)-(b) three aggregated 400 MHz OFDM channels, (c)-(d) four aggregated 400 MHz channels, and (e)-(f) five aggregated 400 MHz channels, respectively. All measurements are performed using a sample rate of 9 GS/s and for all cases, a BER $<10^{-3}$ is observed.

Chapter 8

Predistortion using non-linear RF-DAC

In this chapter, the concepts and results presented in paper C will be extended. The focus will be on comparing the linearization performance in the static case with the performance achieved for modulated signals. Due to limited space in the paper, this comparison was not possible to include there. Limitations with this linearization concept will also be discussed.

8.1 Predistortion concept

This predistortion concept extends the use of a segmented non-linear scaling presented in paper B. Here, the scaling is used not only to linearize the RF-DACs but also the PA they drive. The PA non-linearity is to a large extent defined by its static characteristics, AMAM and amplitude modulation to phase modulation (AMPM). With an inverted AMAM driving characteristic, a linear PA output may be realized. Since the required characteristic is static, it may be realized with a non-linear RF-DAC scaling. By selecting the transistor widths for the different segments, an inverse of the joint AMAM characteristic for the cascaded RF-IQ modulator and PA may be realized. As this characteristic is smooth, only a small number of segments are needed. The required number of segments is dependent on the non-linearity and the targeted RF-DAC resolution.

Using this linearization concept, the AMPM cannot be compensated for. However, through the RF-DAC output matching, it is possible to reduce the impact of small AMPM variations. Thus, a small phase variation may be achieved across a range of RF-DAC bias conditions.

As the expanding non-linear scaling is static, short-term memory effects, for example, caused by rapid changes in the output power cannot be compensated for. Long-term variations, such as temperature variations, may be adapted for through bias adjustments.

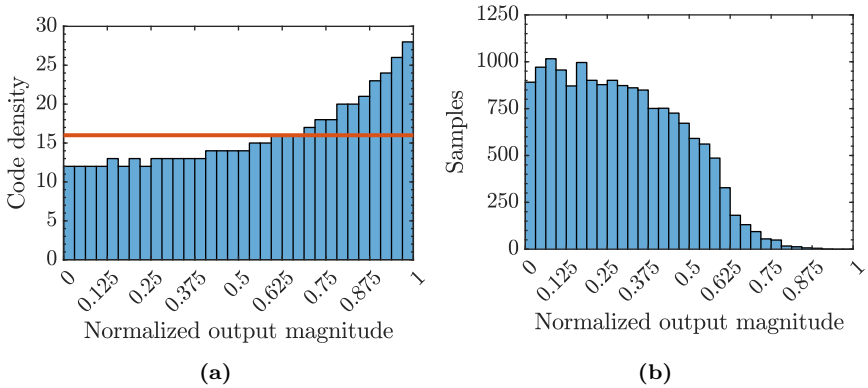


Figure 8.1: (a) Example code density for the expanding non-linear function resulting from using a DPD to linearize the PA non-linearity. The orange line represents the case with uniform code density. (b) Distribution of the real part of the normalized output magnitude for a 256-QAM SC signal. The signal is up-sampled four times and 4096 symbols are used. Both histograms are divided into 32 bins.

8.1.1 Code density

With predistortion implemented in the digital domain, using a uniform DAC to translate the signal into the analog domain, a uniform code density cannot be achieved. When representing an expanding function using uniformly distributed levels, a denser mapping results for the higher input levels, that is a higher code density, compared to the lower input levels. With this linearization concept, the expanding function needed to linearize the AMAM characteristic is realized using segments with unit cells of different sizes. This way, a constant code density is achieved, that is, a uniform mapping from digital code-word to analog magnitude.

In figure 8.1a, a 32-bin histogram, shows the code density as the number of input codes per PA output range. In this figure, an increased code density is observed for higher output levels compared to the uniform code density achieved when the expanding function is realized in the RF-DACs. Correspondingly, a lower code density is observed for lower output levels. The spread in code density is dependent on the amount of non-linearity the expanding function needs to compensate for. In figure 8.1b, the distribution of the real part of the output magnitude for a 256-QAM SC signal up-sampled four times is shown. Here, a majority of the samples are represented by output levels in the lower half of the range. Clearly, a majority of the samples experience a reduced code density.

In a transmitter, the resolution needed to fulfill the performance requirements for modulated signals may be derived from the modulation format in use, assuming uniform quantization levels. For a given range, this also gives the size of the smallest step. To keep the smallest step constant when using DPD,

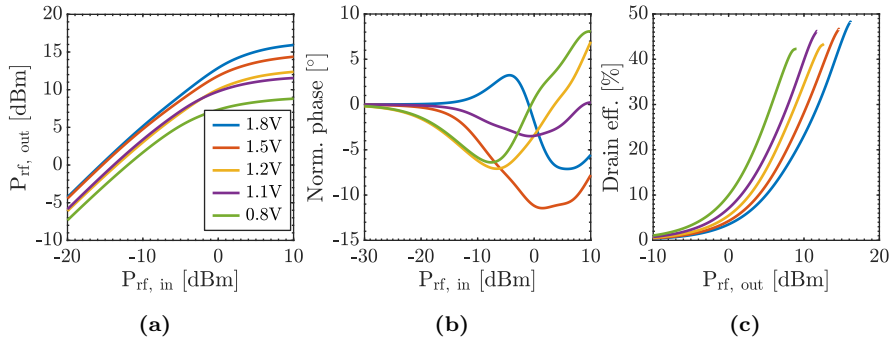


Figure 8.2: (a) AMAM, and (b) AMPM versus PA input power for different supply voltages. (c) PA drain efficiency versus PA output power for different supply voltages. The nominal bias voltage (V_{G2}) for the top transistor is 1.45 V, but it is reduced to 1 V for supply voltages <1.2 V.

additional levels are required, resulting in the need for an increased DAC resolution. Again, the required increase in resolution is dependent on the amount of non-linearity that is compensated for. Thereby, for DPD, there is in addition to the computational cost also a cost for the increased DAC resolution required.

8.2 Static versus modulated performance

In paper C, the performance across LO magnitude and DAC supply voltage was mainly presented for the static case due to space restrictions. To better elucidate how the trade-off between magnitude and phase errors affect the modulated performance, I here present results both for the static case and when modulated signals are used.

In figures 8.2a and 8.2b, the PA AMAM and AMPM characteristics are plotted versus the input power for different PA supply voltages. In addition, in figure 8.2c, the DE is plotted versus the PA output power at various PA supply voltages. Here, one can observe the benefit of, from an efficiency perspective, operating the PA at a reduced supply voltage when a reduced output power is required. This however changes the PA AMAM and AMPM characteristics.

In figure 8.3, the RMS linearity (figures 8.3a to 8.3c), the maximum phase change (figures 8.3d to 8.3f), the EVM (figures 8.3g to 8.3i), and the ACPR (figures 8.3j to 8.3l) are presented at various RF-DAC bias-combinations, that is, LO magnitude and DAC supply voltage. This is done for three different gain settings (G=−5 dB, 0 dB and 5 dB), where G=0 dB is the nominal gain setting used when selecting the non-linear scaling. Through this gain setting, it is possible to study the linearization capabilities for different PA input power requirements. In a system, a reduced gain may result from additional losses

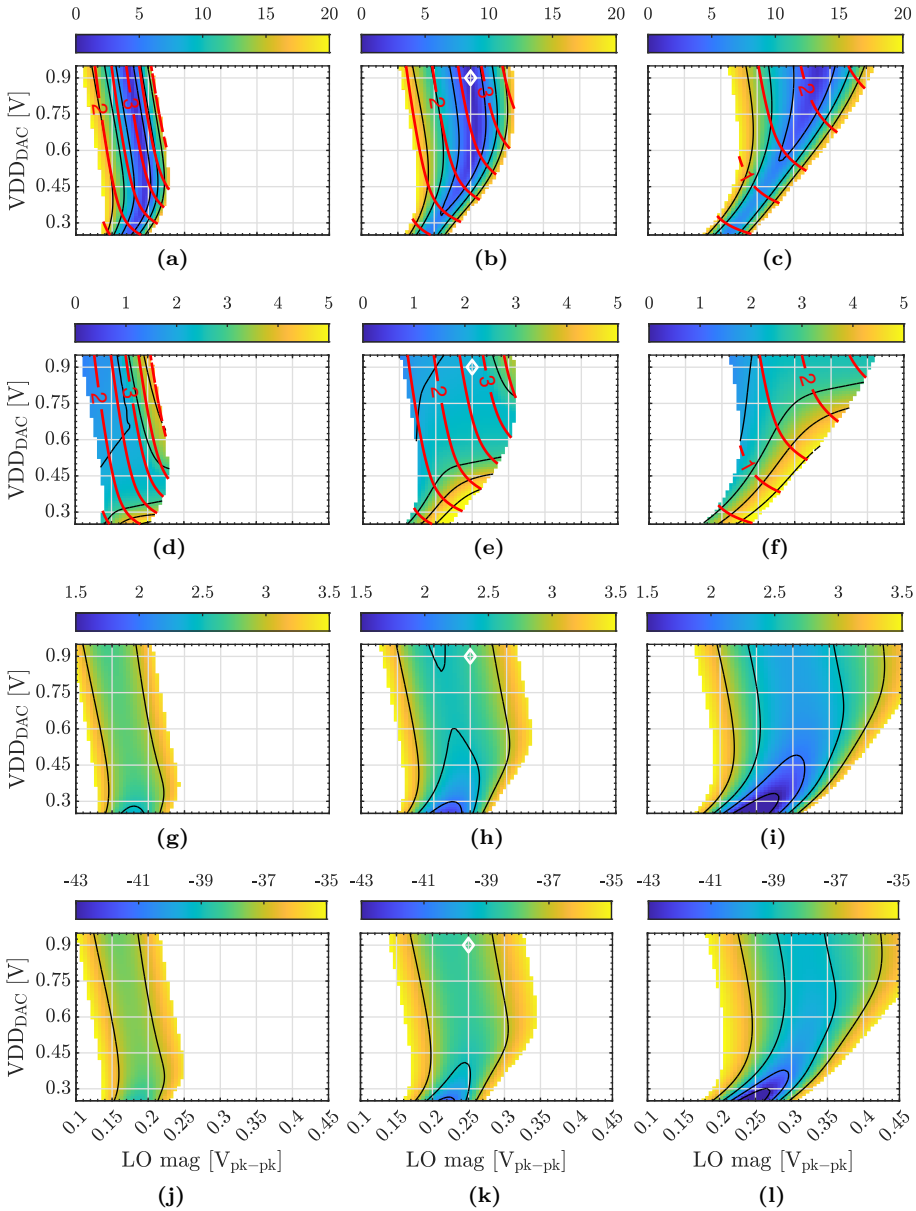


Figure 8.3: (a) to (c) RMS linearity, (d) to (f) maximum phase change, (g) to (i) EVM, and (j) to (l) ACPR, versus LO magnitude and DAC supply voltage. (a), (d), (g), and (j) with gain set to 5 dB, (b), (e), (h), and (k) with gain set to 0 dB, and (c), (f), (i), and (l) with gain set to −5 dB. Red contours indicate PA compression in dB. White dot shows nominal design point. The black contours represent the ticks in the color legend.

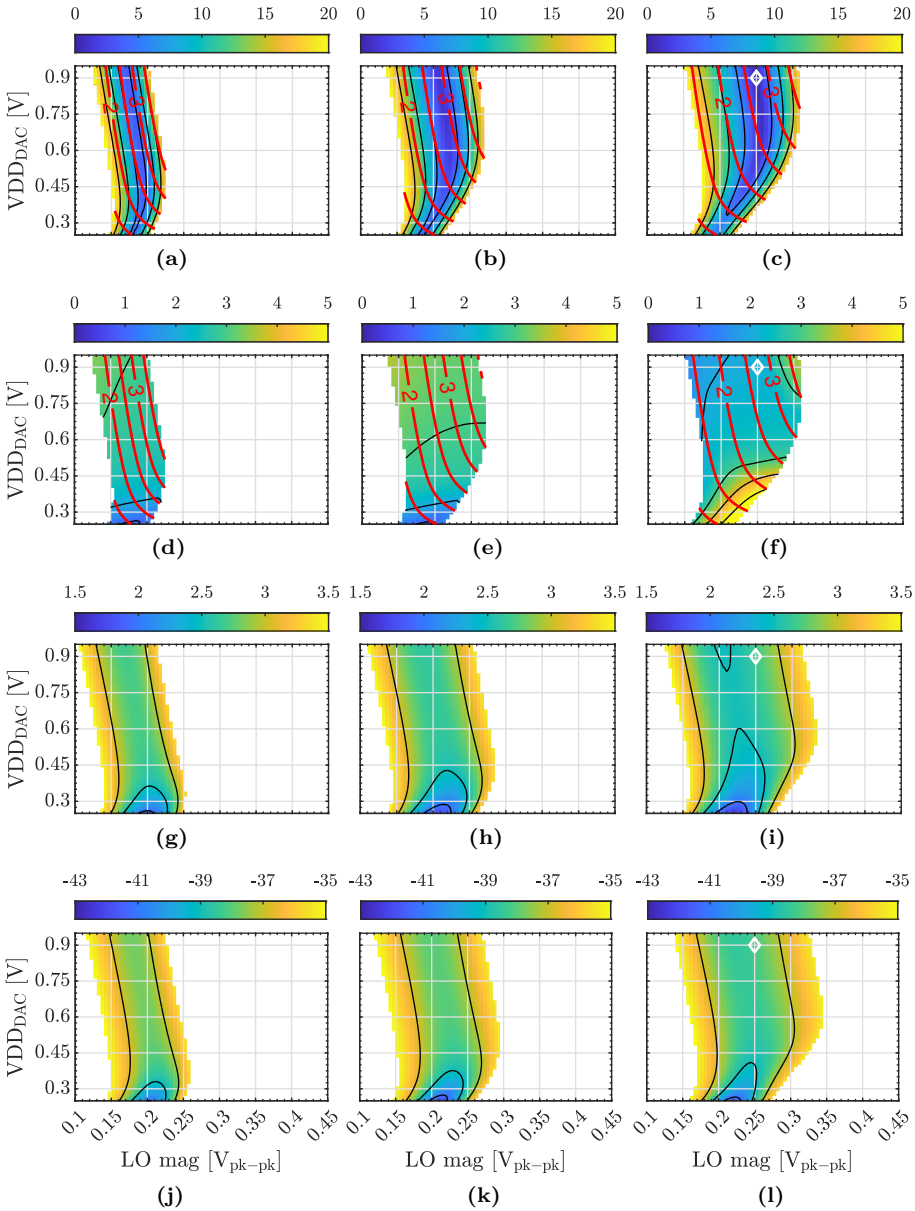


Figure 8.4: (a) to (c) RMS linearity, (d) to (f) maximum phase change, (g) to (i) EVM, and (j) to (l) ACPR, versus LO magnitude and DAC supply voltage. (a), (d), (g), and (j) with PA supply voltage set to 0.8 V, (b), (e), (h), and (k) with PA supply voltage set to 1.2 V, and (c), (f), (i), and (l) with PA supply voltage set to 1.8 V. Red contours indicate PA compression in dB. White dot shows nominal design point. The black contours represent the ticks in the color legend.

in the circuits connecting RF-DACs to the PA. An increased gain may, on the other hand, result from the insertion of an additional amplifier between the RF-DACs and the PA. At the nominal design point, a peak PA input power of $-0.5\,\mathrm{dBm}$ is used in the static case.

Comparing the best-performance bias conditions in the static case with the best-performance settings for modulated signals, a large overlap can be observed across all three gain settings, as seen in figure 8.3. For modulated signals, the optimum-performance settings are shifted slightly towards lower LO magnitudes. This shift is expected since the non-linear scaling is selected through simulations using a single RF-DAC. To represent the targeted Cartesian modulator, two RF-DACs are combined. This results in a slightly increased peak output power when using modulated signals compared to the static case, thus the PA is driven slightly deeper into compression. As a result, for optimum linearization, reduced output power from the RF-DACs is required, which is achieved at lower LO magnitudes. The same thing is observed for all three gain settings.

Above, the linearization capabilities have been studied at different PA input power requirements. For efficient operation across different output power levels, it is desirable to adjust the PA supply voltage. By reducing the PA supply voltage, the efficiency at a given output power level increases, as shown in figure 8.2c. However, with changed PA supply voltage, the AMAM and AMPM characteristics will change, as shown in figures 8.2a and 8.2b. In figure 8.4, the linearization performance, both in the static case and with modulated signals, is shown for three different PA supply voltages ($0.8\,\mathrm{V}$, $1.2\,\mathrm{V}$ and $1.8\,\mathrm{V}$). Since a reduced PA supply voltage results in increased compression, it is, also this time, expected that the optimum is shifted towards lower LO magnitudes and lower RF-DAC output power, which also is observed in the figure.

With predistortion, a higher output power level and efficiency may be achieved at a given EVM and ACPR level. At the nominal design point and with a constant ACPR, the average DE is increased from 7 % to 11.9 % with a $2.7\,\mathrm{dB}$ increase in the average power compared to using uniform RF-DACs. In addition to the ability to linearize the PA through a $7.1\,\mathrm{dB}$ peak output power range, large improvements in the average DE and output power compared to using uniform RF-DACs are also demonstrated. This improvement comes with no other cost than somewhat increased transistor widths in the RF-DACs.

The ability to tune the LO magnitude is already a feature available in the quadrature LO generation used in paper B. From a system perspective, it is desirable to be able to adjust the DAC supply voltage. The simulations show that it is sufficient with a low resolution in the DAC supply voltage stepping to achieve good linearization. In addition, the linearization only needs to adapt to slowly changing effects, thus rapid changes in the DAC supply voltage are not needed.

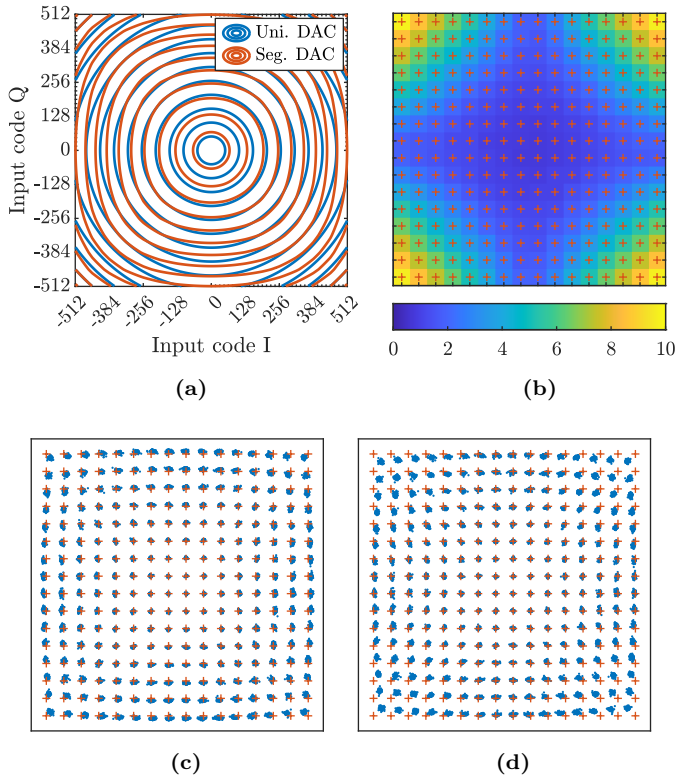


Figure 8.5: (a) Constant output magnitude curves for the RF-DAC output, versus input codes, for both uniform and segmented non-linear RF-DACs. Constellation diagram for cascaded segmented non-linear RF-DACs and PA, (c) using equalization based on all symbols, and (d) using equalization based on the symbols located at the four centermost constellation points. (b) The RMS EVM per constellation point based on the constellation in (d).

8.2.1 Limitations with Cartesian modulator

To understand why the observed optimum is shallower with modulated signals, the potential limitations with this linearization concept need further analysis. Since AMPM cannot be compensated for, it may be assumed that the phase variation will limit the achievable linearization performance. However, as the maximum phase variation is small, it has a small impact on the performance. From figure 8.3, a clear connection between a large phase variation and a reduced modulated performance cannot be seen. This indicates that AMPM only has a small effect on the overall modulated performance, for this combination of RF-DACs and PA.

By excluding the phase, the focus is purely put on the amplitude behaviour and how it limits the performance. In figure 8.5a, constant magnitude contours

for the DAC output are shown versus the input codes, both when using uniform DACs and when using segmented non-linear DACs. With uniform DACs, it is expected that the constant magnitude curves should be round, as shown in the figure. With the segmented DACs, the constant magnitude curves are only round for low input codes. For higher input codes, the shape is translated into a square with rounded corners. With the expanding non-linear function generated by the segmented DAC, there will for high output codes be a larger range in which the other quadrature component does not affect the output magnitude, compared to the uniform case. When following these straight segments, that is, when one of the quadrature components is significantly larger than the other, the expanding non-linear function will compensate for the PA compression well. For input codes in the rounded corners, on the other hand, the PA is driven deeper into compression than what our non-linear scaling compensates for. This is a result of the one-dimensional linearization that this concept builds on. The linearization accuracy will be limited for some output signal combinations. Hence, it is expected that there will be a floor limiting the achievable performance, explaining the shallower optimum observed for modulated signals in figures 8.3 and 8.4.

To illustrate the impact of improper linearization at the corners, figure 8.5d show a constellation diagram where equalization is performed only for symbols at the four centermost constellation points. In figure 8.5b, the RMS EVM is plotted for each individual constellation point, further highlighting where the linearization is accurate. When performing equalization using all symbols, the constellation diagram shown in figure 8.5c results. Here, one can observe that the constellation is expanded compared to figure 8.5d. This behaviour has also been observed in the measurements of the RF-IQ modulator presented in paper B.

8.3 Summary

In this chapter, the concept of code density has been introduced. Its impact on the resolution requirement when using DPD was also discussed. Here, it is clear that DPD not only brings additional computational cost, it also brings higher resolution requirements for the DACs. In addition, this chapter also presented additional results showing the achievable performance using modulated signals. Finally, the limitations with this linearization concept were discussed.

Chapter 9

Performance evaluation of high-speed ADC

High-speed and efficient ADCs are essential in the observation path used when linearizing wideband transmitters. As seen in section 6.3, high-speed ADCs often use replication to overcome the limitations brought by a tight timing budget. However, time-interleaving many ADCs is both complex and costly. To efficiently achieve a high sample rate in a TI converter, each individual converter must have a high sample rate to start with. In addition, replication may also be used within the converter itself. In a SAR converter, the comparator decision and reset time together with its resolution limits the achievable sample rate. The concept of using alternating comparators was first introduced by Kull et al. [144] as a way to eliminate the reset time from the critical timing path, thereby increasing the speed of a single-channel converter.

In paper D, a SAR ADC designed based on the principles introduced in [144] was evaluated to understand its limitations. Through this evaluation, several sources limiting the performance were identified. One is directly related to the alternating comparator topology: a decision-dependent comparator reset time. In this chapter, I will discuss the use of multiple comparators in a SAR converter and the potential implications it may bring.

9.1 Alternating comparators

Alternating comparators have reduced the critical timing path in SAR ADCs by eliminating the reset time from the critical timing path. Asynchronous timing is often used to reduce the time margin needed to handle the magnitude-dependent comparator decision time. With synchronous timing, this margin is needed after each comparison. Combining alternating comparators with asynchronous timing allows us to perform an increased number of comparisons within a given time frame. However, the reset time will be decision-time-dependent, and thus

signal-dependent.

With an incomplete reset, the comparator will be biased towards the result of the previous comparison it performed. In contrast to mismatch, which is static and may be compensated for, this reset-induced offset voltage is dependent on the decision time in the other comparator, and it will therefore not be possible to compensate for.

To overcome the problem with incomplete comparator reset, an individual comparator may be used for each decision [155, 180]. However, a large number of comparators, not only increase the converter footprint, they also increase the complexity of the comparator calibration. Clearly, both the increased calibration complexity and the performance improvement achieved with extended reset must be considered. By introducing a single additional comparator, alternating among three rather than two comparators, the time available for resetting a comparator is doubled, while keeping the complexity and footprint for the comparator calibration small. From figure D.10a (paper D), one can observe that already with a doubled reset time, essentially all reset-induced offset voltage will be eliminated, given that identical comparators are used. Further increasing the number of comparators will increase the complexity of the calibration circuit without any large improvements on the reset-induced offset voltage.

9.1.1 Offset voltage in alternating comparators

Mismatch in comparators results in shifted decision levels. This shift may be seen as offset voltage at the comparator input. With a single comparator, this offset voltage will be static and as long as it is small, calibration will not be required. When multiple comparators are used, they will all experience mismatch in different ways, and thus have different offset voltages. The offset voltage may here be divided into two parts: one common offset voltage, representing the average offset voltage of all comparators, and one difference offset voltage, representing the offset voltage deviation from the common offset voltage. With two comparators, the difference offset voltages are identical in magnitude but have different signs. The common offset voltage will be static, just as the offset voltage in a SAR ADC with a single comparator. In contrast, the difference offset voltage will vary with the comparator being used, thus introducing additional noise.

Simulations of alternating-comparator-based converters have been performed, both using the 8 b redundant scaling used in paper D, and using binary scalings with a resolution of 6–8 b. This is to analyze the impact that difference offset voltage has on the SNDR. The results are shown in figure 9.1. The difference offset voltage is here normalized to the LSB, thereby the absolute offset voltage is different for the three resolutions shown, given a fixed range. The figure shows that the scaling has no impact on the resulting SNDR degradation caused by the difference offset voltage. Already for a small difference offset voltage, a large SNDR reduction is observed. A small difference in the SFDR has been observed between the redundant scaling and the binary scaling. However, this difference is

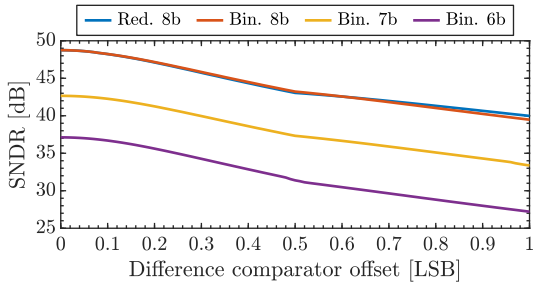


Figure 9.1: SNDR versus difference comparator offset in an alternating comparator topology. Simulations are based on both the 8 b redundant scaling used in paper D, and binary scalings with a resolution of 6–8 b.

not significant. One can also observe that with reduced resolution, the SNDR is degraded with the expected 6 dB/b over the entire range of simulated difference offset voltages.

With alternating comparators, the difference offset will affect each decision differently, making it hard to compensate for the effects in the digital domain. Rather, the comparators need individual calibration to minimize their offset voltage. With individual calibration, both the common offset voltage and the difference offset voltage will be reduced. As each comparator requires its own calibration circuit, the cost of adding additional comparators is large, making the concept of using one comparator per decision costly from a hardware perspective.

9.2 Summary

SAR ADCs using asynchronously controlled alternating comparators suffer from decision-dependent reset times. Using an individual comparator per decision eliminates the issue of incomplete reset, but brings larger and more complex comparator calibration. Already using three alternating comparators, the reset-induced offset voltage is to a large extent eliminated while the cost for comparator calibration is kept at a minimum.

Chapter 10

Conclusions

This thesis contains studies of data converters intended for wideband mm-Wave MIMO transmitters. For such transmitters, efficient use of the hardware resources is critical. The RF-IQ modulator plays a central role here. In this thesis, the possibility of using an RF-IQ modulator as a predistorter has also been investigated. While the RF-IQ modulator has a central role in a wideband transmitter, the ADC is just as important. In this thesis, the impact of offset voltage when alternating between multiple comparators has been evaluated, using a combination of simulations and measurements. When pushing for higher sample rates, duplicated hardware might be beneficial from a timing perspective but it might impact the performance in unforeseen ways as discussed in this thesis.

Below, a summary of the contributions presented in papers A to D will follow. Finally, an outlook on potential future research topics connected to the findings presented in this thesis follows.

10.1 Contributions

This thesis is based on the work presented in the four papers (papers A to D).

Paper A presents a 2×6 b, 8 GS/s Cartesian RF-IQ modulator operating at 17–24 GHz. This was the first modulator to demonstrate the use of non-overlapping LO signals at mm-Wave frequencies, reducing cross-modulation distortion. A double balanced unit cell, combining sign generation with inherent LO leakage neutralization, was also demonstrated. This unit cell topology is also base for invention I. In addition, this modulator demonstrated the highest reported sample rate for a >3 b fully integrated Cartesian modulator.

In paper B, the use of non-overlapping LO signals in a RF-IQ modulator is further explored. Thanks to the non-overlapping LO signals, the RF-DACs can be individually linearized using an expanding segmented non-linear scaling. With binarily grouped unit cells, the segment decoding logic is simple. This

paper also introduces asymmetrical TIAs as a way to maximize the voltage swing and large-signal gain for non-overlapping LO signals. This RF-IQ modulator is the first mm-Wave implementation to demonstrate the transmission of four aggregated 400 MHz OFDM signals.

In paper C, the non-linear scaling concept presented in paper B is extended to linearize a cascaded RF-IQ modulator and PA. The linearization is achieved with no additional hardware. Although relying on a fixed scaling, this concept shows great flexibility in the range of non-linearity that it can handle. This concept is the base for invention II.

The impact of offset voltage in an alternating comparator SAR ADC significantly differs from the static behaviour observed in single comparator SAR ADCs. In paper D, an 8 b SAR ADC is evaluated with focus on the impact of offset voltage, not only static, but also signal dependent. The impact of offset voltage on the signal statistics is studied with offset voltage calibration both enabled and disabled using both measured data and simulation results.

10.2 Future work

Based on the content presented in this thesis, several closely related topics are interesting for further studies, in addition to further investigations of the factors limiting the performance in the data converters presented in this thesis.

In addition to a wide bandwidth, a power-efficient operation is also desirable. In the RF-IQ modulators presented in this thesis, the quadrature LO generation has been responsible for a large portion of the power consumption. To build the most efficient transmitter, the potential benefits of placing a PA at the RF-IQ modulator output must be studied. With reduced output power requirements for the RF-IQ modulator, the power consumption in the quadrature LO generation may potentially be reduced.

The linearization concept presented in paper C has only been evaluated using simulations, although the principles were used in the RF-IQ modulator presented in paper B. It would be useful to show that the principle also works in practice over a wide bandwidth. For this, co-implementation of the expanding non-linear RF-IQ modulator and a PA is required.

With the non-linear scaling, the AMAM non-linearity may be compensated for. It would also be useful to investigate if the RF-IQ modulator could compensate for other non-linear effects, such as AMPM or memory effects. In addition, there are limits to how well a RF-IQ modulator having an expanding non-linear scaling can linearize a PA. A better understanding of these limits and how their impact can be reduced would be highly desirable.

A final question is how DPD-complexity may be reduced when combining it with a non-linear RF-IQ modulator. Also, it would be intriguing to investigate if DPDs should be implemented in a different way when combining them both with the RF-IQ modulator itself and when it is used to drive a PA.

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