Lifetime Modelling of Large Area Solder Joints in Power Electronic Inverter Units

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Declaration of Authorship
Selbständigkeitserklärung

I hereby declare that this doctoral thesis with the title "Lifetime Modelling of Large Area Solder Joints in Power Electronic Inverter Units" has been written independently with no other sources and aids than quoted.

Hiermit erkläre ich, dass ich die vorliegende Doktorarbeit mit dem Titel "Lifetime Modelling of Large Area Solder Joints in Power Electronic Inverter Units" selbstständig und nur unter Verwendung der angegebenen Quellen und Hilfsmittel angefertigt habe.

Allen Jose George
Munich, July 26, 2021

Dedicated to the illustrious Indian scientists, astronomers and mathematicians who have been forgotten in the annals of time and history.

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Though only my name appears in bold on the cover of this thesis, many people have contributed to its production. I owe my gratitude to all those people who have made this research work possible.

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Contents

Abstract

Power electronics (PE) modules in inverter units are a critical part of the Hybrid/Electric vehicles (H/EV) drivetrain as they carry out the important function of power conversion and form the interface between the batteries and the electric motors while driving. The amount of power converted in modern H/EVs is already in the range of hundreds of kilowatts. Consequently, heat generation due to energy loss during the power conversion process is a significant risk as it could lead to device failure due to overheating. The generated heat is usually dissipated via a liquid cooled heat sink called the baseplate. The joining of the baseplate and the PE module is conventionally carried out through processes such as lamination or through thermal interface greases or glues. But as cooling requirements are increasing as a result of devices performing at increasingly higher power ratings, these methods are proving to be no longer sufficient and are being replaced by metallic solders (baseplate soldering) as they offer significantly better thermal conductivity. However, like other interconnect technologies, during reliability tests such as in passive temperature cycling (pTC), the joint between the power module and the baseplate develops cracks at/near the solder-intermetallic compound (IMC) interface. Such cracks increase thermal resistance between the baseplate and the power module and consequently increases the risk of overheating and device failure.

Given that the cracks observed in this research work were found to develop at/near the solder-IMC interface, a study on the IMC layer thickness was carried out. Variations in the growth characteristics of the IMC thickness with different solder profiles and different isothermal ageing conditions was investigated. Additionally, a method for transferring IMC growth results from isothermal ageing to non-isothermal ageing conditions was provided which enables the prediction of IMC thickness under pTC. Subsequently, the influence of IMC thickness on solder joint reliability was assessed through Finite Element Method (FEM) simulations. A detailed reliability investigation was carried out on multiple physical variants of the PE module-baseplate assembly. These variants were aged under three different temperature cycling profiles. Using this, key influence parameters with respect to reliability were uncovered. The experiments were replicated in FEM simulations with identical geometry and loading conditions. The FEM simulations provide an innovative method to account for the thermomechanical stresses induced during the manufacturing process of the PE module substrates, baseplate soldering and temperature cycling in a single simulation. A stress triaxiality and inelastic strain based FEM damage parameter was also formulated which showed excellent correlation with experimental results.

Zusammenfassung

Leistungselektronik (PE) Module in Wechselrichtereinheiten sind ein kritischer Teil des Antriebsstrangs von Hybrid-/Elektrofahrzeugen (H/EV), da sie die wichtige Funktion der Leistungsumwandlung übernehmen und bilden die Schnittstelle zwischen den Batterien und den Elektromotoren während der Fahrt. Die umgewandelte Leistung in modernen H/EVs liegt bereits im Bereich von Hunderten von Kilowatt. Die Wärmeentwicklung durch Energieverluste bei der Leistungsumwandlung, stellt hierbei ein erhebliches Risiko dar, da es zu Geräteausfällen durch Überhitzung führen kann. Die erzeugte Wärme wird in der Regel über einen flüssigkeitsgekühlten Kühlkörper, die sogenannte Grundplatte, abgeführt. Die Verbindung der Grundplatte mit dem PE Modul erfolgt typischerweise durch Wärmeleitfolie, Wärmeleitpasten oder Klebstoffe. Da die Anforderungen an die Kühlung durch immer leistungsstärkere Geräte steigen, reichen diese Methoden nicht mehr aus und werden durch metallische Lote (Grundplattenlöten) ersetzt, da diese eine deutlich bessere Wärmeleitfähigkeit aufweisen. Wie bei anderen Verbindungstechnologien kommt es jedoch bei Zuverlässigkeitstests, z. B. bei passiven Temperaturwechseln (pTC), zu Rissen in der Verbindung zwischen dem Leistungsmodul und der Grundplatte im Bereich der Grenzfläche zwischen Lot und intermetallischer Phase (IMC). Solche Risse erhöhen den Wärmewiderstand zwischen der Grundplatte und dem Leistungsmodul und erhöhen somit das Risiko einer Überhitzung und eines Geräteausfalls.

Aufgrund der in dieser Forschungsarbeit beobachteten Rissbildung im Bereich der Lot-IMC-Grenzfläche wurde eine Studie zur IMC-Schichtdicke durchgeführt. Variationen in den Wachstumscharakteristika der IMC Dicke bei verschiedenen Lotprofilen und unterschiedlichen isothermen Alterungsbedingungen wurden untersucht. Zusätzlich wurde eine Methode zur Übertragung der IMC Wachstumsergebnisse aus der isothermen Alterung auf nicht-isotherme Alterungsbedingungen bereitgestellt, die die Vorhersage der IMC Dicke unter pTC ermöglicht. Anschließend wurde der Einfluss der IMC Dicke auf die Zuverlässigkeit der Lötstelle durch Simulationen mit der Finite-Elemente-Methode (FEM) bewertet. Eine detaillierte Zuverlässigkeitsuntersuchung wurde an mehreren Konstruktionsvarianten des PE Moduls und der Grundplatte durchgeführt. Diese Varianten wurden unter drei verschiedenen Temperaturwechselprofilen gealtert. Auf diese Weise wurden wichtige Einflussparameter in Bezug auf die Zuverlässigkeit aufgedeckt. Die Experimente wurden in FEM-Simulationen mit identischen Geometrien und Belastungsbedingungen nachgebildet. Die FEM-Simulationen stellen eine innovative Methode dar, um die thermomechanischen Spannungen, die während des Herstellungsprozesses der Leistungselektronik Substrate, des Lötens der Grundplatte und der Temperaturzyklen entstehen, in einer einzigen Simulation zu berücksichtigen. Außerdem wurde ein auf Spannungstriaxialität und inelastischer Dehnung basierender FEM-Schadensparameter formuliert, der eine ausgezeichnete Korrelation mit experimentellen Ergebnissen zeigte.

List of Figures

List of Tables

List of Abbreviations

AC	Alternating Current
AF	Acceleration Factor
AMB	Activated Metal Brazing
BC	Boundary Conditions
BEV	Battery Electric Vehicle
BGA	Ball Grid Array
BVP	Boundary Value Problem
CAD	Computer Aided Design
CBGA	Ceramic Ball Grid Array
CFC	Chlorofluorocarbons
CSP	Chip Scale Packages
CTE	Coefficient of Thermal Expansion
CTOD	Crack Tip Opening Displacement
DBC	Direct Bonded Copper
DC	Direct Current
DCA	Direct Chip Attach
DIC	Digital Image Correlation
DoE	Design of Experiments
EoL	End of Life
FEM	Finite Element Method
HCF	High Cycle Fatigue
HEV	Hybrid Electric Vehicle
HEX	Hexahedral Elements
IGBT	Insulated Gate Bipolar Transistor
IMC	Inter-Metallic Compound
IVP	Initial Value Problem
LCF	Low Cycle Fatigue
MF	Multiaxiality Factor
MTTF	Mean Time To Failure
OFAT	One Factor at A Time
PCB	Printed Circuit Board
PE	Power Electronics
PHEV	Plug-in Hybrid Electric Vehicles
pTC	Passive Temperature Cycling
QFN	Quad Flat No-leads
QFP	Quad Flat Package
ROHS	Restriction of Hazardous Substances
SAC	Tin (Sn) Silver (Ag) Copper (Cu) Solder
SAM	Scanning Acoustic Microscopy
TC	Temperature Cycling
TET	Tetrahedral Elements
TF	Triaxiality Factor
THT	Through Hole Technology
TIM	Thermal Interface Materials
TSOP	Thin Small-Outline Packages
VPS	Vapour Phase Soldering
VWA	Volume Weighted Averaging
WLP	Wafer Level Packages

Whatever you do, or dream you can, begin it. Boldness has genius, power and magic in it.

Johann Wolfgang von Goethe (1749 – 1832)
German writer and statesman
As translated by John Anster (1793–1867)

Chapter 1

Introduction

Hybrid/Electric vehicles (H/EV) are no longer a thing of the future but a reality with already more that 7 million such automobiles in the market as of 2019 (Figure 1.1). Electric motors in these vehicles almost exclusively run on alternating current (AC) while the power source, i.e. the batteries, supply direct current (DC). There is thus a need for power conversion. This function is carried out within the Inverter unit by Power Electronic (PE) modules. With the increasing power of modern H/EVs, PE modules are required to convert power in the range of hundreds of kilowatts, or often, even more. There is some inherent energy loss during the power conversion process which manifests itself in the form of heat. It is also known that semiconductor chips in power modules which carry out the switching process during power conversion have become smaller [IL17]. Consequently, PE modules deal with high temperatures and high heat flux density ([De +18]) which is why their construction is built upon power substrates such as Activated Metal Brazing (AMB) or Direct Bonded Copper (DBC) substrates.

Heat generated on the chips is transferred via the AMB/DBC (or similar) substrate onto a liquid cooled metallic heat sink (baseplate) where it is eventually dissipated. It is therefore critical that the adhesive layer between the substrate and the baseplate offers minimal thermal resistance. Conventional assembly methods such as lamination and joining via thermal interface materials (TIM) are proving to be insufficient from a thermal conductivity point of

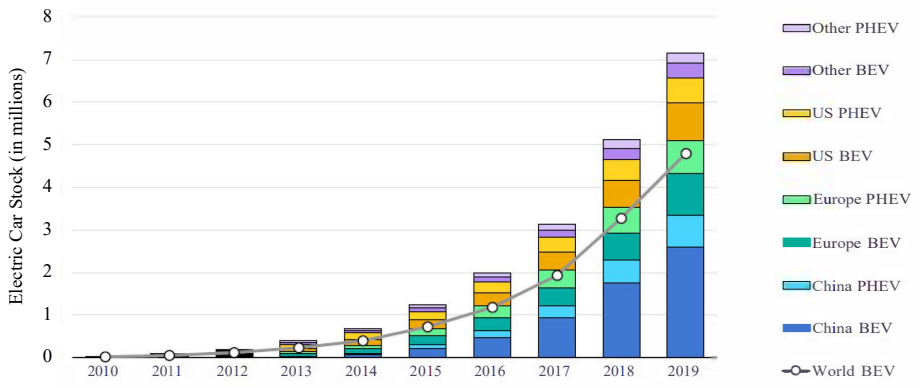


Figure 1.1: Increasing demand of hybrid and electric vehicles [IEA20]

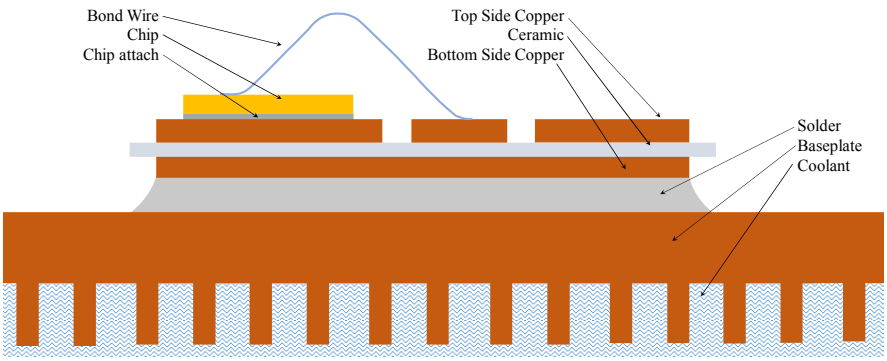


Figure 1.2: Schematic of baseplate soldered substrate

view for many applications and they also show significant degradation in material properties or joint quality during reliability tests such as passive temperature cycling (pTC)[OK11; Sku+13]. As a result, large area solder joints have come to the forefront as the interconnect technology between substrate and baseplate (baseplate soldering as shown in Figure 1.2). They offer not just good mechanical fixation but more importantly, as much as ten times higher thermal conductivity than conventional TIM materials. Having said that, like any other solder interconnect, these large area solder joints also develop cracks under pTC reliability tests. Such cracks increase the thermal resistance between the substrate and the baseplate which could lead to device failure as a result of overheating.

In this research work, an in-depth investigation of the reliability trends of these solder joints with respect to various influence parameters was carried out. The influence parameters included not only variations in construction geometry but variations in pTC profiles as well. A Finite Element Method (FEM) based simulation methodology was developed to account for stresses not just from temperature cycling, as is done in conventional solder joint reliability studies, but also stresses from the manufacturing process of the power substrate and baseplate soldering. From the FEM simulations, a stress triaxiality and inelastic strain based damage parameter was extracted that showed excellent correlation with experimental results. Based on the simulative damage parameter and experimental results, a phenomenological lifetime model is derived which is a powerful tool to predict the reliability of the above-mentioned solder joints under pTC.

If I have seen further than others, it is by standing upon the shoulders of giants.

Isaac Newton (1643 – 1727)
English mathematician, astronomer and physicist

Chapter 2

State of the Art

2.1 Basics of soldering technology

Soldering in modern electronics differs from the commonplace understanding of soldering. Industrial scale soldering processes rarely use the conventional manual methodology employing a soldering iron and solder wire. In many cases conventional soldering techniques are simply not possible mainly due to difficulty of maintaining quality of solder joints or the microscopic sizes of the joints involved. One of the most widely used soldering technique in microelectronics is the Reflow Soldering process.

2.1.1 Reflow soldering

For most large-scale soldering processes in microelectronics, the soldering process starts with the printing or dispensing of the solder in paste form. Solder paste is a suspension of powdered metallic solder (85-90 weight-%, 40-50 volume-%) in a thick medium called flux. The flux is composed of resins, activators, solvents, thixotropic agents and other additives. Solder paste is deposited on the surface to be soldered with the help of a squeegee and stencil as shown in Figure 2.1(a).The deposited solder as a result of this step is shown in Figure 2.1(b). This is followed by a *pick and place step* where the joining partners are assembled and then a heating step is started in a *reflow oven* which melts the paste and fuses the connection between the joining partners. The soldering process comprises majorly four stages, namely; (1) Preheating, (2) Dryout/Soak, (3) Reflow and (4) Cooling. as shown in Figure 2.2. In a conventional reflow oven, heating and subsequent cooling is achieved mainly through convection in an atmosphere of Nitrogen to prevent any oxidation. This is also its weakness. As the heat transfer is achieved through convection from hot gases to the joining partners, the heat transfer rate is low. For components with large thermal masses such as the ones considered in this research work, such a low rate of heating would be insufficient to achieve required soldering temperature profile characteristics. As a consequence, an alternate heat transfer method is required. The alternate method used in this research work is called *Vapour Phase Soldering (VPS)*. A general overview of VPS is discussed in the following section.

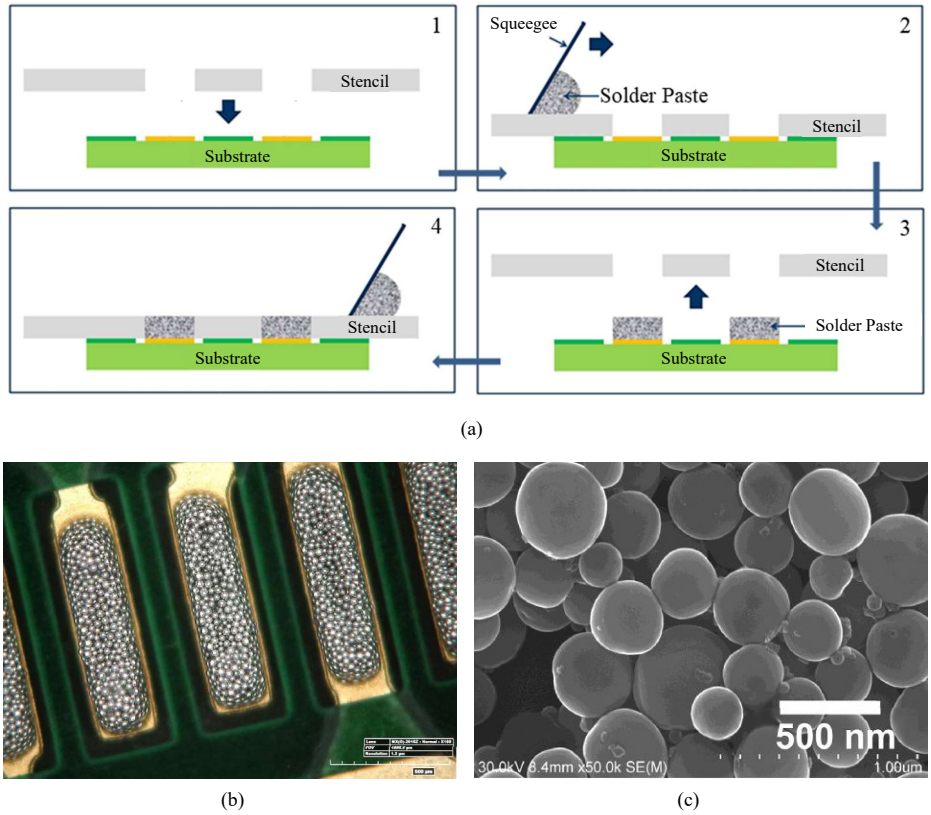


Figure 2.1: (a) Schematic of solder paste printing process. (Modified from [Jou+13]). (b, c) Printed solder paste as seen under optical [Ser16] and electron microscopes [IKP16]

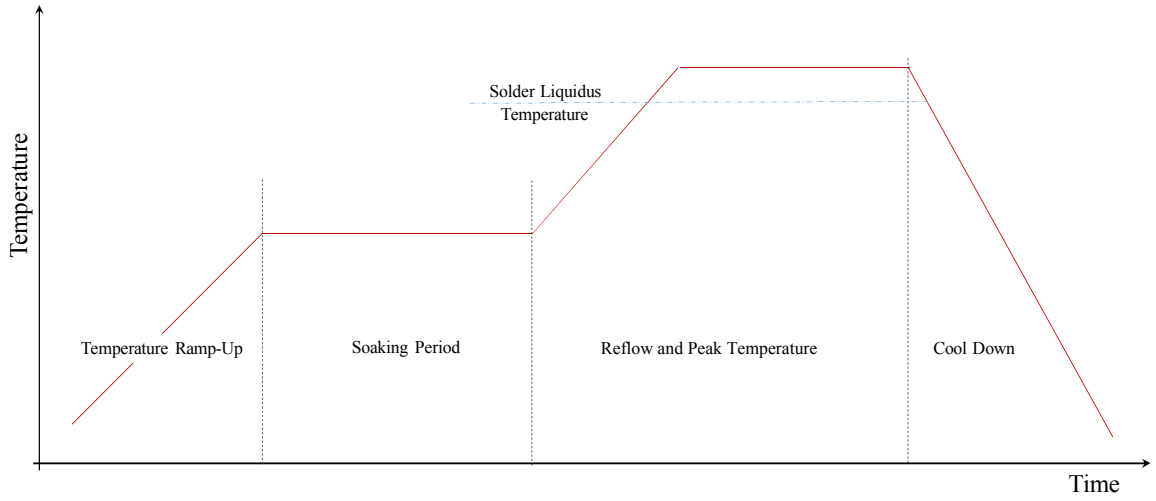


Figure 2.2: Typical soldering profile

2.1.2 Vapour Phase Soldering (VPS)

Vapour Phase soldering is a type of reflow soldering that was first developed in the 1970's by Pfahl and Ammann [PA75] and later developed by Wenger and Mahajan [WM81]. VPS achieves heat transfer through the latent heat of condensation. It works on the principle that when a body with a relatively lower temperature is immersed in the saturated vapour of a boiling liquid, the vapour condenses on the immersed body. This in turn transfers the latent heat of condensation to the immersed body and heats it up. This process continues until the colder body establishes thermal equilibrium with the vapour, *i.e.*, temperature of the vapour and immersed body become equal. The schematic setup of the VPS equipment is shown in Figure 2.3.

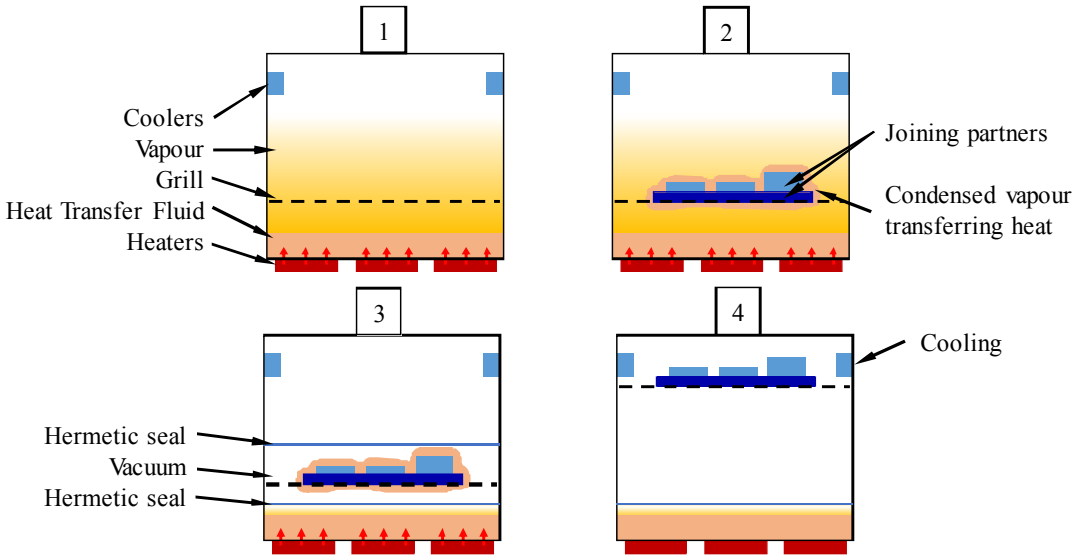


Figure 2.3: Schematic of VPS equipment

Historically, due to the presence of chlorofluorocarbons (CFCs) in the fluids used in the VPS soldering process, there were major restrictions placed on the technology [LT08]. However, since the development of new process materials which are classified as chemically inert and possessing zero ozone depletion potential [Géc14], VPS has found a resurgence, especially in the applications with high thermal mass joining partners (such as in Power Electronics).

As with any other soldering process, the presence of voids and improper cool-down to room temperature results in the reduction of bonding strength of the solder joint. As a consequence, similar to other industrial soldering processes modern VPS equipment comprises vacuuming capabilities during the soldering step and the possibility for controlled cooling to room temperature. In this work, components are soldered using the VPS process due to the large thermal mass of the joining partners. In addition, vacuum soldering is used to reduce voids and integrated fans are used to aid cooling of the components to room temperature after soldering.

2.2 Material and component selection in this research work

2.2.1 Power substrate

As in the case of Printed Circuit Boards (PCB), the function of substrates in power electronics is to enable interconnections and build up circuits. However, in contrast to relatively low powered electrical circuits, power electronic applications offer a major challenge with respect to its current and voltage ratings. Depending on the application, power electronic substrates need to withstand extremely high electrical currents and voltages [BE07; Mat17].

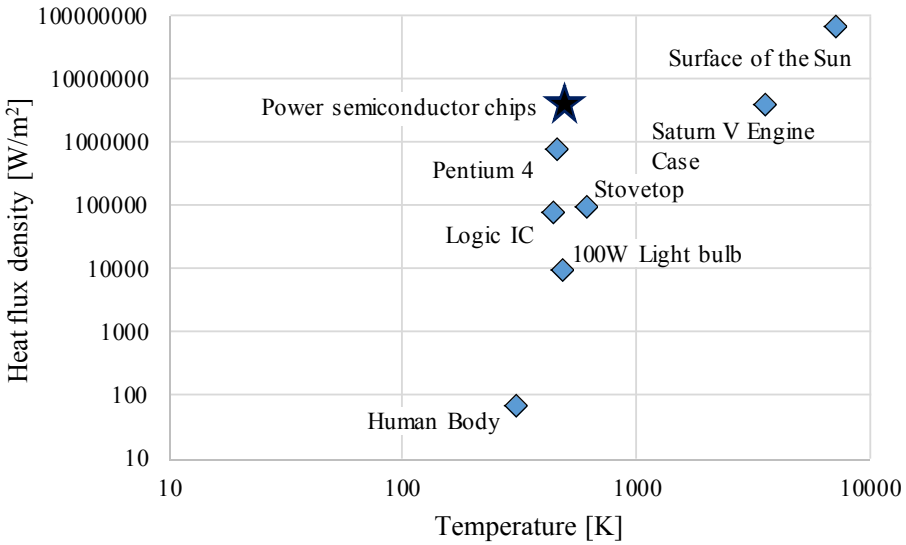


Figure 2.4: Heat flux density for different heat sources (inspired by Dr. W. Tursky, Semikron) [Lut+11]

With regard to heat generation, Figure 2.4 according to [Lut+11] shows the relative positioning of power electronics semiconductor chips among various heat sources. It can be deduced that heat flux values on semiconductor devices may reach in excess of 7 MW/m^2. Additionally, junction temperatures can exceed 175 °C. This means power semiconductor chips combine high temperature with high heat flux density. Thermal management is therefore, of major importance during operational conditions and is one of the decisive factors influencing the choice of an appropriate substrate. Of the many kinds of substrates available, two major kinds of substrates that meet the above explained prerequisites. They are the Direct Bonded Copper (DBC) and Active Metal Brazing (AMB) substrates. Both these substrates have essentially the same physical structure on the macro scale. Figure 2.5 depicts a schematic of the substrate structure. The thickness of the copper and the ceramic layers in these substrates are usually in the range of 200 µm to 800 µm.

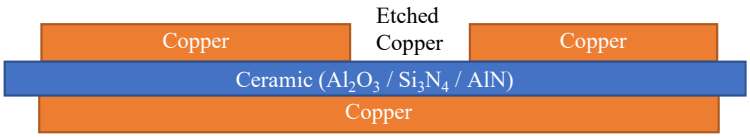


Figure 2.5: Schematic structure of a power substrate

Direct Bonded Copper (DBC)
DBC process uses a conductive copper foil and a ceramic insulator, which is bonded without the use of an additional joining material – thereby the name *Direct Bonded*. The typical manufacturing process begins with a ceramic sheet made of Alumina (Al_2O_3) or Aluminium Nitride (AlN) onto which, a copper sheet is placed which is chemically treated previously to have a thin layer of copper oxide on the surface to be bonded. This assembly is then heated to a temperature of 1065 °C (eutectic temperature of the Cu - O system) in an atmosphere where the amount of oxygen can be carefully controlled. This leads to the formation a strong bond made up of copper and alumina. The corresponding reactions representing this process according to [BE07; Gai19] are as follows.

Under low oxygen partial pressure:

$$\begin{aligned} 4\,Cu + O_2 &\longrightarrow 2\,Cu_2O \\ Cu_2O + Al_2O_3 &\longrightarrow 2\,CuAlO_2 \end{aligned}$$

Under high oxygen partial pressure:

$$\begin{aligned} 2\,Cu + O_2 &\longrightarrow 2\,CuO \\ CuO + Al_2O_3 &\longrightarrow CuAl_2O_4 \end{aligned}$$

In case of substrates with AlN as the ceramic layer, an additional step is required where AlN is heated at about 1200 °C in an atmosphere of O_2 to convert the surface of AlN to Al_2O_3 as per the reaction below. Once the oxidation process is completed, the bonding process is continued as in the case of substrates with Alumina as the ceramic material.

$$4\,AlN + 3\,O_2 \longrightarrow 2\,Al_2O_3 + 2\,N_2$$

Activated Metal Brazing (AMB)
In contrast to the DBC process, AMB process uses an additional joining material, namely the braze alloy, to join the conductive copper foil and a ceramic insulator. According to [FI99; Ins18], active metal brazing is a process in which a so called 'active metal' is added to the braze alloy. The most well-established active metal brazes are based on the 72Ag-28Cu eutectic alloy, to which 1-5 wt% titanium is added as the active metal. The main function is to increase the wetting behaviour of the braze alloy onto the ceramic surface. The ceramic is wet by the formation of an intermetallic compound (IMC) layer which can then form a joint with the braze alloy. AMB process is much better suited for joining Silicon based ceramics such as Si_3N_4 than the DBC process. For example, in case of Si_3N_4, according to [PK95], TiN and Ti_5Si_3 are the intermetallic phases found in the adhesive layer which are formed according to the reaction given below.

$$9\,Ti + Si_3N_4 \longrightarrow 4\,TiN + Ti_5Si_3$$

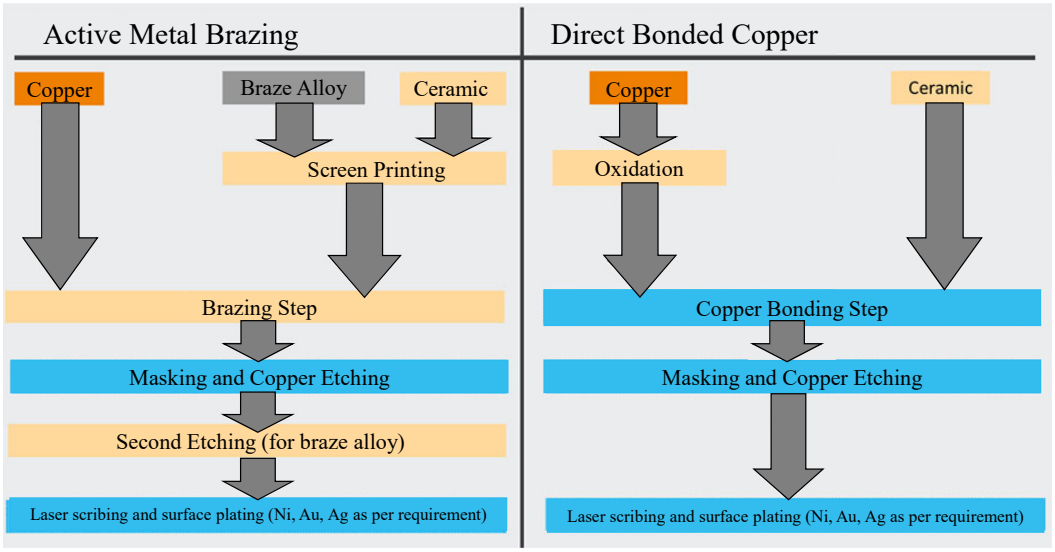


Figure 2.6: Comparison of AMB and DBC Manufacturing process (modified from [Uts+20])

For both substrate manufacturing processes, DBC and AMB, the required circuits are constructed by an etching process that removes copper. In case of AMB, an addition etching step is carried out to remove the IMC layer formed during the brazing step. A step by step comparison of the manufacturing process according to [VL13] is illustrated in Figure 2.6.

Also shown in Figure 2.7 are the reliability results of the manufacturing methods with various ceramic materials under passive temperature cycling. For a temperature swing of 205 °C, Si_3N_4 substrates manufactured using the DBC substrates showed a characteristic life of 2300 cycles while similar substrates manufactured using the AMB process withstood in excess of 5000. Investigations have shown [VL13] that substrates with Si_3N_4 ceramic using DBC and AMB bonding processes lasted longer by a factor of 20 and 50 respectively compared to conventional DBC ceramic materials such as Al_2O_3 or AlN.

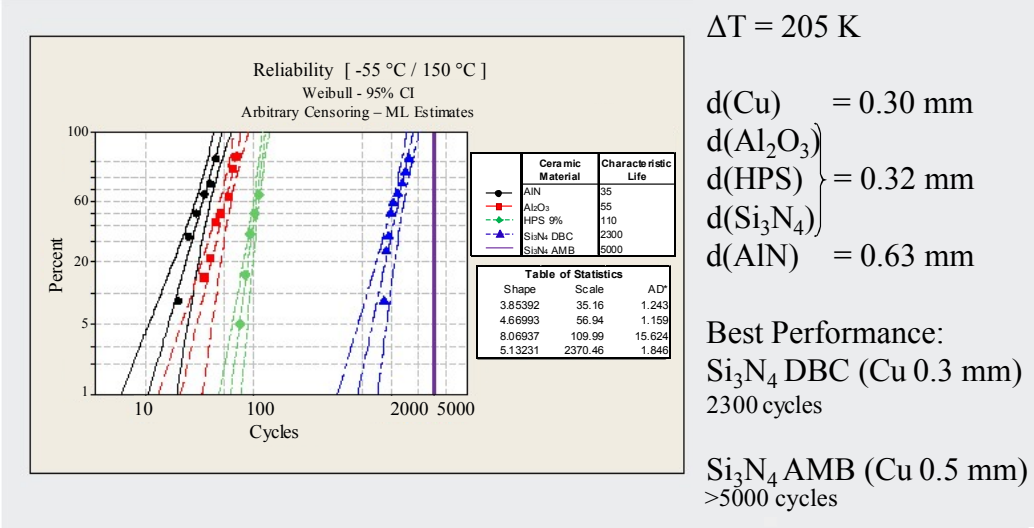


Figure 2.7: Reliability of power substrates with different substrate materials. [VL13]

Comparison of substrate material properties and manufacturing process selection

Due to the extreme conditions in which the above substrates operate, material properties play a very important role in the choice of the materials involved. Table 2.1 briefly summarizes the material properties of ceramics in the commonly available power substrates.

As can be clearly seen, Al_2O_3 offers relatively inferior material properties as compared to AlN and Si_3N_4. Considering the requirements of inverter units [Cur15] in hybrid/electric vehicles and that the temperature cycling reliability of substrates manufactured using the DBC process are also inferior to the AMB process, viable alternatives are the AMB substrates using AlN and Si_3N_4 ceramics. The major trade-off factors between AlN and Si_3N_4 substrates are the thermal conductivity and bending strength. Having said that, due to its higher bending strength, Si_3N_4 substrates can be utilized as thinner layers resulting in comparable thermal conductivity with AlN substrates. Also bearing in mind the prohibitive costs involved with AlN substrates, Si_3N_4 based AMB substrates are chosen for investigation in this research work.

Table 2.1: Material properties of ceramic materials used in power substrates [VL13]

	Al_2O_3	**AlN**	**Si_3N_4**
Thermal conductivity [W/mK]	24	180	90
Coefficient of thermal expansion [ppm]	6.8	4.7	3.4
Breakdown voltage [kV/mm]	20.0	33.6	46.4
Bending strength [MPa]	350	360	700

2.2.2 Heat sinks

The primary function of baseplates is to absorb the heat generated on the power substrate and transfer it to the coolant liquid. In addition to this, it also acts as the platform for mechanical fixation of power substrates. In this context, baseplates are required to have the following major properties

- High thermal conductivity
- Non reactivity with coolants/solvent
- Surface that is wettable by molten solder alloys

Oxygen free high conductivity copper continues to be very popular in commercial use [SC04] due to its high thermal conductivity (398 W/mK), non-reactivity, solder wettable surface and its easy large scale production and machinability.

Among other baseplate materials, Aluminium is also emerging as a contender due to it cost benefits as it is (at the time of writing this document) approximately 3 times cheaper than copper. It is also about 70 % less dense and therefore offers the advantage of light weight construction. It must be noted that Aluminium does not have a solder wettable surface and therefore cannot be soldered on directly. It needs to be made wettable using processes such as electrolytic or electroless nickel plating [Isl+03], gas sprayed copper coating [YM14; Woj+16],

ultrasonic pre-soldering [WHW07] etc. This adds both cost and reliability topics which need to be addressed at the design phase. Metal matrix composite baseplate materials are also found to have been used; although to a smaller extend. A popular material of this type is Aluminium/silicon carbide metal matrix composite or AlSiC. The main advantage of AlSiC is that the CTE of the material can be tailored to requirement based on the relative proportion of the aluminium matrix and the SiC particles [Occ+00]. The major disadvantages are the prohibitive costs, manufacturability and difficult machinability. This research work deals with copper baseplates due to their wide reaching scope and popularity.

2.2.3 Solder alloys as Thermal Interface Materials (TIMs)

Thermal Interface Materials (TIMs) are used in the layer connecting the power substrate and the baseplate. The most vital function of TIMs, is to transfer heat from the power substrate to the baseplate. The thermal conductivity and thickness of this layer therefore, can have a significant effect on the efficient cooling of the active electronic components mounted on the power substrate. Conventional TIMs include greases, gels, adhesives, elastomers, phase change materials etc. There are two major drawbacks to such TIM materials in power electronics applications. Firstly, the thermal performance of TIMs can show significant degradation under high temperature and large temperature swing temperature cycling tests [OK11; Sku+13]. Secondly, the thermal conductivities are usually limited to a maximum of 5 W/mK. According to [Ton11] the increased performance of semiconductor devices in the near future will render the presently known TIMs inadequate. In many power electronic applications, such as in inverter units dealt within this research work, the thermal properties of TIMs are already insufficient.

Due to the above mentioned deficiencies, the overarching trend for high temperature and high heat flux applications, is the replacement of non-metallic TIMs with solders. Considering the vast number of soldering alloys, a screening process is required. The first of such screening steps results from the Restriction of Hazardous Substances (RoHS) legislation of the European Parliament adopted in the year 2006 which rules out all solder alloys containing Lead [Eur11]. Depending on process and procurement based constraints five solder alloys were shortlisted. To further streamline the solder alloys, a sample test predating this doctoral work was carried out with regard to passive Temperature Cycling (pTC) reliability [BZ16a]. Test components were built using the above mentioned five solder alloys and put under a single chamber passive temperature cycling profile of -40 °C / 150 °C with 30 minute hold times at extremum temperatures.

A plot of normalized thermal impedance (Zth) values vs increasing pTC cycles is shown in Figure 2.8. Due to the steep increase in Zth values with pTC cycles, Solder alloy #5 is quite clearly ruled out. Innolot, solder #2 and #4 showed comparable Zth increase with solder #3 showing slightly higher increase in Zth. To decide between these solder alloys, a decision matrix analysis [BZ16c] was performed. The solders were scored and ranked based on criteria listed below.

- Process stability
- Reliability
- Melting temperature
- Cost
- Availability/Suppliers
- Cleaning after soldering
- Developmental effort
- Availability of solder as preforms

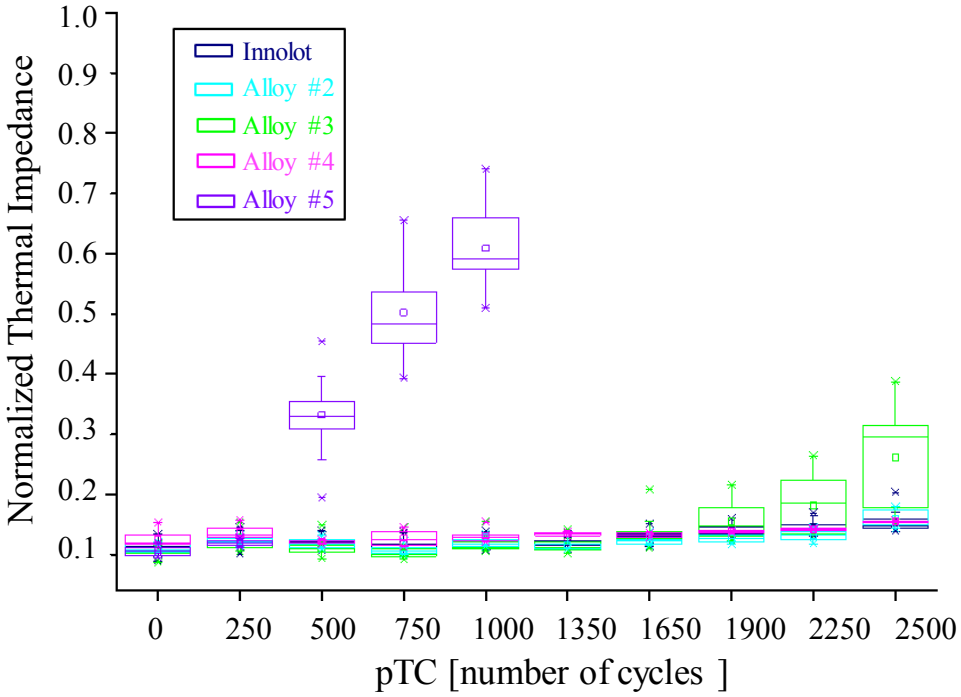


Figure 2.8: Zth increase with pTC test for different solder alloys

Based on these criteria, Innolot was chosen as the primary solder of choice for this study. Detailed version of the decision matrix is provided in Appendix (A) for reference.

2.3 Reliability assessment of solder joints

2.3.1 Brief introduction

In a typical IGBT based motor drive, some of the total controlled power will be dissipated as heat. According to [He+98], it is about 4%. In the automotive industry, many new generation Power Electronic (PE) modules operate on junction temperatures that may exceed 175 °C. It can be thus inferred that PE modules today operate under increasingly severe temperature conditions, influenced both by ambient and service conditions. In addition to this, there are cases were product service life guarantees of up to even 30 years are provided [Wan+14]. As a result, reliability engineering has evolved as a major branch during the design and development phases of PE devices. Due to the increasing thermal load as mentioned before, thermomechanical reliability assessment and lifetime prediction is becoming ever more important.

2.3.2 Reliability assessment in power electronics

[Cia02] provides an excellent overview of major failure mechanism within interconnects of power conversion devices such as inverters. Some of the major failure mechanisms are listed below.

1. Bond wire lift off
2. Bond wire heel cracking
3. Degradation of chip metallisation
4. Brittle cracking of chips and/or its insulating layers and ceramic substrates
5. Degradation of the solder alloy layers

Corresponding to the point *Degradation of the solder alloy layers*, two such critical solder layers can be identified in PE modules:

1. Solder layer connecting the chips (IGBTs, MOSFETs etc.) to the power substrate, *viz.* chip solder
2. Solder layer connecting the power substrate to the baseplate, *viz.* baseplate solder

The scope of this research work is the investigation of degradation of the solder layer connecting the power substrate to the baseplate.

2.3.3 Solder degradation

The solder layer connects various components that could have dissimilar CTEs. The focus of this research work, baseplate solder, connects the power substrate and the baseplate. Depending on the materials used, the CTE mismatch between the baseplate and the power substrate could be as high as 17 ppm per Kelvin. During service life, due to ambient temperature changes and self-heating during operation, PE components can experience large temperature swings. Even in the case of qualification/testing standards for low power microelectronic devices such as in [JED07; AEC14], peak temperatures of 150 °C and temperature swings of more than 200 °C are not uncommon.

Under such temperature conditions, thermomechanical forces that the solder layer must carry frequently exceed the yield strength of material. This results in so called *Low Cycle Fatigue* (LCF). In LCF, thermomechanical fatigue degradation in solder joints initiate due to large scale plastic deformations. This effect was shown for leaded solder joints by [Sat+91]. [Att+92] extended the above work to lead free solder alloys. It was noted that damage occurred not only due to plastic deformation resulting from thermomechanical loading, but also due to creep - a conclusion based on fractographic forensics which showed the presence of creep voids and fatigue striations side by side.

Creep is essentially time/rate dependant plastic deformation (viscoplasticity) occurring often below the classical yield strength of a material. It is strongly influenced by homologous temperature T_{hom} which is defined as in Equation (2.1).

$$T_{hom} = \frac{T_{mat}}{T_{melt}} \tag{2.1}$$

where T_{mat} is the temperature of a material and T_{melt}, its melting point (both temperatures in Kelvin). Higher the temperature, higher is the creeping effect. It is generally known that creep phenomena are active above a homologous temperature of 0.4 [Now+16]. Commonly used solders (leaded and lead free) have a melting temperature of approximately 180 °C to 260 °C. The temperature corresponding to a homologous temperature of 0.4 for these solder alloys is therefore -90 °C to -60 °C. This means, creep effects are present in solder joints practically at all times during service life. Consequently, in addition to conventional plastic deformation due to excessive mechanical loading, creep is also an important concern for solder joint reliability.

In addition to the above mentioned mechanisms, according to [Lec+09], interfaces between the IMC and bulk solder are prime locations for crack initiation and propagation. This is because of the fact that compared to the bulk solder, IMCs are hard and brittle materials. It has a complex crystalline microstructure with only few planes for the movement of dislocations. As a result, they provide very minimal stress relief under applied stress and transfer the stress to the adjoining solder layer. Therefore, the interface between IMC and solder results in an ideal location for delamination type crack growth especially under tensile loads.

Under the effect of the above mentioned mechanisms, the solder layer connecting the substrate to the baseplate develops cracks as shown in Figure 2.9. Such cracks result in an increase of thermal resistance (R_{th}) between the substrate and the cooling baseplate. The relationship between crack growth and increasing thermal resistance was clearly mentioned in [HM13; Lut+11]. The increased thermal resistance in turn reduces the critical capability of the solder joint to efficiently transfer heat generated in the chip which causes a runaway heating effect and subsequently leads to device failure [Lee93; OB79; Pec+97].

As can be clearly inferred, the lifetime of the baseplate solder joint has a direct effect on the overall reliability of the inverter. As a consequence, it becomes of utmost interest to develop a lifetime model that can describe the pTC reliability of the solder joint. The following section reviews the various methods employed in the past to describe the failure mechanism and predict lifetime of solder joints under thermal cycling.

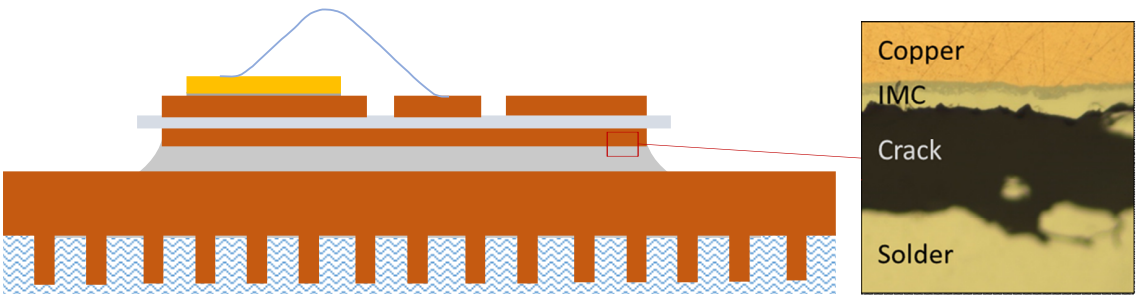


Figure 2.9: Crack in solder layer under passive temperature cycling [Geo+17]

2.3.4 Review of lifetime prediction models of solder joints

Historically, reliability engineering can be traced back to post second world war period. The IEEE Reliability Society was established in 1949 (then Professional Group on Quality Control) followed by Advisory Group on the Reliability of Electronic Equipment in 1950 established by the United States Department of Defence [Rel57]. These focus groups primarily attempted to improve the reliability of vacuum tubes used in radar systems and other electronics. Since then reliability evaluation of micro and macro electronic components has developed into a branch of its own.

According to [XWJ08], reliability is the probability that a component, equipment, or system will perform the required function under different operating conditions encountered for a stated period of time. In electronics reliability literature e.g. [LB17], it is commonly found that the reliability of electronic components strongly exhibits the bathtub curve trend. A bathtub curve as shown in Figure 2.10 has three major sections. First is the infant mortality or early failure regime that are caused due to latent defects in the device. In this regime the failure rate decreases relatively quickly as the latent causes for failure such as handling and installation faults are quickly identified and resolved. This section is followed by the constant failure rate regime where failure rate is low and constant. Following this, the wear out failure regime is encountered where the failure rate increases due to general wear and tear and material degradation.

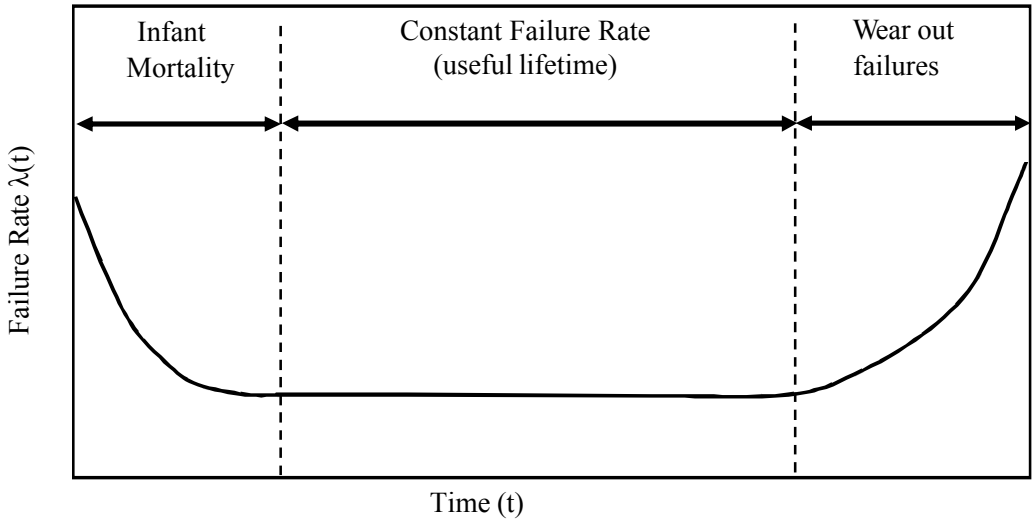


Figure 2.10: Bathtub curve in reliability engineering [Neu04]

Lifetime models seek to describe this wear out region based on MTTF (Mean Time To Failure) or EoL (End of Life) values obtained from accelerated reliability testing. One of the most well established accelerated reliability testing methodologies is the passive temperature cyclic (pTC) method. In a passive temperature cycling test, samples are placed in a temperature and humidity controlled chamber and subjected to cyclic thermal loading as shown in Figure 2.11.

Damage can be induced into the solder layer by adjusting the pTC profile (Figure 2.11) by changing temperatures T_{max}, T_{min}, ΔT, dwell time at extremum temperatures and the temperature gradient during the temperature ramp phases. To qualify components under

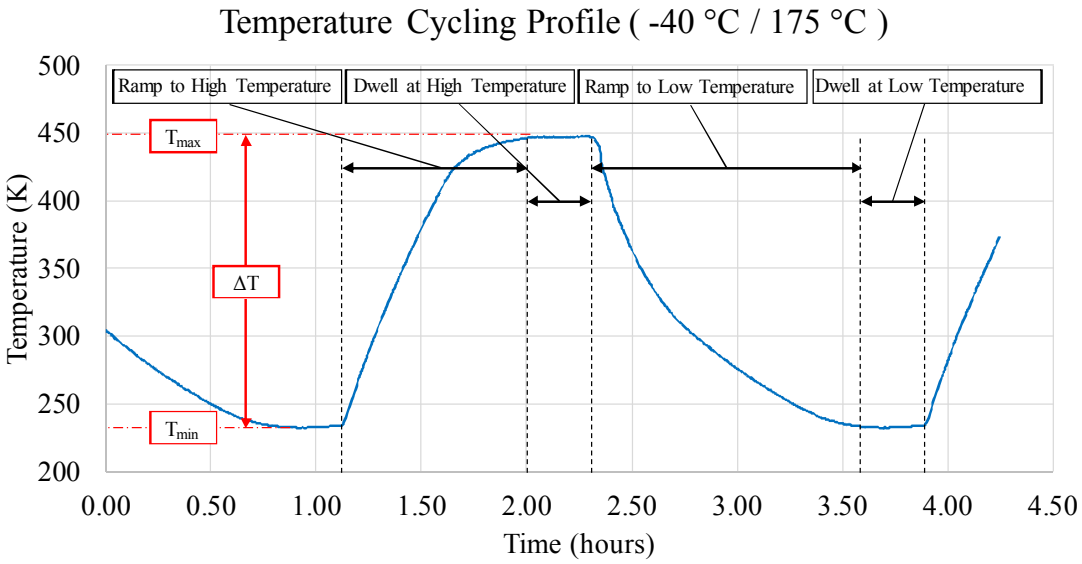


Figure 2.11: Passive temperature cycling

cyclic thermomechanical loading, various accelerated thermal ageing standards such as ones by [JED07], [JED14] or [AEC14] are available. Such accelerated tests induce damage into the solder much faster as the temperature conditions imposed in these tests are usually much harsher that what the devices actually experience.

The reliability data thus collected by experimental testing to obtain EoL or MTTF are used to derive a lifetime model with which service/experimental life can be predicted for new designs. Two major philosophies exist within lifetime modelling, namely,

1. Empirical lifetime models
2. Physics-based lifetime models

2.3.4.1 Empirical models

Empirical models derive a correlation between cycles to failure in an experiment to the potential influence factors from an experiment (for example ΔT in pTC, electrical current density in electro-migration, vibrational frequency in vibration test etc.) or sample conditions (for example, solder joint material properties, wire diameter, solder fillet meniscus etc).

One of the first empirical model used was based on activation energy as proposed by Svante Arrhenius in 1889 [Arr89a; Arr89b] based on the fact that reaction mechanism generally speed up with increasing temperature. The concept can be generalized also to thermally or thermomechanically induced failure mechanism.

$$N_f = Ae^{\frac{E_a}{k.T_m}} \tag{2.2}$$

where N_f is the number of cycles to failure, A is a scaling factor, E_a is the activation energy required to trigger the failure mechanism, k is the Boltzmann constant and T_m is the mean

temperature during the temperature cycling test. Arrhenius form of lifetime model has been used as a basis for many predictive equations. One such well known application was Black's equation [Bla69] used to describe failures due to electro-migration which is of the form

$$MTTF = \frac{A}{j^n} e^{\frac{E_a}{k.T_m}} \tag{2.3}$$

where, j is the current density and n is a fitting exponent. While useful, the Arrhenius model had the obvious disadvantage of not being able to represent the temperature swing ΔT during the temperature cycling experiments which were already known to accelerate failure in solder joints to a great extent.

The resolution to this came from the model inspired by the work of L. F. Coffin [Cof54] and S. S. Manson [Man53]. Coffin and Manson independently proposed a low cycle fatigue life equation for ductile metals as below as shown in Equation (2.4)

$$\frac{\Delta\varepsilon_{pl}}{2} = \varepsilon'_f (2N_f)^c \tag{2.4}$$

where $\frac{\Delta\varepsilon_{pl}}{2}$ is the plastic strain amplitude, $2N$ is the number of reversals to failure (N_f cycles) c and ε'_f are experimental fitting parameters. With the assumption that the plastic strain is induced proportional to change in temperature swing during a temperature cycle, Equation (2.4) can be modified and rewritten as shown in equation (2.5).

$$N_f = C_1 (\Delta T)^{C_2} \tag{2.5}$$

Equation (2.5) has been one of the most popular lifetime models in solder joint fatigue due to its simplicity and utility. However, this model too has its limitations. Firstly, it assumes that plastic strain in the solder material corresponds only to the temperature swing and therefore neglects the fact that at higher temperatures the phenomenon of solder creep is higher (temperature dependant plasticity). As a result, samples cycled under TC profiles with the same ΔT but different T_{max} will, in most cases, have different N_f. This effect cannot be described by the Coffin-Manson model. Another limitation the Coffin-Manson model as in equation (2.5) has, is that it assumes constant CTE at different temperatures which is also an assumption that in many cases is not justifiable. An attempt to resolve these assumptions is by adding an Arrhenius term to equation (2.5) to provide some form of maximum (or equivalently mean) temperature dependence. This equation as is called the Coffin-Manson-Arrhenius model as shown in Equation (2.6).

$$N_f = C_1 (\Delta T)^{C_2} . e^{\frac{E_a}{k.T_m}} \tag{2.6}$$

An alternate way for lifetime prediction is via the accelerations factor AF which is the ratio between life of a component under field conditions N_{field} to that under test conditions N_{test} defined as in Equation (2.7).

$$AF = \frac{N_{field}}{N_{test}} \tag{2.7}$$

As per Equation (2.7), if the acceleration factor is known, depending on the number of thermal cycles a given solder joint can withstand in a test, cycles to failure in the field can

be calculated. Norris and Landzberg in 1969 ([NL69]), provided an empirical formula for AF that included terms to account for thermal cycling frequency (f) and the maximum temperature(T_{max}) which previously discussed models did not. This formula is shown in Equation (2.8).

$$AF = \left(\frac{f_{field}}{f_{test}}\right)^{-m} \left(\frac{\Delta T_{field}}{\Delta T_{test}}\right)^{-n} \left[e^{\frac{E_a}{k}\left(\frac{1}{T_{max,field}} - \frac{1}{T_{max,test}}\right)}\right] \tag{2.8}$$

Norris and Landzberg determined that for SnPb eutectic solder joints, the free parameters m, n and $\frac{E_a}{k}$ had values 0.33, 1.9 and 1414 respectively. A study on SAC solder alloy by [Pan+05] based on sample including ceramic Ball Grid Array (CBGA) components, Chip Scale Packages (CSP), and Thin Small-Outline Packages (TSOP), m, n and $\frac{E_a}{k}$ were found to be 0.136, 2.65 and 2185 respectively. A more extensive study however, by [VF08] showed that the free parameters had the same values for SAC as for SnPb eutectic solder.

Through a series of papers in the early 1980s [Eng82; Eng83; Eng85], Engelmaier provided a semi-empirical lifetime model for solder joint life under temperature cycling in leadless ceramic chip carriers based on the amplitude of cyclic shear strain range. The model is described as per Equation (2.9).

$$\begin{aligned} N_f &= \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon'_f}\right)^{\frac{1}{c}} \\ c &= -0.442 - (6\times10^{-4})T_{mean} + (1.74\times10^{-2})\ln(1+f) \\ \Delta\gamma &= \frac{L}{\sqrt{2}h}\Delta(\alpha\Delta T)_{SS}\times10^{-6} \\ \Delta(\alpha\Delta T)_{SS} &= (\alpha_C - \alpha_S)(T_C - T_O) \end{aligned} \tag{2.9}$$

In the above equations grouped under equation (2.9), ε'_f is the fatigue ductility coefficient, c is the is the fatigue ductility exponent, T_{mean} is the mean cyclic solder joint temperature , f is the cycle frequency ($1 \leq f \leq 1000$ cycles/day), $\Delta\gamma$ is the cyclic shear strain range in a corner solder joint of height h at a distance of L from the neutral point (point of zero strain). $\Delta(\alpha\Delta T)_{SS}$ is the steady state mismatch in thermal strain determined by α_C and α_S which are the CTE values for the component and substrate respectively, T_C, is the steady state operating temperatures for the component and T_O is the power off, steady-state temperature.

As mentioned earlier, empirical models establish simple relationships between the test conditions and experimental life. In this sense, they are relatively easy to derive and is one of the reasons for their popularity. However, such models do not accurately describe the actual physics leading to failure. This is also their greatest weakness. As a consequence, empirical models are applicable to a narrow range of influence parameters and predictions from empirical models that involve extrapolation beyond the experimentally validated range of influence parameters are not trusted. Another issue with the empirical models is it inability

to account for geometric variation. For example, the fitting parameters for AF derived from the Norris-Landzberg model for the same solder alloy will be different for a BGA (Ball Grid Array), QFN (Quad Flat No-Leads), THT (Through Hole Technology) or some other solder joint shape. This again limits their applicability. To overcome these hurdles, Physics based models were proposed to be used for reliability prediction.

2.3.4.2 Physics based models

Instead of external experimental loading conditions, physics based models aim to describe lifetime using internal material variables that induce damage. These variables, among many, majorly include material response variables such as stress, strain, energy etc. According to [LNS00] physics based models fall into three major categories with regard to solder joint reliability as listed below

1. Plastic strain based models
2. Creep strain based models
3. Energy based models

Plastic strain based models

The plastic strain based models have their origins in the works of Basquin [Bas10] that describes the Wöhler line for High Cycle Fatigue (HCF) life using Equation (2.10).

$$\frac{\Delta\sigma}{2} = \sigma'_f(2N_f)^c \tag{2.10}$$

$\frac{\Delta\sigma}{2}$ is the stress amplitude, $2N_f$ is the number of reversals to failure and c and σ'_f are experimental fitting parameters. HCF is nonetheless a completely elastic phenomenon. Solder joints usually fail in the Low Cycle Fatigue (LCF) regime due to plastic deformations and therefore the plastic strain version developed by Coffin and Manson (Equation (2.4)) is used as it assesses the lifetime of a solder joint based on the range of plastic strain in a stabilized stress-strain hysteresis per cycle. The equation proposed by Coffin-Manson (Equation (2.4)) can be written in the form similar to Equation (2.5), but without the assumption that the range plastic strain $\Delta\varepsilon_{pl}$ is linearly related to the temperature swing ΔT as shown in Equation (2.11).

$$N_f = C_1(\Delta\varepsilon_{pl})^{C_2} \tag{2.11}$$

[Sol86; PTS98] have also provided a similar relationship with plastic shear strain as the damage parameter as shown in Equation (2.12) in cases where shear stress is singularly the dominant cause of failure. In this equation N_f, is the number of cycles to failure, $\Delta\gamma_{pl}$ is the plastic shear strain range per cycle and α and K are fitting parameters.

$$\Delta\gamma_{pl} \cdot N_f^{\alpha} = K \tag{2.12}$$

Creep strain based models

As previously mentioned in Section 2.3.3, creep is a major damaging mechanism in solder joints, especially at elevated temperature. As a result, a number of lifetime models based on

creep strain have been proposed in the past. At the microstructural level, creep occurs due to either dislocation movement (*matrix creep*) or due to *grain boundary sliding*. The model be Knecht and Fox [KF91] describes lifetime in term of matrix creep where $\Delta\varepsilon_{mc}$ is the creep strain due to matrix creep, N_f is the number of cycles to failure and C is a fitting parameter.

$$N_f = \frac{C}{\Delta\varepsilon_{mc}} \tag{2.13}$$

Examples for the use of this model can be found in the study [PTS98]. Contribution due a further creep mechanism was accounted for in the study [Sye04] which estimated damage according to Equation (2.14) where ε_1 and ε_1 are creep strains accumulated due to different creep mechanisms. C_1 and C_2 are model fitting parameters.

$$N_f = [C_1\varepsilon_1 + C_2\varepsilon_2]^{-1} \tag{2.14}$$

Energy based models

According to [Das+92], energy is a well suited damage parameter for lifetime models because it is essentially a product of stress and strain and therefore contains information about both the damaging quantities. According to [AZP97; Lia+97], using an energy based approach, lifetime may be predicted using Equation (2.15) which has a similar form as the well know Coffin-Manson equation except that instead of plastic strain, strain energy is used as the damage parameter.

$$N_f = C_1(\Delta W)^{C_2} \tag{2.15}$$

In Equation (2.15), ΔW is the strain energy as calculated from a stabilized stress-strain hysteresis loop during a temperature cycle and C_1 and C_2 are fitting parameters.

A model with a different mathematical structure was provided by Darveaux [Dar+95; Dar97; Zha+03]. In this methodology, the cycles to crack initiation and cycles to failure were treated differently. Equation (2.16) below summarize the model.

$$\begin{aligned} N_0 &= C_1(\Delta W)^{C_2} \\ \frac{da}{dN} &= C_3(\Delta W)^{C_4} \\ N_f &= N_0 + \frac{A}{da/dN} \end{aligned} \tag{2.16}$$

In Equation (2.16), N_0 is the cycles to crack initiation (often defined as crack <200 μm), $\frac{da}{dN}$ is the rate of crack growth, A is the total allowable crack length and N_f, as before, is the total number of cycles to failure. Syed [Sye04] also provided an energy based version of Equation (2.14) where accumulated creep strain is replaced by creep energy density.

Other models

Apart from the models described above, there are many other models proposed for the prediction of solder joint lifetime. For the sake of brevity, some of the notable models are named and cited without discussing the equations involved in detail.

One of the early works in Damage mechanics based lifetime prediction was carried out by [SMK98]. Fracture mechanics based lifetime prediction methodology is shown by [JSP96]

using the Paris-Erdogan law for crack growth [PE63]. Similar procedures are available with damage parameters like the J-integral and crack tip opening displacement (CTOD) - both based in Fracture mechanics. With the evolution of computing capabilities in the field of extended FEM (XFEM), more non-classical approaches to lifetime prediction have also been in use. For example, one of these that is popular and has found application in solder joint lifetime prediction is the Cohesive Zone model ([KR15]).

All the models discussed above involve the estimation of lifetime using some form of internal damage parameter dependent on the response of the material under load. Due to the complexity involved in device functionality, construction, manufacturing processes, operating conditions and material responses, it is often practically impossible to estimate the physical parameters used to evaluate damage and predict lifetime with analytical methods. With the development of the Finite Element Method (FEM) and large scale computational capabilities however, it has become possible to estimate these physical *Damage Parameters* with a high degree of accuracy. The following sections provide an overview of FEM and the mathematical equations describing material behaviour as used in the FEM models in this research work.

2.4 Brief introduction to Finite Element Method (FEM)

FEM is a numerical approximation method for solving Initial and Boundary value problems (IVP and BVP respectively) for partial differential equations. FEM when applied to physical problems such as analysis of new designs is called Finite Element Analysis (FEA). FEA has become exceedingly important as it leads to significant saving in costs, both monetary and temporal. Using FEA, one can build and analyse virtual prototypes of actual systems thereby helping in identification or elimination of detrimental engineering issues early in the product development cycle [Kha13]. Figure 2.12 summarizes the flow of work in an FEA project. FEA in today's scenario is carried out on powerful computers through FEA software, enabling simulations of ever increasing complexity. The simulations in this study are carried out on ANSYS® Workbench 18.2.

In general FEM involves the following steps

Preprocessing: Preprocessing involves the development of an FEM model. In this step, a 1D, 2D or 3D Computer Aided Design (CAD) model is developed. Non-essential entities which do not affect the physics of the problem involved are removed so as to keep the model as efficient (small) as possible without compromising on the quality of the solution. This is called Idealization. Idealization can also involve modelling only one particular quadrant or a section when planar or axial symmetry is present. This is followed by the Discretization step where subdivision of the problem domain into *finite elements* is carried out. To the discretized model, material properties, external or internal loads and boundary conditions (BCs) are applied.

Solving/Numerical analysis: In the Finite element procedure, solutions are carried out by solving matrix equations. Each element has its own matrix of equations (element stiffness matrix) describing its physical behaviour. Depending on the geometry i.e. the relative positions of element in the structure to be analysed, these element stiffness matrices are assembled into what is called the global stiffness matrix which then describes the behaviour of the complete model. Manual calculation (only practical for small problems) or FEA software

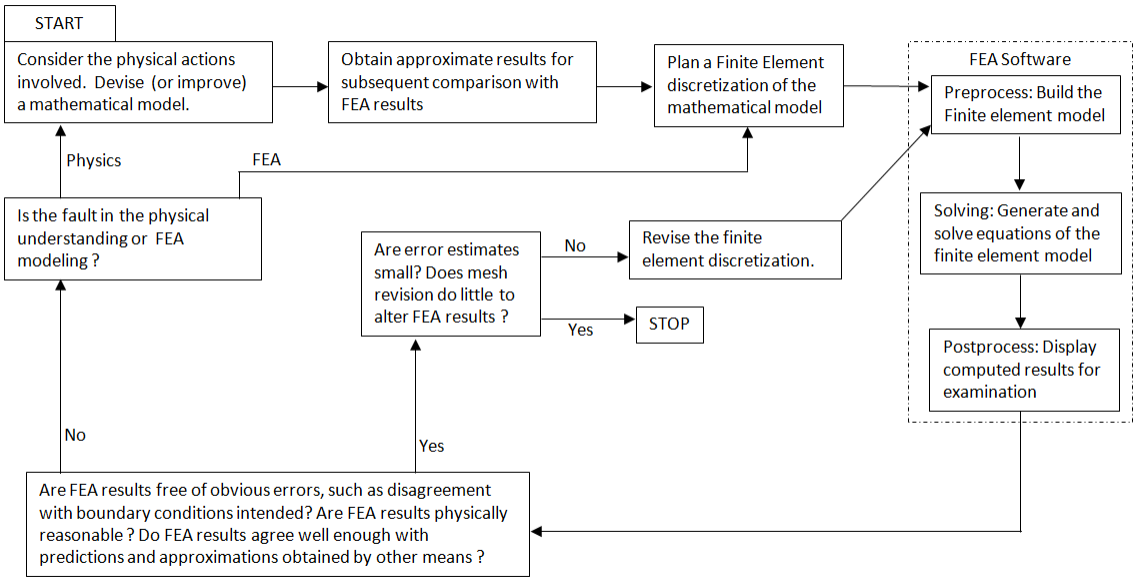


Figure 2.12: Workflow of Finite Element Analysis (FEA) [Coo+07]

solve these matrix equations using a variety of possible equation solving algorithms to obtain values for *field quantities*. Field quantities vary depending on the physics of the problem involved and can be, for example, displacement, temperature etc.

Postprocessing: This step involves the interpretation of results of the solved model. These can be viewed in the form of lists, graphs, contours and animations. The analyst must check results for consistency with actual problem at hand. This implies cross-checking boundary conditions, noting if computed field variables match expected behaviour, checking mesh size dependence and convergence behaviour during solution etc. Postprocessing can also involve manipulation of results obtained from the solution step to suit specific needs and obtain user defined results.

2.4.1 Minimum working example: 1D problem solved using FEM

This section provides a step by step working example that illustrates how FEM works on a basic level. For this purpose, we take a problem of a compound bar made of aluminium and copper with circular cross sections that is rigidly fixed at one end and subjected to a force on the other as shown in the Figure 2.13. The objective is to determine the elongation, strain and stress in the two materials.

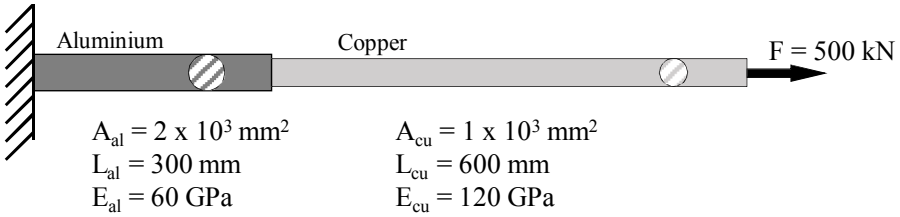


Figure 2.13: Compound bar problem

Description of the physics of the problem
Let us consider an arbitrarily bar that is constrained at one end and is subjected to an axial force F. From basic elastic material laws [Hoo16] we know that

$$E = \frac{\sigma}{\varepsilon} \qquad where, \tag{2.17a}$$

$$\sigma = \frac{F}{A} \qquad and \qquad \varepsilon = \frac{u}{L} \tag{2.17b}$$

E is the Young's modulus of elasticity, σ and ε are the stress and strain in the bar respectively. F is the applied force, A is the area of cross section of the bar, u is the elongation of the bar under force F and L is the original length of the bar. Using Equation (2.17b) in Equation (2.17a) and making F the subject of the equation, we get the relation

$$F = \left[\frac{AE}{L}\right] u \tag{2.18}$$

Equation (2.18), is identical in structure to Equation (2.19), which gives the extension of a linear spring under applied axial load.

$$F = ku \tag{2.19}$$

k is the stiffness of the spring. This means that the bar may be idealized as a spring with stiffness

$$k = \left[\frac{AE}{L}\right] \tag{2.20}$$

Discretization and element formulation
For the discretization step we split the geometry in Figure 2.13 into two bars as shown in Figure 2.14(a). Each of the bars can be represented as an arbitrary "*bar element*" as shown in Figure 2.14(b) with two nodes i and j and with a stiffness k as in Equation (2.20). We consider a case were at each node a force and corresponding displacements are present as in Figure 2.14(c). It can be shown that under equilibrium the following equations are true.

$$F_i = k(u_i - u_j) \tag{2.21a}$$

$$F_j = k(-u_i + u_j) \tag{2.21b}$$

Equation (2.21) can be represented in matrix form as

$$\begin{bmatrix} F_i \\ F_j \end{bmatrix} = \begin{bmatrix} k & -k \\ -k & k \end{bmatrix} \cdot \begin{bmatrix} u_i \\ u_j \end{bmatrix} \tag{2.22}$$

or

$$\{\mathbf{f_e}\} = [\mathbf{k_e}] \cdot \{\mathbf{u_e}\} \tag{2.23}$$

$\{\mathbf{f_e}\}$, $\{\mathbf{u_e}\}$ and $[\mathbf{k_e}]$ are the elemental forces, displacements and the stiffness matrix respectively. The idealized problem can be represented with two finite elements as shown in Figure 2.15 and the individual force balance equations can be written as Equations (2.24) and (2.25).

$$\begin{bmatrix} F_1 \\ F_2 \end{bmatrix} = \begin{bmatrix} k_1 & -k_1 \\ -k_1 & k_1 \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{2.24}$$

$$\begin{bmatrix} F_2 \\ F_3 \end{bmatrix} = \begin{bmatrix} k_2 & -k_2 \\ -k_2 & k_2 \end{bmatrix} \cdot \begin{bmatrix} u_2 \\ u_3 \end{bmatrix} \tag{2.25}$$

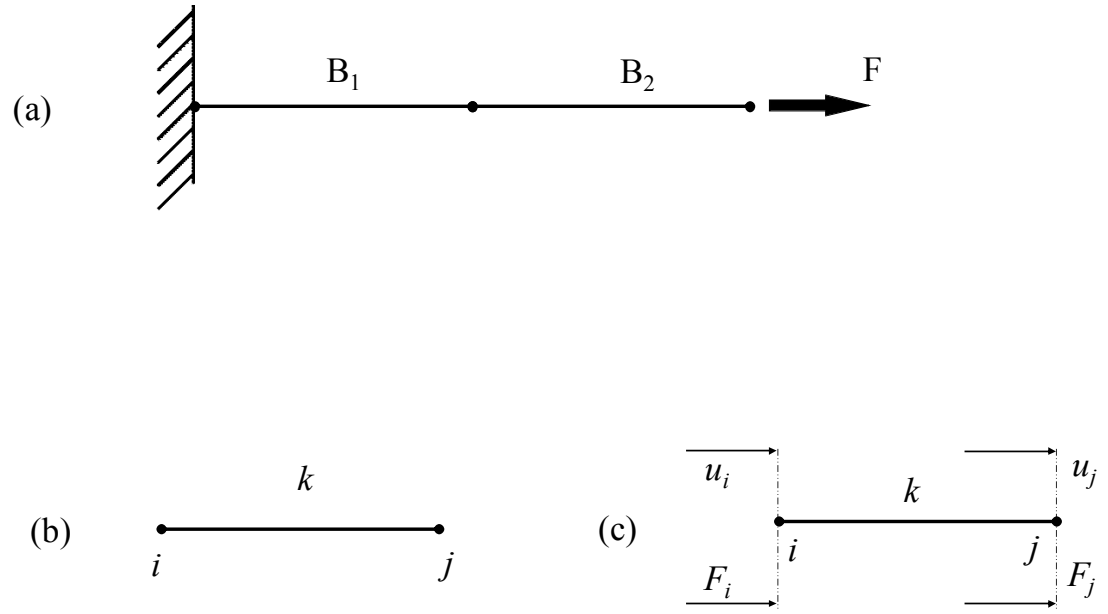


Figure 2.14: Element formulation

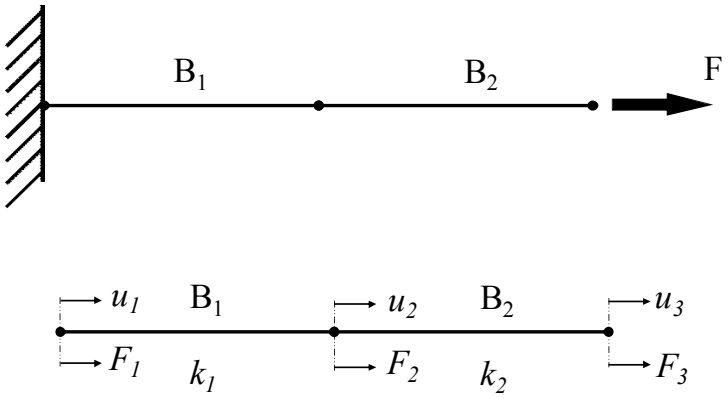


Figure 2.15: FEM equivalent of compound bar

As node 2 is shared between the two elements, the set of Equations (2.24) and (2.25) can be assembled in the form

$$\begin{bmatrix} F_1 \\ F_2 \\ F_3 \end{bmatrix} = \begin{bmatrix} k_1 & -k_1 & 0 \\ -k_1 & k_1 + k_2 & -k_2 \\ 0 & -k_2 & k_2 \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} \tag{2.26}$$

or

$$\{\mathbf{F}\} = [\mathbf{K}] \cdot \{\mathbf{U}\} \tag{2.27}$$

To solve for $\{\mathbf{U}\}$ we invert the *global stiffness matrix* $[\mathbf{K}]$, and multiply with the vector of forces $\{\mathbf{F}\}$.

$$\{\mathbf{U}\} = [\mathbf{K}]^{-1} \cdot \{\mathbf{F}\} \tag{2.28}$$

In Equation (2.28), we set $u_1 = 0$, $F_3 = 500$ kN and set internals forces (here $F_2 = 0$). Solving for u_2 and u_3 we get

$$u_2 = \frac{F_3}{k_1} \qquad u_3 = \frac{F_3}{k_1} + \frac{F_3}{k_2} \tag{2.29}$$

Strains can be calculated as

$$\varepsilon_{B1} = \frac{u_2 - u_1}{L_{B_1}} \qquad \varepsilon_{B2} = \frac{u_3 - u_2}{L_{B_2}} \tag{2.30}$$

and stresses may be calculated as

$$\sigma_{B1} = \varepsilon_{B1} E_{B_1} \qquad \sigma_{B2} = \varepsilon_{B2} E_{B_2} \tag{2.31}$$

The calculated values are tabulated in Table 2.2.

Table 2.2: Extension, strain and stress as calculated from hand calculated FEM method

-	**Extension**	**Strain**	**Stress**
Element B1	1.25 mm	0.00416	250 MPa
Element B2	2.50 mm	0.00416	500 MPa

For comparison, the identical problem is was also simulated using the FEM software ANSYS® using multiple 3D elements and corresponding results are shown in Figure 2.16. As can be seen, the results from the hand calculation and the software are practically identical.

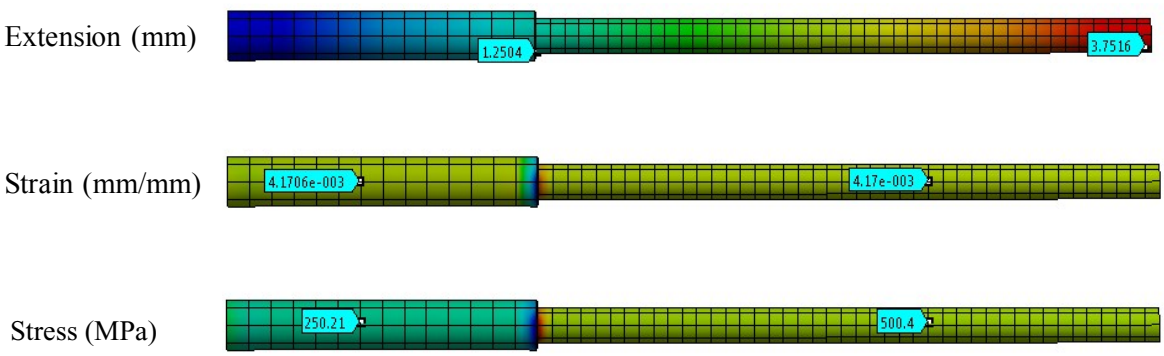


Figure 2.16: Extension, strain and stress in the two bars as calculated from ANSYS®

The minor difference can be attributed to where the stresses are read out and the specific formulation of the problem in the hand calculation method and the more versatile FEM method employed in commercial FEM software. In the discussed problem, the displacement of the bar under a given load was analytically known exactly; which is why the hand calculation uses a so called *strong form formulation* of the problem wherein force balance condition is enforced at each point in the body. For many problems however, an exact analytical solution is not available and approximate solutions are found using a *weak form formulation* of the problem where force balance conditions are enforced in an integral sense. In other words, the displacement vector is so determined that the total energy of the system is minimized.

2.5 Material behaviour: Elasticity and Plasticity

All constrained bodies under the application of an external force undergo deformation. The simplest type of deformation is elastic deformation. Elastic deformation is reversible, *i.e.*, once the external force is removed, the body returns to its original shape. This was first formalised by Robert Hooke [Hoo16] which is today called Hooke's Law which relates stress σ and strain ε, through the modulus of elasticity (also called Young's modulus) E as shown in Equation (2.32).

$$\sigma = E\varepsilon \tag{2.32}$$

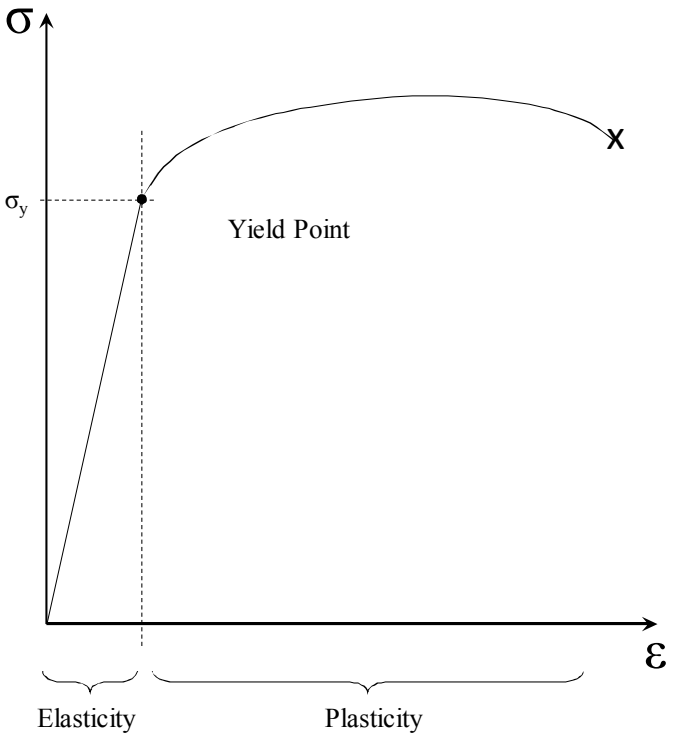


Figure 2.17: Stress-Strain curve (modified from [BN08])

As can be seen in Equation (2.32) and Figure 2.17, stress and strain share a linear relationship. However, this is true only up to a certain point in the stress-strain curve called the yield point. When the stresses are below the yield point, it is said to be in the elastic domain.

Beyond this point the material enters the domain of plasticity, *i.e.*, once the external force is removed, the body does not return to its original shape and consequently results in permanent deformation. In addition to this, typically in the plastic regime, large deformations occur with a relatively small increase in stress.

The total strain (ε^{tot}) can always be expressed in term of an additive decomposition of the elastic (ε^{el}) and plastic (ε^{pl}) part as shown in Equation (2.33).

$$\varepsilon^{tot} = \varepsilon^{el} + \varepsilon^{pl} \tag{2.33}$$

Equation (2.32) and Figure 2.17 show a simplified one dimensional case. In reality, forces and geometries are three dimensional which therefore result in stress and strain with normal and shear components that are represented as a tensor (Equation (2.34)).

$$\boldsymbol{\sigma} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix} \quad , \quad \boldsymbol{\varepsilon} = \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon_{33} \end{bmatrix} \tag{2.34}$$

The principal diagonal entries in the matrix represent the normal stress components while the other entries represent shear stress components. Due to this multidimensional structure of stress in a loaded body, it is useful to have an equivalent scalar value of stress derived from the stress tensor that tells whether the material has plastified or not by comparing it to the one dimensional yield strength. For this purpose, the concept of principal stress space and yield surface must be understood.

The stress tensor is a second order symmetric tensor. Through co-ordinate transformation, it is possible to orient it in such a way that only normal stress are present as shown in Equation (2.35).

$$\tilde{\boldsymbol{\sigma}} = \begin{bmatrix} \sigma_1 & 0 & 0 \\ 0 & \sigma_2 & 0 \\ 0 & 0 & \sigma_3 \end{bmatrix} \quad , \tag{2.35}$$

σ_1, σ_2 and σ_3 are called principal stresses (mathematically, eigen values of the stress tensor) and the corresponding co-ordinate system is called the principal stress space. From the principal stress values, the mean or hydrostatic stress can be computed as in Equation (2.36).

$$\sigma_h = \frac{\sigma_1 + \sigma_2 + \sigma_3}{3} \tag{2.36}$$

Following this, the so called deviatoric stress can be computed according to Equation (2.37) where $\mathbb{I}$ is the identity matrix (principal diagonal terms equal to 1 and others equal to 0).

$$\boldsymbol{\sigma}^{dev} = \boldsymbol{\sigma} - \mathbb{I}\sigma_h \tag{2.37}$$

Finally, the second invariant, J_2, is used to define the equivalent or von Mises stress, σ_{eqv} to determine if a material is yielding.

$$J_2 = \frac{1}{2}\,\boldsymbol{\sigma}^{dev} : \boldsymbol{\sigma}^{dev} \tag{2.38}$$

$$\sigma_{eqv} = \sqrt{3J_2} = \sqrt{\frac{3}{2}\,\boldsymbol{\sigma}^{dev} : \boldsymbol{\sigma}^{dev}} \tag{2.39}$$

In a monotonically loaded body, plasticity is considered to begin when σ_{eqv} equals the yield stress, σ_y, of the material as determined from a uniaxial tension test. Mathematically stated, the criterion for plasticity is as expressed in Equation (2.40) which is called the yield criterion. As this criterion for plasticity is based on the J_2 value, it is also called J_2 *Plasticity*. It is also commonly called von Mises plasticity.

$$f(\boldsymbol{\sigma}) = \sigma_{eqv} - \sigma_y = 0 \tag{2.40}$$

Consequently, in a three dimensional sense, stress states satisfying the Equation (2.40), form a surface called the yield surface. For the sake of understanding, von Mises yield surface can be visualised as a cylinder having radius of $\sqrt{\frac{2}{3}}\sigma_y$ and axis along the line σ_1=σ_2=σ_3 in the principal stress space. Just as the yield point σ_y, marked the distinction between elastic and plastic domains in a 1-D case, the yield surface marks the distinction between elastic and plastic domains in a 3-D case.

In the case where the material satisfies the condition for plasticity and is then further loaded, the plastic strain rate $\dot{\boldsymbol{\varepsilon}}^{pl}$ is expressed according to the *Flow Rule* as in Equation (2.41).

$$\dot{\boldsymbol{\varepsilon}}^{pl} = \dot{\lambda} \frac{\dfrac{\partial f}{\partial \boldsymbol{\sigma}}}{\left|\dfrac{\partial f}{\partial \boldsymbol{\sigma}}\right|} \tag{2.41}$$

where λ is the so called plastic multiplier needed to return the stress state back to the yield surface and f is the yield function. $\frac{\partial f}{\partial \boldsymbol{\sigma}} / \left|\frac{\partial f}{\partial \boldsymbol{\sigma}}\right|$ is the normal to the yield surface. It can be shown that

$$\frac{\dfrac{\partial f}{\partial \boldsymbol{\sigma}}}{\left|\dfrac{\partial f}{\partial \boldsymbol{\sigma}}\right|} = \frac{\boldsymbol{\sigma}^{dev}}{|\boldsymbol{\sigma}^{dev}|} = \boldsymbol{Q} \tag{2.42}$$

Consequently,

$$\dot{\boldsymbol{\varepsilon}}^{pl} = \dot{\lambda}\boldsymbol{Q} \tag{2.43}$$

where $\boldsymbol{Q}$ is a unit tensor normal to the yield surface. Similar to the equivalent stress, an equivalent plastic strain is also defined. In strain rate form, this definition is expressed as

$$\dot{\varepsilon}^{pl}_{eqv} = \sqrt{\frac{2}{3}\,\dot{\boldsymbol{\varepsilon}}^{pl} : \dot{\boldsymbol{\varepsilon}}^{pl}} = \sqrt{\frac{2}{3}}\,\dot{\lambda} \tag{2.44}$$

Under cyclic loading, such as in temperature cycling, evolution of plastic stresses and strains is an important topic - especially in L.C.F. This is discussed in the following section.

2.5.1 Cyclic plasticity

Until now, we have discussed monotonic loading, *i.e.* no reversals in loading conditions. Under temperature cycling the stress state is reversed from tensile to compressive within each TC. Under such cyclic loading, solder materials show so called *strain hardening* phenomena.

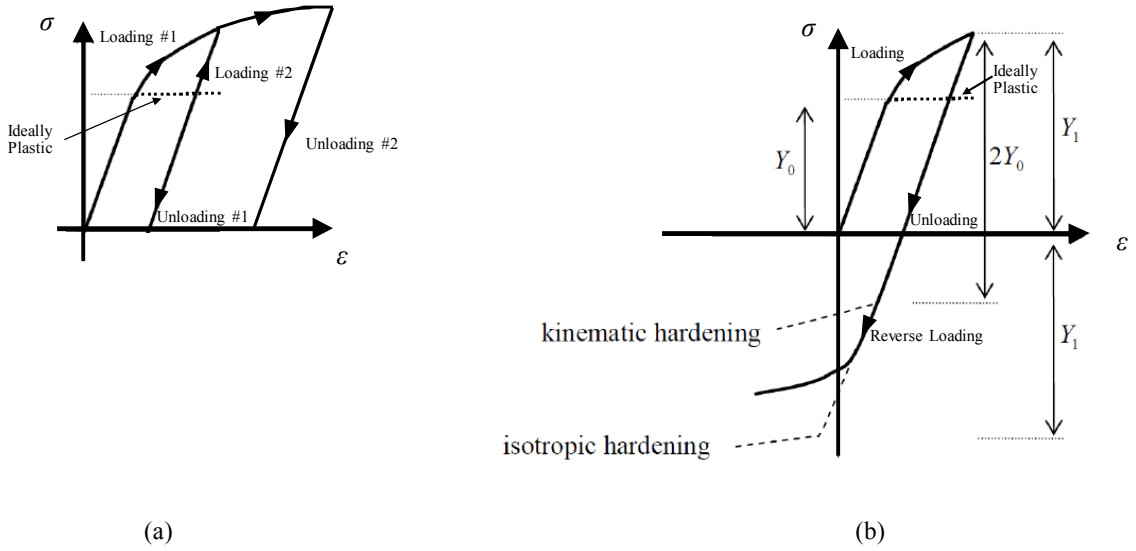


Figure 2.18: Two major strain hardening cases as seen in a 1D case. Modified from [Kel13]

In an ideally plastic case, the stress-strain curve would be flat (zero elastic modulus) after the yield point. However, as shown in Figure 2.18(a), most metals, including many solder alloys show a positive elastic modulus after the yield point. When the material is unloaded, the stress drops to zero following a straight line on the stress strain curve with a slope equal to the elastic modulus. Subsequently, if the material is loaded again from the zero stress state, the material first follows the unloading curve (straight line with elastic modulus as slope) until the most stressed point during the previous loading step is reached and then, follows the plasticity curve again. This means that due to the plastic strain excursion in the first loading step, the material behaved as an elastic material for higher value of stress during the second loading step. This effect is called strain hardening.

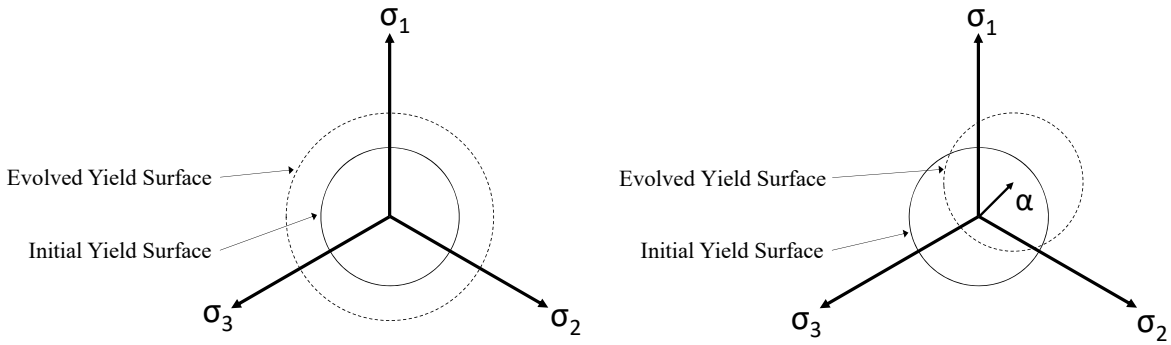
Under cyclic loading (load reversal) as shown in Figure 2.18(b) strain hardening is primarily of two types, namely, Isotropic and Kinematic. In the isotropic case, the hardening takes place symmetrically in both tensile and compressive directions. On the other hand, in the kinematic case, the increase in yield stress in one loading direction (say tensile) is compensated by the decrease in yield stress in the opposite loading direction. This effect is also called the Bauschinger effect.

In a three dimensional sense, isotropic hardening can be visualized in Figure 2.19(a). Here, the cylindrical yield surface grows as the radius of the cylinder uniformly increases with each hardening step. Mathematically, the yield criterion for isotropic hardening can be written as in Equation (2.45).

$$f(\boldsymbol{\sigma}) = \sigma_{eqv} - \sigma_y - H(\xi) = 0 \tag{2.45}$$

Here, σ_y is the initial yield strength of the material, $H(\xi)$ is a hardening function which has, for instance, ε^{pl}_{eqv} (equivalent plastic strain) or other material history state variables as input parameters. While this is an improvement on the perfectly plastic case, it still cannot represent real world phenomena such as the Bauschinger effect and thus limits its utility.

In the case of kinematic hardening, the yield surface translates during plastic flow and therefore enables the description of effects such as the Bauschinger effect [Die61]. This translation of



(a) Isotropic Hardening (b) Kinematic Hardening

Figure 2.19: Isotropic and kinematic hardening. Modified from [Inc16b]

the yield surface is defined using the back stress tensor $\boldsymbol{\alpha}$ as shown in Figure 2.19(b). The yield function for this is defined as in Equation (2.46). In the case where $H(\xi)$ is zero, it is a purely kinematic hardening model where the yield surface moves, but the size of the yield surface does not change. A non-zero $H(\xi)$ indicates a mixed kinematic hardening model where, in addition to the translation of the yield surface, its size can also change.

$$f(\boldsymbol{\sigma}, \boldsymbol{\alpha}) = \sqrt{\left(\frac{3}{2}(\boldsymbol{\sigma}^{dev} - \boldsymbol{\alpha}^{dev}) : (\boldsymbol{\sigma}^{dev} - \boldsymbol{\alpha}^{dev})\right)} - \sigma_y - H(\xi) = 0 \tag{2.46}$$

The evolution of the back stress tensor $\boldsymbol{\alpha}$ can be linearly related with plastic strain (Equation (2.47): Melan and Prager [Pra49]) or non-linearly with respect to plastic strain (Equation (2.48): Amstrong and Frederick [FA07]).

$$\dot{\boldsymbol{\alpha}} = \frac{2}{3}\boldsymbol{C}\dot{\boldsymbol{\varepsilon}}^{\boldsymbol{pl}} \tag{2.47}$$

$$\dot{\boldsymbol{\alpha}} = \frac{2}{3}\boldsymbol{C}\dot{\boldsymbol{\varepsilon}}^{\boldsymbol{pl}} - (\gamma \,.\, \dot{\varepsilon}^{pl}_{eqv})\boldsymbol{\alpha} \tag{2.48}$$

C and γ are material parameters and ε^{pl}_{eqv} is the equivalent plastic strain.

A non-linear evolution of the back stress tensor enables a good representation of non-linear effects such as Bauschinger effect, ratcheting [Bre67] and shakedown [Kön12] phenomena. The Armstrong-Frederick hardening law was further improved by Chaboche [Cha86]. According to the Chaboche model, the back stress tensor evolves as a superimposition of several non-linear Armstrong-Frederick kinematic models as shown in Equation (2.49).

$$\dot{\boldsymbol{\alpha}} = \sum_{i=0}^{n} \dot{\boldsymbol{\alpha}}_i = \sum_{i=0}^{n} \left[\frac{2}{3}\boldsymbol{C}_i\, \dot{\boldsymbol{\varepsilon}}^{\boldsymbol{pl}} - (\gamma_i \,.\, \dot{\varepsilon}^{pl}_{eqv})\boldsymbol{\alpha}_i\right] \tag{2.49}$$

where, n is the number of kinematic models superimposed. It can be noted that the Armstrong-Frederick hardening law can be interpreted as a special case of the Chaboche model with $n = 1$. In a graphical form the evolution of yield function in the plastic regime for a 1D case may be represented as in Figure 2.20.

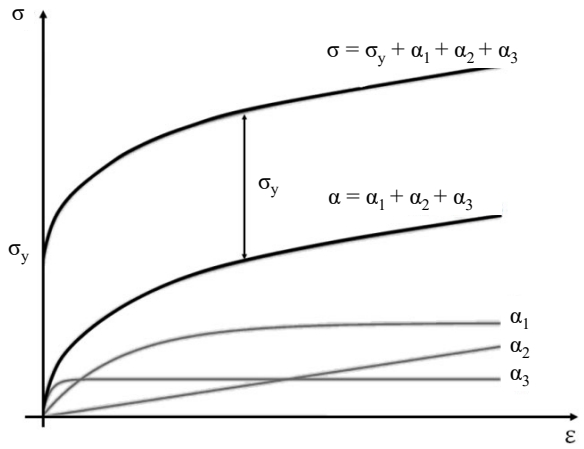


Figure 2.20: Evolution of yield function in the Chaboche model. Modified from [HSŠ12]

2.5.2 Material behaviour: Creep (Viscoplasticity)

Creep is the accumulation of inelastic strain under a constant load (possibly even below its conventional yield point) at elevated temperatures. It is strongly influenced by the homologous temperature (ref. Equation (2.1)) of the material in use. Creep phenomena is active in metals in cases where $T_{hom} > 0.4$ [Ber13]. Due to the high T_{hom} in the field of automotive electronics, solders are highly susceptible to creep.

The typical creep curve is shown in Figure 2.21 which shows three creep regimes. The first regime is Primary (I) creep where the creep rate ($d\varepsilon/dt$) is high but decreases with time. The Secondary (II) creep regime is characterised by constant creep rate and finally, the Tertiary (III) creep rate shows increasing creep rate eventually followed by rupture. The complementary phenomenon to creep is relaxation where the material is subjected to an instantaneous constant strain. The material responds to this strain loading by an instantaneous stress value that decays over time. Creep and relaxation are different manifestations of the same material behaviour, viscoplasticity which is the dependence of stress and strain response on time or the rate at which a load is applied.

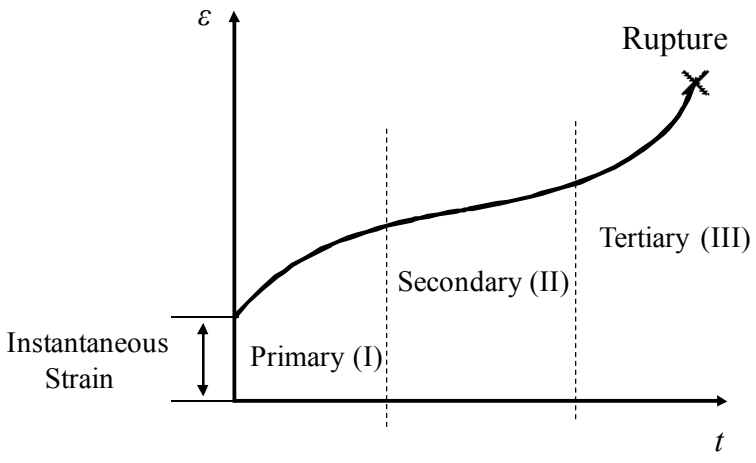


Figure 2.21: Typical creep curve. Modified from [CB09]

2.5.3 Solder material model in this research work

The solder material model used in this study is a unified creep-plasticity model. To account for strain hardening, the Chaboche non-linear kinematic hardening model was used which is calibrated from measurements at four different temperatures. To account for viscoplasticity, the so called exponential visco-hardening model is used. This is calibrated through measurements at four strain rates - also each at four different temperatures.

Material characterisation was carried out at the Fraunhofer Institute IKTS, Dresden in co-operation with Robert Bosch GmbH. The material characterisation for the alloy used predates this work and was based on the doctoral work [Mét19]. It was shown that using the above mentioned material model, effects such as creep, relaxation, strain rate dependence and cyclic plasticity can be satisfactorily calculated using FEM.

2.6 Novelties of this research work

- IMC thickness prediction for non-isothermal cases
- Effect of IMC thickness on reliability for large area solder joints
- Detailed investigation of package geometry on reliability
- Robust manufacturing process simulation for baseplate soldering
- FEM based lifetime model for baseplate solder layer

Science... is a fusion of man's aesthetic and intellectual functions devoted to the representations of nature and is therefore the highest form of creative art.

C. V. Raman (1888 – 1970)
Indian physicist

Chapter 3

Warpage of AMB Substrates and Baseplates

3.1 Introduction

In the field of microelectronics manufacturing and reliability, CTE plays a vital role because a large mismatch between CTEs of different assembled materials leads to shear deformation and consequently failures under thermomechanical loads. An additional effect arising from CTE mismatch is that of warpage which is also of key importance. According to [Lee+14], warpage plays an important role in many failure mechanisms. This can be attributed to the fact that warpage gives rise to residual thermal stresses after soldering [ZXL15], unequal solder joint thickness [Lee11] and crack opening loads during temperature cycling [CJB00; Rze+98].

A few specific results can be seen in the following studies. [HLS01] showed that localized warpage caused cracks in the silicon chips. In lead free BGA solder joints, a complex combination of shear and warpage was reported [Sil+13] to be a driving mechanism for brittle solder joint failure. Within the power electronics field, [Cia02] mentions that bending stress induced due to bi-metallic (or bi-material) warpage leads to cracks.

In power electronics applications such as inverter units, during the soldering process of power substrates to the baseplate and/or reliability test such as passive temperature cycling (pTC), warpage is observed, and all the above mentioned issues co-exist making it a major potential influence factor for thermomechanical reliability. Apart from reliability issues, warpage is also a concern during manufacturing process with regard to calculation of the correct amount of solder required for baseplate soldering or for chip attachment. Not accounting for warpage can result in overflow of excess melted solder or incompletely attached surfaces. The correct prediction of warpage is also important from the perspective of subsequent manufacturing steps such as sintering, wire bonding, moulding etc.

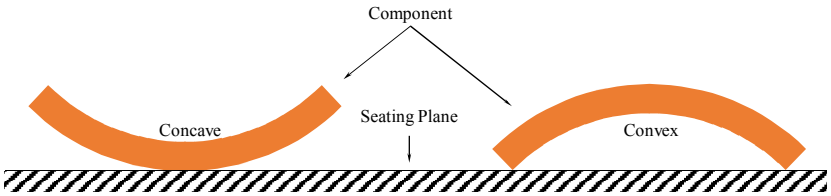


Figure 3.1: Warpage type and naming convention

3.2 Experimental observations

Before the onset of discussing the details regarding warpage, a naming convention for the type of warpage is established here. Warpage is usually observed to be either *Convex* or *Concave*. *Concave* warpage is one where the corners of the component are further away from the seating plane than the middle of the component. Conversely, *Convex* warpage is one were the corners of the components are closer to the seating plane than the middle. This definition is illustrated in Figure 3.1 and consistently used in this doctoral thesis.

Warpage was seen since the initial sample tests for baseplate soldering [BZ16b]. These samples had AMB substrates that were structured (etched copper for circuit layout - ref. Figure 2.5) on the top side while unstructured on the bottom side. They were in this case, 58.3 mm x 58.3 mm in lateral size, had a copper thickness of 0.50 mm and an Si_3N_4 ceramic layer thickness of 0.32 mm. These AMBs were soldered onto copper baseplates that were 200 mm x 90 mm in size with a thickness of 4 mm. In these samples, warpage effect was seen in both, substrates and baseplates (Figure 3.2). Red and bright yellow regions represent locations furthest away from the seating plane.

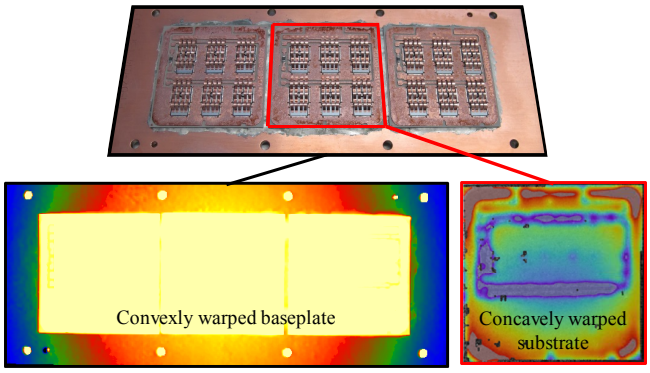


Figure 3.2: Qualitative contour plot of warpage in a baseplate with 3 AMB substrates after soldering

It is clear from the contour plot that for the above shown sample (Figure 3.2), the substrate and the baseplate warp in opposite directions. While the substrate showed concave warpage, the baseplate warpage was of the convex type. Before soldering, at room temperature, no apparent warpage was seen. Therefore, the influence of temperature on warpage was sought and measurements were done on stand-alone (unsoldered) substrates and baseplate at different

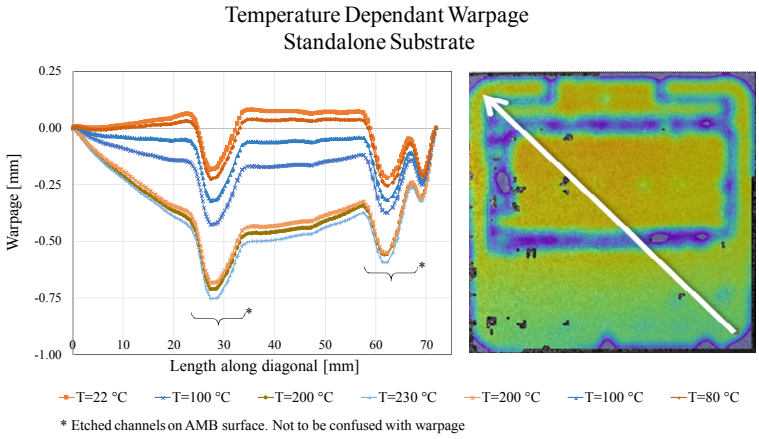


Figure 3.3: Temperature dependence of substrate warpage [GM14]

temperatures ranging from room temperature (22 °C) to soldering temperature (230 °C) using digital image correlation (DIC) [GM14]. The measurements showed that baseplate warpage showed no influence with respect to temperature and remained flat. Substrates however, showed substantial influence with respect to change in temperature. Figure 3.3 shows warpage values for substrates at 22 °C (as delivered), at soldering temperature and finally at room temperature again after cool down.

3.3 Cause of warpage in substrates and baseplate

3.3.1 Substrate warpage

The origin of substrate warpage lies in the so called bi-metallic effect. The bi-metallic effect is encountered when two layers of metals with different CTEs are mechanically constrained and a thermal load, e.g. change in temperature is applied. Application of temperature on a material causes thermal deformation described by Equation (3.1).

$$\Delta L = \alpha L_0 (T - T_0) \tag{3.1}$$

where ΔL is the change in length (thermal expansion or contraction) of the sample, L_0 is the original length, α is the CTE of material, T is the temperature at which ΔL is measured/calculated and T_0 is the initial temperature corresponding to L_0.

In the bi-metallic scenario, one of the two metals deforms more than the other as per Equation (3.1) as different metals have different values for α. As the metallic layers are mechanically fixed/constrained together, the only possibility to accommodate this differential expansion is through geometric curvature. Figure 3.4 shows this effect. The term bi-*metallic* is however a historical artefact as most of its historical applications such as in clockwork, thermostats, thermometers, heat engines etc. employed only metallic materials. Nonetheless, the effect is valid for any material pair of comparable elasticity. Substrate warpage results from the CTE difference between copper (a metal) and Si_3N_4 ceramic (a non-metal). Therefore, strictly speaking, the phenomenon should be called the bi-*material* effect in context of substrate warpage. Nonetheless, in further sections, the two terms are used interchangeably.

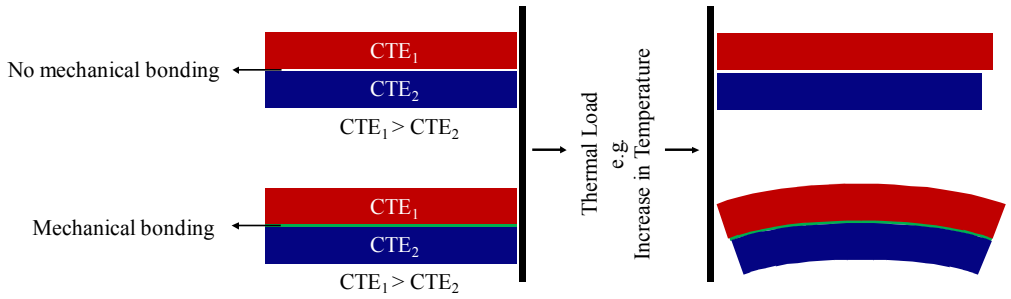


Figure 3.4: Visualisation of the bi-material effect

The AMB manufacturing process strongly joins the copper layer with the ceramic (see 2.2.1). It is important to note that while the CTE of copper is ∼17 ppm, the CTE of the ceramic (Si_3N_4) is only ∼3.5 ppm. Thus, for a copper-ceramic material pair, an increase in temperature would result in the copper layer expanding almost 5 times more than the ceramic layer. As the two layers are constrained due to the AMB manufacturing process, as previously explained, the only way this differential expansion can be accommodated, is through geometric curvature, *viz.* Warpage.

In an AMB substrate however, the ceramic is sandwiched between two layers of copper. This results in material pairs at two locations. Firstly, the *top* AMB copper and the ceramic pair and secondly, the *bottom* AMB copper and the ceramic pair. In this situation, for an increase in temperature, the bottom side AMB copper tends to exert a force that pushes the substrates corner upwards while the top side AMB copper tends to exert a force that pushes the substrates corner downward. If the amount of material available (of comparable thickness) for thermal expansion and consequently the amount of thermomechanical force, is the same on both sides of the ceramic, then the warping effect cancels out from both sides and no net warpage is seen as illustrated in Figure 3.5. It is worthy of note that warpage is an additional out-of-plane deformation superimposed on in-plane deformation. It should however be noted that even in cases when the bending forces are balanced, in-plane shear deformation is always present under temperature change.

It can thus be inferred that warpage in substrates is caused as a result of a difference in the amount of material available for thermal expansion on either side of the substrate ceramic. In the case of substrates where the thermally expandable material is equal on either side of the ceramic mid-surface plane is henceforth called a *Symmetric Substrate*. On the other hand, in the case of substrates where the thermally expandable material is not equal on either side of the ceramic is henceforth called an *Asymmetric Substrate*. With the assumption that the ceramic

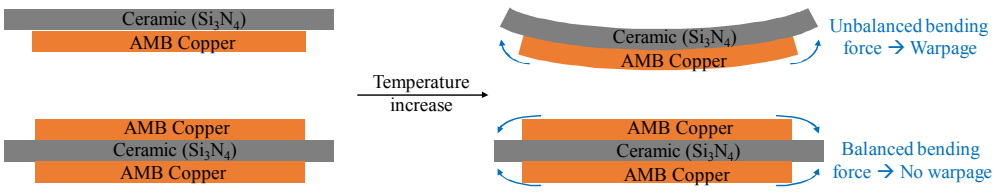


Figure 3.5: Mechanism of substrate warpage

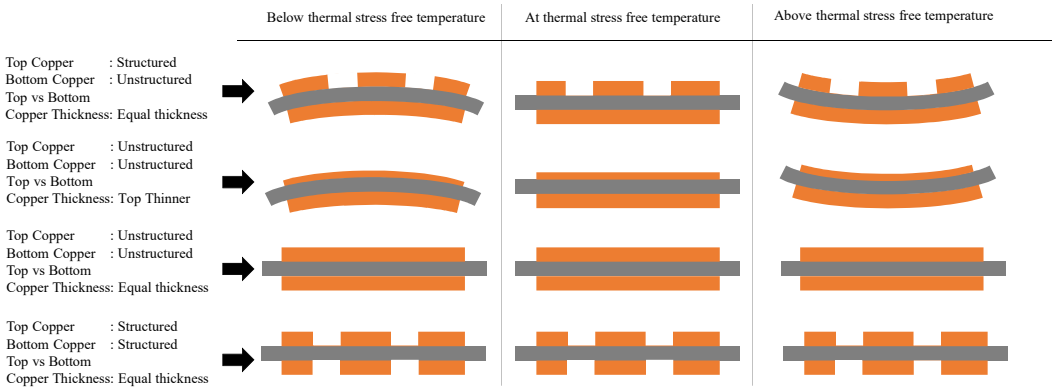


Figure 3.6: Substrate symmetry and possible warpage scenarios

layer brings along no warpage of its own (e.g. due to residual AMB manufacturing stresses) and that the entire substrate has homogenous temperature distribution, only asymmetric substrates result in warpage during temperature changes. Asymmetry in AMB substrates can be brought about mainly through two different ways, namely, differential thickness or differential etching. In the case of differential thickness, the AMB copper thickness on either side of the ceramic is different, resulting in an unbalanced bending force either from the top or the bottom side of the ceramic. In case the thicknesses of copper on both sides is the same an unbalanced bending force between the top and bottom side of the AMB ceramic can be brought about by differential etching, *i.e.* if there is a difference in amount of etching between the top and bottom side AMB copper. Figure 3.6 illustrates the warpage behaviour of various substrate structures under changing temperature conditions.

There can of course, be more complex warpage shapes. An example is shown in Figure 3.7. Here, above the thermal stress free temperature, the substrate would have mixed warpage; convex warpage along one diagonal and concave warpage along the other (vice-versa below thermal stress free temperature). In a three dimensional sense, it would have a saddle shape. These types of substrates are however, not chosen for further investigation as such designs do not add to the existing understanding of the warpage mechanism. Their warpage behaviour can be predicted by either first principles or as described in the sections to follow, by using simulations.

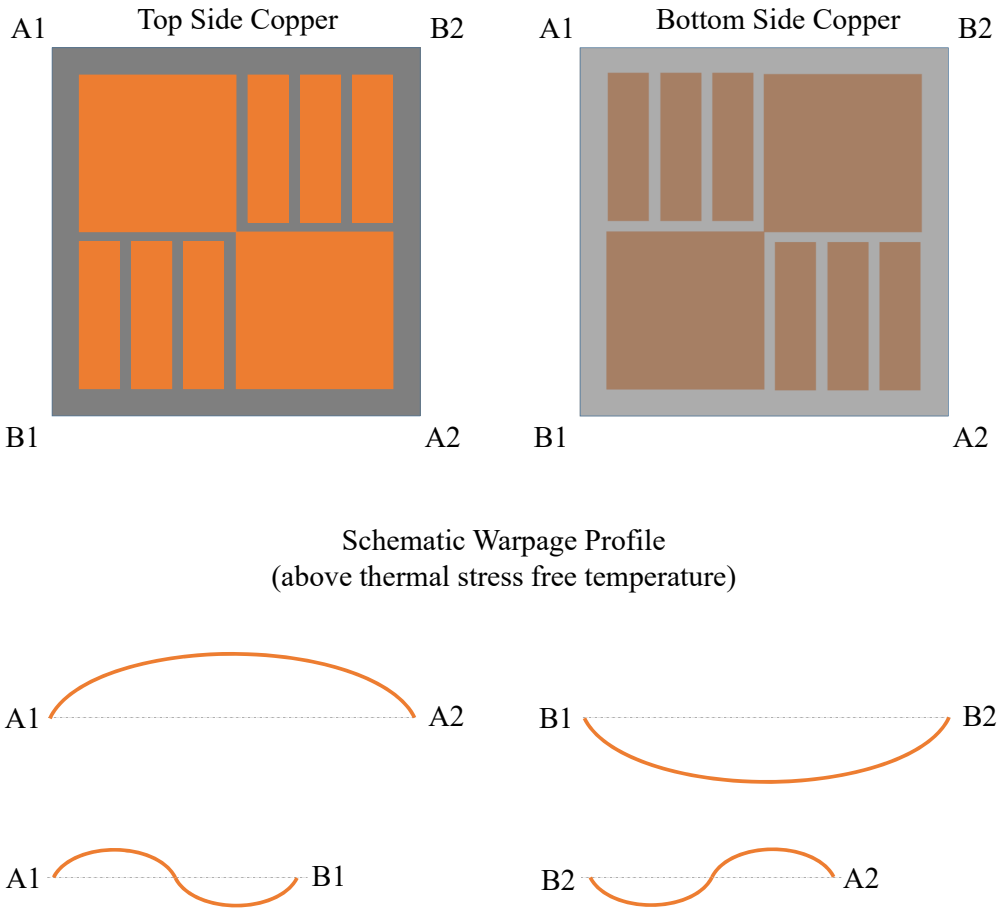


Figure 3.7: Example of a mixed warpage scenario

3.3.2 Baseplate warpage

In the post soldering state, it was not only the substrates, but also baseplates that showed warpage. This was shown in Figure 3.2 and in results seen according to [BZ16b] in Section 3.2. Contrary to substrate warpage, which could be convex, concave or planar depending on the asymmetry of the deformable AMB copper about the AMB ceramic, baseplate warpage was found to be consistently convex (Note that here, $CTE_{AMBaverage} < CTE_{BaseplateCu}$). Additionally, the highest convexity was found directly under the soldered areas. Recall from Section 3.2 that uniform heating and subsequent cooling of stand-alone baseplate (*i.e.* without solder and substrate) resulted in no baseplate warpage.

This meant that the post soldering warpage of the baseplate was not inherent to the baseplate manufacturing or baseplate material but related to the soldering process. To understand the mechanism of warpage in baseplates, it must be recalled from section 3.3.1 that a bimetallic effect manifests itself only if the different involved material layers are mechanically constrained. In other words, if the material with different CTEs are layered upon each other but are able to thermally deform independently of each other, no warping effect occurs.

Before the soldering process starts, the baseplate and substrates are completely free and unconnected as the solder is still in its paste form. As the temperature rises during the controlled heating phase of the soldering process and reaches its peak temperature, both the substrate and the baseplate will have thermally deformed. While the substrate warps in accordance with its asymmetry, the baseplate experiences volumetric thermal expansion as shown in Figure 3.8. However, it is to be noted that both deformations are as of yet independent of each other as at the peak temperature, the solder is molten and therefore offers no structural stiffness. As a result, the baseplate and the substrate are not yet mechanically constrained, and the necessary condition of warpage is not fulfilled.

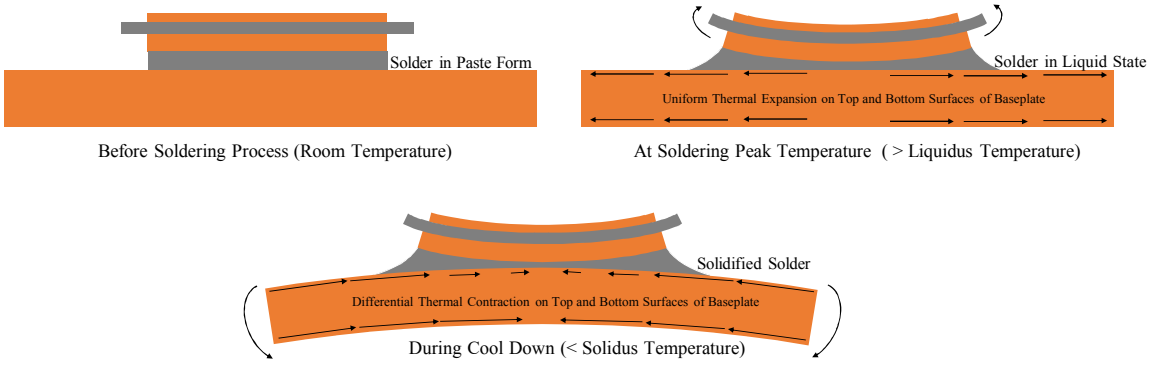


Figure 3.8: Mechanism of baseplate warpage

As the solder begins to cool following the temperature profile of the soldering process, it solidifies below its solidus temperature and results in a mechanical constraint between the substrate and the baseplate. Consequently, only below the solidification temperature does thermomechanical stress (and by extension, warpage) in the baseplate begin to occur. Therefore, the thermal stress free temperature for the baseplate is the solidus temperature of the solder because only below this temperature does thermal stress begin to appear in the baseplate.

As the copper baseplate has much higher CTE as compared to the effective CTE of the substrate, the thermal contraction of the baseplate is higher on it bottom surface than on it top surface which is strongly constrained by the low CTE substrate. This results in a bending force that pulls the edges of the baseplate downwards and gives rise to baseplate warpage. This also explains why baseplate warpage is always convex and has the highest convexity directly under the soldered region where the substrate is joined to the baseplate.

3.3.3 Substrate warpage simulation

For an accurate description of the thermomechanical behaviour of the assembly, it was important that the simulative process acceptably represents the warpage behaviour as this would have an influence on the stress state of the solder layer. As in the case of the experimental observation of warpage, the simulation development was also carried out in two sections, each addressing the issue of substrate and baseplate warpage respectively.

3.3.3.1 Substrate warpage simulation: Thermal stress free temperature

In Section 3.3.1, the mechanism of substrate warpage was discussed. The crux of the discussion was that warpage results only when bodies undergoing temperature changes are constrained together. In the case of the AMB substrate manufacturing process, the mechanical joining is achieved using a thermally activated process (Brazing). It would therefore mean that thermal stress and consequently warpage (if the forces are not symmetrically arranged about the ceramic layer), can develop only below or above this temperature. This temperature is therefore called the *thermal stress free temperature* or *thermal reference temperature* (T_{ref}).

During the AMB manufacturing process two temperatures come up as potential candidates for the thermal stress free temperature. First is the brazing temperature ($\sim$ 780 °C - 800 °C) as this is the temperature at which the copper layer and the ceramic is mechanically joined together. The second candidate for thermal stress free temperature is the temperature encountered during the etching step. Etching is carried out as a separate process at temperatures between 30 °C and 60 °C, after the brazed substrates have been cooled down to room temperature. This could allow the thermal stress in the copper layer of the substrates to relax by heat supplied during etching. It could also be possible that the AMB ceramic and AMB copper have different thermal reference temperatures.

To obtain a better understanding of the thermal stress free temperature, a simple simulation was set up to determine the sensitivity of warpage to the thermal reference temperature of the ceramic and the copper. The construction of the AMB, structured on top and unstructured at the bottom is shown in Figure 3.9(a) while the mechanical boundary conditions of the simulation is shown in Figure 3.9(b).

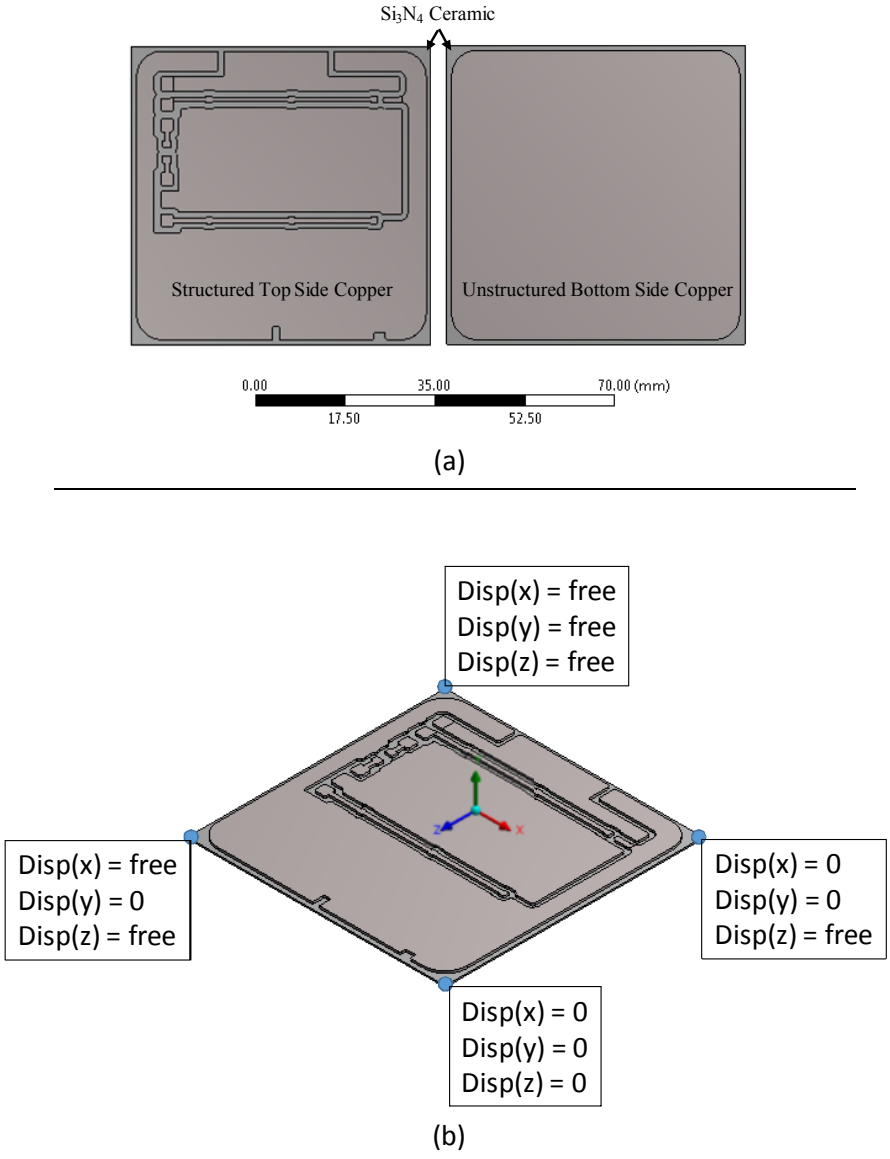


Figure 3.9: Simulation setup for the analysis of warpage sensitivity to thermal reference temperature (T_{ref}).

In the sensitivity analysis, the thermal reference temperature of both, AMB copper and AMB ceramic, are varied independently from 10 °C, 60 °C, 95 °C through 130 °C. Consequently, from the simulations, we can obtain a warpage value for each combination (N_{TrefCu} x $N_{TrefCer}$ = 4 x 4 = 16 in total) of thermal reference temperatures of the AMB copper and ceramic.

Rough estimates for the maximum warpage of the substrate at different temperatures were available from the substrate manufacturer. Using this as a reference point, the relative influence of the thermal reference temperature of AMB copper and the ceramic on warpage could be evaluated qualitatively. Figure 3.10 and Figure 3.11 show the variation of maximum substrate warpage with respect to various thermal reference temperatures for AMB copper and the ceramic.

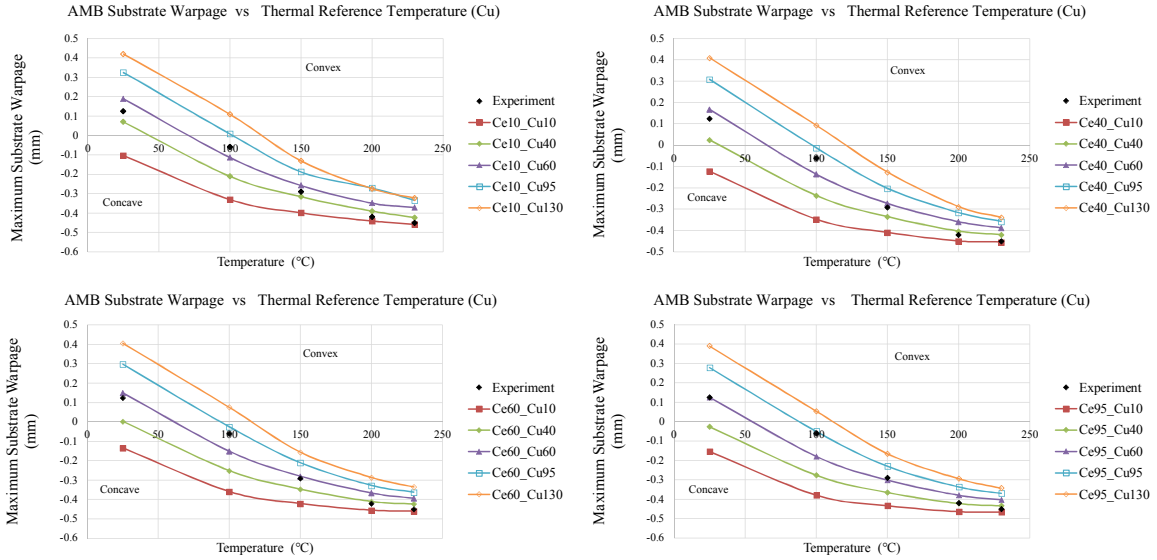


Figure 3.10: Max. Warpage v/s thermal reference temperature of AMB copper

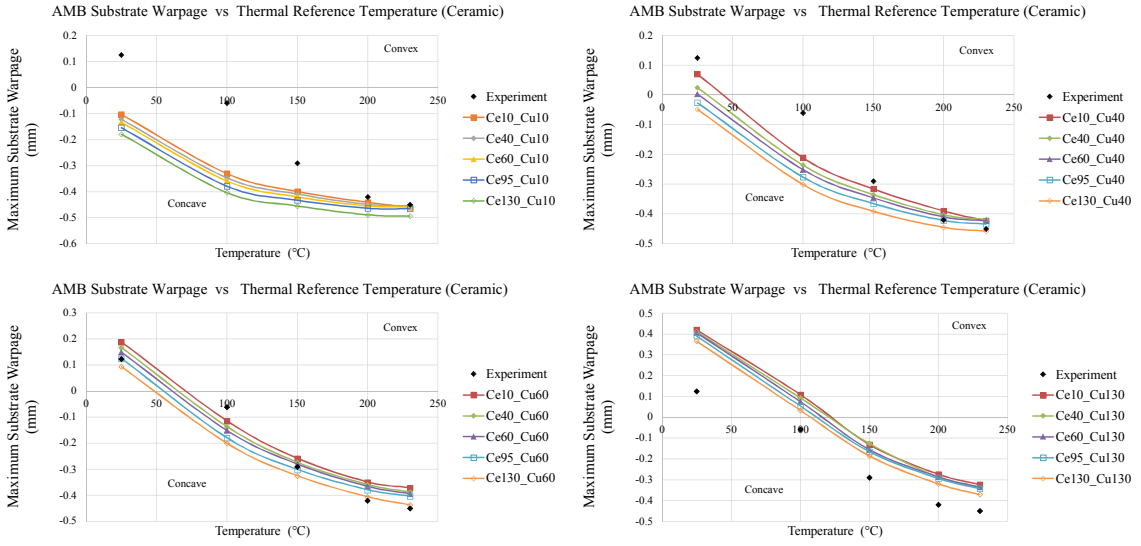


Figure 3.11: Max. Warpage v/s thermal reference temperature of AMB ceramic

From the results of Figure 3.10 and Figure 3.11, two clear conclusions can be made.

1. **Sensitivity of warpage to thermal reference temperature**
   In Figure 3.10, each of the four graphs depict the change in substrate warpage with changing thermal reference temperature of copper while the thermal reference temperature of the ceramic layer is kept constant. The legend in the graphs shows the thermal reference temperature assigned to the copper and ceramic layers. For example, the plot corresponding to the legend entry *Ce10_Cu60* corresponds to the simulation case where the reference temperatures of the ceramic and the copper layers are set to 10 °C and 60 °C respectively.

   It can be seen that for any given thermal reference temperature corresponding to the ceramic layer, warpage shows considerable sensitivity to the thermal reference temperature assigned to copper. Figure 3.11 on the other hand shows that when the thermal reference temperature of copper is kept constant and the thermal reference temperature of the ceramic layer is varied, warpage values show only minor change.

   A physical explanation for this effect simply is that the CTE values of the ceramic layer and copper respectively. The CTE values of copper lies between 17 - 19 ppm/K [Mat01a] while the CTE value of Si_3N_4 is found to be up to only 3.7 ppm/K [Mat01b], *i.e.* much less than copper.

   As already discussed in Section 3.3.1, warpage is a direct result of the differential expansion of two mechanically contained bodies which in turn, is proportional to the CTE of the respective materials. As copper has a much higher CTE as compared to that of Si_3N_4, for the same change is temperature, copper exhibits considerably higher thermal deformation and consequently has a much greater influence on the warpage of the substrate.

   It can therefore be concluded that for all practical purposes, the thermal reference temperature of the ceramic is inconsequential and that the substrate can be considered to have a uniform, effective thermal reference temperature.

2. **Range of thermal reference temperatures**
   In Section 3.3.3.1, two potential candidates for the thermal stress free temperature were mentioned, namely, the brazing temperature and the etching temperature. Referring to Figure 3.11, one can see that the experimental warpage values (black diamond dots) lie close to the simulated warpage values when the copper stress free temperature is set in the rage of 40 °C - 60 °C. In addition to this, Figure 3.11 also shows that as the thermal reference temperature of copper is increased, this progressively results in the overestimation of convexity of the substrate at room temperature and underestimation of concavity at soldering peak temperature (230 °C). Extending this behaviour would mean that if the brazing temperature ($\sim$ 780 °C - 800 °C) is set as the thermal reference temperature, the substrate would exhibit only convex warpage through all the temperatures considered in the above scenarios (25 °C to 230 °C). This is an unrealistic behaviour considering the fact that any substrate with a lower amount of copper on the top side of the substrate as compared to the bottom side (as in the case of the substrates investigated by [BZ16b] mentioned earlier in Section 3.2) is always mildly convexly warped at room temperature (indicating that the difference between room temperature and the thermal reference temperature is small and that T_{ref} > room temperature) and strongly concavely warped at 230 °C (indicating that the difference between soldering temperature of 230 °C and thermal reference temperature is large and that the value of $T_{ref} < 230$ °C).

For the determination of the actual thermal reference temperature, the above two observations, clearly excludes brazing temperature as a potential candidate and narrows it down to a range between 40 °C and 60 °C. Due to the low sensitivity of warpage to the ceramic thermal reference temperature, it can also be assumed that the entire substrate has a homogenous thermal reference temperature and that separate thermal reference temperatures for copper and ceramic are not required in simulations.

3.3.3.2 Substrate warpage: Warpage measurement from cross sections and final determination of thermal reference temperature

The previous sections described how value of T_{ref} was narrowed down to temperatures between 40 °C and 60 °C. To conclusively determine the value of T_{ref} which could accurately predict substrate warpage, cross sections of soldered substrates were used. This is done because below the soldering temperature, the solder is solid, and the substrate can no longer return to its warpage values corresponding to room temperature. This means warpage measurements from cross sections provide us the exact warpage of the substrates in a post soldering state and reflect reality the best.

A total of eight samples were soldered with substrates having top and bottom side structures as shown earlier in Figure 3.9. Cross sections were done through the vertical plane through the middle of the soldered substrates. Assuming the centre of the bottom copper surface as a reference point, is was possible to measure the vertical displacement of the substrate extremities, which gives the absolute value of warpage relative to the centre of the substrates bottom surface. An overview of the process is given in Figure 3.12.

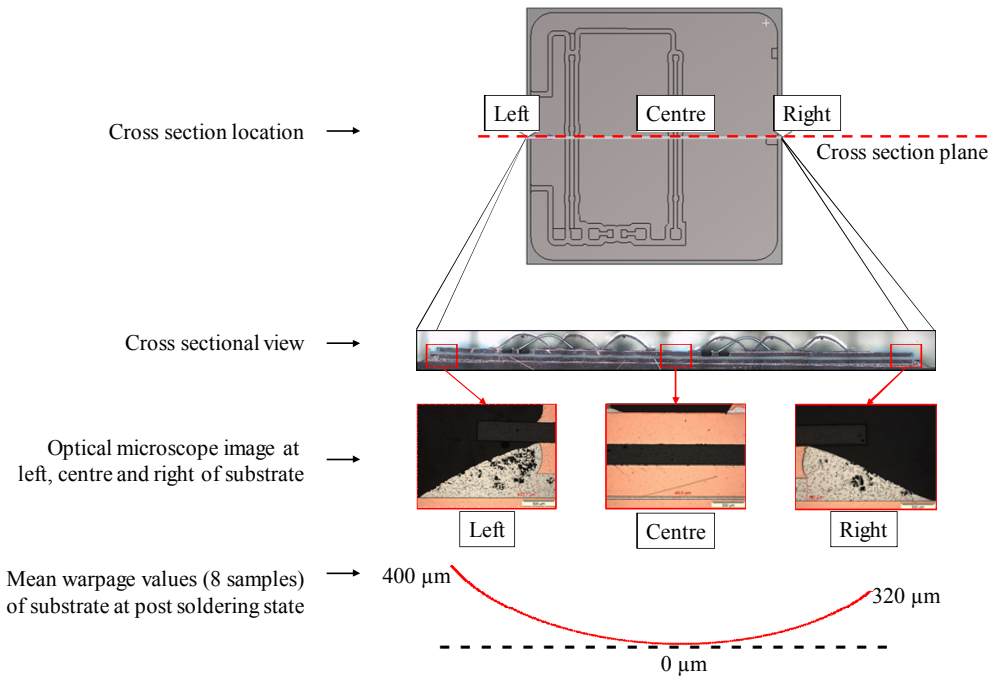


Figure 3.12: Warpage from cross section of soldered samples

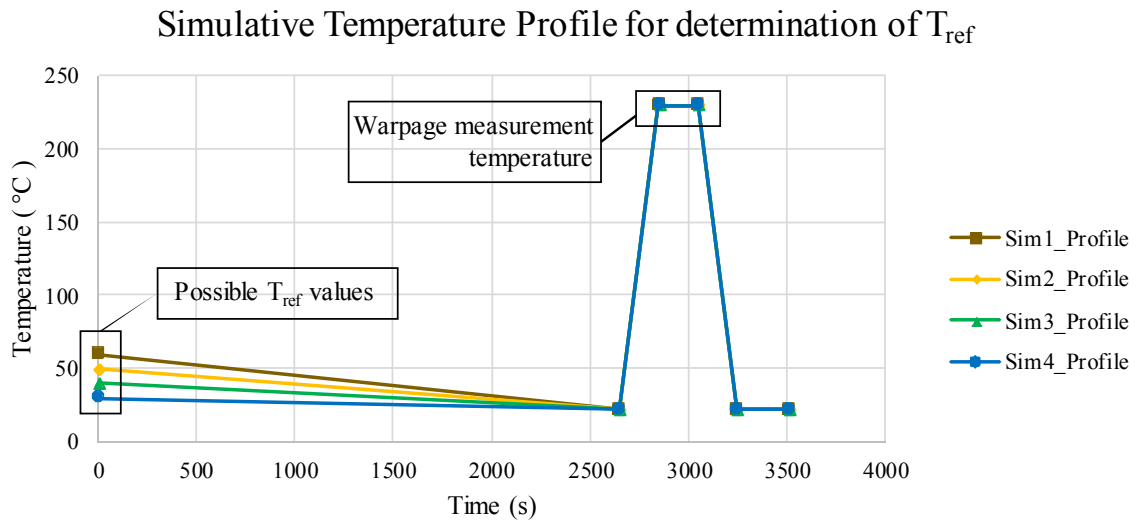


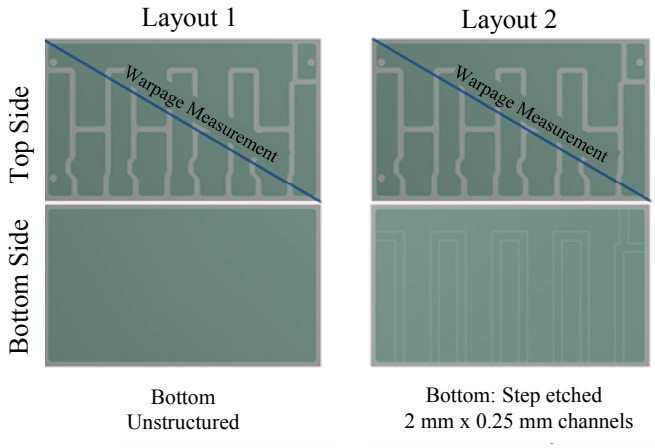
Figure 3.13: Various potential starting T_{ref} values used in determining actual T_{ref} through simulation

Once the warpage at soldering temperature was measured, simulations were carried out to determine the substrate T_{ref}. The simulation starts at the thermal reference temperature (as of yet undetermined but known to lie between 40 °C and 60 °C). In the next loading steps, the temperature is brought down to room temperature (22 °C) and then raised to soldering temperature (230 °C). Figure 3.13 shows the simulative temperature profile applied.

Subsequently, the warpage in the substrates is noted from the simulation at the same cross section plane as in Figure 3.12 at the soldering temperature and compared with the measured results available from cross sections. It was found that a $T_{ref} = 42$ °C matched the cross sectional measurements the best. This value was also verified through two subsequent points.

1. During later exchange meetings with the substrate manufacturer [Iwa+16], it was found that the etching process during substrate manufacturing was indeed carried out within a temperature range of 40 °C - 45 °C. This helps build confidence in the explanation and the simulative validity developed as discussed in the previous sections of this chapter regarding T_{ref} and substrate warpage.

2. Warpage values of substrates with two other layouts were simulated and later compared with warpage measurements. The warpages were compared at delivery, *i.e.* room temperature (22 °C) and at 150 °C. At both temperatures, the simulative results matched very well with the experimental values. The layouts and warpage values are shown in Figure 3.14.



Warpage Values	Layout 1	Layout 2
Measurement @ 22 °C	72 µm	53 µm
Simulation @ 22 °C	84 µm	49 µm
Measurement @ 150 °C	-463 µm	-123 µm
Simulation @ 150 °C	-447 µm	-117 µm

Figure 3.14: Warpage prediction with T_{ref} = 42 °C

3.3.3.3 Substrate warpage: Simulation methodology comparison of substrate CAD design with pre-etched substrate versus substrate CAD design with simulated *in-situ* etching

Until now, the discussion about warpage was limited to a single temperature swing, *i.e.* from room temperature to soldering temperature and back to room temperature. However, for reliability investigations, it is important to understand the behaviour of warpage under temperature cycling. In this regard there are two simulative possibilities that needed to be investigated.

1. Simulation using substrate CAD geometry that already includes the etched structuring. The simulation steps followed in this method is described below.
   (a) Set simulation T_{ref} = 42 °C
   (b) Build and import CAD model into simulation already containing etched structures.
   (c) Start Temperature loading following the Profile:
   T_{ref} → 22 °C → 230 °C → 22 °C → -40 °C → 175 °C → <continue temperature cycling>
2. Simulation using CAD geometry that does not include the etched structuring. The etching is carried out during the simulation by deactivating elements corresponding to the etching locations.
   (a) Set simulation T_{ref} = 42 °C
   (b) Build and import CAD model into simulation containing no etched structures.

(c) Start Temperature loading following the Profile:
T_{ref} → 22 °C → T_{ref} (etching temperature) → Perform etching step by deactivating FEM elements corresponding to etching locations → 22 °C → 230 °C → 22 °C → -40 °C → 175 °C → <continue temperature cycling>

For reliability related predictions discussed in Chapter 5, it was necessary to know the difference in results between the two methods and as to which method was better suited for the purpose of lifetime modelling.

To quantify the difference between the two methods, the steps mentioned above were carried out and 11 simulative temperature cycles were simulated. Within each temperature cycle, the warpage changes from convex to concave or *vice-versa* depending on the symmetry of the copper on the substrates (recall discussion from Section 3.2). Therefore, for each temperature cycle, the absolute value of the change in warpage between the points of minimum and maximum temperature (T_{TCmin} and T_{TCmax} respectively) during the temperature cycle was simulatively measured according to Equation (3.2).

$$\Delta Warp = |(Warp)_{T_{TCmin}} - (Warp)_{T_{TCmax}}| \tag{3.2}$$

In addition to this, the equivalent plastic strain, $\Delta\varepsilon_{eqv}^{pl}$ accumulated in the copper layer during each temperature cycle is also noted according to Equation (3.3) where $(\varepsilon_{eqv}^{acc.pl})_{T_{TCmin}}$ and $(\varepsilon_{eqv}^{acc.pl})_{T_{TCmax}}$ are the plastic strain accumulated up until the beginning and end of the TC cycle respectively (*i.e.* T_{TCmin} and T_{TCmax}).

$$\Delta\varepsilon_{eqv}^{pl} = |(\varepsilon_{eqv}^{acc.pl})_{T_{TCmin}} - (\varepsilon_{eqv}^{acc.pl})_{T_{TCmax}}| \tag{3.3}$$

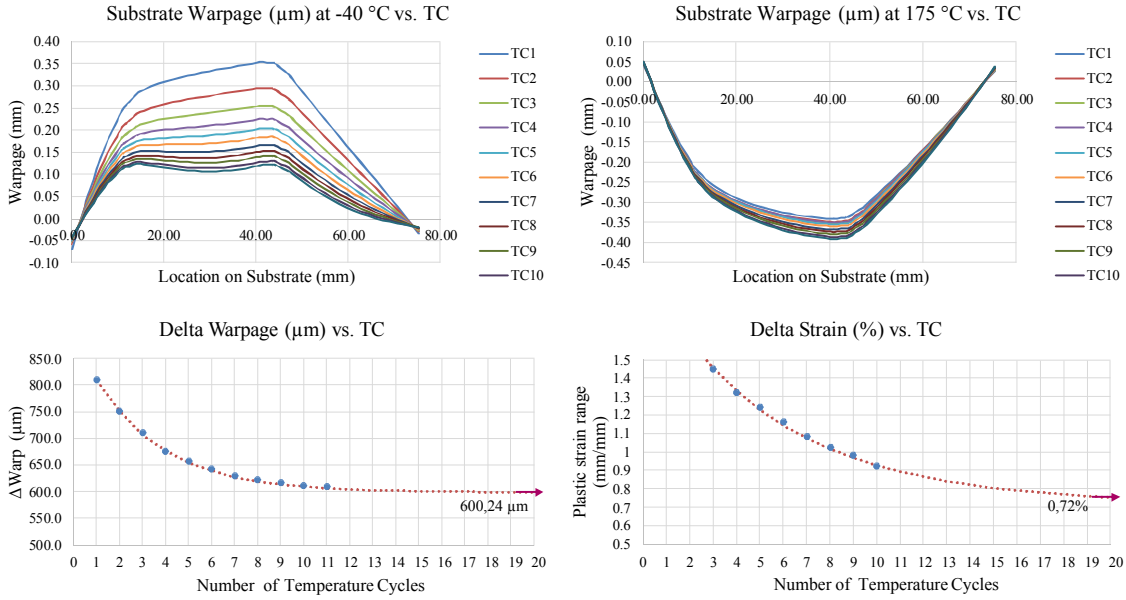
From the graphs presented in Figure 3.15, three conclusions can be obtained.

1. In both model types, with each increasing temperature cycle, the absolute warpage at -40 °C becomes less convex and absolute warpage at 175 °C becomes more concave compared to the warpage in the preceding cycle. The change in magnitude of warpage at -40 °C and at 175 °C is drastic in the beginning and smaller with each subsequent temperature cycle. The reason for this is the work hardening (also called strain hardening) of copper as described in Section 2.5.1. However, it is worthy of note that the magnitude of this change is different at the two extremum temperatures. The stabilization of absolute warpage takes longer at -40 °C than at 175 °C. This can be explained in terms of plasticity of the copper material. As at higher temperature (e.g. 175 °C), more plastic deformation takes place as compared to lower temperature, the material hardens faster (by the same argument, slower at lower temperature e.g. -40 °C).

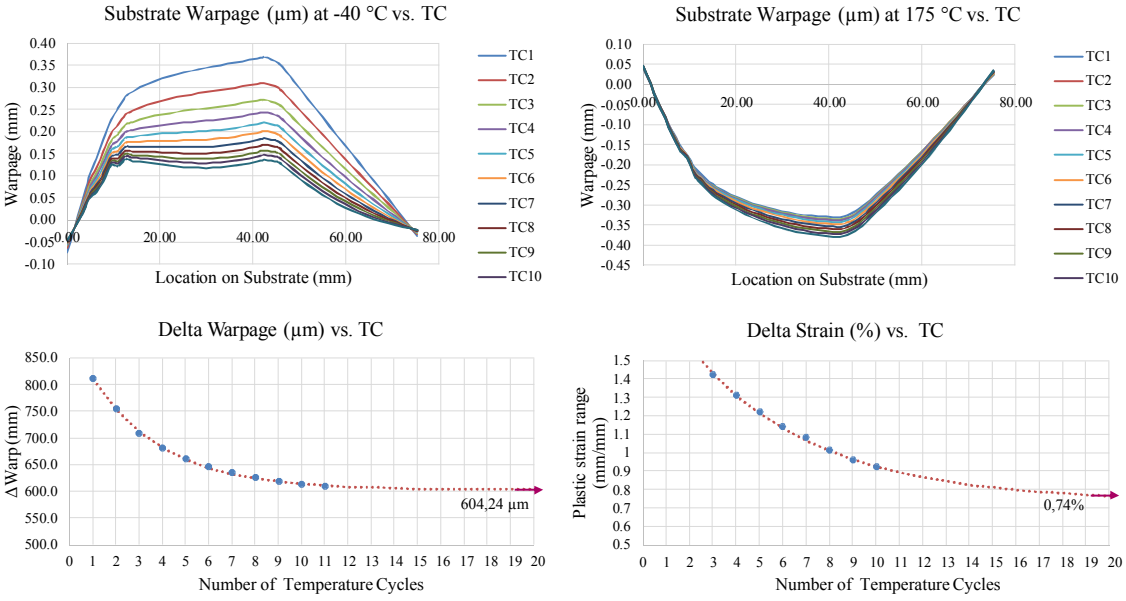
2. In both methods, obtained absolute warpage value is comparable at both evaluation temperatures and $\Delta Warp$ values converge to nearly identical values (∼600 µm).

3. In both methods, obtained plastic strain range in the copper layer is nearly identical and converges to nearly identical values (∼0.73%)

The above mentioned results establish an equivalence between the two discussed simulation methods. As the *in-situ* etching method is more complex, more computationally costly and comparatively less stable during the FEM solution process, for all simulations henceforth, involving etched substrates, the pre-etched CAD method is used.



(a) Warpage and strain characteristics for simulation with *pre-etched CAD*



(b) Warpage and strain characteristics for simulation with *un-etched CAD (in-situ etching)*

Figure 3.15: Warpage and strain characteristics of simulation methodologies using pre-etched CAD and *in-situ* etching

3.3.3.4 Substrate warpage: Geometric sensitivity and warpage reduction strategies

In the previous sections, a reliable substrate warpage simulation method was established. As a subsequent investigative step, warpage sensitivity with respect to copper thickness was sought. For this purpose, simulations were carried out with unstructured substrates where the bottom side copper thickness was kept constant at 0.500 mm and the top side copper thickness was varied. Maximum warpage values at soldering temperature for various top and bottom copper thickness combinations are shown in Figure 3.16. It clearly shows a high sensitivity of warpage with changing copper thickness.

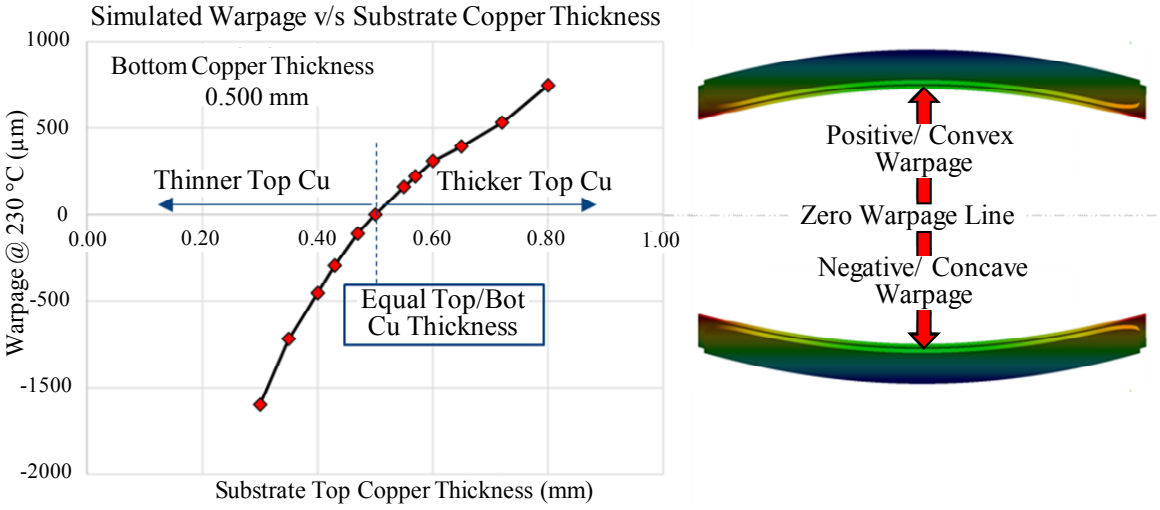
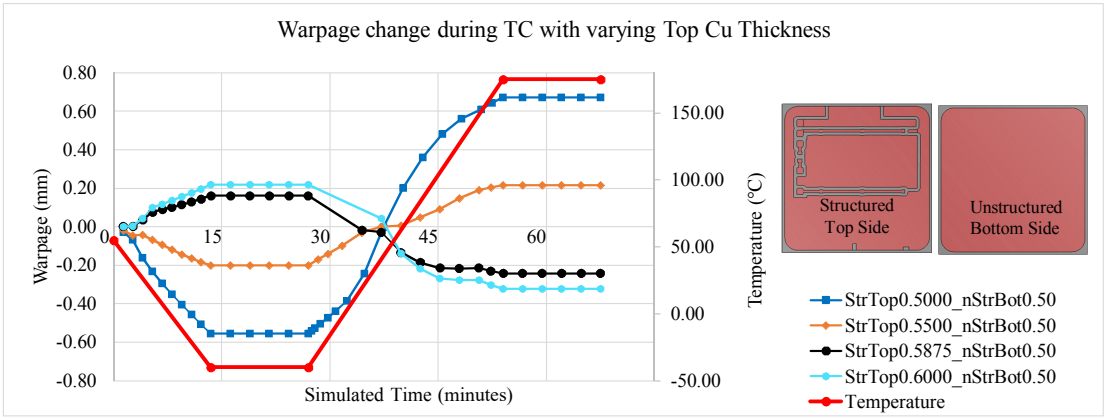


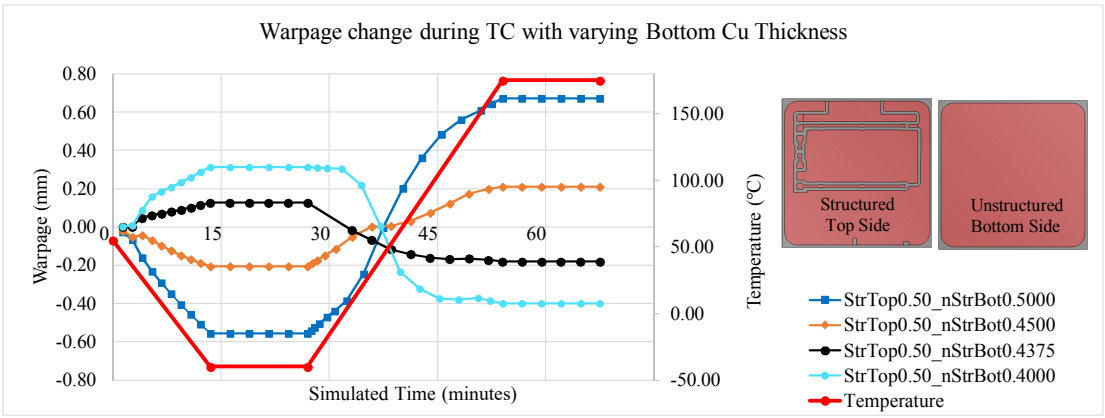
Figure 3.16: Warpage sensitivity with respect to copper thickness

For the sake completeness, similar simulations were also carried out with substrates that were structured on the top side (such substrates are relevant in commercial applications). As can be seen in Figure 3.17(a), the top side copper thickness is varied from between 0.5 mm and 0.6 mm while the bottom side copper thickness is varied between 0.4 mm and 0.5 mm (see Figure 3.17(b)). As in the case of unstructured substrates, warpage shows extreme sensitivity to the thickness of copper. It is worthy of note that just by a small change of 0.1 mm in the thickness of the copper layer, complete reversal of warpage behaviour (from concave to convex or *vice-versa*) can be encountered.

It is clear that for good warpage control in substrates, tight manufacturing tolerances are required. However, most substrate manufacturers provide for a copper layer thickness tolerance range of ±10% of the nominal thickness. This is already very high as demonstrated in Figure 3.17. It is therefore inevitable to discuss the possible strategies to reduce warpage in power substrates.



(a)



(b)

Figure 3.17: Warpage sensitivity of structured substrates with respect to copper thickness

Warpage reduction strategies discussed below relies on three major aspects that influence warpage.

1. **Reducing force due to thermal expansion of copper:** As previously discussed in Section 3.3.1, the main reason for substrate warpage is unbalanced bending forces generated due to thermal expansion of copper. A straight forward approach therefore, to reduce substrate warpage is to reduce the amount of bending force. This can be achieved if the volume of copper available for thermal expansion is reduced. Figure 3.18 (Warpage v/s Copper Thickness) show the warpage profile of the substrate at soldering temperature (230 °C) for different copper layer thicknesses. The reference substrate shown in the figure has a structured top side and an unstructured back side, both with same copper thickness of 0.5 mm (resulting in less copper on the top side and consequently causing concave warpage at 230 °C). Measured between diagonally opposite corners of the ceramic layer, the warpage for the standard 0.5 mm substrates is 0.568 mm. As the thickness on both sides is reduced to 0.3 mm and 0.1 mm, the warpage also reduces due to the reduction in the volume of copper that generates the bending force.

   An interesting aspect to this phenomenon is that the increase of substrate warpage with increasing copper thickness does not continue without limit. After a given value of increase in copper thickness, the warpage starts to decrease again. This occurs due to the fact

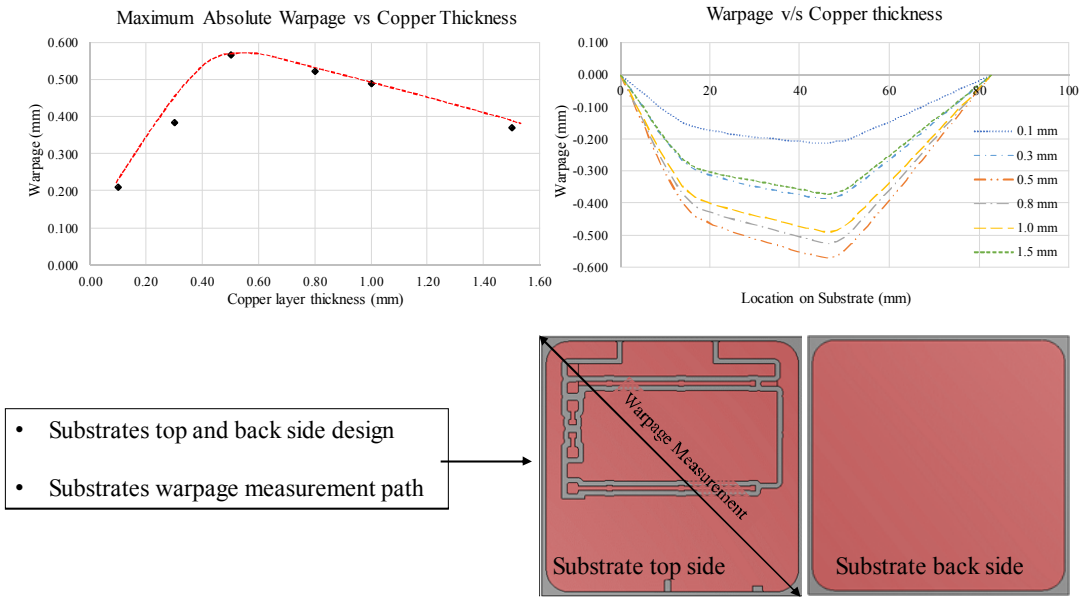


Figure 3.18: Warpage control via Cu thickness

that with increasing thickness of the substrate, the bending stiffness of the substrate also increases. In the example shown in Figure 3.18, the effects of increasing bending force and increasing bending stiffness counteract each other at approximately 0.6 mm for the substrate structure investigated in this section.

Reducing copper thicknesses in AMB substrates may not always be suitable as reducing the copper thickness reduces the current carrying capacity of the substrate. In the other direction, *i.e.* increasing thickness; for acceptable warpage values, the copper thickness required could be unrealistically large depending on the asymmetry. However, a suitable mix of AMB circuit design and unequal copper thickness of the top and bottom sides can prove to be useful especially in commercial applications.

2. **Increasing bending stiffness of the substrate:** Another possible method to reduce warpage is to increase the bending stiffness of the substrate without increasing the bending force contributed by the copper layer (as was the case in the previous point). This can be achieved by increasing the thickness of the ceramic layer which is also stiffer than copper. The simulation results shown in Figure 3.19 demonstrate this effect.

   It must be noted that while warpage is reduced, the effective CTE of the substrates is reduced due the fact that Si_3N_4 has a very low CTE (~3.5 ppm). This increases the overall CTE mismatch between substrate and solder which has a CTE of ~19 ppm. The impact of such mismatch and the additional stiffness that the thicker ceramic brings along is investigated in Chapter 5.

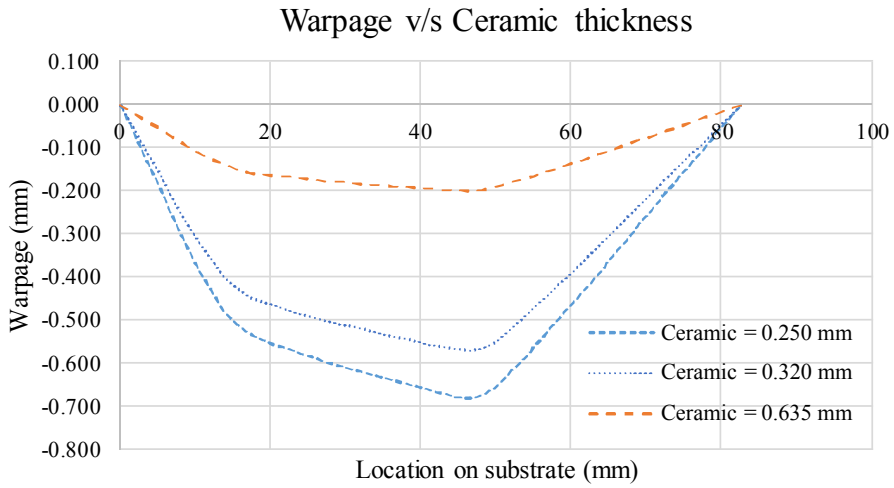


Figure 3.19: Warpage control via ceramic thickness

3. **Copper balance on either side of ceramic:** As already shown in Figure 3.5, if the amount of copper on both sides of the ceramic layer is equal, no warpage results as the force due to thermal expansion (or contraction) of copper is balanced out.

   In practical applications, power substrates are always structured on the top side for circuiting purposes. Therefore, the most obvious method to balance out copper volume on either side of the ceramic is to have the exact same layout on the back side as on the top side. This results in *symmetric* substrates that exhibit no warpage at any given temperature.

   A potential disadvantage to this option is that, as the structuring on the top and bottom side are identical, the etching locations match up and a narrow channel of ceramic is exposed that is structurally not supported by copper on either side. Such locations can be a point of ceramic fracture due to mishandling or other manufacturing processes that must be carried out on the substrate (*e.g.* sintering of chips on substrates which involves the application of high pressure and temperature loads on the substrate surface). Another potential disadvantage is a discontinuous solder-substrate interface due to etched channels on the bottom/back side of the substrate. These discontinuities could result in stress concentration regions and lead to crack initiation in the solder joint. This is illustrated in Figure 3.20.

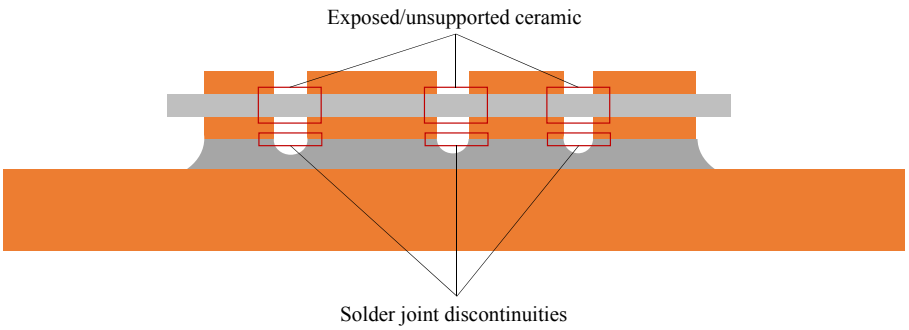


Figure 3.20: Warpage control via symmetric copper structuring and potential disadvantage

A possible solution to this issue can be *step etching* on the back side of the substrate. In this kind of etching, the copper on the ceramic back side is not completely etched to the ceramic layer but only half way through the copper thickness. Depending on the depth of the step etching, the width of the step etched copper surface may be adjusted to balance out copper amount on the two sides of the ceramic. Figure 3.21 shows a substrate with a conventional structured top side copper and the proposed step etched bottom side copper.

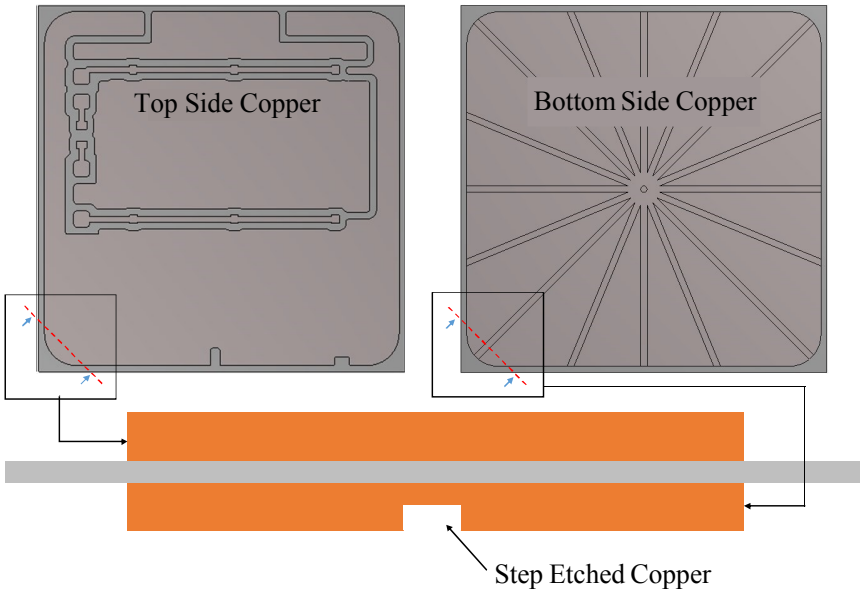
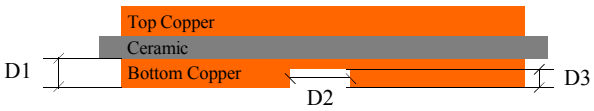


Figure 3.21: Warpage control via step etching

It must be kept in mind that the etching tolerances are still present in case of step etching. Therefore, it was important to also analyse the sensitivity of warpage to the etching tolerances of step etched structures. The general tolerance values of the etching process is 10% of the nominal specified copper thickness, *i.e.*, if the specified copper thickness is 0.2 mm, then the final product after the etching process will have a copper thickness of 0.2 mm $\pm$ 0.02 mm. Consequently, simulations were also carried out with various widths and depths of step etched channels. Figure 3.22 shows these various combinations. $D2$ and $D3$ are varied by 10% of their respective nominal values of 1.000 mm and 0.200 mm.



D1(mm)	D2(mm)	D3(mm)
0.500	1.000	0.180
0.500	1.000	0.200
0.500	1.000	0.220
0.500	0.900	0.200
0.500	1.100	0.200

Figure 3.22: Various combinations analysed to assess warpage sensitivity with respect to step etching tolerance

As can be seen from Figure 3.23, that compared to the conventional substrate with structured top and unstructured bottom side (each 0.5 mm thick), the step etched variants show as much as 5x lesser warpage. In addition to this, warpage in step etch variants also show only minor sensitivity to step etching tolerance. This is due to the fact that during step etching, the 10% tolerance only affects a small region of the substrate copper while in the case conventional substrates, the adjustment of the thickness of the bottom side copper layer through etching affects the entire copper surface.

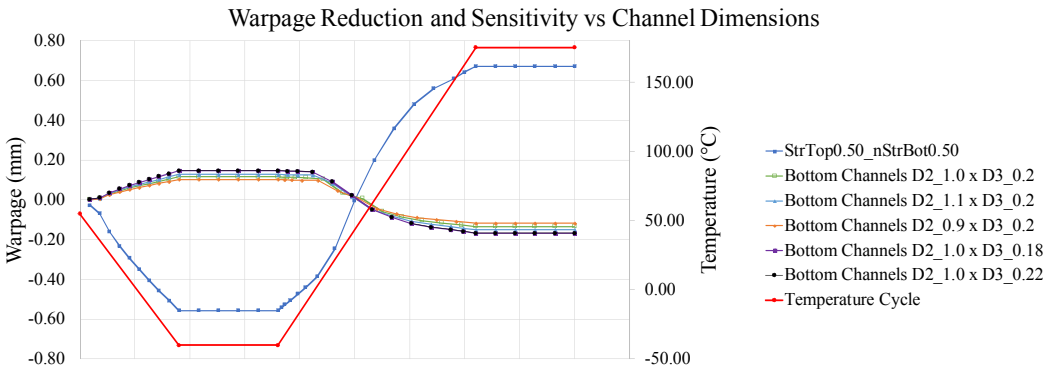


Figure 3.23: Warpage sensitivity with respect to step etching tolerance

3.4 Baseplate warpage and soldering process simulation

In Section 3.3.2, the phenomenon of baseplate warpage was discussed. As this warpage resulted from the differential contraction of the top and bottom surfaces of the baseplate due to the solidification of the solder layer, residual thermal stresses would be built up in the solder material. For a simulation based estimation of lifetime of such components, it was thus imperative that the baseplate warpage effect was correctly represented in simulations.

Methodologies for the structural simulation of physical phase change phenomena can be found in literature for microelectronics and packaging [LL11] and related fields such as welding [Sim+06]. For an FEM based simulation, these studies cite element birth and death as an effective method. According to the *ANSYS*® (FEM simulation software) user's manual, *"This capability is useful for modelling effects due to phase changes (as in welding processes, when structurally inactive molten material solidifies and becomes structurally active)..."*. Similar applications in case of flip chip assemblies were also shown in [Byu14]. The essential idea of the simulation procedure for soldering or for welding is that during the soldering or welding process, the joining material is in the liquid state and makes no contribution to the overall structural stiffness. In a structural sense, it is equivalent to saying that the molten solder is non-existent. To represent this behaviour, during the FEM simulation, the solder elements are simply deactivated by multiplying all its material properties by a very small number (in ANSYS® the default multiplying factor is 10e-6). Subsequently, as the solidification of the solder pool starts, the elements are reactivated to their original material properties which then, contribute to structural stiffness and thermal expansion behaviour of the assembly.

3.4.1 Baseplate warpage: Simulative challenges

Despite the fact that simulative studies of deformation in welded joints and also simulation of assembly of electronics packages exist and the know-how is to some extent transferable to the simulation of baseplate soldering; due to the large size of the joining partners and the significant warpage of the substrates and baseplate, the simulation of the soldering process and consequent warpage of the baseplate throw-up some unique challenges.

Initial simulative attempt
The first attempts made to simulate the soldering process and baseplate warpage was carried out in the steps as shown in the flowchart shown in Figure 3.24.

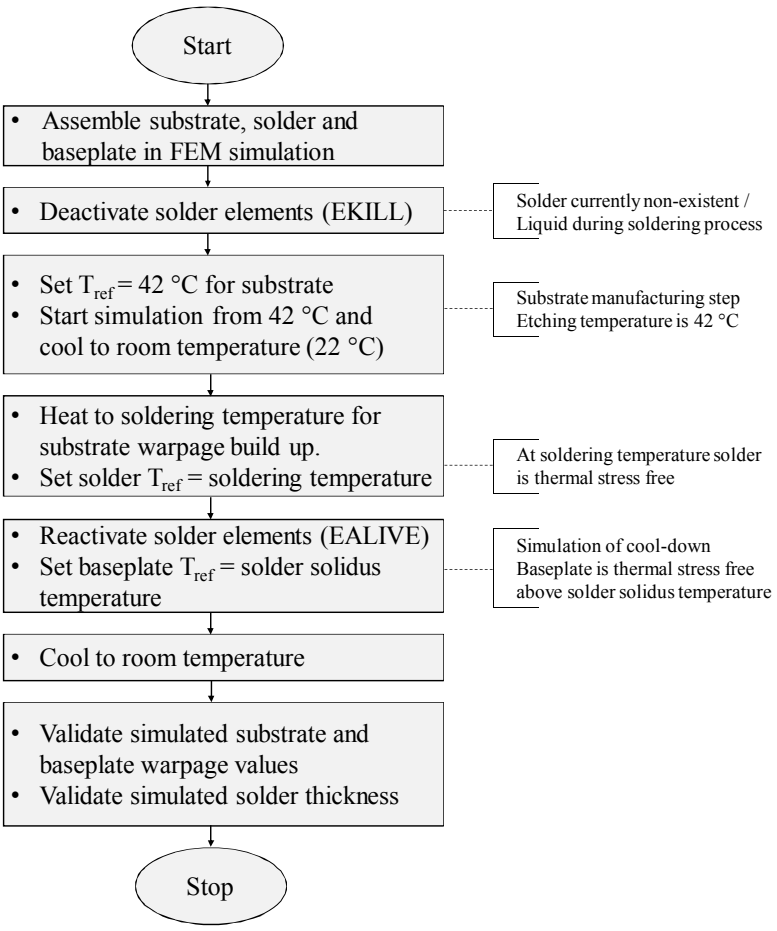
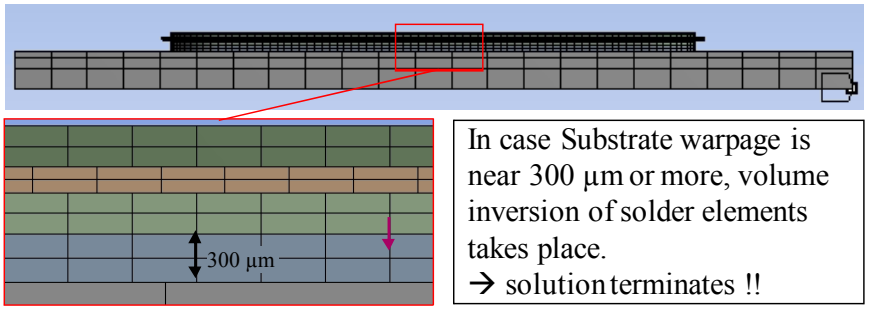


Figure 3.24: Flowchart: Soldering process simulation

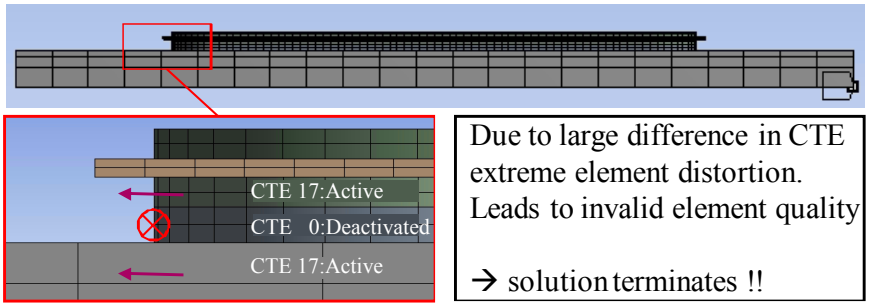
The flowchart for the simulation of the complete manufacturing process mimics the actual manufacturing process in each step. This should have, in principle, been able to account for the warpage of the substrates, replicate the soldering process and consequently predict the warpage produced in the baseplate also. However, the FEM simulations results in severe convergence issues. The reason for failure of convergence was the extreme distortion of the elements in the FEM simulation. This usually can be traced back to deficient displacement boundary conditions/constraints or strong loading gradients. However, in this case, the changing of displacement constraints or applying the thermal load more slowly had no effect

on the convergence behaviour. Material properties were also checked for inconsistencies of units or correspondence to incorrect temperature for temperature dependant material properties. None of the above were erroneous.

As a hint to the convergence issues, it was seen that distortion based errors showed a peculiar pattern. The elements corresponding to the error always occurred in the solder elements either at the corners of the substrates or at the centre. Also, the errors occurred only while the temperature ramp up to soldering temperature or at the soldering peak temperature. At these temperatures, the substrate warpage (concave for top etched and bottom unetched substrates) reaches its maximum absolute values. Additionally, the relative displacement between the substrate and the baseplate also reaches its maximum value. Further analysis of the models revealed two problems.



(a)



(b)

Figure 3.25: Root causes of simulative non-convergence

Both of these problems are schematically represented in Figure 3.25(a) and Figure 3.25(b) and described below

1. **Warpage of the substrate**
   To mimic the soldering process exactly, the initial solder thickness (before simulative soldering step) in the simulation was kept at 300 µm - same as the nominal solder thickness in experiments. However, the simulated warpage of the substrate was more than 300 µm. This results in the centre area of the substrate pushing down on the top surface of a deactivated solder layer through a vertical displacement more that its own thickness. This causes volume inversion of FEM element and leads to so called *negative Jacobian* values. Jacobian is an indicator of the similitude of the shape of elements in the simulation and the ideal, theoretical shape of the elements. Once negative Jacobian values are encountered, FEM simulations are no longer stable and result in non-convergence.

2. **CTE of the deactivated solder**
   It is worthy of note that the element deactivation function in *ANSYS®* not only *zeros* the stiffness (Young's modulus) of the deactivated elements but also all other physical material properties, including CTE. In our case, the solder is the deactivated element layer during the soldering process. On either side of the deactivated solder (set to 0 ppm CTE as a result of element deactivation) is copper (from the substrate and from the baseplate) which has a high CTE of close to 17 ppm. Due to this extremely large difference in the CTE values of the two adjacent layers, high distortion is produced. This ultimately results in extremely bad element quality leading to non-convergence.

3.4.2 Baseplate warpage: A solution for convergence

In the previous section (Section 3.4.1), the underlying problem regarding the simulation of the soldering process was discussed. In this section, the solutions to these issues are explained. Each of the two problems are tackled separately and explained as such.

1. **Warpage of the substrate**
   In case the warpage is more than the initially modelled solder thickness, volume inversion of solder elements takes place and as a result, terminates the solution. This is schematically shown in Figure 3.25(a). This means the modelled initial solder thickness needs to be tailored to the warpage of each substrates. For this purpose, a warpage simulation needs to be done for stand-alone substrates as per the method provided in Section (3.3.3.3). This simulation would provide for the location and magnitude of maximum warpage. If the solder joint thickness in the FEM simulation is modelled with this thickness, i.e. the value of maximum warpage, the thickness of the solder would be zero at the location where the maximum substrate warpage occurs. This meant that the minimum solder joint thickness would have to be more than the maximum warpage of the substrate to avoid convergence problems. The question of course is - how much?

   For the AMB layout as shown in Figure 3.2 or in Figure 3.9(a) the location of maximum warpage was already known and cross sections through this location were also available (Ref. Figure 3.12). From these cross sections, it was determined that in almost all cases the thickness of solder between the baseplate and the point of maximum substrate warpage was ∼80 µm. Therefore, the convergence problems resulting in from the warpage can be solved by modelling a sufficiently thick layer of solder (= maximum substrate warpage + 80 µm)

2. **CTE of the deactivated solder**
   The deactivation of the solder layer using the ANSYS® utility EKILL (short for Element Kill), reduces not only the stiffness but also the CTE of the elements to zero. The effects of this property of EKILL and the subsequent simulative problem is shown in Figure 3.25(b). What was needed was a method to reduce the stiffness of the solder to zero but keep the CTE such that it moved along with the two adjacent joining partners as in reality, the liquid solder would comply to all small movements of the adjacent joining partners- in this case copper. For this purpose, following the EKILL command, a so called MPCHANGE (short for Material Property Change) command is used. This allows to allocate non-zero values to material properties such as CTE values. As the two adjacent layers to the solder layer are made of copper, the CTE values of the solder is temporarily set to the CTE value of copper.

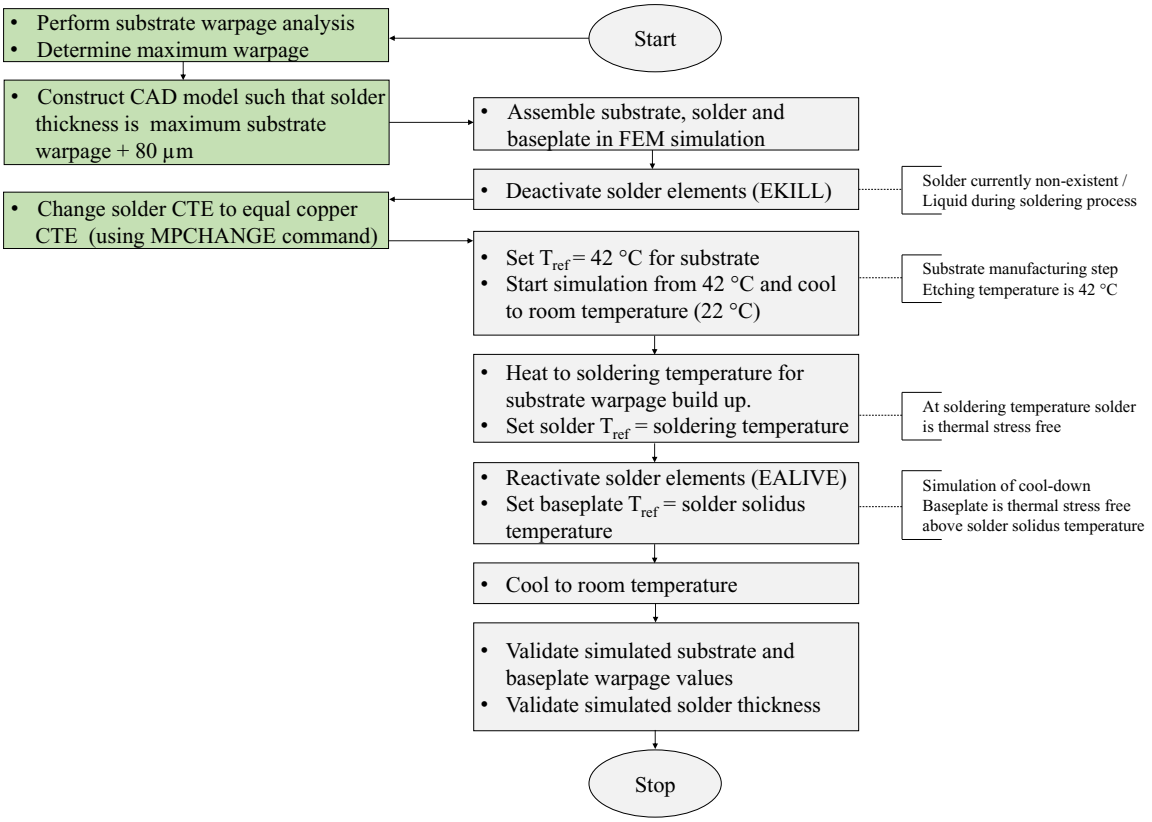


Figure 3.26: Flowchart: Modified soldering process simulation

The implementation of the changed procedure results in a stable simulation method with no convergence problems. The simulation methodology is summarized in the modified flowchart as shown in Figure 3.26.

3.5 Verification of warpage simulation

While the problems regarding the functionality of the simulation methodology mentioned in Section 3.4.2 were solved, its validity was still to be verified. For the method to be acceptable, warpage of the substrate, the baseplate and the variable thickness of the solder joint would have to be correctly predicted at room temperature in the post soldered state.

Substrates and baseplate warpage
The first verification step was done on the warpage of the substrates and the baseplate. Warpage values were measured along paths on the substrates and the baseplate as shown in Figure 3.27

The warpage measurement was done using a contact probe. As per the convention of concave and convex warpage profiles described in Section 3.2 and shown in Figure 3.1, the ends of the warpage measurement path are assumed to be at the same level; and this level is used as the reference with which the vertical displacement (warpage) at other locations is calculated/measured. Only in this case can the warpage measurement be *truly objective* and

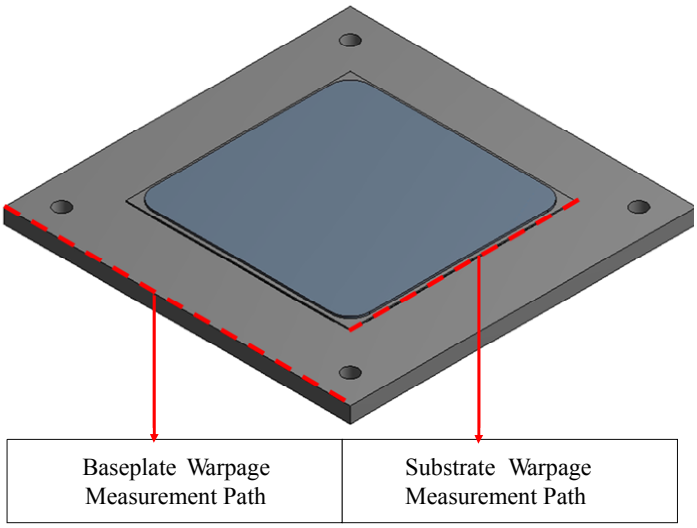


Figure 3.27: Warpage measurement path

independent of the orientation of the measured specimen. It was often seen that due to solder residues stuck to the copper baseplate during the soldering process, the complete assembly was tilted and therefore introduced a rotational measurement error as shown in Figure 3.28. To correct for this tilt, each measurement point is considered as a vector to which a rotational co-ordinate transformation according to Equation (3.4) is applied where the angle of rotation is equal and opposite to the angle of tilt. In Equation (3.4), u_i are the two components of the vector holding the measured information about the location on the substrate and the corresponding values of warpage respectively. v_i represent the same quantities as for u_i but after a rotational co-ordinate transformation through an angle θ.

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{3.4}$$

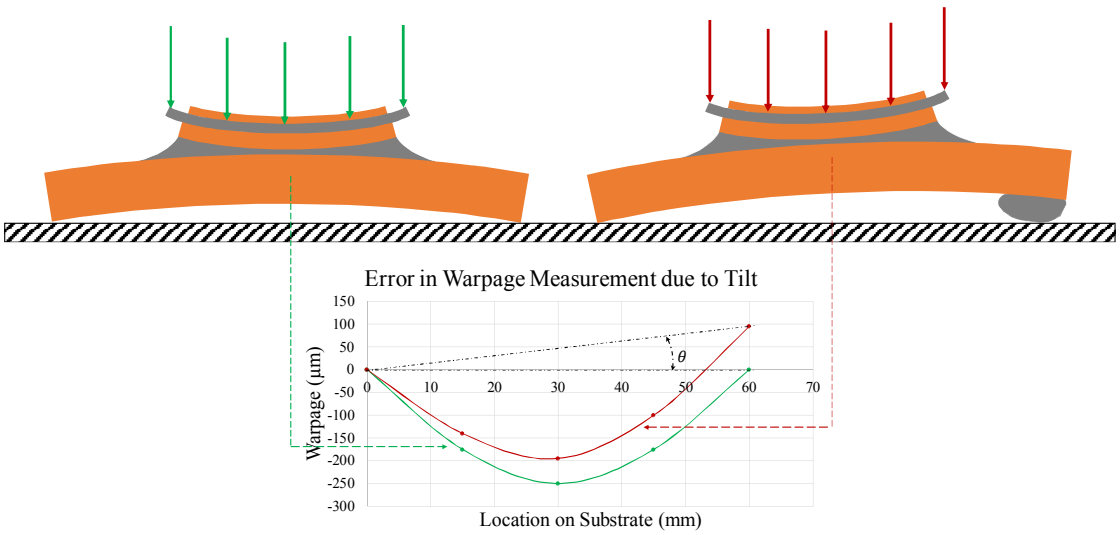


Figure 3.28: Error in warpage measurement due to tilt

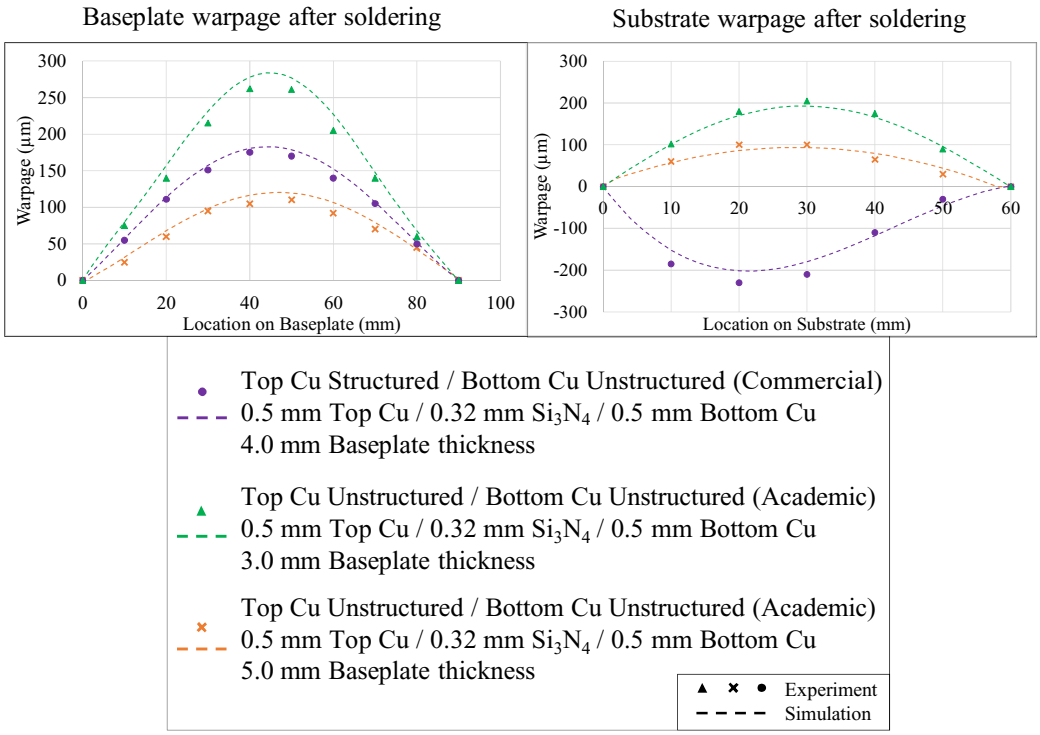


Figure 3.29: Warpage: Simulation v/s Measurement

This measurement and co-ordinate transformation method was carried out for two different variants. The first variant had a baseplate thickness of 3.0 mm and the second was 5.0 mm thick. The substrates used in both cases where unstructured and symmetric.

Figure 3.29 compares the measured warpage values (shown as distinct points) with that of simulation (shown as dotted lines). As can be clearly seen the simulation shows excellent agreement with the measured values. A point of interest is that as the substrates are symmetric, they would ideally show no warpage when not soldered. In the soldered states however, they exhibit a convexly warped shape due to the fact that the baseplate being a much more massive component, has a substantial influence on warpage after soldering. As the solder solidifies and the baseplate contracts differentially on its top and bottom sides, it pulls the substrate periphery along with it and rendering it convex. Even this effect is correctly captured in the simulative process.

Variable solder joint thickness

To verify the variable solder joint thickness, sample with a baseplate thickness of 4.0 mm and structured top side substrate layout as shown in Figure 3.9 was used. For this sample, at room temperature, in the post soldering state, the substrate was concavely warped while the baseplate was convexly warped as shown with purple circular data points in Figure 3.29. Therefore, this sample was ideal to measure the simulation's effectiveness to predict the variable solder joint (ref. Figure 3.12). Solder joint thickness from six samples of the tested variant were available. As can be seen form Figure 3.30, the simulated solder joint thickness (shown as a solid black line) lies well within the range of the measured solder thickness (shown in coloured dotted lines).

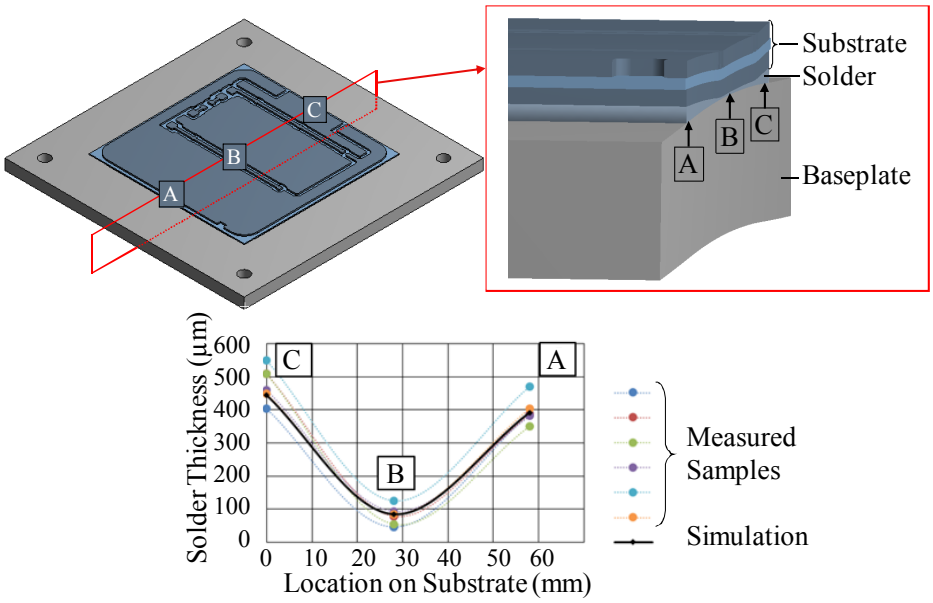


Figure 3.30: Variable solder thickness: Simulation v/s Measurement

The above two results clearly verify that the simulation procedure accurately and satisfactorily accounts for the manufacturing process of the substrate and the assembly process through soldering. This also indicates that the initial stress state of the solder is well accounted for.

3.6 Mesh dependence

Having developed a simulative method to accurately account of the manufacturing process of baseplate soldering, the only further step to make the process completely objective was to carry out a FEM mesh dependence study. It is well known that FEM models can be dependent on the density of the finite element mesh. This means that while the above mentioned simulation method accurately describes the experimental results, it could very well be possible that if the same analysis is carried out by another FEM analyst, the result could come out to be different in case the element type and size are not kept the same as in the simulation carried out in this research work.

It was therefore necessary that a verification of mesh size dependence was done. In case the results varied strongly with respect to the mesh density, a guideline would have to be issued recommending the acceptable element types and sizes for simulating the baseplate soldering process.

Major element types used in this doctoral work (and structural FEM analysis in general) are the hexahedral (HEX) and the tetrahedral (TET) elements. Each of these element types come in two element orders, linear and quadratic. As the different components in our assembly have a uniform cross section, in the case of a HEX mesh, the meshing can be done in a swept fashion and therefore the element size is varied by changing the number of elements

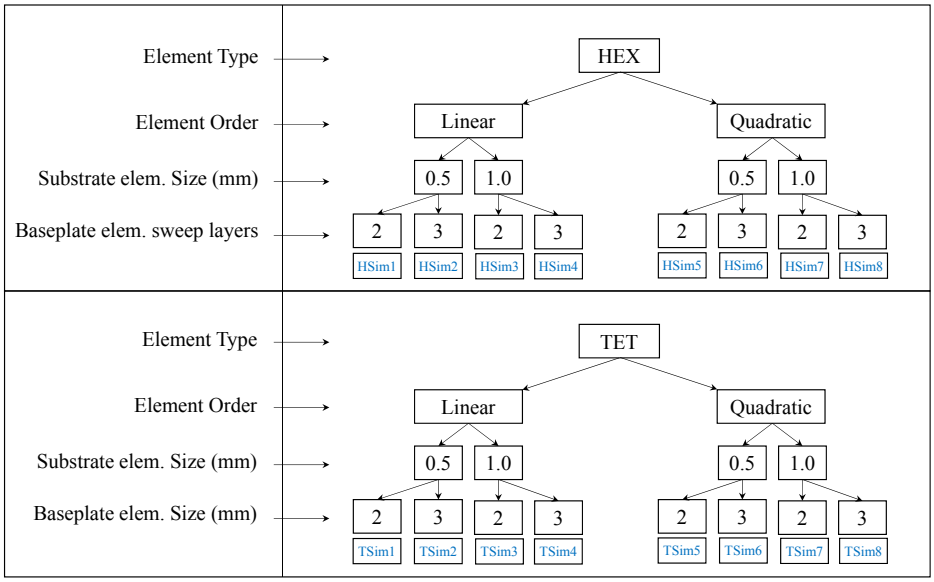


Figure 3.31: Simulated element variations for mesh sensitivity test

through the thickness. In case of a TET mesh, the element size is varied explicitly. In total 16 different combination of element type, element order and element sizes are simulated. An overview of all the variants is shown in the Figure 3.31.

For the simulated variants, the substrate and baseplate warpages and the respective computational times were noted. As can be seen from Figure 3.32, for the model with HEX elements, there is practically no mesh sensitivity at all. For example, the computationally most intensive, HSim6 with the highest element density provided practically the same results as that from HSim3, the model with the lowest element density and computational costs. This means that in case of HEX elemented models, linear elements can be chosen for simulation purposes. On the other hand, models with TET elements did show a sensitivity to mesh density when the elements are of the linear order. This is due to the fact that linear tetrahedral elements tend to be too stiff especially in bending problems. Quadratic elements however are equally capable to predict warpage without any strong mesh dependence. This means that linear TET elements should be avoided while simulating baseplate soldering.

The choice therefore is between linear HEX elements and quadratic TET elements. In general, quadratic TET elements, as seen in Figure 3.31, require longer computational time. They also are more difficult to post process for extraction of stress or strain results from the FEM simulation. As a result, for the further development of the FEM method to include reliability and lifetime modelling topics, element configuration from HSim3 as referenced in Figure 3.31.

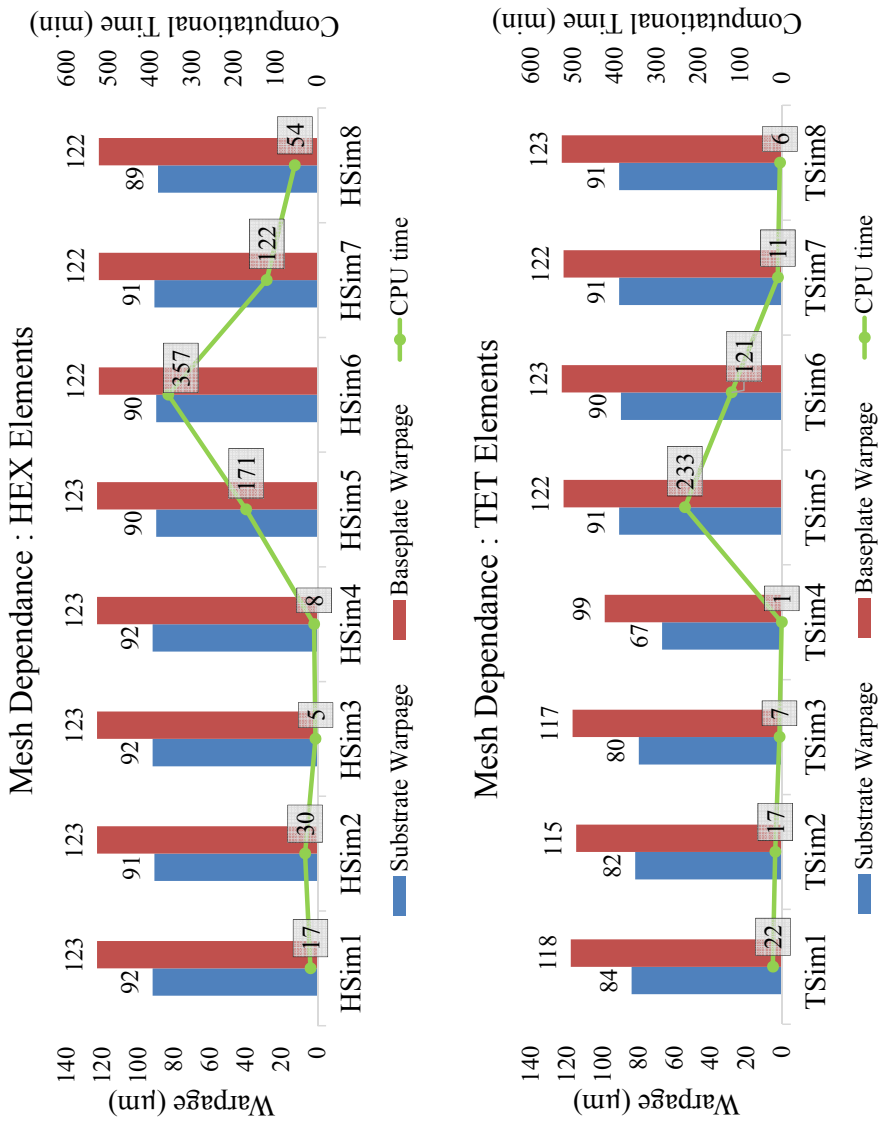


Figure 3.32: Mesh sensitivity results

It has long been an axiom of mine that the little things are infinitely the most important.

Arthur Conan Doyle (1859 – 1930)
British literary author

Chapter 4

IMC Growth and Solder Joint Reliability

4.1 Introduction and motivation

One of the major goals of this study on the reliability of baseplate soldering was to derive a satisfactory simulative (FEM) lifetime model with which the number of thermal cycles to failure could be predicted. Chapter 1 mentioned that unlike conventional solder joints such as in BGA, WLP or QFP components where the crack is found to grow predominantly within the bulk of the solder, baseplate soldered components show cracks at/near the interface of the solder and the substrate, specifically at/near the interface between the solder and the IMC layer on the substrate side of the joint.

In lead free solders, interface cracks between the solder and IMC have been encountered in many cases. IMC related fractures are produced under temperature cycling [RVD04], mechanical shock [BS05; MK05; Hea+05] and vibration [Tu+01]. [YZ13] studied the tensile strength of solder joint with increasing IMC thickness and concluded that the strength of solder joint decreased with the growth in the IMC layer. Similar conclusions were drawn in the study done by [Tu+01], wherein, it was also shown that cyclic bending and vibrational fatigue lifetime considerably decreased with increasing IMC layer thickness. For the sake of completeness, a few more studies are enlisted that infer a reduction in reliability of solder joints with increasing IMC layer thickness [Lee+03; Ma+09; XXF08; Cra11].

As a consequence, it is useful to have a method to predict the rate of growth of the IMC layer and consequently its thickness in solder joints. It is therefore not surprising that a significant amount of research work has been carried out in this regard. [CL00] investigated the thickness increase of the solder joints by varying the hold time at peak temperature during the soldering stage and thereafter further ageing the components at 130 °C for up to 800 hours. To investigate dynamic performance of lead free solder joints, [Ma+09] also studied IMC growth under isothermal conditions of 75 °C, 100 °C and 150 °C. In a related study on the effects of surface finish roughness on IMC Growth, [Rod+10] also conducted isothermal ageing of solder joints. Similar work was also conducted by [XXF08] and [Yu+05]. All the above studies concluded that the thickness of the IMC grows proportional to the square root of ageing time and the rate of growth increases with increasing ageing temperature. In

addition to ageing time and ageing temperature, [Ais+13] cited soldering profile as a factor wherein different soldering profiles can produce different IMC grains structures which in turn, can affect the growth rate of the IMC layer under thermal ageing.

Despite the experimental consensus on the detrimental influence of IMC thickness on reliability, from an FEM perspective, modelling of solder joints is almost always carried out *without* including the IMC layer. This is done under the assumption that the IMC contributes very little to the structural behaviour of the entire assembly and consequently has little effect on thermomechanical reliability. A recommendation against this trend was provided in the study [PFG16], where it was argued that IMC layers should be modelled in the FEM simulations. [BKT09] showed that the crack growth fronts are influenced by the solder/IMC interface and argues for the inclusion of the IMC interface in FEM simulations.

It can be thus concluded that although a considerable amount of research has been carried out regarding IMC growth and its influence on reliability of solder joints, there are gaps in understanding as listed below.

1. **Ageing conditions:** Most studies that investigate the growth of the IMC layer thickness (for example the ones mentioned above [CL00; Ma+09; Rod+10; XXF08]), investigate IMC growth under isothermal ageing conditions. Studies that consider non-isothermal conditions, report the thickness after a given number of cycles but no method to predict it. A straight forward method to estimate IMC thickness under non-isothermal conditions such as temperature cycling or any other arbitrary thermal profile, for example as logged under an active power cycling test was not available.

2. **Solder alloy:** Innolot, the solder alloy considered in this work is relatively less investigated compared to more popular solders such as SAC305. None of the studies mentioned above have investigated Innolot. Solder alloy elements could have a distinct effect on the growth of the IMC layer as previously discussed and therefore needs to be investigated separately.

3. **Solder joint size:** IMC growth studies (as cited before) were carried out exclusively on solder joints in BGA, WLP or QFP components where the solder joint size is in the micrometre scale with the cross sectional height (also called solder standoff) and length of the joint being of roughly the same size. That is, the aspect ratio as seen in cross sections is roughly 1. In this research work, while the bondline thickness (height as seen in cross sections) are a few hundred micrometres, the bondline length (span of the solder joint as seen in cross sections) is in the order of tens of millimetres. In fact, the smallest aspect ratio investigated in this work is 100. The solder joint size in the application investigated in this research work are orders of magnitude larger for which no comparable investigation is available.

4. **FEM analysis:** There is also no decisive consensus on whether the IMC layer should be modelled in the FEM analysis. While most models are built without it, a few investigations, as previously discussed suggest the contrary. This question therefore, also needs to be resolved.

To fill these gaps, this chapter first provides a method to transfer IMC growth data from isothermal ageing conditions to any arbitrary thermal profile. The investigation is done with Innolot as the soldering alloy and solder joints span an area of approximately 56 mm x 56 mm with a thickness of about 300 µm. In addition to this, an FEM based analysis is also carried

out to provided a conclusive answer to whether modelling an IMC layer in the FEM model has a sizeable impact on potential simulative damage parameters. A partial or abridged version of contents discussed in this chapter may also be found in [Geo+17] (©2017 IEEE).

4.2 Experimental investigation and IMC growth calculation

The experimental investigations carried out in this study consisted of four major steps. First was the creation of different soldering profiles within process relevant limits. Second was the build-up of samples and the isothermal ageing of the samples under different high temperatures and ageing durations. Third was the measurement of the IMC layer of samples aged under the aforementioned ageing conditions. Lastly, from the IMC thickness values obtained, a mathematical methodology was derived to transfer isothermal growth results to non-isothermal cases such as temperature cycling. This result was also partly used in FEM simulations to model TC relevant IMC thicknesses and analyse its impact on reliability indicating damage parameters.

4.2.1 Soldering profiles and thermal ageing

As cited in the previous section, soldering profile could potentially have an impact on the rate of growth of the IMC thickness. To investigate this, four different temperature profiles where investigated. The variation parameters in the soldering profile were the cooling rate (high or low) and the hold time (standard or extended) at peak temperature. These were aimed at providing different initial conditions in the solder grain structure with the intention to influence the IMC growth rate. Table 4.1 summarizes the soldering profiles that were used to build up the samples.

Table 4.1: Soldering profile used to build up test samples

Profile characteristics	**Profile name**	**Hold Time (s)**	**Cooling rate (°C/s)**
Hold time: Standard Cooling rate: High	ST_H	140	0.5
Hold time: Standard Cooling rate: Low	ST_L	140	0.3
Hold time: Extended Cooling rate: High	EX_H	185	0.5
Hold time: Extended Cooling rate: Low	EX_L	185	0.3

In order to ensure that the correct temperature values were encountered on the built up samples, thermocouples were placed between the substrate and the baseplate at three locations (corner, centre and edge mid-point) as shown in the Figure 4.1. This set-up would help to give an indication if the entire assembly was uniformly heated without any localised hotspots. The readouts from the thermocouples affirmed that the samples were uniformly heated during the soldering step and also that there was satisfactory match between the required soldering profile parameters as mentioned in Table 4.1 (hold time at peak temperature and the rate of cooling).

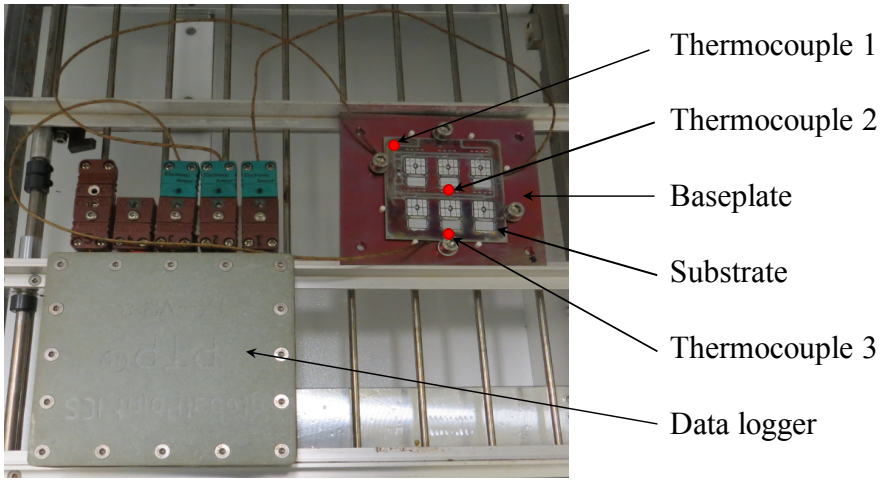


Figure 4.1: Setup for calibration of soldering profile

Once the samples are built up, they are aged under three isothermal temperature conditions *viz.* 125 °C, 150 °C and 175 °C. Samples are taken out for IMC thickness measurement after 0 hours (initial), 200, 500 and 1000 hours of high temperature ageing respectively.

4.2.2 IMC thickness measurements

The IMC layer thickness was measured through cross sections using an optical microscope. For each sample, measurement was done at 20 locations on the solder joint. The measurement of the IMC layer thickness offers a challenge due to its irregular morphology. As a result, an average/equivalent layer thickness was sought.

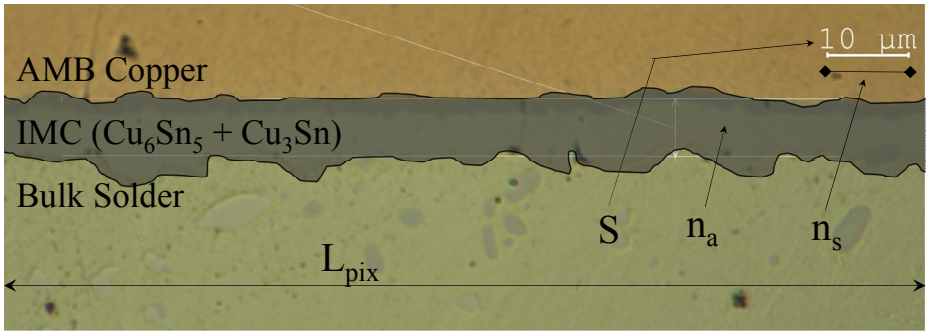


Figure 4.2: IMC thickness measurement [Geo+17]. Trace precipitates from other alloying metals such as Nickel, Antimony and Bismuth are ignored and not shown.

As shown in Figure 4.2, for each image obtained from the microscope, a scale is available showing the dimensions in physical units (S µm). The length of the scale in pixels was also available (n_s). This means that a conversion factor K from the physical dimensions to pixels and vice versa can always be calculated as per the Equation (4.1).

$$K = \frac{S}{n_s} \, (\mu m/pixel) \tag{4.1}$$

The total area occupied by the IMC layer in the microscope image was obtained (n_a in pixels) through a simple image processing software. Consequently, one only needs to divide the IMC area by the length of the image (L_{pix} also in pixel) to obtain the average/equivalent thickness of the IMC layer (in pixels). As the last step the conversion factor from Equation (4.1) is used to obtain the thickness in physical units (h µm) as shown in Equation (4.2).

$$h = \frac{n_a}{L_{pix}} \cdot K\,(\mu m) \tag{4.2}$$

4.2.3 IMC growth results and its mathematical description

Isothermal ageing

It can be noted that directly after soldering, the IMC thickness in all samples was comparable, lying between (2.1 to 3.3 µm). Despite ageing for 1000 hours at 175 °C, the largest difference between the average IMC layer thickness between samples soldered with different soldering profiles was only 1.8 µm. This can be seen in Figure 4.3 which shows the growth of the IMC layer in samples soldered using the four soldering profiles and aged under three ageing temperatures. It can be inferred that at least within the variation limits, soldering profile only had a minor influence on the growth of the IMC layer.

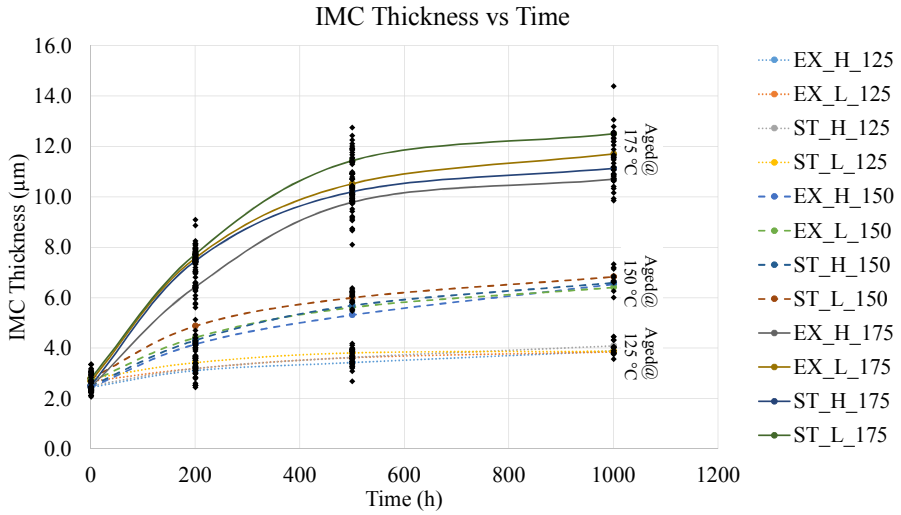


Figure 4.3: IMC layer growth with respect to temperature and ageing duration

The major influence parameters as seen in Figure 4.3 are ageing temperature and duration. This result is consistent with previously published literature. Time dependence is modelled using a parabolic power law with respect to time as shown in Equation (4.3) where h and h_0 are the IMC thickness at initial condition and after isothermal ageing for time t. A is the Arrhenius reaction rate constant.

$$h = h_0 + A\sqrt{t} \tag{4.3}$$

[Tu+01] showed that the plot of IMC thickness versus the square root of time is a straight line and [VRH04] confirmed this result by calculating the time exponents for the two IMC phases to be 0.56 and 0.54 (practically identical) for Cu_3Sn and Cu_6Sn_5 respectively. This meant that, to describe the overall growth of the IMC layer, two separate equation were not

required to be derived. Instead, Equation (4.3) would be sufficient where A would represent an equivalent Arrhenius constant for both layers taken together.

Depending on the dominant contributing IMC growth mechanism, which could be lattice diffusion, interfacial reaction, grain ripening etc., [SFL98], [KT96], [Ehr17] and [PPL04] suggest that the ageing exponent of t could however differ from 0.5, which is the case in Equation (4.3). To keep into account this effect and for the sake of generality, the $\sqrt{t}$ term is replaced with an ageing exponent n thus modifying Equation (4.3) to Equation (4.4).

Temperature dependence is accounted for by an Arrhenius term A in growth equation

$$h = h_0 + At^n \tag{4.4}$$

$$A = A_{sc} \exp(-\frac{\Delta H}{RT}) \tag{4.5}$$

where A_{sc} is an Arrhenius scaling factor, T is the absolute temperature in Kelvin, R is the universal gas constant (= 8.314 J / (mol.K)) and ΔH is the activation energy in (J/mol). To verify if the growth results from this study was valid to be modelled using Equations (4.4) and (4.5), linear regression (least squared error fit) was carried out on average IMC thickness values for each soldering profile and ageing temperature and A_0 and the ageing exponent n were determined. Fitted curves are shown in Figure 4.4. From these curves, n, ΔH and A_{sc} can be determined and are tabulated in Table 4.2.

Table 4.2: Time exponent and Arrhenius parameters for IMC growth with respect to different soldering profiles

Profile name	$\boldsymbol{n}$	$\boldsymbol{\Delta H}$	$\boldsymbol{A_{sc}}$
ST_H	0.503	53967.56	579278.31
ST_L	0.508	49556.65	183121.68
EX_H	0.506	51953.60	309395.05
EX_L	0.506	50795.62	242359.80

Extension to non-isothermal ageing conditions
A major limitation of Equation (4.4) is that it describes the growth of the IMC layer only under isothermal conditions as t is the ageing duration under constant temperature. For a non-isothermal condition such as temperature cycling, the IMC layer grows at different rates at different temperatures and also the time spent at those temperatures can be arbitrarily different. To extend the applicability of this equation to non-isothermal conditions, the direct dependence on ageing duration needs to be modified. This is done by first differentiating Equation (4.4) with respect to time. This gives us the Equation (4.6).

$$\dot{h} = nAt^{n-1} = \frac{nAt^n}{t} \tag{4.6}$$

From Equation (4.4), t^n and t can be expressed as

$$t^n = \left[\frac{h - h_0}{A}\right] \qquad \Rightarrow \qquad t = \left[\frac{h - h_0}{A}\right]^{\frac{1}{n}} \tag{4.7}$$

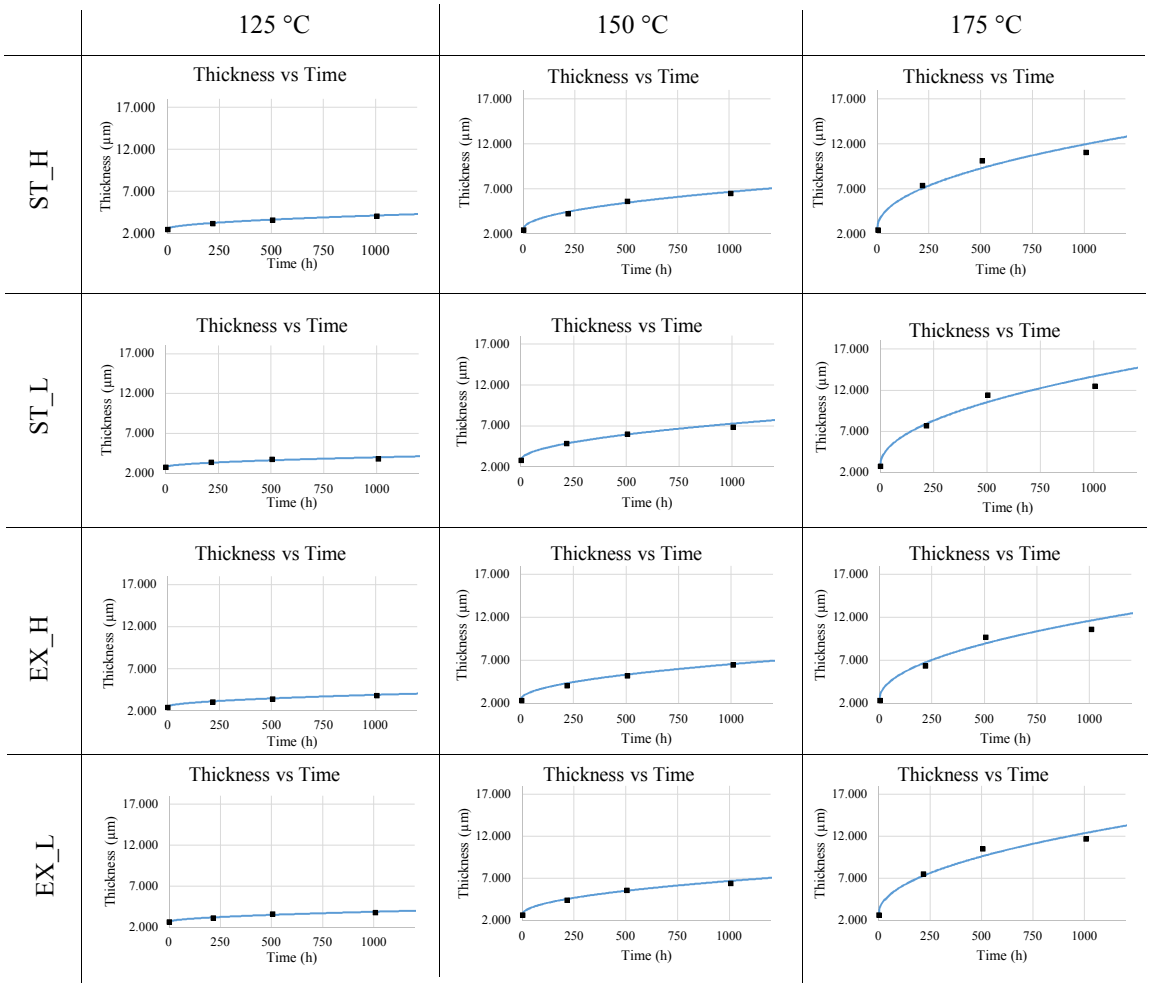


Figure 4.4: IMC thickness fitted to curves as in Equations (4.4) and (4.5)

Equation (4.7) is now used in Equation (4.6) to yield

$$\dot{h} = \frac{nA}{\left[\frac{h - h_0}{A}\right]\left(\frac{1-n}{n}\right)} \tag{4.8}$$

It is to be noted that Equation (4.8) expresses IMC growth rate in terms of the initial and current IMC thickness instead of the ageing duration. Larger the IMC thickness slower the growth rate of the IMC layer which is the behaviour as shown in Figures 4.3 and 4.4. From first principles of differential calculus, the differential Equation (4.8) can be discretized and written in the finite forward difference format (also called the forward Euler method [Eul68]) as shown in Equation (4.9)

$$\lim_{(t_{i+1}-t_i)\to 0} \frac{h_{i+1}-h_i}{t_{i+1}-t_i} = \frac{nA_i}{\left[\frac{h_i-h_0}{A_i}\right]\left(\frac{1-n}{n}\right)} \tag{4.9}$$

$$h_{i+1} = h_i + \frac{nA_i}{\left[\frac{h_i-h_0}{A_i}\right]\left(\frac{1-n}{n}\right)} \cdot (t_{i+1}-t_i)$$

For the calculation of IMC thickness during a non-isothermal process *e.g.* Temperature Cycling (TC), the entire cycle can be split up into many small time steps. From the TC profile, the temperature at any given time can be read out and the Arrhenius growth rate term can be calculated (ref. Figure 4.5, Equation (4.5) and table 4.2). h_0 and n are known from experimental measurement (ref. Figure 4.3) and linear regression (ref. Figure 4.4, table 4.2). $(t_{i+1}-t_i)$ is predefined depending on the number of time splits made in the TC profile (higher the number of splits, higher the accuracy of the thickness prediction and higher the computational time). h_i (current IMC thickness) is always known from $i-th$ step of Equation (4.9). This means that the new IMC thickness at each time step $i+1$ (*i.e.* left hand side of Equation (4.9)), is explicitly expressed as the right hand side which contain terms from the $i-th$ step.

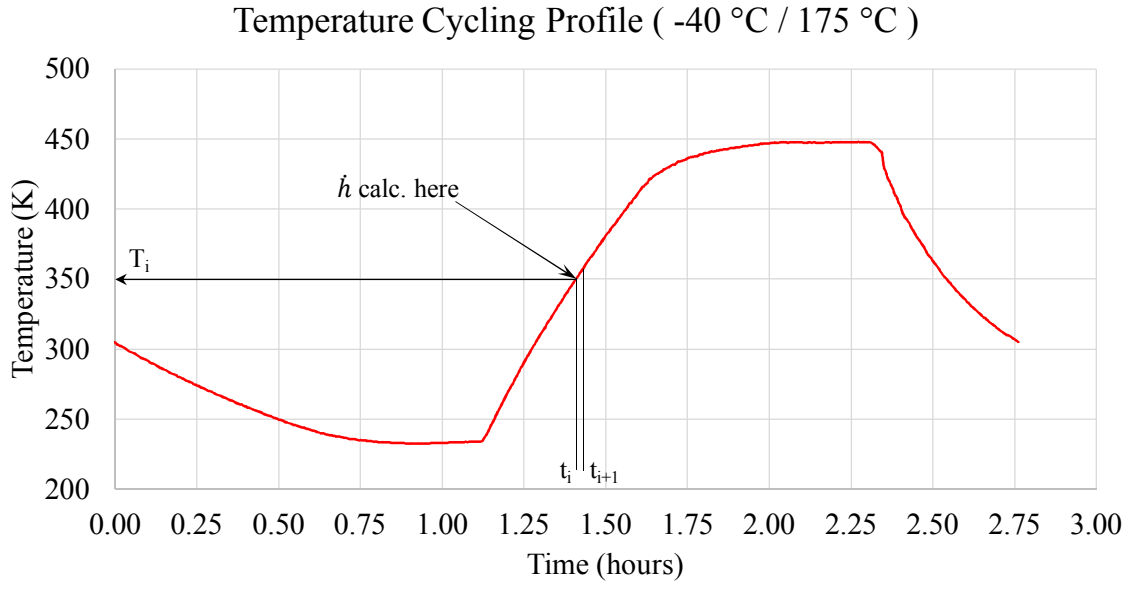


Figure 4.5: Example IMC growth rate calculation from TC profile

The above mentioned procedure was implemented using a MATLAB® script (ref. Appendix B). Figure 4.6 shows the growth of the IMC layer with increasing number of TCs (For this calculation it was assumed that the ST_H soldering profile was used as this is the standard soldering profile use for many applications where Innolot is used as a soldering alloy). It can be clearly seen that on the scale of each individual TC, the IMC grows slowly at low temperatures and faster at elevated temperatures and that the growth slows down with increasing IMC thickness.

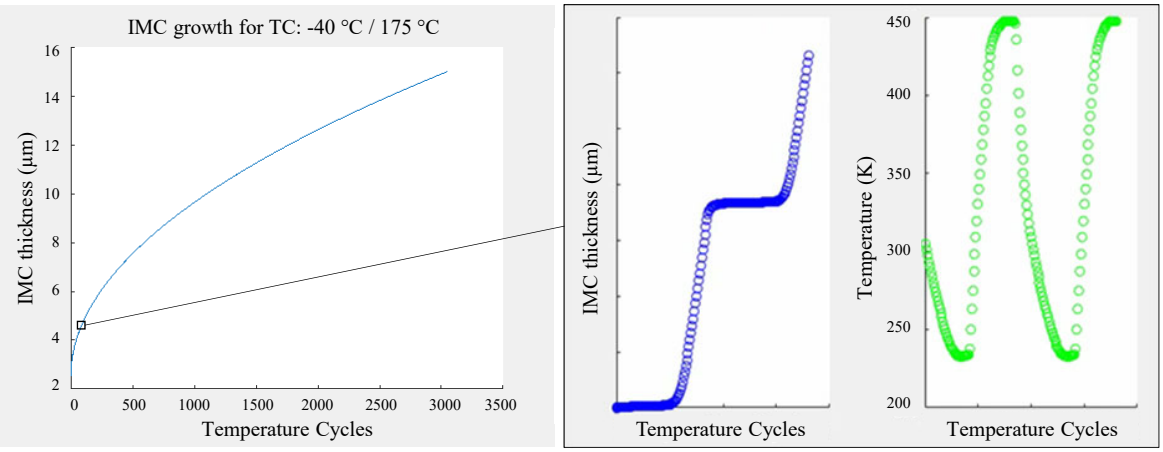


Figure 4.6: IMC layer thickness increase with temperature cycling

To verify the methodology for the prediction of IMC thickness, two samples were chosen that were soldered using the soldering profile ST_H and aged under -40 °C / 150 °C and -40 °C / 175 °C for 2000 and 1000 cycles each. Hold time at extremum temperatures in both TC profiles was 30 minutes each. The prediction and measurement as tabulated in Table 4.3 showed excellent agreement.

Table 4.3: IMC thickness prediction under temperature cycles compared to measurements

Solder alloy	Innolot	Innolot
Soldering profile	ST_H	ST_H
TC profile	-40 °C / 150 °C (2000 TC)	-40 °C / 175 °C (1000 TC)
Predicted IMC thickness	6.213 µm	9.635 µm
Measured IMC thickness	6.287 µm	9.546 µm
Prediction error	1.1%	0.9%

4.3 Simulative study of influence on reliability

One of the motivations of this study as mentioned in Section 4.1 was to simulatively understand the effect of IMC thickness on the reliability of solder joints. Additionally, there is also no consensus on whether the IMC layer must indeed be included during the FEM analysis. Both these issues are dealt with in the following sections.

4.3.1 FEM modelling

Samples investigated in the simulative study have a baseplate that is 200 mm x 90 mm in lateral dimension and is 4 mm thick. The substrates have a lateral size of ∼58 mm x 58 mm. Due to symmetry, a quarter 3D model was constructed to save computational time. As delamination of solder in baseplate soldered components starts at the corners of the solder joint, solder joint corners constituted the major area of interest. For these regions the *sub-modelling* or the *cut-boundary displacement* technique is used. It is based on the St. Venant's Principle [Lov13; Sai56; Inc16a] which states that *"...if an actual distribution of forces is replaced by a statically equivalent system, the distribution of stress and strain is altered only near the regions of load application. The principle implies that stress concentration effects are localized around the concentration; therefore, if the boundaries of the submodel are far enough away from the stress concentration, reasonably accurate results can be calculated in the submodel."*

This idea is used in FEM simulations involving sub-modelling. In this method, first a coarse FEM mesh is created for the entire geometry and the model is solved for displacements. A sub-model (containing the area of interest) is then cut out from the coarse model and displacement results from the coarse model is placed as boundary conditions on the sub-model. The sub-model can be modelled with a much finer mesh mostly leading to more accurate results. The method is schematically shown in Figure 4.7.

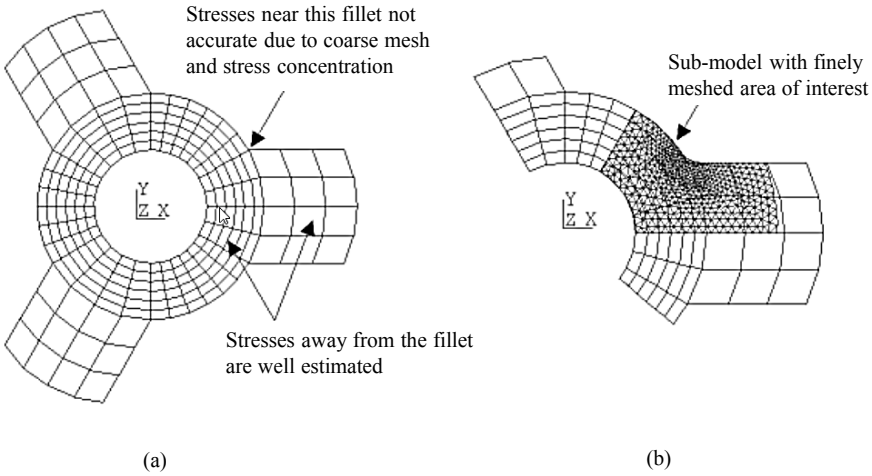


Figure 4.7: Schematic representation of the submodelling method [Inc16a]

4.3.1.1 Geometry, warpage and failure mode

For investigation in this study, three substrate geometries and corresponding warpage conditions are considered- convex, concave and planar (3.3.1). The motivation behind investigating the three warpage conditions is that in the case of concave warpage (thicker bottom side copper), a crack opening mode is encountered during the high temperature region of the temperature cycle which is where creep effects are also dominant due to high homologous temperature. In case of convex warpage, the crack opening mode is encountered during the low temperature region of the TC profile which makes it susceptible to brittle cracking. Planar substrates do not show any warpage during temperature cycling, but in plane thermal expansion and contraction are present anyway leading to in-plane shear stresses. It thus makes sense to investigate all the three warpage cases independently.

Table 4.4: Investigated substrate copper thicknesses and corresponding warpage behaviour

S. No	Top Cu thickness	Bottom Cu thickness	Warp. at high temperature
1	0.3 mm	0.5 mm	Concave
2	0.5 mm	0.3 mm	Convex
3	0.5 mm	0.5 mm	Planar

The substrates are unetched and the warpages are induced by modelling unequal thicknesses of the copper layer in the AMB substrate. The different thicknesses and their warpage characteristics are tabulated in Table 4.4. For all three warpage conditions, IMC layer was introduced in the sub-model. Five such sub-models were created for each warpage case. IMC thicknesses of 0 µm, 6 µm, 8 µm, 10 µm and 13 µm were modelled. These correspond to IMC thicknesses as seen after 0, 250, 600, 1000 and 2000 cycles under the -40 °C / 175 °C TC profile respectively as calculated from the method described in section 4.2.3. The full and submodel of one of the samples is shown in Figure 4.8.

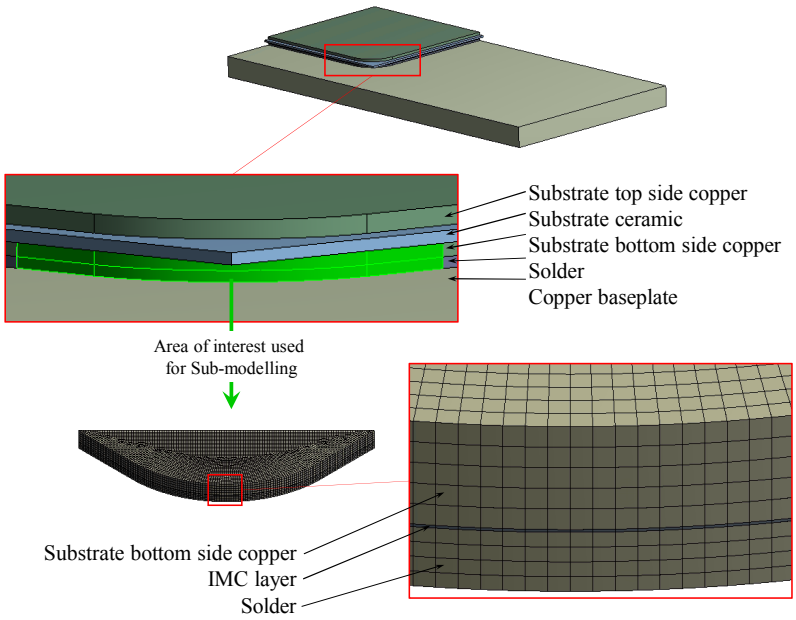


Figure 4.8: Full and sub-models used for this study

4.3.1.2 Loading, boundary conditions and materials

Loading is applied to the model in the form of temperature. Just as in the case with temperature cycling, the model is subjected to uniform temperature change cycling between -40 °C and 175 °C. The temperature ramp and hold time at extremum temperatures are kept at 30 minutes each. As a quarter model is built up, symmetry boundary conditions are applied on the respective symmetry planes. For the model to be statically determinate, a "fixed" or zero displacement boundary condition also needs to be provided. This is provided at one point along the line of intersection of the two orthogonal symmetry planes. These loading and boundary conditions are shown in Figure 4.9 for clarity of understanding.

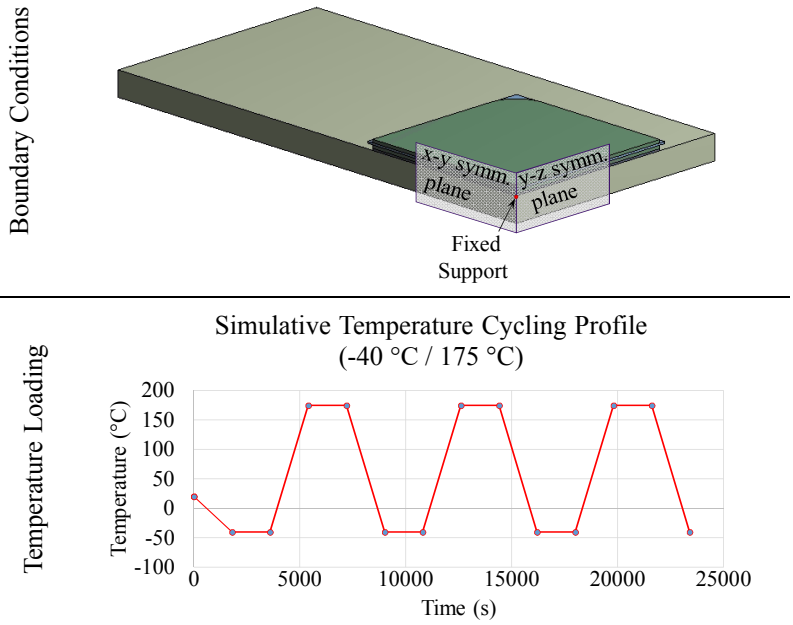


Figure 4.9: Loading and boundary conditions of the FEM model

Material properties used for the simulations are summarized in Table 4.5. IMC material properties are taken as the average value from different literature sources as compiled by [Häs06]. The IMC material has a yield point that is much higher than that of solder, i.e. the solder would degrade much earlier than when the IMC layer starts to plastify. As a result, linear elastic material properties are considered sufficient for the IMC material.

Table 4.5: Material models used for FEM simulation to assess influence of IMC layer

Material	**Material model**	**CTE**
AMB copper	Chaboche plasticity with isotropic hardening	Temperature dependent
Si_3N_4	Linear elastic	Temperature dependent
Solder	Chaboche plasticity with exponential visco-hardening	Temperature dependent
Baseplate copper	Multilinear kinematic hardening	Temperature dependent
IMC	Linear elastic	Constant

Considering the fact that IMC layers are very thin, it was worth examining if crystal orientation of IMC grain would play a role in material properties. Doctoral work [Cho16] showed that mechanical properties such as elastic modulus, yield strength and hardness were effectively independent of crystal orientation for Sn-Cu IMCs. Additionally, [CP12] showed that as the elastic modulus of the IMC was already very high compared to solder and therefore variations in the elastic modulus of IMC had a relatively low influence on the damage in the solder. This justified the use of an averaged (between the two IMC phases) material property for the IMC layer as the idealisation of two IMC layers as one layer simplifies the model geometry and also make the simulation more numerically stable.

4.3.2 Simulative Results

To evaluate the influence of IMC layer and its thickness on reliability on solder joints four damage parameters are evaluated. The details about their evaluation and the reason behind their selection is tabulated in Table 4.6.

Table 4.6: Damage parameters considered to evaluate IMC influence

Damage Parameter	**Evaluation details**	**Reason for Evaluation**
Normal stress	Range over last TC	Indicator of Mode 1 crack (refer [Roy01] for crack modes)
Shear stress	Range over last TC	Indicator of Mode 2 crack (refer [Roy01] for crack modes)
Stress triaxiality	Maximum +ve values over last TC	Indicator of increasing brittle material response
Inelastic strain	Range over last TC	Indicator of plastic damage in solder

These damage parameters are evaluated on individual elements- one element in each element layer as shown in Figure 4.10. The results from the simulation are divided into two sections. The first section (Section 4.3.2.1) shows the influence of IMC layer thickness under different warpage scenarios. The second section (Section 4.3.2.2) presents the extent of influence of the IMC layer *i.e.* the influence of the IMC layer thickness with increasing distance from the IMC layer itself.

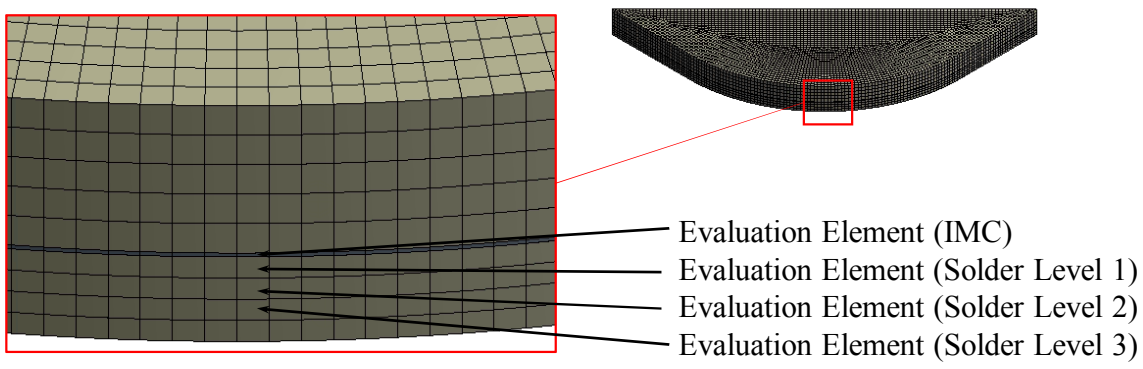


Figure 4.10: Element over which the damage parameters are evaluated

4.3.2.1 IMC influence under different warpage scenarios

This section examines the behaviour of various damage indicators (Table 4.6) with increasing IMC layer thickness for all three warpage scenarios. They are graphically shown in Figure 4.11 from which three observations can be made.

1. FEM models clearly show that in almost all cases increasing IMC layer thickness results in an increment in the values of the damage indicators. Especially in the case of IMC elements, this increment also attains no saturating value and therefore mandates the explicit modelling of the IMC layer in FEM models.

2. Damage parameters corresponding to IMC layer element shows higher sensitivity to IMC thickness increase as compared to the solder layer elements. The solder layer element shows a jump in the damage value when the IMC layer is introduced but further increase of IMC thickness results in only minor increment of the damage parameter. This is a result of the material model used for the solder layer which is a non-linear plasticity model. In such a case, after yield, the increase in stress based damage parameters is relatively low. This reasoning is further supported by the fact that plastic strain values still remain sensitive to IMC layer thickness.

3. On the basis of the damage values obtained from the IMC element, a comparison can be made between the three possible warpage scenarios. For all the damage parameters, that is, range of normal stress, range of shear stress and TF, the models with concave warpage exhibited the highest percentage increase in damage values while convex warpage models resulted in the lowest. Inelastic strain in the solder element showed the same trend as the IMC element with regard to percentage increase of damage parameter.

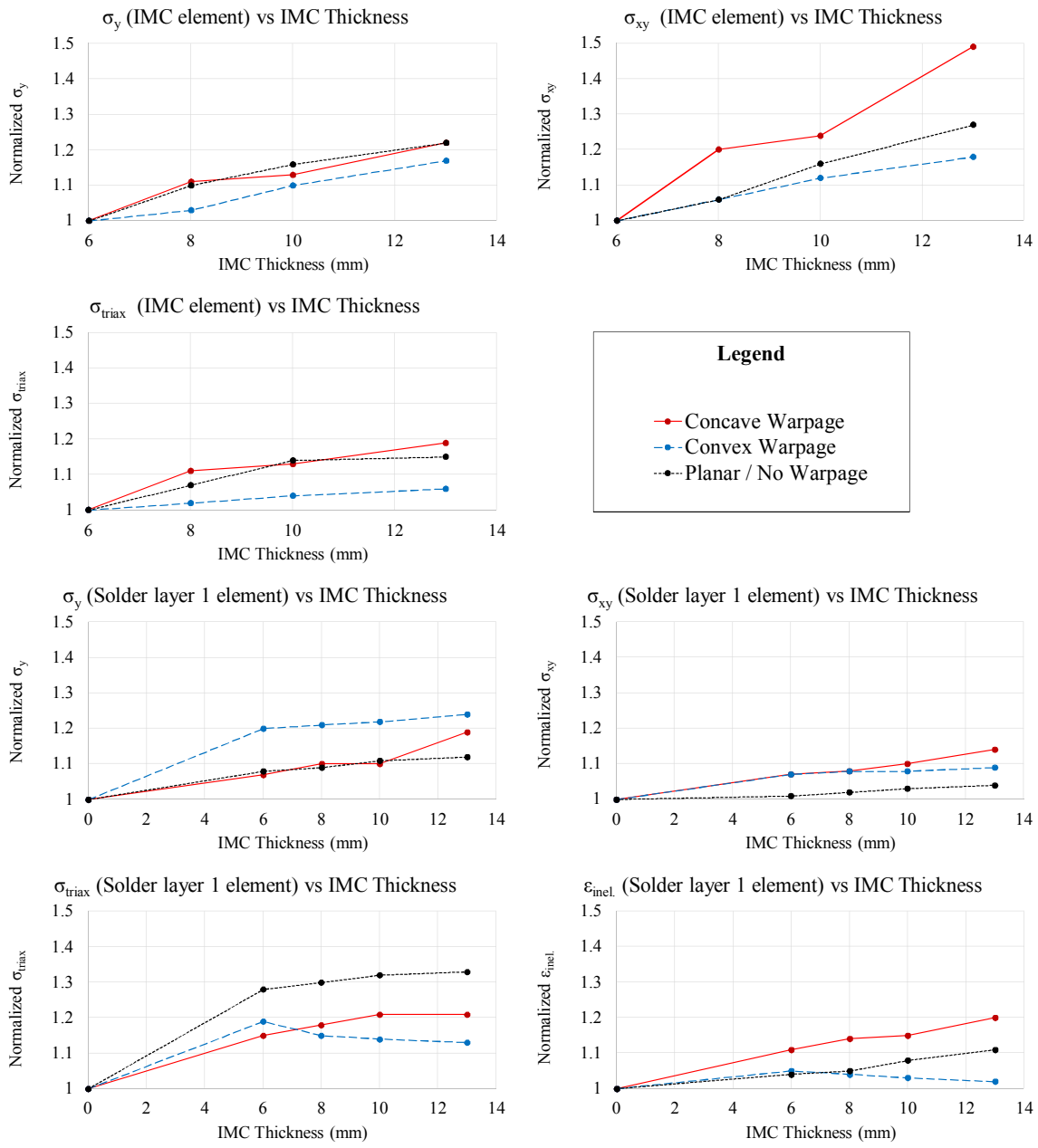


Figure 4.11: Normalised damage parameters in IMC and solder elements for different warpage scenarios

4.3.2.2 Extent of IMC influence within solder layer

Section 4.3.2.1 showed that concave and planar warpage substrates showed the greatest sensitivity to IMC thickness. These two variants were further investigated to find out as to how deep into the solder the influence of the IMC layer extended. For the case with 13 µm IMC layer, Figure 4.12 shows the plot of different normalised damage parameters in three element layers of solder - each layer progressively more distant from the IMC layer. The normalisation is done around the damage parameter values obtained when no IMC layer was present.

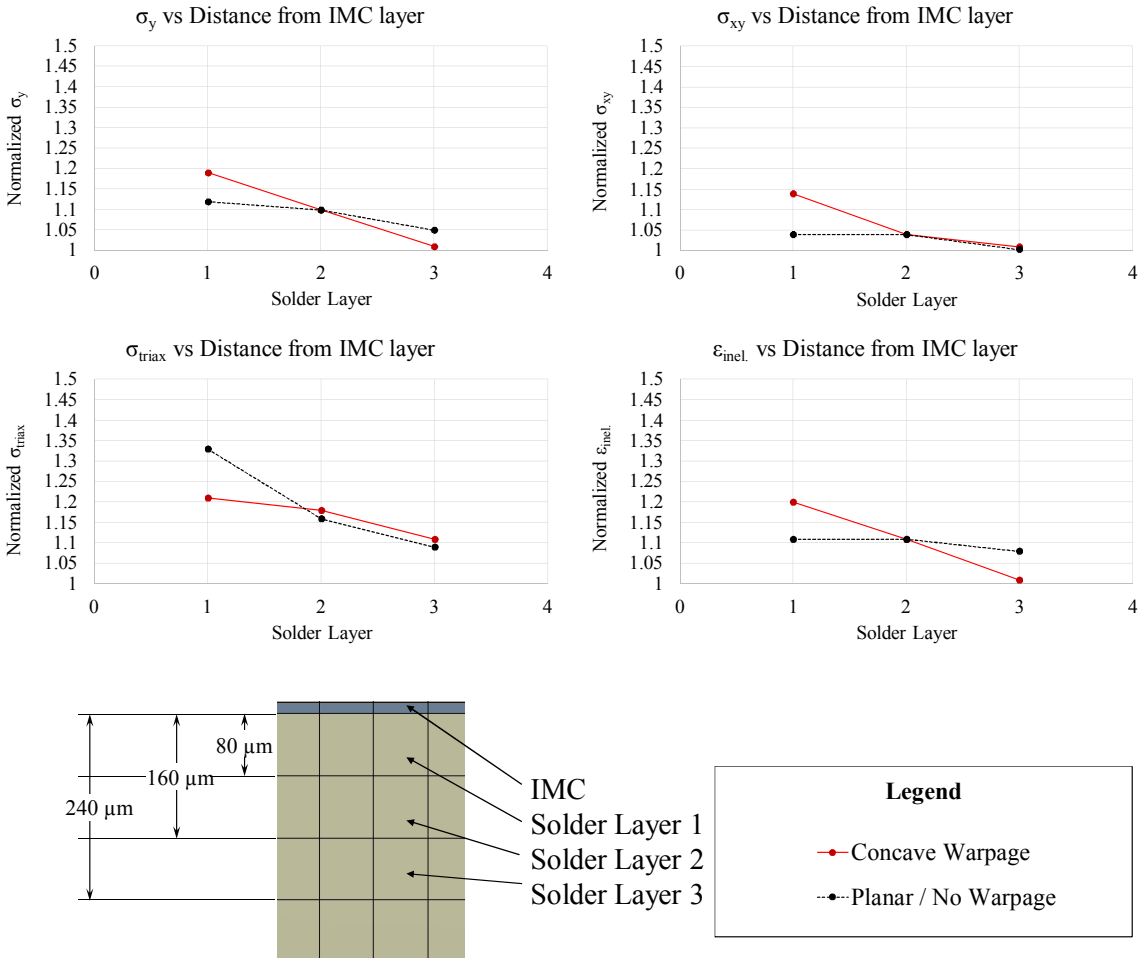


Figure 4.12: Normalised damage parameters at different solder layers (increasing distance from IMC layer)

Taking the example of normalized σ_y, as can be seen from Figure 4.12, the increase in the σ_y value in the first solder layer when a 13 µm IMC layer is introduced is about 20%. The corresponding increase in the second IMC layer is about 10% and the third layer of solder practically not influenced at all. The same trend is seen for all other damage parameters as well. This suggests that the influence of the IMC layer decreases as we move further away from the IMC layer.

From a simulative perspective therefore, it can be inferred that for failure mechanisms where the crack progresses in the bulk of the solder, the explicit modelling of the IMC layer is not necessary as the stress state in the bulk solder is only negligibly affected. On the other hand, in cases where the crack is interfacial (IMC-solder interface) or very closed to the interface, IMC layer should be modelled in the FEM simulation as the interface or the region of close proximity to the interface represents are region where there is a strong influence of the IMC layer.

An experiment is a question which science poses to Nature and a measurement is the recording of Nature's answer.

Max Planck (1803 – 1882)
German physicist

Chapter 5

Reliability Investigation

5.1 Introduction and goals of the investigation

In the case of power module based inverter units, depending on the kind of application, such as in automotive, traction or wind energy, the amount of power converted could range across six orders of magnitude. Due to the wide range of applications, such inverter units comprising PE modules and baseplate are designed in a large variety of physical dimensions. Consequently, their behaviour during soldering and reliability tests such as temperature cycling could also potentially vary to a great extent. These could be different failure mechanisms or altered rates of crack growth. Understanding the failure mechanisms and the corresponding influence factors is of much scientific interest and additionally, a systematic methodology to predict lifetime of the substrate-solder interconnect is of great commercial utility. These two, understanding the failure mechanisms/influence parameters and developing a method for lifetime prediction form the goals of this research work. A partial or abridged version of contents discussed in this chapter may also be found in [Geo+18](©2018 Elsevier).

5.2 Methodology

The complete work has been subdivided into individual sections for a thorough investigation. Each step is discussed in detail in further sections of this chapter. The major steps are listed below.

1. Build-up of a DoE that includes, as exhaustively as possible, all potential influence factors.
2. Perform temperature cycling tests on the various DoE variants.
3. Evaluation of solder degradation using Scanning Acoustic Microscopy (SAM) and cross sections and subsequently determine End of Life (EoL) for the DoE variants.
4. Perform finite element simulations on all DoE variants decided upon in step 1, under identical ageing conditions as in step 2.

5. Identify FEM damage parameters that describe the failure mechanism appropriately and derive a phenomenological lifetime model.

The above mentioned methodology is shown in Figure 5.1.

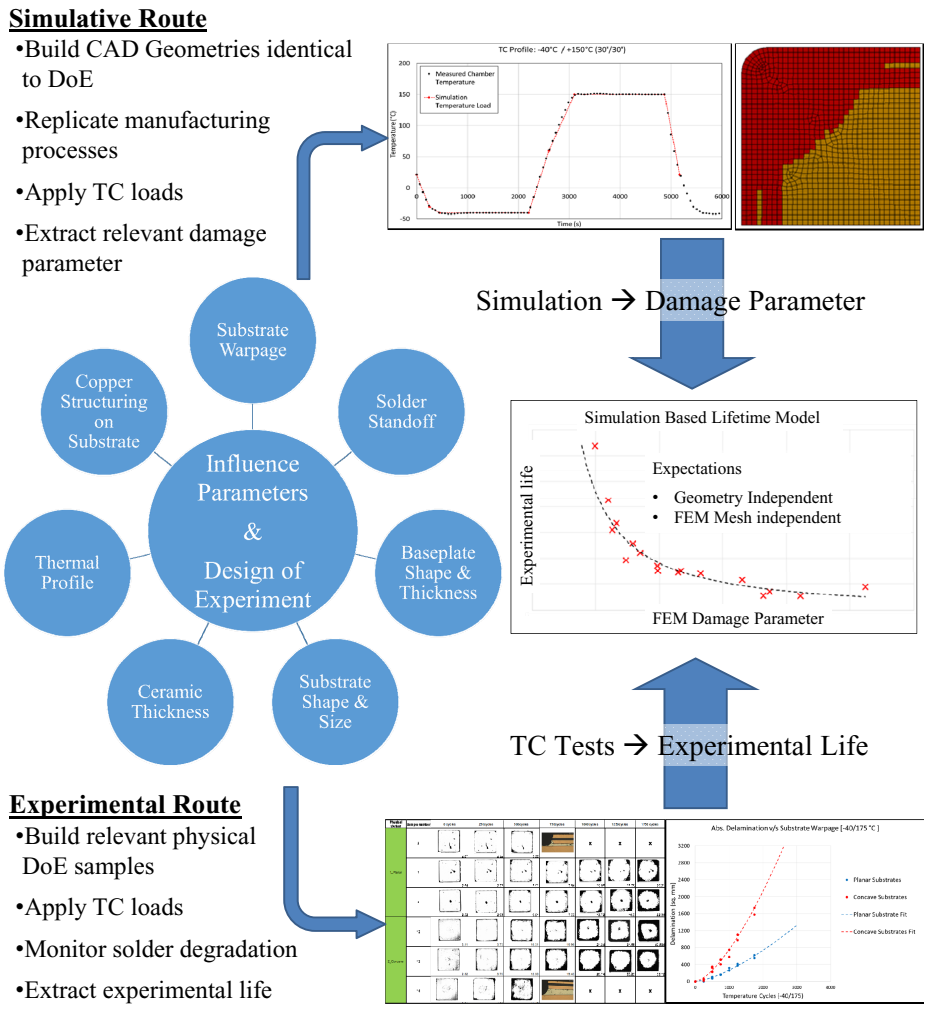


Figure 5.1: Methodology for reliability investigation and lifetime prediction of baseplate soldering

5.2.1 Design of Experiments

The DoE is based on a *One Factor at A Time (OFAT)* scheme. It is already known that more efficient DoE schemes are available. OFAT was chosen keeping in mind two specific reason. The first reason is that the initial know-how of the failure mechanisms and the extent of the influence parameters on these failure mechanisms was very limited. It was also known that systematic errors in the failure analysis procedure was low. Therefore, the two general preconditions for the satisfactory use of the OFAT scheme was met [Dan73]. Secondly, but importantly, a major reason for choosing OFAT was the fact that this work aims at predicting

lifetime of baseplate solder joints simulatively using a *simulation based Damage Parameter*. Savoie [Sav10] showed that there is a strong link between the type of DoE model used and the ability of researchers to detect flaws in computer simulations of physical problems. The study showed that the rate of detection of a simulation based flaw significantly decreases when the experiments used to verify the simulations were based on complex factorial DoEs (usually multiple factors are varied simultaneously in factorial DoEs). It was also demonstrated that this risk of not detecting a mistake in the simulation methodology was significantly reduced when using the OFAT scheme (*"...about half of the one-factor-at-a-time designers successfully recognized the simulation problem, and nearly none of the fractional-factorial designers did so."*).

Given that the initial know-how was low, simulation models for accurate description of baseplate soldering reliability were not available and that the eventual prediction of lifetime was planned to be done via simulations, it was important to keep the above mentioned risk as low as possible. As a result, OFAT intentionally became the less sophisticated but low risk DoE scheme aimed at better understanding of influence parameters and the development of a robust simulation methodology. For the DoE to evaluate the effect of various physical features on reliability of the baseplate solder joints, a large sample space with a wide range of influence parameters were taken into consideration. The factors studied and the rationale behind choosing these influence parameters are explained below.

1. **Substrate warpage:** As described in Section 3.3.1, depending on the copper imbalance on either side of the power substrate, concave or convex substrate warpages can occur. If a substrate warps concavely at high temperature, a crack opening mode is triggered which also coincides with the temperature regime where solder creep effects are dominant. On the other hand, if a substrate warps convexly at high temperature, a crack opening mode is triggered at the low temperature region of the TC profile where the solder is comparatively more brittle. The question on which mechanism dominates the crack growth in solder joints is as of yet unresolved and was an interesting point of enquiry. In addition to this, copper imbalance on the substrate also influences the stress state and the solder joint thickness in the post soldering state. These effects were expected to have a sizeable impact on the reliability of the solder joint.

2. **Baseplate shape and thickness:** The baseplate is by far, the component with the highest thermal mass and volume in the assembly. It is also made of copper that has a high CTE of ∼17 ppm. Therefore, during any given temperature change, the thermomechanical force generated and transferred to the solder layer could be significantly influenced by the baseplate and have a notable effect on the reliability of the solder joint.

3. **Ceramic thickness:** Compared to the other materials in the assembly (copper, solder and IMC), the ceramic material, Si_3N_4, has a much higher Young's modulus and a much lower CTE. Increasing the amount of ceramic would increase of the bending stiffness of the substrate and thereby reduce warpage. On the other hand, this also reduces the effective CTE of the substrate and thereby increases the CTE mismatch between the substrate and the solder.

4. **Substrate shape and size:** Depending on the application, the amount of power to be converted and the number of phases involved with the AC power conversion, PE modules come in a wide variety of sizes. It is usually seen that degradation in solder starts from the corners/boundaries relative to locations of minimum thermally induced mechanical strain. It was interesting to know how the distance from this minimum strain locations (middle of the substrate) influences reliability. This work therefore evaluated this effect by varying substrate size and tracked its influence on delamination behaviour.

5. **Bondline thickness:** In the world of chip scale packages, cracks under passive TC generally occurs in the bulk of the solder joint. The reliability of such solder joints can be improved by increasing the solder stand-off.

   The reasoning behind this is that, increasing the solder joint size provides simply more material over which the thermo-mechanical force is distributed and thereby, lowers the stress (and consequently plastic strain) developed in the solder joint. However, there has been no conclusive evidence for such behaviour in the case of large area solder joints were the cracks lie almost exclusively on/near the interface of the solder and the IMC layer.

6. **Copper structuring on substrate:** From a real-world application point of view, copper imbalance on the power substrate is a direct consequence of etched copper structuring on the top side of the substrates. As such structuring gives rise to warpage in substrates, they were chosen for investigation. Warpage however can be mitigated by having identical structuring on the top and bottom sides of the substrate, which however, results in discontinuities in the solder joint. Whether they play an important role in solder degradation or contribute to additional failure mechanism was unknown.

7. **Temperature cycling profile:** Solder joint degradation is sensitive to the temperature profiles used in pTC test as different profiles induce different levels of thermo-mechanical stress, usually influenced by the temperature swing (ΔT) and creep deformations which is sensitive to (T_{max}). The interplay of these two factors was of interest and the influence of both these factors were evaluated using three different pTC profiles as follows

   - Profile 1: -40 °C / 175 °C
   - Profile 2: -40 °C / 150 °C
   - Profile 3: -15 °C / 175 °C

   The chosen profiles enable the comparison of different extremum temperatures (-40 °C, -15 °C, 150 °C and 175 °C) and also different temperature swings (190 °C and 215 °C). Temperature cycling was carried out using single chambered thermal chambers with 30 minutes hold time at extremum temperatures.

The complete list of the DoE variants is summarized in Table 5.1.

Table 5.1: DoE variants examined in this research

Influence Parameter	Variants	Loading Conditions
AMB top side copper (AMB back side Copper = 0.50 mm)	0.30 mm	Single Chamber TC -40 °C / 150 °C (30 min hold time) -15 °C / 175 °C (30 min hold time) -40 °C / 175 °C (30 min hold time)
	0.50 mm	
	0.57 mm	
AMB back side copper (AMB top side Copper = 0.50 mm)	0.43 mm	
	0.50 mm	
	0.57 mm	
Ceramic Thickness	0.32 mm	
	0.64 mm	
Substrate Aspect Ratio	30 mm x 58 mm	
	58 mm x 58 mm	
	70 mm x 58 mm	
Substrate Size (Constant Aspect Ratio)	30 mm x 30 mm	
	58 mm x 58 mm	
	70 mm x 70 mm	
Structuring on AMB Copper	Top Side Structured, Bottom Side Unstructured	
	Top Side Unstructured, Bottom Side Structured	
	Top Side Unstructured, Bottom Side Structured	
Baseplate Thickness	3 mm	
	4 mm	
	5 mm	
Baseplate Length	90 mm	
	150 mm	
	200 mm	
Solder Bondline Thickness	0.200 mm	
	0.300 mm	
	0.400 mm	

5.2.2 Sample manufacturing

As already mentioned in Section 2.2, the components used in this work involve the diverse materials. They are summarised in Table 5.2.

Table 5.2: Materials involved in DoE variants

Component	**Material**
Substrate Metallization	Copper
Substrate Ceramic	Si_3N_4
Solder	Innolot
Baseplate	Copper

To ensure the correct solder bondline thickness, spacers made of aluminium bond wires of 200, 300 and 400 µm were laser bonded to the surface of the baseplate that is to be soldered. A clean surface for soldering is achieved by cleaning the baseplates using a proprietary method involving acetone, citric acid, deionized water and ultrasonic agitation. To prevent the build-up of oxide layers or contamination due to fat residues during handling, the cleaned baseplates were subsequently sealed into Electro Static Discharge (ESD) secure bags and filled with nitrogen.

Deposition of the solder paste is carried out with the help of a stencil. The metal stencil with thickness of 400, 600 and 800 µm were used. The volume of deposited solder paste is determined by the ratio of the area of the stencil aperture/opening to the area of the aperture walls (so called *Area Ratio* [IPC04]). For an objective evaluation of the solder joints stencils were designed such that all stencils had the same area ratio.

Soldering was carried out using the vapour phase soldering method due to the large thermal mass of the soldered components (ref. 2.1.2). The soldering profile used was the same as ST_H (Table 4.1) used in the IMC study. As the volume of solder used in the baseplate soldering is much higher as compared to chip scale interconnects, surface tension of the molten solder is not usually enough to prevent the solder from flowing astray from the designated interconnect region. To prevent leakage of molten solder, the boundaries of the interconnect regions are lined with Kapton® tape which makes the regions outside the valid interconnect area non-wettable. A step-by-step depiction of the sample build-up is shown in Figure 5.2. Following the manufacturing of the sample, they are cleaned again to prevent any corrosion that could potentially be induced by the flux residues.

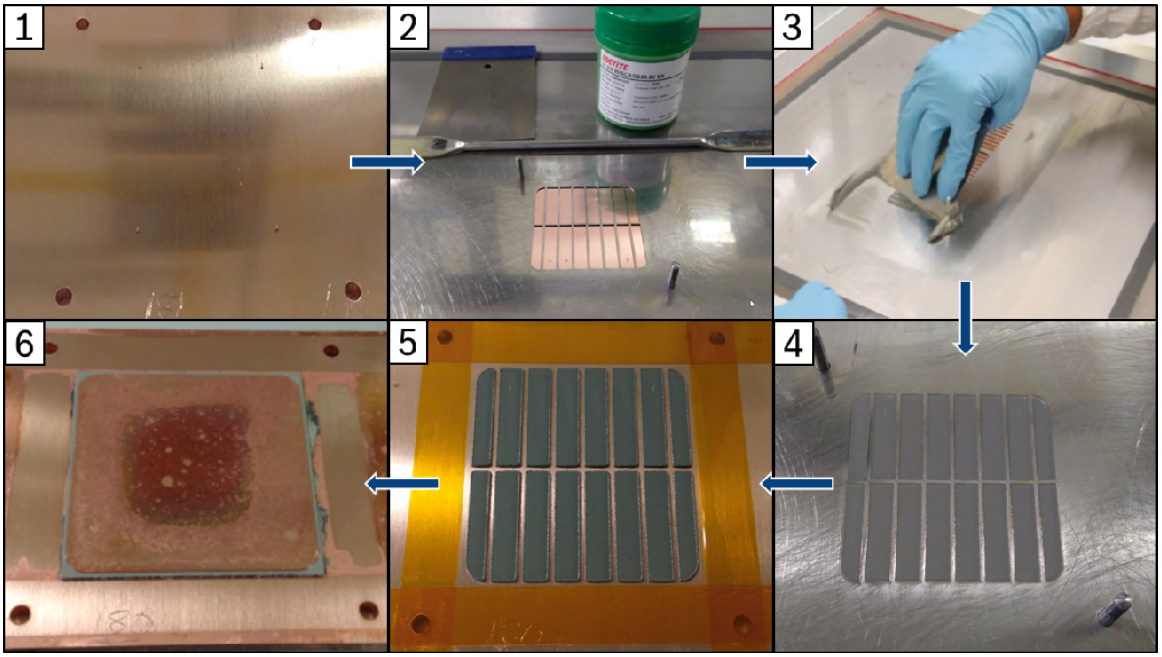


Figure 5.2: Sample build-up of DoE variants

5.2.3 Failure analysis

There are many sophisticated failure analysis techniques available for detection of damage in microelectronics. Some of them include optical, scanning and transmission electron (SEM/TEM) microscopy, X-ray and scanning acoustic microscopy (SAM). Among these, optical microscopy of cross sectioned parts and scanning acoustic microscopy of non cross sectioned samples are used in this research.

Cross sectioning is a process in which the specimen to be investigated is embedded in a transparent colourless liquid epoxy that hardens over a period of time (usually one day). The hardened epoxy with the embedded specimen is ground down on a plane of interest using a series of grinding surfaces and finally polished to a mirror like finish. This can then be viewed under an optical microscope up to 1000x magnification to reveal the location and growth characteristics of cracks. The disadvantage of this method is that it is a destructive process and the cross sectioned part can no longer be used for further TC test. Cross sections therefore are limited in this study to one sample per variant at a specific number of temperature cycles (500 TC) and primarily used to determine the failure mode and the location of the crack.

Scanning acoustic microscopy (SAM) is used to do the bulk of the evaluation of solder degradation. In this technique, high frequency sound waves are produced by an ultrasonic transducer that pass through the analysed samples. Cracks in the samples give rise to additional material interfaces at which the sound waves generated by the transducer are reflected back. These reflected waves can be picked up by the transducer and an accompanying software converts this signal into visual images. The disadvantage of this method is that cracks can be detected on only a particular plane at a given time. This is a problem as in many of the tested samples, the substrates are warped and therefore the cracks do not lie in a single plane. Therefore, the method employed in this study uses a so called S-Scan which is

a through scan mode. Here there is a transducer placed on one side of the sample and an ultrasonic sensor placed on the other side. Using the detector, the SAM device measures the loss in intensity and phase shift of the sound waves generated by the transducer and displays it as a crack map. With this method, the extent cracks in the solder layer can be clearly seen without destroying the component which can then be further subjected to TC testing. Figure 5.3 shows the results from both measurement techniques. The dark regions in the SAM image is where the cracks have progressed while white regions indicate the region where solder is still intact.

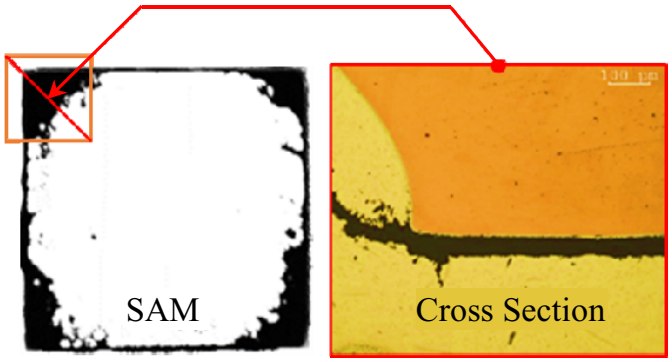


Figure 5.3: Failure analysis using SAM and cross sections [Geo+18]

5.2.4 Quantitative evaluation of failure and End of Life (EoL)

SAM images provide a qualitative measure of the extent of crack progression in the solder layer. A sample SAM image is shown in Figure 5.3 For the purpose is lifetime prediction however, a quantitative measure of crack growth is required. This is done via a MATLAB® image processing script. The script converts greyscale images obtained from the SAM equipment and converts it into a black/white image based on a user defined threshold value. In this study the greyscale threshold value was set to be 50. It then carries out a pixel counting algorithm distinguishing between black and white pixels. Based on these values, absolute and percentage delamination can be calculated.

This procedure is repeated for each variant after each TC sampling step. For TC profiles -40/150 °C and -15/175 °C, sampling is done after every 500 cycles and for profile -40/175 °C sampling was done after every 250 cycles as this was the most aggressive TC profile. With this procedure a degradation log for each sample and TC profile can be maintained. An example degradation log for one of the DoE variants under TC profile -40/175 °C is shown in Figure 5.4. The degradation values as logged in Figure 5.4 can be plotted on a graph and a fitting curve can be calculated. Then, by setting a given percentage delamination as failure criteria, end of life (EoL) values can be extracted for each DoE variant. EoL determination for the degradation log shown in Figure 5.4 is shown in Figure 5.5.

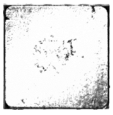
Physical Variant	Sample number	TC_0	TC_250	TC_500	TC_750	TC_1000	TC_1250	TC_1750
2	12	3.11 	3.73 	10.31 	15.96 	21.34 	31.56 	48.59 
	13	2.32 	3.75 	12.56 	19.45 	26.74 	35.26 	53.12 
	14	2.71 	4.58 	14.17 	Sample used for cross sectioning at 500 TC. Consequently, no further SAM results.			

Figure 5.4: Sample degradation log [-40 °C / 175 °C]

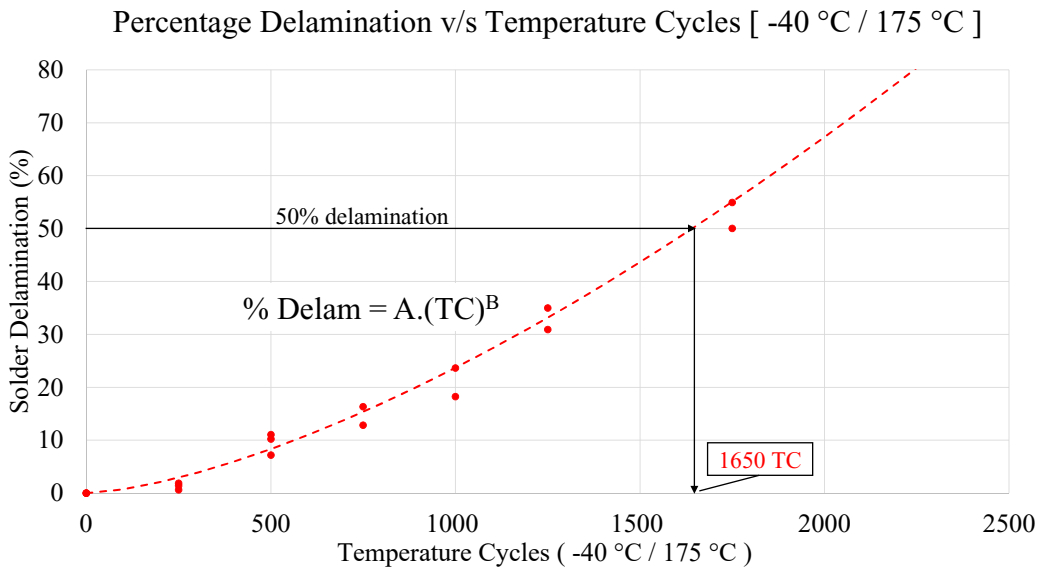


Figure 5.5: End of life determination from degradation log

5.3 Experimental results from temperature cycling tests

The DoE influence parameters as mentioned in Section 5.2.1, show a strong impact on the reliability of the solder joint. The following section documents the failure mode and the extent of solder degradation in various DoE variants as seen in SAM images at 1000 cycles. For the sake of brevity, examples are shown from the -40 °C / 175 °C temperature profile as they show the influence most clearly. The trend of solder degradation is the same in all TC profile cases.

It was seen that the solder layer begins to degrade from the edges and progressively moves inwards. The cracks as seen in cross sections lie almost exclusively on or very close to the interface of the IMC and the solder layer on the substrate side.

5.3.1 Effect of substrate warpage

Warpage has a significant influence on reliability. As can be seen clearly seen in the Figure 5.6, that substrates that tend to warp concavely at high temperature show much faster degradation as compared to planar substrates. This can be explained on the basis that concave substrates result in a crack opening mode at high temperature and parallelly, this is also the temperature regime where creep effects are dominant. As a result, two damaging phenomena are present simultaneously and significantly increases the rate of crack growth. Figure 5.6 also shows that although the crack growth rates are different, the failure mechanism remains the same.

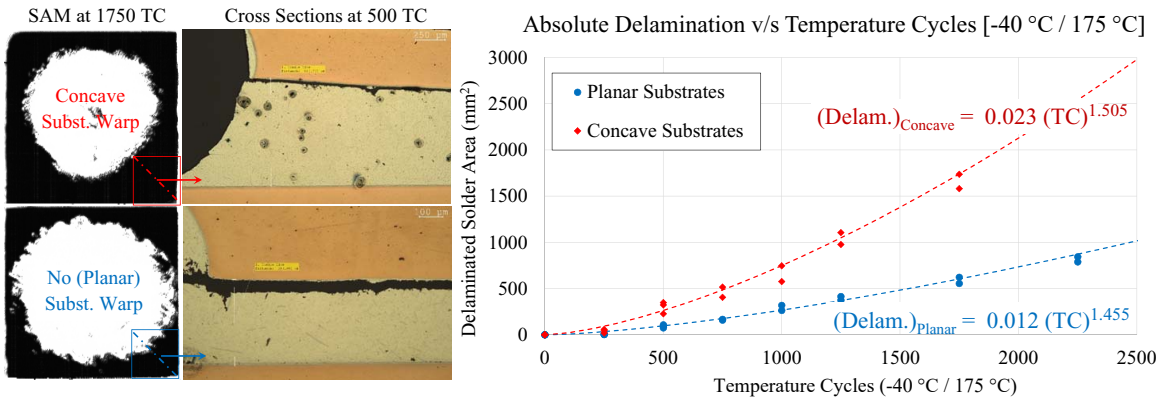


Figure 5.6: Effect of warpage on reliability

5.3.2 Effect of baseplate thickness and shape (Aspect ratio)

The baseplate geometry is varied in two categories. First in which, the lateral size of the baseplate is kept constant and only the thickness is varied, *viz.* 3 mm, 4 mm and 5 mm. Second variation item is that of the lateral dimensions of the baseplate while the thickness is held constant. The investigated variations in lateral dimensions are 90 mm x 90, 90 mm x 150 mm and 90 mm x 200 mm

5.3.2.1 Effect of baseplate thickness

TC results show that thickness of the baseplate has a significant influence on the reliability of the solder joint. As can be seen in Figure 5.7, higher the thickness of the baseplate, faster is the solder degradation. This can be explained on two fronts.

Firstly, the thermo-mechanical force generated due to the expansion and contraction of the baseplate during temperature cycling is also a major cause of degradation of the solder layer. A higher thickness of the baseplate means that a greater amount of thermally deformable material is present and, this consequently results in higher thermo-mechanical force where

relative movement is constrained *i.e.*, the solder-substrate interface. This leads to faster crack growth.

Secondly, as the thickness of the baseplate increases, the bending stiffness of the baseplate also increases ($\propto (thickness)^3$). This means that in case of asymmetric substrates, thicker baseplates offer much higher mechanical resistance to the warping behaviour of the substrate and thereby causing the solder to carry more load causing faster degradation.

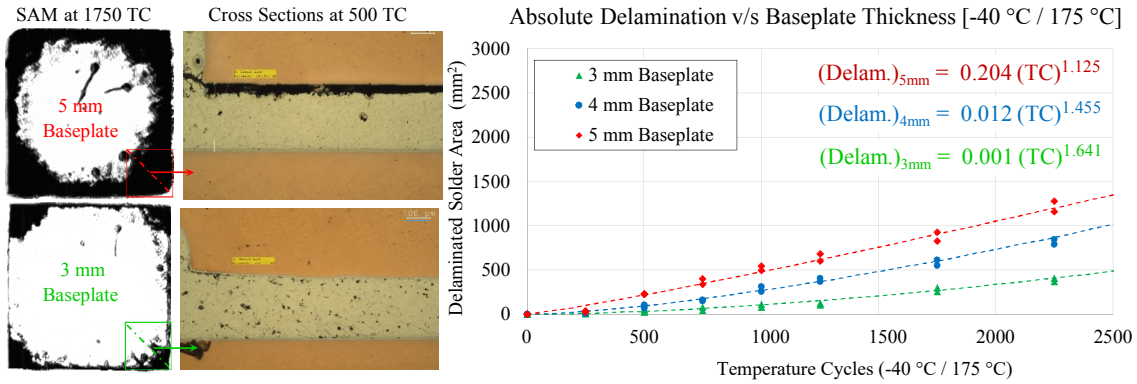


Figure 5.7: Effect of baseplate thickness on reliability

5.3.2.2 Effect of baseplate aspect ratio

Samples with different aspect ratios for the baseplate showed no notable effect on the rate of crack propagation. This is due to the fact that although considerable material is added to the baseplate, this material addition happens away from the soldered region. The added copper is also not constrained in any way whatsoever by the substrate or the solder layer. As a result, the additional copper material deforms independent of the substrate or the attaching solder material and therefore plays practically no role in the degradation of the solder layer. SAM and cross sectional images are shown in Figure 5.8.

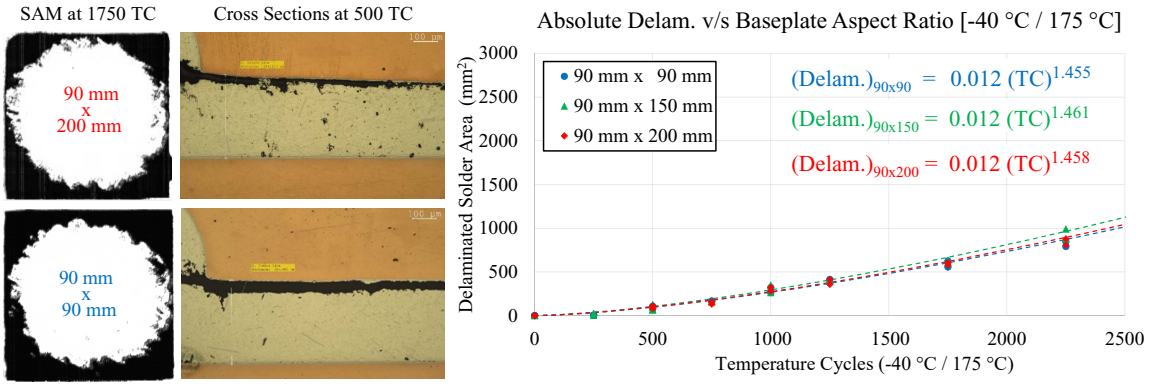


Figure 5.8: Effect of baseplate aspect ratio on reliability

5.3.3 Effect of ceramic thickness

The thickness of the ceramic layer showed one of the strongest influences on the rate of crack growth in the solder layer. There are two major reasons for this. Firstly, the ceramic layer is stiffer than the copper layer of the AMB substrate. A higher proportion of ceramic in the substrate increases the effective stiffness of the substrate. The inherent increase in geometric stiffness due to the increase in thickness is also present. In addition to the increase of stiffness, the ceramic layer has a much lower CTE compared to the copper present in the AMB. According to the Equation (5.1) [Lut09] where d_{Cer}, d_{Cu}, and K stand for the thickness of the ceramic layer, thickness of the copper layer and the ratio of the elastic moduli of ceramic to copper, the increasing ceramic thickness results in a decrease of the effective CTE of the substrate.

$$CTE_{sub} = \frac{CTE_{Cer} + CTE_{Cu}\dfrac{d_{Cu}}{K \cdot d_{Ceramic}}}{1 + \dfrac{d_{Cu}}{K \cdot d_{Cer}}} \tag{5.1}$$

This increases the mismatch in CTE between the substrate and rest of the assembly, namely, the solder and baseplate and consequently results in faster degradation of the solder joint as shown in Figure 5.9.

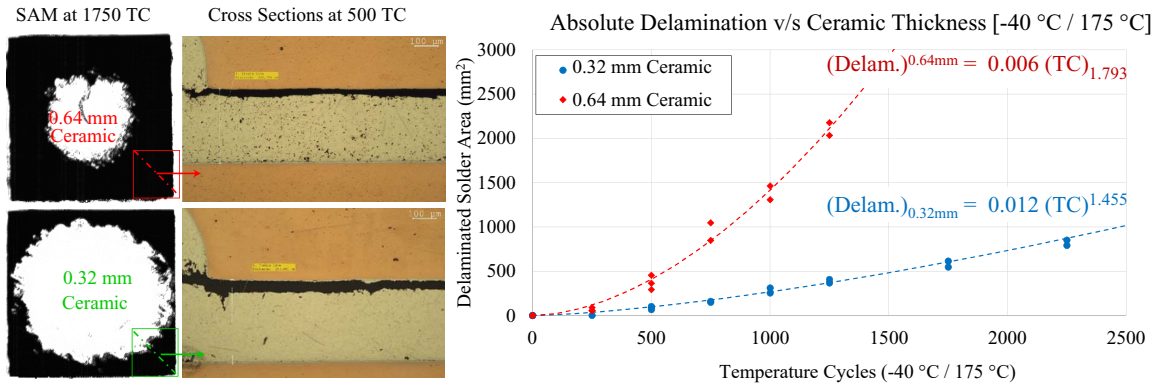
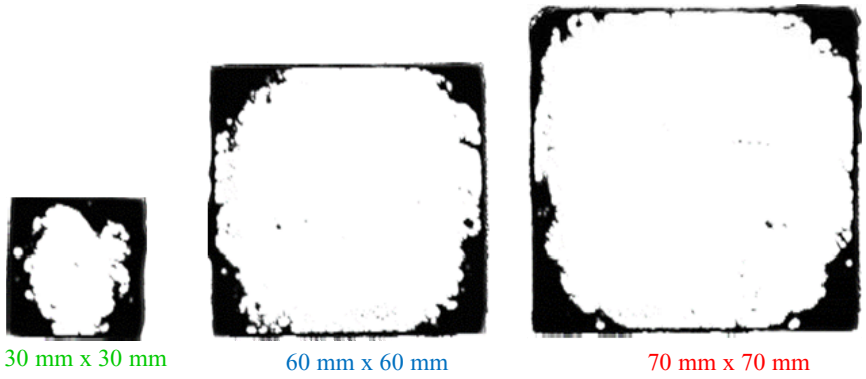


Figure 5.9: Effect of ceramic thickness on reliability

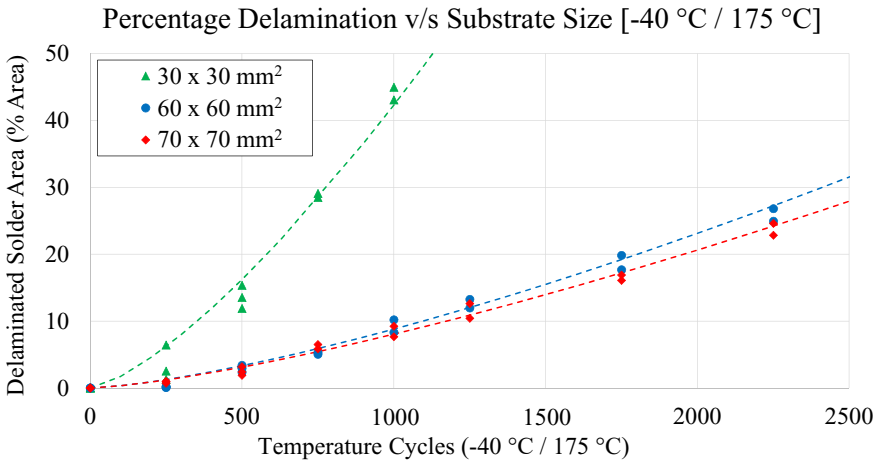
5.3.4 Effect of substrate size and shape

5.3.4.1 Substrate size

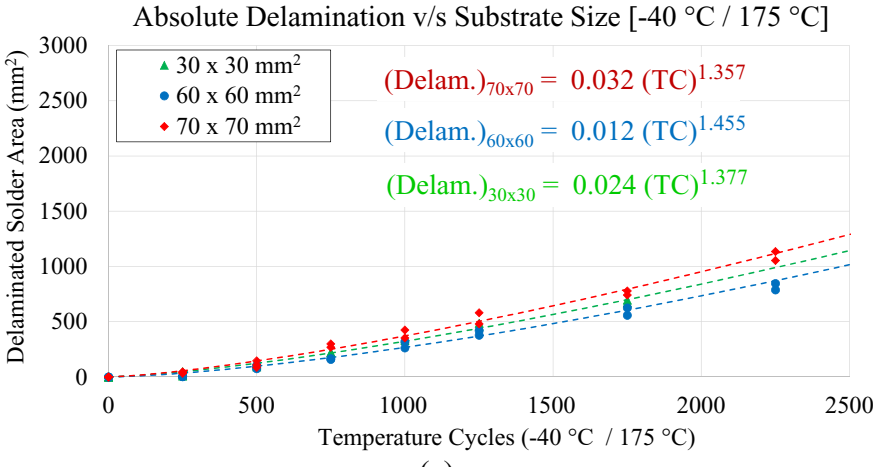
The rate of crack growth was found to be not influenced by the size of the substrate, *i.e.*, the absolute delaminated solder area irrespective of the solder joint was roughly the same. Figure 5.10(a) shows the SAM images after 1000 TC under profile -40 °C / 175 °C. It also shows the increase in absolute and percentage delamination of the solder joints (Figure 5.10(b) and (c) respectively). However, size of the substrates indirectly plays a role in the number of cycles to end of life. Given that the absolute delamination in all three substrate sizes is roughly the same, the smaller substrate sizes will exhibit a higher percentage delamination of the solder layer. As failure criteria is generally set as percentage value of the delaminated soldered surface, smaller sized substrates will fail first.



(a) SAM images at 1000 TC



(b)

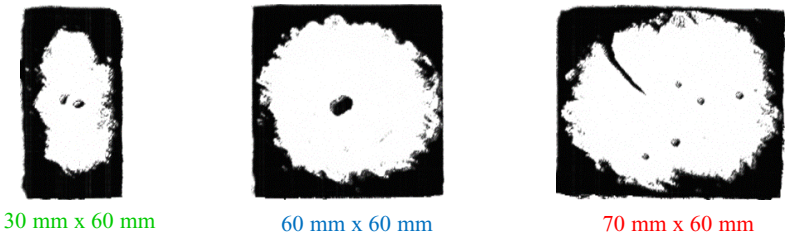


(c)

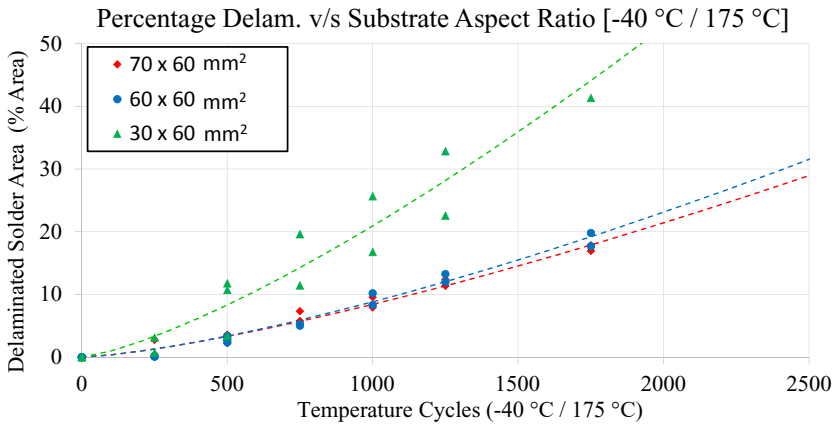
Figure 5.10: Effect of substrate size on reliability

5.3.4.2 Substrate aspect ratio

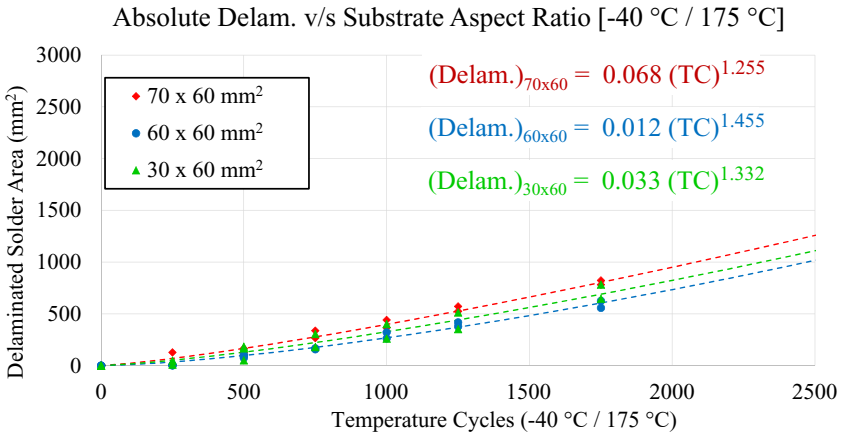
As in the case of samples discussed in Section 5.3.4.1, absolute delamination of solder joints was not influenced noticeably by substrate aspect ratios as seen in Figure 5.11(a) which illustrates SAM images after 1750 TC under profile -40 °C / 175 °C and the increase in absolute and percentage delamination of the solder joints (Figure 5.11(b) and (c) respectively). Consistent with the expectations, as also seen in the previous section, the delamination at the edges is completed first on the shorter edges as crack growth rate remains more or less constant. The influence on lifetime is same as for samples from the previous section, *i.e.*, substrates with smaller area will reach EoL earlier.



(a) SAM images at 1750 TC



(b)



(c)

Figure 5.11: Effect of substrate aspect ratio on reliability

5.3.5 Effect of solder bondline thickness

The effect of solder joint thickness was minimal and to some extent inconclusive. For TC profile -40 °C / 175 °C, thinner solder joints 200 µm showed slower crack growth as compared to thicker solder joints as seen in Figure 5.12 and therefore higher EoL. This behaviour could be attributed to the fact that a thicker solder joint increases the bending stiffness on one side of the interface crack.

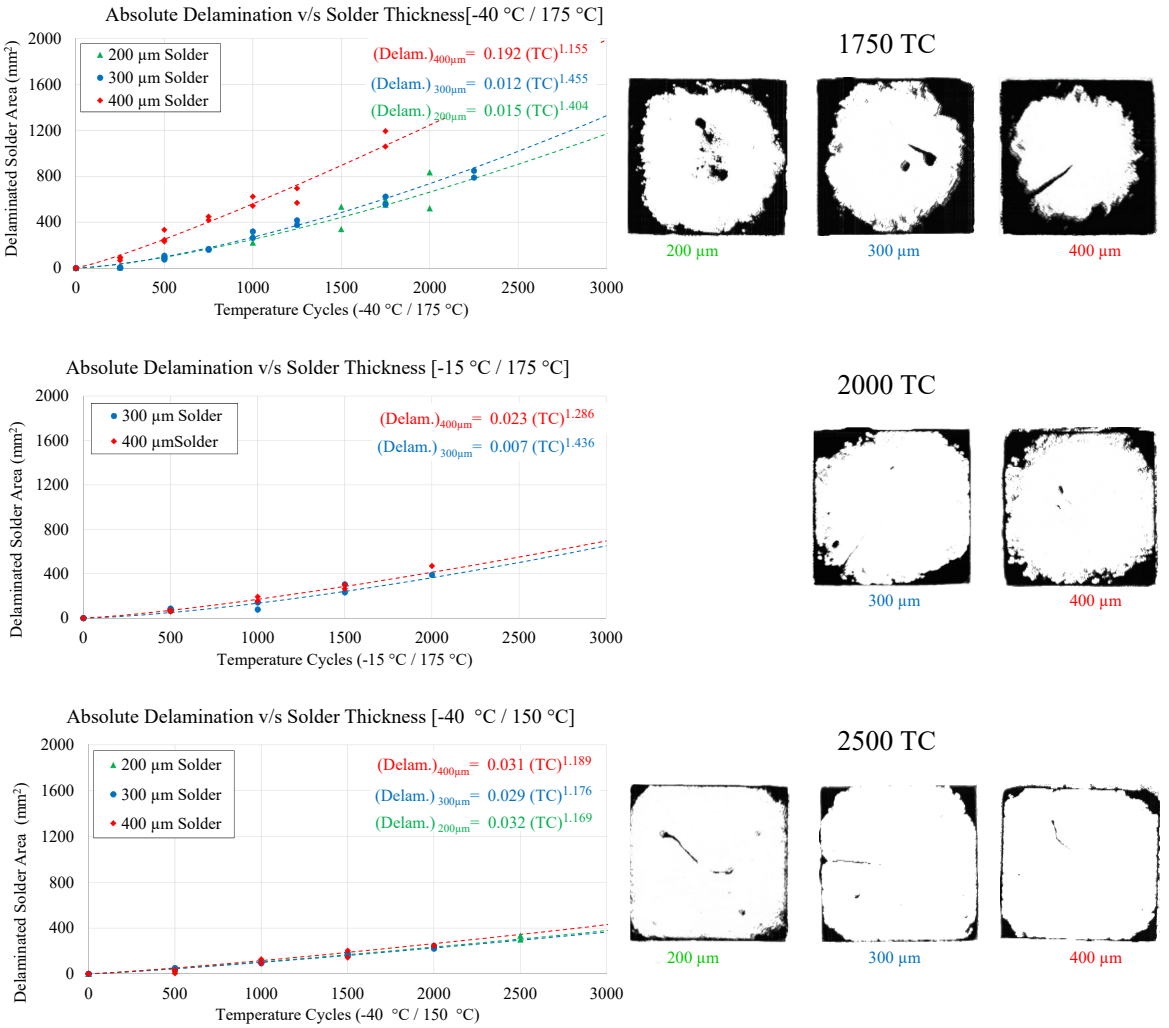


Figure 5.12: Effect of solder bondline thickness on reliability

However, a similar trend was not clearly seen in the specimens aged under the other two temperature profiles, namely, -15 °C / 175 °C and -40 °C / 150 °C. Under these temperature profiles, specimens with different solder bondline thicknesses showed similar crack growth. It can thus be stated that reducing solder joint thickness (at least within the boundaries of this DoE *i.e.* between 200 µm and 400 µm poses no disadvantages from a mechanical reliability standpoint. From a thermal point of view, reducing solder joint thickness reduces the thickness of the thermal path from the heat generating chips to the baseplate (heat sink) which is a significant advantage. Consequently, thinner solder joints can be recommended for such power modules.

5.3.6 Effect of copper structuring on substrate

In section 5.3.1, it was discussed that increasing concave warpage resulted in faster degradation. Some possible methods to reduce the warpage in AMB substrates was already listed in Section 3.3.3.4. One of the possibilities was to have a symmetric copper structure on the top and bottom sides of the substrates. This possibility was also investigated within this DoE and the results are shown in Figure 5.13.

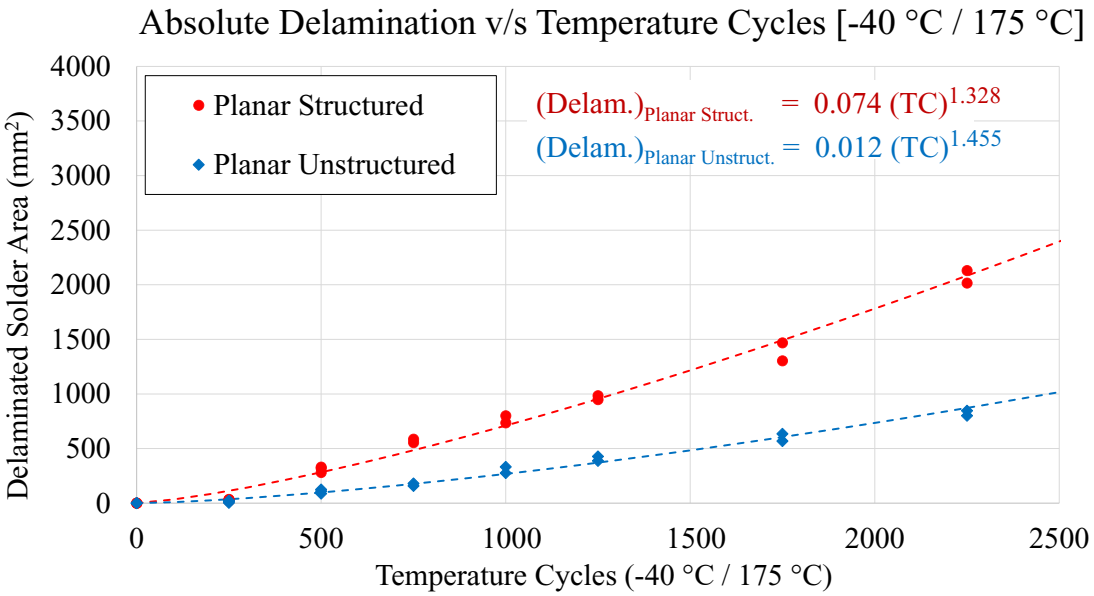


Figure 5.13: Effect of copper structuring on the AMB on reliability

Symmetric structured (identical etching on both top and bottom AMB copper) substrates show solder delamination greater than that of symmetric unstructured (no etching on both top and bottom AMB copper) substrates. This is an interesting result as neither of the two variants have warpage and were expected to have similar rate of crack growth. There are two reasons for this observation.

1. As a result of symmetric etching, solder joints are created only at copper tracks which have relatively a small surface area for the solder to adhere to. These surfaces thus result in a stress concentration and cracks begin to grow from both sides of the copper track-solder interconnect. This effect was verified by measuring IMC thicknesses at various delaminated regions. The idea in the background is that the IMC layer can grow only if the existing IMC layer gets supplied by tin and copper atoms. The only source of tin atoms is the solder layer itself. Once interface delamination has taken place, the supply of tin atom is interrupted and the IMC layer can no longer grow. As the failure mode in the examined samples was cracks at/near the IMC and bulk solder interface, using the IMC growth model derived in Chapter 4, the number of cycles taken until the crack reaches a given location can be calculated. The results of this verification from cross section at 500 TC under -40 °C / 175 °C is shown in Figure 5.14. As clearly seen from the IMC thicknesses, cracks initiate simultaneously from both sides of the copper track and thus considerably reduce time to failure.

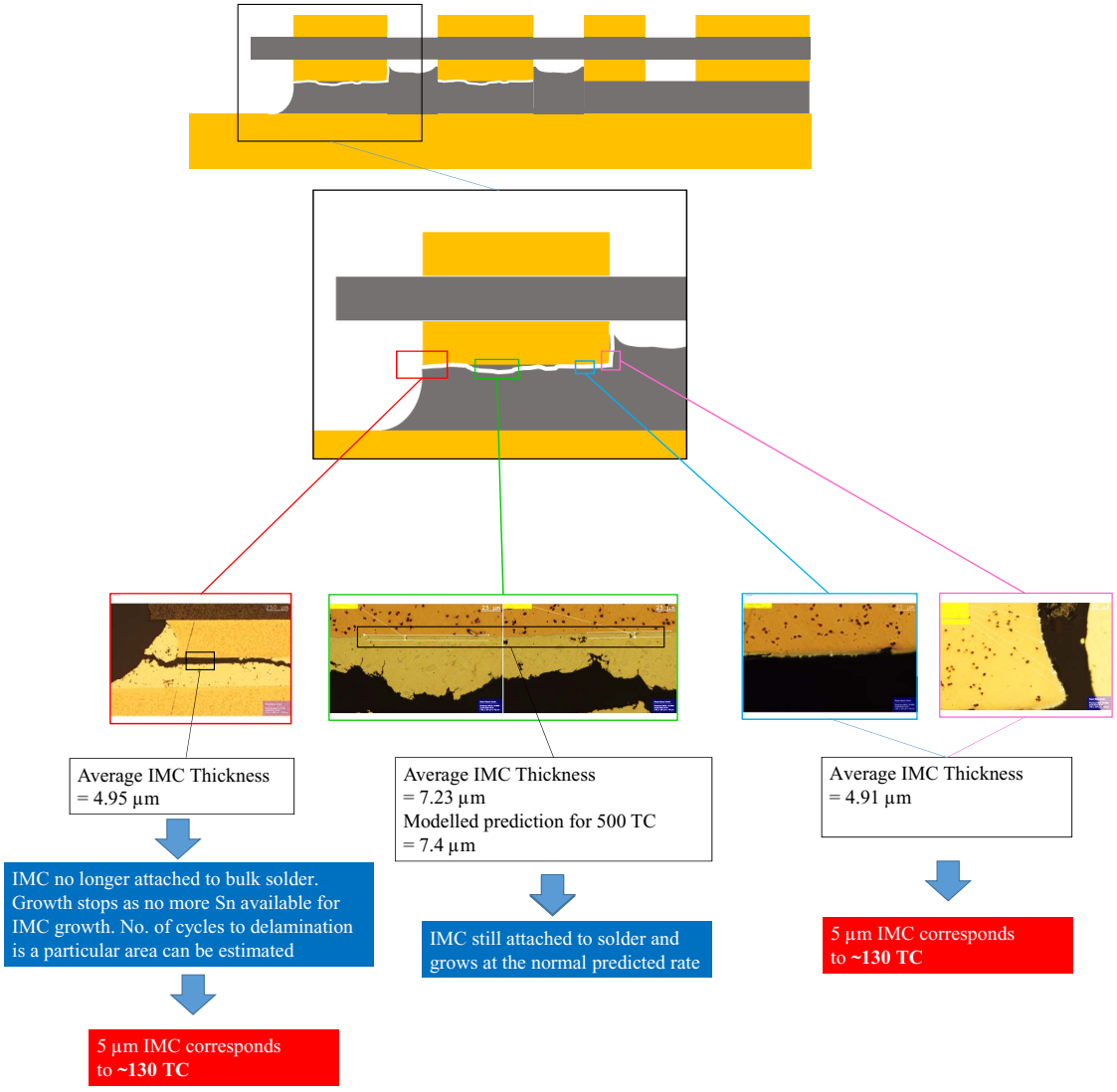


Figure 5.14: Mechanism of faster solder degradation in case of symmetrically structured substrates verified using IMC growth model derived in Chapter 4

2. Etched bottom side channels contribute to discontinuities in the solder joint as in these channels the copper has been completely etched out up to the ceramic surface. As the ceramic itself is not wettable by the molten solder alloy, these locations behave as *predelaminated* areas. Once the crack has grown past the outermost copper track, the crack, by default, jumps to the next copper track where due the effect mentioned in the previous point, a crack may already have initiated. This effect consequently reduces the lifetime of the samples with symmetrically structured substrates.

5.3.7 Effect of TC profile

Temperature cycling profile has considerable influence on the degradation of the solder layer. As can be seen from Figure 5.15, the -40 °C / 175 °C profile with a ΔT = 215 °C and a T_{peak} = 175 °C is the most aggressive. Already at 500 TC cracks between the IMC and solder layer are clearly seen. Profile -40 °C / 150 °C with a ΔT = 190 °C and a T_{peak} = 150 °C is the least aggressive. As seen both in the SAM and cross section images, the cracks are not fully developed. Cross section images do show micro-cracks beginning to form at the substrate corner.

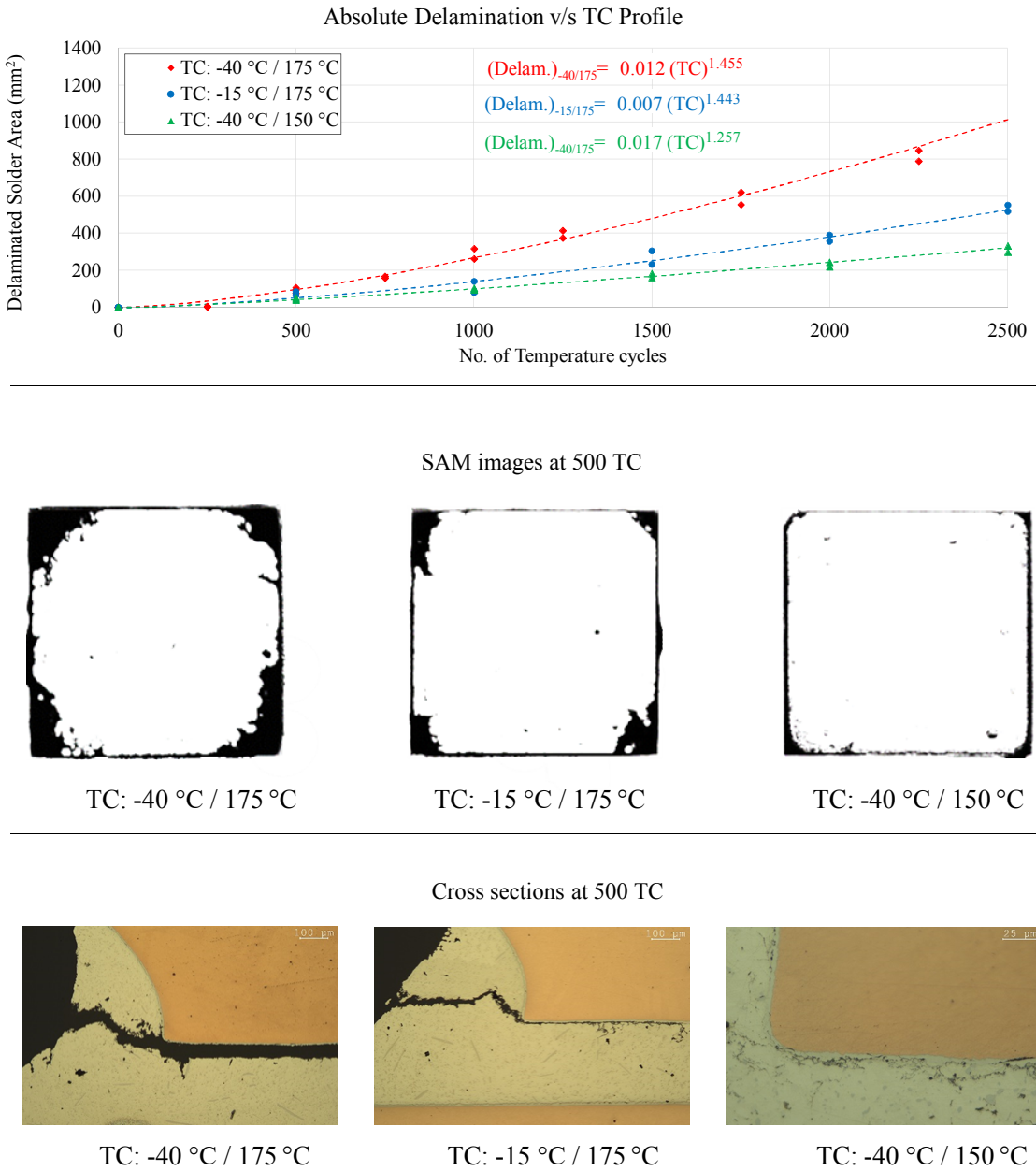


Figure 5.15: Effect of TC profile on reliability

To be noted is that the cracks have not initiated in the solder meniscus. This is evidence of the fact that cracks not only propagate but also initiate at or near the solder IMC interface. Profile -15 °C / 175 °C was designed as a hybrid between the two previously discussed profiles. It has the same ΔT = 190 °C as in Profile -40 °C / 150 °C but a higher T_{peak} = 175 °C. TC testing revealed results halfway between the -40 °C / 175 °C and -40 °C / 150 °C profiles. Cross section images show that the cracks have already initiated, but are however, not as developed as in the -40 °C / 175 °C profile.

It is quite common in the industry and also some academic literature to make estimates of lifetime using acceleration factors that are purely dependent on the temperature swing ΔT. This result clearly shows the fallacy in using such a procedure which could lead to large errors in lifetime estimates. Both ΔT and T_{peak} play significant and independent roles in the degradation of the solder joint.

5.4 Simulation and damage evaluation

As discussed in Section 5.2, for deriving a lifetime model, experimental results for various DoE variants and a simulative damage parameter for each of these variants is required. Section 5.3 already describes the solder degradation trends for the DoE variants under 3 temperature cycling profiles and also how the EoL for these variants has been estimated using a 50% solder delamination failure criteria (Figure 5.5). The experimental results therefore constitute one half of lifetime prediction methodology. The FEM simulative part, that forms the second part is described in the following sections. All FEM simulations in this study are done with the help of the FEM Software ANSYS® Version 18.0

5.4.1 Simulative procedure

5.4.1.1 Temperature loading conditions

Temperature cycling was performed in TC equipment that had a single chamber and employed air as the heat transfer medium. As a result, two effects could have been present that possibly needed to be accounted for in the FEM simulation environment:

1. Due to the large number of samples placed in the same chamber, it was possible that the temperature of the samples lagged behind the temperature of the air in the chamber. It was thus important to know the actual temperatures experienced by the samples, which could then be applied as loading conditions in the FEM simulation.

2. Due to the large thermal mass of individual samples, it was possible that the temperature of the sample periphery and the inner regions of the sample had different temperatures. If this was the case, a transient thermal simulation would additionally be needed which would determine the real time temperature distribution of the samples. This resultant temperature distribution from the transient thermal simulation would then be used as temperature loading conditions instead of a homogeneously applied temperature loading condition.

To resolve the above mentioned two points, a temperature logging setup was built and the temperature of the TC chamber air, solder corner and solder core was logged. The setup and results are shown in Figure 5.16. Two inferences can be made from the results presented in Figure 5.16. First, that although the temperature of the components lags behind the temperature of the TC chamber, this lag is minor, and the temperature ramp rate is not significantly influenced. Moreover, the components reach extremum temperatures simultaneously with the chamber air. The second inference that can be made is about the temperature distribution of the solder joint. As can be seen from Figure 5.16, the thermocouple reading at the corner and core of the solder joint are identical. This means that the entire sample can be assumed to have a uniform temperature distribution during temperature cycling.

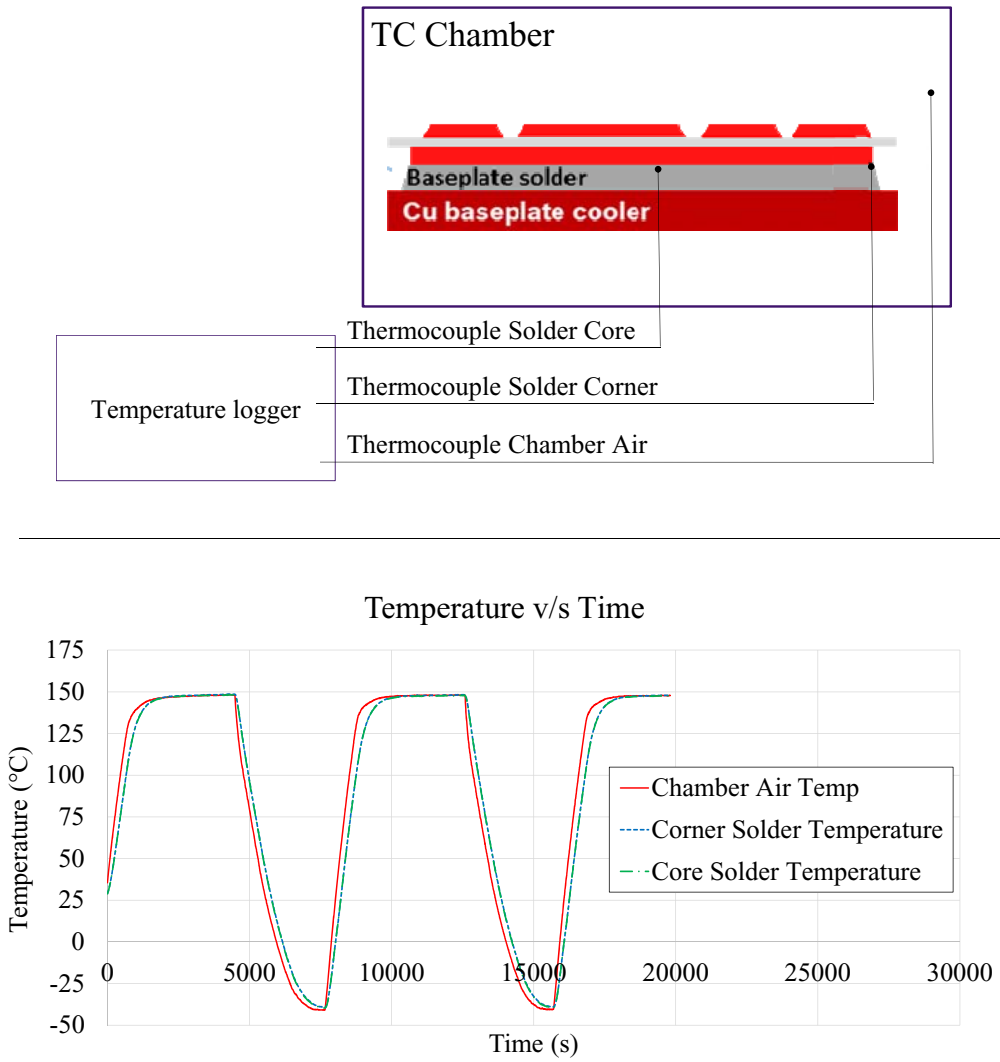


Figure 5.16: Temperature distribution of DoE sample and TC chamber air

Consequent to the above discussion, the temperature loading on the DoE samples in the FEM model is applied as a uniform heating (and cooling) of the entire sample (no transient thermal simulation is required/carried out). The applied temperature was directly logged from the TC chambers in which the samples were aged. The thermal load was applied as a piecewise linear approximation of the temperatures logged in the TC chamber. Figure 5.17 shows FEM temperature loads for the three used temperature cycling profiles.

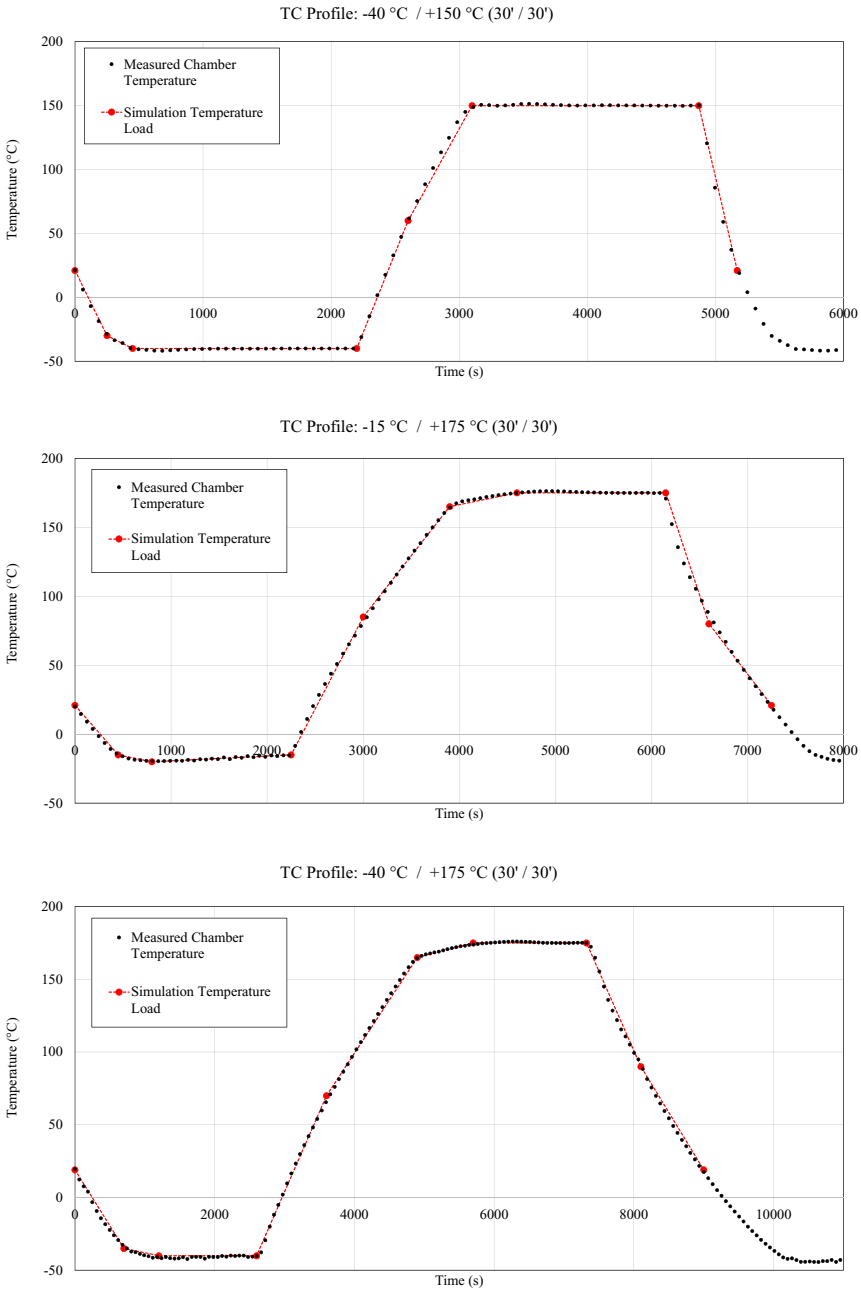


Figure 5.17: Temperature loading for FEM

5.4.1.2 Model and mechanical boundary conditions

FEM model, loading profile and boundary conditions are illustrated in Figure 5.18. Taking advantage of the symmetric structure of the DoE variants, quarter-symmetric models are built up with symmetry boundary conditions applied to the surfaces on the planes of symmetry.

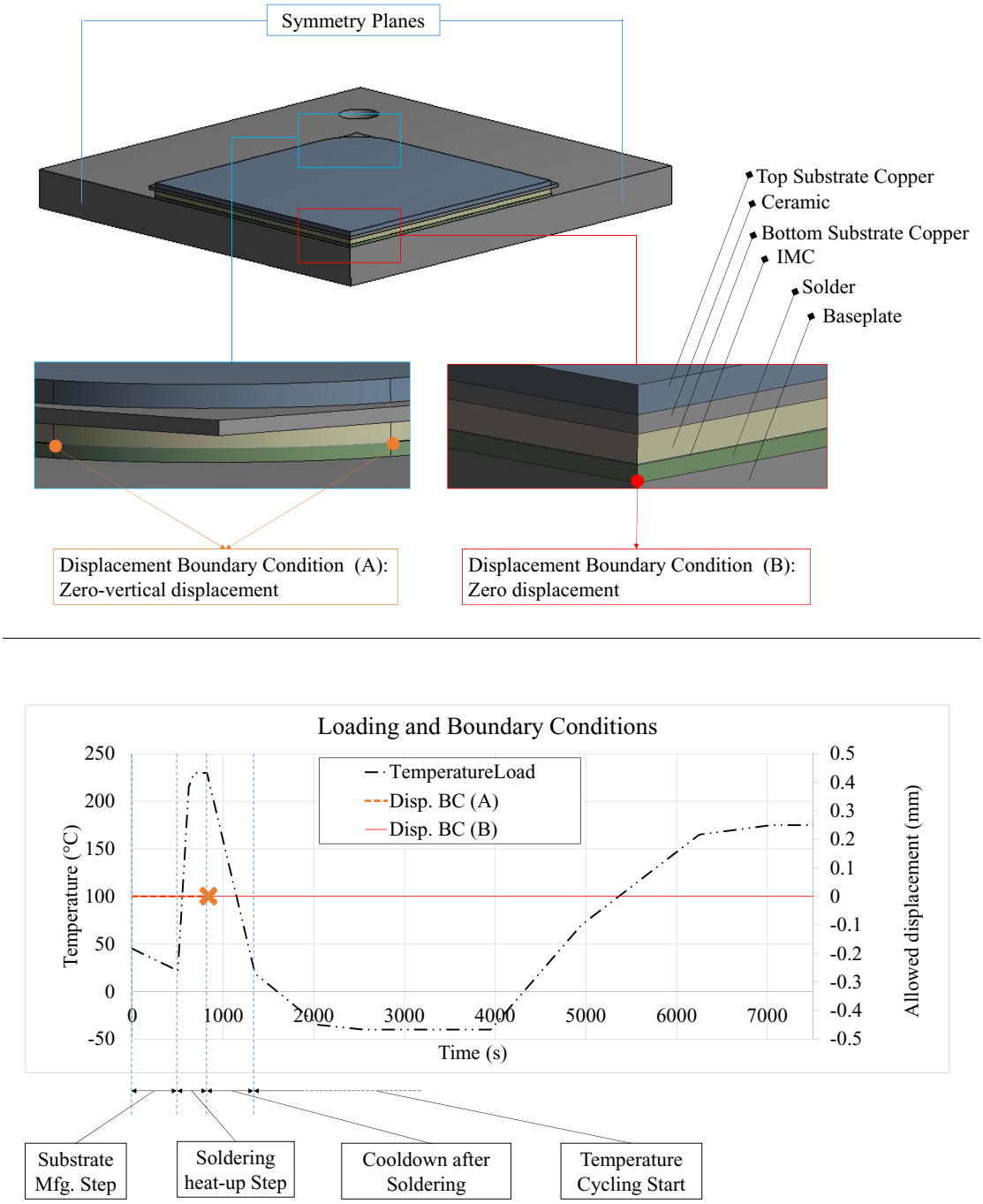


Figure 5.18: Temperature loading for FEM

Apart from the necessary zero displacement boundary condition applied at the intersection of the symmetry planes, zero vertical displacement boundary condition is applied on the bottom side of the substrate corner during the soldering process simulation which helps in numerical stability of the model and the build-up of substrate warpage.

5.5 Lifetime estimation

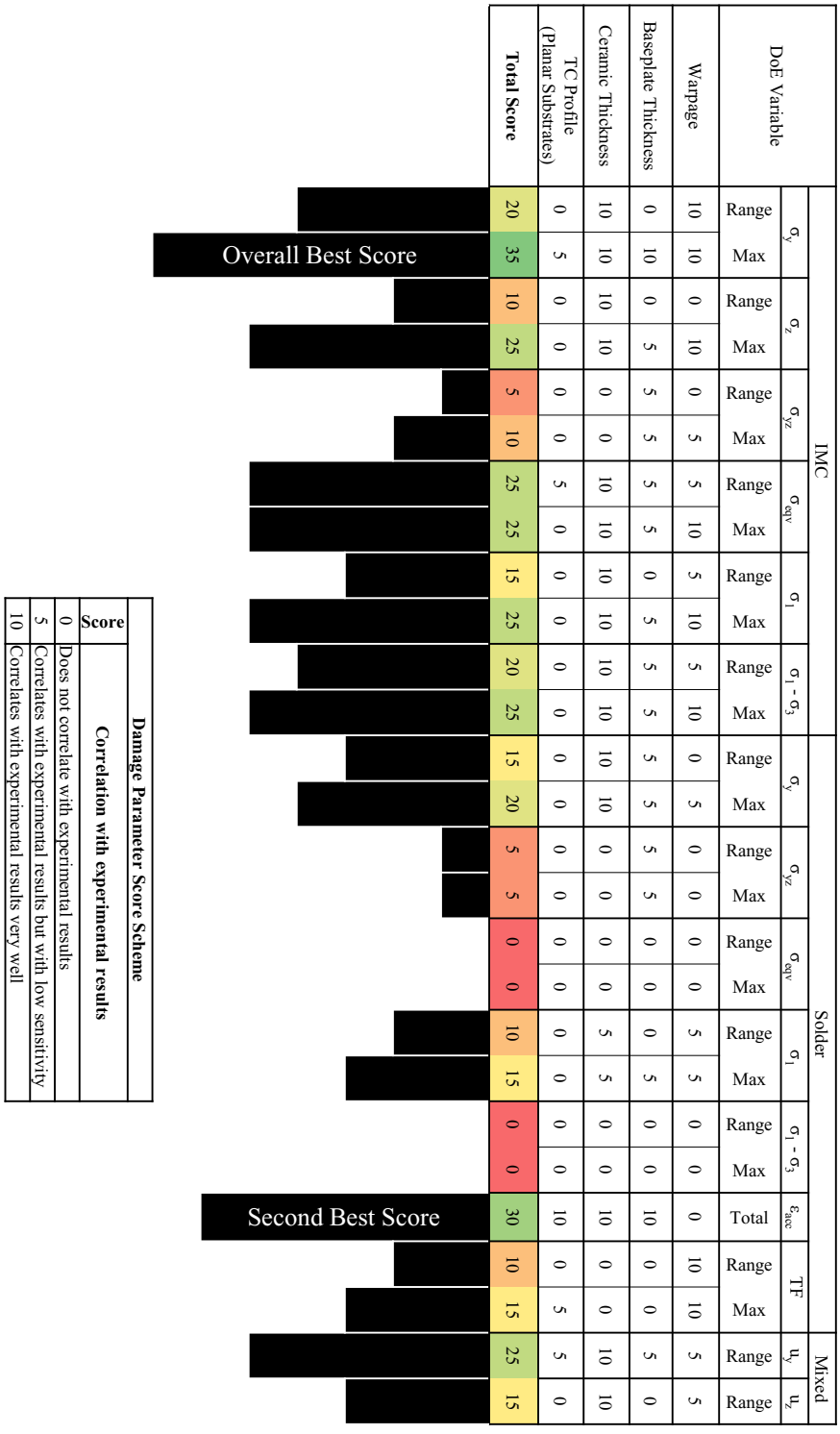
5.5.1 Damage parameters survey

For predicting lifetime through simulations, an appropriate simulative damage parameter needs to be found that satisfactorily describes the failure mechanism, crack growth and lifetime characteristics. Multiple potential damage parameters were surveyed in this research work which are tabulated in Table 5.3.

Table 5.3: Surveyed damage parameters for lifetime estimation

Damage parameter	**Type**	**Description**	**Assessed component**
σ_y	Maximum & Range per TC	Normal stress (out-of-solder plane)	IMC & solder
σ_z	Maximum & Range per TC	Normal stress (along solder diagonal)	IMC & solder
σ_{yz}	Maximum & Range per TC	Shear stress (in solder plane)	IMC & solder
σ_{eqv}	Maximum & Range per TC	Equivalent stress (von-Mises)	IMC & Solder
σ_1	Maximum & Range per TC	First principal stress (Principal planes)	IMC & solder
$\sigma_1 - \sigma_3$	Maximum & Range per TC	Max. shear stress (Principal planes)	IMC & solder
ε_{acc}	Total & Range per TC	Accumulated inelastic strain	Solder
$\sigma_1 - \sigma_3$	Maximum & Range per TC	Max. shear stress (Principal planes)	IMC & solder
TF	Maximum & Range per TC	Stress triaxiality	Solder
u_z	Range per TC	Relative displacement (out-of-solder plane)	IMC & solder
u_z	Range per TC	Relative displacement (along solder diagonal)	IMC & solder

These damage parameters were evaluated to check if they represented the crack growth characteristics for the major influence parameters as seen in the TC results (ref. Section 5.3), *viz.* influence of warpage, baseplate thickness, ceramic thickness and temperature profile. Each damage parameter was scored on its ability to correlate well with the experimental results. The summary of the damage parameter rating is shown in Figure 5.19.



DoE Variable		IMC								Solder								Mixed	
		σ_y		σ_z		σ_{yz}		σ_{eqv}		σ_1		$\sigma_1 - \sigma_3$		σ_y		σ_{yz}		σ_{eqv}	
Warpage	Range	10		0		0		5		5		5		0		0		0	
	Max	10		0		5		10		10		10		5		5		0	
Baseplate Thickness	Range	0		0		5		5		0		5		5		5		0	
	Max	10		5		5		5		5		5		5		5		0	
Ceramic Thickness	Range	10		10		0		10		10		10		10		0		0	
	Max	10		10		0		10		10		10		10		0		0	
TC Profile (Planar Substrates)	Range	0		0		0		5		0		0		0		0		0	
	Max	5		0		0		0		0		0		0		0		0	
Total Score		20	35	10	25	5	10	25	25	15	25	20	25	15	20	5	5	0	0

DoE Variable		Solder						Mixed	
		σ_1		$\sigma_1 - \sigma_3$		ε_{acc}	TF	u_y	u_z
Warpage	Range	5		0		0	10	5	5
	Max	5		0		10	10	5	5
Baseplate Thickness	Range	0		0		10	0	5	0
	Max	5		0		10	0	5	0
Ceramic Thickness	Range	5		0		10	0	10	10
	Max	5		0		10	0	5	10
TC Profile (Planar Substrates)	Range	0		0		10	0	5	0
	Max	0		0		10	5	5	0
Total Score		10	15	0	0	30	10	15	25	15

Damage Parameter Score Scheme	
Score	**Correlation with experimental results**
0	Does not correlate with experimental results
5	Correlates with experimental results but with low sensitivity
10	Correlates with experimental results very well

Figure 5.19: Damage parameter suitability rating

It can be seen from Figure 5.19 that among the various damage parameters that were surveyed, normal stress in the out-of-solder-plane direction evaluated in the IMC layer (σ_y) and the accumulated plastic strain in the solder layer (ε_{acc}) showed the best correlation with the experimental results in most cases. However, these two indicators are not comprehensive. σ_y showed good sensitivity towards different physical variants but *only within* a given temperature profile. For example, ideally, for two identical geometries, normal stress under -40 °C / 175 °C profile should be significantly higher than in -40 °C / 150 °C profile as -40 °C / 175 °C profile results in a much larger delaminated area (ref. Section 5.3.7). However, this was not the case as observed in simulations which can be seen in Figure 5.20(a). Therefore σ_y cannot be used as a universal damage parameter for variants *across all* TC profiles.

It was also known from the experiments that samples with concavely warped substrates show faster degradation as compared to planar substrates (ref. Section 5.3.1). However, accumulated plastic strain (ε_{acc}) for samples with planar substrates was in fact lower than that for samples with concave substrates (see Figure 5.20(b)). This again therefore, cannot be used as a universal damage parameter as it fails to describe a key influence parameter. Consequently, instead of the conventional lifetime models (ref. Section 2.3.4.2), a damage parameter combining both, stress and strain states within the solder was sought.

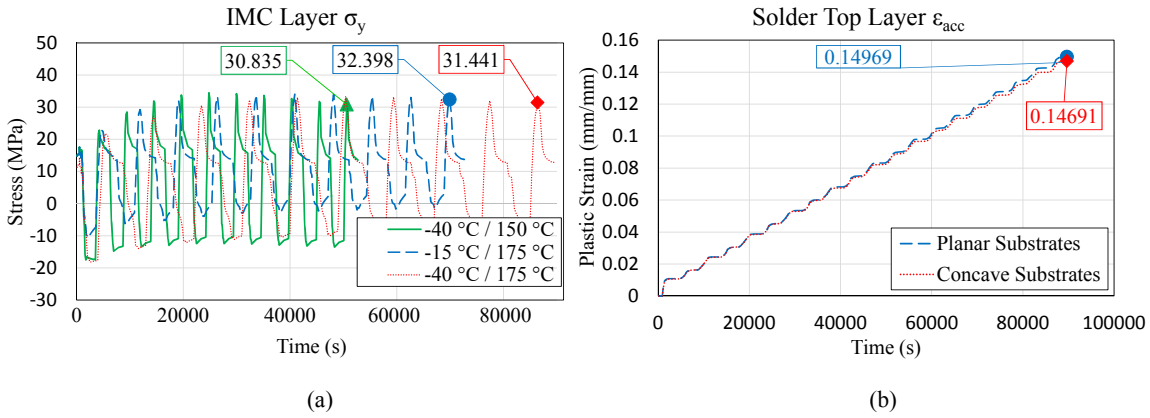


Figure 5.20: Problems with σ_y and ε_{acc} as damage parameters

Studies by [MKB68; RT69; Gur77], have revealed that damage in ductile materials is often the result of nucleation and subsequent coalescence of microscopic voids. This trend is accelerated under high tensile triaxiality of stress. As a result, ductile materials subjected to high tensile triaxiality exhibit an increasingly brittle response [YK93; ZMD93]. Experimental studies by [Zhe+93; BW04; BW05] have shown that in addition to tensile triaxiality, compressive triaxiality can also contribute to damage. A number of researchers have found computational/numerical evidence to support this observation notable among which are [Kwe12; Xue07; NH08; NT09].

[DC59] proposed a method to quantify stress triaxiality using the term Stress Triaxiality Factor (TF) which was defined as the ratio between the hydrostatic component of the stress tensor to the von-Mises stress as in Equation (5.2). According to [Sam+18; Geo+18], for $TF > 1$, tensile loading dominates. For small positive values ($1 > TF > 0$), a mixed tensile and shear loading is encountered. For $-1/3 < TF < 0$, mixed shear and compressive loads are present. For $TF < -1/3$, compressive load is dominant. It has been reported in literature

that accounting for stress triaxiality has led to an improvement in the accuracy of the lifetime prediction in solder joints [Kuc+15; Kuc+16].

$$TF = \frac{\sigma_1 + \sigma_2 + \sigma_3}{\sqrt{\frac{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}{2}}} \tag{5.2}$$

It was found that during temperature cycling the simulated stress triaxiality (TF) in the samples used in this research work (TF) varied between -2.12 and +1.25. Such a large range of TF as seen in simulations means that DoE variants in this research work experience a high degree of triaxiality in each temperature cycle [Geo+18]. A methodology to account for such triaxiality effects has been proposed by Mason and Hardford [MH77] by a so called multiaxiality correction factor (MF) as shown in Equation (5.3)

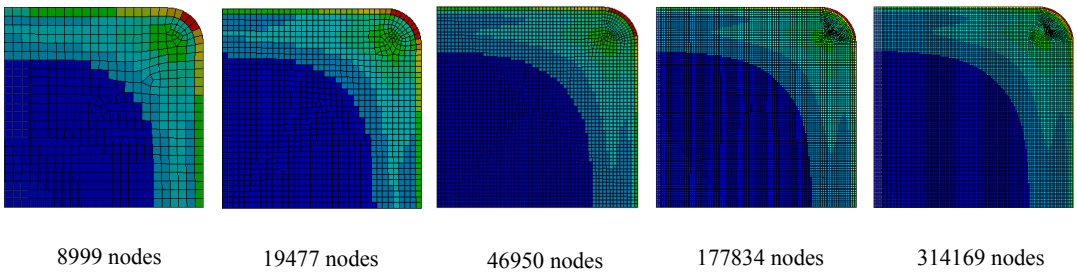
$$\begin{aligned} MF &= TF && for \quad TF \geq 1 \\ &= \frac{1}{(2 - TF)} && for \quad TF < 1 \\ \Delta^* \varepsilon_{pl} &= MF \cdot \Delta \varepsilon_{pl} \end{aligned} \tag{5.3}$$

where $\Delta \varepsilon_{pl}$ is the plastic strain range per cycle. Multiaxiality corrected plastic strain ($\Delta^* \varepsilon_{pl}$) was found to be able to represent the delamination behaviour of all physical variants successfully and also across all temperature cycling profiles. The details about the damage evaluation procedure is mentioned in the following sections.

5.5.2 Damage evaluation

5.5.2.1 Mesh dependence and work-around

In models with regions with stress singularities, mesh dependence of FEM simulation results is a known problem. Prime candidates for the such stress singularities are sharp edges in load bearing parts of the geometry and materials interfaces. As the evaluated area of interest in the samples considered in this study are cracks at/near the interface between IMC and solder, a mesh dependence check was important. For this purpose, an FEM model was constructed using different mesh densities and the build-up of plastic strain in the solder layer was calculated for a temperature change from 25 °C to 175 °C. Figure 5.21(red) shows that, as expected, FEM result parameters (e.g. maximum plastic stain) exhibited a strong dependence on mesh density (size of the FEM elements). Smaller the element size, larger is the value of the plastic strain. This mesh dependence of result parameters can however, be overcome using the so-called Volume Weighted Averaging (VWA) method. This method takes advantage of the fact that as the element density is increased, the value of the result variable, such as stress or strain increases, but occupies a smaller and smaller volume concentrating itself near the singularity. The VWA method can be mathematically expressed as in Equation (5.4) where, n is the number of elements over which the volume averaging is done. $(\varepsilon_{pl})_i$ and V_i are the plastic strain and the volume of the $i - th$ element.



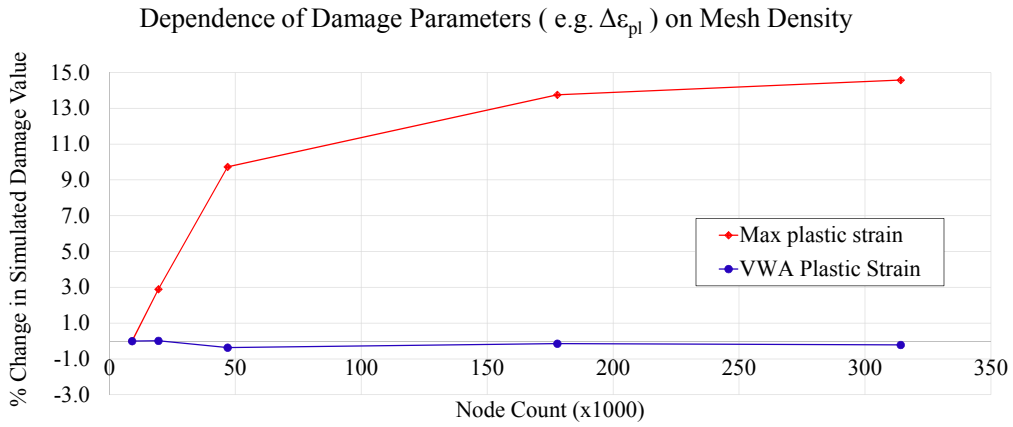


Figure 5.21: Mesh dependence of FEM result parameters (plastic strain shown here as example)

$$(\varepsilon_{pl})_{VWA} = \frac{\sum_{i=1}^{n} [(\varepsilon_{pl})_i \cdot V_i]}{\sum_{i=1}^{n} V_i} \tag{5.4}$$

Figure 5.21(blue) clearly shows that mesh dependence of the FEM result variable after VWA method is negligible (here the example of plastic strain is provided). While the element density increased 35x from ~9000 element nodes to ~314000, the result variable showed a change of less than 0.5%.

5.5.2.2 Cycles to stable hysteresis

As discussed in Section 2.3.4.2, evaluation of damage parameters in components undergoing cycling loading is done when the hysteresis loop exhibited in the stress-strain plot stabilizes. For small solder joints such as in chip scale packages, the stabilization is reached after about three simulative temperature cycles [PS08]. In the case of baseplate solder however, due to its much larger size, it was possible that stabilization took a greater number of cycles. The FEM model was cycled for 45 temperature cycles and the volume weighted average of the plastic strain accumulated over one TC was calculated at various intervals.

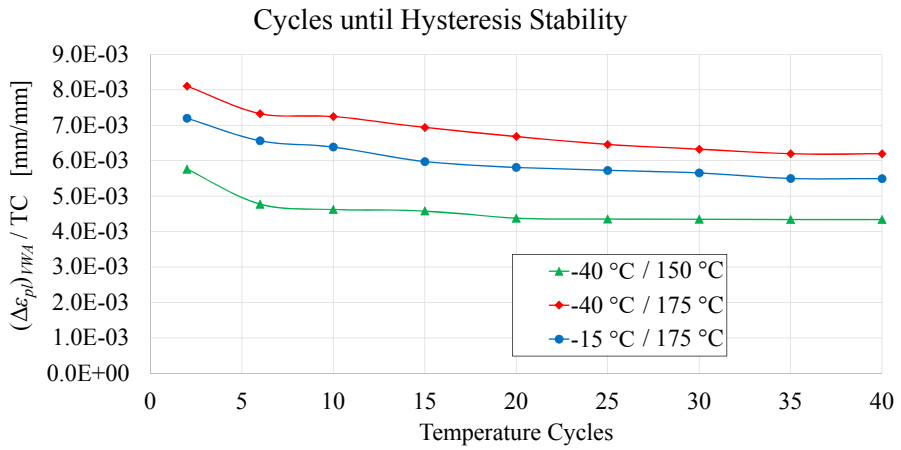


Figure 5.22: Simulative number of temperature cycles required until hysteresis loop stabilizes

Figure 5.22 shows that unlike chip scale packages, baseplate soldered components require many more cycles to reach hysteresis stability. In the case of samples in this study, up to 35 cycles were required. As a result, FEM models of all DoE samples are subjected to 40 simulative temperature cycles and the evaluation of damage is done on the 40th temperature cycle.

To summarize the discussion in the previous sections, a suitable damage parameter was determined, a method for avoiding mesh dependence was implemented and the number of cycles to hysteresis stability was also found out. As a result, an accurate and repeatable calculation of damage could now be made and is discussed in the following section.

5.5.2.3 Calculation of damage parameter for lifetime prediction

Lifetime prediction through FEM simulations for low cycle fatigue primarily employ the Coffin-Manson equation [Cof54; Man53] where the failures can be described in terms of plastic strain. Recall Equation (2.11).

$$N_f = C_1 \cdot (\Delta\varepsilon_{pl})^{C_2}$$

We have however already seen that plastic strain exclusively, did not describe the failures in samples in this research work. Such a case is not uncommon in research concerning fatigue failure in solder joints. This is because the Coffin-Manson Equation assumes that plastic strain is the only contributing factor to damage. The Coffin-Manson equation is a subset of a more general lifetime prediction model where a damage function $\hat{\Psi}$, combining various damage parameters are used in the form such as in Equation (5.5).

$$N_f = C_1 \cdot \left[\hat{\Psi}(\varepsilon, \sigma, E \cdots)\right]^{C_2} \tag{5.5}$$

In section 5.5.1, it was discussed that triaxiality corrected plastic strain demonstrated the best correlation to experimental lifetimes of various samples that underwent temperature cycling. For the lifetime model proposed in this research, triaxiality corrected plastic strain averaged

over a stabilized temperature cycle was developed as the damage function $\hat{\Psi}$. Mathematically it can be expresses as Equation (5.6).

$$\hat{\Psi} = \left[\frac{\int_{t_{TCstart}}^{t_{TCend}} (MF \cdot \varepsilon_{pl}) dt}{t} \right] \tag{5.6}$$

To avoid mesh dependence, $MF \cdot \varepsilon_{pl}$ is volume weighted averaged over 50% of the most loaded/damaged elements in the solder layer near the IMC-solder interface, *i.e.* for $\sum_{i=1}^{n} V_i$ in Equation (5.4), n is such that $\sum_{i=1}^{n} V_i \leq 0.5 V_{tot}$, V_{tot} being the total volume of the solder joint elements at the IMC-solder interface. The averaging volume is set to be 50% as the failure criterion for the experimental determination of N_f was also set to be 50% delamination in the solder. Using Equation (5.6) in Equation (5.5) yields, the lifetime equation presented in this study

$$N_f = C_1 \cdot \left[\frac{\int_{t_{TCstart}}^{t_{TCend}} (MF \cdot \varepsilon_{pl}) dt}{t} \right]^{C_2} \tag{5.7}$$

For each sample investigated in this study, N_f was experimentally determined. The same samples were also simulated and $\hat{\Psi}$ calculated according to Equation (5.6) using an APDL post processing script as shown in Appendix C. A plot of all the relevant DoE samples with $\hat{\Psi}$ on the x-axis and N_f on the y-axis is shown in Figure 5.23. Using linear regression, the fitting parameters were determined as $C_1 = 2.078$ and $C_2 = -1.172$.

$$N_f = 2.078 \cdot \left[\frac{\int_{t_{TCstart}}^{t_{TCend}} (MF \cdot \varepsilon_{pl}) dt}{t} \right]^{-1.172} \tag{5.8}$$

The final lifetime model equation as obtained by correlating the experimental life and the simulated damage parameter is expressed in Equation (5.8) and shown in Figure 5.23.

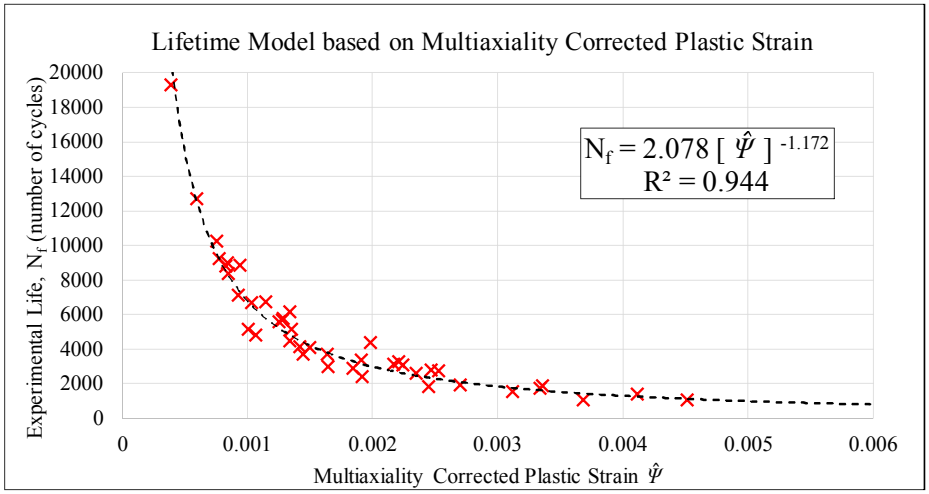


Figure 5.23: Lifetime model for baseplate soldered components under passive TC

As seen from Figure 5.23, the R-squared value (also called co-efficient of determination in statistics) of the lifetime curve that fits the experimental and simulative data was R^2 = 0.944, indicating an extremely good fit. In addition, the correlation coefficient calculated for the predicted and observed life of the investigated samples was r = 0.98, which indicates a highly significant correlation between the predicted and observed TC lives. These statistical indicators reinforce the confidence in the predictive capacity of the derived lifetime model.

As a further verification of the utility of the proposed lifetime equation, two examples are worked out. Both these examples correspond to samples that were not included in the derivation of the lifetime equation.

Example 1: Variant with substrate size 22 mm x 22 mm

Recall from Section 5.3.4.1 that the smallest substrate investigated in the DoE was the 30 mm x 30 mm sized substrate. Another variant available outside the scope of the DoE of this research work was a 22 mm x 22 mm substrate. However, SAM data for only 0 TC and 250 TC under -40 °C / 175 °C was available. Therefore, an experimental estimation of end-of-life (50% delamination) was not readily possible. The thickness of the solder joint and the dimensions of the copper baseplate were the same as in the samples described in Section 5.3.4.1.

It was observed that for planar substrates, all other influence factors kept unchanged, the absolute delaminated area of the solder joint was roughly the same, regardless of the lateral size or aspect ratio of the solder joint. The equations relating the delaminated area and the number of temperature cycles was also provided for each variant. From this data, an averaged rate of delamination can be easily calculated. This is shown in Equation (5.9) where *Delaminated Area* is in mm^2.

$$Delaminated\ Area = 0.0338\,(TC)^{1.355} \tag{5.9}$$

According to Equation (5.9), at 250 TC, 59.9 mm^2 of the solder area should have delaminated. As mentioned before, SAM images at 250 TC were available. In the SAM images, the samples showed a percentage delamination of 13.8% and 13.4% respectively. The lateral area of the solder joint for this variant was 383* mm^2. This corresponds to an absolute delamination of 52.9 mm^2 and 51.3 mm^2. This is close to the delamination estimated by Equation (5.9) and therefore, one can assume that the behaviour of delamination rate, at least as shown by evidence at 250 TC, holds true for the 22 mm x 22 mm substrate size as for other planar substrate sizes.

In light of the above discussion, Equation (5.9) can now be used to determine the number temperature cycles it would take for the solder layer beneath the 22 mm x 22 mm substrate to delaminate by 50% (383 mm^2 / 2 = 191.5 mm^2). The number of temperature cycles thus calculated was 588 cycles. This assembly was then simulated using the methodology detailed in this research work and a damage value of $\hat{\Psi}$ = 8.0518 x 10^{-03} was calculated from the FEM simulation. Plugging in this value into the lifetime equation (Equation (5.8)) yields a lifetime of $N_f = 592$ which is remarkably close to the experimentally deduced lifetime.

*area of the solder joint (383 mm^2) is smaller than the area of the substrate (22 mm x 22mm = 484 mm^2) due the space between the edge of the AMB copper and edge of the ceramic. Also, corners of the AMB copper are rounded off.

Example 2: Variant with warpage (Top side Cu, ceramic and bottom side Cu thickness of 0.50 mm, 0.32 mm and 0.57 mm respectively

Solder delamination with substrates with concave warpage at high temperature was investigated through a substrate that had top side Cu, ceramic and bottom side Cu thickness of 0.30 mm, 0.32 mm and 0.50 mm respectively. In addition to this, a second variant with top side Cu, ceramic and bottom side Cu thickness of 0.50 mm, 0.32 mm and 0.57 mm respectively was also investigated. It was subjected to temperature cycling under the -40 °C / 175 °C profile for 1500 TC. The delamination curve for this variant is shown in Figure 5.24.

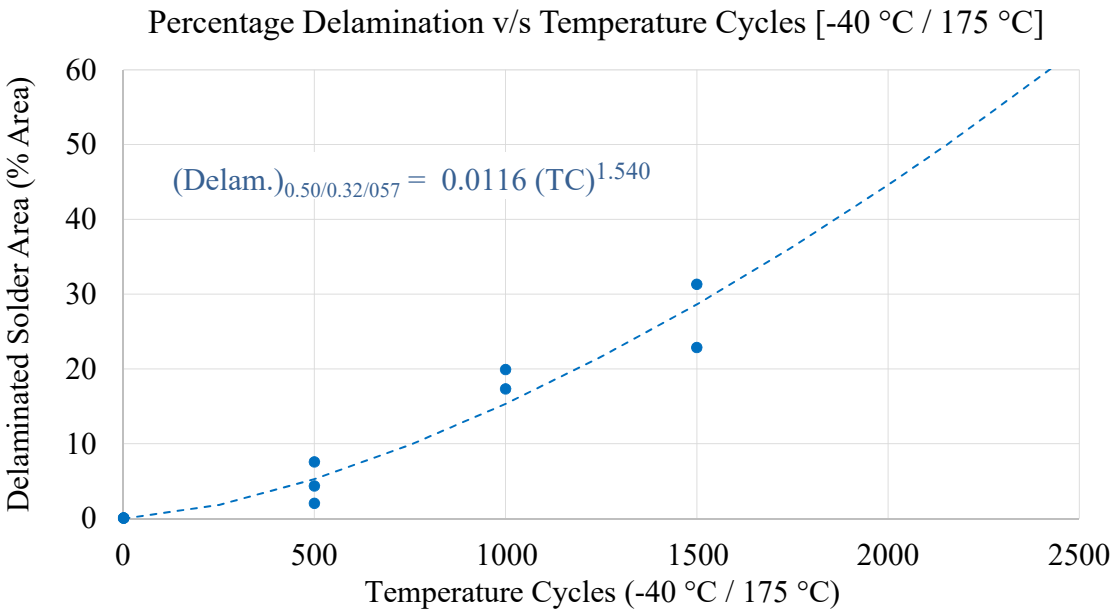


Figure 5.24: Delamination curve under passive temperature cycling for sample in example 2

From this curve, an end-of-life (50% delamination) was calculated to be 2153 cycles. As with other samples, this assembly was also simulated and a damage value of $\hat{\Psi} = 2.843 \text{ x } 10^{-03}$ was calculated from the FEM simulation. Using this value in Equation (5.8) yields a lifetime of $N_f = 2004$ which is only 6.9% away from the experimentally determined life which again is a very good estimate.

Conventional solder joint lifetime models for baseplate solder joints do not account for stress triaxiality and as seen in previous sections, are unable to predict solder joint lifetime with an acceptable degree of accuracy. In some cases, they do not represent the experimental observations at all. As seen from verifications through statistical parameters and worked out examples, the lifetime equation derived in this doctoral work greatly improves upon conventional methods and provides a robust methodology to accurately predict the reliability of baseplate solder joints.

When you reach the end of what you should know, you will be at the beginning of what you should sense.

Kahlil Gibran (1883 – 1931)
Lebanese writer and poet

Chapter 6

Conclusion

6.1 Summary

In this doctoral research work, an extensive investigation was carried out regarding reliability of large area solder joints in power modules used in inverter units under passive temperature cycling loads. The study attempts to better understand the failure mechanism and the various geometrical features and loading conditions that influence the growth of cracks in these solder joints. Furthermore, the study also aimed at developing an FEM based predictive model for lifetime estimation. The major results and corresponding references within this thesis are provided below.

One of the first observations even before the availability of reliability testing results was that of warpage of AMB substrates and baseplates after soldering. With regard to the AMB substrates, it was shown that unequal amounts of copper on the top and bottom side of the substrate ceramic (for example due to etching) would lead to substrate warpage depending on temperature (Figure 3.6). In the case of baseplates however, warpage was consistently found to be convex and a description of the mechanism explaining baseplate warpage was also provided (Figure 3.8).

To predict and account for the warpage of substrates and baseplate during the AMB manufacturing and baseplate soldering processes, an FEM simulation methodology was developed. Very good estimates of warpage (Figure 3.29) and as a consequence, variable solder thickness (Figure 3.30) was made possible using these simulations. This meant that the post soldering stress state of solder could be satisfactorily accounted for in FEM simulations which would later be developed further to also include lifetime prediction capabilities.

Having established a robust FEM methodology to account for the soldering process, attention was turned to the failure mechanism seen during TC tests. It was observed that the cracks in baseplate soldered components occurred almost exclusively at or near the interface of the solder and the IMC layer (Figure 5.3). A study on IMC growth and its role on reliability of baseplate soldered components was thus carried out. Academic literature does suggest that with increasing IMC thickness, solder joints became less reliable; however, process conditions, solder material, solder joints size and ageing conditions were vastly different from the components dealt with in this study. An attempt was therefore made

to investigate the influence of soldering profiles and isothermal ageing conditions on IMC thickness and subsequently the influence of IMC thickness on reliability was investigated via FEM simulations.

It was shown that within the range of the soldering process parameters, soldering profiles had only a minor influence on the thickness of the IMC layer both before and after isothermal thermal ageing. Ageing temperature and duration were the main influence factors concerning IMC growth (Figure 4.3). A finite difference based method was developed (Figure 4.6) to transfer isothermal ageing results to non-isothermal cases which can be especially useful in predicting IMC thickness in case of active and passive TCs.

The influence of IMC layer thickness on the stress state at crack prone locations was carried out using FEM simulations employing the sub-modelling technique. In almost all cases, evaluated damage parameters showed an increase with increasing IMC thickness (Figure 4.11). The simulations also showed that the influence of IMC thickness on the increase in stress values was greatest near the IMC layer and that this influence decreased as one moved away from the IMC layer and further into the solder bulk (Figure 4.12). Based on these results, FEM models for lifetime prediction were built *with* an IMC layer which is otherwise, usually neglected in lifetime prediction FEM simulations.

The largest portion of this research work comprised the reliability investigation and the derivation of a lifetime model for baseplate soldered components. A detailed investigation on the influence of different passive TC profiles and geometric features of baseplate soldered components was carried out. The investigated DoE variants showed a strong dependence on the variation items and a physical explanation of the observed behaviour was provided in Section 5.3.

As far as TC profiles are concerned, it was shown that both, temperature swing and peak temperature play significant and independent roles in solder degradation. This shows that the conventional and very popular empirical lifetime prediction model, the Coffin-Manson model, could result in large errors in lifetime prediction as it considers only temperature swing (Figure 5.15).

With regard to the influence of geometric features (Figure 5.6 through Figure 5.14), concave warpage of substrates (at high temperature), increasing the thickness of the AMB ceramic layer, structuring the bottom side of AMB copper and increasing the thickness of the baseplate-all result in the acceleration of solder delamination. Within the range of investigated substrate sizes, absolute value of delaminated solder area was found to be independent of substrate size and consequently, *percentage value* of delaminated solder area was highest in small substrates. This meant that if the end of life criteria is set to a given percentage delamination value (which is usually the case) smaller substrates would fail earlier. Solder bondline thickness showed a minor influence on the lifetime. A trend was noted that thicker solder joints appeared to delaminate slightly faster, especially under the -40 °C / 175 °C TC profile. However, further confirmation of this effect needs to be carried out.

Following the experimental reliability investigation, an FEM simulation methodology was developed to predict the lifetime of baseplate soldered components. It was found that conventional FEM damage parameters used to predict lifetime such as accumulated inelastic strain per cycle and strain energy per cycle was ineffective in predicting lifetime satisfactorily (Figure 5.19 and Figure 5.20). Among the many evaluated damage parameters, the one

accounting for both plastic strain and stress triaxiality, the so called *triaxiality corrected accumulated plastic strain per cycle* was extracted. This damage parameter showed excellent correlation with experimental EoLs, and subsequently, a lifetime prediction equation was also provided (Figure 5.23). This lifetime model is a powerful and useful tool. A new product design that is to be baseplate soldered, even with a relatively large number of changes in its geometrical features or loading conditions can be quickly and economically estimated using FEM simulations without having to wait for costly and time consuming experimental results to be completed.

To summarize, this work has brought forth a sizeable amount of new information and ideas.

Firstly, the research provided a numerically simple and accurate method and subsequently developed a tool for the prediction of IMC thickness for not just isothermal cases, as was the case for most studies in the field of IMC growth, but also for non-isothermal cases. As shown in this study, the IMC thickness calculation tool can also help in ascertaining the number of temperature cycles until crack initiation, a unique application not yet explored.

Secondly, this study systematically studied the effect of IMC thickness on reliability for large area solder joints. As a result, it settles the debate whether an IMC layer should be modelled in FEM simulation models or not. The study clearly presented under which failure modes IMC layer must be modelled and under which ones, IMC layer may be omitted.

Thirdly, the depth to which substrate and baseplate warpage has been investigated in this study is unprecedented. This also includes a robust manufacturing process simulation for baseplate soldering with respect to warpage to account residual thermal stresses as extensively as possible.

Fourthly, as many as sixty different configurations of baseplate soldered components under passive temperature cycling have been investigated in this study. Such a collection of extensive reliability data is simply not available in contemporary scientific or technical literature and is a sizeable addition to the understanding of this field.

Finally, a new FEM based damage parameter has been proposed in this study as conventional damage parameters failed to explain/predict experimental observations. Based on this damage parameter, a lifetime model for baseplate solder layer is derived, the likes of which are currently not available.

As a part of future investigations, the following points show the scope for further development

6.2 Future Scope

A wide variety of influence factors were investigated in this research work and important and useful results were worked out. However, the technical and scientific landscape of baseplate soldering and its reliability is rich and wide. It is therefore no surprise that there are many topics that are ripe for further investigations. Some of these topics are especially interesting and are discussed below.

- **Change in IMC morphology**: It was shown through FEM simulations that increasing IMC thickness has a negative influence on baseplate soldering reliability. In the FEM

simulation models in this research, the thickness of the IMC layer was kept constant throughout its surface, *i.e.*, surface roughness of the IMC was not accounted for. It is known however that the IMC morphology, especially the Cu_6Sn_5 on the micro scale, has a rough scalloped structure and that as the IMC grows, the surface becomes smoother. From the FEM simulations, the contribution of increasing IMC thickness towards increasing damage in solder was proven but the contribution of the change in morphology of the IMC layer from rough to smooth was not investigated. One can conjecture that with increasing smoothness of the IMC layer the total surface energy of the solder-IMC interface would decrease and therefore would make crack growth easier. This is another area that could be worked on.

- **Solder layer influence**: One of the design variations in the DoE was the variation of the solder layer. With regard to change in solder thickness, there is sparse evidence in literature that reducing the solder thickness could potentially improve reliability of baseplate solder joints. The experimental and simulative evidence in this study also showed a similar trend but not with conclusive confidence. If this effect is true, it is also important to determine until what limits the failure mode of interfacial delamination continues. It is expected that as the solder layer becomes thinner, the failure path may switch from IMC-solder interface to bulk solder and result in an altered (possibly reduced) lifetime. In this sense, one may argue that there lies an optimal solder layer thickness that provided maximum lifetime under passive temperature cycling. The influence of solder thickness needs to be further verified. One may also build variable solder joint thicknesses using partially etched structures on the bottom side copper of the substrate. This possibility has not been studied in this research work and can be further investigated in the future.

  At the time of this study, the shape of the solder meniscus could not be reliably reproduced and therefore for was left out of the DoE. With appropriate solder stops and soldering fixtures, good control over solder meniscus can be realised. Solder meniscus is therefore another design parameter that could potentially be varied and the corresponding influence on reliability studied.

  In this study substrates sizes from 70 mm x 70 mm to 30 mm x 30 mm were investigated. Within this range absolute delaminated solder area was shown to be independent of solder joint area. The failure mode was cracking at/near the IMC solder interface. However, chip scale packages are well known to have cracks in the bulk of the solder joint. This means that as we continue to decrease substrate size (consequently solder joint size), the failure mechanism could switch. This critical size is not determined in this study and would be an interesting and useful addition to this work.

- **Baseplate materials and its finishing for non wettable surfaces**: Copper has been popular as a baseplate material due to its high thermal conductivity, non-reactivity with coolants, solder wettable surface and its easy large scale production and machinability. However, Aluminium has also emerged in the meanwhile as a strong contender due to its cost and weight benefits as it is approximately 3 times cheaper and lighter than copper. However Aluminium has a higher CTE than copper and a lower yield strength. This means that large scale plastic deformation and warpage can be expected. The question then arises if the damage parameter derived in this work would still hold. This question needs to be addressed via reliability testing with aluminium baseplates, material characterisation of aluminium used in baseplates and subsequent FEM modelling.

  Among other materials, Aluminium - Silicon carbide metal matrix composite, also known as AlSiC is also found to have been used as baseplate materials, although to a smaller

extend. The main advantage of AlSiC is that the CTE of the material can be tailored to requirement based on the relative proportion of the aluminium matrix and the SiC particles. AlSiC however is a very stiff material and the effect of such elevated stiffness on baseplate solder reliability and a potential change in failure mechanism is yet to be investigated.

It must be also be kept in mind that both Aluminium and AlSiC are not wettable by solder and that they therefore, need to be plated such that there is a wettable surface for soldering. Consequently, the type of surface treatment, surface roughness, material diffusion - all are valid themes for further investigation.

Appendix A

Solder Priority and Decision Matrix

		Goal 1	Goal 2	Goal 3	Goal 4	Goal 5	Goal 6	Goal 7	Goal 8	Goal 9			
	Answer the following questions for each goal: Which goal is more important Goal 1 or Goal 2, Goal 1 or Goal 3, Goal 1 or Goal 4, ...	Reliability	Cost	Tmax for soldering (concern for passive component)	Preform	RoHs+ (Sb)	Process Stability (Solder splashes, Void)	Cleaning Effort	Developmental Effort	Second Supplier Source	Nominations	Rank	Weightage
Goal 1	Reliability		1	1	1	1	0	1	1	1	**7**	**2**	8.87
Goal 2	Cost	0		0	1	1	0	1	1	1	**5**	**4**	6.63
Goal 3	Tmax for soldering (concern for passive components)	0	1		1	1	0	1	1	1	**6**	**3**	7.75
Goal 4	Preform	0	0	0		1	0	1	0	1	**3**	**6**	4.37
Goal 5	RoHs+ (Sb)	0	0	0	0		0	0	0	0	**0**	**9**	1
Goal 6	Process Stability (Solder splashes, Void)	1	1	1	1	1		1	1	1	**8**	**1**	10
Goal 7	Cleaning Effort	0	0	0	0	1	0		0	0	**1**	**8**	2.13
Goal 8	Developmental Effort	0	0	0	1	1	0	1		1	**4**	**5**	5.5
Goal 9	Second Supplier Source	0	0	0	0	1	0	1	0		**2**	**7**	3.25

Must Goals		Innolot			Alloy #2			Alloy #3			Alloy #4			Alloy #5		
		Information	Yes	No	Information	Yes	No	Information	Yes	No	Information	Yes	No	Info	Yes	No
min 650 cycles -40 °C / 150 °C		Results POC II: > 1500 cycles	X		Results POC II: > 1500 cycles	X		Results POC II: >1250 cycles	x		Results POC II: > 1500 cycles	x		Results POC II:<500 cycles		x
Desired Goals	**Goal Weightage**	**Information**	Rating	Weighted Score	Information	Rating	Weighted	Information	Rating	Weighted	Information	Rating	Weighted	Info	Rating	Weighted
Reliability	9	No failures yet under -40 °C / 150 °C :1500 pTC First failures under -40 °C / 175 °C :1000 pTC	8	72	No failures yet under -40 °C / 150 °C :1500 pTC First failures under -40 °C / 175 °C :1000 pTC	8	72	First failures under -40 °C / 150 °C :1500 pTC First failures under -40 °C / 175 °C :750 pTC	2	18	No failures yet under -40 °C / 150 °C :1500 pTC First failures under -40 °C / 175 °C :500 pTC	4	36		0	0
Cost	7	Comparable to SAC	5	35	Comparable to SAC	5	35	Possibly similar in the long term to SAC, but so far more expensive	5	35	Unknown	5	35		0	0
Tmax for soldering (concern for passive components)	8	Tmax = 230 °C	8	64	Tmax = 260 °C possibly 250 °C is feasible	4	32	Tmax = 230 °C	8	64	Tmax = 240 °C	6	48		0	0
Preform	4	Available with standard flux, tested	8	32	Available with standard flux	7	28	Available with standard flux	7	28	Available without flux	4	16		0	0
RoHs+ (Sb)	1	Small proportion of Sb	4	4	Sb	2	2	No conflict known	8	8	Small proportion of Sb	4	4		0	0
Process Stability (Solder splashes, Void)	10	High proportion of voids with paste but low proportion with preform	6	60	Solder splashing (wetting, dewetting)	5	50	Dewetting	5	50	moderate void content	7	70		0	0
Cleaning Effort	3	Cleaning possible and necessary	5	15	Cleaning possible and necessary	5	15	Cleaning possible and necessary	5	15	Cleaning possible and necessary	5	15		0	0
Developmental Effort	2	Already in use, Simulation material data available	8	16	Standard solder, little experience available	6	12	little experience available	4	8	little experience available	4	8		0	0
Second Supplier Source	6	Possible	8	48	Possible	8	48	Unknown:Own development Heraeus	4	24	Unknown	4	24		0	0
Sum of weighted values:			**346**			**294**			**250**			**256**			**0**	

Appendix B

MATLAB® script for prediction of IMC thickness

```
%-------------------------------------------------
%  Code for calculating the IMC thickness for an arbitrary
   temperature profile using isothermal aging using Finite
   Difference Method
%  Allen Jose George VERSION 3.0 -- Dec 2016

%-------------------------------------------------


%------------ TC Profile INPUT-------------%


%  Read in the file with the temperature profile. The
   temperature profile sheet should be temperature (K) v/s time
    (h) and translated in the time axis such that at 0 seconds
   temperature is 32C. If working directory is the same,
   specify the file name. Else specify the entire path.
Profile     = xlsread('-40_175');
time_stamp  = Profile(:,1);             % Logged time during TC
    cycle
temp_stamp  = Profile(:,2);     % Logged temperature during TC
   cycle
data_pnts   = size(Profile,1);  % Number of data points in TC
   data log


%  TC_Dur stores the last time stamp from TC data log. As
   initial time = 0, TC_Dur also is the cycle time of the
   Temperature cycle.
TC_dur          = Profile(data_pnts,1);
TCplot(:,1)     = 0;            %Stores TC value at each time
```

```
   step
IMCplot(:,1)    = 0;            %Stores IMC thickness value at
   each time step
TEMPplot(:,1)   = 0;            %Stores temperature value at
   each time step


%  INITIAL CONDITIONS INPUT
%  NOTE: h stores current IMC thickness. Slightly offset
   initially to avoid numeric singularity from division by (h-
   h0)
delh        = 0;
delt        = TC_dur/100;        % TimeStep
time        = 0;                 % Initial time
h0          = 2.517;             % Initial IMC thickness
h           = 2.51701;
temp        = 305;               % Temp of the system (initial
   =32C)
TC_count    = 0;                 % Number of TC cycles
incr        = 0;                 % Counter
temp_max    = max(temp_stamp);   % Max temp of the TC Profile


%  ------ IMC Growth Characteristics INPUT --------%
%  Values can be determined from linear regression on
   experimental data. Refer Chapter IMC Study
Q           = 53967.5694125648;  % Activation Energy (J/mol)
R           = 8.314;             % Univ. Gas constant (J/K.mol)
A0          = 579278.314748881;  % Rate constant
n_default   = 0.5;                              % IMC growth
   time exponent


%  gives IMC thickness after 1000 TC
%  alternatively
%  while (h < 8.5 ) gives number of tCs required for IMC
   thickness to reach 8.5micrometres
while (TC_count < 1000 )
incr     = incr + 1;
% calculate current TC cycle count
TC_count = fix(time/TC_dur) + 1;


%  NOTE: Each point in any TC cycle can be traced to a
   corresponding time 'time_eqv' in the first cycle which is
   the data we input. This time_eqv is searched within the
   input profile. Temperature at the 'time_eqv' is interpolated
    between two nearest data points from the input TC Profile
time_eqv = time - (TC_count-1)* TC_dur;
```

```
for i= 1:(data_pnts-1)
if (time_eqv > time_stamp(i)  && time_eqv < time_stamp(i+1))
temp_slope  = (temp_stamp(i+1)-temp_stamp(i))/(time_stamp(i+1)-
   time_stamp(i));
temp        = temp_stamp(i) + temp_slope*(time_eqv - time_stamp
   (i));
end
end


%  NOTE: A  = Growth factor @temp
%  NOTE: delh = IMC thickness increment
n                = n_default;
A                = A0/(exp((Q)/(R*temp)));
delh             = (n*A/((h-h0)/A)^((1-n)/n))*delt;
h                = h + delh;     % New imc thickness
time             = time + delt; % Forward time stepping
TCplot(incr,1)   = time/TC_dur; % Current TC value
IMCplot(incr,1)  = h;           % current IMC thickness
TEMPplot(incr,1) = temp-273;    % current temperature value


% Various plotting options
subplot(1, 2, 1);
scatter(time, temp, 'g');
axis([0 10 200 475])
title('Temp v/s Time(-40C/175C)')
xlabel('Time (hours)')
ylabel('Temperature (K)')
drawnow;
hold on;
subplot(1, 2, 2);
scatter(time, h, 'b');
title('IMC v/s Time (-40C/175C)')
xlabel('Time (hours)')
ylabel('IMC Thickness (micrometres)')
axis([0 10 2.5 3])
drawnow;
hold on;
end


%set(gca,'XMinorTick','on');
%set(gca,'YMinorTick','on');
%plot(TCplot,IMCplot)
%title('IMC growth for TC: -40 C/175 C')
%xlabel('Temperature (K) Cycles')
%ylabel('IMC Thickness (micrometres)')
```

Appendix C

ANSYS® APDL Script for Damage evaluation

```
allsel,all
/post1
set,lastalls
TCstart=184
!Load Step at start of stabilized TC cycle
TCend=191
!Load Step at end of stabilized TC cycle
cmsel,s,Solder
!Selecting Solder elements
esel,u,cent,y,4.17,2
!Unselecting solder element layers below interface layer
*get,my_ecount,elem,,count
!Number of selected elements
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!! Result Parameters at last TC START !!
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
SET,TCstart,LAST
!Result set at start of TC cycles
*GET,TCstartTime, ACTIVE, 0, SET, Time
!Time at current result set
SABS, 0
ETABLE,tvol,VOLU
!       TABLE  1 Volume of selected elements
ETABLE,HydPrss,nl,hpres
!       TABLE  2 Hydrostatic pressure of selected elements
SMULT, HydPrss,HydPrss,,3
!       TABLE  2 updated to (Hydrostatic pressure)/3 for selected
!       elements
ETABLE,EqvStrs,s,eqv
!       TABLE  3 Equivalent Stress in selected elements
SEXP,EqvStrs,EqvStrs,,-1
```

```
!       TABLE  3 updated to (1/Equivalent Stress) in selected
!       elements
SMULT,StrTria,HydPrss,EqvStrs,1,1
!       TABLE  4 Stress Triaxiality in selected elements
ETABLE,AccStrn,nl,epeq
!       TABLE  5 Accumulated strain in selected elements
ETABLE,PlsWork,nl,plwk
!       TABLE  6 Accumulated strain in selected elements
*dim,DamStart,array,my_ecount,5
!  2D array to store element data at begining of last TC.
!  "D Array has the following structure   !
!  COL  1   |  COL  2   |   COL  3    |    COL  4     |   COL  5    |
!___________|___________|_____________|_______________|_____________|
!  El.No.   |  El.Vol.  |  El.Triax.  | El.Pl.Strain  | El.Pl.Work  |
!  El.No.   |  El.Vol.  |  El.Triax.  | El.Pl.Strain  | El.Pl.Work  |
!  El.No.   |  El.Vol.  |  El.Triax.  | El.Pl.Strain  | El.Pl.Work  |
eNumCur=0
*do,i,1,my_ecount
eNumCur=elnext(eNumCur)
DamStart(i,1) = eNumCur
*GET,DamStart(i,2), ETAB, 1, ELEM, eNumCur
!       Writing  element volume from table to array
*GET,DamStart(i,3), ETAB, 4, ELEM, eNumCur
!       Writing  stress triaxiality from table to array
*GET,DamStart(i,4), ETAB, 5, ELEM, eNumCur
!       Writing  acc. plastic strain from table to array
*GET,DamStart(i,5), ETAB, 6, ELEM, eNumCur
!       Writing  acc. plastic work from table to array
*enddo
!       uncomment below four lines if the user
!       want to print the table to a csv file
!       *cfopen,DamstartFile,csv
!       *vwrite,DamStart(1,1),DamStart(1,2),DamStart(1,3),
!       DamStart(1,4),DamStart(1,5)
!       (F16.7,',',F16.7,',',F16.7,',',F16.7,',',F16.7)
!       *cfclose
*do,i,1,my_ecount
*if, DamStart(i,3),GE,1,then
!       Calculating Multiaxiality factor (MF) from Triaxiality
DamStart(i,3)=DamStart(i,3)
!       Updating COL 3 from Elem.Triax. to Multiaxiality factor
*else
DamStart(i,3)=1/(2-DamStart(i,3))
*endif
DamStart(i,4)=DamStart(i,4)*DamStart(i,3)
!       Updating COL 4 from El.Pl.Strain to MF corrected El.Pl.Strain
*enddo
!       Start volume weighted averaging step Procedure
!       Step1: Sort array  (descending) according to the damage
```

```
!       parameter that has to be volume weighted and averaged
SortTmpVar=0
SortIniVar=0
*do,si,1,my_ecount
SortIniVar=si+1
*do,sj,SortIniVar,my_ecount
*if,DamStart(si,4),lt,DamStart(sj,4), then
!       Sorting based on DamStart(*,4)
!       DamStart(*,4) stores MF corrected Elem.Acc.Pl.Strain
SortTmpVar=DamStart(si,1)
DamStart(si,1) = DamStart(sj,1)
DamStart(sj,1)= SortTmpVar
!-------------------------------------!
SortTmpVar=DamStart(si,2)
DamStart(si,2) = DamStart(sj,2)
DamStart(sj,2)= SortTmpVar
!-------------------------------------!
SortTmpVar=DamStart(si,3)
DamStart(si,3) = DamStart(sj,3)
DamStart(sj,3)= SortTmpVar
!-------------------------------------!
SortTmpVar=DamStart(si,4)
DamStart(si,4) = DamStart(sj,4)
DamStart(sj,4)= SortTmpVar
!-------------------------------------!
SortTmpVar=DamStart(si,5)
DamStart(si,5) = DamStart(sj,5)
DamStart(sj,5)= SortTmpVar
*endif
*enddo
*enddo
!! Step 2: Volume Weighting for each element
totvol=0
!       Variable to calculate total volume of selected elements
vol_lim_prct=50
!       Averaging over highest loaded elements that contribute to
!       "vol_lim_prct"% of total volume
vol=0
!       Variable to monitor if volume limit during volume weighting
!       has reached
VWMCS=0
!       Volume weighted Damage(here MF corrected Elem.Acc.Pl.Strain)
my_VWAMCS=0
*do,i,1,my_ecount
totvol=totvol+DamStart(i,2)
!       Caclulating total volume of selected elements
*enddo
vol_limit=(vol_lim_prct/100)*totvol
!       Absolute value corresponding to "vol_limit" % volume
```

```
*do,i,1,my_ecount
*if,vol,ge,vol_limit, then
*exit
*endif
VWMCS=VWMCS+DamStart(i,2)*DamStart(i,4)
vol=vol+DamStart(i,2)
*enddo
my_start_VWAMCS= VWMCS/vol
!       my_start_VWAMCS Stores Volume Weighted Averaged
!       Multiaxiality corrected plastic strain
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!! Result Parameters at last TC End !!
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
SET,TCEnd,LAST
!Result set at End of TC cycles
*GET,TCEndTime, ACTIVE, 0, SET, Time
!Time at current result set
SABS, 0
ETABLE,tvol,VOLU
!       TABLE 1 Volume of selected elements
ETABLE,HydPrss,nl,hpres
!       TABLE 2 Hydrostatic pressure of selected elements
SMULT, HydPrss,HydPrss,,3
!       TABLE 2 updated to (Hydrostatic pressure)/3 for
!       selected elements
ETABLE,EqvStrs,s,eqv
!       TABLE 3 Equivalent Stress in selected elements
SEXP,EqvStrs,EqvStrs,,-1
!       TABLE 3 updated to (1/Equivalent Stress) in selected
!       elements
SMULT,StrTria,HydPrss,EqvStrs,1,1
!       TABLE 4 Stress Triaxiality in selected elements
ETABLE,AccStrn,nl,epeq
!       TABLE 5 Accumulated strain in selected elements
ETABLE,PlsWork,nl,plwk
!       TABLE 6 Accumulated strain in selected elements
*dim,DamEnd,array,my_ecount,5
!  2D array to store element data at begining of last TC.
!  "D Array has the following structure   !
!  COL 1  |  COL 2  |   COL 3    |    COL 4    |   COL 5   |
!_________|_________|____________|_____________|___________|
!  El.No.  |  El.Vol. |  El.Triax.  | El.Pl.Strain | El.Pl.Work |
!  El.No.  |  El.Vol. |  El.Triax.  | El.Pl.Strain | El.Pl.Work |
!  El.No.  |  El.Vol. |  El.Triax.  | El.Pl.Strain | El.Pl.Work |
eNumCur=0
*do,i,1,my_ecount
eNumCur=elnext(eNumCur)
DamEnd(i,1) = eNumCur
*GET,DamEnd(i,2), ETAB, 1, ELEM, eNumCur
```

```
!       Writing  element volume from table to array
*GET,DamEnd(i,3), ETAB, 4, ELEM, eNumCur
!       Writing  stress triaxiality from table to array
*GET,DamEnd(i,4), ETAB, 5, ELEM, eNumCur
!       Writing  acc. plastic strain from table to array
*GET,DamEnd(i,5), ETAB, 6, ELEM, eNumCur
!       Writing  acc. plastic work from table to array
*enddo
!       uncomment below four lines if the user
!       want to print the table to a csv file
!       *cfopen,DamEndFile,csv
!       *vwrite,DamEnd(1,1),DamEnd(1,2),DamEnd(1,3),
!       DamEnd(1,4),DamEnd(1,5)
!       (F16.7,',',F16.7,',',F16.7,',',F16.7,',',F16.7)
!       *cfclose
*do,i,1,my_ecount
*if, DamEnd(i,3),GE,1,then
!       Calculating Multiaxiality factor (MF) from Triaxiality
DamEnd(i,3)=DamEnd(i,3)
!       Updating COL 3 from Elem.Triax. to Multiaxiality factor
*else
DamEnd(i,3)=1/(2-DamEnd(i,3))
*endif
DamEnd(i,4)=DamEnd(i,4)*DamEnd(i,3)
!       Updating COL 4 from El.Pl.Strain to MF corrected El.Pl.Strain
*enddo
!       End volume weighted averaging step Procedure
!       Step1: Sort array  (descending) according to the damage
!       parameter that has to be volume weighted and averaged
SortTmpVar=0
SortIniVar=0
*do,si,1,my_ecount
SortIniVar=si+1
*do,sj,SortIniVar,my_ecount
*if,DamEnd(si,4),lt,DamEnd(sj,4), then
!       Sorting based on DamEnd(*,4)
!       DamEnd(*,4) stores MF corrected Elem.Acc.Pl.Strain
SortTmpVar=DamEnd(si,1)
DamEnd(si,1) = DamEnd(sj,1)
DamEnd(sj,1)= SortTmpVar
!-----------------------------------!
SortTmpVar=DamEnd(si,2)
DamEnd(si,2) = DamEnd(sj,2)
DamEnd(sj,2)= SortTmpVar
!-----------------------------------!
SortTmpVar=DamEnd(si,3)
DamEnd(si,3) = DamEnd(sj,3)
DamEnd(sj,3)= SortTmpVar
!-----------------------------------!
```

```
SortTmpVar=DamEnd(si,4)
DamEnd(si,4) = DamEnd(sj,4)
DamEnd(sj,4)= SortTmpVar
!-------------------------------------!
SortTmpVar=DamEnd(si,5)
DamEnd(si,5) = DamEnd(sj,5)
DamEnd(sj,5)= SortTmpVar
*endif
*enddo
*enddo
!! Step 2: Volume Weighting for each element
totvol=0
!       Variable to calculate total volume of selected elements
vol_lim_prct=50
!       Averaging over highest loaded elements that contribute to
!       "vol_lim_prct"% of total volume
vol=0
!       Variable to monitor if volume limit during volume weighting
!       has reached
VWMCS=0
!       Volume weighted Damage(here MF corrected Elem.Acc.Pl.Strain)
my_VWAMCS=0
*do,i,1,my_ecount
totvol=totvol+DamEnd(i,2)
!       Caclulating total volume of selected elements
*enddo
vol_limit=(vol_lim_prct/100)*totvol
!       Absolute value corresponding to "vol_limit"% volume
*do,i,1,my_ecount
*if,vol,ge,vol_limit, then
*exit
*endif
VWMCS=VWMCS+DamEnd(i,2)*DamEnd(i,4)
vol=vol+DamEnd(i,2)
*enddo
my_End_VWAMCS= VWMCS/vol
!       my_End_VWAMCS Stores Volume Weighted Averaged
!       Multiaxiality corrected plastic strain
my_cycle_time=TCendTime-TCstartTime
!       Duration of one TC cycle
my_damage_1 = my_end_VWAMCS
my_damage_2 = my_end_VWAMCS - my_start_VWAMCS
my_damage_3 = ((my_end_VWAMCS - my_start_VWAMCS)/2)*my_cycle_time
my_damage_4 = (my_end_VWAMCS - my_start_VWAMCS)/2
finish
```

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