Design of an Intelligent, Modular IGBT/SiC Inverter Platform up to 400 kW for Fast Realization of New Test-Bench Concepts

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Abstract

This paper presents an intelligent, modular two level, three phase inverter platform for up to 1200 V DC-link voltage and 400 kW continuous power at 10 kHz switching frequency. It features an integrated signal processing system and various sensors, which allow standalone as well as cross-linked operation. Customizable software of the signal processing system allows easy adaption to different applications such as Active-Front-End (AFE), DC/DC-converters, Dual-Active-Bridges or Drive Inverters. Focus of this paper is a design guideline for an inverter platform which fulfills requirements of various applications with regard to sensor setup, control, failure management and monitoring. Design goal of the platform is a fast setup of new testbench concepts for academic research and novel applications.

1 Introduction

In research it is necessary to have a flexible, fully customizable, and modular inverter platform to cover a broad range of different applications. Since the application may lead to uncertain operating states all parts of the system need to be intrinsically safe and easy to repair, to offer reliable operation. For evaluation of new control algorithms, characterization of electrical machines, inverters, topologies or power grids, precise and adaptable measurement of currents, voltages and temperatures are important. To provide easy and fast replication, the inverter platform needs to be built of as many standardized parts as possible while keeping the custom parts at a low number. Since commercial products are usually limited in customization and not available for the desired applications in this power and voltage range, a new platform needs to be designed [1, 2].

The basic unit of the introduced inverter platform, also known as power electronics building block (PEBB) consist of a six-pulse bridge with its own DC-link capacitors. To fulfill all requirements of the different applications, programmable intelligence and logic is provided directly inside the PEBB by a built-in signal processing. It allows a large degree of customization while also keeping the functions at hardware level, which increases the overall safety while keeping the computing time at a minimum. By changing the FPGA design each module can be adapted to the desired application. All system voltages, currents and temperatures are measured and evaluated by the internal signal processing system to allow a fast response in case of failure. Filtering and preprocessing of the measured data for superimposed signal processing systems are available as well. Furthermore, the powerful FPGA allows a direct implementation of control algorithms inside the PEBB.

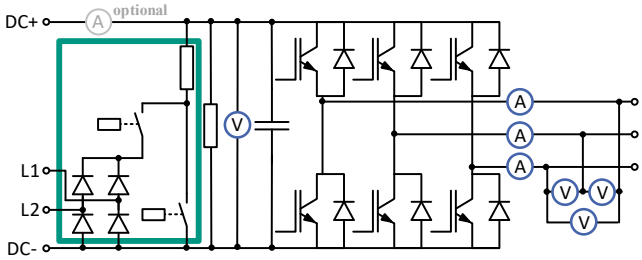

Fig. 1: Schematic of the PEBB including current and voltage sensor setup (blue) and the active pre- and discharging circuit (green).

2 Design of the PEBB

To cover a large variety of different applications the PEBB fits *Infineon XHP, Mitsubishi LV100, Semikron SEMITRANS 20, Fuji M288* and *ABB LinPak* packages. Due to the multiple sources many different IGBT and SiC MOSFET modules up to 1800 A are available and can be fitted to the requirements of the desired testbench. To allow the usage of modules with high current rating the

PEBB is equipped with a total DC-link capacitance of 4.4 mF which enable a maximum of 900 A_{rms} current rating.

The final design of the PEBB is shown in Fig. 2. It is designed to fit a 19" frame with 5 height units at a depth of 56.5 cm. It has a total volume of 44.2 l. The estimated power density using the *Mitsubishi CM1200DC-34X* modules (1700 V and 1200 A) is estimated to 21 kW/l.

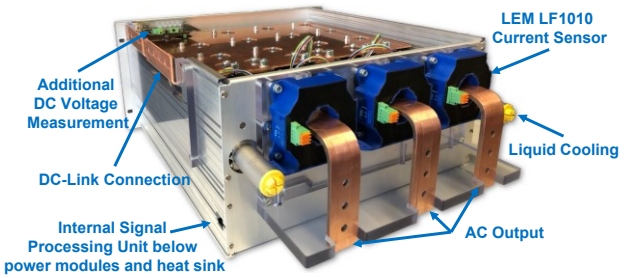

Fig. 2: Back view of the PEBB showing all AC-, DC- and cooling connections.

2.1 Thermal evaluation

The design process is basically driven by the calculations of the maximum RMS currents at the AC and DC terminals of the modules. This depends on the desired application, module characteristic and cooling. Based on those evaluations, the design of the busbars and DC-link capacitor is possible.

This paper shows the design process based on the testbench shown in Fig. 10. Therefore, all critical parts are designed for buck converter, AFE and machine inverter application.

The PEBB was optimized for the usage of the *Mitsubishi CM1200DC-34X* and *ABB 5SFG 1800X170100* with its specs shown in Tab. 1. The heatsink is designed to support up to 4 kW loss per module at a flow rate of 23.5 l/min and inlet temperature of 30°C. Based on an estimation of switching and conduction losses, the maximum junction temperature can be calculated for each module.

$$T_{\mathrm{j,max}} = T_{\mathrm{s}} + \max\left(P_{\mathrm{D}} R_{\mathrm{th(j-s)D}}, P_{\mathrm{IGBT}} R_{\mathrm{th(j-s)IGBT}}\right) \quad (1)$$

Tab. 1: Module Ratings of Mitsubishi *CM1200DC-34X* and ABB *5SFG 1800X170100*

	CM1200DC-34X	5SFG1800X170100
$Type$	IGBT	SiC MOSFET
V_{CES}	1700 V	1700 V
I_C	1200 A	1800 A
P_{tot}	7200 W	6100 W
$T_{j,op}$	150 °C	175 °C

The average conduction losses of the IGBT are estimated using a linear approximation of the forward voltage, with $v_{0,\mathrm{CE}}$ being the collector-emitter saturation voltage at 0 A, r_{D} the differential resistance, $\bar{\imath}_{\mathrm{CE}}$ the average collector and $i_{\mathrm{CE,rms}}$ the collector rms current.

$$P_{\mathrm{C,IGBT}} = v_{0,\mathrm{CE}} \cdot \bar{\imath}_{\mathrm{CE}} + r_{\mathrm{D}} \cdot i_{\mathrm{CE,rms}} \quad (2)$$

The average switching losses are calculated using a linear approximation.

$$P_{\mathrm{SW,IGBT}} = (E_{\mathrm{on,n}} + E_{\mathrm{off,n}} + E_{\mathrm{rec,n}}) \cdot v_{\mathrm{DC}} \cdot \bar{\imath}_{\mathrm{CE}} \cdot f_{pwm} \quad (3)$$

$E_{\mathrm{on,n}}, E_{\mathrm{off,n}}, E_{\mathrm{rec,n}}$ are the normalized switching losses from the datasheet.

$$E_{xx,n} = \frac{\mathrm{E_{xx}}}{v_0 \cdot i_o} \quad (4)$$

2.1.1 AFE and machine inverter application

In AFE or machine inverter application, the AC current is calculated to:

$$\bar{\imath}_{\mathrm{CE}} = \frac{1}{2\pi} \int_0^{\pi} \hat{\imath}_{AC} \cdot \sin(\varphi)\, d\varphi = \hat{\imath}_{AC}/\pi \quad (5)$$

The maximum output power of the inverter is calculated for a DC-link voltage of up to 1200 V and a switching frequency of up to 10 kHz. The maximum junction temperature is limited to 90% of $T_{\mathrm{j,op}}$ and the maximum current to 90% of the maximum current I_{C} according to the datasheet.

Figure 3 shows the maximum output power for the PEBB equipped with three *Mitsubishi CM1200DC-34X* modules. The peak power is 939 kW at 1200 V DC-link voltage and 4 kHz switching frequency.

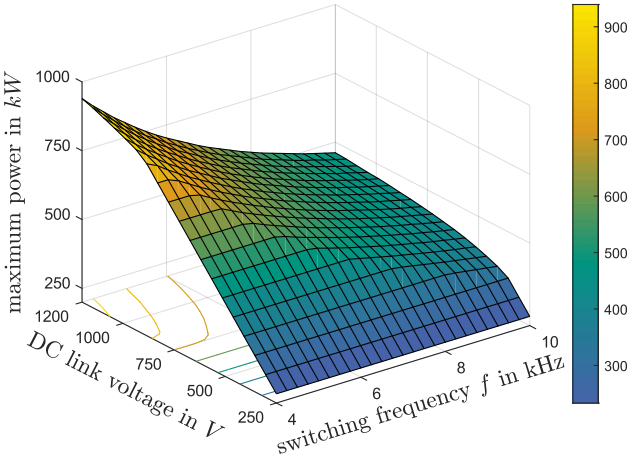

Fig. 3: Maximum power of the PEBB at AFE/machine inverter operation equipped with three Mitsubishi CM1200DC-34X modules.

The total capacitor current can be calculated by [3]:

$$I_{\mathrm{C,RMS}} = \hat{\imath}_{AC}\sqrt{\frac{m\sqrt{3}}{4\pi} + \left(\frac{m\sqrt{3}}{\pi} - \frac{9\cdot m^2}{16}\right)\cdot \cos^2(\phi_{load})} \quad (6)$$

With m defined as:

$$m = \frac{v_{\mathrm{x,1}}}{\frac{1}{2}v_{\mathrm{DC}}} \quad (7)$$

With $v_{\mathrm{x,1}}$ being the fundamental amplitude of the phase voltage. Figure 4 shows the maximum total DC-link capacitor current for the PEBB equipped with three *Mitsubishi CM1200DC-34X* modules.

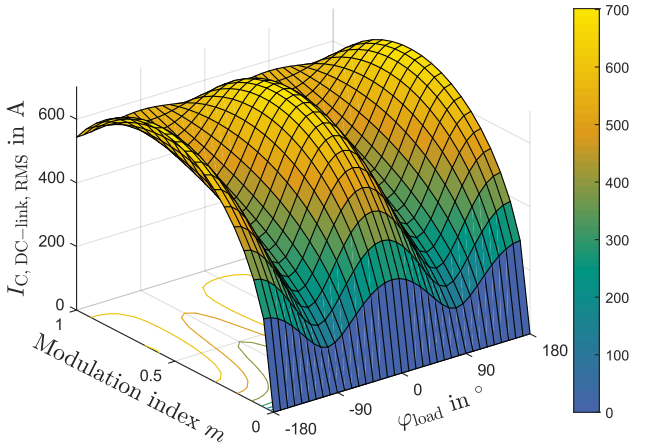

Fig. 4: Maximum capacitor RMS current of the PEBB at AFE/machine inverter operation equipped with three Mitsubishi CM1200DC-34X modules.

2.1.2 Buck converter operation

For buck converter operation, the loss estimations can be calculated equivalent. To limit the maximum busbar temperatures the average current is limited to the maximum phase RMS current calculated in chapter 2.1.1.

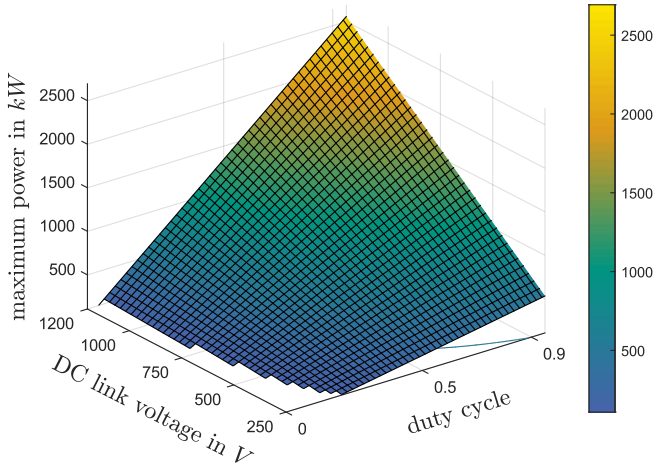

Fig. 5: Maximum power of the PEBB at buck converter operation equipped with three *Mitsubishi CM1200DC-34X* modules.

For all calculations, 8 kHz switching frequency and an inductance of 0.5 mH is assumed. Figure 5 shows the maximum output power. The lowest DC voltage is limited to 48 V to cover the full voltage range from 48 V up to 1200 V for recent traction drive applications.

As expected, the maximum power increases with duty cycle and DC-link voltage. Compared to AFE / machine inverter application, the average switching losses in the low side IGBT / MOSFET decrease due to zero voltage switching.

To reduce the RMS current at the DC-link capacitor and output voltage ripple, the buck converter operates in interleaved mode. The DC-link RMS current can be calculated by [4]:

$$I_{C,RMS} = 3\bar{\imath}_{\mathrm{AC}}\sqrt{\left(D - \frac{\lfloor 3\cdot D\rfloor}{3}\right)\left(\frac{1+\lfloor 3\cdot D\rfloor}{3} - D\right)} \quad (8)$$

D is the duty cycle of each half bridge and $\bar{\imath}_{\mathrm{AC}}$ the average current at each AC busbar.

Figure 6 shows the maximum DC-link current at buck converter operation based on the maximum output current at each setpoint with respect to the loss estimations of Fig. 5.

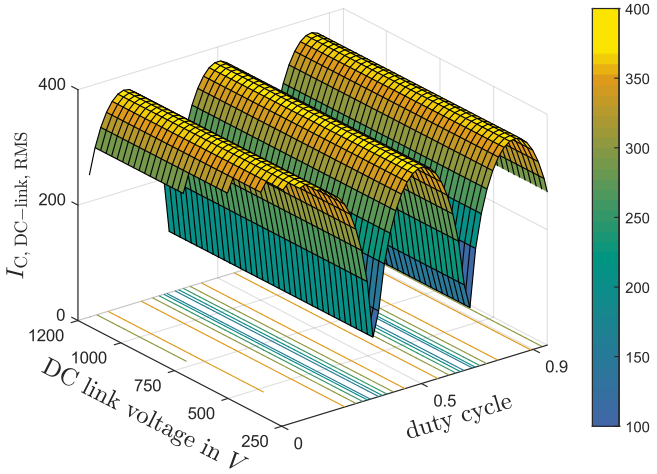

Fig. 6: Maximum capacitor RMS current of the PEBB at buck converter operation equipped with three Mitsubishi CM1200DC-34X modules.

2.1.3 Design of the busbar and DC-link capacitors

The AC and DC busbars are designed to be as large as possible. Therefore, the terminals are placed on different sides of the PEBB as shown in Fig. 2. The AC busbar has a cross section area of 228 mm² and can be increased by doubling the thickness of the AC busbar to 456 mm² for usage of the *ABB 5SFG1800X170100.* The DC busbar is designed to 420 mm² each.

Tab. 2: RMS Currents of each DC-link capacitor and currents, current densities and temperatures (according to DIN 43671) of the DC and coated AC busbar at 35 °C ambient temperature.

	CM1200DC-34X	5SFG1800X170100
$i_{DC-cap,rms}$	41.3 A	62 A
$i_{AC,rms}$	763.7 A	1.14 kA
$j_{AC,max}$	3.3 A/mm²	2.51 A/mm²
$T_{AC,max}$	<75 °C	<75 °C
$i_{DC,rms}$	808.5 A	1.21 kA
$j_{DC,max}$	1.9 A/mm²	2.9 A/mm²
$T_{DC,max}$	<60 °C	<85 °C

Table 2 shows the maximum ratings of the DC-link capacitor and the busbars based on the estimations of the previous chapters. The busbar temperatures are estimated according to DIN 43671. It can be seen that all temperatures are below 85 °C, which is the maximum operating temperature of the *LEM LF1010* current sensor. The isolation is made of Formex® and Polycarbonat which can be operated at up to 115 °C. It should be stated that higher frequencies of the AC current will partially increase current density on the AC busbar due to skin effect. This will increase the busbar temperatures and can therefore lead to power derating.

The DC-link capacitance consists of 12 *Electronicon E50.N15-374NT0* 1200 V 370 µF capacitors, which support 75 A RMS current each at 55 °C ambient temperature. As shown in Table 2 the temperatures of the busbars may exceed the maximum operating temperature, therefore the DC-link capacitors are featured with active cooling. This also increases power density due to smaller packaging. Fig. 7 shows the airflow of the capacitor cooling. Since air temperatures inside the cabinet are usually higher, the air is sucked directly through ventilation slots at the front of the PEBB.

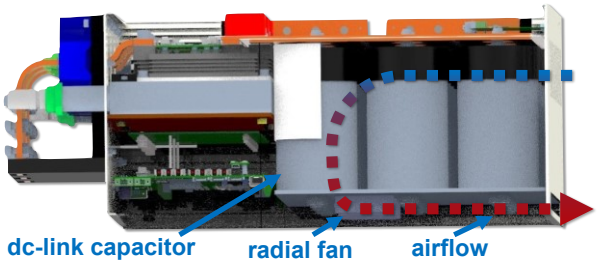

Fig. 7: Airflow of DC-link capacitor cooling.

2.2 Internal signal processing

Tab. 3: Features *Xilinx XC7A50T-2CSG325I* FPGA

Flash Memory	16 Mbyte
Logic cells	52,160
User I/Os	138
GTP Transceiver Speed	6.6 Gb/s

The on-board signal processing unit is shown in Fig. 8. It uses one *Xilinx XC7A50T-2CSG325I* FPGA with its features given in Tab. 3. The large FPGA allows the configuration to be individually matched to the desired application. Preprocessing of the measurement data can additionally reduce the load on a central DSP-unit, which calculates the overlaying control algorithms of the whole application. Furthermore, all critical values are evaluated constantly to allow independent shutdown of each inverter in case of overcurrent, overvoltage, overtemperature or gate driver failure. The error is then communicated using an optical interface and a safety ring circuit. Error indication on the front of the PEBB helps to fix faulty testbench setups.

As described in chapter 3, implementation of control loops such as AFE or buck converter control is possible. This helps to further reduce the system complexity and allows a fast testbench development.

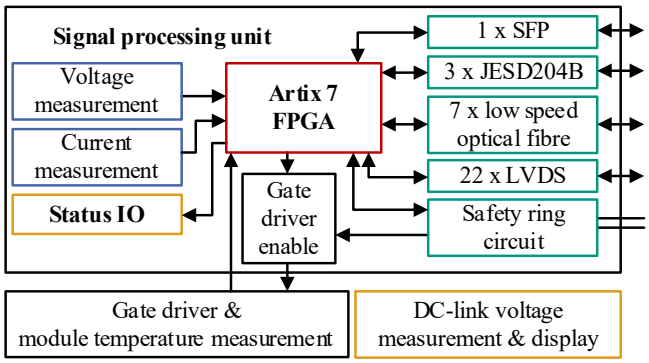

Fig. 8: Overview of the Built-in signal processing unit.

2.2.1 Measurement System

The measurement system shown in Fig. 1 is designed to offer very precise current and voltage measurements.

The AC output and optional DC input current measurement uses the *LEM LF1010* sensors with up to 2200A measurement range at 10 Ω measuring resistance, 200kHz bandwidth and 0.4% accuracy. The voltage measurement is equipped with a fast, active voltage divider circuit with 0.1 % accuracy. The analog to digital

conversion is done directly on the signal processing unit to reduce electromagnetic compatibility (EMC) issues. It uses two *LTC2325-16* ADC converters having a total of 8 channels, 16 Bit resolution and 5 MSPS sample rate for each channel.Temperature measurement of each power module is integrated inside the gate driver. If additional voltage, current or temperature measurements are required, the board can be extended using three *JESD204B* ports or 22 available LVDS lines (Fig. 8).

2.2.2 Optical high-speed communication

All communication is done using optical fibers to provide a galvanic isolation and to improve EMC behavior. The maximum bidirectional data rate for each inverter is 6.25Gb/s. The interface is realized using Small-Factor-Pluggable (SFP) modules with fiber optic interface. Due to the used FPGA highspeed GTP transceivers and protocols, low latency implementation and synchronization of several systems is possible. This also allows distributed control loop designs.

In addition to the SFP interface, 3 low speed optical fibers offer direct control of the gate driver. Furthermore, two bidirectional communication lines with reduced 50 Mbaud data rate for measurement and status data are available.

2.3 Active and passive safety

To increase safety in case of failure or emergency stop an isolated safety ring circuit connection is designed. It can be flexibly configured to directly disable the gate driver or run a predefined shutdown routine. The internal signal processing unit of each PEBB can also disconnect the ring circuit to provide an independent shut down mechanism for a whole test bench. The design of a suitable the shutdown routine is challenging and needs to be adapted to the individual application. To improve EMI robustness, the ring circuit is based on a current signal.

To ensure safe operation for the operator even in case of failure, the DC-link voltage is measured and displayed independent from the signal processing unit (Fig. 2). Furthermore, the DC-link voltage is monitored by each gate driver as backup to the high precision measurements.

A passive and active discharging of the DC-link capacitor is built in. The active discharging also features a precharging circuit for AFE use. (Fig. 1) To comply with typical automotive norms, the active discharging from 1200 V below 60 V can be done in 5s, while passive discharging takes 240s.

2.3.1 Fail safe operation mode for field weakening operation of PMSM

When operating permanent magnet synchronous machines (PMSM) at high rotational speed in the field weakening operation mode, failure or unexpected shutdown of the machine inverter results in high induced voltages, which leads to severe damage of the testbench.

To decrease the risk of overvoltage an active safety feature is implemented. It only activates if overvoltage is detected and no connection to the central signal processing is available. In this case, no field weakening current can be provided, because the current rotor position angle is not available. The PEBB will then immediately turn on its active discharging. Furthermore, the error is communicated using the ring circuit to the other PEBBs inside the testbench, which will also immediately enable active discharging.

To reduce the risk of total damage, the PEBB will then turn on all high side IGBTs/MOSFETs, to short circuit the PMSM. This leads to decreasing DC-link voltage. The short circuit current can be estimated under neglection of the stator resistance by:

$$\hat{\imath}_{\mathrm{PMSM,SC}} = \frac{\psi_{pm}}{L_{\mathrm{d}}} \tag{9}$$

If the DC-link voltage is below 1000 V, the six-pulse bridge will be turned off, which will again increase the DC-link voltage. When it reaches 1300 V, all low side IGBTs / MOSFETs are activated, allowing almost equal power distribution over each half bridge module.

When the voltage drops below 1000 V, the six-pulse bridge will be turned off again, starting a new cycle. Figure 9 shows the simulated results of a PMSM with its characteristics given in Table 4. The simulation was performed using the testbench setup shown in Figure 10.

Tab. 4: Characteristics of the PMSM for testbench fault simulation

Symbols	Parameters	Values
p	pole pair number	3
R_{s}	Stator resistance	7.5 mΩ
L_{d}	d-axis inductance	0.56 mH
L_{q}	q-axis inductance	0.94 mH
ψ_{pm}	permanent magnet flux linkage	0.39 Wb
j	Rotor inertia	0.39 kg m^2

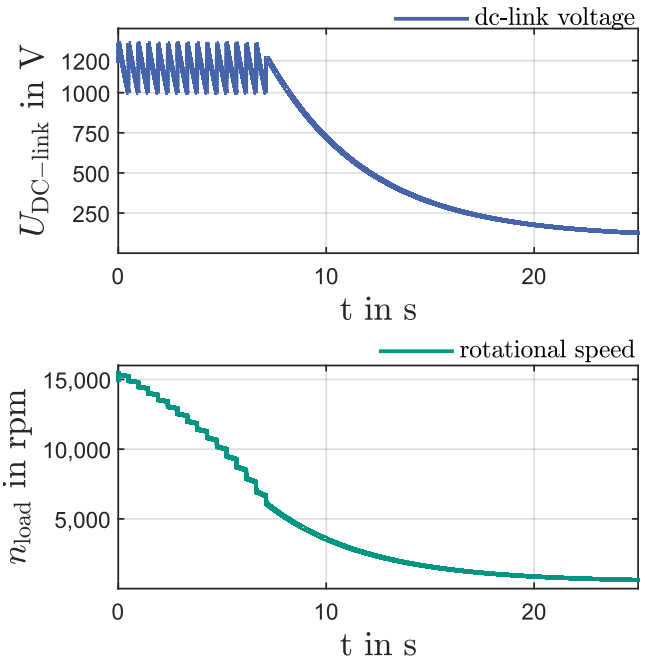

Fig. 9: Simulation of testbench fault in field weakening.

The simulation demonstrates that the DC-link voltage stays within the desired range without any knowledge of machine characteristics and rotor position angle. Therefore, short circuit due to overload of the DC-link capacitance can be avoided.

It should be noted that this active safety feature will only lead to success if the PMSM is designed to be short circuit proof and the short circuit current stays below the maximum current ratings of the module, which is usual in traction drives.

3 Typical application

Fig.10 shows an example of a typical testbench design for traction drives. It is built of four identical PEBBs (marked green in Fig.10). The inverters for both electrical machines are configured identical. The on-board processing system only provides safety features while all control algorithms are implemented on a real-time signal processing system (marked blue in Fig. 10).

The ETI-SoC System (Fig. 11) is used as central real-time processing system and features rapid prototyping using MATLAB / Simulink which allows a fast adaption of the testbench to various motors and test scenarios [5].

It consists of two *Xilinx Zynq-7030* SoCs based on the *AVNET Picozed 7030* System on Module (SoM) board with 16 slots for additional interface cards.

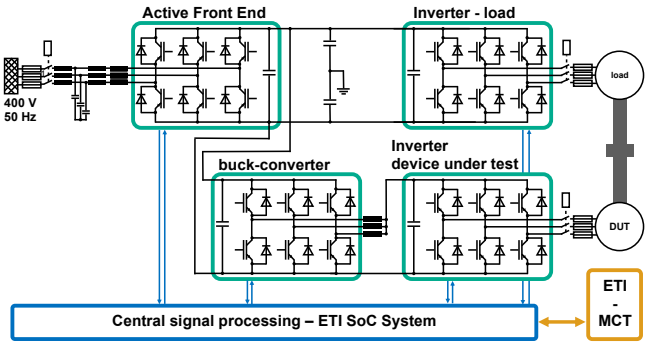

Fig. 10: Design of the testbench based on 4 identical PEBBs and external monitoring by the ETI Monitor-Control-Tool (MCT)

For this testbench setup only one SFP communication card is required to transmit data to and from each PEBB.

The *Kintex – 7* FPGAs of each SoM with 125 000 logic cells enable fast and complex control and signal processing. In addition, two *Arm Cortex A9* cores are available for rapid prototyping. Communication to the *LabVEW* based *ETI-Monitor Control Tool* (ETI-MCT) is done by two 1 Gbit/s ethernet connections.

To allow the evaluation of control algorithms at different state-of-charge, the DC-link voltage of the device-under-test (DUT) inverter can be adapted. This may also be needed if the DUT requires a DC voltage below 650V. Therefore, one or two PEBBs are configured as interleaved buck, boost, or buck-boost converter. The three-phase design reduces the current stress on the DC-link capacitor of the DUT inverter while keeping the dynamics of the control circuit high.

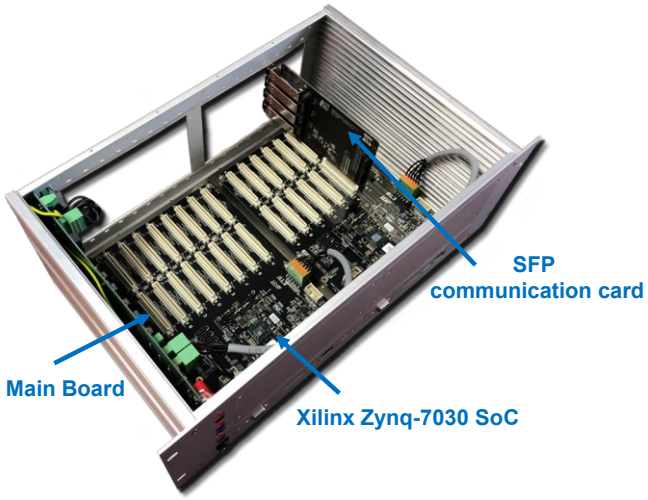

Fig. 11: ETI – SoC System including SFP communication card.

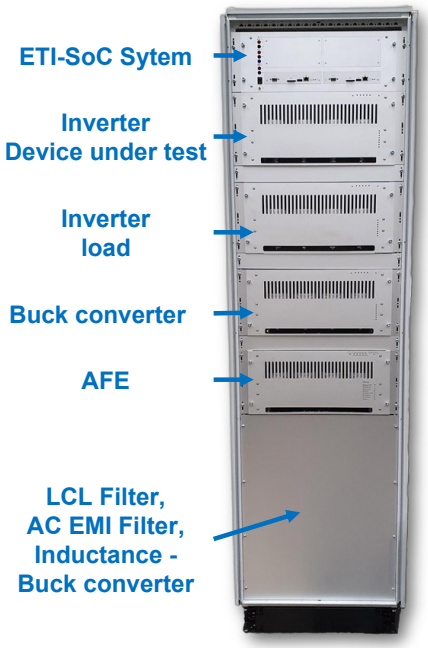

Fig. 12: Testbench setup shown in Fig. 11. Including all Filters and passive components. Dimensions (L x W x H): 1 m x 0.6 m x 2 m.

To increase the overall system performance all control and safety features of the DC/DC converter are implemented on the internal signal-processing system. The ETI-SoC-System only provides the voltage and current setpoints.

The connection to the power grid is done by only one PEBB configured as AFE. This reduces the average required grid power and decreases the size of the line filter, since the AFE only delivers power loss or peak power in event of (de-)acceleration. The AFE is controlled by its built-in signal processing unit to reduce the workload of the ETI-SoC-System. The precharging of the DC-link capacitor is done by the internal circuit which reduces the complexity of the system design.

3.1 EMC improvement on the AFE

Modern 1700V MOSFET/IGBT modules allow higher switching frequencies, which are possible due to higher switching speeds. While this reduces the switching losses, it also raises EMC issues due to higher $\mathrm{d}u/\mathrm{d}t$. Especially when operating a two level AFE at high DC-link voltage, these issues need to be addressed.

Operating the PEBB as AFE using sinusoidal pulse width modulation (SPWM) without further filtering will lead to high common-mode voltages (Fig.13a). This results in EMC issues, which may interfere with current and voltage measurements.

This issue will impair if the DC-link voltage increases, since larger DC-link voltages lead to a lower modulation index. When using SPWM, a lower modulation index increases the on-time of the freewheeling switching states 0 and 7.

While freewheeling switching states have a common mode voltage (CMV) voltage of $\pm u_{DC}/2$, the CMV of the active switching states is only $\pm u_{DC}/6$ and therefore by $2/3$ lower. Consequently, increasing the on-time of the freewheeling states leads to larger common mode voltage-time-areas and therefore potential EMC issues.

To improve EMC behavior, each PEBB features two built-in y-capacitors with up to 800 nF. In addition to the LCL line filter, a common mode choke with 2.5 mH mutual inductance and a common mode saturation current of 3 A is implemented in the testbench to reduce CMV (Fig.10).

To achieve sufficient damping of the electromagnetic interference (EMI) the common mode current through the choke needs to stay below the saturation limit. Thereby the common mode current depends on the voltage-time-areas of the applied common mode voltages.

The Simulation results in Fig. 13 a) and b) show a large improvement of EMC behavior due to the additional filtering by y-capacitors and the common mode choke at 1200 V DC-link voltage. Drawback is the large leakage current, which reaches values close to the saturation current of the common mode choke. This may lead to lower EMC at some operating points. Improvements can be achieved by applying carrier position shift (CPS) modulation [6].

At CPS, the modulation is changed from one carrier signal to three, equally shifted, carrier signals. At modulation indexes lower than 2/3, CPS will perform without usage of the freewheeling states 0 and 7. This reduces the common mode voltage-time-area by approximately 2/3 and is therefore ideal for AFE use at high DC-link voltages.

Fig. 13 c) shows the improvements on common mode voltage, while Fig. 13 d) compares the leakage currents of all methods. As expected, CPS with CM filter outperforms SPWM and is consequently implemented in the built-in AFE control of the PEBB.

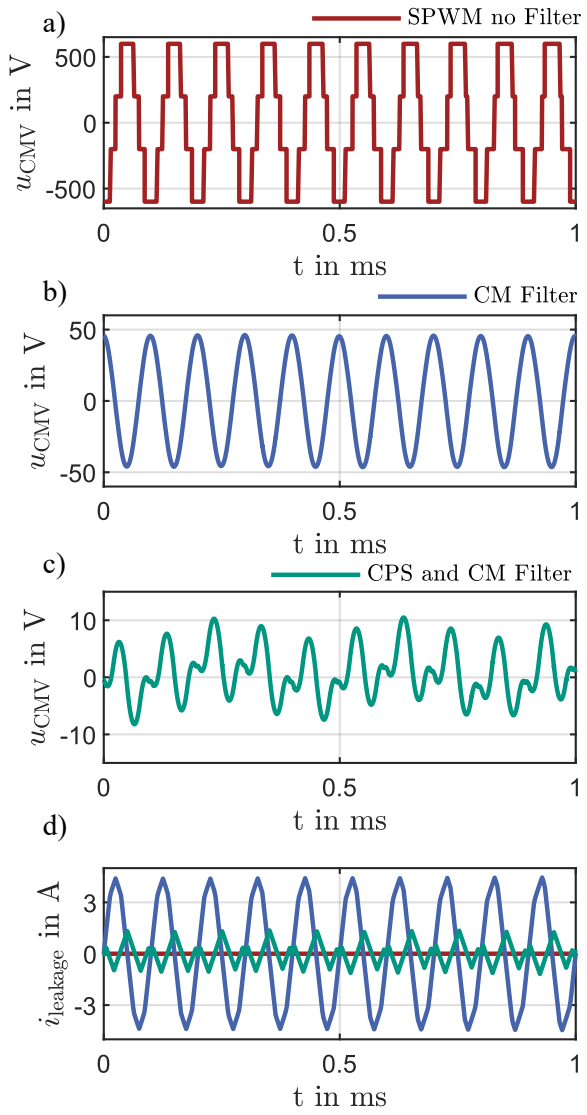

Fig. 13: Common mode voltages of SPWM without filtering a), SPWM with EMI Filtering b), CPS with EMI Filtering c) and leakage currents d)

It should be noted, that CPS will lead to slightly higher total harmonic distortion of the line current, which may result in the need of higher attenuation of the LCL line filter [7].

4 Summary

This paper describes the design process of an intelligent, modular IGBT/SiC inverter platform. The hardware design of the system was performed based on the specs of the IGBT module *Mitsubishi CM1200DC-34X* and the SiC MOSFET module *ABB 5SFG 1800X170100*.

Challenges of high current and DC-link voltage have been evaluated with focus on safety of the operator or researcher. Furthermore, a typical testbench design was described and built-in hardware. Potential EMC issues due to higher DC-link voltage and switching speed were examined and addressed by filtering and modification of the modulation technique.

5 References

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