A 60 kW Power Hardware-in-the-Loop Test Bench for grid emulation based on a Series Hybrid Cascaded H-Bridge Converter

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Keywords

Abstract

In this paper the requirements for a Power Hardware-In-the-Loop (PHIL) system for the emulation of grids and grid faults are discussed. Solutions for all parts of the PHIL system – the power electronics, the signal processing system and the software structure – are presented. Subsequently, an analysis of the accuracy, bandwidth and stability of the PHIL testbench is done and the effects of different interface algorithms are shown. Concluding, measurement results of emulated highly dynamic grid faults such as voltage dips and spikes, distorted grids and weak grid situations are shown, which prove the performance of the PHIL system.

I.   Introduction

Due to the energy transition, the penetration of power electronic systems in energy grids - driven by the decentralization of energy generation and the rise of converter-fed loads - is increasing more and more [1, 2]. This results in a change of the grid structure, which has led to more phenomena and incidents in various scenarios in recent years – ranging from harmonics in offshore wind applications [3], interactions between the controllers of converters with each other or with filter elements [4], resonances triggered by the switching events of converters [5] to instabilities and oscillations between the converters in large photovoltaic plants [6].

To overcome these challenges, it is crucial to know the behavior of the grid connected converters, especially in fault grid conditions such as Low Voltage Ride Through (LVRT) events, weak grid situations or high penetration of harmonics. To generate comparable test conditions for the different Converters Under Test (CUT), a Power Hardware-In-the-Loop (PHIL) system is mandatory. Typically, these fault conditions are emulated without considering the impact of the converter on the point of common coupling (PCC). For a closed-loop emulation of these fault conditions, a low-latency and high-bandwidth PHIL system is required. Therefore, all three parts of the PHIL system are essential: the power electronics, the signal processing system and the software structure. The requirements for these PHIL system parts are discussed in Section II. Subsequently, chapter III outlines the implementation of the applied PHIL system parts. With the knowledge of the PHIL system characteristics, an analysis of the stability, dynamic and accuracy of the grid emulation for different interface algorithms (IA) is performed and described in chapter IV. Finally, the behavior of a 2-level 30 kVA grid connected CUT is analyzed with the presented PHIL system and the corresponding measurement results for a LVRT-event, a weak grid situation and a harmonic distorted grid are shown in chapter V, which demonstrate the performance of the PHIL system.

II.   Requirements for the PHIL system

As mentioned above, all three parts of the PHIL system are important for the emulation of grids or grid fault conditions and for each part individual requirements have to be considered. The requirements placed on the power electronics of a PHIL system which is used for grid emulation are contradictory, especially for the emulation of grid faults. On the one hand, the power electronics must be able to generate a sinusoidal output voltage with a low total harmonic distortion (THD) and a variable amplitude and frequency. On the other hand, the power electronics must be able to provide a highly dynamic output voltage with a small reaction time. This results for example in opposed design criteria for the output filter of the PHIL system. To overcome these contrary requirements, a new topology – the Series Hybrid Cascaded H-Bridge (SHCHB) converter – is used [7].

The signal processing system has to take care of the control of the power electronics, the measurement acquisition and the real-time simulation of the desired grid model, as can be seen in Fig. 1 a). It must be guaranteed that the signal processing system is able to calculate the real-time model of the grid impedance within one digital feedback time $t_{L,D}$. The digital feedback time $t_{L,D}$ is the latency from excitation by the CUT to the response of the PHIL system and it is crucial for the stability of the PHIL testbench [8]. The higher the needed bandwidth/dynamic of the emulated model, the smaller the digital feedback time $t_{L,D}$ must be [9]. Thus, a highly performant signal processing system is necessary to reduce the computation time for the real time model and to enable the emulation of highly dynamic grid faults. Therefore, a proprietary System-on-Chip (SoC) based signal processing system is developed [10], as can be seen in Fig. 4 b).

Besides the hardware part of the PHIL system, the software structure is also crucial to achieve a stable and highly dynamic emulation. Hence, a hybrid control concept is used, where the control of the SHCHB-converter and the computation of the real-time model is distributed between two FPGAs and four ARM-cores, as shown in Fig. 4 a). As a result, the computation can be strongly parallelized which reduces the required computation time and thus enables higher dynamics to be achieved. Additionally, the choice of the interface algorithm (IA) also called Power Interface (PI) is important for the stability and the accuracy of the PHIL system [11]. The IA links the virtual real-time model with the physical part of the PHIL system. In the simplest and most common IA – the Ideal Transformer Method (ITM) – [8], the IA consists only of the PHIL converter as the forward path and the measurement system as the feedback path. In Fig. 1 b), the block diagram of the PHIL testbench with the ITM as the IA is depicted. The transfer functions T_V and T_{Si} describe the PHIL converter and the measurement system behavior, respectively.

Other widely used IAs are the Partial Circuit Duplication (PCD), the Damping Impedance Method (DIM), the time-variant First-Order Approximation (TFA), Transmission Line Model (TLM) and the Feedback Current Filtering (FCF) [8, 11–19]. The different characteristics of the IAs and their influence on the PHIL testbench are discussed in chapter IV.
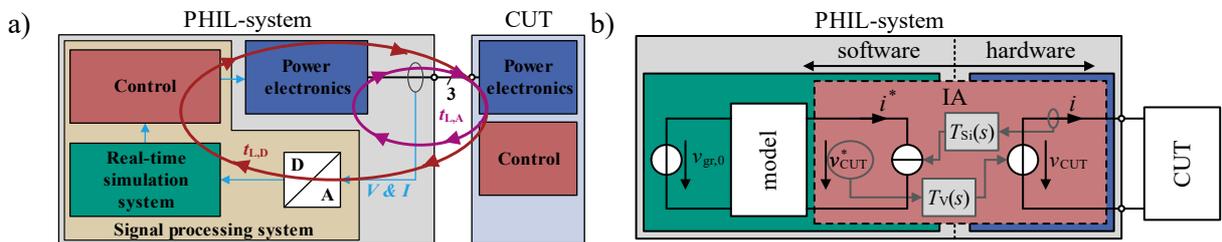

Fig. 1: a) Generalized test setup for grid emulation with a CUT; b) Block diagram of the PHIL testbench with the ITM interface algorithm

III.   The characteristics of the PHIL system components

A   The power electronics part – The SHCHB-converter

The power electronics part of the PHIL system consists of the Series Hybrid Cascaded H-Bridge (SHCHB) converter and three parallel Active Front Ends (AFE) with 25 kVA which supply the SHCHB converter. In Fig. 2 and Fig. 3 a) the SHCHB converter topology and the constructed hardware is shown,

respectively. The SHCHB converter consists of 12 cascaded H-Bridge (CHB) cells, one dv/dt filter and one Linear Power Amplifier (LPA) per phase [7].
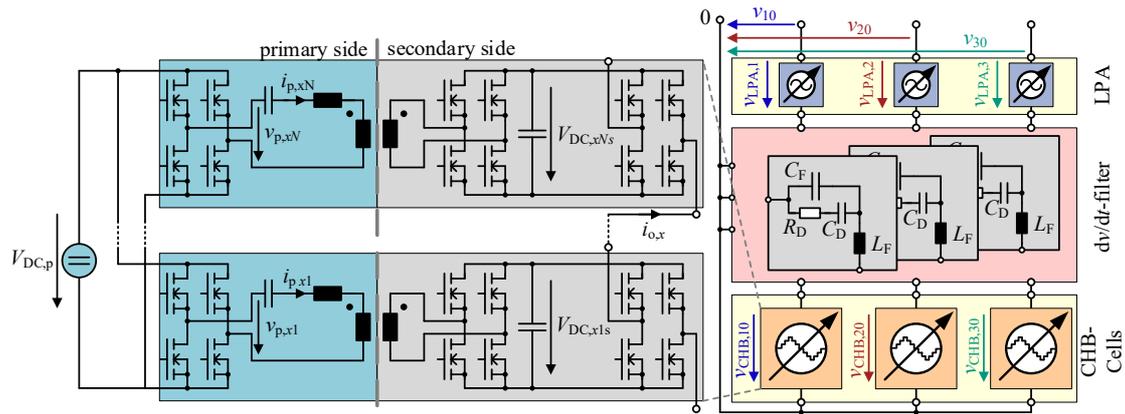

Fig. 2 Series Hybrid Cascaded H-Bridge converter topology

Each CHB cell has an output voltage of +/- 30 V or 0 V. The maximum output current is rated up to 70 A. In Fig. 3 b), the developed board of the CHB cell is shown. The CHB cells and the LPA are connected via a dv/dt filter. Since the dv/dt filter only has to reduce the slope of the square wave output voltage of the CHB cells so that the LPA can compensate this slope, a very high bandwidth of 360 kHz for the dv/dt filter can be selected. The distortions below this bandwidth are compensated by the LPA. In this way, both design goals are met, an output voltage with a low THD of only 0.01 %, as shown in Fig. 13 and a highly dynamic output voltage, as shown in Fig. 7. The developed LPA can provide an output voltage between +/- 30 V and thus can compensate the toggle of one CHB cell. The maximum RMS current is 70 A in all four quadrants [20]. The constructed LPA is shown in Fig. 3 c). Due to this interconnection of the CHB cells, the dv/dt-filter and the LPA, an arbitrary output voltage with a low THD, a high dynamic and a maximum amplitude of 675 V for a three phase AC system or 780 V for an DC system can be provided. The maximum output power of the system is limited to 60 kVA with a maximum RMS output current of 70 A. A precise description of the SHCHB converter, the CHB cells and the LPA is given in [7], [21] and [20], respectively.
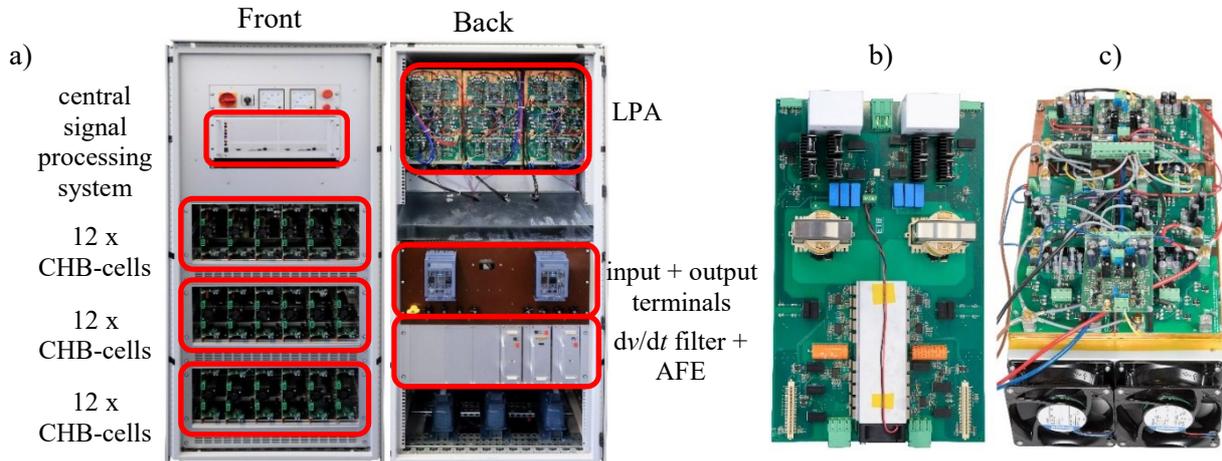

Fig. 3: Constructed Hardware: a) PHIL system front and back view; b) CHB-cell; c) Linear Power Amplifier

B   The signal processing system

The signal processing system consists of two ETI-SoC-Systems as shown in Fig. 4 a) and b). The ETI-SoC-System 1 takes care of the peripherals like the temperature management of the cabinet and the LPAs, the power supply of the LPAs, the main switches etc. Besides that, the voltage control of the primary DC-link voltage $V_{DC,p}$ is implemented on the FPGA of the ETI-SoC-System 1. The subordinated current control of the active front ends (AFE) is managed by the Local Control Unit (LCU) directly on the AFEs. On the ARM-Core 1 of both systems, the communication to the human machine interface (HMI) is implemented via an Ethernet interface. On the Arm-Core 0, the monitoring of all system

variables as well as the global state machines of the PHIL system are realized. Additionally, the calculation of the PCC voltage V_{PCC} is executed on the ARM-Core 0 of the ETI-SoC-system 2.
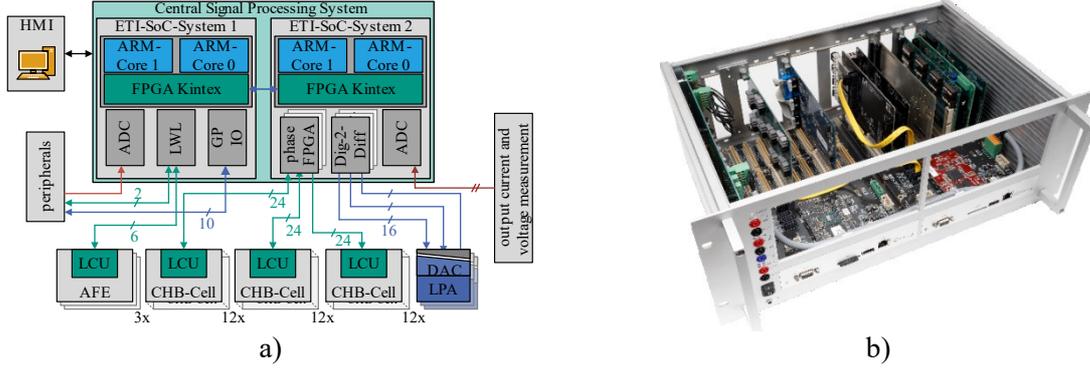

Fig. 4: a) Signal processing structure of the SHCHB-converter; b) constructed central signal processing system with two ETI-SoC-systems

The ADC-extension boards of the ETI-SoC-system shown in Fig. 4 have a sample frequency f_{ADC} of 5 MSPS and are used for the current and voltage measurement of the output of the PHIL system. For each output phase, a separate phase FPGA is used for the communication with all CHB cells of the corresponding phase. Additionally, the sorting algorithm described in [7] as well as the preprocessing and merging of the information of all CHB cells is implemented on these phase FPGAs. The setpoints for the LPAs are generated using a 5 MSPS, galvanically isolated digital-to-analog converter (DAC) that communicates with the ETI SoC system via a 16-bit differential parallel bus.

C   The software structure

The general software structure of the PHIL system is illustrated in Fig. 5. The HMI is used to transmit setpoints, control words and emulation parameters to the ETI-SoC-system. Additionally, status words and the measurements or rather the analysis results, for instance the frequency dependent behavior of the CUT, is received via the HMI. As mentioned above, the control of the SHCHB converter is divided between the two ETI-SoC-systems such that the ETI-SoC-System 2 only has to handle the calculation and the control of the output voltage of the PHIL system v_{x0} $(x \in (a, b, c))$. Hence, the calculation of the desired grid model and the resulting setpoints for the LPA and the CHB cells are the main tasks of the ETI-SoC system 2.
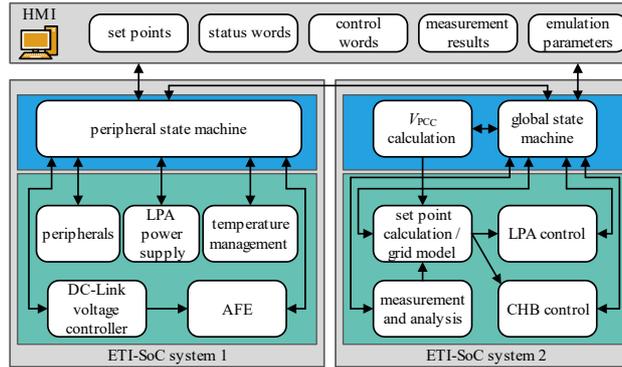

Fig. 5: General software structure of the PHIL system

The setpoint generation is done in a hybrid manner, one part on the ARM core and the other part on the FGPA core of the ETI-SoC-system, as can be seen in Fig. 6. On the ARM core, the voltage of the considered PCC V_{PCC} is calculated by means of a phasor-based grid model. In the simplest case, this voltage can be assumed as an ideal voltage source. The grid impedance between the PCC and the CUT is emulated on the FPGA. Therefore, the given RMS values of the ARM core are converted into ideal and independent instantaneous values for the PCC voltage. Here, three components can be distinguished: the fundamental, the harmonics and the DC part. The fundamental and the harmonics are described with symmetrical components, which are given by the ARM-core. Additionally, the phase between the fundamental and the harmonics can be specified. This allows the PHIL system to emulate unbalanced

grid conditions and grid faults, e.g. line-to-line faults. Besides the AC-system, the PHIL system is also able to provide a DC voltage, which can be artificially distorted by adjustable harmonics.

Parallel to the calculation of the instantaneous values for the PCC voltages (v_{fund}, v_{harm} and v_{DC}), the voltage drop over the emulated grid impedance $\Delta v_{Z\text{grid}}$ is determined. Therefore, the output current i_{out} is required, as shown in Fig. 6. This results in a closed-loop emulation and thus the computation time must be as small as possible to ensure a stable emulation. Hence, the computation is performed on the FPGA with the ADC sample rate of 5 MHz. According to Fig. 6, the overall digital feedback time $t_{\text{L,D}}$ of the PHIL system from the current sensor over the ADC and FGPA to the output terminals of the PHIL system is only 1,1 µs for the LPA and 1,3 µs for the CHB cells.

Subsequent to the calculation of the voltage drop and the instantaneous PCC voltages, the setpoints for the LPAs $v_{\text{out,LPA}}$ and the CHB cells $v_{\text{out,CHB}}$ are determined. Thereby, the internal voltage drop of the CHB cells due to the output current i_{out} is considered. The harmonics of the PCC voltage can be alternatively added to both setpoints or only to the LPA setpoint $v_{\text{out,LPA}}$, so that no high-frequency switching occurs in the CHB cells.
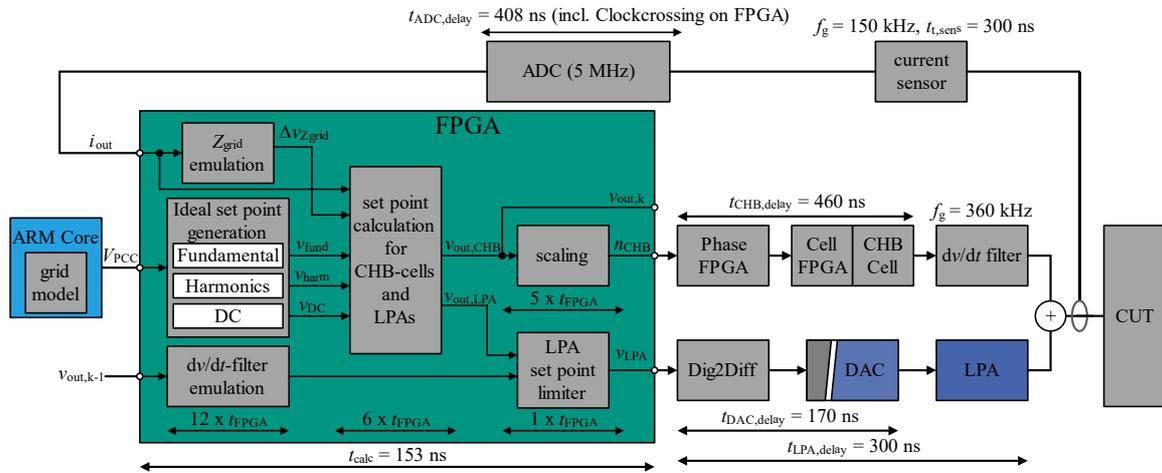

Fig. 6: Setpoint generation for CHB cells and LPAs

The calculated setpoint for the CHB cells must be scaled according to their DC link voltage to get the number of CHB cells that must be turned on to obtain the desired output voltage. Since the LPA automatically determines the difference between the desired total output voltage and the voltage provided by the CHB cells [7], the setpoint for the LPA is the total output voltage v_{x0}. Therefore, it is crucial to know the accurate latencies of the two paths - the CHB path and the LPA path - from the central SoC-system to the response of the CHB cells output and the LPA output, respectively. If the latencies are not correctly considered, the LPA, for example, will receive and act on the new setpoint in the event of a voltage step, while the output of the CHB cells has not reacted yet. This would lead to the saturation of the LPA, since it cannot supply such a high voltage. That behavior can be seen in Fig. 7 a), where the latencies are not correctly taken into account during a 300 V voltage step. As can be seen, an overshoot of the overall output voltage of the PHIL system occur due to the saturation of the LPA .
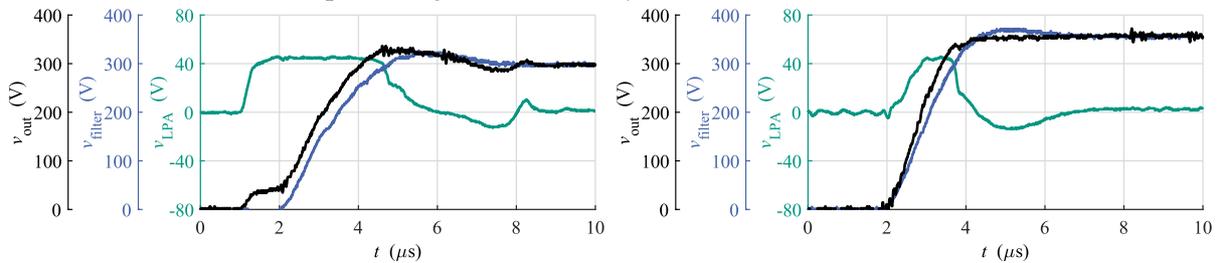

Fig. 7: Step response without consideration of the latency and the dv/dt filter (left) and with consideration (right)

In addition to the latencies, the dv/dt filter has also to be considered for the setpoint generation of the LPA, since it reduces the slope of the CHB cell output voltage during a voltage step. Therefore, parallel to the grid impedance emulation and the calculation of the PCC voltages, the behavior of the dv/dt filter is also emulated on the FPGA. Since the dv/dt filter is a second order filter, a biquad IIR-filter in

transposed direct-form 2 is applied for a higher numerical robustness [22]. The calculated output voltage of the dv/dt-filter is used to limit the setpoint of the LPA within a band of +/- 30 V around this calculated voltage. Considering the different latencies and the behavior of the dv/dt-filter, the saturation of the LPA can be successfully prevented, as can be seen in Fig. 7 b). By means of this setpoint generation, a highly dynamic and stable step response is guaranteed with a settling time of only 2 µs for a 300 V voltage step.

IV. Analysis of the grid impedance emulation

For the analysis of the stability, dynamic and accuracy of the grid impedance emulation, the open-loop and the closed loop transfer function of the PHIL testbench, consisting of the PHIL system and the CUT, must be considered. The choice of the IA significantly influences the transfer function of the PHIL testbench. In the following, four algorithms are analyzed in more detail: the ITM, the DIM, the FCF and a new developed damped ITM algorithm, subsequently named DITM.

The PCD, TFA and TLM are not further considered. The PCD and the TLM need a link impedance between the PHIL system and the CUT which is used for the IA [8, 18, 23] and shown in Fig. 8 b) as Z_{D1}. Since in the given application the characteristics of the grid from the PCC to the CUT is emulated in the model, no additional link impedance is given and thus these two IAs are not usable. For the TFA, the CUT is modeled with a time variant, first-order linear system whose parameters are adapted during the operation. The TFA has problems with numerical instabilities in quasi-stationary states [11], high sensitive to measurement noise [18], limited in use for non-linear or time-variable CUTs [15, 18] and inaccuracy at high frequencies and therefrom unstable behavior [15]. Thus, the TFA is also not further considered.

The block diagram of the PHIL testbench with the ITM is shown in Fig. 1 b), with the FCF and the DIM in Fig. 8 a) and b), respectively.
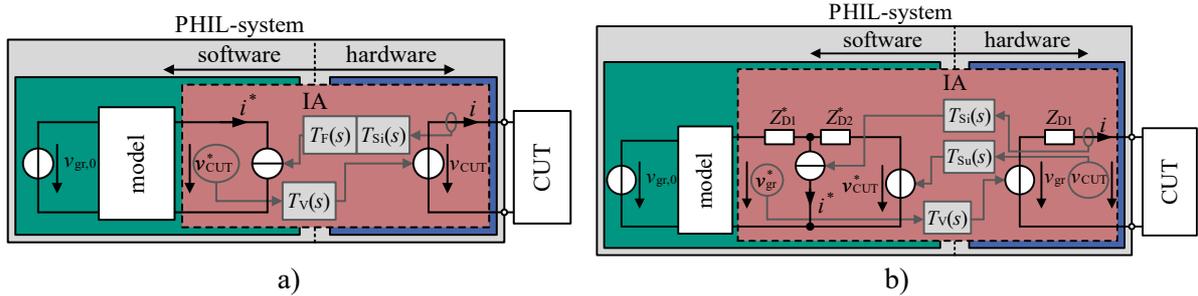

Fig. 8: Block diagram of the PHIL testbench with different interface algorithms: a) the FCF and b) the DIM

T_{Si}, T_{Su}, T_F and T_V are the transfer functions of the current and voltage measurement, the feedback filter and the SHCHB converter, respectively. The damping impedance Z_{D1} between the PHIL system and the CUT is implemented in hardware as well as in software, Z_{D2}^* is only implemented in software. For the DIM, the impedance Z_{D1} can be set to zero [8] and thus no additional damping impedance in hardware is necessary. Assuming that the CUT can be considered as the impedance Z_{CUT} and the grid model as the grid impedance Z_{gr}, the signal-flow graph of the PHIL testbench for the FCF and the DIM can be determined, shown in Fig. 9 a) and b).
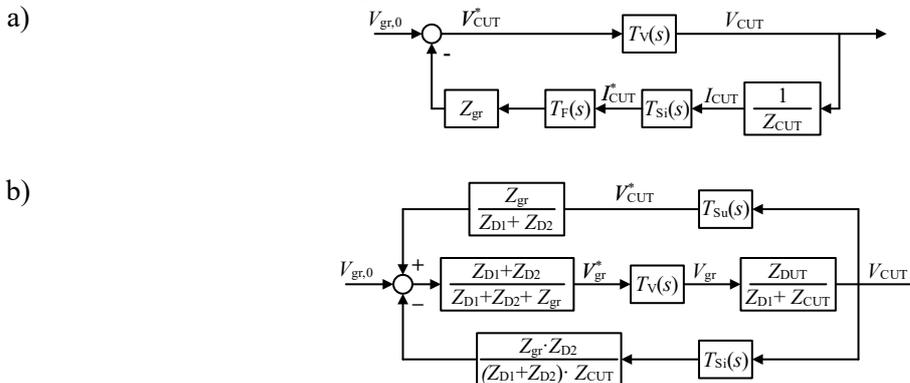

Fig. 9: Signal-flow graph of the PHIL testbench with a) the FCF and b) the DIM interface algorithm

The ITM and the DITM have the same signal-flow graph as the FCF with the additional condition that the filter transfer functions $T_F = 1$. The corresponding open loop transfer functions $G_{o,ITM}$, $G_{o,FCF}$ and $G_{o,DIM}$ as well as the closed loop transfer function $G_{c,ITM}$, $G_{c,FCF}$ and $G_{c,DIM}$ are given by:

$$G_{o,ITM} = \frac{T_V \cdot T_{Si} \cdot Z_{gr}}{Z_{CUT}} \tag{1}$$

$$G_{o,FCF} = \frac{T_V \cdot T_{Si} \cdot T_F \cdot Z_{gr}}{Z_{CUT}} \tag{2}$$

$$G_{o,DIM} = \frac{Z_{gr} \cdot T_V (T_{Si} \cdot Z_{D2} - T_{Su} \cdot Z_{CUT})}{(Z_{CUT} + Z_{D1}) \cdot (Z_{gr} + Z_{D1} + Z_{D2})} \overset{Z_{D1}=0}{=} \frac{Z_{gr} \cdot T_V (T_{Si} \cdot Z_{D2} - T_{Su} \cdot Z_{CUT})}{Z_{CUT} \cdot (Z_{gr} + Z_{D2})} \tag{3}$$

$$G_{c,ITM} = \frac{T_V \cdot Z_{CUT}}{Z_{CUT} + T_V \cdot T_{Si} \cdot Z_{gr}} \tag{4}$$

$$G_{c,FCF} = \frac{T_V \cdot Z_{CUT}}{Z_{CUT} + T_V \cdot T_{Si} \cdot T_F \cdot Z_{gr}} \tag{5}$$

$$G_{c,DIM} \overset{Z_{D1}=0}{=} \frac{T_V \cdot Z_{D2} \cdot Z_{CUT}}{Z_{CUT} \cdot (Z_{gr} + Z_{D2}) - T_V \cdot Z_{gr} \cdot (T_{Su} \cdot Z_{CUT} - T_{Si} \cdot Z_{D2})} \tag{6}$$

Since the line filter of the CUT is an inductance with 1 mH and for high frequencies the passive behavior is dominant, the behavior of the CUT is given by:

$$Z_{CUT} = L_{CUT} \cdot s \tag{7}$$

The grid impedance is assumed to be a RL-equivalent, whereby the relative grid inductance L_{rel} is given by $L_{rel} = L_{gr}/L_{CUT}$.

$$Z_{gr} = R_{gr} + s \cdot L_{gr} = R_{gr} + s \cdot L_{CUT} \cdot L_{rel} \tag{8}$$

The equations (9) to (11) define the transfer functions T_V, T_{Si} and T_{Su} with the propagation delays $T_{D,V}$, $T_{D,Si}$ and $T_{D,Su}$ of 453 ns, 708 ns and 488 ns, respectively. The corresponding bandwidths are 105 kHz, 150 kHz and 1 MHz.

$$T_V = e^{-T_{D,V} \cdot s} \cdot \frac{1}{1 + \frac{s}{2\pi f_{g,V}}} \tag{9}$$

$$T_{Si} = e^{-T_{D,Su} \cdot s} \cdot \frac{1}{1 + \frac{s}{2\pi f_{g,Si}}} \tag{10}$$

$$T_{Su} = e^{-T_{D,Si} \cdot s} \cdot \frac{1}{1 + \frac{s}{2\pi f_{g,Su}}} \tag{11}$$

The feedback filter of the FCF T_F is dimensioned so that for the highest relative inductance L_{rel} the PHIL testbench is stable. A first-order filter topology with a bandwidth of 15 kHz is used for this purpose. For the DITM, the emulated model is directly damped with a parallel damping resistor R_D. The transfer function of the damped model is:

$$Z_{gr} = \frac{R_D \cdot L_{gr} \cdot s}{R_D + L_{gr} \cdot s} + R_{gr} = \frac{L_{gr} \cdot s}{1 + \frac{L_{gr}}{R_D} \cdot s} + R_{gr} = \frac{L_{gr} \cdot s}{1 + s/2\pi f_{D,gr}} + R_{gr} \tag{12}$$

R_D is also dimensioned to achieve a stable behavior for the highest relative inductance L_{rel}. The resulting R_D is 450 Ω yielding a bandwidth $f_{D,gr}$ of 14.3 kHz for $L_{rel} = 5$, 23.9 kHz for $L_{rel} = 3$ and 71.6 kHz for $L_{rel} = 1$. The corresponding Nyquist plots for the open loop transfer function and the corresponding error ϵ of the closed loop transfer function are shown in Fig. 10 and Fig. 11. The error of the closed loop transfer function is calculated according to equation (13), where G_{ideal} is the ideal behavior given by equation (14).

$$\epsilon_{IA} = \frac{G_{IA} - G_{ideal}}{G_{ideal}} \tag{13}$$

$$G_{ideal} = \frac{Z_{CUT}}{Z_{CUT} + Z_{gr}} \tag{14}$$

According to Fig. 10, for the DITM, the FCF and the DIM a stable operation of the PHIL system up to a relative inductance L_{rel} of 5 is possible. For the ITM, the PHIL testbench will be instable for L_{rel} higher than 2.4 and thus this IA is not usable for the given application.
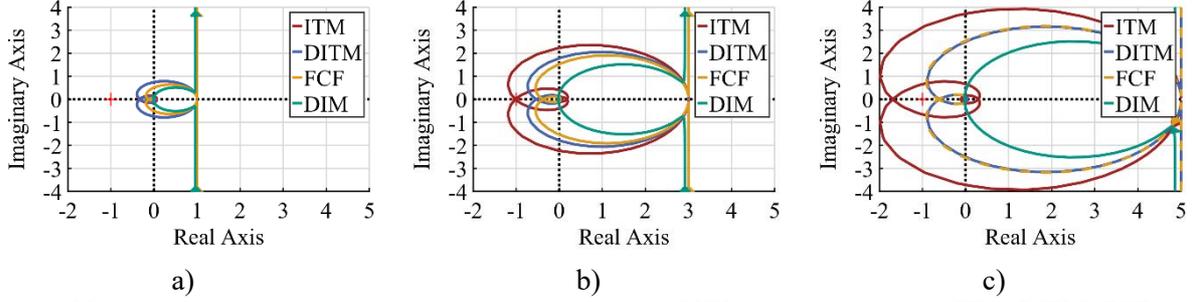
Fig. 10: Nyquist plot of the open loop transfer functions of the PHIL testbench with the ITM, DITM, FCF and DIM as the interface algorithm for a relative inductance L_{rel} of a) 1, b) 3 and c) 5
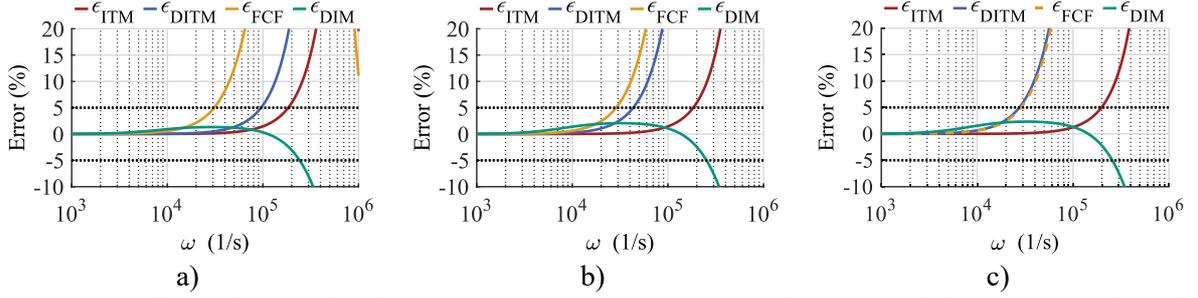

Fig. 11: Error of the grid emulation for ITM, DITM, FCF and DIM as IA for a relative inductance L_{Rel} of a) 1, b) 3 and c) 5

To compare the accuracy of the different IAs, the frequency leaving the 5 % band is considered. According to Fig. 11, the highest accuracy is reached with the DIM for all relative inductances. The DITM and the FCF has the same leaving frequency for $L_{rel} = 5$. For a lower relative inductance L_{rel}, the DITM has a higher accuracy since the bandwidth is increasing. Hence, the FCF is not further considered. In Fig. 12 the simulation results of the DITM and DIM in comparison to the simulated real grid impedance are shown for $L_{rel} = 1$.
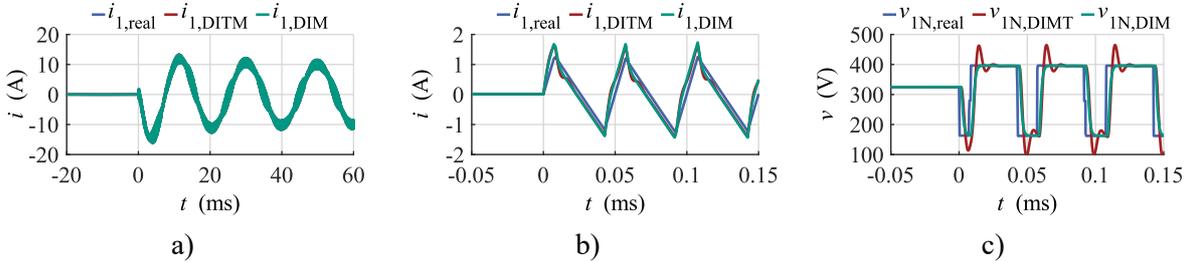

Fig. 12: Simulation results of the grid impedance emulation of phase 1 for $L_{rel} = 1$: a) line current for three mains periods; b) line current for three switching periods; c) line voltage for three switching periods

At $t = 0$ ms the CUT is activated. The simulation results confirm the prediction of Fig. 10 and Fig. 11 that the DIM has higher stability and accuracy as the DITM. Hence, the DIM should be used, if the characteristics of the CUT are known. If the characteristics of the CUT are unknown, the DITM is a possible alternative, since it is still stable and correctly emulates the mean values over a switching period.

V. Analyzed grid states

To examine the behavior of the grid connected CUT, four test scenarios are implemented. First, the basic CUT behavior is analyzed on an ideal grid. Therefore, the PHIL system must provide a sinusoidal waveform with low THD. Depending on the given region/application (e.g. trains, ships, airplanes, etc.), the amplitude and frequency of grid has to be customized. This is done with the given setpoint generator according to Fig. 6. In Fig. 13 a) and b) the measured output voltages at the terminals of the PHIL system as well as the corresponding frequency spectrum for a three-phase AC-system with 50 Hz and 1000 Hz are shown, respectively. The measurements are done with a load current of 25 A. The corresponding THD values for the ideal grid are only 0.01 % for 50 Hz and 0.013 % for 1000 Hz, respectively. The

second test scenario for the CUT are harmonically distorted grids. Therefore, arbitrary harmonics can be added to the fundamental. For the third test scenario, the unbalanced grid situation or the LVRT/HVRT event, negative and zero sequence components can be added to the positive sequence. In Fig. 14 a) and b) these two scenarios are depicted. For the LVRT-event, the positive component is reduced from 300 V to 200 V and a negative component of 100 V is added at $t = 15$ ms. Through this, the voltage of phase one is still 300 V and the voltages of phase 2 and 3 are reduced to 173 V.
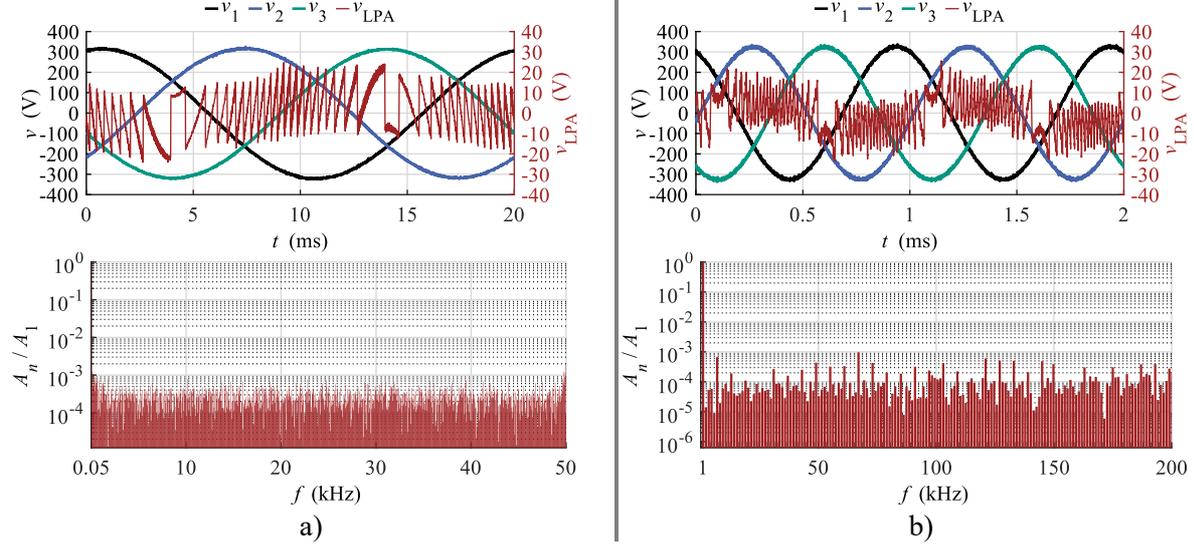

Fig. 13: Measured output voltages and corresponding frequency spectrum for a) 50 Hz and b) 1000 Hz
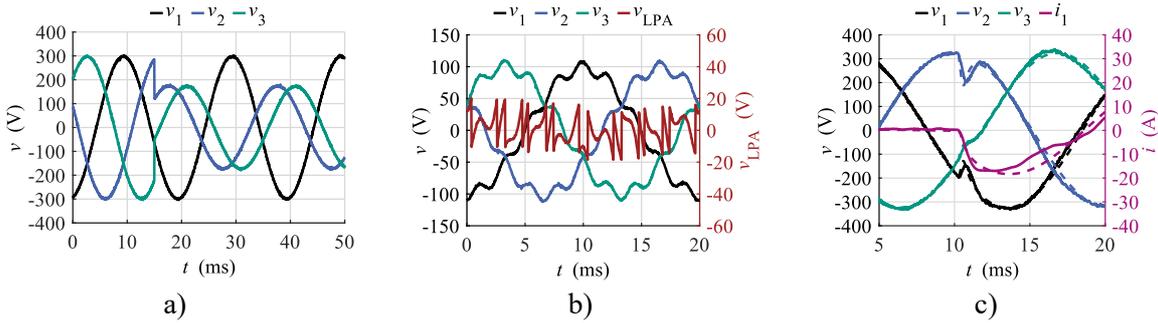

Fig. 14: Emulation of the different grid failures: a) line-to-line failure; b) harmonically distorted grid; c) weak grid situation with an emulated damped RL grid impedance and load step from 0 kW to 10 kW at t =10 ms

For the last test scenario, the grid emulation is activated using the DITM interface algorithm to generate a weak grid situation. The emulated grid impedance is a damped RL-equivalent with $L_{gr} = 5$ mH, $R_{gr} = 200$ mΩ and $R_D = 450\,\Omega$. In Fig. 14 c), the moving average values of the voltage and current waveforms over the 50 kHz control period of the CUT are shown. At $t = 10$ ms, a load step of 10 kW is generated by the CUT. The dashed line are the simulated current and voltage waveforms and the solid line are the measurement results. As can be seen, the measured voltage results are almost identical to the simulated results. The oscillation that occurs at the measured current is caused by the CUT controller and not by the PHIL system and thus is a "desired" oscillation that must be analyzed and can be inhibited by optimizing the CUT controller. Hence, the PHIL system is able to emulate the given line impedance. In the first three test scenarios, the grid emulation was deactivated but it is also possible to combine different test scenarios e.g. unbalanced grid scenario with the grid impedance emulation.

VI. Conclusion

This paper presents the hardware and the software structure of a Power Hardware-In-the-Loop (PHIL) system for emulating various grid situations, such as voltage dips and spikes, distorted grids and weak grid situations to analyze the behavior of grid-connected converters (CUT). The requirements for the different parts of the PHIL system are discussed and their implementation is presented. Subsequently, an analysis of the accuracy and stability of the grid impedance emulation for different interface

algorithm (IA) is done and the most suited IA is chosen for the grid impedance emulation. Measurement results of four test scenarios for analyzing the CUT are presented, which show the performance of the developed PHIL system.

The next rewarding research would be the analysis of the frequency dependent behavior of the CUT with sinusoidal test signals added to the fundamental component for parametrizing the model of the CUT. Thus, a better prediction of the CUT is possible to prevent e.g. unstable grid situations.

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