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Generalised Multistage Modelling and Tuning Algorithm for Class EF and Class Φ Inverters to Eliminate Iterative Retuning

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***Abstract*—The additional complexity of Class EF and Class Φ inverters compared to their Class E counterparts, combined with parasitic effects becoming more prevalent as frequency and power levels increase, results in poor accuracy from traditional design methods, and usually additional iterations of manual retuning are required. Furthermore, after making these additional iterations it is practically impossible to ensure that all the desired design conditions are met in hardware, due to the number of degrees of freedom in these circuits. In this work we propose an approach to simulating and tuning Class EF/Φ inverters, with various levels of accuracy depending on the level of knowledge of the system parasitics. Our method is comprised of a combination of analytic and numerical solving methods thus providing both insight on the progression of the algorithm and computational robustness. The aim of our algorithm formulation is to enable solutions to be found in an automated and fast way. The novelty in our work lies in the design method's concurrent capability to provide a generalised set of design inputs (e.g. DC to AC current gain, arbitrary drain voltage slope at turn on, ϕ-branch resonance, etc.), inclusion of board and device non-linear parasitics, and the ability to design within the set of preferred component values. An example is shown for the design of a 50 W, 13.56 MHz inverter where the experimental setup approaches the theoretical efficiency of 97%, whilst maintaining all of the other design requirements. The algorithm changes the values of the components over 5% to 50% and improves the simulated waveform accuracy by 2 to 12 times compared to the design method based on first order approximations.**

***Index Terms*—Class EF, Class Φ, resonant power converter, inverter design, circuit simulation, high frequency, wireless power transfer.**

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I. Introduction

Transmitting power using a high frequency (HF) induction offers numerous benefits for wireless power transfer (WPT) systems as the link can be realised with miniaturised and lightweight air core coils with high quality factors (Q) that can transmit power efficiently over low coupling [1]–[3]. Advances in wide-bandgap devices make the realisation of HF inductive power transfer (IPT) systems operating in MHz frequency range more attractive, where the Class E type single switch resonant converter circuits demonstrate benefits over the Class D type drivers [4]–[6].

The properties of the basic Class E inverter can be enriched and the design possibilities can be expanded by adding resonant networks in parallel and in series with the series load network [7]–[11]. These topologies have been given different names in the literature based on the resonant frequency of those additional networks and the degree that the input choke is contributing to the rest of the resonant circuit of the inverter. In this work we use the term "Class EF_n" when referring to a design with an infinite choke and "Class Φ_n" when the finite input choke is contributing to the resonant behaviour of the inverter, where "n" is the ratio of the resonance frequency of the single parallel resonant branch (ϕ-branch) over the switching frequency. The two additional degrees of freedom for defining the behaviour of the inverter that the ϕ-branch provides enables the Class EF/Φ inverters to achieve better device power capability utilisation by shaping the drain voltage and to decrease total harmonic distortion (THD) by filtering the output current, compared to the typical Class E converters. These additional degrees of freedom also expand the number of circuit operating properties that can be set independently, beyond what can be achieved with Class E inverters. For example, load independent operation can be achieved with a Class E converter using a finite DC feed inductor [10], [12], [13], but Class EF can do the same with a infinite choke [10], which can be preferable in cases where a low ripple input current is required.

Because of the high number of design variables combined with the low component value tolerances of these resonant circuits, it is typical that additional manual retuning is required, which is an iterative procedure based on trial and error [10], [14]–[16]. This process is not trivial and requires high level of insight and experience [14], [16], [17], especially at high operating frequency and power level. Most importantly though,

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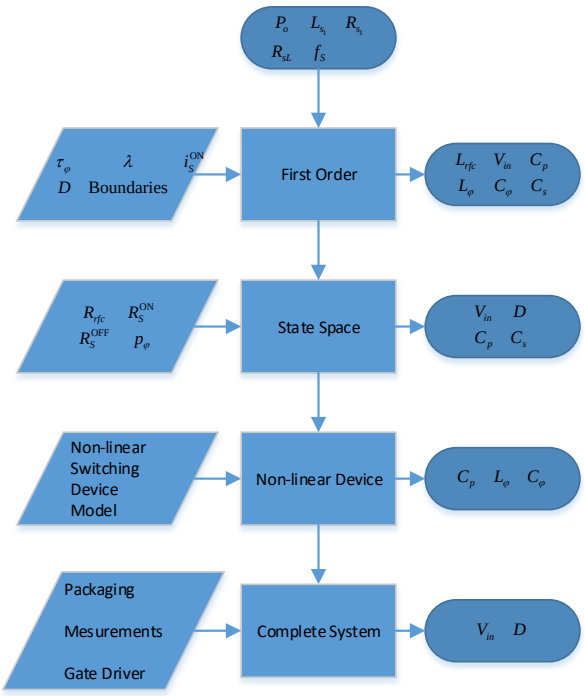

Fig. 1. Class EF/Φ inverter design flowchart diagram.

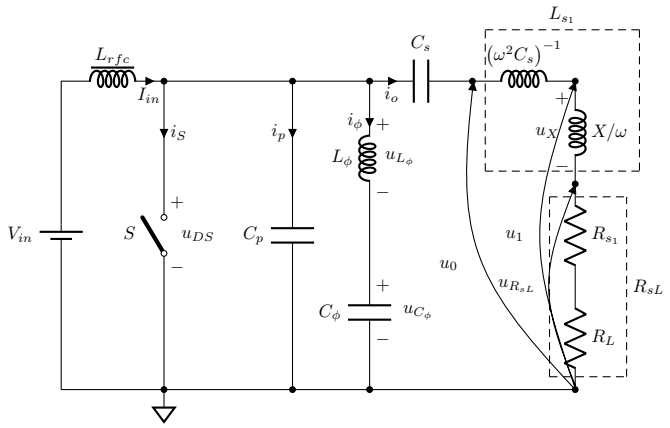

Fig. 2. Circuit diagram of Class EF/Φ inverter using the first order formulation.

after such alterations to the original design, it is not guaranteed that the final experimental setup will still remain true to the initial design requirements [18].

The main motivation leading to this work is to eliminate the need of manual retuning of Class EF/Φ inverters, by developing a robust and reproducible design method, which can be fully automated and produces reliable results with high accuracy. In addition, our method is able to cater for designs based on specification of several different properties of the converter circuit such as, the DC to AC current gain, the slope of the drain voltage at turn on while maintaining zero voltage switching (ZVS) at the specified ϕ-branch resonance frequency. The scope of this work is to explain the details of the proposed design algorithm rather than propose specific inverter designs.

Our proposed algorithm provides different levels of precision, depending on the amount of information that is available about the system. Different complexities of models from ideal first order (FO) approximations to state space (SS) models with a non-linear switching device are used. Furthermore, in order to take full advantage of the design degrees of freedom that the Class EF/Φ inverter provides, this algorithm regularly ensures during its progression that the required properties of the circuit are maintained until the end, with no external supervision form the user being needed.

II. Overview

The inverter design process flow chart is illustrated in Fig. 1. It consists of four main, interdependent steps executed in sequence, which are further explained in the corresponding sections. Depending on the desired accuracy of simulation to experimental matching requirements, the tuning process can be terminated at the end of any of the specified steps of the procedure.

The first step of the design algorithm (section III) is based on FO analysis of the circuit. It is the least accurate part of the proposed tuning process. However, it is the only one that uses analytic expressions, and its main contribution is that it provides a good starting point for the iterative methods that follow, ensuring speed and convergence. Typically, the component values that this part of the design algorithm produces are not very accurate, mainly due to its inherit simplification, as explained in subsection III-A. The accuracy of the outputs can be evaluated by an LTspice simulation, which will determine whether the subsequent steps of the algorithm need to be applied.

The second tuning part, analysed in section IV, is based on SS representation of the circuit and resolves any approximation and simplification errors caused by the first part. The accuracy of the outcome of this algorithm step should be practically enough when the switching frequency is low enough so that the shunt capacitor value (circuit diagram details given in subsection III-A) is substantially higher than the effective output capacitance of the device (for a given power level). This is due to the fact that the values of the energy storing components are related to the operating frequency. Usually, when this is the case, the effect of the rest of the parasitic capacitances of the device along with the stray package inductances and gate driver imperfections are negligible, too. If any of the two first steps of the algorithm fail to converge or produce a realistic result, it is an indication that the operation requirements cannot be met with the given input conditions.

The third part introduces a more representative non-linear model of the switching device and compensates for the changes caused by the parasitics of the device, and is discussed in section V. Proceeding to this part of the algorithm is required at higher switching frequencies, as the theoretical speed threshold of the converter is approached. If this part

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TABLE I
INPUTS AND OUTPUTS OF FIRST ORDER TUNING EXAMPLE

	Quantity	Value	Unit
Inputs	P_o	50	W
	τ_ϕ	2	–
	λ	5	–
	i_S^{ON}	0	A
	R_{sL}	8.6	Ω
	R_{s_1}	346	mΩ
	L_{s_1}	1.24	μH
	f_S	13.56	MHz
	D	30	%
	Boundaries	$\left\{i_\phi, u_{C_\phi}\right\}$	–
Outputs	V_{in}	78.835	V
	C_p	228.971	pF
	L_ϕ	536.941	nH
	C_ϕ	64.141	pF
	C_s	150.317	pF

doesn't converge, it means that the parasitics of the transistor of choice cannot be absorbed in the circuit.

The fourth part includes effects caused by the unavoidable mismatch between the theoretical optimal component values and their actual experimental measurements and is given in section VI. This stage is essential when this mismatch becomes substantial, mostly due to limitations of off the shelf passive component values. The last two parts also include the effects of the packaging of the device and gate drive signal shaping resistances. Convergence failure during the last part of our algorithm shows that the circuit design cannot be realised with preferred values.

The description of the experimental setup and circuit examples used for the verification of the performance of our proposed method are given in section VII and in the Appendix. Measurements are taken across a variety of operating conditions and the evaluation of the accuracy and contribution of each tuning step is performed.

III. FIRST ORDER APPROXIMATION

The first section of the proposed tuning algorithm uses a FO approximation. The derivation of the design equations and the corresponding assumptions they are based on have been extensively described in [5], [18]–[21] for infinite choke Class E, in [22], [23] for the finite choke Class E, in [7], [24], [25] for the Class Φ, and in [10], [26] for the Class EF inverter. Second order approximations for the simulation of Class E inverters have been applied in [27]. In this work we formulate the problem using a combination of the analytic methods mentioned above in a way that provides both control and insight to the user about the tuning of the resulting circuit. This part of the design algorithm is the only one that is based on analytical synthesis; the rest use iterative optimisation. As stated previously, the design algorithm uses the FO approach as an initial point for the iterative procedures that follow in the next steps, for faster and more controlled convergence.

A. Design and Simulation Equations

The circuit diagram of an ideal Class EF/Φ inverter is shown in Fig. 2. In this work we implement the Class EF/Φ inverter as a primary coil driver in WPT applications. In the diagram of Fig. 2, L_{s_1} is the transmitter (Tx) coil inductance and R_{sL} is the series combination of the primary coil resistance (R_{s_1}) with the equivalent resistance of the secondary reflected to the primary ($R_L = R_{sL} - R_{s_1}$), with zero reflected reactance [5]. The final component of the series load network is the C_s capacitor. The input choke inductance (L_{rfc}) can be regarded as either finite (Class Φ) or infinite (Class EF). C_p is the shunt capacitor to the switching device (S) and L_ϕ in series with C_ϕ form the added resonant ϕ-branch network parallel to the load network, which is absent in the Class E inverter.

As shown in Fig. 1, the FO design process of the inverter begins by determining the requirements of the IPT system, namely the output power P_o and switching frequency f_S. Then, we define the desired characteristics of the circuit, i.e., the frequency of the ϕ-branch normalised to f_S (τ_ϕ), the duty cycle (D), the ratio λ of the peak output current (I_m) to the input current (I_{in}) (which represents the DC to AC current gain), and the current through S at turn-on (i_S^{ON}). R_{sL} is defined according to the inductive link properties and the corresponding choice of L_{s_1}, while R_{s_1} is an intrinsic property of L_{s_1}.

We assume that the load network Q is high enough, i.e., $\omega L_{s_1}/R_{sL} > 15$ [5], so that the current through the coil can be approximated as sinusoidal [19]: $i_o(\theta)/I_{in} = \lambda \sin(\theta + \phi)$, where ϕ is the output current phase relative to the gate signal of the switching device [20], and $\theta = \omega t$ is the angular time in radians, with $\omega = 2\pi f_S$ being the angular switching frequency and t being the time. The input current is $I_{in} = I_m/\lambda$, where $I_m = \sqrt{2P_o/R_L}$. Since the only losses incorporated in the circuit are in the Tx coil, $V_{in} = \lambda I_m R_{sL}/2$. If it is preferable to design with the input voltage set as condition, then the last equation needs to be solved for λ instead.

Since S is modelled as an ideal switch, there is no voltage drop across it when turned on and no current flows through it during turn-off. Also, the current through C_p during turn-on is considered to be zero. By applying Kirchhoff's voltage (KVL) and current law (KCL) to the ϕ-branch and solving the resulting differential equation for the ϕ-branch current using the Laplace transform we get:

$$\left.\frac{i_\phi(\theta)}{I_{in}}\right|_{\theta_{\mathrm{ON}}^+ \le \theta \le \theta_{\mathrm{OFF}}^-} = A_1\left(i_\phi\left(\theta_{\mathrm{ON}}^+\right)\right)\cos(\tau_\phi\theta) + B_1\left(u_{C_\phi}\left(\theta_{\mathrm{ON}}^+\right)\right)\sin(\tau_\phi\theta) \tag{1}$$

$$\left.\frac{i_\phi(\theta)}{I_{in}}\right|_{\theta_{\mathrm{OFF}}^+ \le \theta \le \theta_{\mathrm{ON}}^-} = A_2\left(i_\phi\left(\theta_{\mathrm{OFF}}^+\right)\right)\cos(\tau_2\theta) + B_2\left(u_{C_\phi}\left(\theta_{\mathrm{OFF}}^+\right)\right)\sin(\tau_2\theta) - P_1\sin(\theta+\phi) + K_1 \tag{2}$$

where $\theta_{\mathrm{ON}}^+ = 0$, $\theta_{\mathrm{ON}}^- = 2\pi$ and $\theta_{\mathrm{OFF}} = \theta_{\mathrm{ON}}^- D$ are the boundary angles at turn-on and turn-off, respectively; $A_{1,2}$ and $B_{1,2}$ are boundary conditions dependent coefficients; u_{C_ϕ} is the voltage across C_ϕ; $K_1 = p/\lambda$; $\tau_2 = \tau_\phi/\sqrt{K_2}$ and $K_2 = 1 - K_1$; and $P_1 = p\tau_2^2/(\tau_2^2 - 1)$.

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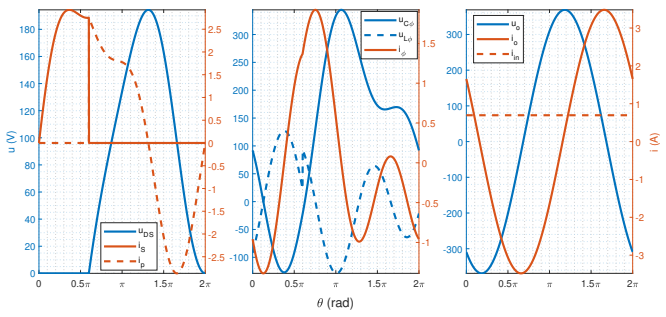

Fig. 3. Inverter waveforms of the numerical example given in Table I. The voltages are shown in blue on the left-hand side vertical axes of the graphs and the currents in orange on the right-hand side. The parts of the circuit each individual waveform corresponds to is given in Fig. 2. The graph on the left shows the shunt network waveforms, the middle graph represents the ϕ-branch and the graph on the right has the input-output waveforms.

By definition, the voltage across L_ϕ (u_{L_ϕ}) and u_{C_ϕ} can be directly calculated from i_ϕ:

$$\frac{u_{L_\phi}(\theta)}{V_{in}} = \frac{\omega B_C L_\phi}{a} \cdot \begin{cases} \tau_\phi \left[B_1 \cos(\tau_\phi\theta) - A_1 \sin(\tau_\phi\theta)\right], \\ \theta_{\text{ON}}^{+} \le \theta \le \theta_{\text{OFF}}^{-} \\ \tau_2 \left[B_2 \cos(\tau_2\theta) - A_2 \sin(\tau_2\theta)\right] - P_1 \\ \cdot \cos(\theta+\phi), \ \theta_{\text{OFF}}^{+} \le \theta \le \theta_{\text{ON}}^{-} \end{cases} \tag{3}$$

$$\frac{u_{C_\phi}(\theta)}{V_{in}} = \frac{k}{a} \begin{cases} \frac{A_1}{\tau_\phi}\sin(\tau_\phi\theta) - \frac{B_1}{\tau_\phi}\sin(\tau_\phi\theta), \\ \theta_{\text{ON}}^{+} \le \theta \le \theta_{\text{OFF}}^{-} \\ \frac{A_2}{\tau_2}\sin(\tau_2\theta) - \frac{B_2}{\tau_2}\sin(\tau_2\theta) \\ + P_1\cos(\theta+\phi) + K_1\theta + E, \\ \theta_{\text{OFF}}^{+} \le \theta \le \theta_{\text{ON}}^{-} \end{cases} \tag{4}$$

where $B_C = \omega C_p$, $k = C_p/C_\phi$, and

$$\begin{aligned} \theta_{\text{ON}}^{-} a &= K_2\left(\theta_{\text{OFF}} - \theta_{\text{ON}}^{-}\right)^2 + P_2\left[\sin(\theta_{\text{OFF}}+\phi)\right. \\ &+ \left(\theta_{\text{ON}}^{-} - \theta_{\text{OFF}}\right)\cos(\theta_{\text{OFF}}+\phi) - \sin\phi\left.\right] + \frac{A_2}{\tau_2}\left[\frac{1}{\tau_2}\right. \\ &\cdot \left(\cos(\tau_2\theta_{\text{ON}}^{-}) - \cos(\tau_2\theta_{\text{OFF}})\right) + \left(\theta_{\text{ON}}^{-} - \theta_{\text{OFF}}\right) \\ &\cdot \sin(\tau_2\theta_{\text{OFF}})\left.\right] + \frac{B_2}{\tau_2}\left\{\frac{1}{\tau_2}\left[\sin(\tau_2\theta_{\text{ON}}^{-})\right.\right. \\ &\left.\left. - \sin(\tau_2\theta_{\text{OFF}})\right] - \left(\theta_{\text{ON}}^{-} - \theta_{\text{OFF}}\right)\cos(\tau_2\theta_{\text{OFF}})\right\} \end{aligned} \tag{5}$$

$$\begin{aligned} E &= P_1\left[\frac{\cos\phi}{K_2\tau_2} - \cos(\theta_{\text{OFF}}+\phi)\right] - K_1\theta_{\text{OFF}} \\ &+ \frac{B_2}{\tau_2}\left[\cos(\tau_2\theta_{\text{OFF}}) - \frac{1}{K_2}\right] - \frac{A_2}{\tau_2}\sin(\tau_2\theta_{\text{OFF}}). \end{aligned} \tag{6}$$

If we were to derive the exact waveform expressions of the inverter in Fig. 2, we should be solving a 6th degree differential equation (which is the approach we follow in the 2nd part of this proposed design algorithm). However, doing so results in overly complicated analytical expressions of very limited practical use. Even the approximation of infinite L_{rfc} and high Q output network still requires solving a 3rd order differential equation with two boundary conditions (device turned-off and on). For comparison, the Class E inverter requires solving just one FO differential equation [19].

To overcome this, we made one more simplification, which despite introducing another source of error, results in a more manageable expression with a good trade-off of accuracy to complexity: we treat the ϕ-branch independently of the shunt capacitor network during turn-off. This is also obvious from the formulation of the current through the ϕ-branch equations that follows, which incorporates only four boundary dependent parameters ($A_{1,2}$,$B_{1,2}$) instead of six, which effectively reduces the degree of the differential equation from three to two. This results in simpler and more compact analytic waveform expressions. The choice of the ϕ-branch specifically is also based on the fact that during turn-on it is already independent of the shunt capacitor, since the device is shorting it. It should be mentioned that this approach is fairly typical in the existing literature [10], [26]. The additional source of error introduced by this approach is eliminated by the more accuracy-based iterative tuning process of the subsequent algorithmic stage in section IV, which simulates the circuit using the full sixth degree state space differential equation solution.

Given the above reasoning, the on-off boundary conditions of the ϕ-branch-shunt network can involve any combination of two signals among the drain voltage (u_{DS}), i_ϕ and u_{C_ϕ}. Different combinations of boundary conditions will provide different inverter designs, for the same inputs. The designer can choose the preferred boundaries based on the component values that they provide and the focus of the modelling accuracy of the FO approximation, since the parts off the circuit that the boundaries are applied will be simulated with more precision. As an example, we provide the exact equations satisfying the switching continuity conditions for the i_ϕ and u_{C_ϕ} boundaries. By using (1), (2) and (4) to satisfy the boundary continuity conditions we get $[A_1,\ B_1,\ A_2,\ B_2]^T = \mathbf{B}^{-1}\mathbf{a}$, where

$$\mathbf{a} = \begin{bmatrix} K_1 - P_1\sin(\theta_{\text{OFF}}+\phi) \\ K_1 - P_1\sin\phi \\ \frac{P_1\cos\phi}{\sqrt{K_2}} \\ P_1\left[\cos(\theta_{\text{OFF}}+\phi) - \left(1+\frac{1}{\tau_2 K_2}\right)\cos\phi\right] \\ + \left(\theta_{\text{ON}}^{-} - \theta_{\text{OFF}}\right)K_1 \end{bmatrix}. \tag{8}$$

By applying KCL while the device is not conducting and incorporating i_o and (2), the normalised current through C_p is given by:

$$\begin{aligned} \left.\frac{i_p(\theta)}{I_{in}}\right|_{\theta_{\text{OFF}}^{+} \le \theta \le \theta_{\text{ON}}^{-}} &= K_2 + P_2\sin(\theta+\phi) \\ &- A_2\cos(\tau_2\theta) - B_2\sin(\tau_2\theta). \end{aligned} \tag{9}$$

The voltage across the device during the off time is directly derived from integrating (9):

$$\begin{aligned} a\left.\frac{u_{DS}(\theta)}{V_{in}}\right|_{\theta_{\text{OFF}}^{+} \le \theta \le \theta_{\text{ON}}^{-}} &= K_2\theta - P_2\cos(\theta+\phi) \\ &- \frac{A_2}{\tau_\phi}\sin(\tau_\phi\theta) + \frac{B_2}{\tau_\phi}\cos(\tau_\phi\theta) + C \end{aligned} \tag{10}$$

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$$\mathbf{B} = \begin{bmatrix} \cos\left(\tau_\phi \theta_{\mathrm{OFF}}\right) & \sin\left(\tau_\phi \theta_{\mathrm{OFF}}\right) & -\cos\left(\tau_2 \theta_{\mathrm{OFF}}\right) & -\sin\left(\tau_2 \theta_{\mathrm{OFF}}\right) \\ 1 & 0 & -\cos\left(\tau_2 \theta_{\mathrm{ON}}^{-}\right) & -\sin\left(\tau_2 \theta_{\mathrm{ON}}^{-}\right) \\ \sin\left(\tau_\phi \theta_{\mathrm{OFF}}\right) & -\cos\left(\tau_\phi \theta_{\mathrm{OFF}}\right) & 0 & \dfrac{1}{\sqrt{K_2}} \\ 0 & \dfrac{1}{\tau_\phi} & \dfrac{\sin\left(\tau_2 \theta_{\mathrm{ON}}^{-}\right) - \sin\left(\tau_2 \theta_{\mathrm{OFF}}\right)}{\tau_2} & \dfrac{\cos\left(\tau_2 \theta_{\mathrm{OFF}}\right) - \cos\left(\tau_2 \theta_{\mathrm{ON}}^{-}\right) - \dfrac{1}{K_2}}{\tau_2} \end{bmatrix} \tag{7}$$

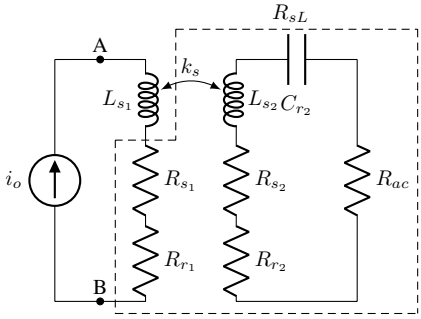

Fig. 4. WPT link with a current source as inverter, series secondary tuning capacitor and AC load.

where

$$C = \frac{A_2}{\tau_2}\sin\left(\tau_2 \theta_{\mathrm{OFF}}\right) - \frac{B_2}{\tau_2}\cos\left(\tau_2 \theta_{\mathrm{OFF}}\right) - K_2 \theta_{\mathrm{OFF}} + P_2 \cos\left(\theta_{\mathrm{OFF}} + \phi\right). \tag{11}$$

Applying KCL while the switching device is conducting, by combining (1) and i_o, gives the normalised current through the device:

$$\left.\frac{i_S\left(\theta\right)}{I_{in}}\right|_{\theta_{\mathrm{ON}}^{+} \le \theta \le \theta_{\mathrm{OFF}}^{-}} = 1 - A_1 \cos\left(\tau_\phi \theta\right) - B_1 \sin\left(\tau_\phi \theta\right) - \lambda \sin\left(\theta + \phi\right). \tag{12}$$

Applying the ZVS condition through (10) results in the equation:

$$C\left(p, \phi\right) = P_2\left(p, \phi\right)\cos\phi + \frac{A_2\left(p, \phi\right)}{\tau_2\left(p\right)}\sin\left(\theta_{\mathrm{ON}}^{-}\tau_2\left(p\right)\right) - \theta_{\mathrm{ON}}^{-} K_2\left(p\right) - \frac{B_2\left(p, \phi\right)}{\tau_2\left(p\right)}\cos\left(\theta_{\mathrm{ON}}^{-}\tau_2\left(p\right)\right). \tag{13}$$

The drain current is equal to i_p at turn-on, because of the discharge of the shunt capacitor. Hence, we can apply the condition of the drain current at turn-on by using (9):

$$\frac{i_S^{\mathrm{ON}}}{I_{in}} = K_2\left(p\right) + P_2\left(p\right)\sin\phi - A_2\left(p, \phi\right) \cdot \cos\left(\theta_{\mathrm{ON}}^{-}\tau_2\left(p\right)\right) - B_2\left(p, \phi\right)\sin\left(\theta_{\mathrm{ON}}^{-}\tau_2\left(p\right)\right) \tag{14}$$

where i_S^{ON} is the drain current at turn-on. Since the boundary dependent parameters $A, B_{1,2}(p, \phi)$ are interconnected, in this work we solve the combined system of $A, B_{1,2}$, (13) and (14) using the trust-region-dogleg algorithm described in [28], [29].

The input voltage is equal to the mean of the drain voltage, hence $C_p = \omega V_{in}/(a I_{in})$. Using the definition of the loading parameter [30], we get $C_\phi = pC_p/(\lambda - p)$. The ϕ-branch inductor is calculated from the resonance frequency, $L_\phi = (\omega\tau_\phi)^{-2} C_\phi^{-1}$.

Following the convention proposed in [19], we define u_X as the fictitious voltage across the residual series reactance $X = \omega L_{s_1} - (\omega C_s)^{-1}$ of the load network at f_S (X is assumed to be infinite at any other frequency), since C_s and L_{s_1} are not exactly at resonance. We also define the voltage u_1 as the combined effect of voltage across R_{sL} ($u_{R_{sL}}$) and u_X. The magnitude of u_1 is equal to the Fourier component of u_{DS} at f_S, which results in the relation:

$$\pi B_C \lambda R_{sL}\sqrt{1 + \tan^2\psi} = K_2 f_1\left(\psi\right) + P_2 f_2\left(\psi\right) + \frac{A_2}{2\tau_2} f_3\left(\psi\right) + \frac{B_2}{2\tau_2} f_4\left(\psi\right) \tag{15}$$

where ψ is the phase difference between i_o and u_1, and

$$f_1\left(\psi\right) = \sin\left(\phi + \psi\right) - \left(\theta_{\mathrm{ON}}^{-} - \theta_{\mathrm{OFF}}\right)\cos\left(\phi + \psi\right) - \sin\left(\theta_{\mathrm{OFF}} + \phi + \psi\right) \tag{16}$$

$$f_2\left(\psi\right) = \frac{\cos\left(2\phi + \psi\right)}{4} - \pi\left(1 - D\right)\sin\psi + \frac{\cos\left(2\theta_{\mathrm{OFF}} + 2\phi + \psi\right)}{4} - \frac{\cos\left(\theta_{\mathrm{OFF}} - \psi\right)}{2} + \frac{\cos\psi}{2} - \frac{\cos\left(\theta_{\mathrm{OFF}} + 2\phi + \psi\right)}{2} \tag{17}$$

$$f_3\left(\psi\right) = \frac{\sin\left(\left(\tau_2 + 1\right)\theta_{\mathrm{ON}}^{-} + \phi + \psi\right)}{\tau_2 + 1} + \frac{\tau_2 \sin\left(\left(\tau_2 + 1\right)\theta_{\mathrm{OFF}} + \phi + \psi\right)}{\tau_2 + 1} + \frac{\tau_2 \sin\left(\left(\tau_2 - 1\right)\theta_{\mathrm{OFF}} - \phi - \psi\right)}{\tau_2 - 1} - \frac{\sin\left(\left(\tau_2 - 1\right)\theta_{\mathrm{ON}}^{-} + \phi + \psi\right)}{\tau_2 - 1} - \sin\left(\tau_2 \theta_{\mathrm{OFF}} + \phi + \psi\right) - \sin\left(\tau_2 \theta_{\mathrm{OFF}} - \phi - \psi\right) \tag{18}$$

$$f_4\left(\psi\right) = \frac{\tau_2 \cos\left(\left(1 - \tau_2\right)\theta_{\mathrm{OFF}} + \phi + \psi\right)}{1 - \tau_2} - \frac{\cos\left(\left(1 - \tau_2\right)\theta_{\mathrm{ON}}^{-} + \phi + \psi\right)}{1 - \tau_2} - \frac{\tau_2 \cos\left(\left(\tau_2 + 1\right)\theta_{\mathrm{OFF}} + \phi + \psi\right)}{\tau_2 + 1} - \frac{\cos\left(\left(\tau_2 + 1\right)\theta_{\mathrm{ON}}^{-} + \phi + \psi\right)}{\tau_2 + 1} - \cos\left(\tau_2 \theta_{\mathrm{OFF}} - \phi - \psi\right) + \cos\left(\tau_2 \theta_{\mathrm{OFF}} + \phi + \psi\right). \tag{19}$$

The series load capacitance is derived from X, $C_s = (\omega L_{s_1} - R_{sL}\tan\psi)^{-1}\omega^{-1}$, where ψ is calculated by solving (15)

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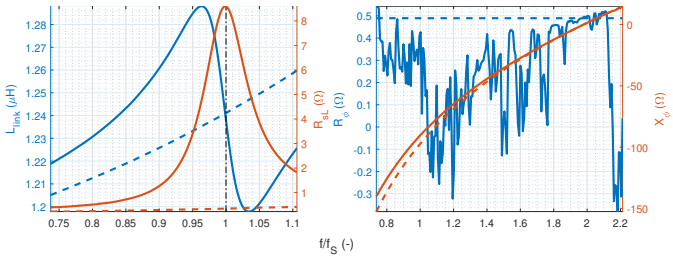

Fig. 5. Inductance and series resistance measurement of the fully loaded (solid line) and unloaded (dashed line) IPT link (left), and total series resistance and reactance measurements (solid line) and fitting curves (dashed line) of the ϕ-branch with impedance analyser, where $X_{\phi}^{\mathrm{fit}}(f) = \left(2\pi f L_{\phi} C_{\phi} - 1\right) / 2\pi f C_{\phi}$.

using a combination of bisection, secant, and inverse quadratic interpolation methods described in [31], [32].

The normalised voltage across the Tx coil is:

$$\frac{u_o(\theta)}{V_{in}} = \frac{B_C \lambda}{a}\left(\omega L_{s_1}\cos(\theta+\phi) + R_{sL}\sin(\theta+\phi)\right). \quad (20)$$

The minimum impedance value of the input choke must be substantially higher than the input resistance of the inverter [21], $L_{rfc} \gg R_{in}/\omega$, where $R_{in} = \lambda^2 R_{sL}/2$. For the special case of the inverter with a finite DC-feed inductance and $50\,\%$ duty cycle the input inductance value can be calculated using the expression proposed in [33] combined with R_{in}.

B. Measurements and Numerical Example

The application of the FO tuning equations is presented in the numerical example below. This example is further developed and improved in the following chapters of this paper. The inputs that were chosen to define the circuit properties are given in Table I, along with the corresponding outputs of the algorithm. The waveforms across various parts of the circuit shown in Fig. 2 are given in Fig. 3.

The complete WPT system of the experimental setup is shown Fig. 4 [34]. The inverter is represented as a current source connected to the Tx coil and the Receiver (Rx) coil (L_{s_2}) is connected to an AC load (R_{ac}) via a series tuning capacitor (C_{s_2}), k_s is the coupling factor and $R_{r_{1/2}}$ is the radiation resistance of the Tx and Rx, respectively.

R_{ac} consists of 12 LTO100F100R0JTE3 AC resistors in parallel. Because of the relatively low value of R_{ac} we opt for a series-tuned secondary [5], where the theoretical value of the tuning capacitor is $C_{s_2} = (\omega^2 L_{s_1})^{-1}$ since the two coupled coils are identical in our setup, whereas the generalised computation of the tuning capacitors is given in [35]. The WPT coils consist of two planar spiral turns made of FR-4 printed circuit board (PCB) with maximum outer radius $r_o = 10.5\,\mathrm{cm}$, minimum inner radius $r_i = 6.75\,\mathrm{cm}$, track width of $1\,\mathrm{cm}$, across distance $d_s = 12\,\mathrm{cm}$ with zero lateral misalignment and angle. An estimation of the order of magnitude of the radiation resistances of the coils based on the size and geometry mentioned above, based on [36], gives $R_{r_{1/2}} \approx 1.137\,\mathrm{m\Omega}$.

The impedance measurements of the fully loaded ($k_S = k_S^{\max}$) and unloaded ($k_S = 0$) IPT link taken with an impedance analyzer (E4990A Impedance Analyzer from Keysight Technologies) across the points A and B in Fig. 4 are provided in Fig. 5. The value of C_{s_2} was manually adjusted using the tuning method described in [37] starting from the theoretical value. The measurements were taken from the empty inverter board with only the Tx coil soldered in place. This way, the adjustment of C_{s_2}, which in our setup are $3\,\mathrm{kV}$ C0G capacitors, naturally incorporates the stray inductances and capacitances of the PCB and the rest of the passive components, and the measurements represent the effective values of the circuit components. If a parasitic extraction tool is available, the incorporation of their effect can be done a posteriori in the calculations with the individual component values, however the above mentioned method of measurements gave the most accurate results when compared to the theoretical predictions.

The numerical values of the equivalent series resistances in the measurements of Fig. 5 and Table I are several orders of magnitude larger than $R_{r_{1,2}}$, and thus their effect can be considered negligible. An analytical approximation of the Tx inductance can be derived by [38], $L_{s_1} \approx 1.062\,\mu\mathrm{H}$. This estimation agrees with the measurements of Fig. 5, if we take into consideration and add the effects of the stray inductances of the SMA connectors. The coupling factor is calculated using the formula in [37] and the experimental measurements as inputs, $k_s^{\max} \approx 8.011\,\%$. It must be noted at this point that the link was neither optimised for radiation [36], nor gain [39].

The aim of this inverter circuit example is to achieve maximum efficiency at the lower ISM bands. In order to be able to measure AC current accurately, we limit the output power within the capabilities of the current probe at these frequencies, namely Keysight N2783B. We set the ϕ-branch to resonate at double the switching frequency to reduce THD [5], [40]. We minimise the ohmic losses by reducing the currents and increasing the voltages in the circuit through a high λ value. Additionally, we minimise the switching device losses by applying zero derivative switching (ZDS), despite that this condition will result in non load independent operation, as defined in [10]. The duty cycle was chosen based on [10]. The output power capability and distribution of device stress is mainly determined by λ and D; high λ and low D increase the current demands and decrease the voltage requirements and vice versa. The boundaries were selected according to the signals that we want to simulate more accurately.

By comparing the input requirements in Table I with the waveforms in Fig. 3 we can verify that all the desired properties of inverter are met. The limitation of the applied boundary conditions is revealed through the discontinuity during switching of u_{L_ϕ}.

IV. State Space Tuning

Analytical expressions for designing Class E inverters at any load network Q have been derived in [41], [42]. An alternative approach of deriving design equations based on fitting datasets is presented in [14]. Search optimisation algorithms based on the more accurate linear SS simulation of the circuit have also been used for defining the passive component values

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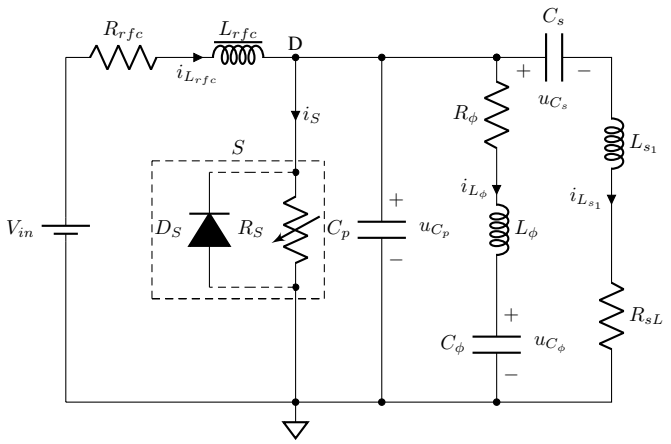

Fig. 6. Circuit diagram of Class EF/Φ inverter using the State Space formulation.

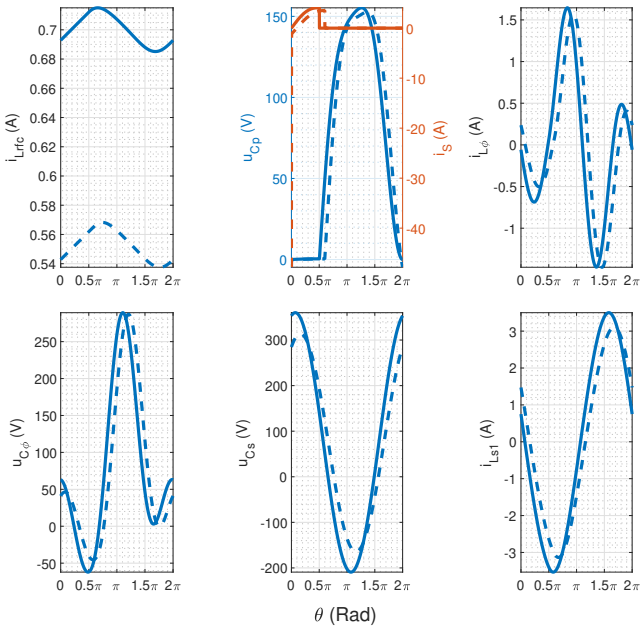

Fig. 7. Simulation of the Class EF_2 inverter waveforms using state-space formulation. The dashed line is used to represent the design that occurs from the FO tuning method and the solid line shows the state-space tuned inverter.

of the inverter [8], [30], [43], with the downside that such numerical approaches provide limited insights and control of the tuning process to the user, do not provide such a broad range of design input parameters, are relying on random initial parameters to run and are usually computationally demanding and provide no guarantee of a practically realisable design output. An extension to traditional first order design methods is proposed in [44] using higher order analysis but some of the design component values need to be set initially, which may be problematic.

The second tuning step of the proposed algorithm uses a piece-wise SS representation for the formulation of the problem. However, instead of using a predefined optimisation tool for the design process, we develop a custom Newton based iterative method, starting from the solution of the previous step. The SS simulation resolves the approximation errors of the FO analysis and the aim of the numerical optimisation is to fine-tune the inverter while maintaining the required design properties. The advantages in modelling accuracy of the SS approach compared to FO approximations in Class E converters is demonstrated in [45], [46].

A. Simulation Equations

At this part of the algorithm, we replace the infinite choke with its actual measured value, and we model the switching device as a variable resistance $R_S^{\mathrm{ON/OFF}}$. Also, as shown in Fig. 6, we incorporate the series resistance R_{rfc} of the input choke, and Q factor of the ϕ-branch through the parameter $p_\phi \equiv \tau_\phi \omega / \left. Q_{L_\phi}(f)\right|_{f=\tau_\phi f_S}$, since $R_\phi = p_\phi L_\phi$ is proportionate to the windings L_ϕ.

The 6th order system of linear SS differential equations of the inverter is solved separately for the on/off periods, in a piece-wise linear manner, and its solution is given by:

$$\begin{aligned}\mathbf{q}(\theta)\big|_{\theta^+_{\mathrm{ON/OFF}} \le \theta \le \theta^-_{\mathrm{OFF/ON}}} &= \mathrm{e}^{\left(\theta-\theta^+_{\mathrm{ON/OFF}}\right)\mathbf{A}_{\mathrm{ON/OFF}}} \\ &\cdot \mathbf{q}\left(\theta_{\mathrm{ON/OFF}}\right) + \mathbf{A}^{-1}_{\mathrm{ON/OFF}} \\ &\cdot \left(\mathrm{e}^{\left(\theta-\theta^+_{\mathrm{ON/OFF}}\right)\mathbf{A}_{\mathrm{ON/OFF}}} - \mathbf{I}\right)\mathbf{b}\end{aligned} \tag{21}$$

where $\mathbf{I}$ is the identity matrix, $\mathbf{b} = V_{in}(\omega L_{rfc})^{-1}\mathbf{e}_1$ with $\mathbf{e}_i$ being the single entry column vector whose i^{th} element is one and the rest are zero, and the state matrix and vector are defined as follows:

$$\begin{aligned}&\mathbf{A}_{\mathrm{ON/OFF}} = \\ &\frac{1}{\omega}\mathrm{diag}^{-1}\left(L_{rfc}, C_p, L_\phi, C_\phi, C_s, L_{s_1}\right) \\ &\cdot \begin{bmatrix} -R_{rfc} & -1 & 0 & 0 & 0 & 0 \\ 1 & \dfrac{-1}{R_S^{\mathrm{ON/OFF}}} & -1 & 0 & 0 & -1 \\ 0 & 1 & -R_\phi & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & -1 & -R_{sL} \end{bmatrix}\end{aligned} \tag{22}$$

$$\begin{aligned}\mathbf{q}(\theta) = \big[\ & i_{L_{rfc}}(\theta) \quad u_{C_p}(\theta) \quad i_{L_\phi}(\theta) \quad u_{C_\phi}(\theta) \\ & u_{C_s}(\theta) \quad i_{L_{s_1}}(\theta)\ \big]^T.\end{aligned} \tag{23}$$

The boundary continuation conditions when the switching device is turning on and off during one period are calculated by applying the Schur complement [47]: $[\mathbf{q}(\theta_{\mathrm{ON}}),\ \mathbf{q}(\theta_{\mathrm{OFF}})]^T = \mathbf{C}^{-1}\mathbf{E}$, where

$$\mathbf{E} = \begin{bmatrix} \mathbf{A}^{-1}_{\mathrm{OFF}}\left(\mathrm{e}^{\left(\theta^-_{\mathrm{ON}}-\theta_{\mathrm{OFF}}\right)\mathbf{A}_{\mathrm{OFF}}} - \mathbf{I}\right)\mathbf{b} \\ \mathbf{A}^{-1}_{\mathrm{ON}}\left(\mathrm{e}^{\theta_{\mathrm{OFF}}\mathbf{A}_{\mathrm{ON}}} - \mathbf{I}\right)\mathbf{b} \end{bmatrix} \tag{24}$$

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TABLE II
INPUTS AND OUTPUTS OF STATE SPACE CLASS EF_2 TUNING EXAMPLE

	Quantity	Value	Unit
Inputs*	I_m	3.481	A
	L_{rfc}	72	µH
	R_{rfc}	500	mΩ
	R_S^{ON}	100	mΩ
	R_S^{OFF}	650	MΩ
	p_ϕ	1×10^6	$\Omega\,\mathrm{H}^{-1}$
Outputs	V_{in}	75.7	V
	D	25.169	%
	C_p	284.559	pF
	C_s	143.166	pF
Relative Change	$\delta(V_{in})$	−3.977	%
	$\delta(D)$	−16.103	%
	$\delta(C_p)$	21.277	%
	$\delta(C_s)$	−4.757	%

*The inputs given in this table are in addition to the data of Table I.

$$\mathbf{C}^{-1} = \begin{bmatrix} \left[\mathbf{I} - \mathrm{e}^{\left(\theta_{\mathrm{ON}}^{-} - \theta_{\mathrm{OFF}}\right)\mathbf{A}_{\mathrm{OFF}}} \mathrm{e}^{\theta_{\mathrm{OFF}}\mathbf{A}_{\mathrm{ON}}}\right]^{-1} & \mathbf{0} \\ \mathbf{0} & \left[\mathbf{I} - \mathrm{e}^{\theta_{\mathrm{OFF}}\mathbf{A}_{\mathrm{OFF}}} \mathrm{e}^{\left(\theta_{\mathrm{ON}}^{-} - \theta_{\mathrm{OFF}}\right)\mathbf{A}_{\mathrm{OFF}}}\right]^{-1} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{I} & \mathrm{e}^{\left(\theta_{\mathrm{ON}}^{-} - \theta_{\mathrm{OFF}}\right)\mathbf{A}_{\mathrm{OFF}}} \\ \mathrm{e}^{\theta_{\mathrm{OFF}}\mathbf{A}_{\mathrm{ON}}} & \mathbf{I} \end{bmatrix} \tag{25}$$

and $\mathbf{0}$ is the zero matrix. The current through the switching device is given by the relation:

$$i_S(\theta)|_{\theta_{\mathrm{ON/OFF}}^{+/-} \le \theta \le \theta_{\mathrm{OFF/ON}}^{+/-}} = \frac{u_{C_p}(\theta)}{R_S^{\mathrm{ON/OFF}}}. \tag{26}$$

Simulating the inverter with (21) gives a more accurate and realistic representation of the operation of the circuit (Fig. 7) compared to the FO formulation, since the assumptions and simplifications that are incorporated in the FO equations are no longer present in the SS approach. By comparing the waveforms in Fig. 3 with the equivalent part of Fig. 7, neither the required design properties of Table I nor the soft switching conditions are met, and further tuning is required.

The additional input parameters needed for the SS simulation in Fig. 7 along with the ones in Table I, are given in Table II. I_m is calculated in the previous tuning step, as described in subsection III-A, and the rest of the input values are based on the component selection of the experimental setup, which are more thoroughly presented and justified in subsection IV-C. Specifically for the input choke, the impedance value chosen in Table II is around 57 times higher than the FO input resistance of the inverter, which practically acts as an infinite choke. The input component values for this stage of the algorithm are not limited only to the ones produced by our proposed first tuning step, but can be derived by any arbitrary design algorithm for Class EF inverters that needs additional correction, as long as the formulation of input conditions matches, such as the special cases discussed in [10].

TABLE III
INPUTS AND OUTPUTS OF STATE SPACE CLASS Φ_2 TUNING EXAMPLE

	Quantity	Value	Unit
Inputs*	L_{rfc}	600	nH
Outputs	V_{in}	77.068	V
	D	20.817	%
	C_p	515.532	pF
	C_s	142.641	pF
Relative Change	$\delta(V_{in})$	−2.368	%
	$\delta(D)$	−30.61	%
	$\delta(C_p)$	125.152	%
	$\delta(C_s)$	−5.107	%

*The inputs given in this table are in addition to the data of Tables I and II.

B. Iterative Tuning Process

In this section we introduce a tuning method using the SS representation in order to correct the inaccuracies caused by the FO formulation. We choose to keep the ϕ-branch unaltered and adjust the rest of the control parameters accordingly to reassure that the circuit is operating as defined by the input parameters in Table I. This corresponds to readjusting P_o, λ, $u_{C_p}\left(\theta_{\mathrm{ON}}^{-}\right)$ and i_S^{ON} at their desired values by optimising for V_{in}, D, C_p and C_s.

The input voltage determines the output current and hence power. C_s sets the load network impedance, which primarily defines λ but also shapes the drain voltage waveform. C_p and D also shape the drain voltage, with the first one mainly contributing to the value at turn-on and the latter mostly affecting the derivative. Changing the combination of L_ϕ-C_ϕ while keeping τ_ϕ constant also affects the drain voltage shape, however including them as independent variables in the iterative scheme impacts the convergence negatively and makes it uncontrollable.

The state vector formulation in (21) is defined in terms of matrix exponentials which is not a convenient form for dealing with the output current characteristics. By approximating the output current waveform using the sine wave fit algorithm proposed in [48] we can solve for peak output current as well as minimise the THD. The sine coefficients of the fitted waveforms are $y_n = z_1 \cos\theta_n + z_2 \cos\theta_n + z_3$, where $n = 1, 2, ..., N$, N is the waveform discretisation number, $\mathbf{z} = \left[\mathbf{D}^T\mathbf{D}\right]^{-1}\mathbf{D}^T\mathbf{y}$, $\mathbf{y} = \left[i_{L_{s_1}}(\theta_1), \ ..., \ i_{L_{s_1}}(\theta_N\right]^T$, $\theta_n = (n-1)2\pi/(N-1)$, and

$$\mathbf{D} = \begin{bmatrix} \cos\theta_1 & \sin\theta_1 & 1 \\ \cos\theta_2 & \sin\theta_2 & 1 \\ \vdots & \vdots & \vdots \\ \cos\theta_n & \sin\theta_n & 1 \end{bmatrix}. \tag{27}$$

We define the following system of non-linear equations in the form of a vector function:

$$\mathbf{f}(\mathbf{x}) = \begin{bmatrix} u_{C_p}(\theta_{\mathrm{ON}}; \mathbf{x}) & i_{C_p}\left(\theta_{\mathrm{ON}}^{-}; \mathbf{x}\right) - i_S^{\mathrm{ON}} \\ \sqrt{z_1^2(\mathbf{x}) + z_2^2(\mathbf{x})} - I_m & z_3(\mathbf{x}) \\ \dfrac{\max\limits_{\theta} \left|i_{L_{s_1}}(\theta; \mathbf{x})\right|}{I_{L_{rfc}}(\mathbf{x})} - \lambda \end{bmatrix}^T \tag{28}$$

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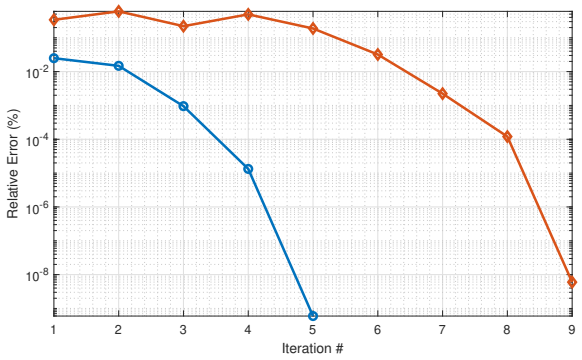

Fig. 8. Convergence progression of the termination condition. The blue circles correspond to the Class EF_2 and the orange diamonds to the Class Φ_2 inverter examples presented in this paper.

where $\mathbf{x} = [C_p,\ D,\ V_{in},\ C_s]^T$; and $I_{L_{rfc}}$ is the DC component of $i_{L_{rfc}}$ which can be obtained either arithmetically e.g., through the trapezoidal rule [49], or by analytically integrating (21). The peak output current in the fifth element of (28) can be calculated by setting the derivative of (21) to zero. The circuit design resulting from the solution of (28) corresponds to the required conditions for ideal tuned operation of the Class EF/Φ inverter, based on the inputs in Table I. More specifically, the first component of (28) is the ZVS condition, the second one sets the slope of the drain voltage at turn-on to the desired value, the third condition sets the output current amplitude according to P_o and the fifth component controls λ. The fourth component of (28) is the DC part of $i_{L_{s_1}}$ and combined with the third component result in reducing THD, when satisfied.

We solve (28) using the combined gradient-descent and Newton's method iterative algorithm mentioned in [50]:

$$\mathbf{x}^{(m+1)} = \mathbf{x}^{(m)} - \left\{\gamma\left(a_N\left[\mathbf{J}_\mathbf{f}^T\mathbf{J}_\mathbf{f}\left(\mathbf{x}^{(m)}\right)\right]^{-1} - a_{GD}\mathbf{I}\right) + a_{GD}\mathbf{I}\right\}\mathbf{J}_\mathbf{f}^T\left(\mathbf{x}^{(m)}\right)\mathbf{f}\left(\mathbf{x}^{(m)}\right) \tag{29}$$

where m denotes the iteration index, γ is the mixing parameter of Newton's and gradient-descent methods, a_N and a_{GD} are the respective converging coefficients and $\mathbf{J_f}$ is the Jacobian matrix of $\mathbf{f}$ with respect to $\mathbf{x}$. The condition that needs to be satisfied for the termination of the iterative process in (29) is $\|\mathbf{x}^{(m} - \mathbf{x}^{(m-1)}\|_\infty / \|\mathbf{x}^{(m)}\|_2 < \epsilon$, where ϵ is the error tolerance.

The partial derivatives of the Jacobian components that cannot be directly computed, i.e. the exponential derivatives with respect to C_p and C_s, can be calculated by any combination of the methods described in [51], [52]. The method described in [51] uses the complex step derivative approach and is simpler to implement as well as less computationally demanding compared to the one in [52]. However, the approach of [52], which is based on matrix diagonalisation, provides a better insight on the actual analytic equation of the derivative. We provide bellow the exact equations of these terms for both approaches, where the subscripts "CS" and "MD" denote the complex step and the matrix diagonalisation derivatives, respectively:

$$\left.\frac{\partial_{CS}\mathrm{e}^{\left(\theta-\theta^+_{\mathrm{ON/OFF}}(\mathbf{x})\right)\mathbf{A}_{\mathrm{ON/OFF}}(\mathbf{x})}}{\partial C_{p/s}}\right|_{\mathbf{x}=\mathbf{x}^{(m)}} = \frac{\mathrm{Im}\left(\mathrm{e}^{\left(\theta-\theta^+_{\mathrm{ON/OFF}}\left(\mathbf{x}^{(k)}\right)\right)\mathbf{A}_{\mathrm{ON/OFF}}\left(\mathbf{x}^{(m)}+\mathrm{j}h\mathbf{e}_{1/4}\right)}\right)}{h} \tag{30}$$

$$\frac{\partial_{MD}\mathrm{e}^{\left(\theta-\theta^+_{\mathrm{ON/OFF}}(\mathbf{x})\right)\mathbf{A}_{\mathrm{ON/OFF}}(\mathbf{x})}}{\partial C_{p/s}} = \mathbf{X}_{\mathrm{ON/OFF}}(\mathbf{x}) \cdot \mathbf{V}_{p/s}^{\mathrm{ON/OFF}}(\mathbf{x};\theta)\,\mathbf{X}^{-1}_{\mathrm{ON/OFF}}(\mathbf{x}) \tag{31}$$

where j is the imaginary unit and h is an infinitesimal positive number [51]. $\mathbf{X}_{\mathrm{ON/OFF}}$ is the matrix whose i^{th} column is a right eigenvector corresponding to the eigenvalue $d_i^{\mathrm{ON/OFF}}$ of $\mathbf{A}_{\mathrm{ON/OFF}}$: $\mathbf{A}_{\mathrm{ON/OFF}} = \mathbf{X}_{\mathrm{ON/OFF}}\mathbf{D}_\mathbf{A}^{\mathrm{ON/OFF}}\mathbf{X}_{\mathrm{ON/OFF}}$, where $\mathbf{X}_{\mathrm{ON/OFF}}$ and $\mathbf{D}_\mathbf{A}^{\mathrm{ON/FF}} = \mathrm{diag}(d_1^{\mathrm{ON/OFF}},\ ,...,\ d_6^{\mathrm{ON/OFF}})$ can be calculated using the QZ decomposition method [53]. The individual entries of $\mathbf{V}_{p/s}^{\mathrm{ON/OFF}}$ are given by:

$$V_{p/s}^{\mathrm{ON/OFF}}[i,j](\mathbf{x};\theta) = \begin{cases} G_{p/s}^{\mathrm{ON/OFF}}[i,j](\mathbf{x})\left(\mathrm{e}^{\left(\theta-\theta^+_{\mathrm{ON/OFF}}(\mathbf{x})\right)d_i^{\mathrm{ON/OFF}}(\mathbf{x})}\right. \\ \left. -\mathrm{e}^{\left(\theta-\theta^+_{\mathrm{ON/OFF}}(\mathbf{x})\right)d_j^{\mathrm{ON/OFF}}(\mathbf{x})}\right) \Big/ \left(d_i^{\mathrm{ON/OFF}}(\mathbf{x}) \right. \\ \left. -d_j^{\mathrm{ON/OFF}}(\mathbf{x})\right),\ i \neq j \\ G_{p/s}^{\mathrm{ON/OFF}}[i,i](\mathbf{x})\left(\theta-\theta^+_{\mathrm{ON/OFF}}(\mathbf{x})\right) \\ \cdot\,\mathrm{e}^{\left(\theta-\theta^+_{\mathrm{ON/OFF}}(\mathbf{x})\right)d_i^{\mathrm{ON/OFF}}(\mathbf{x})},\ i = j \end{cases} \tag{32}$$

where

$$\mathbf{G}_{p/s}^{\mathrm{ON/OFF}}(\mathbf{x}) = \mathbf{X}^{-1}_{\mathrm{ON/OFF}}(\mathbf{x})\frac{\partial\mathbf{A}_{\mathrm{ON/OFF}}(\mathbf{x})}{\partial C_{p/s}} \cdot \mathbf{X}_{\mathrm{ON/OFF}}(\mathbf{x}). \tag{33}$$

C. Class EF_2 Inverter Tuning Example

In this subsection we further improve the numerical example of the Class EF_2 inverter presented in part III-B of this work by using the SS formulation. The additional inputs needed for the computational process, to the ones given in Table I, as well as the resulting adjusted component values with their relative change to the previous tuning step, are given in Table II. The inductance of the choke was measured using the method described in subsection III-B at f_S and its series resistance was measured with a multimeter (Keysight 34465A Digital Multimeter), since the input current is mostly DC. Based on the peak of the drain voltage and current waveforms in Fig. 3 as well as the switching frequency requirements, the switching device of choice is the GS66504B from GaN Systems, which is where the ON and OFF resistances in Table II were derived. The value of p_ϕ was based on the properties of the air-core inductors at $\tau_\phi f_S$ used in the ϕ-branch [3]. The waveforms of the improved design are shown in Fig. 7 displayed in solid

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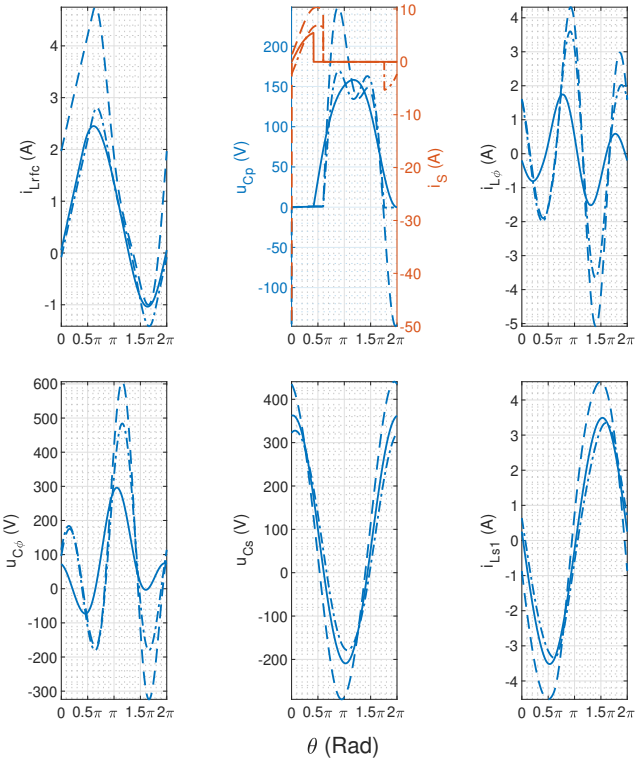

Fig. 9. Simulation of the Class Φ_2 inverter waveforms using state-space formulation. The dashed line is used to represent the design that occurs from the FO tuning method, the dashed-dotted line shows the FO design with an antiparallel diode incorporated into the device and the solid line shows the state-space tuned inverter. The negative limit of the i_S overshoot in the graph is not shown to its full amplitude for improved readability and scaling, since it doesn't provide any meaningful information.

line, compared to the ones from the FO tuning method, shown with dashed lines.

In this example, we calculated $I_{L_{rfc}}$ numerically and used the pure Newton version of (29). For the Jacobian computation we implemented the approach in (30). The iterative progression of the solution convergence of (28) is shown in Fig. 8. Apart from I_m, which was calculated in the previous tuning step, the choice of the component values in Table II are based on their experimental measurements and datasheets.

D. Class Φ_2 Inverter Tuning Example

As mentioned in the Introduction, in this section we show the design of a Class Φ_2 inverter in order to demonstrate the versatility and the design possibilities that the proposed SS tuning method can provide. In the numerical example in subsection IV-C, the inductance of the input choke is large enough so that it can be regarded as infinite. However, by reducing the value of the choke inductance, relative to the inverter input resistance, we get closer to the Class Φ_2 operation.

The inputs and outputs for the Class Φ_2 inverter design example are given in Table III, in addition to the component values required from Tables I and II. Here, the impedance of the input choke is half of the input resistance and the condition for infinite input choke operation does not apply. The progress

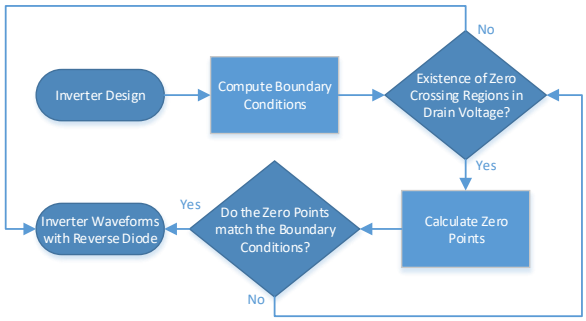

Fig. 10. Flowchart of the algorithm proposed in subsection IV-E for simulating the effect of the intrinsic reverse conducting diode of the switching device to the waveforms of the Class EF/Φ inverter using the state space formulation.

of the convergence procedure is shown in Fig. 8. The FO inverter design that is used as an initial point for the iterative process is again the one mentioned in III-B. The waveforms of the SS variables in Fig. 6 before and after the application of the SS tuning method are shown in Fig. 9.

As expected, the FO method is even more inaccurate when using a finite input choke, since it is based on an infinite input choke assumption. This limitation is reflected in the difference of the waveforms shapes before and after tuning in Fig. 9 as well as the miss-match of the corresponding parts of Fig. 3 and Fig. 9. Also, the tuning process was slower compared to the Class EF_2, as shown in Fig. 8, mostly because the FO initial point of the iterative method is by definition less suitable for the Class Φ inverter design. However the algorithm still manages to produce an inverter design that complies with (28).

E. Simulation of the Device Anti-parallel Diode

As shown in Fig. 7 and Fig. 9, simulating the circuit in Fig. 6 using (21) with the switching boundaries doesn't incorporate the effect of the reverse conducting diode, which is an intrinsic property of power MOSFETs [54] and HEMTs, since the device is blocking both positive and negative current when turned off. The impact of the antiparallel diode to the behaviour of the circuit can be included by adding to the a priori known switching boundary conditions the points in time where u_{C_p} changes polarity during turn-off. However, the process of figuring out the parts of the period during which the reverse diode is conducting is not straight forward and requires a dynamic calculation approach. In this subsection, we propose an iterative scheme, which is broken down in the flowchart in Fig. 10, for the calculation of the time points within a period where the reverse diode turns on and off.

The algorithm begins by setting the inverter design with the corresponding component values and computing the state vector waveforms, as described in subsection IV-A. The next step involves figuring out whether and when the drain voltage during turn-off changes polarity. Solving for the zeros of u_{C_p} is achieved first by splitting the waveform in a predefined number of equal pieces and checking forward in time if the

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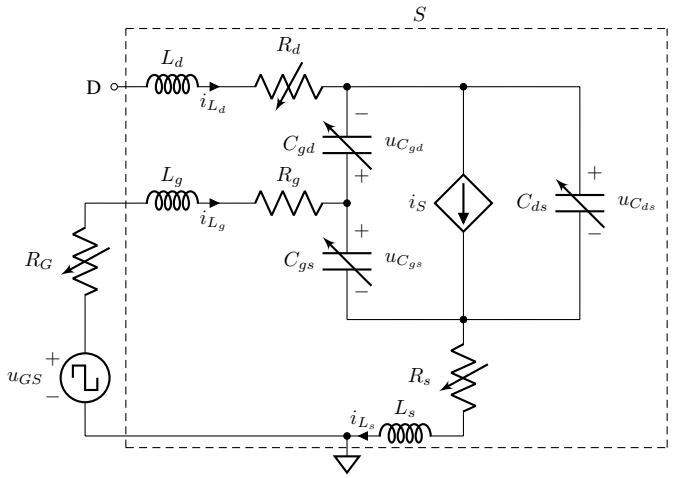

Fig. 11. Circuit diagram of a non-linear model of the switching device in the Class EF/Φ inverter, including parasitic capacitances and resistances, stray package inductances and input gate signal with ON/OFF resistors.

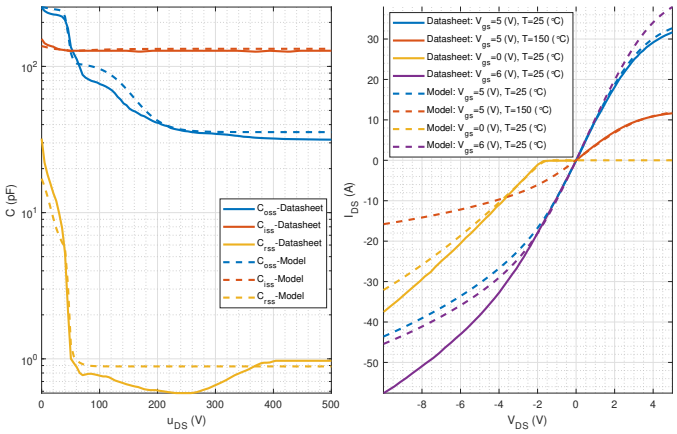

Fig. 12. Visual comparison of the dependence of the internal non-linear capacitances (left) and the drain current (right) on the drain voltage between the datasheet and the fitted model curves. For the case of the drain current, the choice of gate bias and temperature were chosen so that they reflect as closely as possible the numerical example of our experimental setup operation. For the top graph we set $u_{GS} = 0\,\mathrm{V}$ and $T_n = 27\,^{\circ}\mathrm{C}$ for the bottom one.

boundaries of a part have opposing signs. If a waveform part crosses zero, we solve for that point using the Two-Point Newton method in [55], starting the iteration from the edge points. If, however, no such point exists in the entirety of the drain voltage during turn-off, the reverse diode is not conducting and the simulation process is terminated. Once we have solved for all the potential zero crossing points with the current boundary conditions, we readjust the boundary conditions accordingly for the next iteration. At every boundary condition, the conducting state of the device is switched.

The iterative process has converged once the boundary conditions have reached a steady equilibrium, which is applied using the normwise backward error for linear equations [56]:

$$\frac{\|\mathbf{d} - \mathbf{A}_{n-1}\mathbf{c}\|_\infty}{\|\mathbf{A}_{n-1}\|_\infty \|\mathbf{c}\|_1 + \|\mathbf{d}\|_\infty} < \epsilon \tag{34}$$

where $\mathbf{c} = \mathbf{q}(\theta_1) - e^{(\theta_n - \theta_{n-1})\mathbf{A}_{n-1}}\mathbf{q}(\theta_{n-1})$ and $\mathbf{d} = (e^{(\theta_n - \theta_{n-1})\mathbf{A}_{n-1}} - \mathbf{I})\mathbf{b}$.

As an example for the demonstration of the algorithm in Fig. 10 we use the FO design with finite choke of subsection IV-D, since the diode conduction part of the period is substantially larger compared to the corresponding Class EF_2 design. The termination tolerance is 10^{-6}. The resulting waveforms are shown in Fig. 9 and it took 4 iterations for the scheme in Fig. 10 to converge. The need for the iterative scheme in order to determine the reverse diode conducting regions becomes clear from Fig. 9, since the actual point in time that the antiparallel diode of the device begins to conduct does not match exactly the zero crossing point of the non diode drain waveform.

V. Tuning with a Non-Linear Device

Sections III and IV simulate the device behaviour as an ideal switch and a variable resistor, respectively. However, power MOSFETs have non-linear parasitic capacitances [54] which not only introduce delays but also, specifically C_{oss} for the cases of Class E [57] and Class EF inverters [58], are part of the shunt network and their effect should be taken into account in the tuning calculations in order to get accurate results. As we've already shown in section IV, the FO approach is not suitable for Class EF/Φ inverter designs, which means that the method proposed in [57] is not ideal for this case, and [58] is based on manual tuning and fitting of the waveforms along with experimental measurements. A numerical design procedure for Class E inverters at 50% duty cycle is presented in [13], however it is not directly applicable to Class EF inverters. If a detailed and extensive model of the parasitics of the device is not available, the iterative tuning method in our previous work [59] is a powerful option. However it doesn't incorporate the gate drive signal in the calculations and focuses only on maintaining ZVS, while the other properties of the circuit may be altered during the tuning process.

In this section we propose an iterative tuning method, that will further adjust the design produced in IV so that it absorbs the unwanted effects of the device parasitics and the non-ideal gate drive signal, while maintaining all the required input design properties. The circuit model of the device as well as the simulation equations derived in this section are generally applicable to any transistor. The same applies to the tuning methodology proposed, which is universal. However, since we are dealing with non-linear effects uniquely defined by the specific semiconductor device used, the exact functions of the parasitics behaviour need to be defined accordingly for each individual transistor model.

A. System Modelling

The circuit diagram of the Class EF inverter topology that is used for simulation in this chapter is, for the most part, the one shown in Fig. 6 with a different, more thorough and realistic, transistor model. The switching device is modelled as a non-linear voltage-dependent current source along with a network of non-linear voltage-dependent capacitances [60], [61] and temperature-dependent resistors, as shown in Fig. 11. The stray inductances caused by the packaging of the device

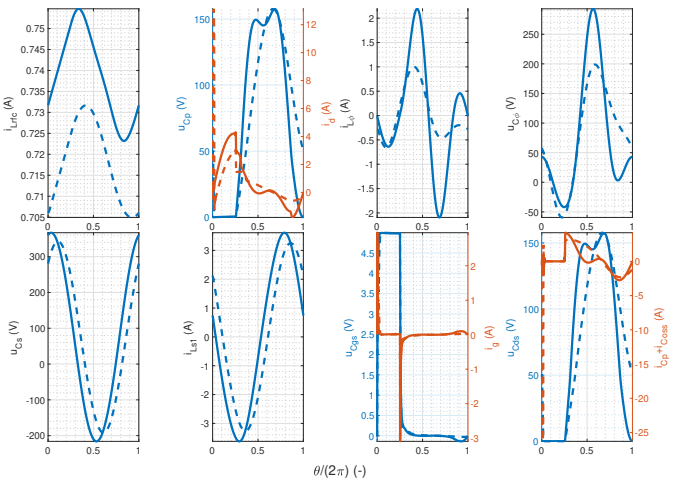

Fig. 13. Simulation of the Class EF_2 inverter using the numerical simulation with the non-linear switching device model. The dashed waveforms correspond to the linear State Space design and the solid ones represent the tuned version.

are incorporated in the computations as inductors at the pins of the device.

Since the three capacitors in Fig. 11 form a delta network, only the voltages across two of them are considered independent SS variables. In this work we choose $u_{C_{gd}}$ to be the dependent one, which is related to the other two device capacitor voltages by the relation: $u_{C_{gd}}(\theta) = u_{C_{gs}}(\theta) - u_{C_{ds}}(\theta)$. The same principle applies for the currents through the package inductances, which form a star network connected at a hypernode. The dependent variable of choice is i_{L_s}, which is given by the relation: $i_{L_s}(\theta) = i_{L_g}(\theta) + i_{L_d}(\theta)$.

Applying KVL and KCL to the inverter with the non-linear device model in Fig. 11 leads to the non-linear 10^{th} order differential equation of the system given below:

$$\omega \mathbf{M}(\mathbf{v}) \frac{\mathrm{d}\mathbf{v}(\theta)}{\mathrm{d}\theta} = \mathbf{U}(\mathbf{v}, u_{GS}, T)\,\mathbf{v}(\theta) + \mathbf{e}_1 V_{in} + \mathbf{n} u_{GS}(\theta) + \mathbf{m}(\mathbf{v})\, i_S(\mathbf{v}, T) \tag{35}$$

where T is the temperature of the device,

$$\mathbf{M}(\mathbf{v}) = \mathrm{diag}\left(L_{rfc}, C_p, L_\phi, C_\phi, C_s, L_{s_1}, L_{gds}, L_{gds}, C_{gds}(\mathbf{v}), C_{gds}(\mathbf{v})\right) \tag{37}$$

$$\mathbf{v} = \begin{bmatrix} i_{L_{rfc}} & u_{C_p} & i_{L_\phi} & u_{C_\phi} & u_{C_s} & i_{L_{s_1}} \\ i_{L_g} & i_{L_d} & u_{C_{gs}} & u_{C_{ds}} \end{bmatrix}^T. \tag{38}$$

$$\mathbf{n} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & n_{ds}+1 & -1 & 0 & 0 \end{bmatrix}^T \tag{39}$$

$$\mathbf{m}(\mathbf{v}) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & m_{dg}(\mathbf{v}) \\ -m_{gs}(\mathbf{v}) \end{bmatrix}^T \tag{40}$$

$$C_{gds}(\mathbf{v}) = m_{gs}(\mathbf{v}) \frac{\partial Q_{C_{ds}}(\mathbf{v})}{\partial u_{C_{ds}}} + \frac{\partial Q_{C_{gs}}(\mathbf{v})}{\partial u_{C_{gs}}} + \frac{\partial Q_{C_{gs}}(\mathbf{v})}{\partial u_{C_{ds}}} \tag{41}$$

$$m_{ds}(\mathbf{v}) = \frac{\partial_{u_{C_{ds}}} Q_{C_{ds}}(\mathbf{v})}{\partial_{u_{C_{gd}}} Q_{C_{gd}}(\mathbf{v})} + 1 \tag{42}$$

TABLE IV
INPUTS AND OUTPUTS OF THE CLASS EF_2 INVERTER TUNING EXAMPLE WITH A NON-LINEAR DEVICE MODEL

	Quantity	Value	Unit
Inputs*	T_n	27	°C
	T	27	°C
	Device	GS66504B	–
	Gate Driver	GLMG1020	–
Outputs	C_p	108.196	pF
	C_ϕ	88.374	pF
	L_ϕ	389.703	nH
	R_ϕ	389.703	mΩ
Relative Change	$\delta(C_p)$	−61.978	%
	$\delta(C_\phi)$	37.781	%
	$\delta(L_\phi)$	−27.422	%
	$\delta(R_\phi)$	−27.422	%

*The inputs given in this table are in addition to the data of Tables I and II.

$$m_{dg}(\mathbf{v}) = \frac{\partial_{u_{C_{ds}}} Q_{C_{gs}}(\mathbf{v})}{\partial_{u_{C_{gd}}} Q_{C_{gd}}(\mathbf{v})} - 1 \tag{43}$$

$$m_{gs}(\mathbf{v}) = \frac{\partial_{u_{C_{gs}}} Q_{C_{gs}}(\mathbf{v})}{\partial_{u_{C_{gd}}} Q_{C_{gd}}(\mathbf{v})} + 1 \tag{44}$$

$L_{gds} = (n_{ds}+1)L_g + L_d$, $n_{gs} = L_g/L_s$, $n_{ds} = L_d/L_s$, $R_{\text{gate}}(u_{GS}) = R_G(u_{GS}) + R_g$, $Q_{C_{gs}}$, $Q_{C_{ds}}$ and $Q_{C_{gd}}$ are the electrical charges in of the corresponding capacitors of the circuit in Fig. 11, and R_G is the resistance for shaping the rise and fall of the gate signal of the switching device.

The input gate signal is determined by the characteristics of gate driver circuit used in the experimental setup, which in our case is the LMG1020, and is modelled as an ideal pulse wave:

$$u_{GS}(\theta) = \begin{cases} 5\,\mathrm{V}, & 0 \le \theta < \theta_{\text{OFF}} \\ 0\,\mathrm{V}, & \theta_{\text{OFF}} \le \theta < \theta_{\text{ON}}^- \end{cases}. \tag{45}$$

The effect of the temperature on the device operation was emulated by the internal drain and source temperature dependent resistances $R_{d/s}(T, T_n)$, where T_n is the reference temperature, which are modelled using the linear FO approximation [62]. The equations of the capacitances and the current source in Fig. 11 are defined based on the small signal and DC MOSFET models described in [63]. The fitting of the drain and source resistances, the drain current, and the internal capacitors of the device on the datasheet curves is performed using the Levemberg-Marquardt damped least-squares method, described in [64] combined with information from reverse engineering the LTspice model provided by the manufacturer.

A demonstration of the visual fitting and comparison between some specially selected data from the datasheet measurements of the device and the above mentioned internal device component models is given in Fig 12. The chosen data curves are the ones quantitatively closest to our case study. A more detailed investigation of C_{oss} losses in a device level approach is presented in [65], [66].

Since (35) is a non-linear system of differential equations, it cannot be solved analytically as in subsection IV-A. For this reason, we approximate the solution of (35) using the numerical approach described in [67]. We define the application

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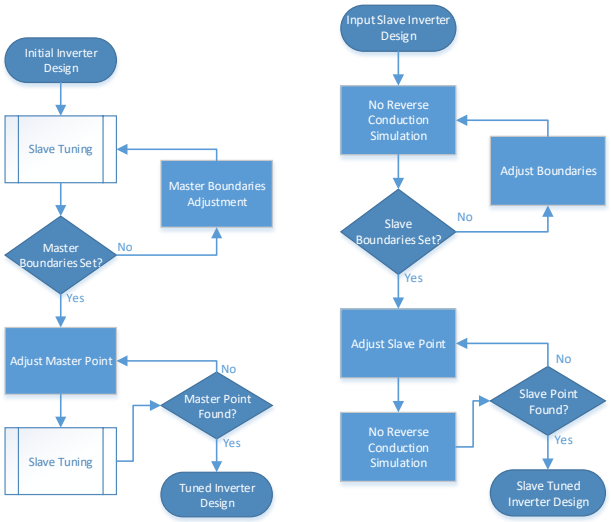
$$\mathbf{U}=\begin{bmatrix} -R_{rfc} & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & -1 & 0 & 0 & -1 & 0 & -1 & 0 & 0 \\ 0 & 1 & -R_{\phi} & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & -R_{sL} & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 & -n_{ds}R_s-(n_{ds}+1)R_{\text{gate}} & 0 & 0 & 0 \\ 0 & n_{gs}+1 & 0 & 0 & 0 & 0 & R_{\text{gate}}-n_{gs}R_s & -n_{gs}(R_d+R_s)-R_d & 1 & -n_{gs}-1 \\ 0 & 0 & 0 & 0 & 0 & 0 & m_{ds} & -m_{dg} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & m_{gs} & 0 & 0 \end{bmatrix} \tag{36}$$



(a) Master Tuning (b) Slave Tuning

Fig. 14. High level flowchart diagrams of the "master" and "slave" tuning processes for adjusting the drain voltage characteristics of the non-linear switching device in a given Class EF inverter design. The subprocess of the "slave" tuning algorithm in (a) is explained in more detail in (b).

of the implicit Crank-Nicolson discretisation formula via an arithmetic mean to (38): $\mathbf{v}_{n+1/2}(\mathbf{v}_{n+1}) \coloneqq (\mathbf{v}_{n+1}+\mathbf{v}_n)/2$, where $\mathbf{v}_n \equiv \mathbf{v}(\theta_n)$. Substituting (38) with $\mathbf{v}_{n+1/2}$ in (35), approximating the derivative with the FO terms of the Taylor series and rearranging the terms appropriately results in $\mathbf{g}(\mathbf{v}_{n+1}) = \mathbf{H}(\mathbf{v}_{n+1})\mathbf{v}_{n+1} - \mathbf{h}(\mathbf{v}_{n+1})$, where

$$\begin{aligned}\mathbf{H}(\mathbf{v}_{n+1}) &= \frac{\omega}{\Delta_n\theta}\mathbf{M}\left(\mathbf{v}_{n+\frac{1}{2}}\right) - \frac{1}{2} \\ &\cdot \mathbf{U}\left(\mathbf{v}_{n+\frac{1}{2}}, u_{GS}(\theta_{n+1})\right)\end{aligned} \tag{46}$$

$$\begin{aligned}\mathbf{h}(\mathbf{v}_{n+1}) &= \left(\frac{1}{2}\mathbf{U}\left(\mathbf{v}_{n+\frac{1}{2}}, u_{GS}(\theta_{n+1})\right) + \frac{\omega}{\Delta_n\theta}\right. \\ &\left.\cdot\mathbf{M}\left(\mathbf{v}_{n+\frac{1}{2}}\right)\right)\mathbf{v}_n + \mathbf{e}_1 V_{in} + \mathbf{n}u_{GS}(\theta_{n+1}) \\ &+ \mathbf{m}\left(\mathbf{v}_{n+\frac{1}{2}}\right) i_S\left(\mathbf{v}_{n+\frac{1}{2}}\right)\end{aligned} \tag{47}$$

and $\Delta_n\theta = \theta_{n+1} - \theta_n$. The converged value of $\mathbf{v}_{n+1}$ is produced by the following iterative scheme:

$$\mathbf{v}_{n+1}^{(m+1)} = \mathbf{v}_{n+1}^{(m)} - r\mathbf{J}_{\mathbf{g}}^{-1}\left(\mathbf{v}_{n+1}^{(m)}\right)\mathbf{g}\left(\mathbf{v}_{n+1}^{(m)}\right) \tag{48}$$

where r is the relaxation parameter.

The individual entries of the Jacobian matrix in (48) are defined as:

$$\begin{aligned}J_{\mathbf{g}}[i,j](\mathbf{v}_{n+1}) &= H_{i,j}(\mathbf{v}_{n+1}) \\ &+ \gamma\left(\sum_{l=1}^{N_{\mathbf{v}}}\frac{\partial H_{i,l}(\mathbf{v}_{n+1})}{\partial v_{n+1}[j]}v_{n+1}[l] - \frac{\partial h_i(\mathbf{v}_{n+1})}{\partial v_{n+1}[j]}\right)\end{aligned} \tag{49}$$

where $N_{\mathbf{v}}$ is the size of the state vector. The mixing parameter in (49) refers to the Newton ($\gamma = 1$) and Picard ($\gamma = 0$) iterations. The inverse of $\mathbf{J}_{\mathbf{g}}$ can be calculated either directly or by applying the bad Broyden method [68]:

$$\begin{aligned}\mathbf{J}_{\mathbf{g}}^{-1}\left(\mathbf{v}_{n+1}^{(m)}\right) &= \mathbf{J}_{\mathbf{g}}^{-1}\left(\mathbf{v}_{n+1}^{(m-1)}\right) \\ &+ \frac{\Delta_m\mathbf{v}_{n+1} - \mathbf{J}_{\mathbf{g}}^{-1}\left(\mathbf{v}_{n+1}^{(m-1)}\right)\Delta_m\mathbf{g}_{n+1}}{\|\Delta_m\mathbf{g}_{n+1}\|_2^2}\Delta_m\mathbf{g}_{n+1}^T\end{aligned} \tag{50}$$

where $\Delta_m\mathbf{v}/\mathbf{g}_{n+1} = \mathbf{v}/\mathbf{g}_{n+1}^{(m)} - \mathbf{v}/\mathbf{g}_{n+1}^{(m-1)}$. However, even when using (50) there is still the need for either an explicit computation or an approximation of the inverse of (49) for the initial iteration, since every subsequent calculation depends on the value of the previous iteration.

The termination condition used in (48) is the equivalent of the one used in subsection IV-A adjusted to $\mathbf{v}_{n+1}$: $\|\Delta_m\mathbf{v}_{n+1}\|_\infty/\|\mathbf{v}_{n+1}^{(m)}\|_2 < \epsilon_{\mathbf{v}}$, where $\epsilon_{\mathbf{v}}$ is the relative error tolerance for the state vector approximation. The initial boundary conditions of (35) mainly affect the convergence speed of the differential equation solution until it reaches steady state and in this work we propose three different ways. The first and simpler possible approach is to start off with a zero state vector and let it evolve until convergence. Another approach, which is by default used in LTspice transient simulations, is to treat the inductors as short circuits and the capacitors as open circuits. Then, the currents through the inductors and the voltages across the capacitors are determined by the independent current and voltage sources in the circuit topology, accordingly. The third suggested approach for defining the initial conditions of the differential equation is to use the state vector values from the previous tuning step, i.e. the linear SS model. The simulation is considered to have reached steady state when the state vector behaviour over a period is not evolving anymore and the process has converged. The condition that we use to determine the termination of the computations is based on the relative error of the DC component of the inverter input current

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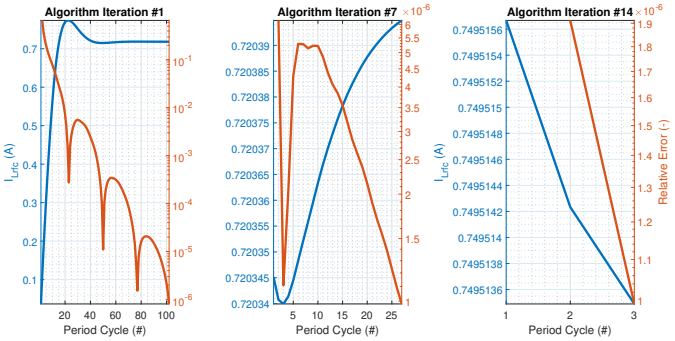

Fig. 15. Convergence of the input current value and its relative error of the Class EF_2 simulation with a non-linear device model for various indicative stages of the tuning algorithm.

between the last two periods: $|I_{L_{rfc}}^{(m_T)} - I_{L_{rfc}}^{(m_T-1)}|/I_{L_{rfc}}^{(m_T)} < \epsilon_T$, where $I_{L_{rfc}}$ is calculated using the trapezoidal method for numerical integration [49], m_T is the iteration index of complete periods computations and ϵ_T is the corresponding error tolerance.

B. Tuning Method

A tuning algorithm for adjusting the drain voltage and slope at turn-on using the shunt and series load capacitors for the Class E inverter is proposed in [69]. However, changes in the value of C_s result in changes in the output power of the inverter, and further tuning of the input voltage, Tx coil inductance and load is required to maintain the desired circuit properties. The higher dimension of degrees of freedom in the Class EF/Φ inverter, compared to the Class E counterpart, enables the absorption of the unwanted effects of the switching device on the shape of the drain waveform using the combination of the shunt and the ϕ-branch capacitors, which introduce minimum effects on the output power of the circuit. Instead of the ϕ-branch capacitor, we could also adjust the duty cycle to control the drain voltage slope at turn-on, however this would result in changes in λ, which corresponds in deviation of the inverter behaviour from the input design requirements.

The proposed tuning process is explained in the flowcharts shown in Fig. 14. It is composed of two parts, the "master" and the "slave" tuning methods. The master tuning method (Fig. 14a) dictates the results of the slave tuning method (Fig. 14b) and the algorithm terminates when the conditions of both processes are satisfied. Both methods are based on the same principle: first set appropriate boundaries in such way that a solution exists within the resulting range, and then search for the solution in it.

The goal of this algorithm is to set the value of the drain voltage to zero, by adjusting the value of C_p, as well as the drain current to i_S^{ON} at turn-on, using C_ϕ. Any adjustments to C_ϕ are followed by the corresponding alterations of L_ϕ according to τ_ϕ, and R_ϕ, so that the resonant frequency of the ϕ-branch filter remains constant. The order in which the two tuning requirements, the drain voltage and current values, will be assigned to the master and slave iterative schemes is up to the designer to choose and affects primarily the convergence but could also lead to different results. For example, the EF_2 example that we use in this work uses the C_ϕ tuning as the master scheme and the C_p as the slave, as it is discussed in the following subsection. However, tuning the inverter example in the Appendix with this method requires the implementation of the opposite master-slave assignment order, compared to the example mentioned above, in order to achieve convergence. The requirement for the tuning process to be repeated iteratively originates from the fact that the effects of C_p and C_ϕ are interconnected and not independent and their adjustments must be treated simultaneously. Instead of the actual drain voltage, we track the $u_{C_{ds}}\left(\theta_{\mathrm{ON}}^{-}\right)$ state variable, since it is the internal signal of the device that controls i_S. As for the drain current, we use the combination of the shunt capacitor current and the output capacitor current of the device:

$$i_{C_p}\left(\theta_{\mathrm{ON}}^{-}\right) + i_{C_{oss}}^{*}\left(\theta_{\mathrm{ON}}^{-}\right) = i_{L_{rfc}}\left(\theta_{\mathrm{ON}}\right) - i_{L_\phi}\left(\theta_{\mathrm{ON}}\right) - i_{L_{s_1}}\left(\theta_{\mathrm{ON}}\right) - i_S^{*}\left(\theta_{\mathrm{ON}}^{-}\right) \tag{51}$$

where i_S^* is the current of the dependent source in Fig. 11 without reverse conduction during turn-off.

The "Initial Inverter Design" in Fig. 14a can be defined with one of the ways proposed in subsection V-A. The "Input Slave Inverter Design" in Fig. 14b is always set to the state vector of the previous iteration, since this approach achieves convergence faster as the iterations advance.

The "No Reverse Conduction Simulation" block in Fig. 14b begins with a simulation according to subsection V-A until steady state is achieved. The property of reverse conduction during turn-off in the device is modelled through the behaviour of i_S and controlled by the sign of $u_{C_{ds}}$. To simulate the device as if it was not reverse conducting we first need to locate the zero crossing point of $u_{C_{ds}}$ and then extend with the evolution of i_S^* from that point until $\theta = \theta_{\mathrm{ON}}^{-}$. The search of the zero crossing point can be done either by looking for $u_{C_{ds}}(\theta) < 0$ forward in time or for $u_{C_{ds}}(\theta) > 0$ backwards in time, with the choice of the search direction affecting the speed of the algorithm. The reason for calculating the electrical signals in the circuit without the property of reverse conduction is because this way we can achieve a better estimation of how far from the solution the current state is during the iterative tuning process and adjust the solver accordingly with more precision, since during reverse conduction both conditions will be close to zero, regardless of how detuned the circuit is.

The block for computing the limits of the boundaries uses the same methodology for both the master and the slave part of the tuning algorithm. First we check whether the existing design constitutes the upper or the lower boundary, based on the sign of the corresponding termination condition. Then, the opposite boundary is updated iteratively until the required sign condition is satisfied. This approach ensures that the resulting range contains a solution since the boundaries are of opposing signs and the transfer function of the inverter is continuous. The update of the component for the opposing boundary limit is computed using the relation $C_{p/\phi}^{(m+1)} = (1 \pm t_{C_{p/\phi}})C_{p/\phi}^{(m)}$, where $t_{C_{p/\phi}} \in (0,1)$ is a parameter that determines the extent of the update. High values of $t_{C_{p/\phi}}$ will require fewer iterations to converge, however low values will result in smaller range, hence better solution approximations for the following steps

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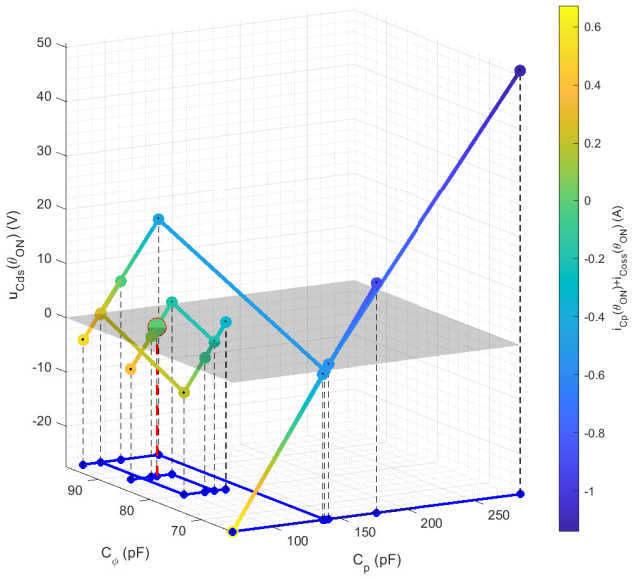

Fig. 16. Four dimensional phase space representation of the tuning algorithm evolution using the non-linear switching device model. The blue line is the two dimensional reflection on the input plane of the higher level convergence path.

of the algorithm. One more way to control the speed and accuracy of the boundaries computations, and differentiates the master block to its slave counterpart, is to update the slave parameter mentioned above before each "Slave Tuning" block: $t_{C_{p/\phi}}^{(m_M+1)} = (1 + t_C^S) t_{C_{p/\phi}}^{(m_M)}$, where m_M is the iteration index of the "Master Tuning" block and $t_C^S \in (-1, 1)$ is a parameter that determines the incremental update of the slave boundary update parameter and can have an effect on the speed of the process by taking advantage of the fact that as the algorithm evolves the approximation of the solution improves.

Once the range and limits of the boundaries are well defined, we use the algorithm proposed in [70] to find the roots of the condition functions within. This algorithm uses a combination of inverse quadratic interpolation and bisection methods for locating the zero of the function in a computationally efficient way, depending on its properties.

The slave tuning block tries to follow the changes introduced by the master tuning method, since every time the master block updates, the slave block needs to re-adapt accordingly. The procedure converges after the two conditions are satisfied simultaneously and the final inverter design is defined.

C. Simulation and Tuning Example

Instead of using the full model in Fig. 11, at this point of the tuning algorithm (3rd part of the flowchart in Fig. 1) we use a reduced model by omitting the effects of the package parasitic inductances and the rise/fall gate resistances. Reducing the accuracy and level of detail of the model is acceptable in this case, since the transistor introduces relatively low stray package inductance and its effect does not affect significantly

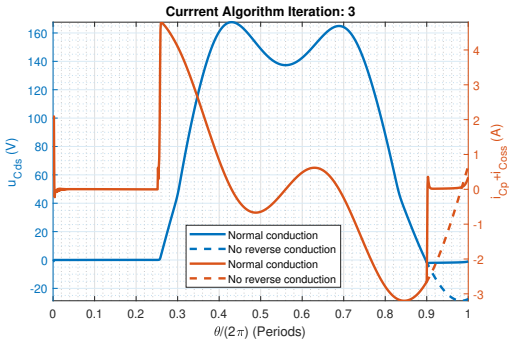

Fig. 17. Example of the output of the "No Reverse Conduction Simulation" block in Fig. 14b, as described in subsection V-B.

the overall behaviour of the circuit. The reduced accuracy of simulation is counterbalanced by a significant increase in computational speed, both because the SS model has fewer degrees of freedom (8 instead of 10) and the discretisation number is not required to be as large compared to the full device model, since there is no need for capturing the ringing caused by the packaging stray inductance. Mathematically, this process is equivalent to equating R_{gate} to R_g, omitting the 7th and 8th rows and columns in (35) and replacing with the following expressions in the corresponding places:

$$i_{L_d} = \frac{u_{C_p} - u_{C_{ds}} + \dfrac{R_s}{R_g + R_s}\left(u_{GS} - u_{C_{gs}}\right)}{R_d + R_s + \dfrac{R_S^2}{R_g + R_s}} \tag{52}$$

and $i_{L_g} = (u_{GS} - u_{C_{gs}} - R_s i_{L_d})/(R_g + R_s)$.

The simulated waveforms of the inverter SS variables before and after tuning are shown in Fig. 13. The design and algorithm inputs, in addition to the ones uses in the previous tuning steps of the algorithm, as well as the output component values and performance metrics of the iterative process are presented in Table IV. The use of the last four tolerance criteria in the "Parameters" section of the table is explained in [70]. As expected, the adjustment of the shunt capacitor value is the most prevalent ($\sim$60 % decrease from the value of the linear SS tuning in Table II), mainly to compensate for the effect of the output capacitance of the switching device. Also, from Table IV we can confirm that the accuracy of the termination conditions agrees with the tolerance demands. This fact can also be confirmed form the corresponding waveforms at the bottom right corner in Fig. 13, where both the soft switching as well as the slope of the drain voltage requirements at turn-on have been restored. Also, by comparing the tuned waveforms in Fig. 7 with Fig. 13 we can confirm that no additional stresses were introduced on the circuit components by the non-linearities of the device, and the tuning algorithm successfully absorbed the any potential unwanted effects.

A characteristic visual demonstration of the output of the process represented by the "No Reverse Conduction Simulation" block in Fig. 14 and further explained in subsection V-B is shown in Fig. 17. Without this process the magnitude and direction of the incremental adjustment of the shunt and ϕ-branch capacitors would be inaccurate, since the drain

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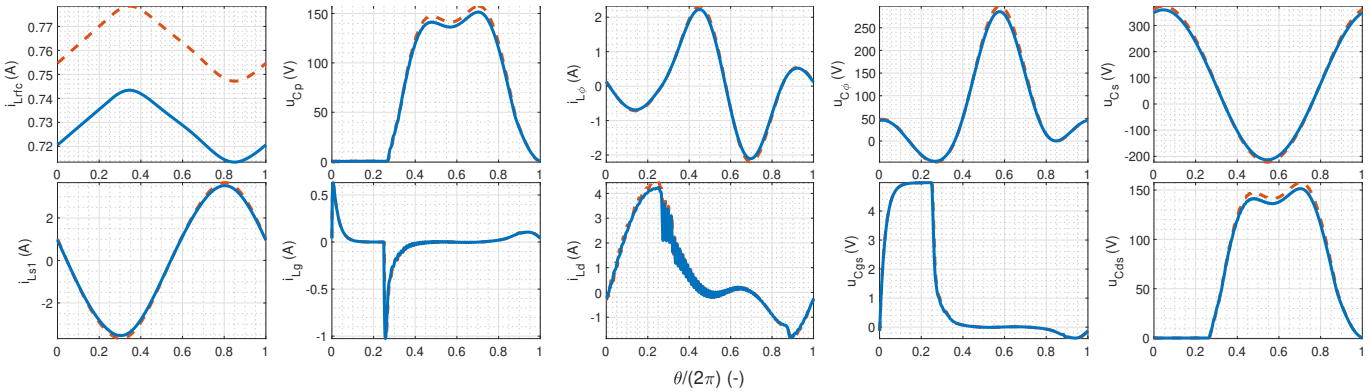

Fig. 18. Waveforms of the state space vector in (38) before (dashed orange line) and after (solid blue line) adjusting the electrical input signals of the inverter for absorbing the undesired effects of the measurement mismatch with the ideal theoretical design component values.

TABLE V
INPUTS AND OUTPUT OF THE CLASS EF_2 INVERTER TUNING EXAMPLE WITH A COMPLETE NON-LINEAR SYSTEM MODEL

	Quantity	Value	Unit
Inputs*	T	40	°C
	C_p	111	pF
	L_ϕ	391	nH
	R_ϕ	489	mΩ
	C_ϕ	90	pF
	C_s	142	pF
	R_G^{ON}	5.3	Ω
	R_G^{OFF}	2.2	Ω
Outputs	V_{in}	73.055	V
	D	24.93	%
Relative Change	$\delta(C_p)$	2.592	%
	$\delta(L_\phi)$	0.333	%
	$\delta(R_\phi)$	25.48	%
	$\delta(C_\phi)$	1.84	%
	$\delta(C_s)$	−0.814	%
	$\delta(V_{in})$	−3.494	%
	$\delta(D)$	−0.95	%

*The inputs given in this table are in addition to the data of Tables I, II and IV.

voltage and current waveform values at turn-on during reverse conduction are not representative of the extend of the detuning.

The figures that follow display the convergence properties of the simulation method (Fig. 15) and tuning algorithm (Fig. 16) described in subsections V-A and V-B, respectively. The relation between the choice of the initial conditions and the computational speed and efficiency of the simulation process is demonstrated in Fig. 15. By using the state vector at turn-on from the previous iteration as initial conditions for the current step during the evolution of the Slave Tuning block in Fig. 14a, the required number of iterations for convergence is reduced drastically, as shown by comparing the graphs in Fig. 15 from left to right. A four dimensional phase space representation of the evolution of the tuning algorithm in general is given in Fig. 16. The spiral shape of the reflection of the path to the plane defined by the C_p and C_ϕ axes proves that actively adjusting $t_{C_{p/\phi}}$ does accelerate the search to convergence.

VI. MEASUREMENTS AND TUNING OF THE EXPERIMENTAL SETUP

In this section of the paper we explain the mechanisms involved in the last tuning step of Fig. 1, i.e. the "Complete System" process block. The theoretical design procedure for defining the component values of the circuit has been completed in the previous tuning steps, and the resulting values are used as guidelines for populating the PCB accordingly. However the actual measured values of the components in the final topology will almost certainly deviate from the ideal case, due to limited off-the-shelf component selection and tolerances.

This issue is typically resolved by performing additional manual retuning [15], [17]. The manual retuning steps are usually based on empirical observation and provide more qualitative instead of quantitative and precise guidelines [10], [14], [18] and tend to require multiple repetitive incremental adjustments based on trial and error. Here, we propose a post-measurement iterative scheme to readjust the operation of the inverter to the actual components using only the provided electrical signals of the board, while still maintaining the desired behaviour based on the input features.

A. Component Measurements and Simulation

For simulating the inverter and computing the corresponding waveforms we used the full switching device model along with the method described in subsection V-A, and the values of the component measurements used are given in Table V. As initial boundary conditions for the simulation calculations we use the SS vector values from the previous tuning step along with (52) and i_{L_g}. This choice results in the fastest computational speed, since the gate shaping resistance and stray package inductance along with the relatively minor deviations of actual components from the ideal values (ranging from 0.12% to 2.59%) results in the initial point not being far from the final solution.

The ON and OFF gate signal shaping resistances are measured individually using the TTi LCR400 Precision LCR Bridge and the package inductances are derived by reverse engineering the LTspice model of the transistor, since the

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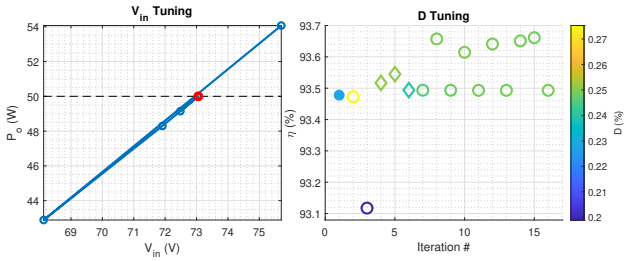

Fig. 19. Tuning progress of the input voltage to achieve the desired output power level (left), which is indicated with the dashed line, and the optimisation search of the duty cycle for maximum efficiency (right). The blue circles on the left graph indicate the intermediate points during the solving process and the red one is the final result. On the left graph, the full circle represents the initial point, the rhombuses are points found with golden section search, and the circles are derived using parabolic interpolation.

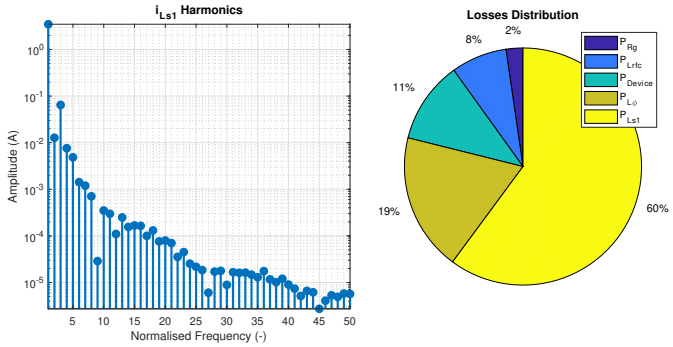

Fig. 20. Amplitude of the output current Fourier series coefficients (left) and relative distribution of the total losses of the Class EF_2 inverter example (right).

datasheet does not provide quantitative stray inductance information. It must be mentioned at this point that the above measurements may divert when applied at MHz frequencies because of instrument and spice model limitations, however their overall effect to the operation of the circuit is not crucial in terms of optimal tuning. Also, the ON and OFF gate resistances selection is based on experimental verification rather than theoretical optimisation, since this kind of investigation is out of the scope of this work.

The shunt and series load capacitors are measured while soldered in place at f_S, as described in subsection III-B. Another option could be to measure the impedance of the fully populated series load branch, i.e. C_s and fully coupled Tx and Rx coils, and fit a series damped resonant model on the measurement point at switching frequency. This is the approach that we use for the ϕ-branch components values derivation, which is based on fitting on the curves of the total impedance within f_S and $\tau_\phi \times f_S$, as shown in Fig. 5. It must be noted that the resistance measurement is unreliable (existence of sections with negative value) because of the high Q factors [71] of the inductors and capacitors used. Also, for the case of C_p and ϕ-branch the probes are connected during measurements to compensate for their additional capacitance to the system. If PCB board and component parasitics, either obtained through impedance measurements or by software extraction, are to be included separately, they can be directly added to the formulation of (36). This applies for both linear and non-linear components. Linear board parasitics can also be simulated in the second part of the algorithm through (22).

The resulting waveforms of the inverter simulation are given in Fig. 18, based on the inputs shown in Table V. As previously, input data that has already been mentioned in previous parts of the paper and have not been altered are ignored. The effects of the ON and OFF gate resistance and the package inductances can be noticed when comparing $u_{C_{gs}}$ and the current through the drain of the device between Fig. 13 and Fig. 18. Specifically, the softer voltage level transitions of $u_{C_{gs}}$ are caused by R_G and the HF ringing oscillations of i_{L_d} after turn-off are driven by the stray package inductances. The ringing of i_{L_d} would be more pronounced across the whole period if the design did not have ZDS. According to subsection V-C, in order to successfully capture these HF ringing transitions in simulation, a finer discretisation is required, which is double that used in the previous section.

B. Explanation and Results of the Tuning Method

This last part of the tuning process consists of two separate and independent iterative schemes that aim to optimise the operation of the final experimental evaluation of the inverter board by adjusting the input voltage and duty cycle in order to achieve the desired power output level with maximum possible efficiency. If we had perfectly ideal components, i.e. linear as in section IV, we would expect that the input voltage would only affect the magnitude of the electrical signals of the inverter proportionally, without disturbing the soft switching conditions and desired operation properties of the circuit. However, the non-linear output capacitance of the device results in loss of ZVS when the input voltage deviates from its optimal value. Also, the duty cycle has an impact on the power throughput of the system, since it changes the equivalent input resistance of the circuit. The above stated reasons basically mean that although we defined the optimisation of each parameter independently, their effect is interconnected, and hence the proposed tuning method should be applied repeatedly until the desired accuracy level is reached. In our case, since the mismatch of the components is low, as mentioned in the previous subsection, and the GS66504B device has low package inductance, a single iteration of the algorithm gives satisfactory level of accuracy and was enough for practical application. Another detail worth mentioning is that optimising the duty cycle for efficiency in general and not strictly to achieve ZVS may be more beneficial in practice and lead to better designs, since with real, non-ideal parts in the circuit ZVS does not always translate to better overall performance, as explained in [15] and shown in the Appendix.

The tuning of the input voltage follows the flowchart shown in Fig. 14b, with the differentiation that instead of using simulation results with no reverse conduction, we use simulation results of the normal device operation. The condition for the boundaries definition is that the two boundary values of the input voltage define a range that includes the desired output power level, by using $t_{C_{p/\phi}}$ but adapted to V_{in}. If more than one repetitions of the full algorithm are applied,

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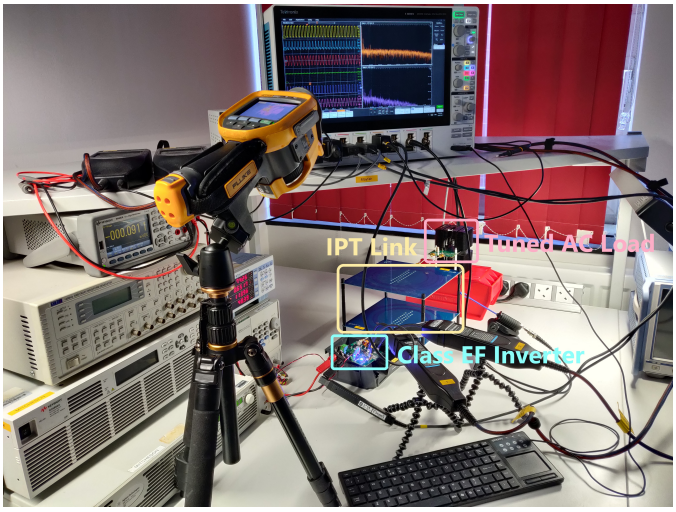


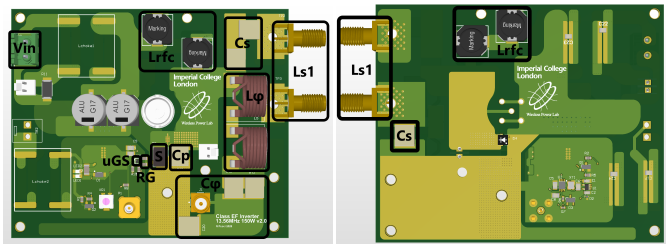
Fig. 21. Photograph of the final experimental setup during operation connected to the oscilloscope for performance verification. The individual parts of the system are highlighted accordingly.

we can use t_C^S to speed up the process, which is not the case of our example. The rest of the algorithm evolution follows exactly the description in subsection V-B. The convergence progression of the algorithm is shown in Fig. 19 and the algorithm parameters and outputs are presented in Table V.

After the input voltage is defined, we proceed by optimising the duty cycle in order to maximise the total efficiency (η) of the inverter. We apply a combined minimisation algorithm comprised of golden section search and parabolic interpolation methods, which are explained in more detail in [31], [32] to find the local minimum of $-\eta$ within a predefined range. The progression of the duty cycle search of the minimiser is given in Fig. 19 and the corresponding algorithm parameters used for our example are shown in Table V.

The SS waveforms of the final design of the Class EF_2 inverter model are given in Fig. 18, and the resulting adjusted parameters and performance metrics of the tuning algorithm are shown at the bottom section of Table V. At this point, it must be clarified that the efficiency on the vertical axis of the right graph in Fig. 19 includes the losses of the link due to the Q factor of the primary coil, whereas the efficiency value stated in Table V corresponds to the efficiency of the inverter only (which is the most common way of defining efficiency in the literature). In both cases the provided power from the gate drive signal is incorporated in the calculations. The efficiency of the real world setup is expected to be lower due to the losses of the gate drive circuit, which the model of an ideal signal generator cannot capture, however the power consumption of the gate drivers for GaN devices can be regarded as negligible compared to the losses of the power components, because of their relatively low input capacitance.

A clearer picture of the percentage distribution of the losses, including the losses of the Tx coil, are given in the pie chart in Fig. 20. The aim of a low current design, as mentioned in subsection III-B, results in relatively low heat dissipation of the passive components. The ZDS condition and low duty cycle design also contributes to achieving low conduction and



(a) Top view (b) Bottom view

Fig. 22. 3D model of the Class EF/Φ inverter PCB. The common mode choke tracks as well as the capacitor voltage deviders are shorted in the real board and the anti-parallel diode is removed. The Tx coil is connected to the SMA connectors.

switching losses on the device. Also, the correct frequency tuning of the ϕ-branch to the desired frequency is confirmed from the Fourier coefficients distribution of the output current in the left graph of Fig. 20, where the amplitude of the 2nd harmonic is suppressed. The contribution of tuning the ϕ-branch to the second harmonic is also reflected in the low THD value of the output current (Table V).

VII. Experimental Verification of the Inverter Performance

A photograph of the experimental setup of the Class EF inverter board, IPT link, and AC load board connected to the Tektronix MSO58 mixed signal oscilloscope is shown in Fig. 21. In addition, we use the Fluke Ti400 infrared camera for monitoring the temperatures of various components on the inverter board and the Yokogawa WT310 digital power meter for measuring the inputs of the system. A more detailed image of the inverter board is shown in Fig. 22. The switching signal for the gate driver can be generated either directly from an external signal generator (TTi 100MHz Arbitrary Waveform Generator TGA12104) or a combination of a crystal oscillator (SG-210STF from Seiko Epson Corporation) and a flip-flop (NC7SV74 from ON Semiconductor), using a potentiometer for duty cycle control. The gate driver signal and input DC voltage were provided with external power supplies (U8032A from Keysight and N8741A from Agilent Technologies, respectively).

The measured waveforms of the inverter board over a range of various loading situations are shown in Fig. 23. Measurements across indicative loading situations over the entire possible load variation range are taken, for more accurate post-measurement characterisation of the inverter and evaluation of the degree of precision of the tuning algorithm and simulation methods. The measurements of u_{C_p} and u_{C_ϕ} are performed using the Tektronix TIVH08 probe with the SQPIN 500X sensor tip cable, since they provide accuracy over a combination of high bandwidth and high voltage. For measuring $i_{L_{rfc}}$ and $i_{L_{s_1}}$ we use the N2783B current probes because their coupling with the IPT link is minimal. The input voltage to the gate of the GaN device is measured with a Tektronix TPP1000 probe. The power meter measurements are presented in Table VI, along with the duty cycle, input voltage and equivalent reflected load for each case.

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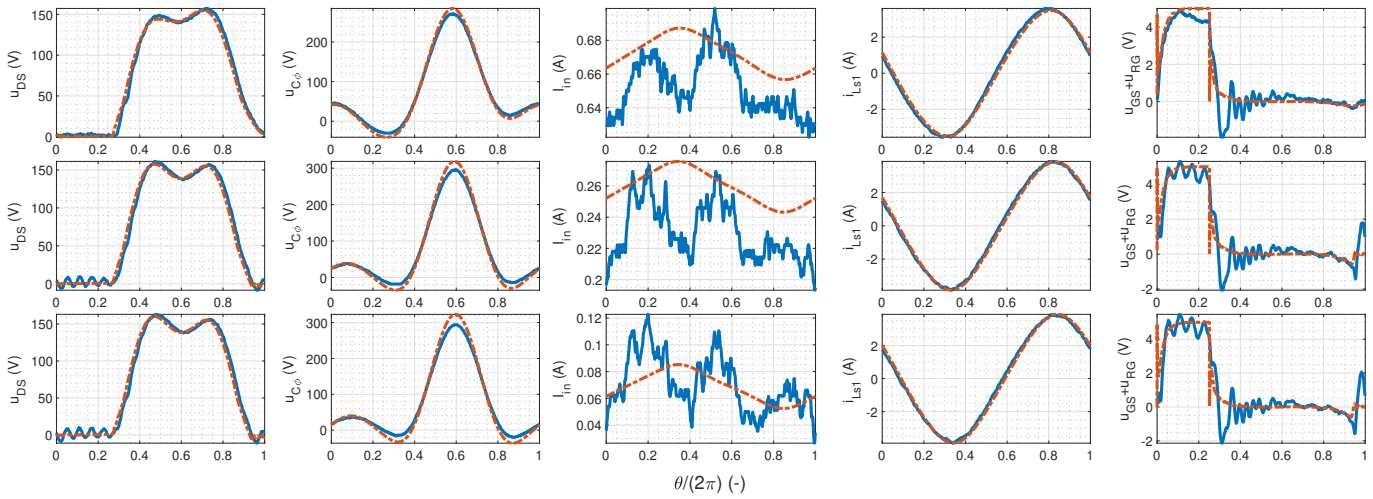

Fig. 23. Comparative display of the experimental waveforms of the inverter extracted from the oscilloscope (blue) over the corresponding outputs of the LTspice model (orange), with 75 V input voltage along different coupling ranges. The first row shows the fully loaded system, the second row shows the results for the same load coupled over a larger gap ($R_{sL} = 2.5\,\Omega$), and the third row is the completely decoupled case.

TABLE VI
EXPERIMENTAL MEASUREMENTS AND TX IMPEDANCE ERROR CORRECTING PARAMETERS FOR THE LTSPICE SIMULATION

		Unloaded	Semi-loaded	Optimal	Overpowered
R_{sL}	(Ω)	0.346	2.5	8.6	8.6
V_{in}	(V)	75.25	75.25	75.25	125.09
D	(%)	25.17	25.17	25.17	30.85
P_{in}	(W)	5.52	18.05	48.58	153.58
R_{in}	(Ω)	1025.6	313.86	116.57	101.89
$p^{*}_{L_{s_1}}$	(%)	1	1	1	1
$p^{**}_{R_{sL}}$	(%)	30	0	−3	−3

$^{*}L_{s_1}^{\text{LTspice}} = \left(1 + p_{L_{s_1}}\right) L_{s_1}^{\text{E4990A}}$.
$^{**}R_{sL}^{\text{LTspice}} = \left(1 + p_{R_{sL}}\right) R_{sL}^{\text{E4990A}}$.

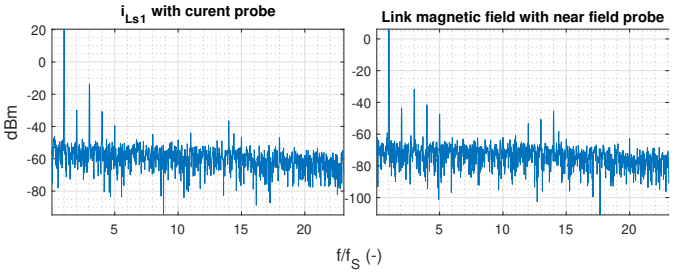

Fig. 24. Spectrum view from the oscilloscope of the output current measurement using a current probe (left) and a qualitative representation of the magnetic field close to the IPT link using a near field probe. The relative positioning of the link and the near field probe is shown in Fig. 21.

A. Error Analysis

The corresponding LTspice simulations are also given for comparison in Fig. 23. For the simulation, we use some correction parameters to compensate for the possible Q factor measurement errors of the IPT link, which are given in the last rows of Table VI. These parameters are set to achieve the best matching to the experimental waveforms. As expected, the inductance measurement of the Tx coil, as well as the equivalent series resistance for the link instances with higher coupling are extremely accurate, given the HF measurement condition. However, a 30 % adjustment was required for the real part of the impedance of the Tx coil when uncoupled, which is in agreement with the limitations of the measuring instrument, according to [71].

Some of the errors between simulation and measurements can be attributed to measurement artifacts. The mismatch of the voltage across the ϕ-branch is due to the error introduced by the high attenuation of the probe (2×500X) combined with offset accuracy limitations of the oscilloscope. The main cause of the noise on the input current measurement is the placement of the current probe before the decoupling capacitors, along with lack of common mode filter and oscilloscope scaling errors and probe DC measurement limitation. The placement of the probe used for the measurement of the input gate voltage resulted in it being affected by the magnetic field of the IPT link as well as introducing parasitics to the gate path, which results in noise on the gate signal and a slight delay to the measured drain voltage compared to the simulation.

Other errors between the theoretical expectations and measurements can be attributed to inaccurate modelling. For example, the higher amplitude oscillations of the real drain voltage, which are more prevalent when ZDS is not achieved, are most probably due to an underestimation of the stray inductance of the GS66504B packaging. The spikes during transition of the LTspice input gate voltage are a simulation phenomenon caused by the switching of different turn-on and turn-off resistance values. In addition, as shown in Fig. 12, the behaviour of the simulation model of the GS66504B is not in complete agreement with its datasheet. However, the most important limitation of the simulation method is that the behaviour of the passive elements in the inverter can be more accurately approached to capture a larger range of frequencies if a more complex network of passive elements is used to model them. A demonstration of this fact is shown in the existence of higher frequency harmonics of the Tx current

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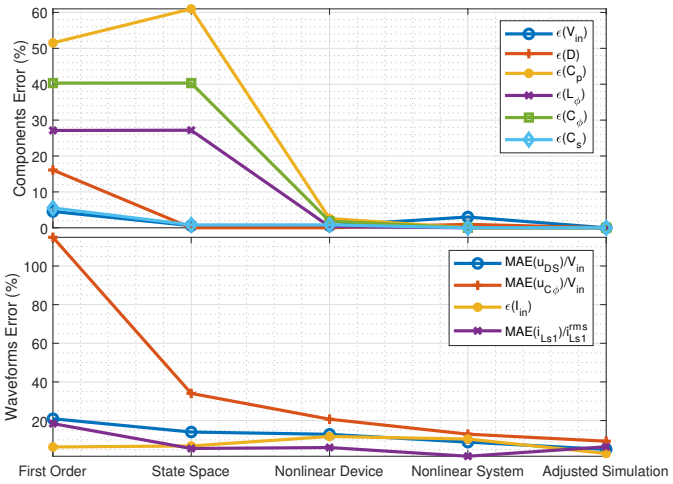
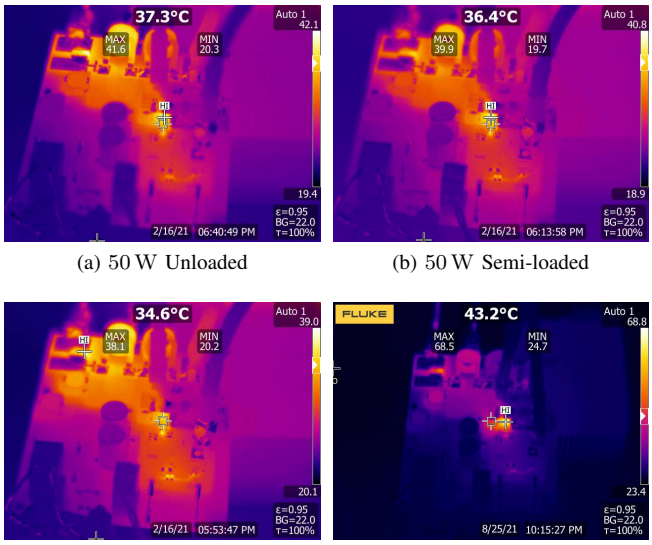


Fig. 25. Progressions of error metrics regarding the component values and the waveforms fitting between the tuning algorithm stages and the experimental data. The percent error (ϵ) is based on the absolute change and the fitting metrics of the waveforms are normalised using experimental data. For the case of the input current we used the DC values of the waveforms, to filter out the noise of current probe measurements.



(a) 50 W Unloaded (b) 50 W Semi-loaded

(c) 50 W Fully loaded (d) 150 W Fully loaded

Fig. 26. Thermal image of the inverter board during operation using the infrared camera for four different loading and powering scenarios. As we deviate from the optimal operating point (c), the thermal stresses on the components rise. The safe thermal limit of the design with the given passive cooling solution is shown in (d).

present in Fig. 24, compared to Fig. 20. Although this modelling complexity can be easily incorporated to our proposed simulation method so that the tuning of the inverter does compensate for the resonant effects of the passive components, it increases the computational requirements disproportionately to the advantages it offers. This is further supported by the practically insignificant level of deviation between the waveforms of Fig. 18 and Fig. 23 which show the primary voltages and currents in the circuit.

The tracking of the progression of specific error metrics with regards to the experimental measurements as the algorithm transitions between its various stages is displayed in Fig. 25. The normalised deviation between the component values and waveforms at each stage of the algorithm compared to the final experimental values, is shown. Since the DC component of u_{DS} and u_{C_ϕ} is set by V_{in}, we normalise the mean absolute error (MAE) of these waveforms accordingly, which represents the average of the absolute difference between the actual and predicted values in the data set [72]. The MAE of $i_{L_{s_1}}$ is normalised using its measured RMS value. The rest of the absolute error metrics are normalised using the corresponding experimental measurement.

Overall, for our Class EF_2 example, we observe that stopping the design procedure at the FO stage produces component values that are between $5\,\%$ and $50\,\%$ away from the true experimental values. After the final part of the algorithm, the component errors have been eliminated and the accuracy of the waveform simulations has been improved two to twelve times, depending on the case. Furthermore, the limitations of the first order modelling due to boundary definition in Fig. 3 is reflected to the fitting error of u_{C_ϕ} in Fig. 25, and the accurate predictions of u_{C_ϕ} are crucial for reflected load estimation techniques [73]. It must be noted that the computational penalty for achieving these results is insignificant compared to the benefits, since the total computation only takes a couple of minutes to run on an Intel Xeon E5-2630 v3 CPU using Matlab R2020b.

As mentioned before and verified by Fig. 25, the FO stage is only used to provide an initial estimation to be used as starting point for the iterative tuning schemes that follow, and none of the component values that are derived from this stage remains unaltered as the algorithm progresses. The SS stage contributes mainly to the adjustment of V_{in}, D and C_s, whereas the third step corrects the ϕ and shunt networks. The last part of the algorithm acts as a final fine tuning stage, which in our case turned out to be unnecessary because of precise selection of passive components and low parasitics of the device.

B. Verification through Implicit Measurements

We use the spectrum analyser feature of the MSO58 to generate the graphs in Fig. 24. The magnitude, i.e. the vertical axes, can only be measured in dBm, assuming a $50\,\Omega$ impedance, which makes the data in Fig. 24 useful only in a qualitative way. For the near field measurements of the magnetic field created by the inductive link we use the $25\,\mathrm{mm}$ Aaronia RF Near Field Probe. Both measurements show the filtering effect of the second harmonic on the output of the inverter, and agree with the simulated model in Fig. 20. Since the effect of the ϕ-branch is tested indirectly, we conduct two different kinds of measurements to avoid any room for error.

The thermal performance of the inverter is shown in Fig. 26 across a variety of operating conditions. The images were captured after the inverter was running long enough to achieve steady state temperature with no active cooling. The components that tend to be stressed the most, according to Fig. 26, are in agreement with the power distribution predicted in Fig. 20. The small form factor of the transistor makes its thermal

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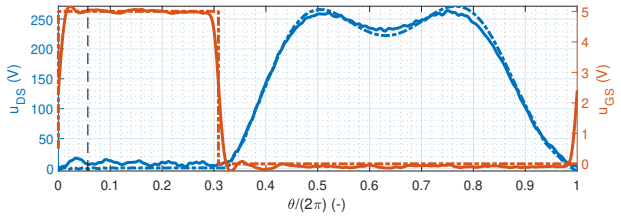

Fig. 27. Drain voltage and gate signal from experimental measurement (solid line) and LTspice simulation (dashed line) for Class EF_2 inverter with the maximum input voltage that the given thermal dissipation setup allows for safe operation. The duty cycle is manually adjusted to avoid reverse conduction and decrease the power consumption of the switching device , with the dashed black line representing the turn-on time point of the non-adjusted duty cycle.

dissipation challenging and this is reflected in the measurements. The inductor in the ϕ-branch also is a significant cause of loss because of its finite Q factor. The final component that undergoes significant heating is the series load capacitor, because of the high output current, as shown in Fig. 18. In Fig. 20 the ohmic losses of the capacitors are included in the corresponding series inductances, so high temperatures of C_s were expected.

Since the design procedure is defined so that the inverter is optimised for a single operating point, we expect maximum efficiency to be achieved when the full load is connected, which is confirmed from Fig. 26c. As the distance between the two coils increases, decreasing the coupling, the efficiency starts to drop and temperatures rise. The worst case scenario is when the Tx coil is completely decoupled from the load, which is confirmed in Fig. 26a. For this reason, the power consumption of the freewheeling inverter in Table VI is higher than the expected losses in the board when running under full load. Combined with the Tx Q factor correction in Table VI, the theoretical efficiency statement in Table V holds. However, these temperature deviations are very subtle and the inverter can in practise operate safely across the full range of possible couplings.

The inverter is supposed to be capable of operating not only among a range of coupling factors but also with various power levels supplied. The descending nature of C_{oss} while the drain voltage increases (Fig. 12) and its direct correlation with the effective value of C_p, combined with the fact that efficiency-wise, reverse conduction is a much more preferable operation condition compared to hard switching, makes the optimal input voltage the lower bound of supplied power level. The upper limit of V_{in}, for the given thermal solution used in our experimental setup, is also given in Table VI, which corresponds to three times the optimal power. A comparative presentation of the u_{DS} and u_{GS} waveforms from measurement and LTspice simulation is given in Fig. 27, and the accuracy of the simulation method and measurements is confirmed again. The thermal image of the inverter for this operation instance is shown in Fig. 26d, where now the switching device clearly becomes the limiting factor. It should be noted that by increasing the input voltage from the optimal value, with the optimal load connected, the device starts reverse conducting, and thus the overall efficiency drops

TABLE VII
INPUTS, OUTPUTS AND MEASUREMENTS OF THE LOAD INDEPENDENT CLASS EF INVERTER EXAMPLE

	Quantity	Value	Unit
Inputs*	τ_ϕ	1.7	–
	λ	4	–
	i_S^{ON}	−4	A
Outputs	V_{in}	57.33	V
	D	34.82	%
	C_p	65.252	pF
	L_ϕ	320.01	nH
	C_ϕ	147.521	pF
	C_s	126.79	pF
Measurements*	P_{in}	50.19	W
	R_{in}	65.487	Ω

*Including the data of previous relevant Tables.

because of increased conduction losses. We compensate for this effect by increasing the duty cycle manually, until ZVS is achieved.

VIII. CONCLUSION

A detailed and thorough description and application of a novel proposed algorithm, along with the underlying mathematical expressions, is presented for designing Class EF/Φ inverters. The algorithm can easily be implemented in computer code and offer an automated solution for determining the component values of the circuit with high accuracy. All design equations and calculation details are provided in order to make this work completely reproducible.

The design procedure offers to the user the ability to determine a variety of operating parameters (loading factor, ϕ-branch frequency, drain current at turn-off), according to the requirements of the application. The algorithm is general and covers both finite and infinite choke topologies. The proposed method is divided into four subroutines, where each consecutive one offers higher accuracy compared to the subsequent one, and can be terminated after any of these four stages, depending on the level of detail of available measurements.

The algorithm is then applied to design a Class EF/Φ inverter and the experimental results match the simulation without the requirement of manual retuning. This example includes the effects of both linear networks for simulating passive components as well as non-linear semicoductor modelling. The level of accuracy achieved from this work is demonstrated and verified with experiments. Having the level of control that this algorithm provides over the behaviour of HF resonant systems, as in the case of HF-WPT applications, can enable us to confidently define the safe operation limits of the system, which is also demonstrated experimentally.

APPENDIX

In order to further showcase the capabilities of our proposed design method, we apply it to the load independent Class EF inverter introduced in [10]. We use the same inductive link, load, power level and transistor as in the main body of this paper, however the circuit design inputs are completely

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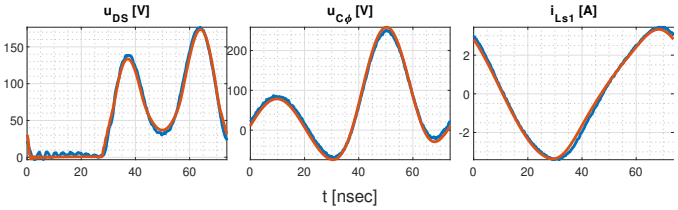

Fig. 28. Simulated (orange) and measured(blue) waveforms of the voltage across the drain and the ϕ capacitor and output current of the load independent Class EF inverter example.

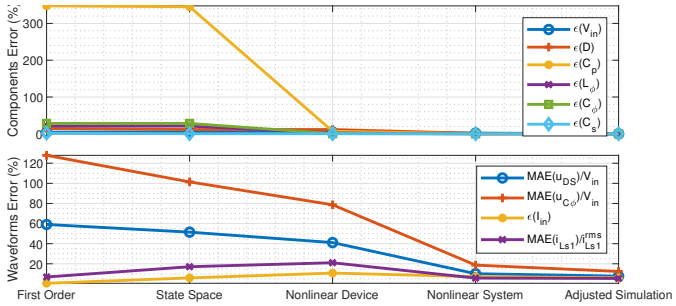

Fig. 29. Progression errors of the tuning algorithm in correspondence to Fig. 25 for the load independent Class EF example.

different to the Class EF_2 example, as can be confirmed from Table VII. This way a direct comparison between the two can be made, since the application remained the same.

The final component values of the experimental setup as well as measurements are given in Table VII and Fig. 28. The level of agreement between experimental and simulated waveforms in Fig. 28 again confirms the high accuracy of our tuning method. The change in simulation accuracy when comparing the first step of the algorithm to the last can exceed $120\,\%$ and component values can be off by more than $300\,\%$. The output capacitance from Fig. 12 of the device at input voltage for our two experimental examples is quite similar, however the change in C_p in Fig. 25 and Fig. 29 is different by seven-fold. This observation confirms that the widely accepted technique in the literature of using the mean of the drain voltage to calculate the effective output capacitance of the device is oversimplified and unreliable. Interestingly, after the efficiency maximisation during the fourth step of our algorithm, the final design was slightly hard switching, as can be seen in Fig. 28, which although being seemingly unusual agrees with the definition of "optimal operation" in [17]. Indeed, slight hard switching, reduces device stresses and increases power capability, which is even more effective in non ZDS conditions.

The THD of the Class EF_2 example is below $1\,\%$, whereas on the load independent one is $9\,\%$. This is visually noticeable from the output current waveforms in Fig. 23 and Fig. 28 and is a consequence of the ϕ branch resonant frequency of the two instances. Although the load independent design has significantly larger duty cycle than the EF_2, the latter has over $40\,\%$ higher power capability, assuming equal output power. Notwithstanding that precise efficiency measurements on an AC load can be challenging at MHz frequencies, since the two setups share the same link, we can calculate their efficiency ratio using only input power and output current measurements. The Class EF_2 example is $16\,\%$ more efficient overall. By combining the simulated ϕ branch current and the corresponding Q factor, the losses on L_ϕ on the load independent example are roughly three times higher than its counterpart. Lastly, the device temperature on the EF_2 is half of that on the load independent.

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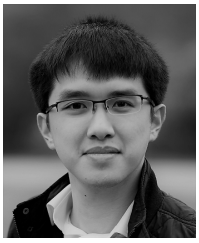

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