Title: Printed Synaptic Transistors based Electronic Skin for Robots to Feel and Learn

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Abstract: Electronic skin for the next-generation of robots is expected to have biological skin-like multimodal sensing, signal encoding and pre-processing. To this end, it is imperative to have high-quality, uniformly responding electronic devices distributed over large areas and capable of delivering synaptic behaviour with long- and short-term memory. Herein, we present a transformative approach to realise synaptic transistors (12×14 array) using ZnO nanowires printed on flexible substrate with 100% yield and high uniformity. The presented devices show synaptic behaviour under pulse stimuli, exhibiting excitatory (inhibitory) post-synaptic current spiking rate dependency plasticity, and short-term to long-term memory transition. The as-realised transistors demonstrate excellent bio-like synaptic behaviour and show great potential for in-hardware learning. This is demonstrated through a prototype computational e-Skin, comprising of event-driven sensors, synaptic transistors, and spiking neurons, bestowing biological skin-like haptic sensations to a robotic hand. With associative learning, the presented computational e-Skin could gradually acquire the human body like pain reflex. The learnt behaviour could be strengthened through practice. Such a peripheral nervous system–like localised learning could substantially reduce the data latency and decrease the cognitive load on the robotic platform.

One-Sentence Summary: E-Skin mimics the neural pathway for tactile signal processing, bestowing skin-like haptic sensations to robots.

Main Text:
INTRODUCTION

Skin, the largest organ in the human body, comprises thousands of receptors, distributed over ~18 sq. ft area, playing a critical role in the way we interact with the environment (1-3). It efficiently handles a large amount of tactile sensing data from all over the body and has served as the inspiration for artificial e-Skin (3-5). As a result, the e-Skin research has greatly advanced in recent years (6-8). However, existing implementations of e-Skins may not be sufficient as the large amount of tactile data, acquired from the skin, needs to be encoded, transmitted, and pre-processed too – similar to biological skin (9-11). It is challenging to fully emulate such functionalities owing to difficulties in terms of realising uniformly responding electronic devices, especially synaptic devices, over large-area flexible/stretchable substrates (11-16). Currently, memristor and synaptic transistor are the two promising candidates for the hardware-implemented synaptic devices (17-20). However, the fabrication complexity and notable device-to-device and cycle-to-cycle non-uniformity of memristors (such as form, set and reset voltage), especially in a crossbar array configuration, make it challenging to use them on large-area flexible substrates. Likewise, most of the currently reported work on synaptic transistor focus on a small number of devices (21-24), with almost no statistical information on the yield, uniformity, large-area weight modulation ratio, etc. Without such knowledge, the higher-level design and implementation of a synaptic transistor-based neuromorphic system are hardly possible either for online or offline learning (25-28).

Considering the surface coverage and the softness of the biological skin, large-area fabrication of electronic devices on the flexible/stretchable substrates is needed. To this end,

printed electronics has opened the avenue which could meet these requirements in a cost-effective manner (29-34). Specifically, the printed semiconducting metal-oxide nanowires (NWs) are promising candidates for the computational e-Skin because of their high aspect ratio, unique electrical/optoelectrical properties, good mechanical flexibility, and compatibility with various printing technologies (35-37). However, one critical but universal challenge in printed electronics is the trade-off between spatial coverage and device uniformity - both of which are vital for robotic e-Skin. This problem is more challenging for NWs based devices (i.e., transistors), as precise dimensional control and placement is difficult (38, 39).

Herein, we present a holistic approach for realising highly uniform (synaptic) transistors based on printed ZnO NWs for computational e-Skin. The arrays are composed of 168 devices with 100% yield, showing high DC response uniformity that surpasses (or is on par with) the state-of-the-art devices based on ZnO (Si) NW fabricated using expensive technology such as electron-beam lithography (EBL) (38, 39). The as-realised devices show a synaptic behaviour like the biological synapse, i.e., conductance modulation based on the previous operation history, spiking-rate dependency, and short-term to long-term plasticity transition. With the previously demonstrated biocompatibility in ZnO NW (40), the work presented here may also be promising for future integration with the biological systems.

The bio-mimicking synaptic behaviour opens interesting avenue for the in-hardware learning. To illustrate this, a computational e-Skin prototype, composed of sensory neuron, synapse and cuneate neuron, has been realised (See Figs. 1a and 1b). The prototype fully maps the functionality of tactile neural pathway in the human body for the data encoding, transmitting, and processing; the neuron used in the pathway converts the input signal into action potentials (spikes) following biological principles, i.e., all-or-none rule, spatiotemporal summation, etc. Thanks to the bio-plausibility of the as-realised system (synapses and neurons), the demonstrated e-Skin shows the capability of associative learning and the further strengthening behaviour by practising, all from the in-skin hardware. This advances the previous work in e-Skin (or artificial tactile pathway) by the demonstration of in-hardware associative learning and rehearsal behaviour (19, 41, 42). The large-area computational e-Skin requires tactile neural pathways to cover the full body with a "many-to-many" neural connection. Such a hyperconnected network could enable a far more complicated learning behaviour and built-in intelligence while substantially decreasing the data latency. To this end, the hardware implementation of large-area distributed sensing and computing requires the as-realised synaptic transistor to have a good synaptic behaviour, e.g., enough on/off ratio, good spatial uniformity, etc. This is important given that previous studies have indicated that a lack of these properties could lead to a drastic decrease of the neural network accuracy (25-28). To clarify this, a neural network simulation has also been carried out with the data from the hardware implemented synaptic devices, showing an average recognition rate of ~93% based on the MNIST dataset. This is close to the full software approach (97%) and validates the potential of using the as-presented synaptic devices to realise large-scale neural network.

We believe, our work paves the way for the future realisation of large-area, computational e-Skin, and can be of interest to a broad range of readers working on neurorobotics, neuroprosthetics, smart wearables, healthcare monitoring, and printed/flexible electronics.
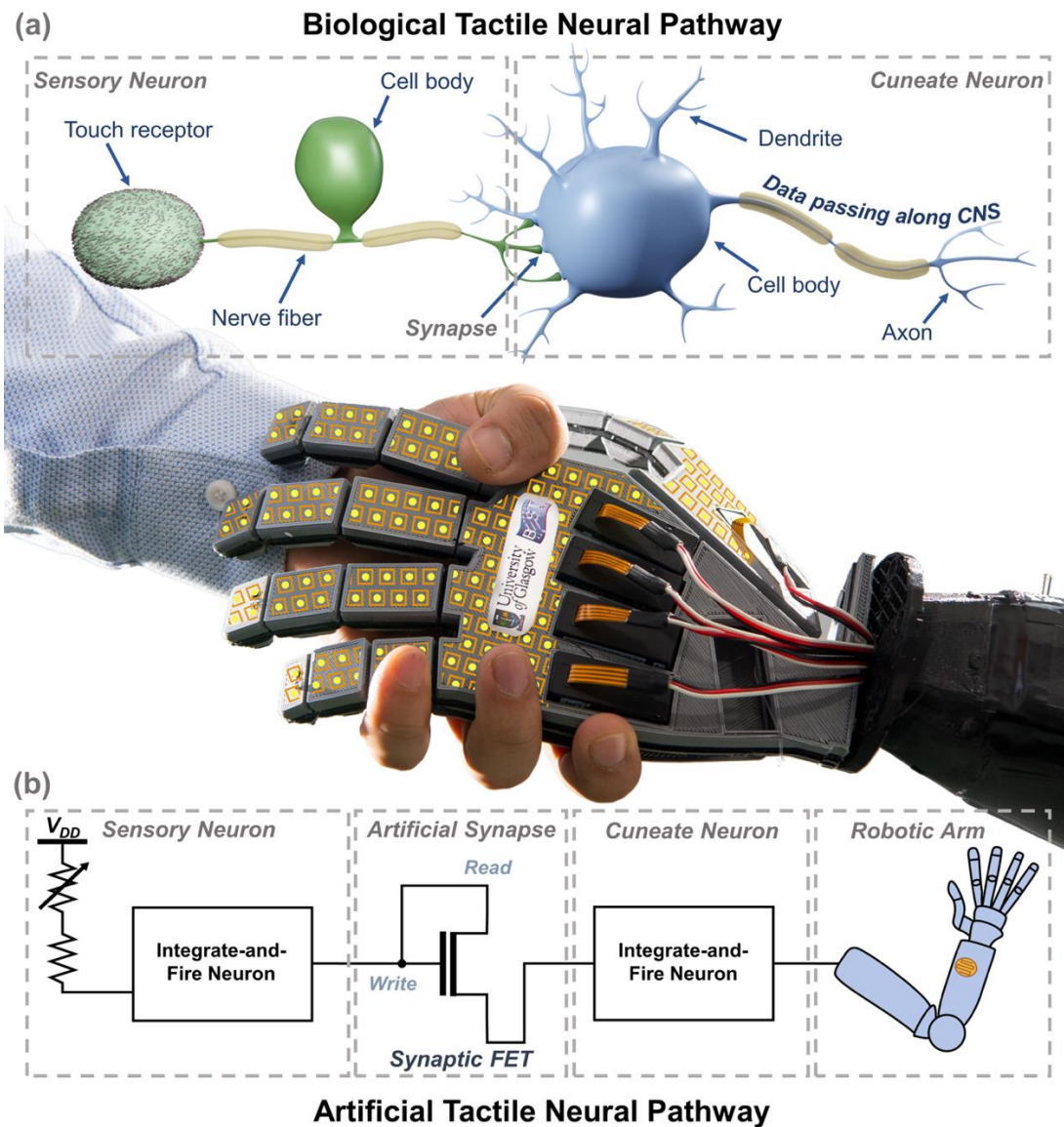
Fig. 1. The biological and artificial tactile neural pathway. (a) The biological tactile neural pathway. (b) The artificial tactile neural pathway. The connection for the artificial neural pathway is for illustration purpose only. The detailed connection is explained in Figure 5a.

RESULTS

To fully mimic the peripheral nervous system (PNS) in the human body, hardware building blocks that can function as receptors, synapses, and neurons, over a large area are prerequisites. The work presented here mainly focuses on synapses and thereafter hardware-enabled, localised learning behaviour. The neuron is realised from the off-the-shelf components (see Supporting Video 1).

HARDWARE IMPLEMENTATION OF SYNAPTIC TRANSISTORS

The bottom-gated transistors are realised by contact printing ZnO NWs from its donor to the receiver substrate, followed by photolithography, metallisation, and lift-off to define the source/drain electrodes. The receiver substrate (Si with 300 nm SiO_2) can be either a bare

wafer (so that it leads to rigid devices) or spin-coated polyimide (PI) layer (~2 µm thick). After device fabrication, the spin-on PI can be peeled off from its carrier, leading to flexible devices (see Figs. S1 to S3 and Methods).
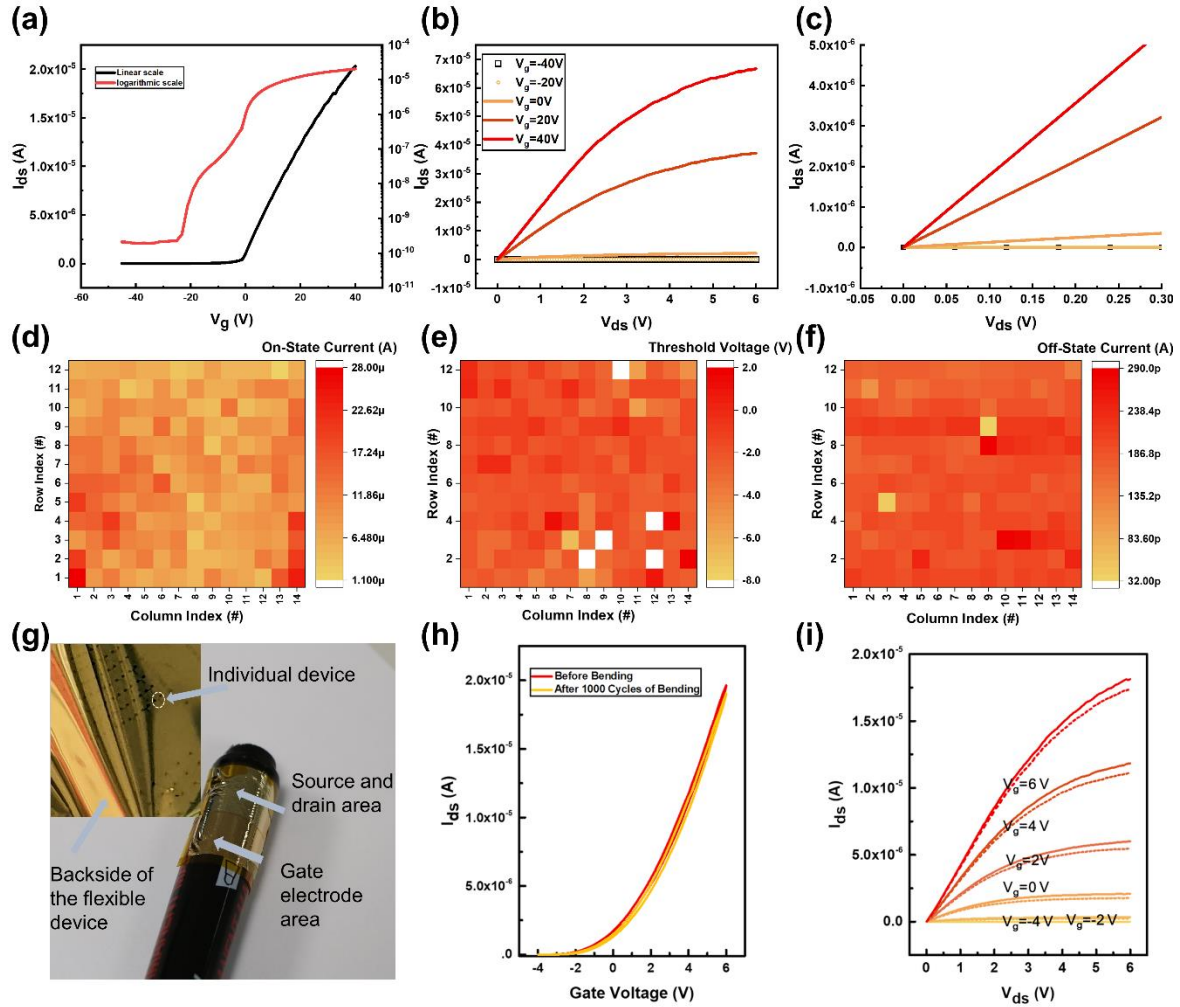

Fig. 2. The DC test of the transistors. (a) The transfer characteristics at a V_{ds} of 1V. The channel length and width of the device are 10 and 220 µm, respectively. (b) and (c) The output characteristics at a high and low drain-to-source bias, respectively. (d), (e) and (f) The spatial distribution of the on-state current, threshold voltage and off-state current from the transistor matrix, respectively. (g) The photograph showing the flexibility of the devices realised on PI. (h) and (i) The transfer and output characteristics before and after the bending test. The transfer characteristics was measured at a V_{ds} of 6V. The figures 2a to 2f are from tested rigid devices to prevent any probing induced extrinsic factors; The figures 2g to 2i are from flexible device, showing that the same method can be applied to realise a flexible device matrix.

The devices realised based on the printed NWs show a 100% device yield, an ohmic output behaviour (see Figs. 2a, 2b, 2c) with a clear saturation at a bias voltage V_{ds} of 5 V, and a good spatial uniformity for several important device metrics such as on-state current (Fig. 2d), off-state current (Fig. 2f), on-off ratio, and threshold voltage (Fig. 2e). In general, achieving a good spatial uniformity for NW based devices is more challenging when compared to devices based on thin-film or 2D materials. This is owing to the difficulties related to good control over the material dimensions and registrations (see Supporting Information, Section 1) (38, 39, 43, 44). In view of these challenges, the results presented here mark substantial advances as they surpass or are on par with the state-of-the-art top-

gated FETs with an excellent control over diameter and registration (see Table S1). Furthermore, our approach is compatible with the flexible substrate, which holds great promise for applications such as large-area computational e-Skin for robotics, smart wearables, health monitoring, and prosthetics. The field-effect mobility of the ZnO based FET is estimated to be ~ 55 $cm^2/V \times s$. The device performance from the as-realised flexible device is robust against various mechanical bending states with almost no performance variation (Fig. S4), which is a crucial prerequisite for the application in flexible electronics. This is different from the previous reports, as the bending of the device would lead to noticeable performance variation (45). We also tested the cyclic bending performance of the ZnO NW based FETs for 1000 cycles (at the bending radius of ~20 mm) and no notable variation in transfer and output characteristics was observed (Figs. 2h and 2i). This, along with negligible shift of threshold voltage (from -2.3 V to -2.1 V), confirms excellent stability upon mechanical deformations (see Fig. S4). The excellent DC behaviour of the as-realised ZnO NW FETs holds great promise for realising functional circuits, e.g., the neuron circuit required in the later study.

The transistors we presented here well-emulate the function of biological synapse: with positive (negative) pulse stimuli at the gate terminal, the drain-to-source current decreases (increases) because of the field-effect. After the stimuli, the current does not go back to the original state immediately. Instead, it goes to a lower (higher) level and gradually returns to the former conductance in a quasi-exponential manner, exhibiting an inhibitory (excitatory) synaptic behaviour (see Figs. 3a and 3b). In the biological system, the information is passed between the neurons by emitting conductive ions (e.g., Na^+, Ca^{2+}, Cl^-) known as neurotransmitters. Under its influence, the neuron becomes depolarised (excitatory) or hyperpolarised (inhibitory) from its resting state, and gradually recovers. Similarly, the observed synaptic behaviour from the presented device is attributed to the movement and trapping/detrapping of the charge carriers to those surface states under the external gate voltage bias: at the resting state (Fig. 3c, t<0), the occupied surface states density and the charge carrier density in the channel are in the equilibrium condition; once the gate voltage increases (decreases) (Fig. 3c, t=0), the electron density in the channel also increases (decreases). This breaks the previous equilibrium condition, leading to more electrons trapped at the surface states (more trapped electrons escaping from the surface states). After the gate voltage returns to the resting level (Fig. 3c, t>0), the carrier density in the channel becomes lower (higher) than the previous resting state level owing to a higher (lower) surface states occupancy; the unbalanced surface states occupancy gradually returns to the equilibrium condition by discharging electrons to the channel (charging electrons from the channel), leading to an inhibitory (excitatory) post-synaptic behaviour (Fig. 3c, t>>0). This explanation is supported by a control experiment: after a conformable deposition of high-quality top-gate dielectric (Al_2O_3) by ALD, the synaptic behaviour vanishes (Fig. S5), confirming the synaptic behaviour is originated from the surface states from the ZnO NWs rather than bottom gate dielectric. The amplitude of the synaptic behaviour is dependent on the base carrier density in the channel: a higher carrier density would lead to a more prominent synaptic behaviour for both excitatory and inhibitory cases (Figs. 3d and 3e).
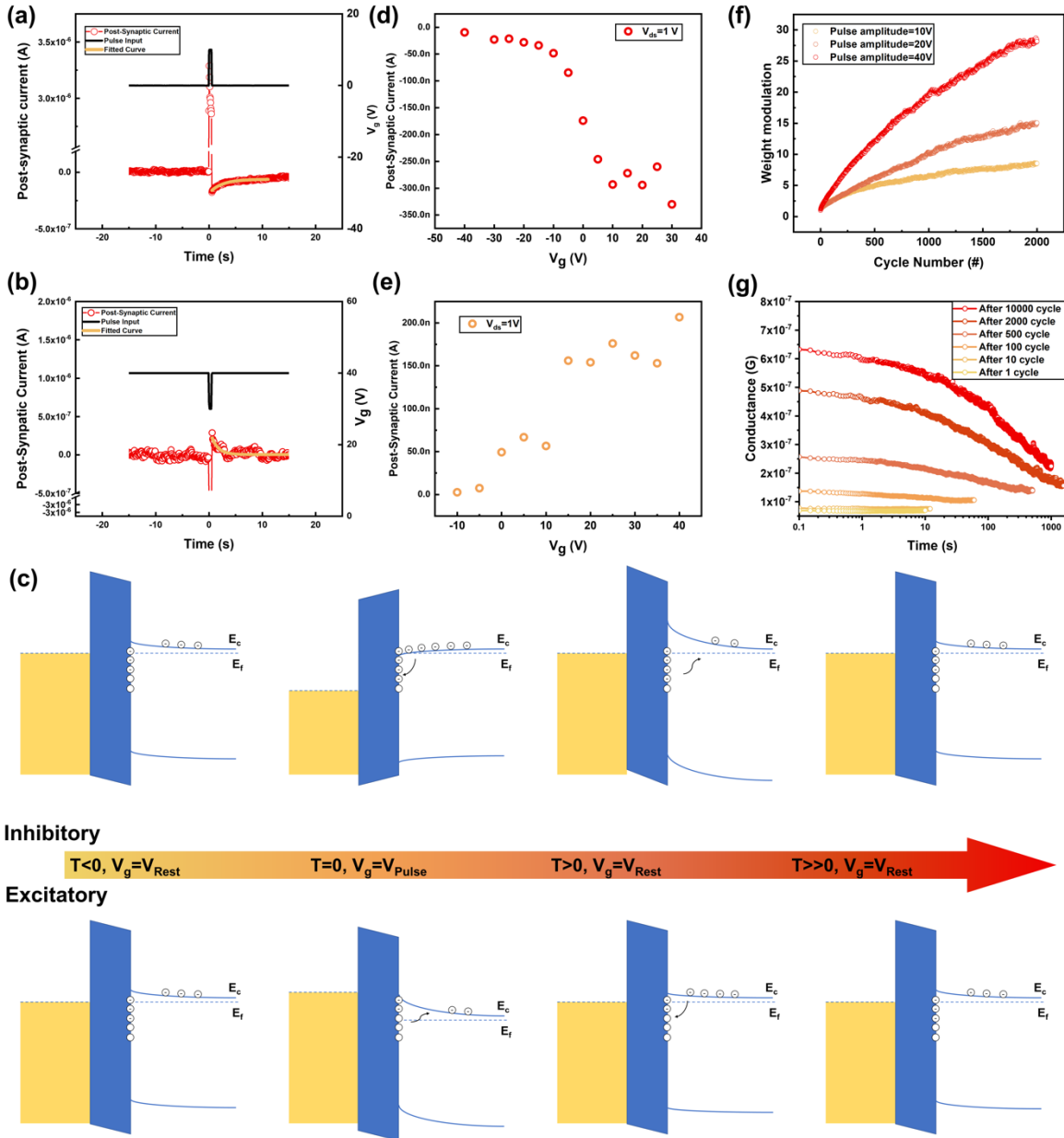
Fig. 3. The synaptic behaviour of the ZnO NW based transistor. (a) and (b) The inhibitory and excitatory post-synaptic current (IPSC and EPSC) realised in transistor. (c) The band diagram explaining the origin of the synaptic behaviour. (d) and (e) The dependence between the value of the post-synaptic current and the gate voltage at the resting state. (f) The change of modulation ratio of the conductance with respect to the number of the pulses applied to the device. The pulse width is~300 ms and the interval time between two neighbouring stimuli is~100 ms. (g) The recovery behaviour of the synaptic device after certain numbers of pulse stimuli, showing a transition between short-term memory to long-term memory with increased number of input pulses.

It is believed that in the biological system, the increase in the amplitude and/or the frequency of applied stimuli can strengthen the synaptic behaviour along with the transformation of short-term memory (STM) to long-term memory (LTM) through rehearsal (46, 47). Similar behaviour has been observed in our device: A change in synaptic weight from 58.3 nS to 1.64 µS (~2800%) (Fig. 3f, red curve) was observed owing to an increase in both the

amplitude and the number of the pulse stimuli. After training, the conductance of the synaptic device gradually recovers to the previous state, representing the natural forgetting process. Nevertheless, with repeated stimuli or rehearsal, the retention time increases from several seconds to several minutes, which indicates a transformation from STM to LTM (Fig. 3g). We also tested the frequency dependency of synaptic behaviour. The increase of pulse number and pulse frequency increases the synaptic behaviour, which is a good analog of the biological behaviour of paired-pulse facilitation (depression) and spiking-rate dependent plasticity (SRDP) (see Figs. S6 and S7). Overall, the as-presented device shows a good similarity to the biological synapse, which opens the possibility for the development of the bio-inspired neuromorphic system as discussed in the following section.

TACTILE NEURAL PATHWAY CAPABLE OF IN-SKIN LEARNING

Skin, distributed with thousands of receptors, could efficiently collect, transmit and pre-process the tactile data in real-time, yet maintain an ultra-low power consumption. This far surpasses most state-of-the-art robotics. Furthermore, human exhibits great adaptability, accommodating to the ever-changing environment based on the previous experience (e.g., learning). In this regard, the biological skin offers a fascinating solution for sensation and perception and acts as an excellent model for reverse engineering. Herein, we present a computational e-Skin prototype that fully mimics the biological, tactile neural pathway.
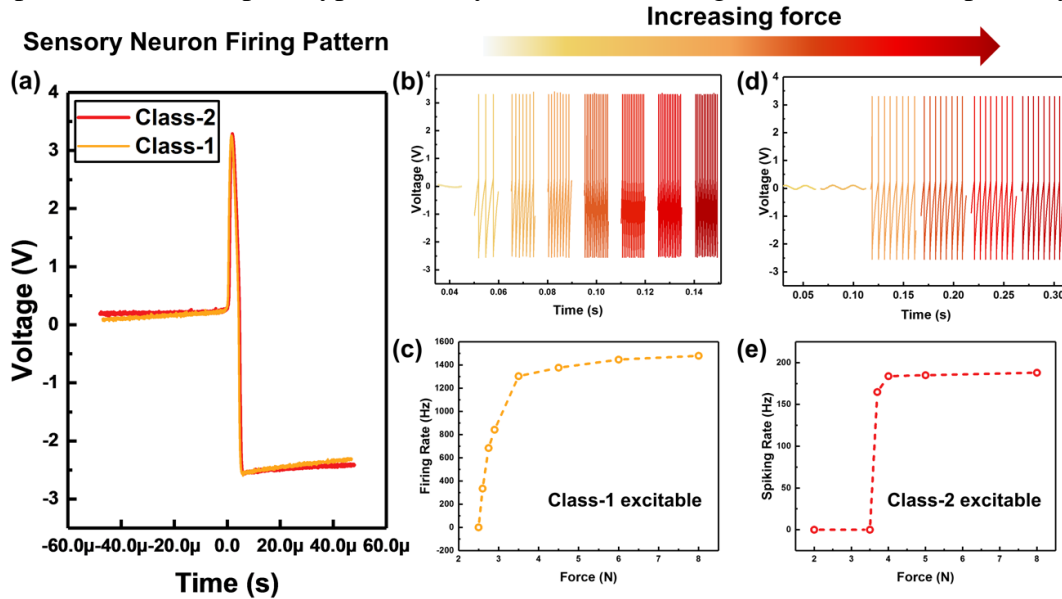

Fig. 4. The firing pattern of the sensory neuron. (a) The single spike from the sensory neuron. (b) and (c) The change of the firing rate with respect to the applied force for the class-1 excitable neuron. (d) and (e) The change of the firing rate with respect to the applied force for the class-2 excitable neuron.

Just like its biological counterpart (Fig. 1a), the artificial neural pathway consists of a (layer of) sensory neuron(s) and a (layer of) cuneate neuron(s), interconnected via synapse (Fig. 1b). The analogue tactile signal is thus transduced into spikes in the first layer and further processed in the second layer. An "integrate-and-fire" neuron circuit like the one proposed in ref. (48) has been adopted to realise the functionality of the spiking neuron (see Fig. S8). With respect to the arrangement of the sensory neuron, a resistive sensor (force sensitive resistor, FSR) is serially connected with a fixed value resistor, acting as a viable load to the neuron circuit as shown in Fig. 1b. Unlike previous approaches (19, 49), this layout offers a more bioplausible spiking pattern which contains the depolarisation and hyperpolarisation stage (Fig. 4a), crucial for the later realisation of "bio-like" learning in the e-Skin. The output spiking pattern from the sensory neuron can be tuned by the value of the built-in

resistor. For example, using the FSR with a 1 MΩ (or lower) resistor, the sensory neuron circuit exhibits a class-1 excitable behaviour (50), that is, the firing rate positively related to the applied stimuli (Figs. 4b and 4c). Meanwhile, the FSR connected with a resistor of 10 MΩ (or higher) would lead to a class-2 excitable behaviour (spiking rate independent with the incoming stimuli if it is higher than the threshold (50) (Fig. 4d and 4e). It should be noted that both designs offer event-driven sensing, drastically reducing the latency of the tactile data which needs to be fed into the neural pathway. In this work, we adopt the latter design to act as the artificial nociceptor and further use it to emulate the pain reflex observed in biology.

Fig. 5. The demonstration of the artificial tactile neural pathway capable of "in-skin" learning. (a) The detailed operation scheme for the tactile neural pathway (b) The spiking signal used for the writing stage. (c) Without a teacher signal, the computational e-Skin cannot learn, so that it does not respond to applied force. (d) With a teacher signal, the computational e-Skin can realise localised learning. The threshold shown in the figure is for illustration purpose only. (e) The firing pattern of the cuneate neuron (second-order neuron) before and after associative learning, with the applied force on the sensor. (f) The photos showing the acquired pain reflex after associative learning right on the skin level.

Hardware implemented neural system opens the possibility of realising "bio-like" learning behaviour. In the biological neural system, the synaptic weight is determined by a pair of pre- and post- neuron spiking signals, i.e., spiking-time dependent plasticity (STDP) and burst-time dependent plasticity (51, 52). A pair of synchronised spikes changes the synaptic weight according to their relative timing and thus leads to the learning behaviour. By contrast, a standalone incoming signal should not affect the synaptic weight much, as in this scenario, the pre- and post- spiking signal is regarded as highly unsynchronised. In biological view, this opens the room for the neural system to react only to those conditions they are supposed to or trained to. In the presented artificial neural pathway, this is demonstrated by the presented synaptic device along with the spiking neuron circuit capable of delivering the highly bio-plausible action potentials. The synaptic device passes the spiking signal to the next level (read) as well as changes its own weight under the pre- and post- spiking pair (write); each pressing of the sensor should cover at least one write and one read process (Fig. 5a). The switching of the read and write could be achieved in various manners, for example, by using a global clock signal. In this regard, a clock of 1000 Hz should be enough for tactile sensing as the average tactile reaction time observed in the human body is ~ 200 ms (53), 200 times longer than a clock cycle. The detailed connections of each node of the synaptic transistor (for the read and write modes) are summarised in Fig. 5a. It should also be noted that to achieve more effective training, the sensory signal used in the write mode is amplified by ~4 times (Fig. 5b). This could be potentially avoided by using a four times thinner dielectric from the synaptic transistor; thus, the amplitude of the sensory spiking could stay the same for both modes.

The untrained scenario of the tactile neural pathway is shown in Fig. 5c. With only the sensory spiking, the weight of the synaptic device remains almost the same, thus the second-order neuron stays silent. This is owing to the use of the biological spiking patterns from the sensory neuron: As discussed in Figs. 3a and 3b, the positive (negative) electrical stimulus leads to an inhibitory (excitatory) behaviour to the synaptic device; the co-existence of the electrical stimulus in both direction within one pulse would then open the room for the synaptic weight to stay unchanged. In this scenario, the synaptic device cannot be trained by a single pulse from the sensory neuron, as a pre-spiking signal alone leads to no post-spiking signal under a low-weight synaptic connection, and this failure of excitation remains in loop. From a functionality point of view, this represents an unconfigured computational e-Skin, like those patients who suffer from hypoesthesia and partially lost their somatosensation, which stops them from responding to certain types of stimuli (e.g., pain) in a certain part of their body, because of the loss of the previous synaptic weight.

Clinically, those patients may regain the sensation by passive sensory training using peripheral electrical stimulation, which externally modulates the synaptic plasticity. Despite the optimal stimulation frequency and waveform for this purpose are still ambiguous, it is generally accepted that a longer electrical stimulation leads to stronger plasticity modulation

(54). Similarly, the presented computational e-Skin could be configured to react to certain behaviour through a teacher signal to evoke the second-order neuron's firing through associative learning. The required teacher signal was employed right at the time of the touch (see Fig. 5b), which excites the second-order neuron and trained the synapse. As shown in Fig. 5d, the weight of the synaptic transistor was facilitated to ~50 nA after the associative learning, and such an effect was not disturbed by the stimulation of the sensors (Fig. 5d). Owing to the excitatory of the synapse, the second-order neuron receives a stronger input that is larger than its firing threshold, thus changing from the non-firing to the firing condition (Fig. 5e). Furthermore, just like the clinical observation, the longer the teacher-sensory signal pair was applied, the stronger the associated learning would become (see Supporting Videos 2 and 3 and Fig. S9 showing STM and LTM after associative learning). After teaching, the learnt behaviour is strengthened/retained if it is practised regularly so that the pre-neuron spiking would evoke a post-neuron spiking and such a synchronised spiking pair could rehearse the associated behaviour on time (See Fig. S10 and Supporting Video 4). After training, the second-order neuron fires an action potential whenever there is an over-threshold stimulus on the sensor in the neural pathway; by contrast, without training (or without pressing), the second-order neuron remains in the subthreshold oscillation (or off-state) (Fig. 5e). Such in-skin learning is attractive as this could drastically reduce the data latency and minimise the cognitive load of the central control unit of the robot. This is especially important for tactile sensing as large number of tactile receptors (mechano, thermal, pain) distributed all over the skin and it is challenging to carry large-scale tactile data from PNS to central nervous system (CNS). The methodology presented here mimics the biological process in tactile sensation and perception, where the tactile information is locally pre-processed in PNS before transferring (9, 10), complementing the functionality of the CNS. In the work presented here, the neural signal from the tactile pathway was fed into a robotic arm (from Universal Robots). After associative learning, the robotic hand acquires the pain reflex, like the one possessed by the human body (see Fig. 5f and Supporting Videos 1 and 5). Compared to the previous demonstration of the artificial tactile pathway (19, 41, 42), the work presented here fully mimics the neurological principles, thus showing the capability of localised learning directly on the hardware level.

TOWARDS LARGE-AREA, MULTIFUNCITONAL E-SKIN
Skin contains many multimodal sensors, with different threshold and receptive fields. Along with the associated neurons and synapses, it forms a large-area neural system covering the whole body. It is necessary to extend the above-presented "one-to-one" biological neuron pathway into a "many-to-many", multilayer neural network capable of doing cognitive tasks using various methods including supervised, unsupervised and reinforcement learning (see Fig. S11 along with the detailed discussion in the Supporting Information, Section 8). One critical step towards this is the realisation of large-area synaptic devices. In practice, hardware-implemented synapses have several limitations such as finite weight modulation ratio with discrete values, spatial non-uniformity, and the device yield problem. Although the neural network is naturally resilient to some of these limitations, studies have shown that a high weight modulation range for the synapse with decent uniformity is necessary to obtain a good network accuracy (25-28). This has posed the requirement for the hardware-implemented synaptic devices. Herein, as a step towards the large-area, computational e-Skin, we systematically evaluated the synaptic behaviour from the transistors. For all the devices, a series of 100 excitatory pulses has been used and the conductance was measured. The as-realised devices show a good weight modulation ratio (>500%) for most of the devices (>80%) with fine modulation steps, which is beneficial for the neuromorphic system realization (25-28) (Figs. 6a, 6b, 6c and 6f). The conductance of the synaptic devices with respect to the input pulse cycle is presented in Figs. 6a to 6c; 100% of the as-realised devices

show the synaptic behaviour with a cell-to-cell variation (σ/μ) of ~96% and ~133% at the 100th and 0th cycle, respectively (Fig. 6d), larger than the non-uniformity in the DC response. To further verify the applicability of the as-realised devices for neuromorphic computing, we used the weight data from the realised synaptic devices to simulate a 3-layer, feedforward neural network. Based on the spatial (14×12 devices) and temporal (0 to 100 cycles) weight distribution from 168 devices, we have extrapolated to obtain a dataset of 101771 groups (101 discrete weight value for each group) by assuming both datasets following the same distribution (see Figs. 6d, 6f, 6g, 6h, S12 and S13). The weights constructed "hardware library" and trained to recognise handwritten digits by using the MNIST dataset (Fig. 6i). Such a strategy enables us to evaluate the quality of synaptic behaviour from the all devices instead of a single device. For comparison, we also simulated the full analogy weights to represent the software approach. The neural network simulation has been repeated 10 times and the average accuracy is presented here. As can be seen in Fig. 6j, the recognition accuracy based on the hardware simulation is ~93% at the 6th epoch, which is only 4% less than the software-based simulation. This indicates a good synaptic performance from the transistors and hence a good indication for using it to realise large-scale neural network. By contrast, with a decreased weight modulation ratio or high non-uniformity from the synapses, the constructed neural networks were shown to have a notably lower recognition accuracy (27).

Experimental Synaptic behaviour over a large area
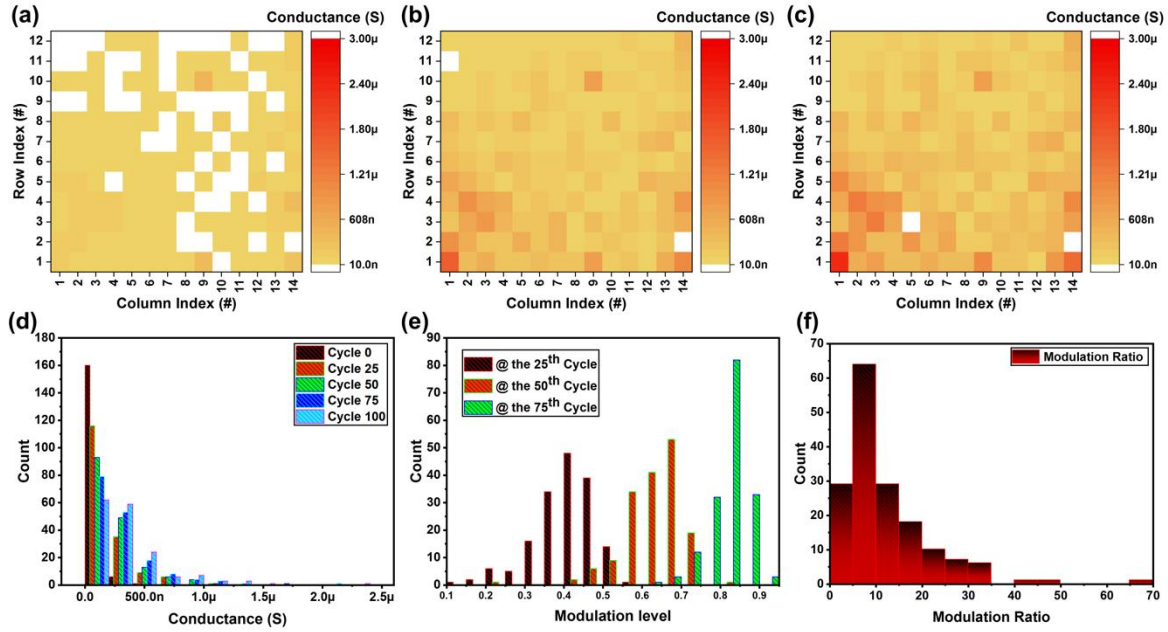
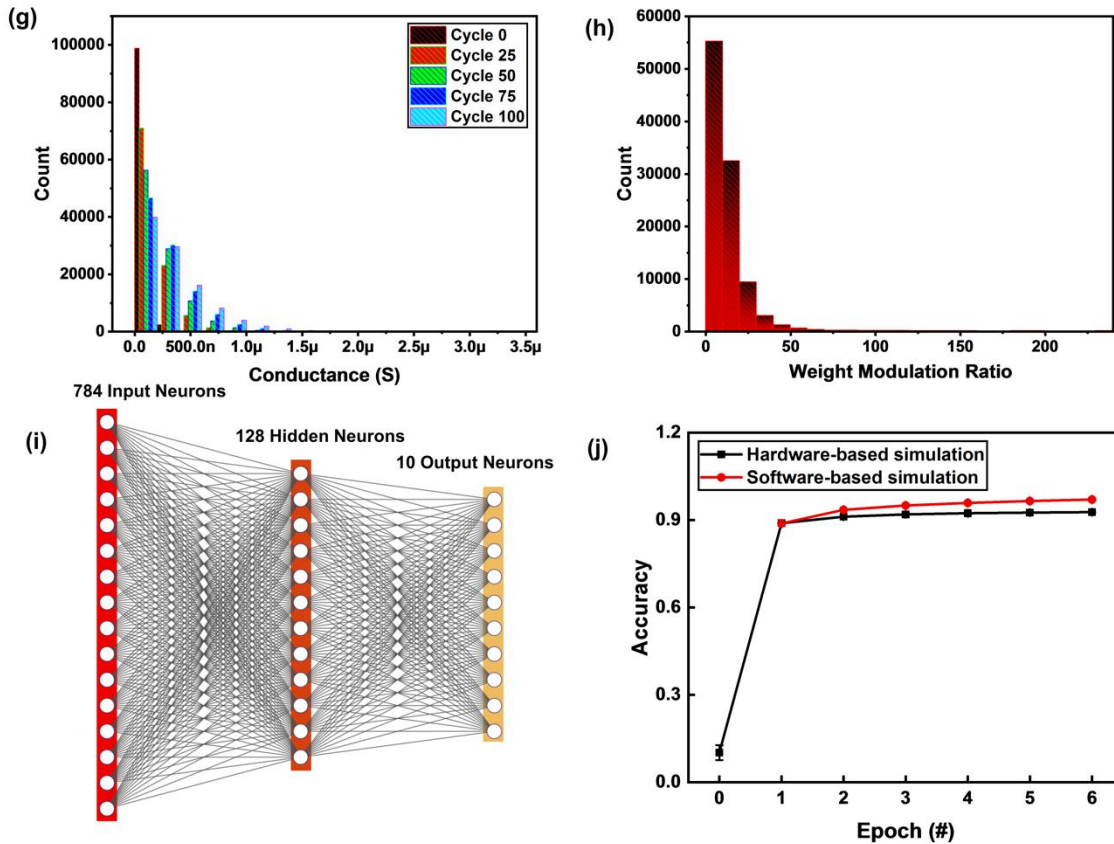# Simulated Synaptic behaviour for classification task

Fig. 6. The large-area synaptic responses and the neural network simulation. (a), (b) and (c) The spatial distribution of the conductance of the pixel at the 0th, 50th and 100th cycle, respectively. (d), (e) and (f) The distribution of the conductance, modulation level and modulation ratio, respectively. The modulation level at the ith cycle is defined as $(Gi-G0)/(G100-G0)$. (g) and (h) The distribution of the conductance and weight modulation level from the extrapolated hardware dataset. The dataset comprises of 101771 group of conductance information. Within each

group, the conductance level is changed from cycle 0 to cycle 100. (i) The three-layer feedforward type neural network trained for the handwritten digits classification. The training was done using MNIST dataset. (j) The comparison between the software-based training and hardware-based training.

DISCUSSION

We have realised large-area, uniform, printed synaptic transistors and further use them to realise computational e-Skin. The e-Skin mimics the biological tactile neural pathway and offers an in-skin computing (learning) capability. Such a distributed learning through hardware holds great potential for the next-generation robots, as it will drastically decrease the cognitive load on their central control units. Notably, there are also several limitations from the work presented here: only the synaptic transistor in the neural pathway is realised on the flexible substrate. Also, in the computational e-Skin prototype, we demonstrated an "one-to-one" neuron control with learning capability. Further extending this work towards all-printed, flexible artificial neural pathway in a "many-to-many" neural network fashion would enable a fully flexible e-Skin with much higher built-in intelligence. Nevertheless, we believe this work, as the first step, paves the way for the future realisation of large-area, multifunctional, and fully printed computational e-Skin.

MATERIALS AND METHODS

Nanowire Synthesis: The ZnO NW was synthesised by chemical vapour transport method using a tube furnace. Before synthesis, the substrate (Si) was treated by Poly-L-lysine solution 0.1 % (w/v) in H_2O for 20 s, followed by Au nanoparticle (diameter of 80 nm) suspension treatment for 40 s. The substrate was then rinsed with RO (Reverse osmosis) water and cleaned by a mild oxygen plasma (80 W) for 200 s. The Si substrate with Au nanoparticles was then loaded into the furnace for ZnO NW synthesis with a mixture of 0.5 g Zn O powder and 0.5 g graphite powder as the source material. The placement of the substrate with respect to the source can be found in the supporting information. Notably, such placement has been found to offer a good spatial uniformity. The synthesis was carried out at 880°C for 2 hrs with the Ar acting as the carrier gas of ~1500 sccm.

Receiver substrate preparation: Si substrate with 300 nm thermally oxide layer was used as the rigid substrate. Before NW printing, the substrate was deposited with 70 nm SiNx for surface passivation with ICP 380 from Oxford Instrument. The flexible receiver substrate was prepared by spin-coating PI layer on top of the Si (with 300 nm oxide layer) carrier wafer. The PI was spin-coated at 500 rpm for 5 s and 2000 rpm for 60 s. The spin-coating was carried out twice, with a 140°C soft-baking of 5 mins between each coating. The sample was ready for use after a full curing at 250°C for 2 hrs. After all the fabrication process, the PI layer can be peeled off from the carrier wafer, leading to a flexible film with as-realised devices.

Contact printing: The contact printing process was carried out using an automated, home-made setup (55). The setup can deliver a close-loop control of the printing process in terms of the contact pressure, sliding speed, sliding stroke, etc. The conformable contact was guaranteed by a specifically designed self-levelling system. The printing process has been monitored by two micro-cameras from two perpendicular directions. The printing process together with the automated setup has been explained in our publication (55).

Device fabrication: After printing, the sample was baked at a hotplate at 160°C ~180°C for 5 mins. Without such a baking process, the NW would be substantially disturbed in the following lithography process due to the weak van der Waals contact between the NWs and the underlying substrate. The sample was then spin-coated with LOR10A at 6000 rpm for 30 s, baked at 150°C for 2 mins, then spin-coated with S1818 at 4000rpm for 30 s and baked at 115°C for 3 mins. The exposure was carried out by Mask Aligner 6 for a duration of 6 s. The sample was then developed in MF319 for 85 s, followed by metal deposition (8 nm Ti and 50 nm Au) and lift-off. The lift-off process was carried out in MICROPOSIT remover 1165 for 30 mins under the 50°C water bath. Such a long-time water bath could effectively remove most of the printed NWs, unless they are buried under the source and drain contacts.

Device measurement: The device was measured in the ambient condition with the semiconductor measurement unit B1912 from Keysight. Due to the resolution of our measurement system for the pulse test, we kept a constant white light excitation for all the devices to see the synaptic behaviour. The devices are measured all together at the same condition to minimise those non-uniform extrinsic factors. For synaptic measurement, pulse voltage signals with positive and negative polarities were applied to gate terminal and drain-to-source current was measured keeping the drain voltage constant. The drain-to-source current measured after pulse signal is referred as post-synaptic current.

Statistical analysis: The statistical analysis performed in the manuscript, including the distribution identification, normality test, random data generation, was carried out using Minitab or MATLAB.

Neuron circuit implementation: The neuron circuit was implemented by using two CMOS dual complementary pair ICs (CD4007). Its circuit diagram was shown in the supporting information.

Robot Experiment: A Nucleo board was used to sample and detect the spiking signal. Whenever a continuous spiking signal is detected, a control command was sent to trigger the UR5 arm. The threshold needs to be chosen properly so that on one hand, it would not be triggered by any noise signal; on the other hand, it should lead to a prompt reaction. The GPIO pin was left on high for 50 ms to ensure detection by the UR5 arm.

Neural Network Simulation: We evaluated the uniformity of the hardware synaptic behaviour in the framework of supervised learning in neural network. The 3-layer feedforward neural network was trained using the Tensorflow library for Python 3.7. The training was carried out with the loss function of "Sparse Categorical Crossentropy" and the activation function of hyperbolic tangent function (Tanh). For hardware-based simulation, the initial weight of the entire neural network is assigned to be the conductance data from the 0th cycle, but in a random manner. The computation of gradients was carried out by backpropagation method, but at the hardware constrain condition. This was mimicked by choosing the closest weights from the extended hardware dataset (Fig. 6g) at each epoch with respect to the software-training value and use this for further update. For simplicity, the hardware weights are all scaled by a factor of 10^6.

Supplementary Materials

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Acknowledgments:

Author contributions: F.L. and R.D. conceived the idea. F.L. and A.C. carried out the NW synthesis with the support from D.S.; A.C. performed the NW contact printing. F.L. fabricated the devices both on rigid and flexible substrate. F.L. and S.D. performed the DC and pulse measurement of the devices; M.S. simulated and implemented the neuron circuit. F.L. and M.S. realised the tactile neural pathway with the help from S.D.; M.C. realised the clock signal control of the system; R.C. carried out the robot control study and performed the neural network simulation; F.L. and R.D. wrote the paper, and all authors provided comments and agreed with the final form of the manuscript. R.D. provided the overall supervision of the work.

Competing interests: The authors declare that they have no conflict of interest.

Data and materials availability: All (other) data needed to evaluate the conclusions in the paper are present in the paper or the Supplementary Materials.

Printed Synaptic Transistors based Electronic Skin for Robots to Feel and Learn
(Supporting information)

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1. Large-area, uniform NW based device by contact printing approach
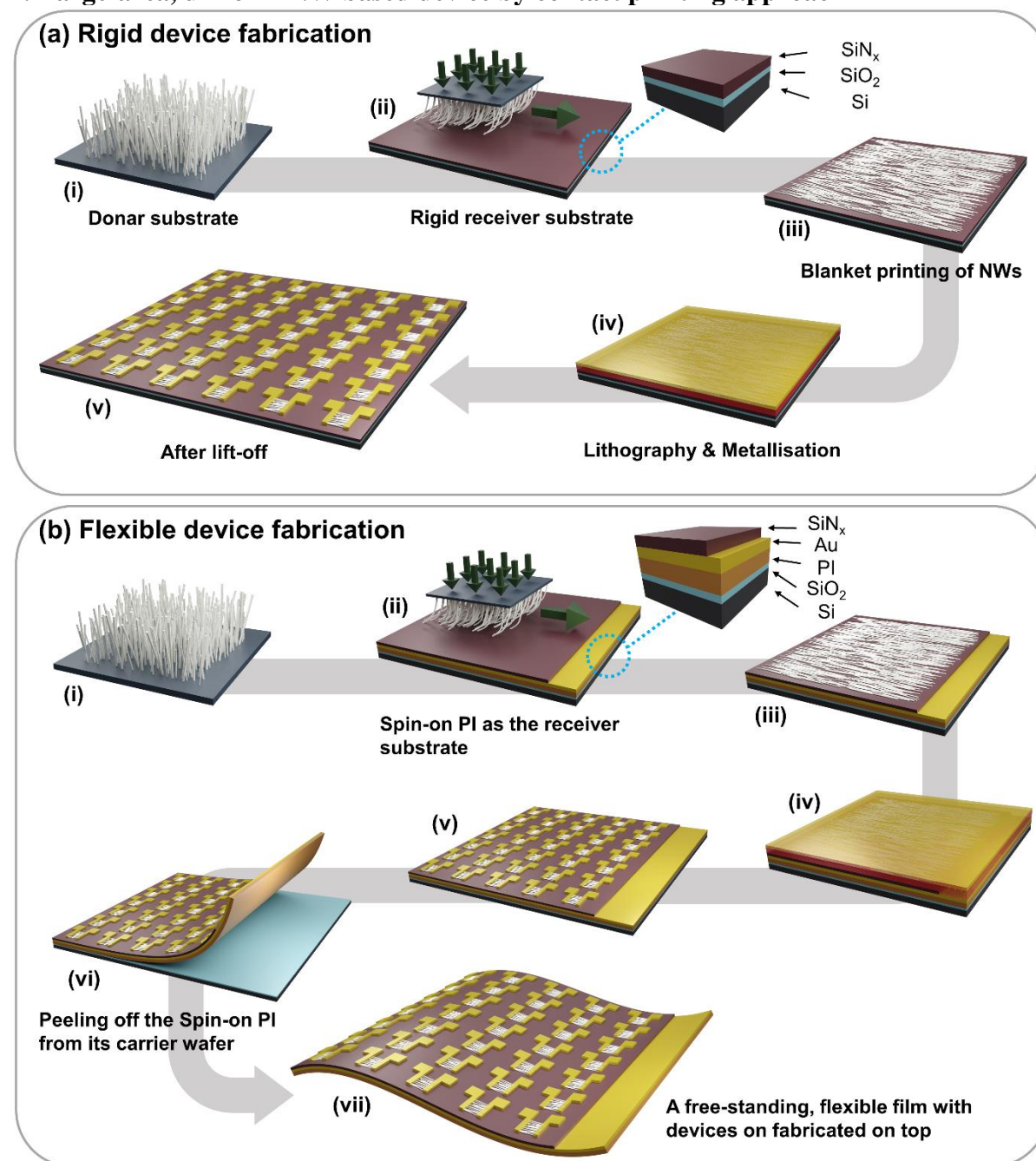
Figure S1: The detailed fabrication process flow. The fabrication processes for (a) rigid and (b) flexible devices.

The uniform, large-area flexible NW transistor matrix is achieved based on three important aspects, namely a) uniform ZnO NW synthesis with a controlled diameter on the donor substrate; b)

automated, highly controlled, planar-to-planar NW printing; and c) Ohmic contact formation and interface engineering under the thermal budget limit from the flexible, polymeric substrates.

a) For NW synthesis we have used the chemical vapour transport (CVT) method with Au nanoparticles as the catalyst. We chose the commercial Au nanoparticle dispersion (with well-defined diameter) and deposited them on the surface of the donor substrate (Si) for NW synthesis. The donor was then loaded into a tube furnace for the CVT process. We also noted that the placement of the donor substrate during the synthesis also plays an important role. For this, we explored several arrangements and the one shown in Fig. S2 gave the best outcome. The uniform colour in the middle region in photograph (Fig. S2b) indicates a uniform synthesis. In addition to NWs, it is also possible to have few ZnO flakes (Fig. S3c), which may bridge the source and drain electrodes and could lead to some non-uniformity among devices. To avoid this, we used the optimised pressure (10~15 kPa) during printing of NWs, which ensured low density and the size of the printed flakes, as can be seen in Fig. S3.
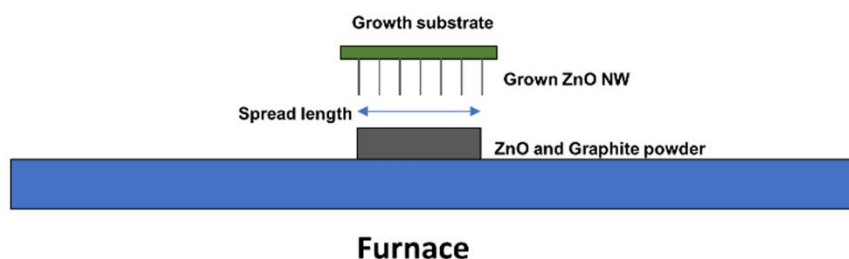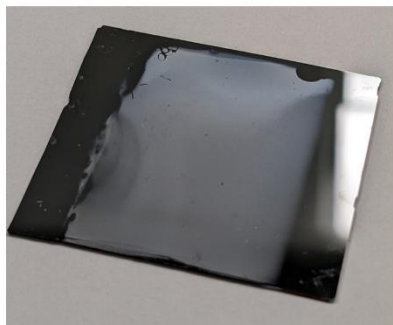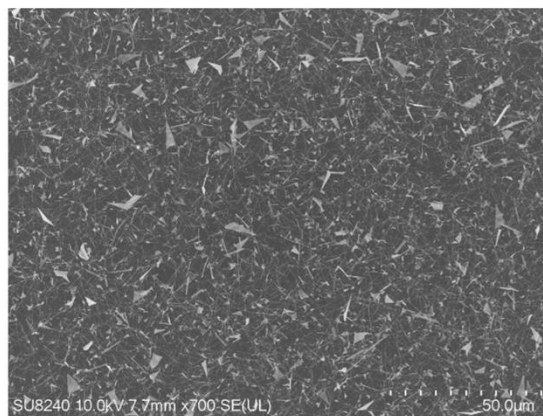
880degree 2hr
9.5cm spread length
ZnO 0.5g+Graphite 0.5g

Figure S2: The detail in ZnO NW synthesis. (a)The schema showing the ZnO NW synthesis condition. (b) A typical photograph showing the donor substrate with synthesised NWs. (c) Typical SEM images in central area.

b) The printing process and printing parameters (e.g., pressure, sliding distance, etc.) also play an important role for uniform device performance. For this, we developed an automated contact printing system (described in Ref. (55)) with self-alignment of the donor and receiver substrates.

The self-alignment system guarantees the conformable contact between the donor and the receiver substrates and minimises the spatial variation. The printing system utilises two high-resolution linear stages to control the movement of the donor and the receiver substrates. A load cell is used to monitor the pressure between the donor and the receiver substrates, and a close-loop control system is employed to maintain the pressure at the optimised pre-set value.
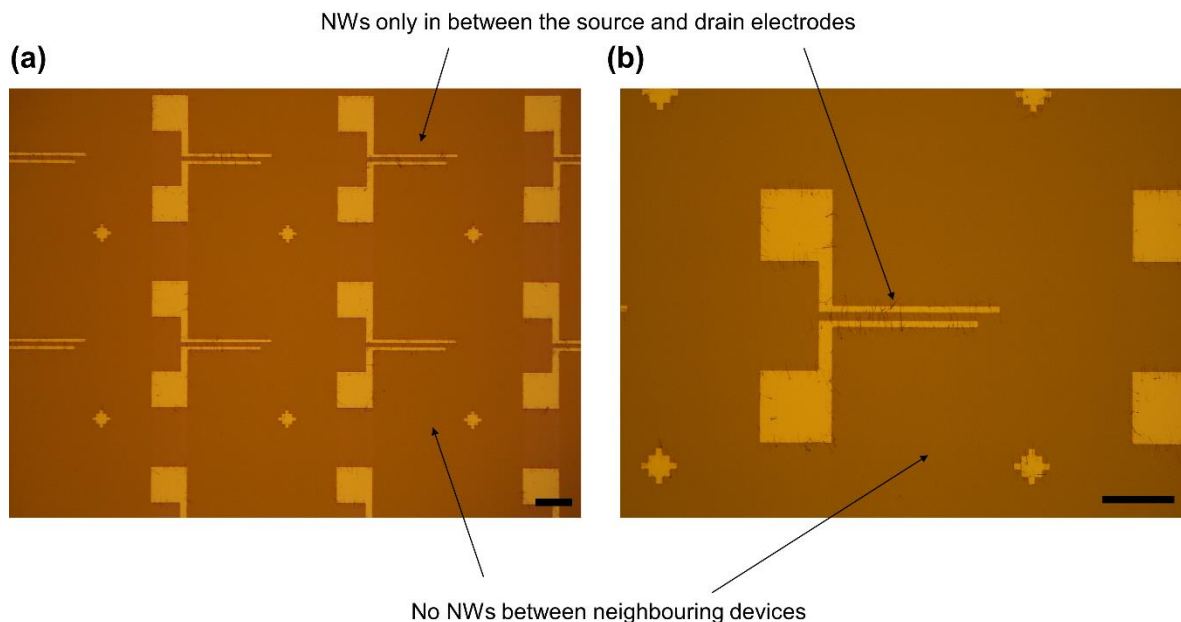

Figure S3: The optical microscopy images showing the fabricated devices. (a) and (b) The optical images of NW based devices under various magnifications. The scale bars in both images are 100 μm.

c) The device fabrication (source and drain electrodes deposition, the choice of dielectric) are also important. The key steps showing the NWs based printed electronic layers and their further processing leading to fabrication of devices are shown in Fig. S1 and the optical images of fabricated devices are shown in Fig. S3. It may be noted that the density, length, diameter of the nanowires is uniform within a certain area, owing to the control of the synthesis, and printing. Along with the key aspects mentioned below, it leads to high yield and uniformity of our devices. The key steps for device fabrication are:

1) The printing of NWs is a blanket printing (Fig. S1a (iii) or Fig. S1b (iii)). However, for large-area device fabrication, we do not want the excess NWs to stay in between the devices, as this may lead to unwanted interconnectivity. For this, we used a carefully optimised baking temperature of 160°C~180°C for 5 mins to moderately increase the NW-substrate adhesion after NW printing. This guarantees the NWs are stable enough in the lithography process (e.g., spin-coating, development). On the other hand, the NW-substrate adhesion should not be too strong to prevent the removal of excess NWs in the lift-off stage. One example is shown in Fig. S3. As can be seen, the NWs are only in between the source and drain electrodes. The lift-off was carried out by immersing the sample into MICROPOSIT Remover 1165 for around 30 mins at 50°C. No sonication was required.

2) We used the SiN_x as the nanowire-dielectric interface which is critical to achieve an ohmic contact and a narrow range of threshold voltage.

Above are all the technical aspects to realise a high yield and uniformity to the ZnO NW based transistors. Table S1 shows the uniformity comparison of the FETs based on 1D materials.

Table S1. Comparison of the uniformity in FETs based on 1D materials.

Material	Device architecture	Device number, yield	Uniformity in on state current	Uniformity in threshold voltage (V)	on/off ratio	Compatibility with flexible substrate	Synaptic behavior	Ref #
ZnO NW	Top gate	100, 85%	NA	-7.0 ± 1.5	50~700	No	NA	(38)
Si NW	Top gate	NA, <90%	P_{90}/ P_{10}~2.6[1]	1.7 ± 0.2	~10^4	NA	NA	(39)
CNT	Top gate	300, NA	100% in the range of 2.3-5.5 µA	-0.17±0.017	~10^5	NA	NA	(56)
CNT	Top gate	90, 100%	100% in the range of 46-189 µA	NA	~10^5	NA	NA	(57)
ZnO NW	Bottom gate	168, 100%	P_{90}/ P_{10}~2.8 (9.2±3.2 µA)	-1.8± 2.0	~10^5	Yes	Yes	This work

P_{90} and P_{10} denote the 90th and the 10th percentile, respectively.

2. ZnO NW based FET tested under various bending states
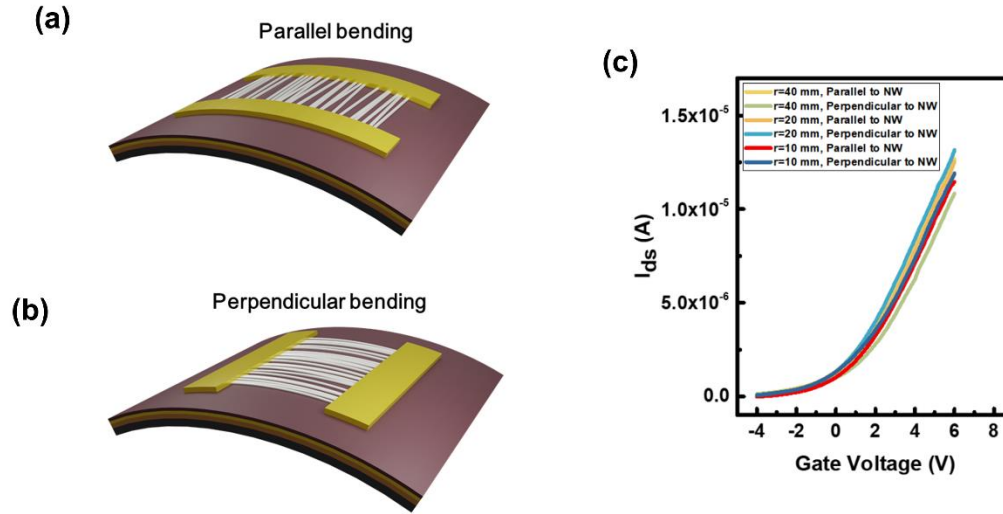

Figure S4: The flexibility test. (a) and (b) The schema showing the defination of parallel and perpendicular bending. (c) The transfer characteristics under various bending conditions.

As can be seen from the Fig. S4, the transfer characteristics of the device remain stable under various bending states. The threshold voltage, V_{th}, is extracted to be -2.5 V, -1.8 V, -2.2 V, -2.3 V, -2.1 V, -2.4 V, respectively, in the sequence shown in Fig. S4c (from top to bottom).

3. ZnO NW FET after depositing 40 nm Al_2O_3 by ALD

The Fig. S5 shows the transfer curves from two top-gated FETs after depositing 40 nm Al_2O_3 by ALD. As can be seen from the Figs. S5a and S5b, these two devices show a substantial threshold voltage shift. Such variation in threshold voltage and on-state current could be found all over the as-realised top-gate device matrix, which indicates that the non-uniform diameter in the device channel could result in notable device-to-device variation without the surface states induced "high-pass filter". The output of FET shows a good ohmic contact even without the bottom-gate dielectric passivation (Fig. S5c). The deposition of the top-gate dielectric would also lead to a loss of the synaptic behaviour, as shown in Figs. S5d and S5e.

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[1]P_{90} and P_{10} denote the percentile 90 and percentile 10 of the group of data, respectively. The data is extracted from the figure.
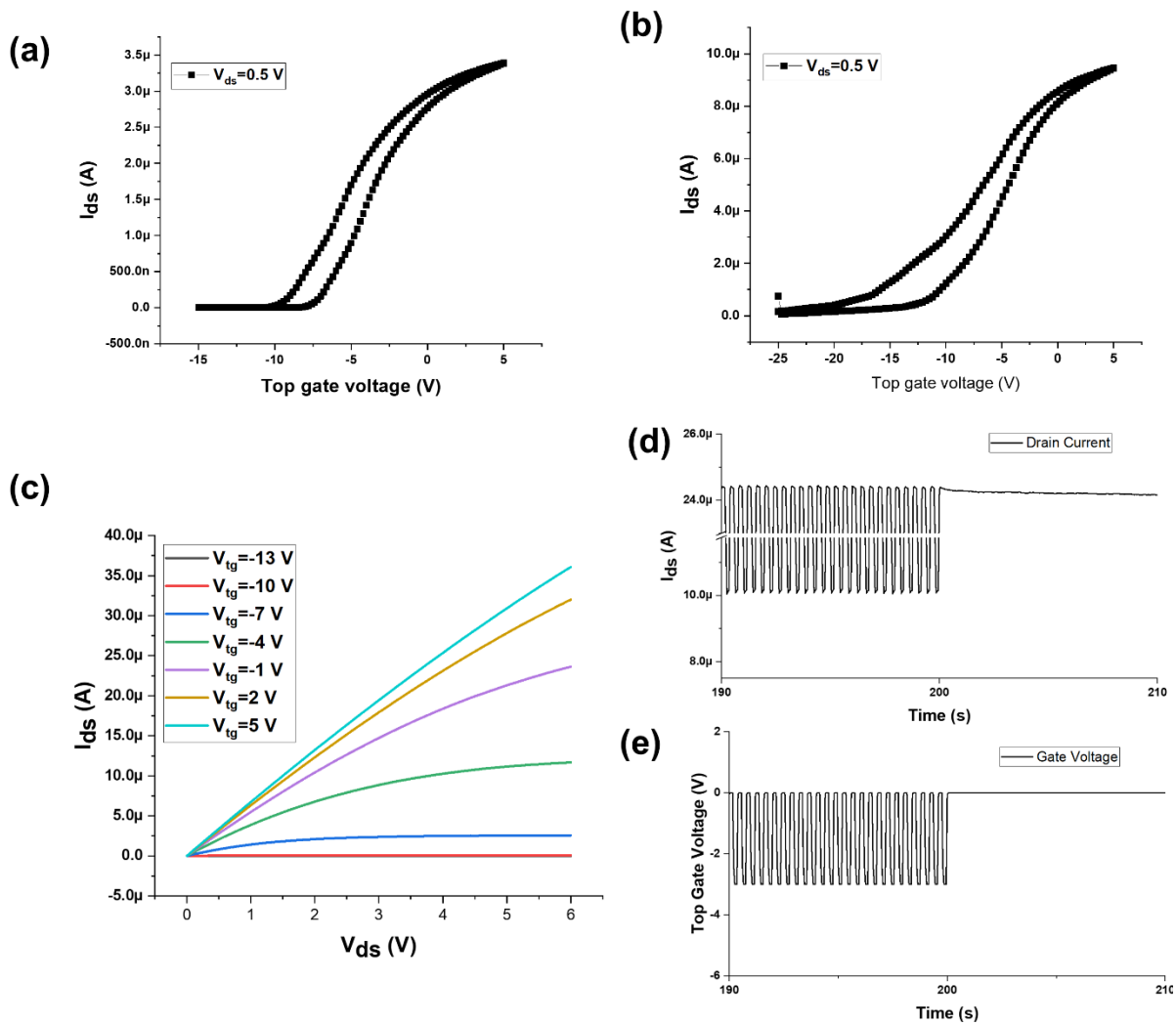
Figure S5: The top-gate device. (a) and (b) The transfer curves from two top-gated ZnO NW based FETs. (c) The output curves from the top-gated ZnO NW based FET without bottom gate dielectric passivation. The change of drain current (d) under a pulse gate voltage input, (e) showing that after depositing a layer of top-gate dielectric by ALD, the synaptic behaviour vanishes, confirming that the origin of the observed synaptic behaviour should be from the surface states.

4. PPD, PPF, SRDP of the synaptic device.
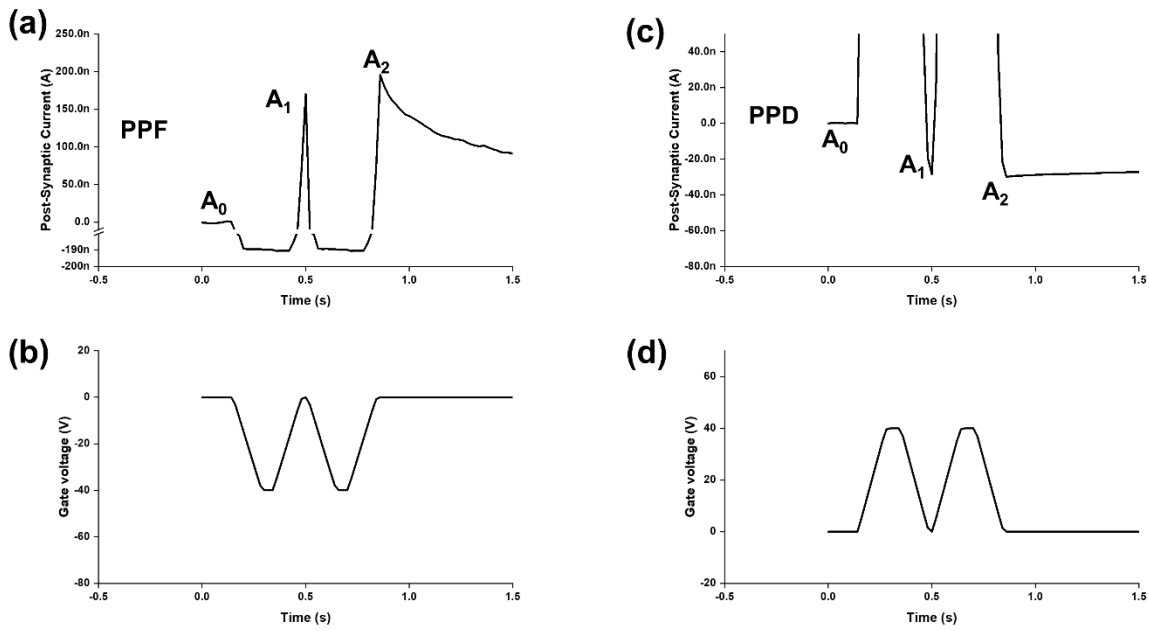
Figure S6: The PPF, PPD behaviour of the synaptic transistor. (a) and (b) The paired-pulse facilitation. (c) and (d) The paired-pulse depression.
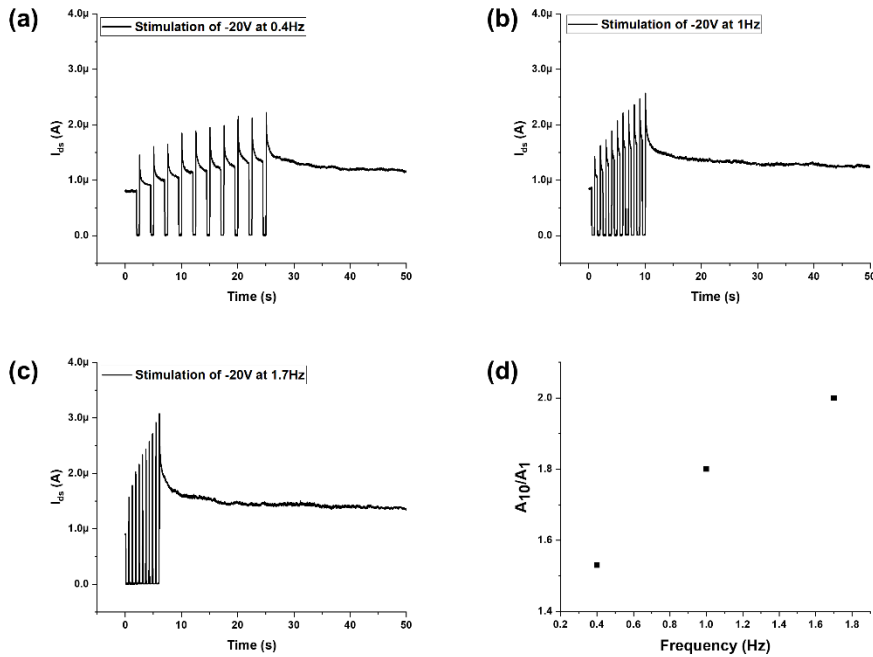

Figure S7: The modulation of the amplitude of the post-synpatic current vs pulse frequency (SRDP). (a), (b) and (c) show the device response for 10 cycles of consecutive pulse stimulation at a frequency of 0.4 Hz, 1.0 Hz and 1.7 Hz, respectively. (d) The frequency response of the synaptic device. The $A_{10}(A_1)$ indicates the amplitude of the post-synpatic current under at the 10th (1st) cycle of input pulse stimulus.

5. Neuron circuit diagram and simulation

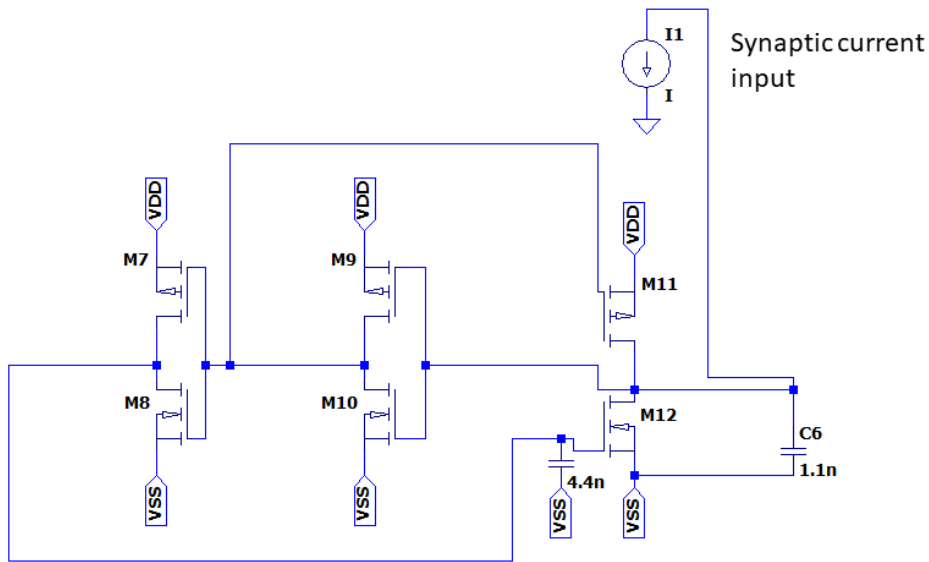The neuron circuit used in the work is shown in Fig. S8.

Figure S8: The circuit diagram of the neuron circuit.

6. The STM to LTM transition of the synaptic transistor when stimulated by the "Press-Teach" pulse pair

We have tested the synaptic behaviour of the transistor under various duration of the "press-teach spiking pair" as shown in Fig. S9. The durations of the stimulations were set to 2 s, 20 s, and 2 mins, respectively. As can be seen in the Figure S9, the longer the stimulation time for "press-teach spiking pair" is, the stronger is the synaptic behaviour. The conductance of the device gradually decays after stimulation is over. We fit the decaying behaviour with an exponential decaying function (*58*). The time constant is extracted to be ~16.7 s, 97.9 s, and 617.4 s, respectively. This indicates that with an increase of stimulation time, the synaptic behaviour from the device changes from short-term to long-term.
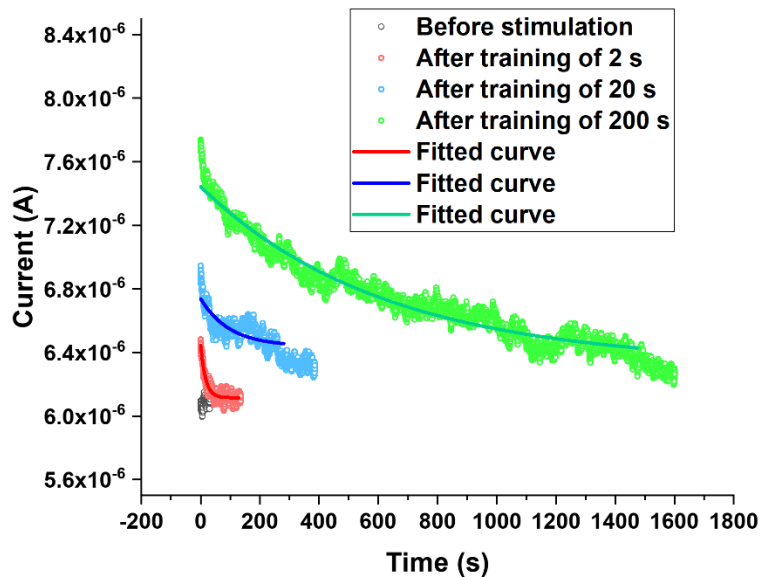

Figure S9: The STM to LTM transition of the synaptic device using the "press-teach spiking pair" shown in Figure 5.

7. The ability to strengthen the learnt behaviour with practising

The decreasing synaptic weight over a period is a natural forgetting process, which is important for humans, for example, to clear out "all those learnt extraneous things, which otherwise could clutter our neural system" (*59*). On other hand, forgetting a behaviour that we would like to retain can be problematic too. In reality, this may be prevented by two means:

1) A long teaching time, either one-off or multiple times over a period. The supporting Videos 2 and 3 show such behaviours. But this may be less frequently seen in the real life, since one may not expect a teacher to come and teach for a long time or again and again. And yet, one may still forget what has been taught over time, if one has a bad memory.

2) More likely, the situation would be that one learns something from a teacher. After the teacher has left, one could strengthen/retain the learnt behaviour by practising (rehearsal). If the rehearsal is done from time to time, one cannot forget the learnt behaviour.

The proposed artificial neural pathway can mimic the "strengthening by practising" phenomenon as well. For this, the spiking signal from the second level neuron needs to be fed back to the synaptic transistor (Fig. S10a). The co-existence of the spiking signal from the first level and the feedback signal from the second level could train the synaptic device (Fig. S10d), just like the phenomenon shown in Figures 5a 5b, 5d and 5e, where the co-existence of the spiking signals from the first level neuron and the "external teacher signal" could train the synaptic device.

We have presented a possible method to implement the feedback system to demonstrate "strengthening by practising". To this end, we used a global clock signal of 5 Hz to realise the switching between the "Read" and "Write" stages for the artificial neural pathway (Figures R11b and R11c). For the spiking signal from the cuneate neuron, we employed a delay to the signal. The delay matches with the global clock frequency so that the spiking signal (from the cuneate neuron) in the "Read" stage could be delayed to the "Write" stage and it is also in phase with the sensory spiking (Figs. R9c and R9d), just as the case shown in Figure 5b. The delay could be realised by digital (e.g., digital signal processing) or analogue manner (e.g., the delaying IC MN3005 or TDA 1022). For more efficient training, the delayed signal has been amplified and clamped towards a positive value. With proper device engineering (e.g., decreasing the dielectric thickness), this may not be required.

The Supporting Video 4 shows the "strengthening by practising" behaviour from the as-developed neural pathway: at the beginning, there is no feedback. The firing of the cuneate neuron is weak (at a rate of 20~50 Hz, see Supporting Video 4). Once the feedback is introduced, the firing of the cuneate neuron gradually strengthens over time. And this goes in loop. After ~20 mins, the firing rate of the cuneate neuron reaches ~160 Hz (Supporting Video 4). This mimics the scenario that "practising after being taught" could strengthen the learnt behaviour over time. By contrast, if at the beginning, the weight of the synaptic transistor cannot lead to the firing of the cuneate neuron, the latter cannot fire over time by practising, even with the feedback. This is because the signal from the cuneate neuron is too weak, and the feedback could not lead to the sufficient strengthening of the synaptic weight from the transistor. This shows the importance of the teacher, without which the correct practising does not even exist. This also ends in loop.

Overall, we demonstrate the "strengthening by practising" behaviour for the proposed artificial neural pathway. It should be noted that the proposed method is only one possible way to realise the feedback, and it depends on the type of synaptic device used in the whole system.
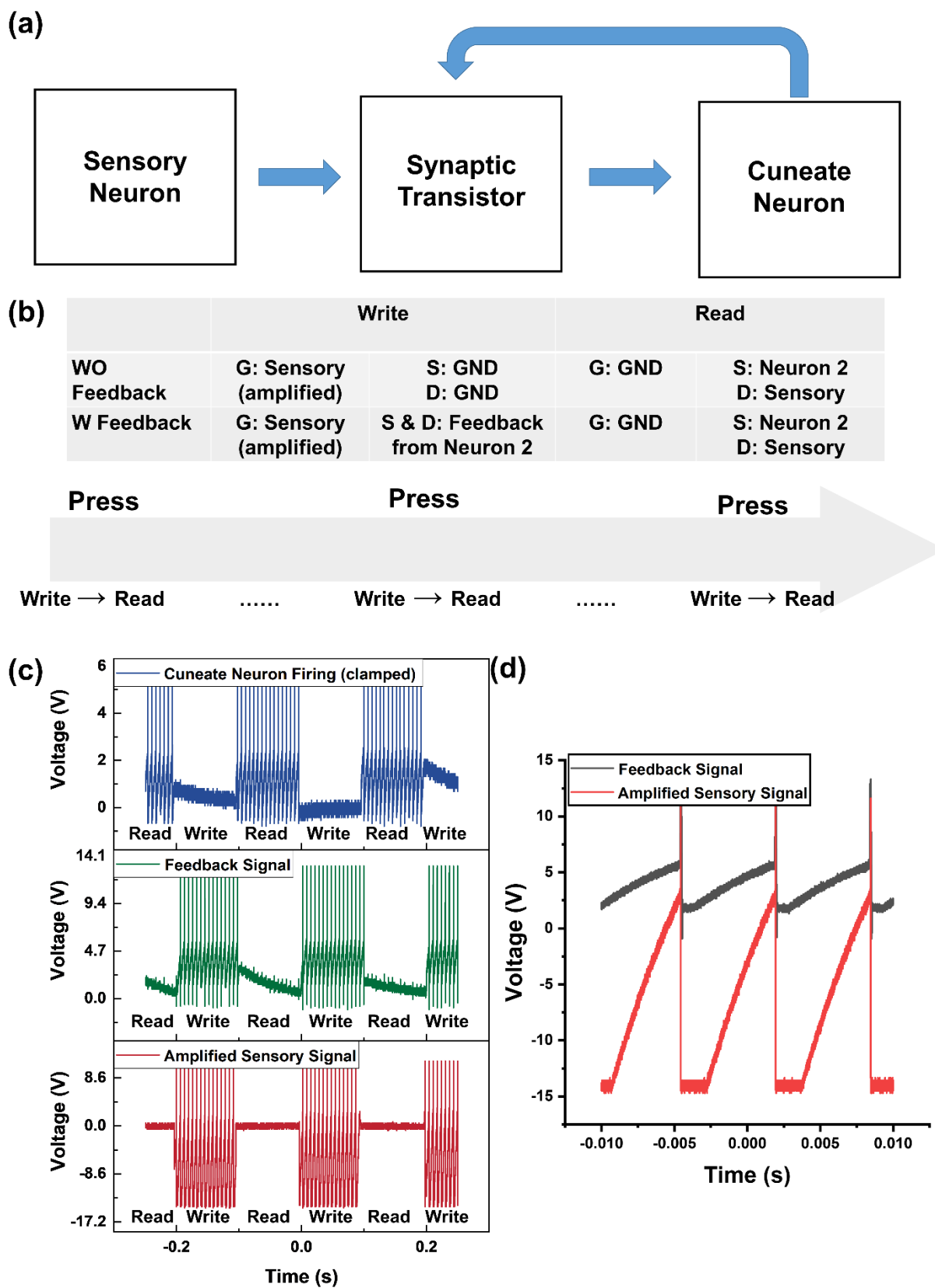
Figure S10: The rehearsal process demonstrated by the artificial neural pathway. (a) The schema showing the rehearsal process. (b) The detailed operation scheme for the tactile neural pathway. (c) The spiking signals used for rehearsal process at both read and write stages. (d) The zoomed in figure showing the pairing of the sensory spiking and the feedback spiking.

8. A possible neural network structure for the proposed e-Skin and the realisation of reinforcement learning

As discussed in the manuscript, for the computational e-Skin, we need a "many-to-many" neural network. For this, we need to consider the structure of the neural network. We propose a two-layer neural network as a possible solution (see Fig. S11). The sensory neurons in the first layer are locally interconnected, and the outputs are then fed into the cuneate neurons in the second layer. This is similar to the case of reservoir computing, as the sensory input would be mapped into the higher dimensional space in the first layer and further computation would be carried out in the second layer (so that complicated tasks can be realised by using a network of two layers). Interestingly, this is also similar to the biological case, where the mechanoreceptors in the biological skin are interconnected locally (*60, 61*). Nevertheless, in the biological skin, the case is more complicated, as the skin is soft and would deform under external pressure. It is argued that the deformation would lead to the change of the receptive fields (*62, 63*), thus influencing the tactile sensation (*64*). This is believed to be the unique aspect of tactile sensing.
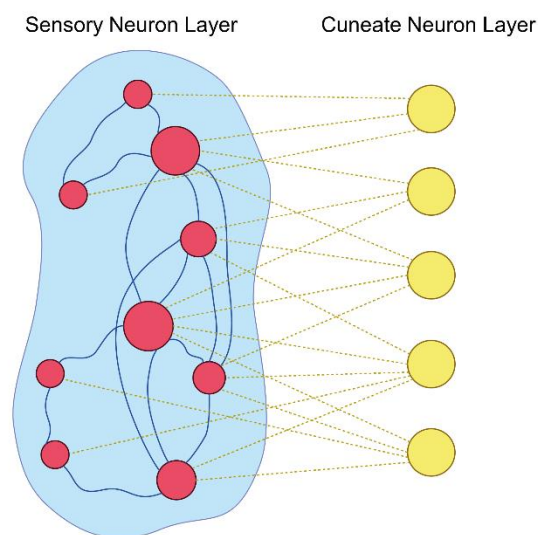

Figure S11: The proposed structure of the neural network for the computational e-Skin.

The learning behaviour of the e-Skin is also something we need to consider. Specifically, reinforcement learning is an important aspect of biological learning. The presented associative learning (in the main text) is localised learning. Except for this, there should also be a global control, so that the desired learnt behaviour can be strengthened, and the undesired behaviour can be forgotten. In biology, it can be partially achieved by the "reward circuit" and the "punishment circuit" inside the brain (reinforcement learning) (*65*). For robots, we can mimic such a system in different ways. For example, Q-learning can be adopted for robot control. While this is indeed fascinating, the hardware implementation of such an algorithm requires specific and usually complicated hardware (*66*), and this is by now in the form of a non-flexible platform. Owing to these, it may be more suitable to be arranged in the central control system equivalent to the brain. Deep Q-learning is also interesting, and the Ref. (*67*) discusses the possible hardware implementation method; but owing to the same challenge, this may not be suitable to put in the skin level as well. Nevertheless, we do believe that introduction of reinforcement learning at the e-Skin can be beneficial. One potential way is to use the "three-factor learning" (*68, 69*). In biology, associative learning is often influenced by the "third factor", to give a global control of the learning process (*68, 69*). For example, dopamine as a reward can lead to synaptic facilitation and acetylcholine as a punishment can lead to depression (*70, 71*). It would be interesting to mimic such behaviour in order to mimic the "biological reinforcement learning" process in robots: for example, part of the reinforcement learning process (the "three-factor" synaptic behaviour") can be realised

at the skin level and the rest (e.g., determining reward/punishment) can be realised using the central control panel. However, with respect to the artificial synaptic device, how to incorporate such an environmental effect as the "third factor" to modulate the synaptic behaviour, similar to that observed in the biological system, has still not been explored. This would be our future goal.

9. Distribution identification for the large-area synaptic transistor matrix

The weight modulation ratio from the as-realised device matrix is found to follow a lognormal distribution, with a p value of 0.258>0.05 (Fig. S12). The conductance at the 100th cycle from the as-realised device matrix is found to follow a Gamma distribution, with a p value of 0.131>0.05 (Fig. S13). In this regard, the extrapolated dataset is assumed to follow the same distribution for the weight modulation ratio and the final state conductance, with the same shape and scale factor.
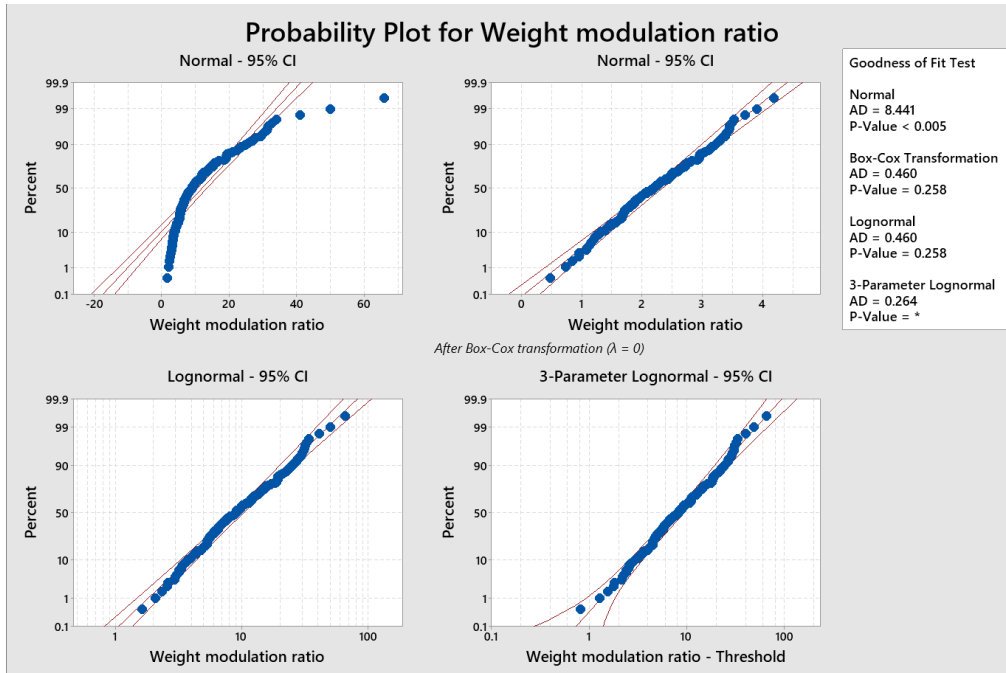

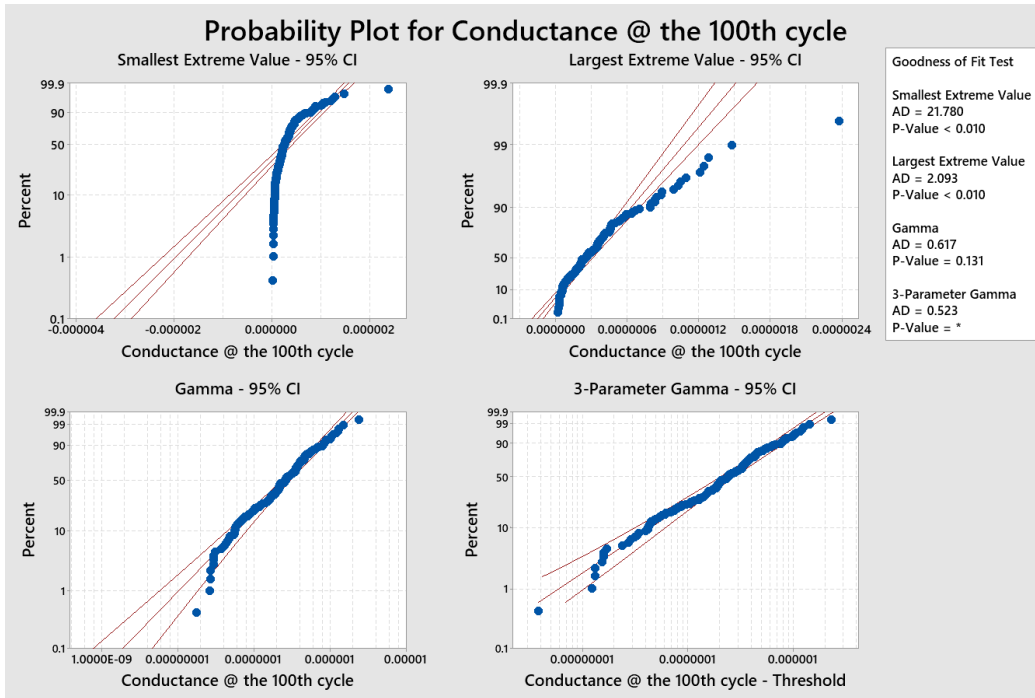Figure S12: The indentification of the distribution type for the weight modulation ratio.

Figure S13: The indentification of the distribution type for the synaptic transistor conductance @ the 100th cycle.