A Less-Intrusive Approach to Stabilize VSC Transmission against Highly Variable Grid Strength

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***Abstract*— A less-intrusive solution to stabilize a Voltage Source Converter (VSC) over an unknown grid strength is presented in this paper. The existence of equilibrium point is investigated as a pre-requisite to stabilization. By partially imposing grid forming control, a simple auxiliary outer loop is proposed to exhaust the physical limit of power delivery in steady state and provide support to fault-ride-through operations over a wide range of grid strength. The proposed control can be used to upgrade a commissioned VSC with inner current loop intact; it also offers a non-intrusive solution to stabilize VSCs externally. The effectiveness of the proposed approach and schemes are verified by analysis in frequency domain and case studies in time domain including change of grid strength and fault-ride-through.**

***Index Terms*— voltage source converter, grid strength, voltage stability, voltage sensitivity, stabilization, damping, fault-ride-through.**

I. Introduction

Indexed by Short Circuit Ratio (SCR), the grid strength of a power network can be variable， which can impact the integration of a Voltage Source Converter (VSC) [1]. The variation can be caused by fast-developing incidents, such as depletion of a hydro power plant, isolation of a faulty power line, network operations, etc., which are usually temporary [2]. On the other hand, the change of SCR values can also be caused by a slowly-evolving process such as replacement of centralized synchronous generators with renewables, which is ever-lasting and already witnessed by Great Britain power network [1]. For both scenarios, the variation can be significant [2]. One seldom-explored issue is whether those commissioned VSCs can sustain with such variations that they were not designed for. Obviously, a robust solution against the variation of grid strength is expected for those VSCs, either implemented by VSC vendors or utilities.

The control strategies of a VSC can be divided into 2 types: inner loop for voltage regulation [3-5] and inner loop for current regulation [6-8].

By mimicking the behavior of synchronous machines, control strategies using inner voltage loop, which are often referred to as Virtual Synchronous Machine (VSM) [3] or equivalently power synchronization control [4][5], can offer stability in weak grids [4][5], as well as strong grid [3]. However, they are limited by the difficulties in handling transient current, which requires a mode switching to ride through a fault [9].

Typically using current feedback control for the inner loops, classical vector control offers capability in handling transient current as well as steady-state, and is implemented in most commissioned VSC projects [10]. A well-recognized challenge for classical vector control is the risk of instability in weak grids [10]. This is a result of its original design assumption, which presumes that the grid strength is always adequate, and the VSC's impact to the grid is negligible [6]. Such assumption has been proved invalid for weak grid conditions due to two amplified issues, i.e. small-signal damping [11-14] and the constraint of power flow [15][16].

Since PLL has been blamed as the cause of negative damping in weak grids [17-18], intensive researches have been carried out to mitigate the impact brought by PLL [19-23]. The corresponding approaches can be categorized into two types: 1) tuning the parameters of a PLL [22][23]; 2) modifying the structure of PLL [19][20]. By reducing the gains of a PLL in weaker grids, the former type can effectively improve system damping when the grid condition is fixed or known; however, its robustness is undermined when the grid strength is unknown in a fast-developing event, e.g. fault isolation. By adding extra compensation or modifying the closed-loop design of a PLL [19][20], the latter approach can be designed with better damping against *SCR* variations. However, the absence of effective reactive power dispatching scheme limits the operational margin, particularly over the grid conditions of low *SCR* values and high *X*/*R* ratios [21]. Known as "var/volt" droop, reactive power/voltage droop can provide automatic voltage support [22]; nevertheless, its coupling effect with electromagnetic damping has been overlooked and therefore not adequately investigated. Further, , for most studies reported, stability analysis are based on a granted equilibrium point [3-21], but how it is reached has not been explicitly explained.

Recognizing PLL not the sole disturbing element for vector control in weak grids, another category of control approaches introduce outer loops to mitigate instability of vector control [24-26]. Compensating reactive current according to active current, an active power based feed-forward process can provide appropriate reactive power; at the meantime, it also improves damping in extremely weak grids. Nevertheless, this scheme requires instantaneous information of grid impedance, which is demanding in case of a significant grid change [24]. As an alternative solution, cross-coupling control is effective in addressing the issues of damping and reactive power at the same time, but its effectiveness is sensitive to variations of operational points and grid conditions. As a result, it is subject to dedicated design of gain scheduling scheme, which is of high complexity when grid strength is highly variable [25].

Moreover, for both PLL and outer loop approaches reported, the access to the internal control of the main VSC is essential [17-26]. In reality, it is inconvenient for the owners

to upgrade those commissioned VSCs due to legal disputes and access difficulties.

As a non-intrusive solution, battery storage/STATCOM has been suggested to provide damping service for wind farms with VSM control [27]. With the challenge of handling transient current inherited from VSM, such external stabilizer requires extra current rating to ride through a fault, which would add up to the capital cost significantly.

Another type of VSC control cascades inner loops of current with deterministic outer loops, i.e. voltage/frequency droops [28][29]. By applying closed-loop controls over the full vector of terminal voltage, such control scheme is desirable for island mode as a grid-forming scheme [33]. When the grid strength is significantly variable, a trade-off between the accuracy of power dispatching and coordination among voltage sources is expected. Thus, complex parametric tuning or mode switching will be again expected according to instantaneous grid condition. Practically, it is rarely implemented by VSCs of large scale.

In this paper, a simple approach of partial grid-forming is proposed. By analysing equilibrium region of VSC operation, selected voltage loops are proposed given the constraint of power flow and electromagnetic dynamics. Comparing with known approaches, the proposed scheme can provide an improved performance with the following benefits altogether: (1) robustness against unknown grid strength over a wide range (from SCR = 0.9~∞) including the region of dQ/dV<0; (2) flexibility as a less- or non-intrusive solution to commissioned VSCs; (3) improvement of transient stability during a Fault-Ride-Through (FRT) under extremely weak grid conditions. Besides, the mechanism of instability in weak grid is also updated other than the known issue of PLL.

The rest of this paper is organized as follows. The system benchmark model, static operational constraints of power flow is introduced in Section II; the principles, dynamic analysis and time domain case studies of the proposed control scheme are presented in Section III; the non-intrusive stabilization schemes and case studies are introduced in Section IV, and the conclusion is finally drawn in Section V.

II. Steady State Constraints and Equilibrium Point

A. System layout and cascaded control for VSC

In order to analyze the performance of a vector control based VSC in weak grids, a benchmark system is established in Fig. 1 as shown, where the classical average converter model is used in this paper [20-28].

Illustrated by the main circuit in Fig. 1, R_1 and L_1 are the resistance and inductance of the VSC reactor; C the VSC filter capacitance; R_T , L_T the grid transformer resistance and leakage inductance; R_{Net} and L_{Net} the equivalent resistance and inductance of the AC grid; V_C and V_{conv} the magnitudes of the capacitor voltage and the modulated voltage of the VSC bridge ; R_2 and L_2 the equivalent total converter side impedance of the grid and transformer; p_1 and q_1 the active and reactive power of VSC flowing towards grid side; p_2 and q_2 the active and capacitive reactive power flowing into the grid; q_c the capacitor reactive power flowing into the grid; $\overrightarrow{\boldsymbol{I}_2}$ the grid current vector.

The classical vector control of VSC in d-q reference frame is also incorporated in Fig. 1, where instantaneous values are considered: V_{Cd} and V_{Cq} refer to the capacitor voltage components in d- and q- axis; i_{Cd} and i_{Cq} the VSC current components in d- and q- axis; i_{Cd}^* and i_{Cq}^* the reference values of i_{Cd} and i_{Cq}; V_{Convd}^* and V_{Convq}^* the modulated voltage order of VSC in d- and q- axis; V_c^* and p^* are the references of capacitor voltage the active power; V_{cd}^* and V_{cq}^* are the references of outer voltage control loops; are the dispatched active and reactive power respectively. Ignoring the modulation harmonics, the average model is used in the time domain simulation of this paper.

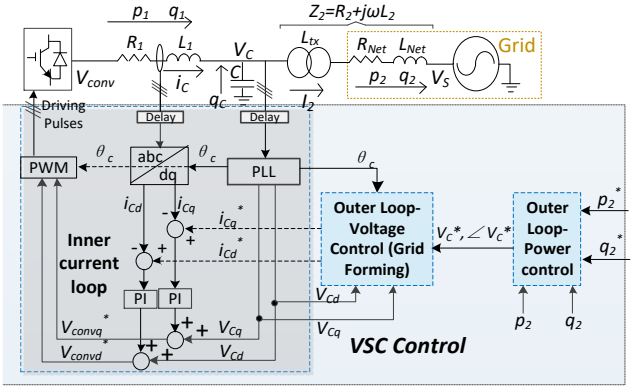


Fig. 1. Generic benchmark VSC model with cascaded grid forming control.

To preserve the capability of FRT, inner current loops are essential. Despite various implementations and adopted reference frame, the control structure of a cascaded VSC control can be generalized as Fig. 1 shows [28][29][33]. With the closed-loops of a complete voltage vector feeding inner loops, the VSC terminal can operate as an ideal slack bus with improved damping and robustness against grid conditions [30]. However, when a VSC is to operate as a non-slack bus, further outer power loops have to be cascaded [33].

Nevertheless, the provision of order for a complete voltage vector requires the references of active power and reactive power simultaneously. When the grid strength is variable, the reactive power compensation is sensitive to grid conditions and the mitigation will involve further loops. This will lead to a very complex control design. Therefore, this paper proposes a simpler control strategy to suit the need for non-slack bus VSCs with variable grid strength.

B. The Non-equilibrium region and static voltage sensitivity

This section investigates how power dispatching will affect the existence of equilibrium point over variable grid strength.

From Fig. 1 and using the grid voltage as the reference vector, there is [24]

$$-1 \le (P_2\omega L_2 - Q_2R_2)/(V_CV_S) = sin\theta_C \le 1 \quad (1)$$

$$-1 \le (V_C^2 - Q_2\omega L_2 - P_2R_2)/(V_CV_S) = cos\theta_C \le 1 \quad (2)$$

where P_2 and Q_2 are the phasor average form of p_2 and q_2, respectively. By applying $(1)^2 + (2)^2$ on both sides of the equal sign, (1)(2) will lead to

$$(P_2\omega L_2 - Q_2R_2)^2 + (V_C^2 - Q_2\omega L_2 - P_2R_2)^2 = (V_CV_S)^2 \quad (3)$$

To ensure the existence of a real solution of the equilibrium voltage V_c to (1)(2), there is [16][24]

$$\Delta = (2P_2R_2 + 2\omega L_2Q_2 + V_S^2)^2 - 4[(-R_2Q_2 + \omega L_2P_2)^2 + (P_2R_2 + \omega L_2Q_2)^2] \geq 0 \quad (4)$$

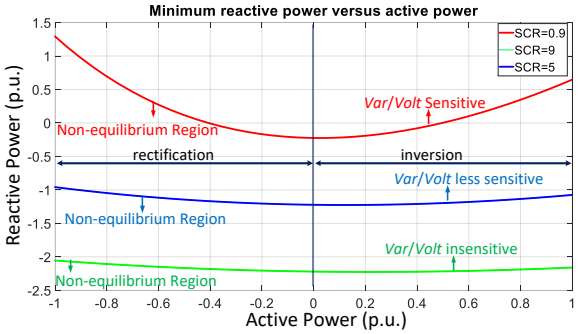
Solving (4) for Q_2, there is

$$Q_2 \geq \frac{-V_S^4 - 4Q_2R_2V_S^2 + 4R_2^2Q_2^2 + 4\omega^2L_2^2P_2^2}{4\omega L_2V_S^2 + 8P_2R_2\omega L_2} \quad (5)$$

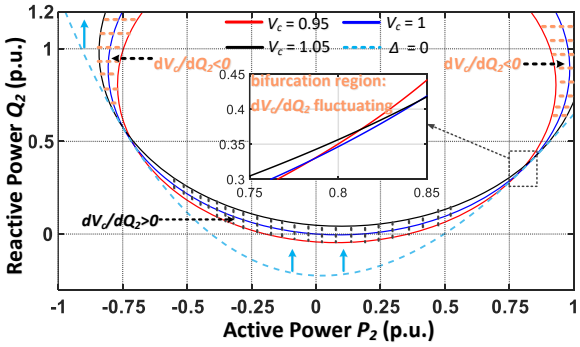
The inequities of (1)(2)(4) are sufficient and necessary condition to ensure existence of equilibrium point. Assuming $R_2 << \omega L_2$ for transmission network, there is $\omega L_2 \approx 1/SCR$, and $p_1 = p_2$, (4) can be re-organized as

$$Q_2(P_1, SCR) \geq \frac{(-V_S^4 - 4P_1R_2V_S^2 + 4P_1^2/SCR^2 + 4Q_2^2R_2^2)SCR}{4V_S^2 + 8P_1R_2} \quad (6)$$

Assigning various values of *SCR* to (5), the minimum required reactive power is illustrated in Fig. 2(a). As shown, when the grid is strong (*SCR* = 5, 9), the minimum reactive power is below zero (inductive reactive power referred to as negative). When the grid is very weak, *SCR* = 0.9 for instance, the minimum has to be well above zero. This minimum reactive support is monotonic for a bidirectional power flow.



(a) non-equilibrium region with Variable SCR



(b) operating region when SCR = 0.9

Fig. 2. Equilibrium region in *Q*-*P* plane

Keeping irrelevant variable constant in (3), the static sensitivity of voltage in respect to reactive power can be obtained as

$$\frac{dV_c}{dQ_2} = \frac{V_c^2\omega L_2 - R_2^2Q_2 - \omega^2L_2^2Q_2}{2{V_c}^3 - V_c(2Q_2R_2 + V_S^2) - 2V_c\omega L_2Q_2} \quad (7)$$

, which is a non-linear and non-monotonic function of grid condition and power.

By keeping V_c = 0.95, 1 and 1.05 p.u., the *Q*-*P* curve of *SCR* = 0.9 is illustrated in Fig. 2(b). As shown, to reach the physical limit of active power between the curves of V_c = 0.95 and 1.05 p.u., the equilibrium point has to withstand with both positive voltage sensitivity (for low power) and negative voltage sensitivity (for high power).

To prevent voltage collapse, a robust reactive power compensation scheme is essential to ensure the existence of voltage equilibrium and to mitigate the impact of negative voltage sensitivity at the same time.

C. Securing an equilibrium point with var/volt regulation

In this section, it is mathematically proved that why a local var/volt droop of high stiffness is beneficial to secure an equilibrium point. Considering a feedback var/volt droop with a reference voltage V_C^* as

$$K = \frac{Q_2}{V_C^* - V_C} \quad (8)$$

and substitute (8) into (3), there is

$$\begin{aligned} &{V_C}^4 + 2\omega L_2KV_C^3 - 2K^2V_C^*(\omega^2L_2^2 + R_2^2)V_C \\ &+K^2(\omega^2L_2^2 + R_2^2){V_C^*}^2 + (\omega^2L_2^2 + R_2^2)P_2^2 \\ &+(-2P_2R_2 - V_S^2 - 2\omega L_2KV_C^* + K^2\omega^2L_2^2 + K^2R_2^2)V_C^2 \\ &= 0 = f(V_C) \end{aligned} \quad (9)$$

Since $f(V_C)$is 2nd order differentiable, to secure an equilibrium point within the maximum voltage deviation ΔV_{max} from the reference value V_C^*, one sufficient condition to ensure the existence of V_C within $[V_C^* - \Delta V_{max}, V_C^* + \Delta V_{max}]$ is

$$f(V_C^* - \Delta V_{max}) < 0 \quad (10)$$

and

$$f(V_C^* + \Delta V_{max}) > 0 \quad (11)$$

Considering $f(V_C)$ as a function of *K*, (8) can be re-arranged as

$$l(K) = f(V_C) \approx \left(\frac{1}{SCR}(V_C^* - V_C)K + V_C\right)^2 - V_C^2 + {V_C}^4 + (-2P_2R_2 - V_S^2)V_C^2 + \frac{P_2^2}{SCR^2} \quad (12)$$

and its differential in respect to *K* can be obtained as

$$\begin{aligned} l'(K) &= 2\left(\frac{1}{SCR}(V_C^* - V_C)K + V_C\right)\frac{1}{SCR}(V_C^* - V_C) \\ &= \begin{cases} -2\left(-\frac{\Delta V_{max}}{SCR}K + V_C^* - \Delta V_{max}\right)\frac{\Delta V_{max}}{SCR}|_{V_C = V_C^* - \Delta V_{max}} \\ 2\left(\frac{\Delta V_{max}}{SCR}K + V_C^* + \Delta V_{max}\right)\frac{\Delta V_{max}}{SCR}|_{V_C = V_C^* + \Delta V_{max}} \end{cases} \end{aligned} \quad (13)$$

Combining (12) with the following practical constraints

$$K > 0,\ 0 < \Delta V_{max} \ll 1,\ SCR > 0,\ 0 < V_C^* \approx 1,\ -1 \leq P_2 \leq 1 \quad (14)$$

when

$$\frac{V_C^*}{\Delta V_{max}} > \frac{K}{SCR} + 1 \quad (15)$$

, for any valid value of $\Delta V_{max}, V_C^*, SCR, P_2$, there is

$$\begin{cases} l'(K)|_{V_C = V_C^* - \Delta V_{max}} < 0 \\ l'(K)|_{V_C = V_C^* + \Delta V_{max}} > 0 \end{cases} \quad (16)$$

, which implies that within the range of (14)(15), a greater value of *K* contributes to satisfying (10) and (11), and is therefore beneficial to ensure an equilibrium point in the interested range $[V_C^* - \Delta V_{max}, V_C^* + \Delta V_{max}]$.

Once an equilibrium voltage exists, var/volt droop can linearize the *Q*-*V* process. As is demonstrated by the simplified block diagram in Fig. 3, where *H*(s) is the plant of V_c(s)/q_2(s) and the simplified closed-loop transfer function is

$$V_c(s)/V_c^* = KH(s)/(1 + KH(s)) \quad (17)$$

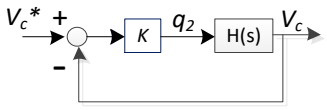


Fig. 3 Simplified Block Diagram of Voltage Control

From (17) and Fig. 3, when $|KH(s)|$>>1, there is $V_c/V_{ref} \approx 1$. This implies that if the droop gain is sufficiently large, it will force the local voltage to settle in close vicinity of the reference value and mitigate the impact of grid strength variations at steady state.

D. Numerical design for a practical var/volt droop

As an illustration, the most adverse condition of VSC-HVDC integration in GB power network is reported to be an *SCR* between 1.2 and 6 [2]. Given a declining grid strength in reality, *SCR* = 0.9 is considered as an adequate boundary in this paper. Considering an *X*/*R* ratio as $\omega L_2/R_2 = 10$ and sensibly assuming $V_C V_G \approx 1$ for simplicity, the required reactive power can be solved with the constraint of (1) and (2) re-organized as (18) and (19)

$$Q_2 \le V_C V_S \cdot \frac{1}{R_2} + p_2 \cdot \frac{\omega L_2}{R_2} \tag{18}$$

$$Q_2 \ge -V_C V_S \cdot \frac{1}{R_2} + P_2 \cdot \frac{\omega L_2}{R_2} \tag{19}$$

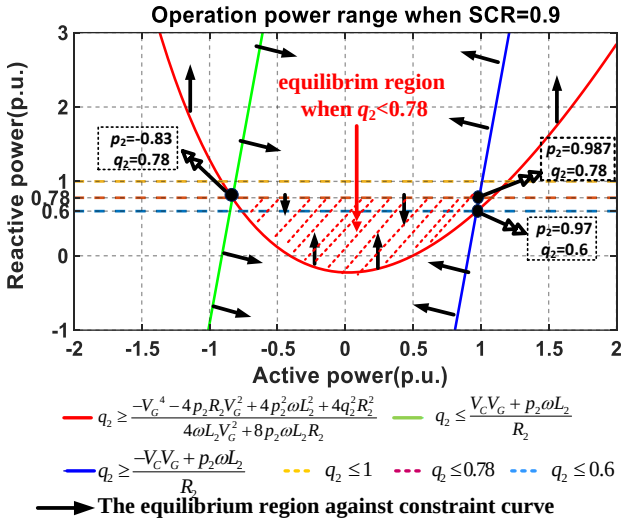


Fig. 4. Static operating region in an extremely weak grid

When the grid is extremely weak, (18)(19) becomes a significant constraint. This is visualized in Fig. 4. It can be seen that to enable an active power of 0.987 p.u., the reactive power has to be above 0.78 p.u.; and the minimum reactive power has to go up to 1 p.u. to enable an active power of 1.01 p.u.. Meanwhile, it could also be found that the rectifying active power (DC to AC) cannot exceed -0.83 p.u. due to the constraint denoted by (18), the green curve. Therefore, for an optimal usage of converter rating, a sensible range of active power is considered between -0.83 p.u. to 0.987 p.u., which corresponds to a maximum reactive power Q_{2max} = 0.78 p.u..

The minimum local voltage to satisfy Inequs. (1)(2)(14) can be obtained as

$$V_C \ge \frac{P_1 - Q_2 R_2 SCR}{SCR \cdot V_S} \tag{20}$$

where (20) is obtained by substituting $\omega L_2 \approx 1/SCR$ into (1) considering (14). The largest steady state voltage deviation occurs when the reactive power reaches the highest magnitude. To optimize the converter rating, the maximum voltage deviation $\Delta|V_C|_{max}$ should correspond to maximum power according to (6). Therefore, the reference voltage can be obtained by combing (8)(20) as

$$V_C^* \ge (Q_{2max} - Q_C)/K + \frac{P_1 - Q_2 R_2 SCR}{SCR \cdot V_S} \tag{21}$$

In reality, the permitted voltage variation is usually between 5% to 10%; therefore, a voltage deviation of $\Delta V_{C\,max}$ = 3% is illustrated in this paper. Assigning a sensible size of shunt capacitor as Q_c = 0.1 p.u., droop gain can be obtained with (8) as *K* = (0.78-0.1)/3% = 22 And then, the reference $V_C^* = 1.04\ p.u.$ can be obtained with (21) by assigning the boundary values as P_1 = 0.987 p.u., Q_2 = 0.78 p.u., *SCR* = 0.9 when V_s = 1 p.u..

To sum up Section II, it has been proved that a local var/volt droop of high stiffness is an essential option to secure an equilibrium voltage against unknown grid strength. However, such design has not taken the impact of electromagnetic process into account, which is inadequate for stabilization.

III. Electromagnetic Dynamic Analysis and the Proposed Damping Enhancement Control

A. Analytical model in frequency domain and initial settings

To further find out how the var/volt droop may affect the small-signal damping including electromagnetic dynamics, an analytical model in frequency domain is established. In this model, the electromagnetic dynamics of inductive and capacitive elements, PLL, coordinate transformations, current control are considered altogether [20][25].

By aligning the d-axis with the voltage vector of the main grid, the electrical circuit is modeled as (22), and the associate state space is defined in (23) and (24).

$$\dot{x} = Ax + Bu \tag{22}$$

$$x = \left[i_{cd}\ i_{cq}\ V_{cd}\ V_{cq}\ i_{2d}\ i_{2q}\right]^T \quad ; \quad u = \left[V_{sd}\ V_{sq} V_{convd}\ V_{convq}\right]^T \tag{23}$$

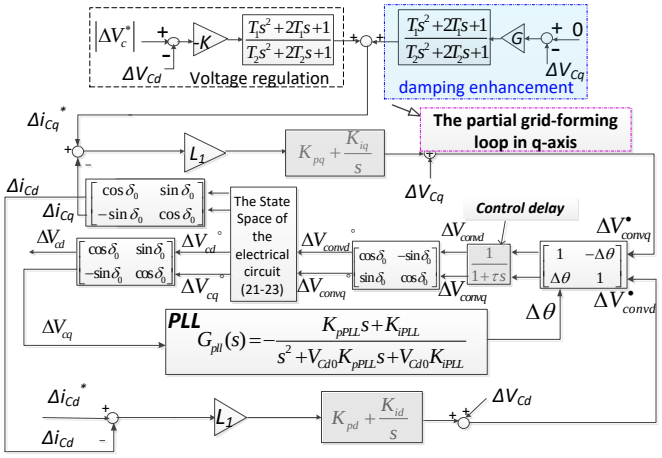
$$A = \begin{bmatrix} -\frac{R_1}{L_1} & \omega & -\frac{1}{L_1} & 0 & 0 & 0 \\ -\omega & -\frac{R_1}{L_1} & 0 & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C} & 0 & 0 & -\omega & -\frac{1}{C} & 0 \\ 0 & \frac{1}{C} & \omega & 0 & 0 & -\frac{1}{C} \\ 0 & 0 & -\frac{1}{L_2} & 0 & -\frac{R_2}{L_2} & \omega \\ 0 & 0 & 0 & \frac{1}{L_2} & -\omega & -\frac{R_2}{L_2} \end{bmatrix} \quad B = \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 \end{bmatrix} \tag{24}$$

By incorporating (22) with the small-signal model of current control, coordinate transformation and PLL, a comprehensive frequency domain model is established as Fig. 5 (a) shows.

In the model shown by Fig. 5 (a), where K_{pd} and K_{id} refer to the PI regulator gains of the d-axis current loop, respectively; K_{pq} and K_{iq} the proportional and integral gains of the q-axis current loop. In the rest of the paper, the gains of PI regulators for d- and q- current loops are set to make bandwidths of both current loops at 50 Hz (when connecting

to an infinite bus) [20]; K_{pPLL} and K_{iPLL} the proportional and integral gains of PLL, which are set to make a natural frequency of 5 Hz and damping coefficient of 1 when tracking a stiff 3-phase source [20]; δ_0 the operating power angle between VSC capacitor and the main grid. V_{cd} and V_{cq} refer to the capacitor voltage components in d- and q-axis; V_{cond} and V_{conq} are referred to as the converter voltage components in d- and q-axis, respectively. V_{cd0} and V_{cq0} are the operational points of the capacitor voltage in d- and q- axis. The input and output signal of the electrical plant is shifted by the power angle δ_0, to adapt to the voltage reference frame aligned with the capacitor voltage for VSC control. The delay caused by digital control is modeled as a first order process with a time constant of τ, which is set at 0.002 s for a switching frequency of 2.5 kHz each cyle and symmetrical pulse width modulation [34][35] for an adverse control delay.

The signal i_{cd}* comes from the output of the power loop. As is shown in Fig. 5(c), the power loop is mainly a feed-forward process with the assistance of an integral control to mitigate the steady state error. The integral gain is assumed sufficiently small that its dynamics is negligible for simplicity, V_{cn} is a constant value of nominal voltage.



(a) Analytical model of VSC in frequency domain

(b) Uncompensated partial grid-forming (c) Active power loop

Fig. 5. Analytical model of the VSC

B. *The dynamic impact a standard var/volt droop*

From this section on, all initial parametric settings are by default as what is suggested in Section II-D and III-A unless otherwise stated. The operational point of full power inversion corresponding to (22) is calculated as

$x_0 = [0.7584; 0.8724; 0.1428; 1.016; 0.86; 0.8866]^T$

$u_0 = [1; 0; 0.09; 1.1636]^T$

With "the voltage regulation" and the "partial grid-forming loop" replaced by a standard var/volt droop according to (7) and Fig. 3 in the model of Fig. 5(a), root locus analysis is carried out against an increased gain value of K, as Fig. 6 shows. As illustrated, when SCR = 9, the increased value of K from 0 to 9.5 can initially improve system damping by pushing the main pole towards the left side; this damping improvement saturates when K is around 4.5, and then increasing K starts to degrade damping thereafter. When the grid becomes weaker as SCR =3, damping improvement saturates earlier around K = 2.5.

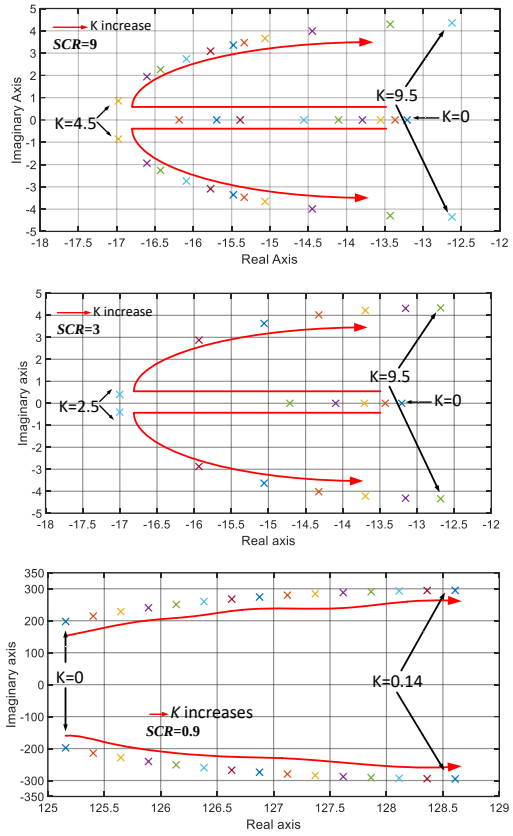


Fig. 6. Root locus against the gain of volt/var droop with variable SCR

To enable larger values of droop, lead-lag compensators are commonly used to fix the gain margin at low frequencies [32]. This approach is based on a presumption that there is a positive gain margin when the gain is sufficiently small. Such presumption is valid for the cases as SCR = 3, 9 in Fig. 6. However, when the grid becomes extremely weak, as the case of SCR = 0.9 in Fig. 6, there is no positive margin from K = 0; therefore, neither gain tuning nor any lead-lag compensator alone can stabilize the system in this case. From physical point of view, since the operating point is within the region of $dQ/dV<0$ shown in Figure 2(b), a positive feedback is introduced by the var/volt droop of (7) at 0 Hz in d-q frame, which cannot be compensated.

Therefore, to stabilize the system, the control structure has to be modified. Since the analysis in this section keeps PLL setting identical to strong grids, this instability mechanism is independent from PLL.

C. *Damping enhancement and its small-signal analysis*

To mitigate the impact of the positive feedback introduced by reactive compensation, a partial grid-forming feedback control is proposed, which is shown in Fig. 5(b). This design is based on 2 considerations:

1) A reactive power perturbation of Δq_p injected to the local bus will lead to q-axis current perturbation $\Delta i_p = -\Delta q_p / V_{c0}$. According to the electromagnetic dynamics of (22)-(24), there is

$$C\,\Delta V_{Cq}/dt = \Delta i_p = -\Delta q_p / V_{c0} \tag{25}$$

$$\frac{d\Delta i_{2q}}{dt} \approx \frac{\Delta V_{Cq}}{L_2} \tag{26}$$

Substitute (26) into (25) yields

$$\frac{d\Delta i_{2q}}{dt} \approx \frac{-1}{L_2 C V_{C0}} \int \Delta q_p dt \tag{27}$$

Equ. (27) implies that a positive reactive perturbation tends to decrease q-axis current on the grid side. This will initiate the fore cited positive feedback process introduced by the interaction between negative voltage sensitivity and the volt/var droop, which is demonstrated in Fig. 7. However, according to (25), this process has to gone through an electromagnetic process (charge the local capacitance *C*) to make it happen.

Using this partial grid-forming control shown in Fig. 5(b), this capacitive transient can be held back. As is shown in Fig. 7, by mitigating the charging transient of q-axis voltage, one chain of the positive feedback loop is broken so the system is stabilized.

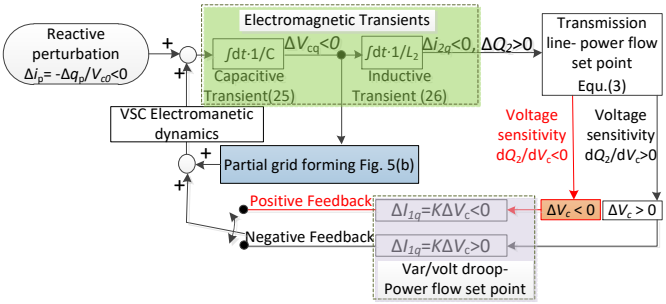


Fig. 7. Simplified principle of electromagnetic stabilization

2) Due to the presence of PLL, the steady state value of V_{cq} converges at 0. By setting the reference value of V_{cq} at 0, the steady state output of the regulator will also settle at zero. Thus, the operating point will not be shifted by this auxiliary control. Physically, it means that this added loop will not consume any current at steady state.

By replacing "voltage regulation" and "partial grid-forming loop" in Fig. 5(a) with the controls in Figs. 5(b), a root locus is obtained with an adverse condition of *SCR* = 0.9 and *K* up to 25, as Fig. 8 shows.

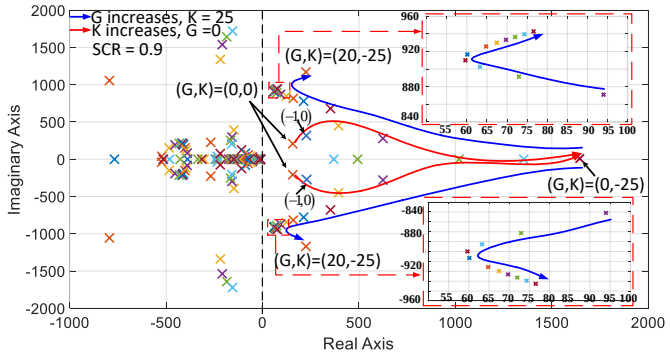


Fig. 8. Root locus for standard var/volt droop and simple virtual conductance

As is indicated by the red arrow in Fig. 8, increasing the value of *K* to 25 can adversely bring the real component of the main pole as far as 1600; whereas by introducing the partial grid-forming loop, the main pole can be pushed back towards the left plane when gain of the partial grid-forming loop *G* increases, indicated by the blue pointer. However, this improvement is saturated when the real component is approximately 100 in the right plane. This means that a standard q-axis grid-forming loop is inadequate for such condition.

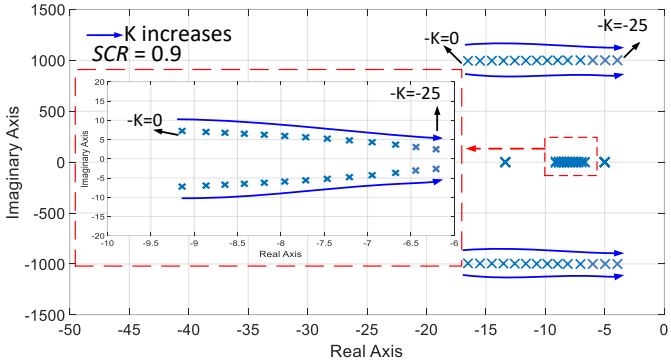


Fig. 9. Root locus with the proposed outer loop control

To further improve small-signal damping, a 2nd order lead-lag controller $\left(\frac{T_1 s+1}{T_2 s+1}\right)^2$ is proposed for the input of q-axis current as shown in Fig. 5 (a). By setting *G* = 16, a pre-fixed constant as T_2=0.2s and T_1=0.04s, root locus against the var/volt gain is again depicted in Fig. 9, with identical operational points used in Fig. 8.

As indicated by the blue arrow in Fig. 9, "the proposed damping outer loops" changes the distribution of the main poles from Fig. 8. Although the increased *K* value is still pushing the main poles towards the right plane, all the poles are distributed within the left plane while the range of *K* is unchanged. This indicates that the proposed outer loop control approach can effectively accommodate the conflict between var/volt droop and small-signal stability in this case.

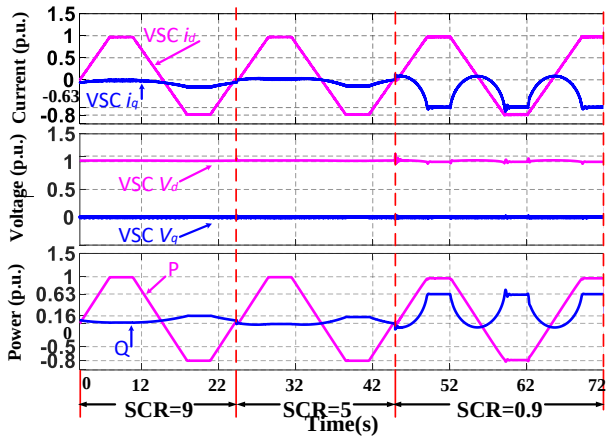
Given the volume of control parameters, i.e. gains of PI control, PLL, 2nd order regulator, etc., it is impractical to tune all of them analytically. Instead, this paper recommends fixed heuristic settings in p.u. and specifies the applicable conditions. Given a sensible range of grid strength, the pre-fixed parameters, along with the proposed control, have demonstrated stability in frequency domain, which indicates an expected robustness in time domain.

D. Time domain case studies

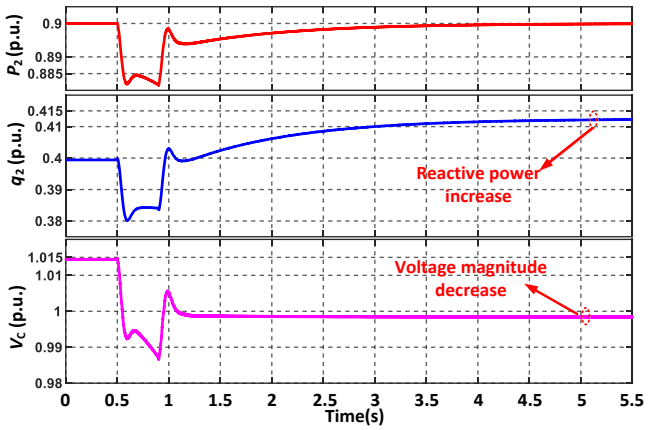
To verify the robustness of the proposed outer loop control against variable grid conditions, a time domain case study is carried out based on the instantaneous average converter model so electromagnetic dynamics are reflected.

To test the robustness of the control against full range of active power, a power ramp test of 0.25 p.u./sec for full delivery range is carried out in Fig. 10(a), the test starts with the situation when the VSC is connecting to a strong grid of *SCR* = 9. And then, a ramp order for i_d is given at a rate of 0.25 p.u./s till 1 p.u.. After the ramp has reached 1 p.u., the

ramp heads down towards -0.83 p.u. with a ramp of -0.25 p.u./sec. After staying at 0.83 p.u. for a few seconds, the ramp heads back to 0 p.u.. Throughout this test cycle, the control setting is unchanged and maximum reactive current demand is no more than 0.16 p.u.. Due to the use of a strong Var/Volt droop, the voltage is almost at the same level as the grid side. This shows that the settings designed for an extremely weak grid is compatible with a strong grid.



(a) power ramp test over variable grid strength

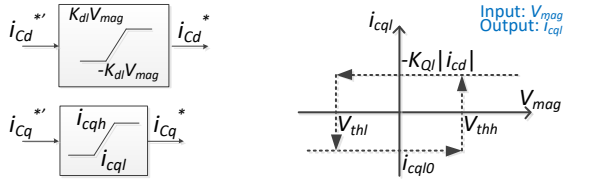


(b) reactive power change in dQ/dV<0 region (SCR = 0.9)

Fig. 10. Power ramp test with stabilization

To test the robustness against SCR variation, at Time = 24 s in Fig. 10(a), an *SCR* change is emulated to switch *SCR* to 5. Then, the ramp test cycle repeats. It can be seen that the responses of voltage and reactive current are hardly changed, which demonstrate rather consistent performance in strong grid.

At time = 45 s in Fig. 10(a), another *SCR* change is made to bring *SCR* to 0.9. When the ramp limit of 1 p.u. and -0.83 p.u., is reached, the reactive power autonomously reached approximately 0.63 p.u., which corresponds well to Fig. 4, given a local capacitor of 0.1 p.u.. The voltage is dropped by approximately 0.03 p.u. at steady state. This is a result from the strong var/volt droop and corresponds to the design with (8). It also worth mentioning that when Time = 48s ~ 53s and Time = 48s ~ 53s, the operating power is above 0.8 p.u. when V_c > 1.0 and *SCR* = 0.9, which is in the region of dV_c/dQ_2<0.



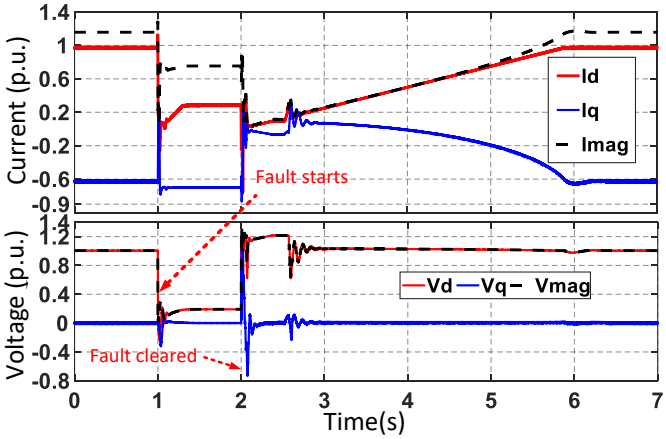
(a) Current saturations (b) hysteresis for q-axis current lower limit

Fig. 11. Dynamic current saturation

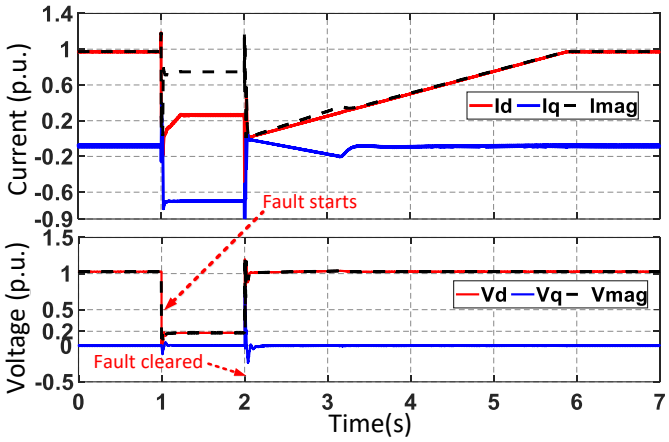
Throughout the ramp test in Fig. 10(a), K is fixed at 22 and the rest of parameters are identical to the ones used in Fig. 9. This time domain simulation result corresponds to the analysis of frequency domain against SCR variations in Section III-C.

To further verify the control in the region of dQ/dV<0, a reactive change is tested in Fig. 10(b), in which the active power starts at 0.9 p.u. when *SCR* = 0.9. At time = 0.5 s in Fig. 10(b), a reactive power disturbance is added to the VSC order which eventually leads to an increase of reactive power from 0.4 to 0.412 p.u.. Due to a power loop, the active power recovers 0.9 p.u. after the transient, but the voltage V_c drops from 1.015 p.u. to 0.998 p.u., which implies that an increase of reactive power to the grid is decreasing local voltage so the system is operating in an dQ/dV<0 region. This well corresponds to the situation estimated in Fig. 2(b) and shows that with the proposed electromagnetic damping scheme, voltage collapse is avoided successfully.

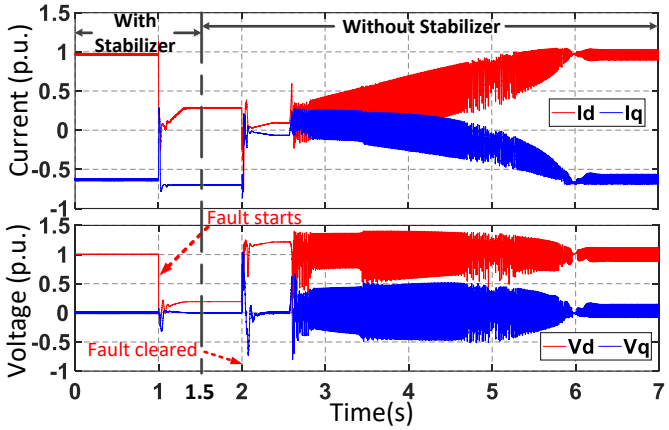
To test the impact of the proposed control to transient response, a fault-ride-through test is carried out. A dynamic current saturation strategy is employed to facilitate the process. As is shown by Fig. 11 (a), during significant voltage transient, the d-axis current order i_{cd}* is capped in proportion with $K_{dl}V_{mag}$, where V_{mag} is the magnitude of the capacitor voltage in per unit and K_{dl} is a positive constant. As is show by Fig. 11(b), a hysteresis is used to determine the lower limit of q-axis current, i_{cql}. The value of i_{cql} is dynamically set at $-K_{ql}|i_{Cd}|$ to avoid excessive reactive current at steady state in normal state; whereas, when the voltage dropped below a threshold V_{thl}, a fixed saturation point, i_{cq0}, is set to limit the current magnitude.



(a) SCR = 0.9 with stabilizer



(b) SCR = 9 with stabilizer



(c) SCR = 0.9 with stabilizer disabled during the fault

Fig. 12. Fault-ride-through test with variable grid stength

To illustrate the compatibility of an adverse FRT, specific settings are made as K_{dl} = 1, i_{cqh} = 1 p.u., and K_{Ql} = 0.7 and the fault-ride-through test is illustrated when *SCR*=0.9 in Fig. 12(a). As shown, the active power starts at 1 p.u. since Time = 0 s; a 3-phase fault happens at Time = 1 s. The fault brings the voltage magnitude to approximately 0.25 p.u.. Due to the dynamic saturation scheme and the presence of inner current loops, d-axis current is regulated at 0.25 p.u. During the fault, the q-axis current is regulated at the pre-defined saturation point -0.7 p.u.. Another fault-ride-through test is demonstrated when *SCR* = 9 in Fig. 12(b). As seen, the performance is largely similar to *SCR* = 0.9. The main difference introduced by weak grid is more transient oscillations at the fault and clearance. This is expected, as the damping in a weaker grid is degraded while the control settings are unchanged. However, the transient magnitudes of both voltage and current are still within a range of 1.4 p.u. and 0.9 p.u., respectively, which is acceptable.

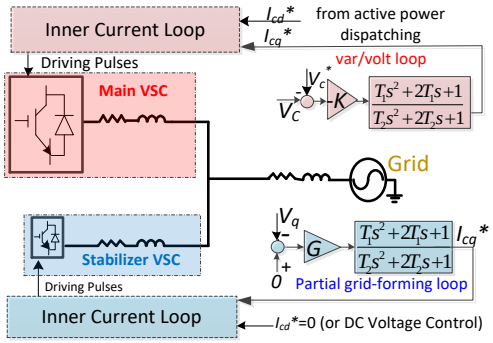
A further comparison FRT test is provided in Fig. 12(c), where all the condition are identical to the case of SCR = 0.9 in Fig. 11(a) except for the stabilizer disabled from Time = 1.5 s. As seem, at the settled point during the fault, the stability is not affected as the VSC is de-loaded; however, when the fault is cleared and the VSC starts to recover the active power, the system starts to oscillate at Time = 2.6 s. This is due to a degraded damping with greater power output [26] and the presence of strong var/volt droop adds up to this negative damping, which leads to oscillation when the VSC loading is below 0.2 p.u..

As the faulty types, FRT strategies and grid codes may vary, the actual FRT performance varies in real world practices. The scope of this paper cannot exhaust all the cases but only illustrates the compatibility with an adverse case. Nonetheless, the preservation of current loops should enable compatibility with other FRT strategies.

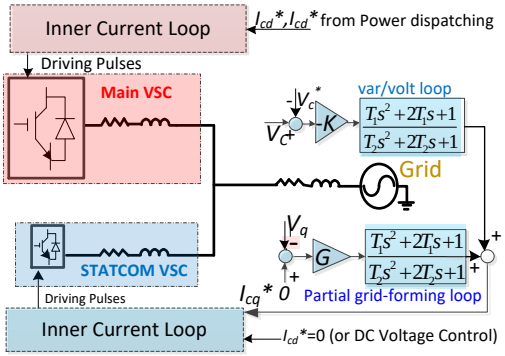
IV. Stabilizer as a Non-intrusive Solution

In this section, the grid side solution to improve damping is derived. To implement, the proposed damping enhancement control can be carried out by an external stabilizer out with the main VSC.

Since the damping enhancement scheme proposed in Fig. 5(a) completely keeps the inner loops intact and consumes zero current at steady state, the damping can be provided by a free-standing VSC, namely the "zero-current" stabilizer to the AC grid connected.



(a) Damping by "zero-current" stabilizer



(b) Damping by STATCOM

Fig. 13. Schematics of non-intrusive stabilization

By putting away the delivery of apparent power, the scheme of "zero-current" stabilizer can be derived from Fig. 5(a) as Fig. 13(a) shows. A ramp test is carried out to test in Fig. 14 with the control parameters used in Section III-D. As shown, when d-axis current i_d of VSC ramps up from t = 0 s at a rate of 0.25 p.u./s, the reactive current of the main VSC drops to around -0.67 p.u., which again correspond to the analysis in Section II-A. A moderate voltage overshoot of 1.25 p.u. occurs when the ramp stops at Time = 4 s. At the meantime, the stabilizer is consuming zero-current at steady state as expected. After Time = 4 s, a stabilizer transient current of 0.022 p.u. (peak value) occurs by the stoppage of the power

ramp. Such transient is caused by the rate of change of the current ramp. During Time = 6 ~ 9 s in Fig. 14, the stabilizer is disabled and oscillation immediately occurs. The oscillations disappears immediately after the stabilizer is re-enabled at Time = 9 s, which verifies the effectiveness of the external stabilizer.

Practically, the declination of DC voltage caused by semiconductor power losses can be recovered by a DC voltage loop and/or a storage so as to maintain an essential level for modulation [31].

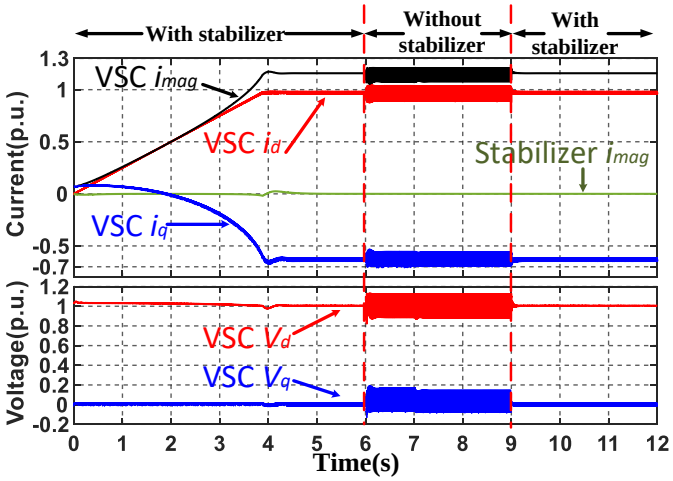


Fig. 14. Ramp test with "zero-current" stabilizer scheme

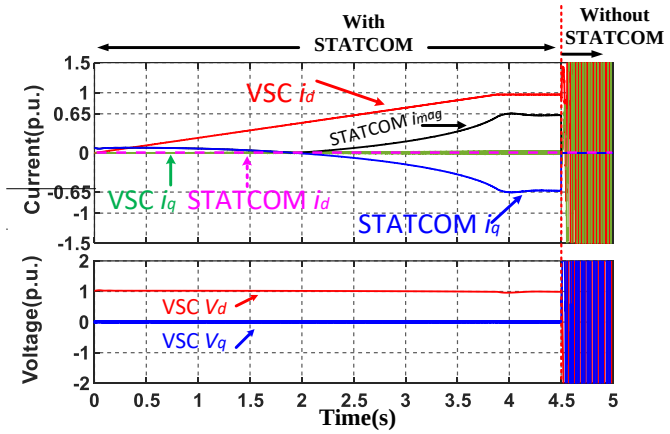


Fig. 15. Ramp test with STATCOM scheme

As an alternative scheme, the damping can be carried out along with var/volt droop externally, which is shown by the "main VSC+STATCOM" in Fig. 13(b). A similar ramp test as Fig. 15 is carried out with such scheme. As shown, the voltage and active power performance is almost identical as the previous "zero-current" scheme in Fig. 14(a); meanwhile, the provision of reactive current is shifted to the STATCOM. Consequently, the current magnitude of STATCOM has come to approximately 0.7 p.u.. When the STATCOM is disconnected in Fig. 15, the system starts to oscillate, which is more violently than Fig. 14. This is because the oscillations are triggered by the non-existence of equilibrium point and this oscillation cannot be mitigated by damping.

Discussion: For "all-in-one" scheme, grid conditions have to be fully predictable at the design stage to optimize the power capacity. For the STATCOM scheme, it is more suitable to "patch" a commissioned VSC with a declining fault level, but considerable reactive power capacity is expected. For the stabilizer scheme, it offers physically plug-and-play solution with zero steady state current.

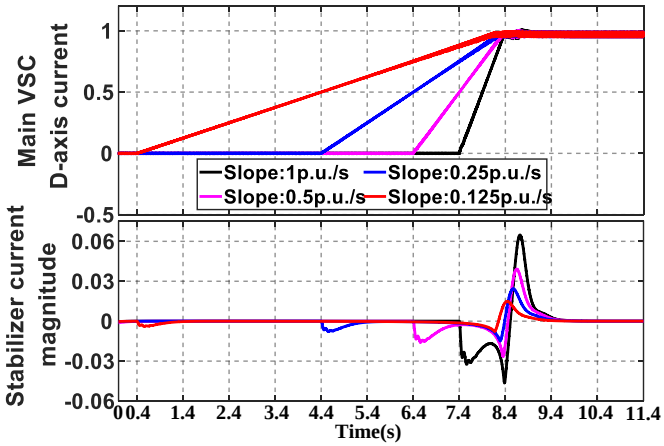


Fig. 16. The comparison of stabilizer transient current

Although the stabilizer is designed to consume zero current at steady state, it does respond to an electro-magnetic transient, i.e. the change of injecting current. To illustrate, a comparison analysis is carried out with various power ramps (of the main VSC), shown by Fig. 16. It can be seen that when a ramp is applied to the main VSC, the peak current of the stabilizer occurs at the stoppage of the ramp. When the ramp is large, at 1 p.u./second for instance, the peak current of the stabilizer can be up to 6.5% p.u. at Time = 8.7 s. When the ramp is slower, such transient current drops as well. The lowest peak can be down to 1.5% p.u. for a ramp of 0.125 p.u./s. This reveals that the size of the stabilizer depends on the intended rate of change of active current/power. By reducing the allowed ramp rate of active power, the size of stabilizer can be limited to a low level.

V. Conclusion

As is summarized in Fig. 17, given a conventional vector control in weak grids, the instability is originated with two causes: 1) non-existence of equilibrium point, 2) negative damping. While a strong var/volt droop is beneficial to secure an equilibrium point with unknown grid strength, it amplifies the negative electromagnetic damping introduced by $dQ/dV<0$. This instability mechanism is independent from tuning of PLL or current loops.

As an auxiliary control, the proposed partial grid-forming loop in q-axis can mitigate the conflict between strong var/volt droop and electromagnetic damping. With a pre-fixed parametric setting (var/volt droop, current regulators, PLL, lead-lag regulator), this scheme can exhaust the physical limit of power delivery in very strong grids as well as extremely weak grids (SCR = 0.9, X/R =10). With appropriate control over electromagnetics, the proposed control can cover the operating region of $dQ/dV<0$ and support FRT when the grid strength is unknown.

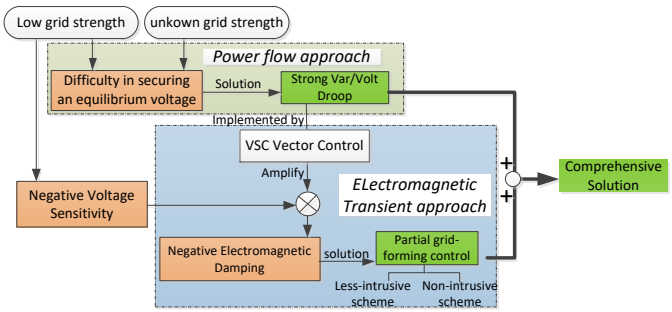


Fig. 17. Instability mechanism and solution

The proposed control also offers an equally effective solution for utilities and/or VSC owners. With such non-intrusive solution, there is no need to physically access those commissioned VSCs. Implemented by an external converter, namely a dedicated stabilizer, storage, STATCOM or any VSC, the proposed control can provide electromagnetic damping service to another VSC nearby with no impact on its set points of power flow. The size of the stabilizer is generally proportional to the rate of change of active power and therefore can be limited by capping the rate accordingly.

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APPENDIX I SYSTEM SPECIFICATIONS

Symbol	QUANTITY	Value
	Base voltage (instantaneous)	Rated phase voltage amplitude
	Base current (instantaneous)	$3/\sqrt{2}\times$ rated phase current amplitude
	Base power	VSC rated power
V_s	grid voltage (p.u.)	1
SCR	short circuit ratio	0.9, 9
X/R	*X/R* Ratio of the grid	10
X_1	VSC Inductance (p.u.)	0.2
R_1	VSC resistance (p.u.)	0.05
Q_C	Shunt compensation (p.u.)	0.1
K	*Var/vol*t droop gain (p.u./p.u.)	22
K_{pd}	proportional gain of d-axis current loop	$200\,\pi L_1$
K_{pq}	proportional gain of q-axis current loop	$200\,\pi L_1$
K_{id}	integral gain of d-axis current loop	$10000\,\pi^2 L_1$
K_{iq}	integral gain of q-axis current loop	$10000\,\pi^2 L_1$
K_{pPLL}	proportional gain of PLL	20π
K_{iPLL}	integral gain of PLL	$100\,\pi^2$
G	gain of q-axis voltage loop (p.u./p.u.)	16
T_2, T_1	constants of lead-lag compensator	0.2, 0.04
f	Frequency (Hz)	50
τ	aggregated delay of VSC control (second)	0.002
	Simulation time step (second)	0.0001
K_{dl}, K_{Ql}	FRT Settings	1, 0.7
i_{cqh}, i_{cql0}	FRT Settings (p.u.)	1, -0.67
V_{thh} V_{thl}	FRT Settings (p.u.)	0.9, 0.1

APPENDIX II COMPARISONS OF VSC CONTROL STRATEGIES IN WEAK GRIDS

Approach	Verified applicable *SCR* in steady state	Robustness against the variation of grid strength	Non-intrusive stabilization availability	Support to FRT
VSM [3]-2011 power synchronization [4]-2010 [5]-2019 [9]-2018 [27]-2020	*SCR* = 1, 2.24, 22.1	high	Yes	No; has to switch to current loops during a severe fault
Frequency damping compensation to PLL [12]- 2019	*SCR* = 1.5	Low	No	Yes
Current error Compensation to PLL [20]-2018	*SCR* = 1~ *X*/*R* = 4, inversion	High	No	Yes
Outer loop: gain scheduling cross-coupling control [25] - 2015	SCR = 1, *X*/*R* = 10, *Q*c = 0.2, bidirectional	Low	No	Yes
Outer loop: active current/power Feed forward [24] -2017	*SCR* = 1, X/R =10, bidirectional	Median	No	Yes
Outer loop: voltage and d-axis current errors compensation to outer power loop [26] -2019	*SCR* = 0.95~ *X*/*R* =10, $P \leq 0.9$ p.u. inversion	Median	No	Unspecified
The proposed "partial grid -forming"	*SCR* = 0.9, 5, 9 *X*/*R* = 10, bidirectional -0.83<*P*≤0.99	High	Yes	Yes

APPENDIX III COMPARISONS OF STABILIZER, STATCOM AND SYNCHRONOUS CONDENSER

	Synchronous Condenser	**STATCOM**	**The proposed external physical stabilizer**
Stabilization with power flow approach	Yes	Yes	No
Stabilization with electromagnetic transient approach	No	Originally no, but can be enabled by embedding the proposed control	Yes
Robust against polarity change of voltage sensitivity	No	Originally no, but can be enabled by embedding the proposed control	Yes
Steady State current rating	High: proportional to reactive power	High: proportional to reactive power	Zero