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A Low Power Sigma-Delta Modulator with Hybrid Architecture

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Abstract: Analogue-to-digital converters (ADC) using oversampling technology and Σ-Δ modulation mechanism are widely applied in digital audio systems. This paper presents an audio modulator with high accuracy and low power consumption by using discrete second-order feedforward structure. A 5-bit SAR (Successive-approximation-register) quantizer is integrated into the chip, which reduces the number of comparators and the power consumption of the quantizer compared with Flash ADC type quantizers. An analogue passive adder is used to sum the input signals and it is embedded in a SAR ADC composed of capacitor array and a dynamic comparator which has no static power consumption. To validate the design concept, the designed modulator is developed in a 180 nm CMOS process. The peak SNDR (signal to noise distortion ratio) is calculated as 106 dB and the total power consumption of the chip is recorded as 3.654 mW at the chip supply voltage of 1.8 V. The input sine wave of 0 to 25 kHz is sampled at a sampling frequency of 3.2 Ms/s. Moreover, the results achieve 16-bit ENOB (effective number of bits) when the amplitude of the input signal is varied between 0.15 V to 1.65 V. By comparing with other modulators which were realized by 180nm CMOS process, the proposed architecture outperforms with lower power consumption.

Keywords: Feedforward modulator, quantizer, SAR, Σ-Δ modulator.

1. Introduction

The rapid development of the Internet of Things (IoTs) demands sophisticated electronics to support the vision of smart cities [1]. High-performance ADCs are frequently used in embedded systems such as mobile phones, iPad, interactive multimedia systems and so on [2][3]. All of these devices require that the conversion chip has a high signal-to-noise ratio (SNR). There are many types of ADCs [4], the traditional ones are pipelined, successive-approximation-register (SAR) and Σ-Δ, which have been developed rapidly in recent years.

A traditional pipelined ADC consists of resistor divider, comparator, buffer and encoder. Its advantage is high A/D conversion speed, however, it suffers from having a low resolution, high

power consumption, high cost and less precision. In contrast to pipelined ADC, an SAR ADC is comprised of a comparator, a D/A converter, a comparison register SAR, a clock generator and a control logic circuit. Its operating principles is to continuously compare the sampled input signal with a known voltage and then convert it into a binary number [5][6]. Due to the matching errors of internal components of SAR ADC, it is widely used in medium and low speed and medium resolution sensor networks. Although SAR ADC [7] has power consumption efficiency, it is difficult to realize high precision due to its structural characteristics and requires additional correction circuits which increases component overhead and power consumption of ADC[8]. To combat with the above defficiencies, the core technologies of Sigma-Delta modulator which are based on the oversampling and noise shaping technologies were proposed to achieve high speed and high precision. Moreover, sigma-delta modulator can easily obtain higher performance in low-order quantization, while the quantizer of Sigma-Delta modulator usually adopts traditional Flash structure, which leads to the higher power consumption of the circuit. As sigma-delta ADC adopts the same technologies as sigma-delta modulator, it reduces the requirements for component matching, saves cost, and is relatively easy to realize conversion accuracy of more than 14 bits, thus being suitable for applications in low power consumption modules[9][10].

Combining the advantages of SAR and sigma-delta ADCs, this paper proposes an architecture that combines SAR and sigma-delta ADCs. That is sigma-delta low power consumption, high precision modulator based on SAR structure quantizer [11]. ADC of this structure can reduce quantization noise in the required signal frequency band through noise shaping and oversampling technology, improving analogue-to-digital converter SNDR (signal to noise distortion ratio). At the same time, due to the use of SAR quantizer, modulator power consumption is also reduced compared with traditional sigma-delta modulator [12].

The structure of this paper can be summarized as follows. Section 2 provides an overview of the improved modulator based on SAR quantizer. This section is followed by the overall circuit structure verification. In Section 4, the key circuit design of the modulator is presented, including the circuit design and optimization of the quantizer module and the improvement of the amplifier. In section 5, the integrator circuit module anlsysis is described and it covers the design of transconductorance operational amplifer ciruict and reference voltage source, while section 6 discusses the pre-circuit simulation and verification. The layout of the chip is presented in Section 7 and the feasibility of this structure is verified in Section 8, followed by the conclusion in Section 9.

2. Improved Σ-Δ Modulator Based on SAR Quantization Structure

The quantization noise is determined by the bit number of the quantizer. The higher the bit number, the smaller the noise[13]. Compared with the single-bit quantization structure, the multi-bit quantization structure not only improves the modulator performance but also reduces the total system power consumption and improves the stability of the system. However, if the quantization bit is too high, the conversion rate will be reduced.

Choosing a five-bit quantization structure and multiple bits can also reduce the performance requirements of the integrator[14]. For a stable integrator, it adopts a second-order or cascade structure as a high-order single-loop structure. Meanwhile, to reduce the power consumption and swing requirement of the modulator, the modulator adopts a low swing circuit structure[15], and the integrator only processes the residual value between the quantization result of the quantizer and

the input signal, which has a small amplitude. The noise shaping effect can be achieved by using the second-order integrator structure, and the stability of the system also remains good.

Hence, a second-order five-bit modulator structure is proposed, as shown in Figure 1. The integrator in the modulator is formed by a discrete switched capacitor and transconductance operational amplifier, and the discrete switched capacitor makes the integrator insensitive to jitter caused by clock[16]. Because the swing of the integrator is affected by the swing of the operational amplifier, the transconductance operational amplifier generally adopts sleeve structure. At the same time, the active adder which adds the feedforward result of the integrator, the input signal is replaced by the passive adder, which further reduces the power consumption of the system[17].

In order to realize low power consumption circuit, there are many existing structures and schemes for Σ-Δ modulator module such as [18] where the Σ-Δ modulator based on SAR quantization structure is reported. It adopts a 2nd order integrator with 4-bit quantizer architecture and conducts post-simulation on the circuit behaviour, circuit itself, and at the layout level, which verifies the feasibility of the scheme.

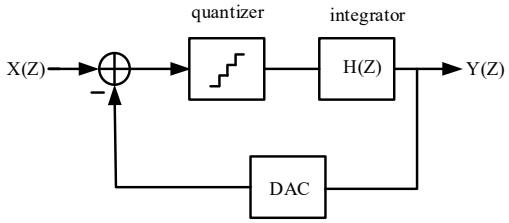


Figure 1. Sigma-delta ADC system block diagram

Fig. 1 shows a Sigma-delta ADC system framework which consists of a reusable 5-bit SAR ADC and two integrators. The input signal X(Z) first enters the quantizer for five-bit quantization. The quantization result of each bit is fed back to the input signal port through the D /A converter, and subtraction is performed with it. Therefore, the voltage processed by the quantizer is the difference between the quantization result and the input signal, and the power consumption is lower than that of the comparator. After five-bit quantization, the difference between the final quantization result and the input signal is sent to the integrator. The integrator only deals with the quantization error, and the integrated result Y(Z) is sent back and added in the next quantizer sampling to obtain higher conversion accuracy.

In a traditional feedforward modulator, an amplifier is required to form an active analogue adder [19] at the ADC input node, which increases the power consumption of the modulator. In this paper, a multi-bit feed-forward [20] ADC without active analogue adder is adopted to overcome the power issue. The passive adder embedded in SAR ADC is implemented by using a separate capacitor array [21] and a dynamic comparator [22]. The integrator is realized by a ring amplifier without static current. The capacitor array of the SAR ADC samples the input signal, and the capacitor C_S samples the integrator output. After this sampling operation, the SAR ADC quantizes the sampled signal in a binary search mode and outputs it through DAC. Finally, a residual voltage V_{RES} is generated on the top plate of the capacitor array.

$$V_{RES}(z) = V_{IN}(z) - V_{DAC\_OUT}(z) \quad (1)$$

where V_{IN} is the input sample signal and V_{DAC_OUT} is the output voltage of the DAC. The residual voltage is then processed by a two-stage integrator in the integration phase of the ADC.

Whereas the digital output of the current sample V_{DAC_OUT} (k) can be expressed as:

$$V_{DAC\_OUT}(z) = V_{IN}(z) + V_{RES}(z) * H(z) + Q(z) \quad (2)$$

where H(z)is the transfer function of the integrator, and Q(z)represents the quantization noise and comparator noise of the ADC. Substituting VRES of equation (1) into equation (2), the following system transfer function (3) is obtained.

$$V_{DAC\_OUT}(z) = V_{IN}(z) + 1/(1 + H(z))Q(z) \quad (3)$$

The signal transfer function and noise transfer function can be obtained from equation (3), as shown in equation (4) and(5).

$$STF(z) = z^{-2} \quad (4)$$

$$NTF(z) = (1 - z^{-1})^2 \quad (5)$$

Where STF is a signal transmission function and NTF is a noise transmission function. It can be seen from equation (5) that NTF is a high-pass function, and the system suppresses the noise at low frequency, thus achieving a higher signal-to-noise ratio in bandwidth.

In the proposed architecture, SAR quantizer is not only used to realize the quantization of modulator but also used to realize the summation of the input signal and feedback signal in the traditional modulator. In this way, the sampling capacitance of the first integrator in the modulator can be multiplexed with the capacitance of SAR quantizer, thus reducing the power consumption and area of the modulator[23]. Another advantage is that multiplexing technology provides a signal feed-forward path for the modulator, forming a feed-forward modulator structure, which makes the output swing of the integrator independent of the input signal of the modulator, thus improving the overload rate of the modulator. Therefore, the requirements for amplifiers in integrators are greatly reduced, allowing smaller open-loop gain and lower bandwidth. Because the input signal of the modulator is directly sampled to the capacitor array of the quantizer without going through the integrator, the sum swing of the integrated output is very small, and the analogue adder with too large swing is not needed, which reduces the design difficulty of the modulator.

Based on multiplexed SAR quantizer and feedforward technology, the proposed modulator can handle the input signal range close to full amplitude. Therefore, the small capacitance can meet the requirements of circuit thermal noise[24]. The quantizer only needs half of the clock cycle to sample the output of the integrator, and the small C_S can greatly reduce the requirements for the second-stage integrator.

3. The overall circuit design of the modulator

The circuit schematic diagram of the multi-bit modulator is shown in Fig.2. It consists of an integrator, a quantizer, a clock circuit, a capacitor array, a DAC and other units. The main circuit of the modulator is composed of a quantization part and integration part. The clocks in the circuit are the integrator clock and the SAR quantizer clock. The working timing of the whole modulator is shown in Fig.3. In the sampling phase (φ1/φ1d) which is the sampling clock of the integrator, the quantizer requires to complete sampling and digital conversion. In the integration phase (φ2/φ2d) which is the integration clock of the integrator, the quantization result is fed back to the input via DAC and subtracted from the input signal. CLKC is the control clock of quantizer comparator, which is generated by the internal circuit of the quantizer. This scheme focuses on the low power consumption design of amplifiers and quantizers[25]. In the imaginary frame of Fig. 2, VREFP and VREFN are positive and negative reference voltages respectively, while VCM is common-mode voltage, Vin and Vip are input signals, and CLKC is the control clock of the comparator. To obtain the required VREFP=1.8V, ADC needs 16 cell capacitors. The clock switch φs is closed in the sampling stage of the quantizer. Meanwhile, φ2 is closed during the whole working period of the

quantizer and is turned off when the integrator results are sampled. φ1 is closed when the quantizer samples the integrator result. Vfp and Vfn are the integration results of integrator feedforward to the positive and negative terminals of the quantizer.

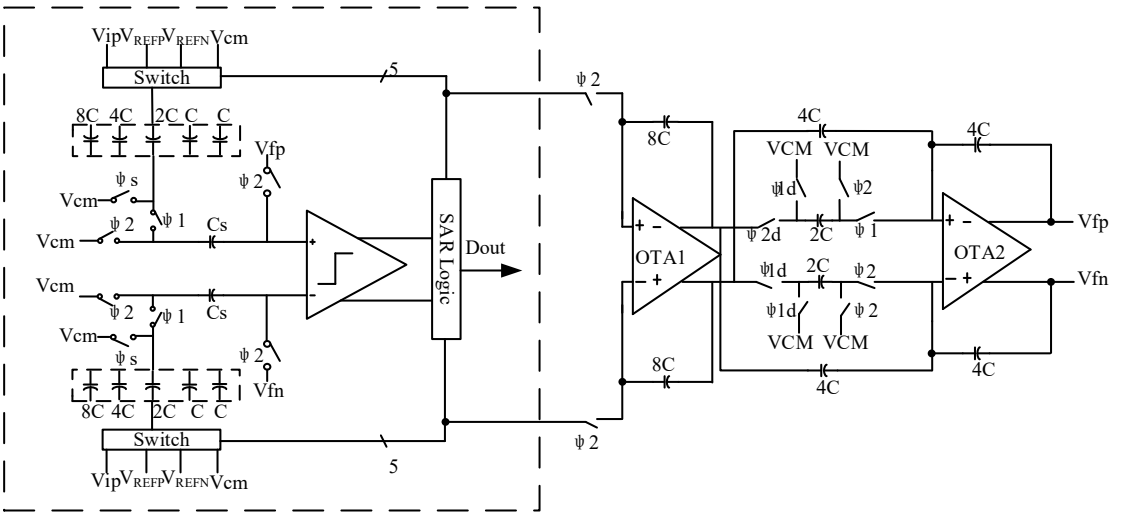


Figure 2. General circuit structure diagram.

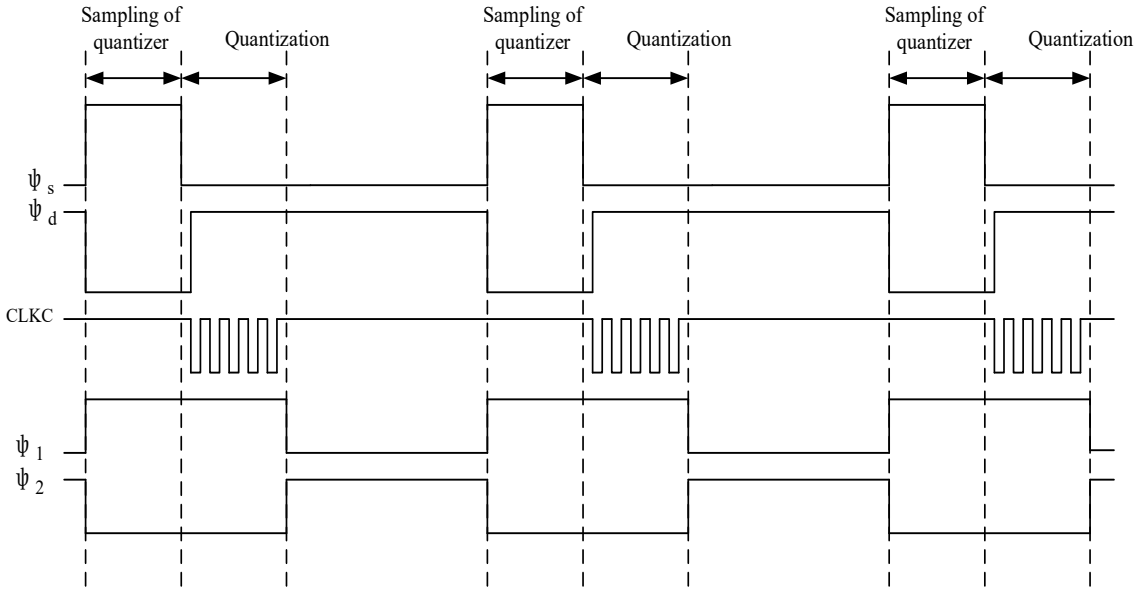


Figure 3. Modulator timing diagram. Where φs is the quantization sampling clock, φd is the quantization conversion clock, and Clkc is the comparison clock of the SAR comparator[26].

4. Quantizer Circuit Module Analysis and Optimization Design

Flash ADC is usually used as a quantizer in multi-bit quantization modulator. Flash ADC requires multiple comparators and also has the problems of matching circuit and large dynamic power consumption[27]. If a pre-amplifier is added at the front end of the comparator, static power consumption will be increased. In order to address the above-mentioned problems, a scheme of the modulator using 5-bit SAR ADC as quantizer is proposed. SAR ADC has no static power consumption, and the precision is 5 bits, which has no problem of matching circuit. The sampling frequency of the designed Δ-Σ modulator is 3.2 Ms/s. At this sampling rate, 5-bit SAR ADC has lower power consumption compared with Flash ADC. In addition, the SAR quantizer structure is used to implement the addition of the adder output signal and the input signal. The adder adds the

feedforward signals of the integrator. The output swing of integrators is very small, which leads to a very small output swing of the adder and therefore greatly reduces the requirements for the amplifier.

The working process of the quantizer is divided into sampling [28] and digital conversion. Both of these two processes are completed in the sampling phase (φ1/φ1d) of the integrator. To avoid using an external high-frequency clock, the comparator clockin within SAR quantizer is generated by the SAR internal circuit, and the specific operation timing is shown in Fig.3. In the sampling phase (φs), MSB sampling capacitor is connected to VREFP, and the lower plate of the other capacitors is connected to VREPN. The SAR capacitor array samples the output of the integrator while the input signal is sampled to a capacitance equivalent to the entire SAR capacitor array. After the sampling is completed, the sampling switch is turned off to start digital conversion. The capacitor upper plate sampling the input signal is connected to the common mode VCM, and the SAR quantizer obtains the conversion result through successive comparison[29]. At the same time of completing the conversion, the SAR quantizer receives the addition of the adder output signal and the input signal. After the digital conversion process is completed, the SAR quantizer outputs the conversion result through control logic.

4.1 Sampling module

Input signal sampling is mainly realized by gate voltage bootstrap switch circuit, capacitor array and sampling common-mode voltage. Compared with the transmission gate and MOS switch, the gate voltage bootstrap switch is more stable and has lower transmission loss, but the chip area is large, so it is only used in sampling. There is no need for 32 unit capacitors, but only 16 unit capacitors.

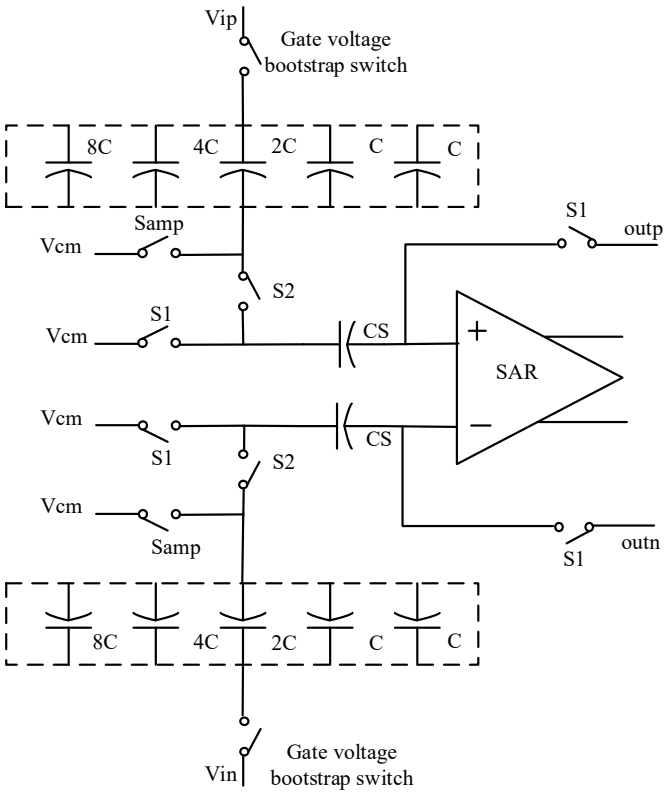


Figure 4. Quantizer sampling circuit

In the quantizer sampling input signal and conversion stage, S1 is always open and S2 is always closed. Samp and the gate voltage bootstrap switch are switched off after completing sampling. When sampling the output of the integrator, switch S1 is closed and switch S2 is open, the upper plate of capacitor C_S is connected to a common-mode voltage, and the lower plate is connected to integrator output voltages outp and outn. After sampling the integrator, the switch S1 is turned off, and the input signal is sampled by the quantizer. The switch S2 is closed, and the voltage value of the upper plate of the capacitor C_S becomes the sampled voltage values Vin and Vip, and the lower plate is suspended. By combining the sampling structure of the input signal with the sampling structure of the output of the integrator, the quantizer sampling circuit is formed as shown in Fig. 4.

This part mainly optimizes the circuit structure in the following two aspects. First, in order to reduce the power consumption and chip area of the whole circuit, capacitance multiplexing circuit is adopted. Its structure can reduce the number of capacitors and by choosing a relatively large capacitor size, it makes the capacitor matching better. In the second aspect, proper logic control circuit is adopted in the logic control of quantizer. As shown in Fig. 4, the logic levels of the two points on the left side of the CS capacitor are controlled to maintain a constant common mode level in the whole quantization process, thus reducing errors caused by inconsistent common-mode levels.

4.2 SAR comparator module

SAR comparator adopts differential structure. It compares the analogue signal obtained by the sampling capacitor with the analogue signal obtained by adding the integrator output and input signal, to finally obtain a digital signal. At the same time, the comparator adopts a dynamic latch structure, which further reduces the power consumption of the system [30]. The latch structure saves the comparison result every time and then resets the comparator state to realize multiplexing. The multiplexing function is completed by the output of the comparator itself cooperating with the external clock circuit. After the output of the comparator is generated, the comparator stops working and reset to prepare for the next comparison. The latch function is realized by SAR logic control structure, and the quantized values obtained by five comparisons are saved one by one and output in parallel [31]. Compared with the traditional comparator, SAR comparator adopts PMOS design and achieves multiplexing function, and its corresponding schematic diagram is shown in Figure 5.

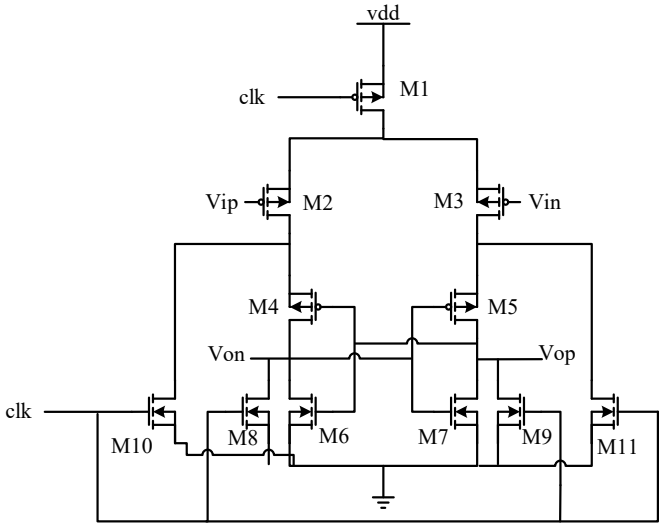


Figure 5. SAR comparator structure

In Fig. 5, Vin and Vip are the positive and negative input ports of the comparator, and Von and Vop are the positive and negative output ports of the comparator. PMOS transistors M2 and M3 are differential input stages connected with input signals. PMOS transistors M4 and M5 have positive feedback structure, M6 and M7 realize common source amplification, and NMOS transistors M8, M9, M10 and M11 are used for resetting. When the clk signal is at a high level, it is reset. At this time, NMOS transistors M8, M9, M10 and M11 are turned on, and M8 and M9 discharge the output ports, i.e. Von and Vop at the same potential and turn on the PMOS transistors M4 and M5. M10 and M11 make the drain potentials of M2 and M3 which is equal to realize reset. This can be achieved by comparing M2 and M3 when the clk signal is low which is equivalent to the terminal volage of Vip greater than the terminal voltage of Vin. At this time, the channel width is opened by M2 which is smaller than M3, and the drain potential of M3 is pulled up quickly, reaching a high level first, so that M4 is turned off and the drain potential of M2 is no longer changed. Then Vop outputs a high level and Von outputs a low level to complete the comparison[32].

5. Integrator Circuit Module Analysis and Optimization Design

Combining the designed transconductance operational amplifier with the switched capacitor, the circuit structure outside the imaginary frame in Figure 2 is obtained. Under the control of the clock switch, the sampling and integration of the integrator are completed. In the figure, φ 2/φ 2d is an integral switch, and φ1/φ1d is a sampling switch, both of which are transmission gates controlled by two clocks that do not overlap each other in which φ1/φ1d is closed and φ2/φ2d is open. During this period, the quantizer performs sampling and conversion, that is, sampling by the first integrator. Meanwhile, the second-stage integrator samples the results of the first-stage integrator where φ2/φ2d is closed and φ1/φ1d is open. During this period, the quantization result of the quantizer is fed back to the input terminal through DAC and subtracted from the input signal and sent to the integrator. The first-stage integrator integrates the difference signal, and the second-stage integrator integrates the first-stage result, that is, the output of the integrator is delayed from the input signal by the input signals of two quantizers.

The main components of integrator are transconductance operational amplifier and discrete switched capacitor. Traditional integrators generally adopt feedback structure, and input signals

need to be added before each stage of integrator input, resulting in a complex circuit structure. In order to further reduce the power consumption of the integrator, a feedforward structure is adopted. This architecture only needs to add the input signal before the first stage input of the integrator and is insensitive to the distortion of the operational amplifier in the integrator. As the swing is small where the swing of each operational amplifier is about 200MV, it optimizes the current demand of the amplifier and hence reduces power consumption. Because SAR ADC is used as the quantizer and the integrator processes the residual difference between the quantization result and the input signal, the first integrator needs no sampling capacitor, which further saves the chip area and hence elaborates the optimization of this part of the circuit.

5.1Design of transconductance operational amplifier circuit

According to the principle explanation of transconductance operational amplifier, the circuit result shown in Figure6 is designed. In the figure, except M3, M4, M12 and M13 are NMOS transistors, others are PMOS transistors. MOS transistors M1 and M2 are used as differential pairs, M3 and M4 are used as active loads, and M5 provides a constant current source to complete the differential input stage. The source follower is composed of M6 and M8, M7 and M9, and provides static bias for M10 and M11 at the same time. The VGS of M6 and M7 determines the DC voltage difference between the gates of output stages M10 and M12 and M11 and M13. by adjusting the width-length ratio of M6 and M7, the output offset can be guaranteed to be zero. Resistors and capacitors form a frequency compensation network, which is bridged between the input and output ends of the output amplifier stage.

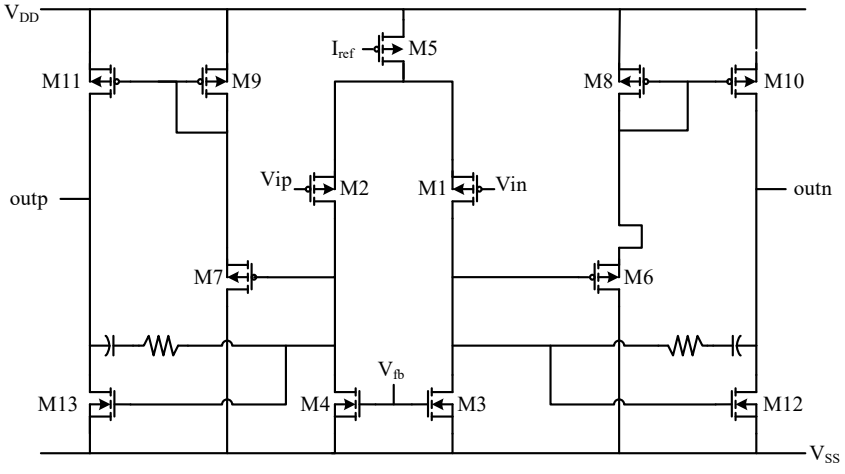


Figure 6. Schematic of Transconductance Operational Amplifier

5.2 Design of reference voltage source

Fig. 7 is a circuit design diagram of a reference voltage source. As can be noticed, the sources and drains of PMOS transistors M5, M10 and M11 are connected to form a capacitor, which makes the matching design of M1~M4 stabilize the current of the current mirror. M6~M9 and capacitors together stabilize the supply current of M1~M4. PNP transistor VT_2 is formed by connecting four VT_1 in parallel to ensure the proportion.

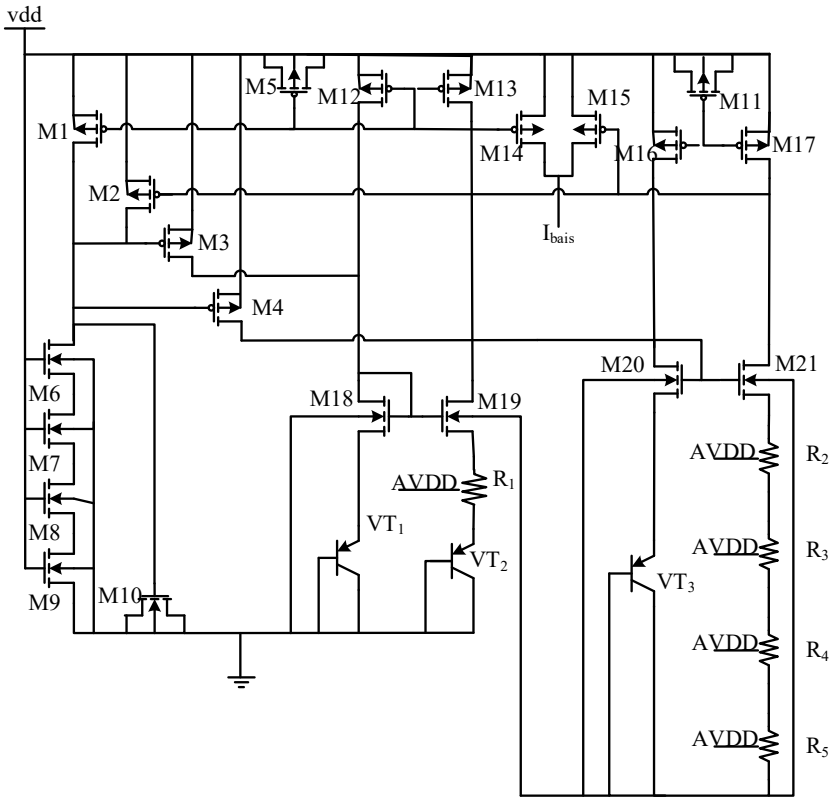


Figure7. Circuit diagram of the reference voltage source

6. Pre-circuit Simulation and Verification

According to the proposed design concept, each module of the modulator is designed separately. In this section, the functional simulation of the designed circuit is carried out by using Cadence spectre simulation software to verify the design scheme and the feasibility of the circuit. The designed clock circuit is integrated and packaged, and the whole clock signal is generated by an external clock, and the clock control timing of the modulator is simulated. The full simulation circuit is shown in Figure 8. As can be seen, the voltage amplitude of CLK is set to 1.8V, the period is 312.5ns, the rising and falling times are both 900ps, and the pulse width is 155ns. The clock signal label in the figure corresponds to the design.

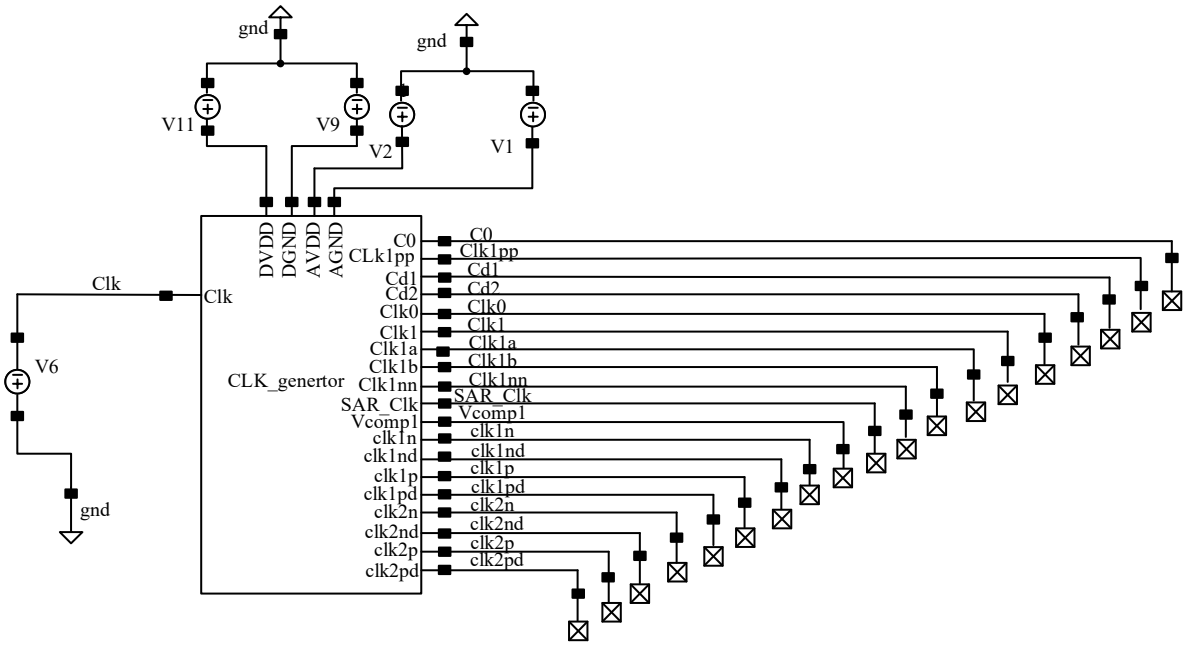


Figure 8. Clock circuit simulation design

The simulation results can be divided into two parts, the first part is quantizer sampling clock, quantizer switching clock and circuit switching clock signal, as shown in Figure 9. The second part is integrator clock, quantizer sampling clock and DAC transmission clock, are depicted in Figure 10. Through the simulation results of the clock circuit, it can be concluded that the clock unit design of each module of the modulator is reasonable, and the clock control signal meets the timing function of each module of the modulator.

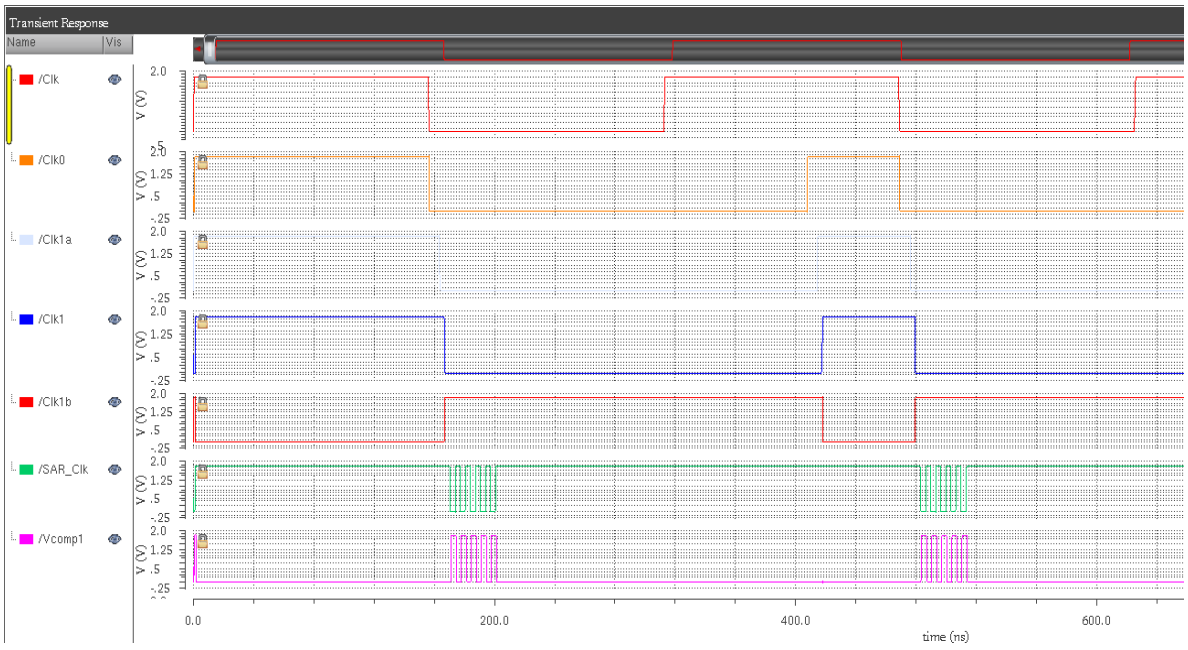


Figure 9. Simulation diagram of the overall clock of quantization part

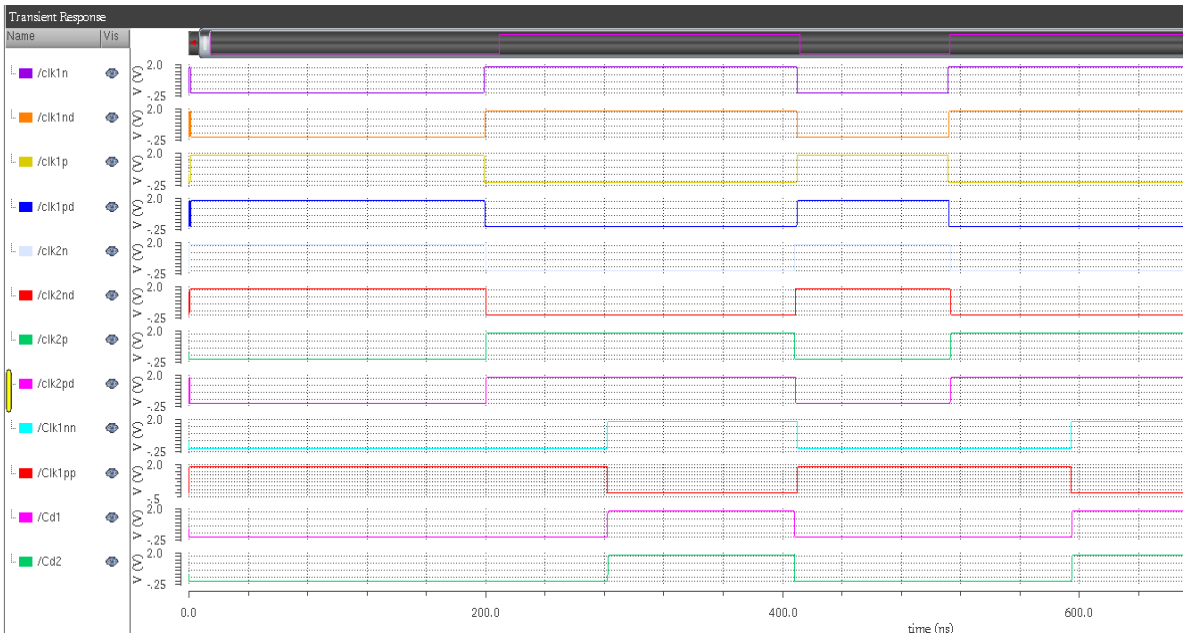


Figure 10. Overall clock simulation diagram of the integral part

Through the simulation and analysis of the modulator clock unit, the correctness of the overall timing logic of the designed modulator is verified. After each module unit of the circuit is designed, the overall circuit of the modulator circuit is simulated. The simulation circuit is shown in Figure 11, and the signal label in the figure is given in Table 1. Since CLK2p and CLK1p are the integrator integration phase and sampling phase clocks respectively, only one of them will be explained below.

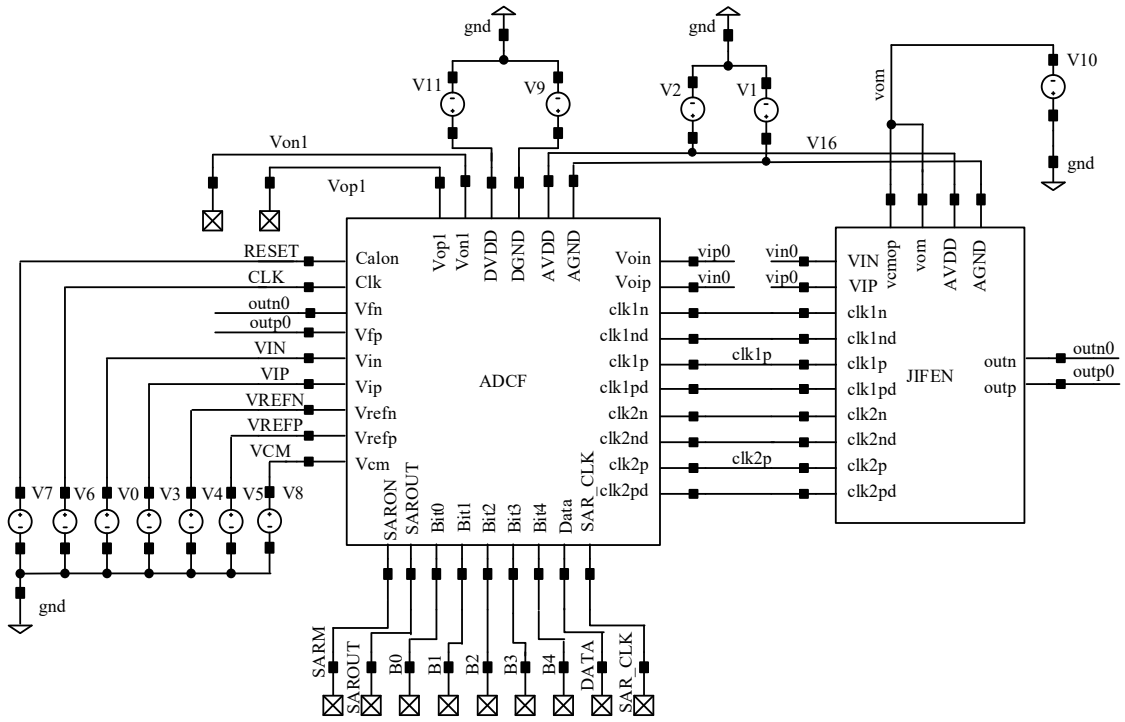


Figure 11. Overall simulation structure diagram of the modulator

Table 1.Data Description Table of Modulator Structure Diagram

Name	Representative significance	Name	Representative significance
RESET	Modulator reset signal	CLK	Total clock input signal
outn0	Negative feedforward of integrator	VREFP	voltage reference
outp0	Integrator forward feed	VCM	common-mode voltage
VIN	Negative input signal	VREFN	Terminal voltage at ground
VIP	Positive input signal	Von1	DAC negative feedback
B0~B4	Five-bit quantization	Vop1	DAC positive feedback
DATA	Quantization result output clock	vip0	Negative input of integrator
SARIN	Comparator negative signal	vin0	Positive input of integrator
SAROUT	Positive signal of comparator	clk2p	Integrator integrated phase clock

As Cadence spectre takes a long time to simulate the time above microsecond level, and can't simulate the RESET signal in a short time, the RESET is not verified here, so that its grounding has no effect on the circuit. This simulation mainly verifies the logic output of the main signal of the modulator and further confirms the logic function of the modulator. The overall simulation is shown in Figure 12.

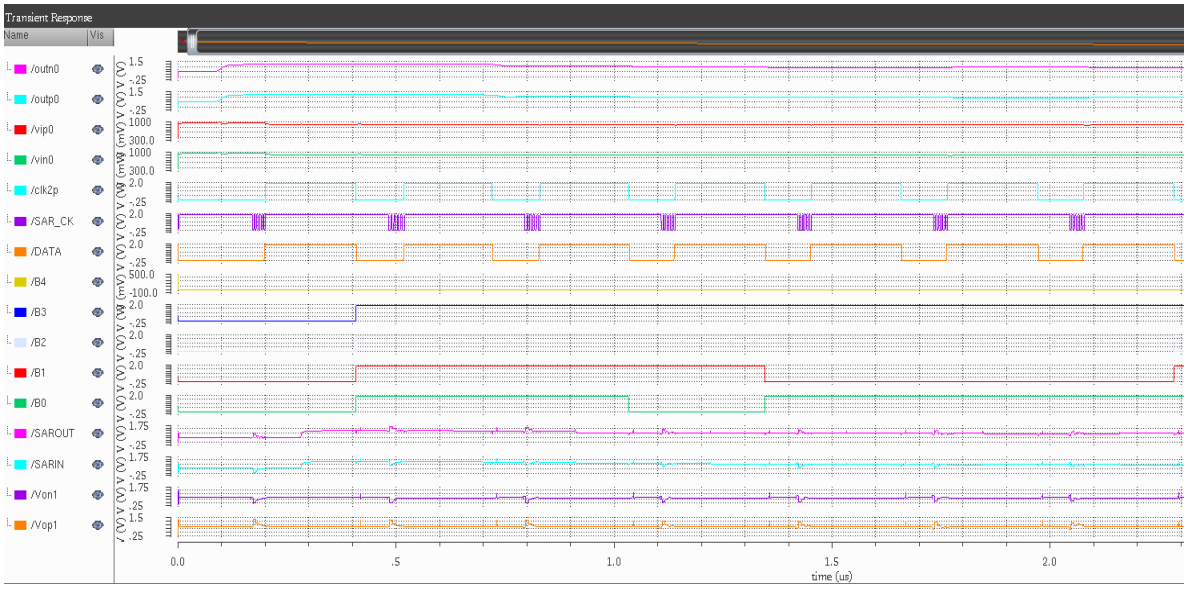


Figure 12.overall function simulation diagram of the modulator

By analyzing the simulation results, it can be concluded that after being processed by an integrator, the voltage amplitude of the comparator entering the quantizer is increased to a certain extent, and the voltage applied at both ends of the comparator is appropriately increased, which

makes the comparator more stable and also improves the accuracy. The quantizer also works normally under the action of the clock circuit, and the five-bit quantization output of the quantizer and the sampling clock of the quantizer output meet the predetermined output result. The main input/output signals and working clocks of the quantizer and integrator in the simulation diagram correspond to the working principle of the modulator described in the previous section, which verifies the rationality of the proposed working principle of the modulator.

7. Layout Design

The layout drawing and verification are completed using SMIC 180nm process. A bootstrap switch is used at the input of ADC to reduce the nonlinearity of on-resistance. The chip makes use of several capacitor units to form capacitors and achieves accurate proportional matching of coefficients. The differential structure of the capacitor array is completely symmetrically distributed on both sides of the comparator, which is used to improve the overall anti-noise capability of the circuit [33]. The digital control logic is uniformly placed at the back end of the chip, and the digital part and the analogue part are effectively isolated to reduce the interference of digital noise on the front-end analogue module. The overall design structure ensures the symmetrical arrangement of analogue parts of the ADC.

The test chip is fabricated with 180nm CMOS process. The design does not require any high precision capacitance and low threshold voltage process. Fig. 13 shows a micrograph of the chip. The overall chip area is 1360μm²×1360μm² and the core area is 966μm²×748μm².

Table 2.Parameter comparison

	Power Consumption (mW)	Frequency (MHz)	FOMs (dB)	CMOS Technology (μm)	SNDR (dB)	OSR	AREA (mm^2)
[34]	14.7	8.0	172.2	0.18	105.9	128	-
[35]	8.1	-	-	0.18	81.0	-	-
[36]	6.65	960	150.7	0.028	-	48	0.015625
[37]	12.7	0.64	165.0	0.35	-	320	11.48
[38]	475	2.5	-	0.25	100.0	-	-
[39]	18.5	-	-	0.65	72.3	-	0.25
[40]	5	256	160.4	0.13	74.4	64	0.33
[41]	16	600	166.0	0.090	78	30	0.36
[42]	3.2	1	165.6	0.35	100.2	250	3.8
This work	3.65	3.2	169.4	0.18	106	128	0.56

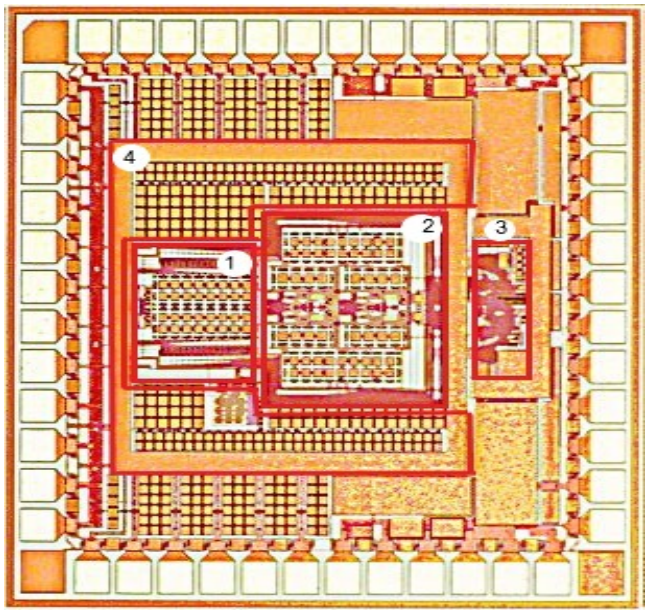


Figure 13. Modulator Chip Layout where (1) the multiplexed sampled capacitor array, (2) the 2nd order integrator, (3) the comparator and (4) the power supply

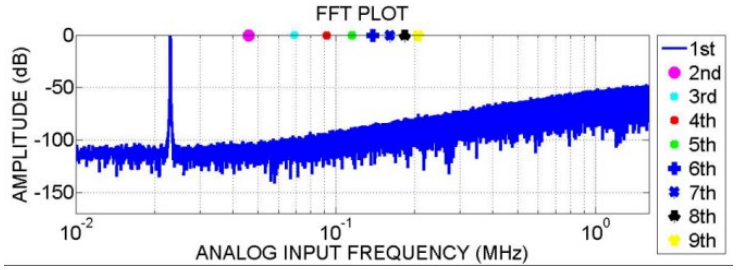
8.Chip Testing and Comparison of previous works

The performance comparison of the presented work with other published works can be found in Table 2. As can be seen, the designed modulator chip has lower power consumption and better performance against others. By measuring the voltage and current on the PCB of the Chip, the test power consumption of this design chip is found to be 3.654mW. However, there are some losses from the auxiliary devices and power supply on the testing board, which is resulted from the high test data. If other device losses and power losses are not considered, the actual power consumption of the chip is less than 2.5mW. Reference [18] adopts a 2nd order 4-bit quantizer structure which has a simulated power consumption of 69μW and lower than the proposed architecture. However, it adopts 65nm process and the simulated data doesn't consider the power and circuit loss, so it cannot be compared on the same level. Meanwhile, the SNDR value of the proposed architecture is 106dB which demonstrates the obvious advantages of the proposed architecture.

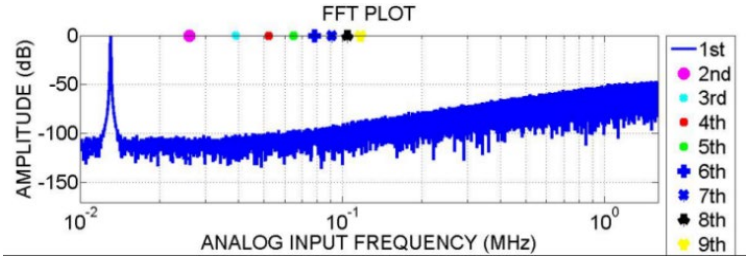
By using 3.2 MS/s sampling rate, the output power spectrums with the oversampling ratio of 128 of the delta-sigma ADC at three selected differential input sine waves, i.e. 5.1K, 12K and 23K are shown in Fig.14. In the current architecture, when the signal bandwidth (25K) is fixed, the oversampling ratio(OSR) is determined by the expected precision of the modulator and the highest sampling rate of the sampling circuit. For quantization noise, the higher the oversampling ratio is, the higher the signal-to-noise ratio (SNR) can be achieved by the modulator. However, the final accuracy of the modulator depends on the upper limit of the accuracy that can be realized by the sampling circuit, thus limiting the sampling rate of the modulator and ultimately affecting the oversampling ratio of the modulator.

The results confirmed the consistent performance of the output power spectrums across the desired operating input sine wave frequency band from 0 to 25 KHz. To evaluate the corresponding SNDR performance, Fig.15 illustrates the measured SNDR against the input signal frequency. It can be seen that the peak SNDR is 106dB at 3kHz and the lowest SNDR is 101 dB at 25 KHz. Figure 15 shows the SNDR point connection diagram of different integer signal frequencies under the same signal amplitude in the actual test. As can be seen, SNDR decreases with the increase of signal

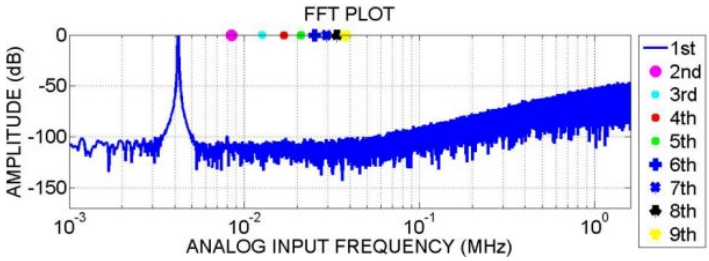
frequency due to the presence of clock jitter and nonlinear factors. The data weighted averaging (DWA) is used in the feedback capacitor array, which reduces the harmonic components such as second harmonic and third harmonic caused by capacitor array mismatch, thus improving the overall dynamic range. The test results show that the dynamic range can exceed 100dB. The total power consumption of the chip is 3.654mW. The supply voltage of both analogue and digital circuits is 1.8V and the FOMs is 169.4 dB.



(a) Spectrum Output of Modulator at 23K Input Frequency



(b) Spectrum Output of Modulator at 13K Input Frequency



(c)Spectrum Output of Modulator at 5.1K Input Frequency

Figure 14. Output Power Spectrum of Modulator at Different Input Frequencies.

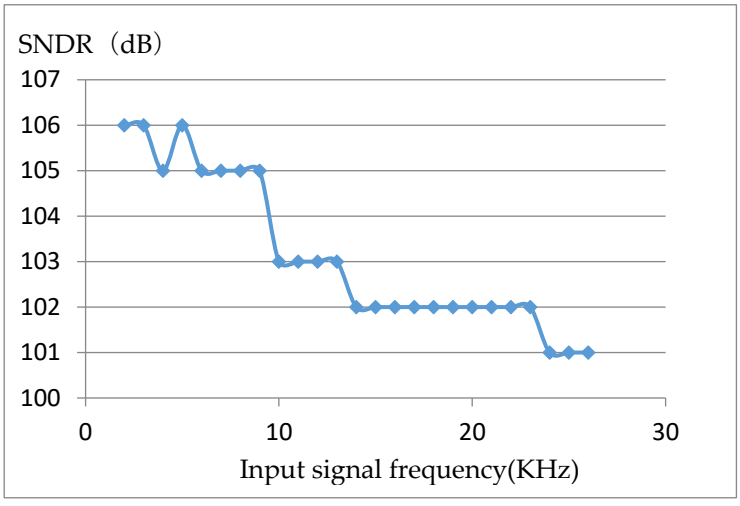


Figure 15. Measured relationship between input signal frequency and SNDR.

9. Conclusions

Employing a 2nd order 5-bit quantization structure, a Σ-Δ modulator with low power consumption and high-resolution modulator scheme was proposed for analogue-to-digital converters. Through optimizing the circuit structure, a reusable quantizer sigma-delta modulator based on SAR structure was presented. Under the condition of 128 oversampling rate, it demonstrates a resolution of 16 bits, the power consumption of 3.654 mW and FOMs of 169.4 dB for 0 to 25 kHz analogue signals, which has higher data conversion efficiency and higher optimal value. These results confirmed that the modulator of this structure meets the requirements of low power consumption and high precision for audio applications. The whole modulator was realized by SMIC single-layer polysilicon 6-layer metal 180nm CMOS process where the working power supply voltage was 1.8V. In comparison with other reported modulators realized by 180nm CMOS process, the proposed architecture offers several advantages and is far superior retrospectively with lower power consumption.

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References

1. SQ Khan, A Ghani, M Khurram, " Frequency-dependent synaptic plasticity model for neurocomputing applications", International Journal of Bio-Inspired Computation, 16 (1), 56-66, 2020.
2. A Ghani, CH See, V Sudhakaran, J Ahmad, R Abd-Alhameed, "Accelerating Retinal Fundus Image Classification Using Artificial Neural Networks (ANNs) and Reconfigurable Hardware (FPGA)", Electronics 8 (12), 1522, 2019.
3. A Ghani, "Healthcare electronics—A step closer to future smart cities", ICT Express 5 (4), 256-260, 2019.
4. Federico N. Guerrero,Enrique M. Spinelli. ''A simple encoding method for Sigma-Delta ADC based biopotential acquisition systems,'' Journal of Medical Engineering & Technology., vol.41,2017.
5. Cao Tianlin.Han Yan.Zhang Shifeng. et al.'' A Low-power High-resolution Band-pass Sigma-delta ADC for Accelerometer Applications,'' Semiconductor technology and science., vol.17, pp. 438-445, 2017.
6. Hongmei Chen.Li Wang.Ting Li.Lin He and Fujiang Lin."A 0.6V 19.5μμW 80dB DR ΔΣ Modulator with SA-Quantizers and Digital Feedforward Path,"Journal of Circuits, Systems and Computers,vol. 26, no. 07, 2017.
7. Digita Behnam Samadpoor Rikan. Hamed Abbasizadeh.Sung-Han Do. Dong-Soo Leeand Kang-Yoon Lee. "Digital Error Correction for a 10-Bit Straightforward SAR ADC," IEIE Transactions on Smart Processing and Computing, vol. 4, no. 1, February 2015.
8. Maysam Ghovanloo,Hangue Park."A 13-bit noise shaping SAR-ADC with dual-polarity digital calibration,"Analog Integrated Circuits and Signal Processing, vol.75, no. 3, pp. 459-465, 2013.
9. Y. Yang."Digital Post-Calibration and Design of a 5 bit 1.5GHz Flash ADC,"Journal of Beijing University of Technology,vol. 32, no. 9, pp. 932-936, 2012.
10. Akira Matsuzawa.Masaya Miyahara."SAR+Δ-Σ ADCs with open-loop integrator using dynamic amplifier,"IEICE Electronics Express.
11. Deng Yuqing.Tang Ning.Zhang Cheng and Chen Ke."Design of an over-sampling digital filter for high-resolution Σ-ΔDAC," 2011 International Conference on Electric Information and Control Engineering, Wuhan,pp. 5817-5820, 2011.

12. Diwakar Krishnamoorthy.“Low voltage Delta-Sigma Modulator with full range and unidirectional output,”IEICE Electronics Express.,vol.12, no.3, pp.1, 2015.
13. A. Dendouga,M.L. Hafiane,N. Bouguechal,S. Oussalah,S. Barra,S. Kouda. ‘’Analog design-for-testability technique for first-order sigma delta ADC,’’ Measurement.,vol.46,2013.
14. Tao Sha.Rusu Ana.“A comparative design study of continuous-time incremental sigma-delta ADC architectures,”International Journal of Engineering Research and Applications., vol.44,no.12,pp.150-153, 2016.
15. Frick.Dadouche.Berviller.‘’Adjustable Nyquist-rate System for Single-Bit Sigma-Delta ADC with Alternative FIR Architecture,’’ International Journal of Electronics., vol.103, no.9,2016.
16. C.Pan,H.San,“A low-distortion delta-sigma modulator with ring amplifier and passive adder embedded SAR quantizer,” ISPACS.,vol.25,no.6,pp. 299–302, Nov,2015.
17. Qi Fan.Ning Ning.Qi Yuand Da Chen.“A High-Performance Operational Amplifier for High-Speed High-Accuracy Switch-Capacitor Cells,” Journal of electronic science and technology of china ,vol. 5, no. 4, 2007.
18. Radjen, D., Anderson, M., Sundström, L. et al. A low-power 2nd-order CT delta–sigma modulator with an asynchronous SAR quantizer. Analog Integr Circ Sig Process 84, pp.409–420 ,2015.
19. Y. Lim ,M. Flynn.“A 100 MS/s, 10.5 Bit, 2.46 mW Comparator- Less Pipeline ADC Using Self-Biased Ring Amplifiers,” IEEE ISSCC 2014 Dig of Tech.,vol.30, no. 11, pp. 202–203, Feb, 2014.
20. Y.Zhang, H.YangG, Wei Jinbao.“A High Precision CMOS Opamp Suitable for ISFET Readout,”Journal of Semiconductor., vol.22,no. 4 , pp.686-692, 2008.
21. T. B. Cho, D. Kang, Chun-Huat Heng and Bang Sup Song. "A 2.4-GHz dual-mode 0.18-/spl mu/m CMOS transceiver for Bluetooth and 802.11b," IEEE Journal of Solid-State Circuits, vol. 39, no. 11, pp. 1916-1926, Nov. 2004.
22. ZeinabHojati,MohammadYavari.” An NTF-enhanced incremental ΣΔ modulator using a SAR quantizer,” Integration ,vol.55, pp. 212-219,September 2016.
23. Tao Yin,Fubin Xin,Fanyang Li,Fei Liu,Haigang Yang. ‘’A hybrid Sigma-Delta modulator with reusable SAR quantizer,’’ IEICE Electronics Express.,vol.16,no.3,2019.
24. Li Di,Qian Xuejun,Li Runze,Fei Chunlong,Jiang Laiming,Chen Xuyuan,Yang Yintang,Zhou Qifa. ‘’High Resolution ADC for Ultrasound Color Doppler Imaging Based On MASH Sigma-Delta Modulator,’’ IEEE transactions on bio-medical engineering., vol.67,no.5,pp. 1438-1449, 2020 .
25. S.Ma, Y.Han Yan,Huang Xiaowei,Yang Li Wu.“A High-Performance, Low-Power ΣΔ Modulator for Digital Audio Applications,”Journal of Semiconductor., vol.15, no.10 ,pp.2050-2056 ,2008.
26. Mohammad reza farsi,Khalil monfaredi. “Design and simulation of high precision second-order sigma-delta modulator for bluetooth applications,”Journal of Engineering Science and Technology vol. 13, no. 10,pp.3071 – 3079 , 2018.
27. Zhongyi Fu.Xian Tang.Kong-Pang Pun.“Use DAS algorithm to break through the device limitations of switched-capacitor-based DAC in an ADC consisting of pipelined SAR and TDC,” Solid State Electronics., vol. 16, no.3, pp.119-125,2017.
28. AtaKhorami.RoghayehSaeidi.ManojSachdev.MohammadSharifkhani.”A low-power dynamic comparator for low-offset applications” Integration Volume 69, pp. 23-30, November 2019.
29. J. Shen et al., "A 16-bit 16MS/s SAR ADC with on-chip calibration in 55nm CMOS," 2017 Symposium on VLSI Circuits, Kyoto, pp. 282-283, 2017,
30. A.M. Abo and P.R. Gray.“A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,”Journal of Solid-State Circuits.,vol.34,no.5, pp.599–606, May 1999.
31. Rongshan Wei, Jue Wang, Haiji Su.“A fast-response reference voltage buffer for a sigma-delta modulator,”IEICE Electronics Express., vol.15, no. 8, 2018.
32. Taheri, S.; Yuan, J.-S.‘’Mixed-Signal Hardware Security: Attacks and Countermeasures for ΔΣ ADC,’’Electronics. ,2017.
33. Wu, J.; Wu, J. ‘’A 12-Bit 200 MS/s Pipelined-SAR ADC Using Back-Ground Calibration for Inter-Stage Gain,’’ Electronics., 2020.
34. J. Wu, Z. Zhang, R. Subramoniam and F. Maloberti, "A 107.4 dB SNR Multi-Bit Sigma Delta ADC With 1-PPM THD at -0.12 dB From Full Scale Input," in IEEE Journal of Solid-State Circuits, vol. 44, no. 11, pp. 3060-3066, Nov. 2009.

518 35. K. Lee, M. R. Miller and G. C. Temes, "An 8.1 mW, 82 dB Delta-Sigma ADC With 1.9 MHz BW and -98 dB
519 THD," IEEE Journal of Solid-State Circuits, vol. 44, no. 8, pp. 2202-2211, Aug. 2009.
520 36. M. Chen et al."27.5 A pixel-pitch-matched ultrasound receiver for 3D photoacoustic imaging with
521 integrated delta-sigma beamformer in 28nm UTBB FDSOI," 2017 IEEE International Solid-State Circuits
522 Conference (ISSCC), San Francisco, CA, pp. 456-457, 2017.
523 37. M. Steiner and N. Greer."15.8 A 22.3b 1kHz 12.7mW switched-capacitor ΔΣ modulator with stacked
524 split-steering amplifiers," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco,
525 CA, pp. 284-286, 2016.
526 38. R. Brewer, J. Gorbold, P. Hurrell, C. Lyden, R. Maurino and M. Vickery, " A 100dB SNR 2.5MS/s output
527 data rate ΔΣ ADC," ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits
528 Conference, 2005., San Francisco, CA, Vol. 1, pp. 172-591 ,2005.
529 39. Y. Jung, H. Roh and J. Roh, " An Input-Feedforward Multibit Adder-Less Δ−Σ Modulator for Ultrasound
530 Imaging Systems," IEEE Transactions on Instrumentation and Measurement, vol. 62, no. 8, pp. 2215-2227,
531 Aug. 2013.
532 40. R. Rajan and S. Pavan."29.1 A 5mW CT ΔΣ ADC with embedded 2nd-order active filter and VGA
533 achieving 82dB DR in 2MHz BW," 2014 IEEE International Solid-State Circuits Conference Digest of
534 Technical Papers (ISSCC), San Francisco, CA, pp. 478-479, 2014.
535 41. K. Reddy et al. "A 16mW 78dB-SNDR 10MHz-BW CT-ΔΣ ADC using residue-cancelling VCO-based
536 quantizer," 2012 IEEE International Solid-State Circuits Conference, San Francisco, CA, pp. 152-154, 2012.
537 42. Risheng Lv, Weiping Chen, and Xiaowei Liu,” A High-Dynamic-Range Switched-Capacitor Sigma-Delta
538 ADC for Digital MicromechanicalVibration Gyroscopes” Micromachines (Basel),Vol.9,no.8,2018 .

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