Design considerations for high power converters interfacing 10 MW superconducting wind power generators

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Abstract: The design of power electronic converters for the integration of wind generated power into the grid is more and more important due to a new class of Superconducting Generators (SG) with power ratings of up to 20 MW. High efficiency of power converters for high power applications is mandatory in order to reduce the overall cost of the system. This paper proposes a design method to minimise the cost of the system by finding the optimal number of power devices and capacitors for different high power converter topologies. The investigation focuses on determining the optimal number of voltage levels for a Back-To-Back (BTB) Neutral Point Clamped (NPC) converter. The design method is demonstrated by estimating the cost of different BTB NPC power converter topologies for the integration of a 10 MW SG to the grid.

1. Introduction

Power electronic converters play an important role in the wind energy industry since they are the link between the wind power generator and the grid. The importance of the power electronic converters is expected to increase due to the new generation of direct-drive Superconducting Generators (SG) with power ratings up to 20 MW [1]-[3].

The design of a power converter for high power applications is a complex and critical task since many parameters, such as the converter topology, rated power, DC-Link voltage, number of voltage levels, semiconductors, capacitors, etc., need to be defined before the design of the converter begins. Normally, some of the parameters for the design of a converter, such as the rated power and the DC-link voltage, are imposed by external factors whereas the topology, power devices and number of voltage levels are chosen by the designer. The right selection of the aforementioned parameters can improve the performance of the system as well as reduce the investment cost.

Different multilevel converter topologies have been proposed for the integration of high wind power generators to the grid [4]. In general, the three major multilevel converter topologies are: (i) cascaded H-Bridges [5] (ii) flying capacitors [5] and (iii) Neutral Point Clamped (NPC) diode converters [5], [6]. A big advantage of multilevel flying capacitor converters and NPC converters is the possibility of arranging them in the Back-To-Back (BTB) configuration. As a consequence, power, voltage and frequency of the input and output can be completely controlled. BTB converters configurations are also known as universal power conditioners [5], [7]. In this work, among the multilevel converter topologies, the NPC converter has been chosen over the cascaded H-bridge and flying capacitor converters. The NPC topology shares a DC-Link

for all its phases whereas the cascaded H-Bridge converter requires a separate DC voltage source for each H-Bridge in cascade and therefore it cannot be connected in the BTB arrangement [5]. The multilevel flying capacitor topology requires extra capacitors when compared to the NPC topologies and hence the cost and size of the converter increase up to unacceptable levels [5]. One of the drawbacks of the NPC inverter topologies is voltage balancing across the series of capacitors in the DC-Link. However, the BTB NPC topology enables the balance of the capacitors DC voltage without any external or extra circuitry [8]-[10].

One of the key factors in the design of multilevel converters is to determine the number of required voltage levels since it directly affects the voltage and current ratings of the power devices to be used. Increasing the number of voltage levels has some advantages and disadvantages. The main advantages of using power converters with more than two voltage levels can be listed as [3], [5] voltage stress for each device and capacitor is lower, enabling the use of low voltage rating devices which are usually cheaper than high voltage rating devices; lower dV/dt, lower total harmonic distortion, and better performance with respect to the two-level converters for the same switching frequency.

The disadvantages of using more than the minimum number of voltage levels are as follow [5]: complex control, more computational resources due to the increase of control complexity, and necessity of using clamping diodes in NPC topologies.

Since the number of power semiconductor devices increases as the number of levels, researchers have focused on developing new topologies to reduce the number of switches in a converter [12]-[23]. Different approaches to reduce the number of switches have been taken. They can be grouped as: symmetric configurations [12]-[20], asymmetric configurations [15], [16], [19], [21], [22] and hybrid configurations [23]. However, the problem of finding an optimal number of voltage levels for the NPC BTB converters for a given power semiconductor is not tackled in literature. This paper proposes a method of determining an optimal number of voltage levels of a BTB NPC converter for selected voltage and current ratings of converter power devices. This optimisation is of particular importance for high power medium voltage wind power applications, in particular, for a new class of 10-20 MW superconducting offshore wind generators [1]. It should be noted that for the design of high power converters, both the quality of the output voltage and the minimisation of the number of power devices and capacitors are equally important, as they directly affect the overall system cost and efficiency. The aim of the paper is then to highlight the importance of the optimisation of the number of voltage levels, in that, an improved performance can be obtained by increasing the number of voltage levels while using the same number of power devices and capacitors as in the two level topology. The increased number of voltage levels results in minimising or eliminating of passive output

filters which are normally required to fulfil the power quality requirements from both the generator and the grid side.

This paper is organised as follows. Section 2 describes the BTB NPC converter topology providing the equations to determine the number of required power devices with respect to the number of voltage levels of the converter. Section 3 deals with the classical design considerations for high power converters. Section 4 presents the optimization method proposed in this paper. The proposed method finds optimal numbers of voltage levels for the selected power device voltage ratings accounting for the total number of power IGBTs and capacitor required. Section 5 defines a global optimal number of voltage levels for a BTB NPC converter. Finally, section 6 summarises the main findings of this work.

2. System structure

The three-phase 2-level BTB converter considered in this work is composed of six legs connected in parallel with a common DC-Link, Fig. 1. Each leg of the converter consists of a series connection of Basic IGBT Units (BIUs), whereas the DC-Link consist of a Basic Capacitor Unit (BCU). Each BIU of the converter leg is in general built of many IGBT Units (IUs) connected in series and parallel, as it is illustrated in Fig. 2.(a). An IU refers to a power device module that consists of an IGBT and an antiparallel diode. As for the BIU, the BCU that forms the DC-Link is also built of many capacitors in series and in parallel, Fig. 2.(b). In summary, a 2-level BTB converter is composed of 12 BIUs and 1 BCU, as it is shown in Fig. 1.

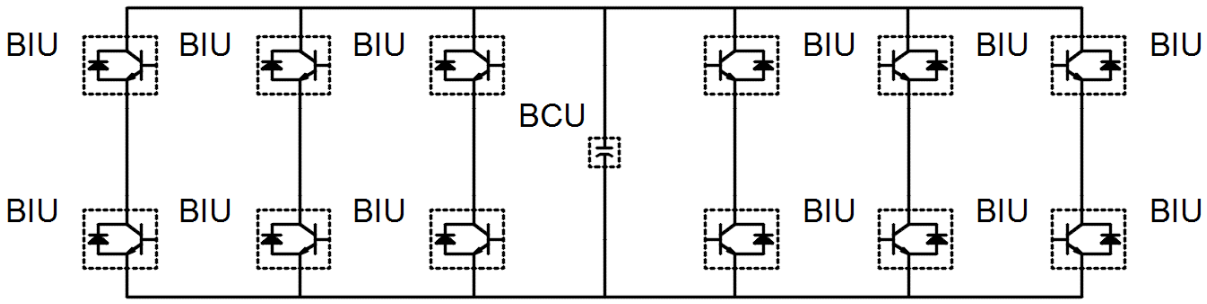


Fig. 1 *2-level BTB converter*

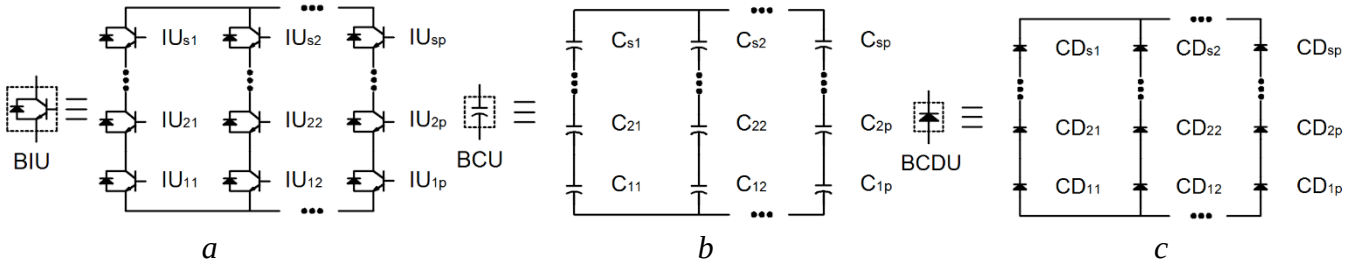


Fig. 2 *Representation of a*

a Basic IGBT Unit (BIU)
b Basic Capacitor Unit (BCU)
c Basic Clamp Diode Unit (BCDU)

For multilevel BTB NPC converter topologies, additional power diodes are required to create 3 or more voltage levels at the three-phase terminals of the converter. Fig. 3 shows a basic n-level NPC converter leg. Each Basic Clamping Diode Unit (BCDU) is built of many power diodes, namely Clamping Diodes (CDs), in series and in parallel, Fig. 2.(c). The BCDUs are connected in series to each other and in parallel to the BIU to create BTB NPC converter topologies with 3 or more levels. For example, a 3-level BTB NPC, Fig. 4, converter requires in total 24 BIUs, 12 BCDUs and 2 BCUs.

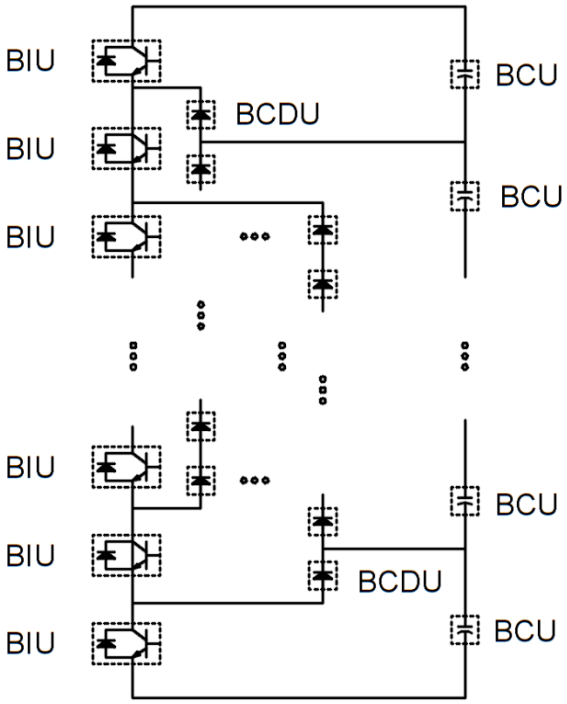


Fig. 3 *n-level NPC converter leg*

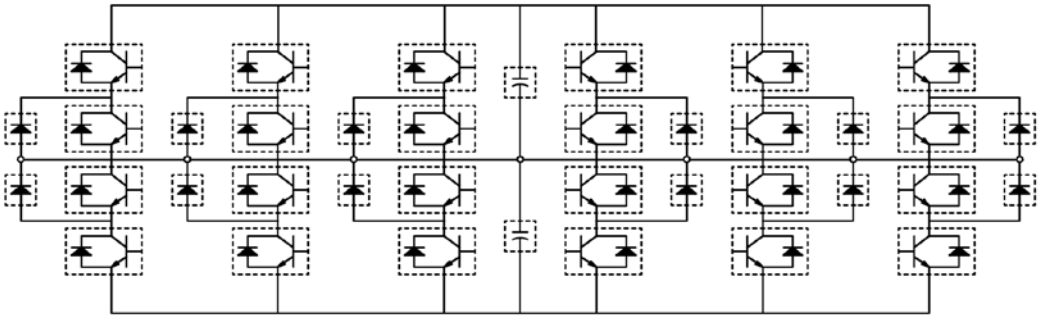


Fig. 4 *3-level BTB NPC converter.*

Equations (1)-(3) define the total number of IUs, CDs and capacitors with respect to the number of voltage levels of the BTB NPC power converter [5], where n is the number of voltage levels, B_{device} and

B'_{device} represent respectively the total number of IU and CDs per BIU and BCDU, and C_{cap} is the total number of capacitors per BCU.

$$IUs = 12 \cdot B_{device} \cdot (n-1) \tag{1}$$

$$CDs = 6 \cdot B'_{device} \cdot (n-2) \cdot (n-1) \tag{2}$$

$$Capacitors = C_{cap} \cdot (n-1) \tag{3}$$

The voltage that a single BIU has to block reduces as the number of converter levels increases. Hence, for a certain value of the DC-Link, a 2-level converter may need two IUs (B_{device} = 2) per BIU to block the full DC-Link voltage, making a total of 24 IUs for a whole converter. However, since the blocking voltage for a BIU used in the 3-level topology reduces by half, only one IU (B_{device} = 1) per BIU is necessary to block the full DC-Link voltage. Therefore, a total of 24 IUs (i.e. the same number as in the 2-level converter) is necessary to create the 3-level voltage converter. A similar principle applies for the capacitors. Thus, rearranging the connections of the IUs and capacitors, a higher number of voltage levels can be achieved with the only extra cost caused by the necessity of using CDs as defined by (2).

3. Classical design

The classical design of a BTB NPC converter usually begins by determining the line-to-line grid voltage (V_{ll}) and the rated power (P_n) that the converter has to feed into the grid. Once both parameters are defined it is possible to calculate the minimum value of the required DC-link voltage (V_{DC}) and the peak current that semiconductors have to endure according to (4) and (5) respectively.

$$V_{DC} = \sqrt{2} \cdot V_{ll} \cdot (1+S) \tag{4}$$

$$I_p = \frac{\sqrt{2} \cdot P_n}{\sqrt{3} \cdot V_{ll}} \tag{5}$$

where S is the safety factor and its value is within 10% to 20% [24], V_{ll} is the line-to-line voltage, P_n is the generator rated power, I_p is the peak current and V_{DC} is the DC-link voltage.

The next step is to determine the number of required voltage levels of the converter. The voltage that each BIU, BCDU or BCU has to endure (V_{sblock_n}) reduces as the number of the voltage levels of the converter increases according to:

$$V_{sblock\_n} = \frac{V_{DC}}{(n-1)} \tag{6}$$

Once the voltage that the semiconductors and capacitors have to block has been calculated, the process of determining the necessary number of IUs, CDs and capacitors per basic unit begins. The process is described in the following subsections in detail.

3.1. Semiconductors

3.1.1 IGBT Units: IUs have certain limitations regarding the maximum voltage and current they can block and endure. The maximum peak voltage that IUs can endure must not exceed 80% of their rated voltage (V_{dev}), and the DC voltage should not exceed 50% of V_{dev} [25]. Therefore, the required number of IUs connected in series to block the DC-link voltage (B_{s_n}) is a function of the numbers of voltage levels of the converter and can be obtained by:

$$B_{s\_n} = \max\left(ceil\left(\frac{V_{sblock\_n}}{0.8 \cdot V_{dev}}, \frac{V_{sblock\_n}}{0.5 \cdot V_{dev}} \right) \right) \tag{7}$$

where n is the number of voltage levels of a BTB converter. Equation (7) can be further simplified as:

$$B_{s\_n} = ceil\left(\frac{2 \cdot V_{sblock\_n}}{V_{dev}} \right) \tag{8}$$

IUs also have limitations from the current point of view. Therefore, the maximum repetitive current peak value, I_p, should not exceed 70% of the rated DC IU current, I_{dev}, [25]. Hence, the required number of IUs connected in parallel (B_p) is given by:

$$B_p = ceil\left(\frac{I_p}{0.7 \cdot D \cdot I_{dev}} \right) \tag{9}$$

Although there is no limitation to the number of IUs that can be connected in parallel, under the worst case conditions the current is concentrated in one IU and hence the rated DC current has to be additionally decreased by the current derating factor (D) [25]:

$$D = \frac{1 + \frac{\left(B_p - 1\right) \cdot \left(1 - \alpha/100\right)}{1 + \alpha/100}}{B_p} \cdot 100 \tag{10}$$

where B_p is the number of parallel connections and α is the current unbalanced rate. To calculate the number of IUs in parallel an iterative process is necessary. In the worst scenario the value of D can be calculated for an infinite number of parallel connections as:

$$D = \lim_{B_p \to \infty} D = \frac{1 - \alpha/100}{1 + \alpha/100} \cdot 100 \tag{11}$$

Finally, the total number of IUs per BIU is calculated from (12) and the total number of IUs per converter is a function of the number of converter voltage levels and can be calculated from (1).

$$B_{device} = B_{s\_n} \cdot B_p \tag{12}$$

3.1.2 Clamping Diodes: The process to determine the number of CDs for a BTB NPC converter is exactly the same as the one described in the previous subsection for the IUs, by replacing the specific values of IU voltage and current ratings with the diodes ones. The total number of CDs for the whole converter is calculated from (2).

3.2. DC-Link Capacitors

According to [26], the total capacitance of a DC-Link for a 2-level BTB converter (C_c) can be obtained as:

$$C_c = \frac{P_n}{2 \cdot f_{sw} \cdot V_{DC}^2 \cdot \Delta u} \tag{13}$$

where f_{sw} is the switching frequency and Δu is the voltage ripple in percentage usually limited to a maximum of 1%. It should be noted that for a NPC BTB converter, the capacitors that form the DC-Link are connected in series and thus the design capacitance per BCU (C_{design_n}) is a function of the number of voltage levels and can be calculated as:

$$C_{design\_n} = (n-1) \cdot C_c \tag{14}$$

The required number of capacitors in series per BCU (C_{s_n}) that form the DC-Link reduces as the number of voltage levels of the NPC BTB converter increases and can be calculated as:

$$C_{s\_n} = ceil\left(\frac{V_{sblock\_n}}{V_C}\right) \tag{15}$$

where V_C is the rated voltage of the selected capacitor to be installed. The number of capacitors in parallel per BCU depends on the number of capacitors in series per BCU, since the capacitance of one BCU is reduced by connecting more capacitors in series. Therefore, the necessary number of capacitors in parallel (C_{p_n}) to satisfy the design capacitance of one BCU defined by (14), can be obtained by

$$C_{p\_n} = ceil\left(\frac{C_{design\_n}}{C_{cond} \diagup C_{s\_n}}\right) \tag{16}$$

where C_{cond} is the capacitance of each capacitor that forms the BCU. Finally, the total number of capacitors per BCU is calculated from (17) and the total number of capacitors in the DC-Link is calculated from (3).

$$C_{cap} = C_{s\_n} \cdot C_{p\_n} \tag{17}$$

4. The optimal number of voltage levels

In the classical design of power converters the number of voltage levels is normally set before the design process begins. As a consequence, there is no guarantee that the chosen number of voltage levels is the optimal level either from the point of view of IGBTs or capacitors, since one or both of them might be oversized. For example, after designing a converter based on a selected IGBT and an initially proposed number of voltage levels, it is possible to rearrange the same number of IGBTs in series and parallel connections in a different way to achieve a higher number of voltage levels with an increase in the price of the converter only due to the CD.

The advantage of optimizing the number of voltage levels of the converter is the improvement of the efficiency of the system. On the contrary, a small increase in the price of the converter, due to the usage of CD, is its biggest disadvantage. However, this increase in cost can be overcome by the reduction in the overall cost of the entire system due to the fact that by increasing the number of voltage levels the size and cost of the output filter decreases. Since optimizing the number of voltage levels improves the efficiency of the system, this section is devoted to find the optimal numbers of voltage levels from the point of view of the required number of (i) IGBTs and (ii) capacitors.

4.1. Considering IGBTs Only

This subsection presents the equations for calculating all possible optimal numbers of voltage levels for a selected IGBT voltage and current ratings. Since the BTB NPC converter topology is modular, the two level converter is always one of the optimal configurations from the point of view of the required total number of IGBTs. Furthermore, the maximal optimal converter level is achieved when the number of IGBTs in series per one BIU is equal to 1 (i.e. B_{s_n} =1) since the number of IGBTs connected in parallel, per one BIU, is independent of the number of voltage levels. Therefore, for a selected IGBT, the maximal optimal voltage (n_{max}) level will be:

$$n_{\max} = ceil\left(B_{s\_2} + 1\right) \tag{18}$$

Due to the modular characteristic of the BTB NPC converter, any converter level between 2 and n_{max} could be optimal. To discern which levels are optimal, the modular property of the BTB NPC converter is applied. Hence, all the levels that fulfil (19) are optimal from the point of view of the number of IGBTs and they are noted by n_o in the rest of the paper. Therefore, a higher voltage level can be achieved with no extra cost of IGBTs if they are the only ones considered in the cost optimization process.

$$\mathrm{mod}\left(B_{s\_2} \cdot \frac{1}{(n_o - 1)} \right) = 0 \quad \text{for } 2 \le n_o \le n_{\max} \tag{19}$$

The increase in the number of voltage levels with no extra cost in the cost of IGBTs brings the advantages and disadvantages of using multilevel topologies in general, as stated in Section 1. To illustrate the proposed optimisation approach for finding optimal numbers of voltage levels for a BTB NPC converter, three different IGBT modules [27] listed in Table 1 are considered. Table 1 presents the identified optimal numbers of voltage levels n_o for the converter interfacing a 10 MW SG to the grid of 3300 V line to line voltage. The results are obtained by considering the safety factor S of 15% (S = 0.15).

Table 1 IGBTs Considered for the converter design [27]

V_{ce} (V)	I_{ce} (A)	Cost (€/IU)	n_{max}	n_o
1200	3600	1343.19	10	2, 4, 10
1700	3600	1792.06	8	2, 8
3300	1500	2102.70	5	2, 3, 5

Table 2 shows the number of IGBTs in series, parallel per BIU and the total number of IU per converter for the three different IGBTs considered in this paper to design a BTB NPC converter from 2 to 10 voltage levels. It is worth noticing that for the optimal voltage levels of each considered IGBT, the number of IU in series is different per BIU but the total number of IU per converter remains constant. Fig. 5 shows the total cost of IGBTs as a function of the number of voltage levels for the 10 MW grid interfacing BTB NPC. Since for the 1200V/3600A IU the optimal voltage levels are 2, 4 and 10, the total number of IUs is the same per converter, the IUs cost is also the same (Fig. 5, blue bar). If 1700V/3600A IU is used, 2 and 8-level converters have the same cost IUs (Fig. 5, red bar), while if 3300V/1500A IUs are used, 2, 3 and 5-level converters are optimal solutions (Fig. 5, green bar).

Table 2 Number of IGBTs in series, parallel and total for a BTB NPC converter to feed a 10 MW SG at 3300 V line to line

Switch Level	1200V/3600A			1700V/3600A			3300V/1500A		
	Series	Parallel	Total	Series	Parallel	Total	Series	Parallel	Total
n	B_{s_n}	B_p	*IUs*	B_{s_n}	B_p	*IUs*	B_{s_n}	B_p	*IUs*
2	9	1	108	7	1	84	4	3	144
3	5	1	120	4	1	96	2	3	144
4	3	1	108	3	1	108	2	3	216
5	3	1	144	2	1	96	1	3	144
6	2	1	120	2	1	120	1	3	180
7	2	1	144	2	1	144	1	3	216
8	2	1	168	1	1	84	1	3	252
9	2	1	192	1	1	96	1	3	288
10	1	1	108	1	1	108	1	3	324

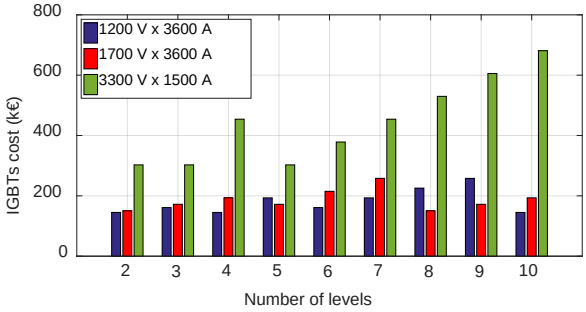


Fig. 5 *IGBTs cost as a function of the number of levels of the converter. 1200V/3600A (blue bar), 1700V/3600A (red bar), 3300V/1500A (green bar).*

4.2. Considering DC-Link Capacitors Only

The optimal number of voltage levels can also be determined from the point of view of the capacitors that form the DC-Link of the BTB NPC converter. As stated in the previous subsection for the IUs, the two level converter topology is always one of the optimal configurations. Due to the modular property of the BTB NPC converter, the two-level converter topology is also always one of the optimal configurations from the point of view of the required total number of capacitors. Furthermore, the maximal optimal number of voltage levels is achieved when the number of capacitors in series is equal to 1.

It should be noted that the number of capacitors in series affects the number of capacitors in parallel since the capacitance of the BCU reduces as more capacitors are connected in series. The negative effect of the reduction of the equivalent capacitance in the DC-Link of a two-level converter due to the required series connection of capacitors for a given DC-Link voltage level is eliminated in topologies with three and more voltage levels by employing (14). Therefore, the maximal optimal number of voltage levels from the point of view of the necessary number of capacitors (n'_{max}) is achieved when the number of capacitors in series (per one BCU) is equal to 1 and the number of capacitors in parallel is equal to the 2-level converter design requirement. The maximal number of voltage levels that fulfil the above condition can be calculated as:

$$n'_{\max} = ceil\left(C_{s\_2} + 1\right) \tag{20}$$

Due to the modular characteristic of the BTB NPC converter, all the levels between 2 and n'_{max} could be optimal. As in the previous subsection, all the levels that fulfil (21) are optimal from the point of view of the capacitors and they are noted by n'_o. Hence a higher converter level can be achieved with no extra cost of capacitors if they are the only ones considered in the cost optimization process.

$$\operatorname{mod}\left(C_{s\_2} \cdot \frac{1}{\left(n'_0 - 1\right)}\right) = 0 \quad \text{for } 2 \le n'_0 \le n_{\max} \tag{21}$$

The calculation of the optimal voltage level from the capacitors point of view is summarized by the results in Table 3, where the features of the capacitors considered, their cost [28] and the optimal voltage levels are shown.

Table 3 Capacitors considered for the converter design [28]

Capacitance (mF)	Voltage (V_C) (V)	Cost (€/Capacitor)	n'_{max}	n'_o
3	800	288.4	8	2, 8
1.6	1150	217.49	6	2, 6

Table 4 shows the number of capacitors in series, parallel per BCU and the total number of capacitor per converter for the two different capacitors considered to design the BTB NPC converter from 2 to 10 voltage levels. It is worth noticing that for the optimal voltage levels the total number of capacitors is the same than for the 2-level converter although the number of capacitors in series is different. Fig. 6 shows the cost for the DC-Link as a function of the number of voltage levels of the BTB NPC converter. Since the smallest number of capacitors to form the DC-Link corresponds to 2, the optimal voltage level, whilst the cost is also the cheapest. Hence, the cheapest cost for the 3mF/800 capacitor is for the 2 and 8 voltage level converter (blue bar) and for the 1.6mF/1150V capacitor is for the 2 and 6 voltage levels (red bar).

Table 4 Number of capacitors in series, parallel and total for a BTB NPC converter to feed a 10 MW SG at 3300 V line to line

Capacitor Level	3 mF/800 V			1.6 mF/1150 V		
	Series	Parallel	Total	Series	Parallel	Total
n	C_{s_n}	C_{p_n}	*Capacitors*	C_{s_n}	C_{p_n}	*Capacitors*
2	7	67	469	5	90	450
3	4	77	616	3	108	648
4	3	86	774	2	108	648
5	2	77	616	2	143	1144
6	2	96	960	1	90	450
7	2	115	1380	1	108	648
8	1	67	469	1	126	882
9	1	77	616	1	143	1144
10	1	86	774	1	161	1449

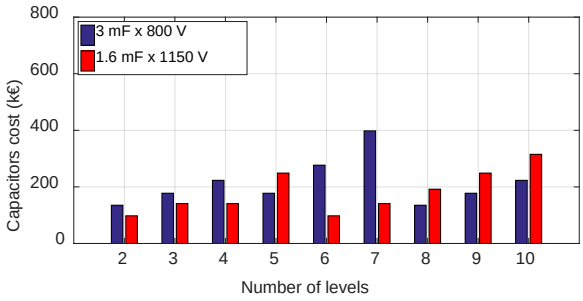


Fig. 6 *Capacitors cost as a function of the number of levels of the converter levels. 3mF/800V (blue bar) and 1.6mF/1150V (red bar).*

5. Global optimisation

In the previous sections, the optimal number of voltage levels for the multilevel BTB NPC converter was determined without taking into account an additional cost due to the usage of CDs which are needed to clamp the converter three-phase output terminals to different DC-Link voltage levels. Therefore, in this section the number of required CDs is included in the optimization process and the converter is then said to be globally optimized with respect to the number of voltage levels.

The calculation of the number of CDs is explained in detail in Section 3. The voltage and current ratings of the diodes selected are listed in Table 5. Table 6 shows the number of CDs needed for different multilevel BTB NPC converter topologies interfacing a 10 MW SG to the grid of 3300 V line-to-line voltage. The number of CDs is independent of the number of IUs and capacitors. Fig. 7 shows the extra cost due to the usage of CDs for different multilevel BTB NPC converter topologies.

Table 5 Diodes considered for the converter design [28]

V_{ce} (V)	I_{ce} (A)	Cost (€/Diode)
1700	800	144
1700	3600	1316

Table 6 Number of diodes in series, parallel and total for a BTB NPC converter to feed a 10 MW SG at 3300 V line to line

Diode Level	1700V/800A			1700V/3600A		
	Series	Parallel	Total	Series	Parallel	Total
n	B_{s_n}	B_p	*CDs*	B_{s_n}	B_p	*CDs*
2	0	0	0	0	0	0
3	4	6	288	4	1	48
4	3	6	648	3	1	108
5	2	6	864	2	1	144
6	2	6	1440	2	1	240
7	2	6	2160	2	1	360
8	1	6	1512	1	1	252
9	1	6	2016	1	1	336
10	1	6	2592	1	1	432

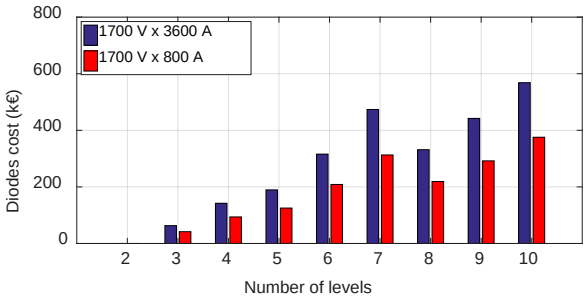


Fig. 7 *Diodes cost as a function of the number of levels of the converter. 1700V/3600A (blue bar) and 1700V/800A (red bar).*

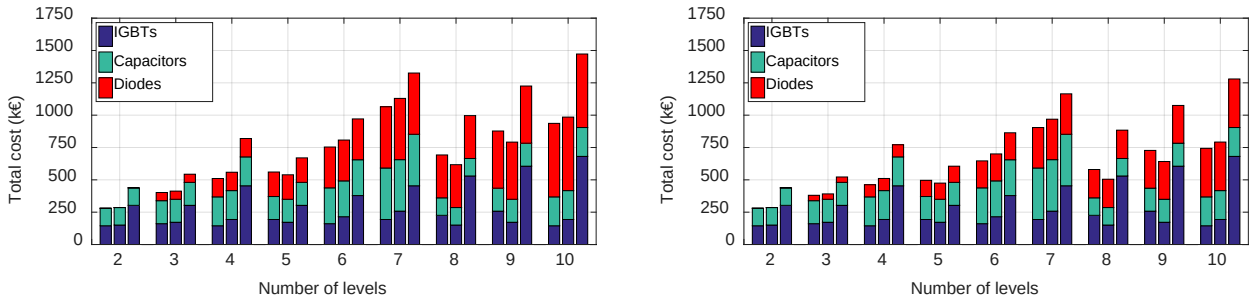
The determination of the global optimal number of voltage level for a converter is carried out according to the following steps:

1. Calculate the optimal number of voltage levels (n_o) for a selected IGBT module as explained in section 4.1.
2. Calculate the rated voltage of the capacitor that forms the BCU for each optimal number of voltage levels from step 1, according to

$$\frac{V_{DC}}{n_o - 1} \leq V_C < \frac{V_{DC}}{n_o - 2} \tag{22}$$

3. Calculate the extra cost due to additional CDs, as explained in section 3.1.2, for each optimal number of voltage levels from step 1.
4. Compare the extra cost due to the CDs with the cost of the output filters for each optimal number of voltage levels.

In order to make the optimization process more comprehensive, Fig. 8 show the overall cost of the BTB NPC converter considering the total number of required IUs, CDs and capacitors for different case studies considered in this paper. The results show that the cheapest converter is always the two level topology as there is always an extra cost due to CDs in the BTB NPC converter. An extra cost due to the IUs and capacitors can also be present if the chosen IU or capacitor has not been optimized.



a *b*

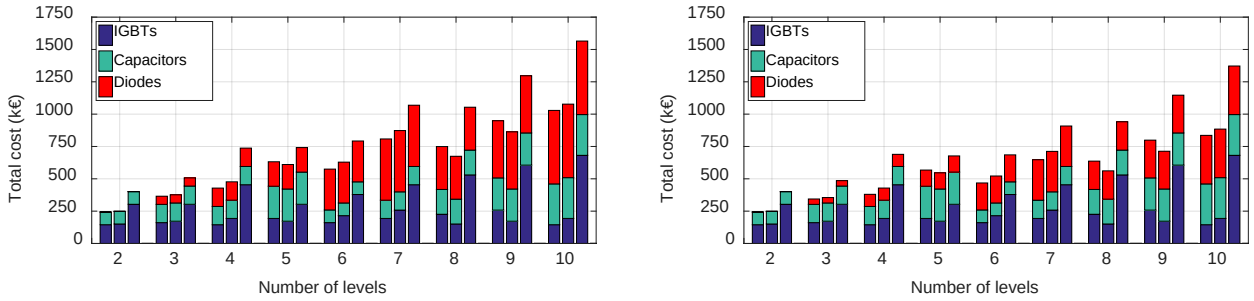


Fig. 8 *Total converter cost as a function of the number of levels of the converter with*
a 1700V/3600A diodes, 3mF/800V capacitors
b 1700V/800A diodes, 3mF/800V capacitors
c 1700V/3600A diodes, 1.6mF/1150V capacitors
d 1700V/800A diodes, 1.6mF/1150V capacitors
IGBTs used in (a), (b), (c) and (d): 1200V/3600A (first column for each level), 1700V/3600A (second column for each level) and 3300V/1500A (third column for each level) IGBTs

The optimal converter level is always a compromise between the extra cost due to CDs and the cost of output filters, even though both IUs and capacitors have been optimized. Thus, if the output filter is not taken into account in the cost optimization, as it is in this paper, it might be possible to have an optimized converter which cost is higher than one which has not been optimized, with respect to the required number of IUs and capacitors. This effect is clearly seen in Fig. 8.(a) where the cost of the IGBTs and capacitors is optimized for the eight level for IUs of 1700V/3600A and capacitors of 3mF/800 V (the bar in the middle for each level in Fig. 8.(a)), since the cost of the IGBTs and capacitors is the same as for the 2 level converter. Nevertheless, due to the usage of additional CDs, the 8-level converter is more expensive than the 3-level, although for the 3-level converter neither the IGBT nor capacitors have been optimised. Taking into account the cost of the output filter in the optimization process is very difficult since the output filter design depends on many variables which are out of the scope of this paper.

6. Conclusions

This paper has compared the classical design of a BTB NPC converter with the proposed new design strategy for a BTB NPC converter for high power SG applications. The proposed design strategy optimizes the use of IGBTs and capacitors for achieving a higher number of voltage levels in a BTB NPC converter topology. The first step in this design approach optimizes the number of voltage levels from the IGBTs point of view. The second part does the optimization from the point of view of the number of capacitors that form the DC-Link. Finally, the proposed method optimizes the number of voltage levels considering both IGBTs and capacitors and thus optimizing the converter in a global sense.

The results of the global optimization show that the cheapest converter is always the 2-level converter if the cost of the output filter is not considered in the converter design. Furthermore, increasing the number

of voltage levels always produces an extra cost due to the necessity of using CDs. Hence, the global optimal design of the number of voltage levels for high power converters for wind power applications is always a compromise between the extra cost due to the use of CDs when the number of voltage levels of the converter increases and the reduction in the cost of the output filters, since the reduction in the output filter cost can be greater than the extra cost due to the use of CDs for achieving a higher number of voltage levels.

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8. References

[1] Innovative Wind Conversion Systems (10-20MW) For Offshore Applications (INNWIND). http://www.innwind.eu/, accessed 23 June 2016.

[2] K. Ma and F. Blaabjerg, "Thermal optimised modulation methods of three-level neutral-point-clamped inverter for 10 MW wind turbines under low-voltage ride through," *IET Power Electron*., vol. 5, no. 6, pp. 920-927, July 2012.

[3] K. K. Gupta, S. Jain, "Comprehensive review of a recently proposed multilevel inverter," *IET Power Electron*., vol. 7, no. 3, pp. 467-479, March 2014.

[4] Z.Q. Zhu, J.B. Hu, "Electrical machines and power-electronic systems for high-power wind energy generation applications, Part II: Power electronics and control systems," *COMPEL: The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, vol. 32, no. 1, pp.34-71, 2013.

[5] J. S. Lai, F.Z. Peng, "Multilevel converters-a new breed of power converters" *IEEE Trans. Ind. Appl*., vol.32, no.3, pp.509-517, May/Jun 1996.

[6] A. Nabae, I. Takahashi, H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Appl*., vol.IA-17, no.5, pp.518-523, Sept. 1981.

[7] L.M. Tolbert, F.Z. Peng, T.G. Habetler, "A multilevel converter-based universal power conditioner," *IEEE Trans. Ind. Appl.*, vol.36, no.2, pp.596-603, Mar/Apr 2000.

[8] M. Marchesoni, P. Tenca, "Diode-clamped multilevel converters: a practicable way to balance DC-link voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 752-765, Aug 2002.

[9] T. Ishida, K. Matsuse, T. Miyamoto, *et al*, "Fundamental characteristics of five-level double converters with adjustable dc voltages for induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 775-782, Aug 2002.

[10] Z. Pan, F. Z. Peng, K. A. Corzine, *et al*, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1698-1706, Nov.-Dec. 2005.

[11] K. K. Gupta and S. Jain, "Topology for multilevel inverters to attain maximum number of levels from given DC sources," *IET Power Electronics*, vol. 5, no. 4, pp. 435-446, April 2012.

[12] M.F. Kangarlu, E. Babaei, S. Laali, 'Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources', *IET Power Electron.*, 2012, 5, (5), pp. 571–581

[13] K. K. Gupta, S. Jain, "Multilevel inverter topology based on series connected switched sources," *IET Power Electron*., vol. 6, no. 1, pp. 164-174, Jan. 2013.

[14] A. Masaoud, H. W. Ping, S. Mekhilef and A. S. Taallah, "New Three-Phase Multilevel Inverter With Reduced Number of Power Electronic Components," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6018-6029, Nov. 2014.

[15] A. Ajami, M. R. Jannati Oskuee, M. T. Khosroshahi, *et al*, "Cascade-multi-cell multilevel converter with reduced number of switches," *IET Power Electron*., vol. 7, no. 3, pp. 552-558, March 2014.

[16] A. Ajami, M. R. J. Oskuee, A. Mokhberdoran, *et al*, "Developed cascaded multilevel inverter topology to minimise the number of circuit devices and voltage stresses of switches," *IET Power Electron*., vol. 7, no. 2, pp. 459-466, February 2014.

[17] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, *et al*, "Switched-diode structure for multilevel converter with reduced number of power electronic devices," *IET Power Electron*., vol. 7, no. 3, pp. 648-656, March 2014.

[18] M. Toupchi Khosroshahi, "Crisscross cascade multilevel inverter with reduction in number of components," *IET Power Electron.*, vol. 7, no. 12, pp. 2914-2924, Dec. 2014.

[19] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, *et al*, "Reduction of Power Electronic Elements in Multilevel Converters Using a New Cascade Structure," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 256-269, Jan. 2015.

[20] E. Zamiri, N. Vosoughi, S. H. Hosseini, *et al*,"A New Cascaded Switched-Capacitor Multilevel Inverter Based on Improved Series–Parallel Conversion With Less Number of Components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3582-3594, June 2016.

[21] E. Babaei, M. F. Kangarlu, M. A. Hosseinzadeh, "Asymmetrical multilevel converter topology with reduced number of components," *IET Power Electron*., vol. 6, no. 6, pp. 1188-1196, July 2013.

[22] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, *et al*, "Novel Topologies for Symmetric, Asymmetric, and Cascade Switched-Diode Multilevel Converter With Minimum Number of Power Electronic Components," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5300-5310, Oct. 2014.

[23] R. Shalchi Alishah, D. Nazarpour, S.H. Hosseini, *et al*, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels", *IET Power Electron*., vol.7, no.1, pp. 96‑104, 2014.

[24] B. Backlund, M. Rahimo, S. Klaka, *et al*, "Topologies, voltage ratings and state of the art high power semiconductor devices for medium voltage wind energy conversion," Proceeding on Power Electronics and Machines in Wind Applications, 2009, pp. 1-6.

[25] "High voltage IGBT module application manual", *Hitachi power semiconductor device, Ltd*., Dec 2009.

[26] X. Zeng, Z. Chen, F. Blaabjerg, "Design and comparison of full-size converters for large variable-speed wind turbines," *European Conference on Power Electronics and Applications*, 2007.

[27] www.uk.mouser.com, accessed 23 June 2016.

[28] INNWIND, "Deliverable D3.32 Converter designs based on new components and modular multilevel topologies", September 2014, http://www.innwind.eu/ accessed 23 June 2016.