Current Transformer Circuits for Power Electronics Applications

John Neville McNeill MPhil CEng MIET

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"*Is there any knowledge in the world which is so certain that no reasonable man could doubt it?*"

Bertrand Russell, "The Problems of Philosophy", 1912

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Declaration

The work in this thesis is based on the research carried out at the School of Engineering, Napier University, Edinburgh, UK. No part of this thesis has been submitted elsewhere for any other degree or qualification and it is all my own work unless referenced to the contrary in the text.

Signed: Neville McNeill

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ABSTRACT

This thesis investigates the operation of the current transformer (CT) when sensing return-to-zero current pulses in power electronic circuitry.

The CT's output signal is normally rectified when sensing current pulses and the effects of the different rectification techniques on peak current and average current droop are evaluated. Initially, the various current sensing techniques and their application in power electronics circuits are reviewed. The CT and both diode and synchronous rectification are then reviewed in more detail.

Operation of the CT with diode rectification (DR) and natural resetting is investigated. Three operating modes are identified. These are the discontinuous magnetizing current, continuous magnetizing current and discontinuous secondary current modes. The error (droop) in the average output signal obtained is found to be predominantly defined by CT core losses. Coefficients are given for correcting the error due to droop, provided that the discontinuous secondary current mode is avoided. Diode rectification with the dual CT arrangement is also investigated.

Operation of the CT with synchronous rectification (SR) and natural resetting is then investigated. The SR topologies possible using a discrete MOSFET are categorized. During experimentation the arrangement used to drive the MOSFET's gate is found to be important if distortion is to be minimized. It also is found that the average current droop is dependent on the oscillatory behaviour of the resetting circuit and has an effectively random component. The magnitude of this component is defined by the voltage drop exhibited by the SR MOSFET's intrinsic anti-parallel diode.

SR is then implemented using a commercially available analogue switch. The problems detailed with the use of a discrete MOSFET are largely alleviated. Another benefit is that the increased restriction on maximum duty factor imposed by introducing a discrete MOSFET is also eased. However, whichever SR technique is

implemented, an operational amplifier is used and the transient response of this circuit element is important.

A method of minimizing droop by indirect sensing of the CT's peak core flux excursion is then presented. A corresponding correcting voltage is applied in series with the CT's output terminals during a current pulse. The magnitude of this voltage is based on the magnitude of the resetting voltage sensed during previous switching cycles. A circuit is implemented and simulated. Experimental results are presented.

A switched-mode circuit operating at a frequency higher than that of the main power circuit is then used to apply the correcting voltage with the objective of reducing the power drawn. Again, the circuit is implemented and simulated and experimental results are presented.

CONTRIBUTION TO KNOWLEDGE

The main contributions claimed by the author are as follows:

1. Operation of the current pulse transformer when used with diode rectification, an active load and natural resonant resetting is investigated. Three modes of operation are identified and described. These are the discontinuous magnetizing current, continuous magnetizing current and discontinuous secondary current modes. It is shown that, at certain combinations of frequency and duty factor, the error in the average output signal obtained is predominantly defined by core losses in the CT. Simple piecewise power-law and ramp-on-a-step correction terms dependent on duty factor are shown to be appropriate for substantially correcting the error due to droop, provided that the discontinuous secondary current condition is avoided.
2. Average current droop in the dual CT arrangement when used with diode rectification has been evaluated. It is found that, although applying the correction terms used with the single CT arrangement may be ideal, a substantial reduction in droop may be achieved in this case by the simpler approach of adding in a fixed offset term which is independent of duty factor.
3. Although factors for correcting the average current droop due to core losses may be introduced, two criteria have to be satisfied. Firstly, accurate data on the CT's core losses is required. Secondly, the core losses should ideally exhibit a temperature coefficient of zero. With ferrite materials in particular, the losses vary non-linearly with temperature over the typical operating temperature of a CT. An additional important practical issue is that the op-amp should exhibit symmetrical positive and negative-going slew rates.
4. Natural resonant resetting of the current pulse transformer when used with synchronous rectification (SR) realized with a discrete MOSFET is investigated. The possible SR topologies are categorized. It is found that the arrangements used to drive the SR MOSFET's gate are important if unwanted transient output signals and steady-state distortion in the circuit's output signal

are to be avoided. The error in the average output signal obtained is also influenced by the oscillatory behaviour of the resetting circuit and has an effectively random component, the magnitude of which is defined by the voltage drop exhibited by the SR MOSFET's anti-parallel diode.

5. Using an analogue switch is preferred for realizing SR as this problem is largely alleviated, as is the distortion introduced by the presence of the MOSFET's inter-terminal capacitances and gate charging current. However, the transient (slewing) performance of the operational amplifier still affects the minimum droop attainable.
6. An active technique is investigated for reducing droop in the CT. This is applied to a CT in an otherwise conventional diode rectifier and resistive load configuration. Feedback is applied such that the CT's secondary terminal voltage is preset during a current pulse in response to the resetting voltage sensed during previous switching cycles. A circuit implementation has been investigated, results are given and a simulation has been presented. It is found that, in steady-state operation and with integral feedback, average current droop may be effectively removed if the current waveform is rectangular. This includes operation at low primary currents where the problem of operation in the discontinuous secondary current mode is virtually eliminated. With current waveforms containing a triangular component, some distortion is incurred. This can be minimized by ensuring that the circuit's time constant is large compared to the current pulse's duration. However, the transient (slewing) performance of the operational amplifier becomes npn-problematic.
7. The feasibility of using a switched-mode stage to provide the correcting voltage to a CT used with reset voltage feedback is demonstrated. This has the advantage that circuit efficiency is improved provided that the fixed losses are not excessive. Furthermore, cooling of a linear regulator is not problematic. However, a ripple voltage is superimposed onto the desired signal which is disadvantageous if the scheme is to be used for sensing peak currents as well as average currents.

LIST OF FIGURES

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LIST OF PRINCIPAL SYMBOLS

a	Exponent defining dependence of magnetic material loss per unit volume on excitation frequency	per-unit
A_1	Cross-sectional area of toroidal magnetic path within Rogowski coil	m^2
A_e	Effective area of magnetic circuit	m^2
B	Magnetic flux density	T
B_{ac}	Peak magnitude of alternating magnetic flux density	T
B_r	Remnant magnetic flux density	T
B_{sat}	Magnetic flux density at saturation	T
C	Capacitance	F
C_e	Coefficient of eddy current loss per unit volume in magnetic material	$Ws^2m^{-3}T^{-2}$
C_{eq}	Lumped equivalent capacitance across CT's secondary terminals	F
C_h	Coefficient of hysteresis loss per unit volume in magnetic material	$Ws^2m^{-3}T^{-a}$
C_{iss}	MOSFET common-source input capacitance	F
C_{oss}	MOSFET common-source output capacitance	F
C_{rss}	MOSFET reverse transfer ("Miller") capacitance	F
d	Exponent defining dependence of magnetic core material loss per unit volume on flux excursion	per-unit
d_i	Inner diameter of toroidal shape	m
d_o	Outer diameter of toroidal shape	m
d_s	Skin depth of conductor	m

D	Peak droop in signal obtained when sensing current pulse	per-unit
D_{ave}	Average droop in signal obtained when sensing current pulse	per-unit
E	Energy	J
f	Frequency	Hz
h	Height of toroidal shape	m
H	Magnetizing force	Am
H_c	Coercive magnetizing force	Am
i_D	MOSFET drain current	A
i_G	MOSFET gate current	A
i_{ideal}	Ideal measured output current	A
i_{loss}	Component lost from ideal output current	A
i_m	Instantaneous magnetizing current referred to CT primary winding	A
i_{m2}	Instantaneous magnetizing current referred to CT secondary winding	A
$i_{m2(ave)}$	Average magnetizing current referred to CT secondary winding	A
i_p	Current in CT's primary winding	A
i_{sense}	Actual measured output current	A
i_2	CT secondary terminal current	A
$I_{m2(0)}$	Magnetizing current referred to CT secondary winding at power switch turn-off	A
I_p	Magnitude of rectangular current pulse in CT's primary winding	A

J	Current density	A/m^2
k	Constant	per-unit
k_{CSR}	Value of current sense ratio of current-sensing MOSFET	per-unit
k_v	Constant giving ratio of two voltages	per-unit
l_e	Effective length of magnetic circuit	m
L	Inductance	H
L_m	Transformer primary magnetizing inductance	H
L_{m2}	Transformer secondary magnetizing inductance	H
L_1	Transformer primary side leakage inductance	H
L_2	Transformer secondary side leakage inductance	H
n	Turns ratio	per-unit
N	Turns number	per-unit
N_l	Turns number per unit length	m^{-1}
P_v	Power dissipation per unit volume	W/m^3
Q	Charge	C
R	Resistance	Ω
R_B	Burden resistance	Ω
R_C	Critical resistance	Ω
$R_{DS(on)}$	MOSFET on-state resistance	Ω
R_G	Resistance in series with power device gate electrode	Ω

R_m	Transformer magnetizing branch equivalent resistance	Ω
R_s	Diode slope resistance in forward conduction	Ω
R_1	Transformer primary conductor resistance	Ω
R_2	Transformer secondary conductor resistance	Ω
t	Time	s
t_c	Time for current in inductor to decay to zero	s
T	Period of repetitive waveform	s
T_{off}	Off-time of switch in power converter	s
T_{on}	On-time of switch in power converter	s
T_r	Resonant period	s
T_{reset}	Reset period required by current transformer	s
v_{DS}	MOSFET drain-source voltage	V
v_{GS}	MOSFET gate-source voltage	V
v_m	Voltage across transformer magnetizing branch referred to primary side	V
v_{m2}	Voltage across transformer magnetizing branch referred to secondary side	V
v_{out}	Output voltage	V
$v_{out(ave)}$	Average output voltage	V
v_2	Transformer secondary terminal voltage	V
V	Voltage	V
V_e	Effective volume	m^3
V_f	Diode forward voltage drop	V
$V_{GS(th)}$	MOSFET gate-source threshold voltage	V

$V_{(BR)DSS}$	MOSFET breakdown drain-source voltage	V
V_{reset}	Reset voltage applied to CT	V
W	Power	W
W	Power loss in core of magnetic component	W
δ	Duty factor	Per-unit
δ_{max}	Maximum duty factor	Per-unit
δ_{TH}	Threshold duty factor	Per-unit
ϕ	Magnetic flux	Wb
ϕ_{pk}	Peak magnetic flux excursion	Wb
μ_0	Permeability of free space	1.257×10^{-6} Hm^{-1}
μ_r	Relative permeability	Per-unit
ρ	Resistivity	Ωm
τ	Time constant	s
ω	Angular frequency	radians/s
ω_r	Resonant angular frequency	radians/s

LIST OF PRINCIPAL ABBREVIATIONS

ac	Alternating current
BJT	Bipolar junction transistor
CCM	Continuous conduction mode
CMCM	Continuous magnetizing current mode
csa	Cross-sectional area
CSR	Current sense ratio of current-sensing MOSFET
CT	Current transformer
dc	Direct current
DCM	Discontinuous conduction mode
DMCM	Discontinuous magnetizing current mode
DR	Diode rectification
DSCM	Discontinuous secondary current mode
emf	Electromotive force
EMI	Electromagnetic interference
IC	Integrated circuit
IGBT	Insulated gate bipolar transistor
JFET	Junction field effect transistor
LEB	Leading edge blanking
mmf	Magnetomotive force

MnZn	Manganese Zinc
MOSFET	Metal oxide semiconductor field effect transistor
OCT	Optical current transformer
pu	Per-unit
PFC	Power factor correction
PWM	Pulse width modulation
SNR	Signal-to-noise ratio
SOT	Set-on-test
SR	Synchronous rectification
TCR	Temperature coefficient of resistance
UCP	Unidirectional current pulse
UCPT	Unidirectional current pulse transformer

CHAPTER 1

INTRODUCTION AND OVERVIEW OF CURRENT SENSING TECHNIQUES FOR POWER ELECTRONICS APPLICATIONS

1.1 Overview and Organisation of Thesis

The operation of the current transformer (CT) in switched-mode power conversion applications is investigated in this thesis. More specifically, its behaviour in unidirectional current pulse (UCP) sensing applications is studied. The objective is to find practical ways of improving its performance in low-cost applications. A drawback with the CT is that "droop" occurs as some of the current being measured during a pulse flows into its magnetizing branch. Another important feature is that the pulse's duty factor has to be restricted to allow sufficient time to reset the CT's core material between pulses. Both these limitations are investigated here.

As low-cost applications are of interest, only arrangements using the "simplest" possible CT construction are investigated. That is, the CT is constructed around a continuous toroidal ("ring") core with a single secondary winding and a single primary "winding" where the primary conductor is passed once through the core's aperture.

The output signal from a unidirectional current pulse transformer (UCPT) is normally rectified. A passive diode or a synchronous rectifier may be used. Operation of the CT with both these techniques is investigated.

A reset voltage feedback technique is also investigated whereby a compensating voltage is applied in series with the CT's secondary terminals during a current pulse to minimize distortion. The magnitude of the correcting voltage is based on the magnitude of the CT's resetting voltage-time product sensed during the power converter's previous switching cycles. The feasibility of using a switched-mode stage to apply the compensating voltage with reduced power dissipation is also evaluated.

In this chapter different current sensing techniques are compared by way of a literature review. A preliminary discussion of synchronous rectification is included. Although the use of the CT in power conversion applications is the subject of this thesis, other power electronics applications, for example machine-drive inverters, are discussed where this is relevant prior art. In Chapter 2 a more specific literature review of the CT is presented. The main body of the work is included in the subsequent chapters.

1.2 Current Sensing Requirements in Switched-Mode Power Converters

Current sensing may be required at several locations in a power converter circuit. As an example, Figure 1.1 outlines a typical off-line isolated-output ac-dc converter. This circuit comprises a boost converter input stage in conjunction with a full-wave rectifier for ac-dc conversion with power factor correction (PFC) and a forward converter for dc-dc conversion with an isolated output. Winding N_3 on the isolation transformer (T1) forms the core reset circuit in conjunction with D_r.

Sensing of the input current (i_A) may be required by the boost converter's control circuit to enable it to force the average input current to accurately follow the profile of the supply voltage and therefore minimize the magnitudes of the harmonic currents drawn. High-bandwidth sensing of the current through TR2 (i_B) is normally required to implement peak current control and device protection. Accurate sensing of the average output current (i_C) may be required in various applications, such as power converters for battery charging, where the correct charging profile has to be applied. Where modular power converters are run in parallel for increased power throughput, i_A or i_B is normally controlled in response to a common current demand signal to ensure effective current sharing between the modules [1].

As stated in Section 1.1, the UCPT is investigated here. This is appropriate for sensing the transformer's primary current in "single-ended" topologies such as the forward converter in Figure 1.1 and also the flyback converter. However, in topologies such as

the half-bridge circuit where the power transformer is driven with a symmetrical primary current waveform then an ac current transformer may be used.

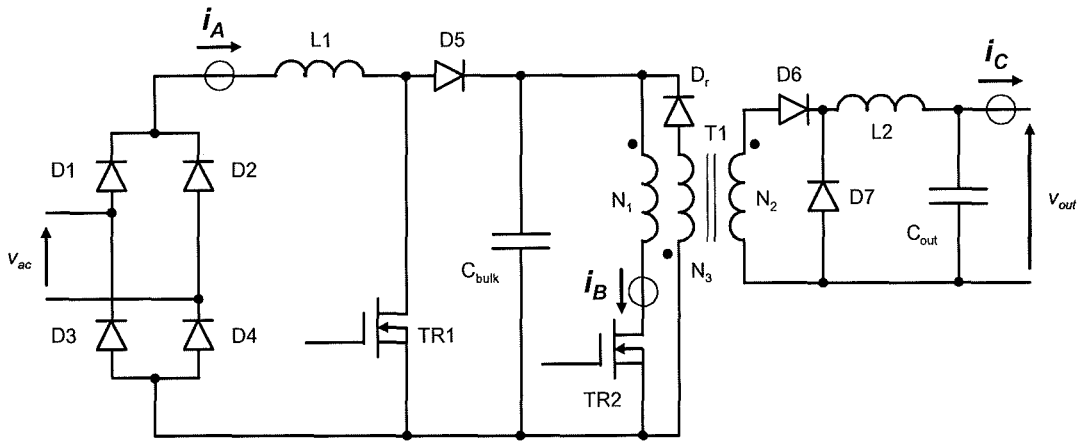


Figure 1.1. Typical Off-Line Power Converter Showing Locations where Current Sensing may be Required

1.3 Overview of the Principal Current Sensing Techniques

Various techniques may be used for sensing current [2] of which the CT is only one. Their respective advantages and disadvantages are listed in Table 1.1.

1.3.1 The Sense Resistor

The sense resistor is, in principle, simple. However, developing a large voltage across the resistor is desirable to provide a high signal-to-noise ratio (SNR). This implies a high resistance value which in turn leads to high power dissipation. Where the current to be measured is within an electronic power converter, a high SNR is particularly desirable due to the high level of ambient conducted and radiated electrical interference generated by power device switching transients.

Sense resistor	Simple	Large volume
	Accurate, but trimming operation may be required to attain required accuracy	No inherent galvanic isolation
	Good frequency response (provided low-inductance construction is implemented)	Relatively high "footprint" area may be required
		High power consumption
Use of parasitic resistance in power converter's choke	Low-cost, discrete resistor is not required	Choke's resistance and inductance need to be known for accurate measurement: difficult to achieve and both are temperature-dependent
	"Low-footprint" solution	No inherent galvanic isolation
Current-sensing MOSFET	Minimal extra circuitry	No inherent galvanic isolation
	Low losses	Unwanted spikes due to transformer action between power and current sense circuits
		Frequency response is limited
Hall-effect sensor (open-loop)	Accurate (1 % linearity error typical)	Expensive (gapped core and Hall-effect element required)
	Inherent galvanic isolation	Frequency response limited to approximately 200 kHz
Hall-effect sensor (closed-loop)	Very accurate (0.1 % linearity error typical)	Expensive (gapped core, Hall-effect element and compensating winding required)
	Inherent galvanic isolation	Frequency response limited to approximately 200 kHz
Rogowski coil	Accurate	Prone to time-dependent integral drift. Complex circuitry required to minimize this
	Inherent galvanic isolation	Cannot sense dc
		Accuracy dependent on physical dimensions and orientation of current-carrying conductor in coil's aperture
Current transformer	Accurate (0.1 % achievable provided the design takes account of distortion due to droop)	dc current cannot be sensed without additional circuitry
	Good high frequency response, however, a low frequency asymptote exists below which excessive droop results	Duty factor typically constrained to 90 % if saturation of core material is to be avoided
	Inherent galvanic isolation	

Table 1.1 Overview of the Principle Current Sensing Technologies

For high accuracy the resistive element has to be constructed from a material with a low temperature coefficient of resistance (TCR). Kelvin ("four-wire") connections are also desirable. With Kelvin connections, separate terminals are provided to connect a pair of power leads and a pair of sense leads to the resistor. The circuit formed by connecting the sense leads does not incorporate the junctions between the power leads and the resistor. Variations in the junction resistances, which are significant if the element resistance is low, therefore have a minimal effect on accuracy.

Another drawback with the sense resistor is its lack of inherent galvanic isolation. This may be required for safety reasons, to realize level-shifting or to minimize interference. Even where safety or interference considerations are not problematic, for example, in power converters where the control circuitry is referenced to the power conversion circuitry, a level-shifting capability may still be required. However, some manufacturers have produced ICs to perform this function, for example [3].

A variant of the sense resistor technique extracts the signal developed across the inevitable parasitic resistance in a power converter's choke from that across its terminals [4, 5]. This avoids the introduction of a discrete sense resistor and its consequent losses and "footprint" requirement. However, as the conductor material is invariably copper, with a TCR of approximately 0.39 %/°C, inaccuracy occurs due to thermal effects. Also, the "cold" resistance of the conductor may, in any case, be poorly defined as its cross-sectional area and length may vary between units due to manufacturing tolerances. Furthermore, the circuit extracting the signal needs to have a corner frequency matched to that formed by the choke's inductance and parasitic resistance. Variations in the inductance attributable to changes in the magnetic material tolerances and temperature are therefore also problematic.

1.3.2 The Current-Sensing MOSFET

A current-sensing MOSFET is shown in the circuit in Figure 1.2. In this device, one or more of the cells within the MOSFET are left in an "open-source" arrangement [6-

8]. The current through these cells is a small proportion, given by the "current sense ratio" (CSR), of the drain current. This current does not flow into the main source terminal but, instead, flows into a fourth terminal. It is then sensed by means of a burden resistor or an operational amplifier circuit. Some high-frequency problems are encountered [6, 7]. Firstly, the CSR varies during switching as the gate voltage changes and the device moves through its linear region. Secondly, in a practical device package, there is some magnetic coupling between the main and the signal-carrying source connections. This results in unwanted transient voltages being induced in the signal-carrying lead. In Figure 1.2 an operational amplifier in an inverting configuration is used to present a virtual ground connection to the sense connection. This has the advantage that the sharing ratio is unaffected by the emf which would be developed across a burden resistor. The value of the CSR is given by k_{CSR}.

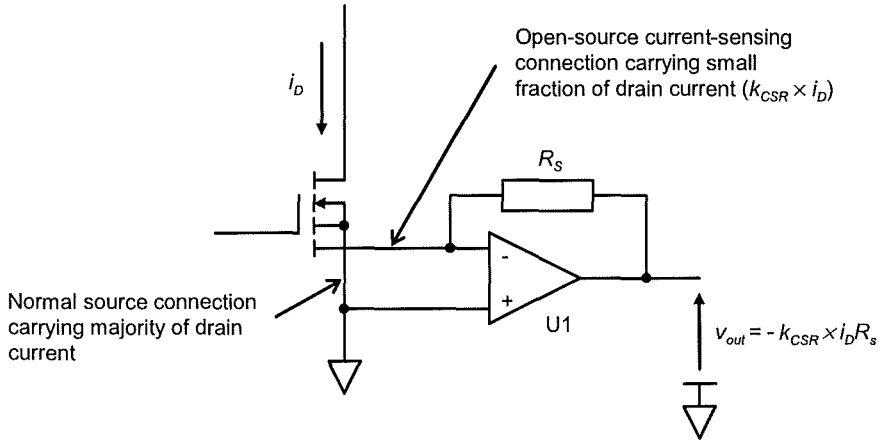


Figure 1.2. Current-Sensing MOSFET Circuit

1.3.3 Use of MOSFET On-State Resistance as a Sense Element

The MOSFET is one of the principle devices used in power converters and its on-state characteristic may be approximated as a resistance ($R_{DS(on)}$). The current through it can therefore be derived by sensing the voltage across its power electrodes. However, this resistance is normally subject to wide production tolerances. Although this can be

compensated for by using a set-on-test (SOT) procedure for individual units, accuracy is still poor as the $R_{DS(on)}$ value also has a positive temperature coefficient of approximately 0.9 %/°C. However, although not generally accurate enough for absolute measurement purposes, this technique is suitable for use in peak current control loops where it has been implemented in commercially available power control ICs [9]. An on-line technique for calibrating the voltage sensed across a MOSFET at the expense of increased circuit complexity is introduced in [10]. An auxiliary switch and a sense resistor are connected in parallel with the MOSFET and every 1000 or so cycles this network is switched on instead of the MOSFET to obtain an accurate current measurement for calibration purposes. As the sense network is only switched on occasionally, the effect on circuit efficiency is minimal.

1.3.4 The Hall-Effect Sensor

The Hall-effect sensor [11, 12] provides galvanic isolation, low losses from the circuitry under measurement and, particularly in its closed-loop variant, very good linearity (typically better than 0.1 %). The cost of this sensor is high, in particular in the case of the closed-loop type where, in addition to the Hall-plate and the core-gapping operation, a compensating winding is also required.

Although the losses seen by the power circuitry under measurement are low, the Hall-plate has to be supplied with an excitation current from the low-voltage control circuitry. Furthermore, the circuitry in the closed-loop variant has to supply some power to drive current through the secondary winding. Even where the current under measurement is zero, some additional "standby" current is still drawn by the closed-loop variant. This is because, to minimize "crossover" distortion, the secondary winding is driven from a Class-AB amplifier which inevitably draws some quiescent or "standing" current.

Whilst the linearity of the Hall-effect sensor is good, it may exhibit an offset error. This is primarily attributable to inconsistencies in the doping of the Hall-plate and

misalignments of the two voltage sense connections made to the Hall-plate. The error is also time and temperature dependent. One application in which the presence of an offset error may be particularly problematic is in grid-connected inverter topologies where it may lead to the unwanted injection of a dc current into the grid. However, a technique is presented in [13] where the output current of such an inverter is measured by a Hall-effect sensor which is continually self-calibrating.

Although exhibiting high dc accuracy, the Hall-effect sensor has a typical bandwidth of typically less than 200 kHz. It is therefore not always suitable for measuring instantaneous currents such as i_B in Figure 1.1 for the purpose of peak current control.

An arrangement similar to the Hall-effect sensor is the magneto-resistive sensor [14, 15] where a material exhibiting a change in resistance when exposed to an incident flux density is used as the detector element. Unlike the Hall-effect sensor, the signal derived from the device is symmetrical with respect to the null incident flux point and the direction of the current producing the flux is therefore more difficult to ascertain. The combined Wheatstone bridge and "barber-pole" technique described in [14] and [15] is used to address this difficulty. Another arrangement similar to the Hall-effect sensor is the magneto-impedance sensor [16].

The optical current transformer (OCT) [17] is similar in that a device senses the magnetic flux attributable to a current in a nearby conductor. The OCT exploits the Faraday effect where the polarization of a light beam in a material is changed by an incident flux density (depending on the material's "Verdet" constant). Although more complicated than other magnetic flux sensors, the OCT is attractive for use in transmission networks where the demanding insulation requirements between the grid voltage and monitoring equipment are readily met by the use of an optical fibre. Drawbacks are that it is sensitive to vibration and variations in temperature. (Although referred to as a "CT", the OCT does not operate as a transformer in the commonly-accepted sense where a voltage across a winding around a magnetic circuit induces a voltage across a second winding. It is therefore grouped here with the Hall-plate and other sensors which sense the flux density produced by a current under measurement.)

The Hall-effect sensor is usually manufactured as a purpose-built device. However, an alternative method [18] for realizing the open-loop variant is to embed the Hall-plate in the air-gap of an existing magnetic circuit, for example, a choke, located in the path of the current to be measured, as the flux density in the air-gap is, ideally proportional to the current in the choke's winding. This provides a low-cost and low-footprint solution. However, a compromise between the choke's physical size and the achievable accuracy is required. This is because the flux swing has to be restricted due to the non-linearity of the material's *BH* curve to attain improved accuracy.

1.3.5 The Rogowski Coil

The Rogowski coil [19, 20] may be used for sensing ac currents and return-to-zero current pulses. It exhibits galvanic isolation and low losses. As it is constructed around an air-cored coil, saturation of magnetic material and a consequent non-linear response are not problematic. It operates according to Ampere's and Faraday's Laws and yields an output voltage, v_{out}, given by:

$$v_{out} = \mu_0 N_l A_1 \frac{di}{dt} \tag{1.1}$$

where μ_0 is the permeability of free space, A_1 is the cross-sectional area within the toroidal shape formed by the coil and i is the current under measurement. The conductor carrying this current is normally passed once through the aperture encircled by the toroid. N_l is not the number of turns, but is the number of turns per unit length of the toroid. v_{out} is integrated, usually with operational amplifier circuitry to give a voltage proportional to the instantaneous current. As the integrator cannot be perfect, it inevitably exhibits integral drift. This precludes its use for measuring dc currents or current pulses above a certain length. A further issue is that the gain is dependent on the physical dimension "A_1". Therefore, to obtain high accuracy increased cost is incurred by the need to ensure that the coil is manufactured to specified tolerances or that the gain of the electronic circuitry is accurately calibrated. Another geometrical

consideration is that, for Equation (1.1) to be valid, A_1 has to be small compared to the area of the aperture enclosed by the toroid.

As an integrator is used, a high-tolerance capacitor is normally required for an accurate gain. This may be an expensive component when compared to other current sensors which rely for accuracy on a high-tolerance signal resistor. (Instead of operational amplifier circuitry, a simpler passive RC circuit may be used to realize an approximate integrator in low-specification applications.)

The Rogowski coil exhibits some sensitivity to the position of the current carrying conductor within its aperture and the angle at which the conductor enters the plane of the coil. It also exhibits some sensitivity to currents in conductors outside the coil's aperture. In particular, it acts as a "search" coil with one turn when subjected to fields from external current-carrying conductors and the more complicated central return-loop conductor arrangement described in [21] is required to alleviate this effect.

Power electronics applications for which the Rogowski coil has been found suitable are the measurement of phase winding currents in switched reluctance machines [22] and the sensing of transient current waveforms in insulated gate bipolar transistor (IGBT) modules [23] to assess the current distribution between die in parallel. In [22], the current waveforms being measured (in the case of non-zero speed operation) are return to-zero-current pulses and in [23] only transient information is required. Integrator drift is therefore not problematic in either of these applications as the sensor can be periodically reset. Another related application is for sensing currents in the rotor bars of an induction machine [24]. The Rogowski coil is suitable here as these currents do not have a dc component.

1.3.6 The Current Transformer

The CT cannot inherently sense dc currents and, in UCP sensing applications, exhibits droop and can only sense pulses up to a limited duty factor. However, provided these

limitations can be addressed, the CT is a feasible low-cost sensing technique in many power converter applications [25]. For switched-mode applications, the CT is usually constructed using a toroidal magnetic core carrying a single primary winding and a large number of secondary windings, typically between 100 and 500. Advantages of the toroidal shape are that very low leakage inductances are achievable and that the magnetic circuit is continuous without air gaps. The effective permeability of the magnetic circuit is therefore the same as that of the core material's permeability.

As mentioned in this chapter, the CT cannot inherently sense dc currents and the Hall-effect sensor has a limited bandwidth. However, hybrid sensors have been developed to address these problems which use a Hall-effect device to detect dc and low frequency currents in conjunction with a CT to sense high-frequency components and thus provide an extended bandwidth [26]. Another hybrid sensor combines a sense resistor and isolating amplifier arrangement with a CT to realize a dc current sensor with isolation and a high (1 MHz) bandwidth [27]. (Current sensing techniques other than the CT may be hybridized in a similar way. For example, a Hall-effect sensor may again be used to sense dc and low frequencies, but with a Rogowski coil to detect the high-frequency components [28]).

As shown in Figure 1.3, a burden resistor (R_B) is normally used to provide an output voltage proportional to the secondary and hence, ideally, the primary current. Unlike the closed-loop Hall-effect sensor the energy required to drive current through the secondary winding is drawn from the primary circuit. (An exception is found with electronically-assisted CT arrangements.)

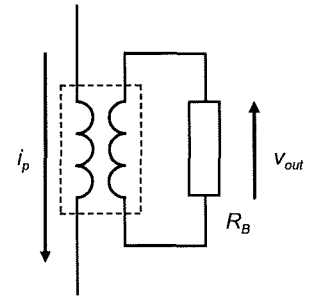


Figure 1.3. CT with Load (Burden) Resistance

The characteristic dimensions of the CT's magnetic circuit are its effective area and effective length. However, unlike the Rogowski coil, these dimensions do not affect the fundamental accuracy of the technique but, instead, only affect the error term attributable to the magnetizing current drawn.

It is frequently asserted that the CT is an expensive component, usually when it is compared with the sense resistor. However, a high-wattage and high-tolerance power resistor with a low TCR element material and Kelvin connections is not necessarily inexpensive. Also, cooling, and, if required, isolation or level-shifting requirements add to the cost of the sense resistor. An important practical point concerning cost is that, as the CT is normally constructed with one primary "turn", the primary to secondary isolation requirements are particularly easy to meet without incurring high cost. To do this, the primary conductor can normally carry a suitable layer of insulation or be sleeved to meet the "creepage" and clearance requirements specified by regulatory agencies. This is not usually the case with the other magnetic components found in a power converter, for example, the power voltage transformer.

CT's operating at switched-mode frequencies normally use "soft" ferrite core materials with a manganese-zinc (MnZn) active material due to the combinations of relatively high permeabilities and low core losses which are attainable with this material. "Soft" in this context means that the material has a low coercivity (H_c). The relatively low saturation flux density (B_{sat}) of these materials of 250-400 mT is generally not problematic in CT applications at power electronic switching frequencies.

The performance of a CT may be improved by operating it in an electronically-assisted mode where a tertiary flux-change sense winding is used [29]. The end of the secondary winding normally connected to the secondary circuit's reference voltage is instead connected to an amplifier which adjusts the terminal voltage in response to any flux-change detected by the tertiary winding. This minimizes the magnetizing current drawn, and hence the droop. Like the Rogowski coil, ac currents or current pulses may be sensed, but not steady-state dc currents. Although the technique has

been demonstrated to be suitable for cost-effective sensing of current pulses in automotive actuator applications, the particular permutation of performance improvement and complexity here is not necessarily optimal for switched-mode applications. In summary, the principal limitations of the CT are that:

- currents with a dc content cannot be sensed without the use of ancillary circuitry
- inaccuracy arises due to droop
- the duty factor of the current pulse it can sense is limited

These limitations and mitigating techniques are investigated in this thesis.

As stated in Section 1.1, an objective of the research presented in this thesis is to gain the best performance from the "simplest" physical CT construction. That is, generally a CT manufactured by laying a single secondary winding onto a continuous toroidal core shape. An assumption made is that the cost of using electronic circuitry to enhance the performance of a CT is low compared to implementing a more complex physical CT configuration, for example, using a tertiary winding as described in [29].

The Hall-effect sensor and CT are discussed separately in Sections 1.3.4 and 1.3.6. (For convenience, any technology which directly senses the flux attributable to a current under measurement is grouped with the Hall-effect sensor.) However, it may be argued that the closed-loop Hall-effect sensor is in effect an electronically-assisted CT. At high frequencies CT action is dominant whilst at low frequencies the action of the Hall-effect sensor dominates. It may also be regarded as an inherently hybrid current sensing method by default whereas in [26] a hybrid design is actively pursued.

In order to minimize droop in the signal obtained derived from a given CT three fundamental approaches may be taken, as summarized in Figure 1.4.

Firstly, the external impedance seen by the CT may be minimized, in turn minimizing the voltage impressed across its magnetizing branch.

Secondly, the CT's secondary terminal voltage may be actively controlled to minimize the voltage impressed across its magnetizing branch. This may be done in two ways: if the secondary series impedance of the CT is known, a voltage equal to the product of this impedance and the secondary current may be maintained at the CT's secondary terminals. This, ideally, results in zero voltage being impressed across the magnetizing branch. Alternatively, the voltage may be controlled by detecting and nullifying any flux in the CT's core. The flux may be detected directly or indirectly.

Thirdly, if the error introduced by current being drawn by the CT's magnetizing branch can be predicted, correcting terms may be introduced into the output signal.

Aspects of all three of these approaches are investigated in this thesis.

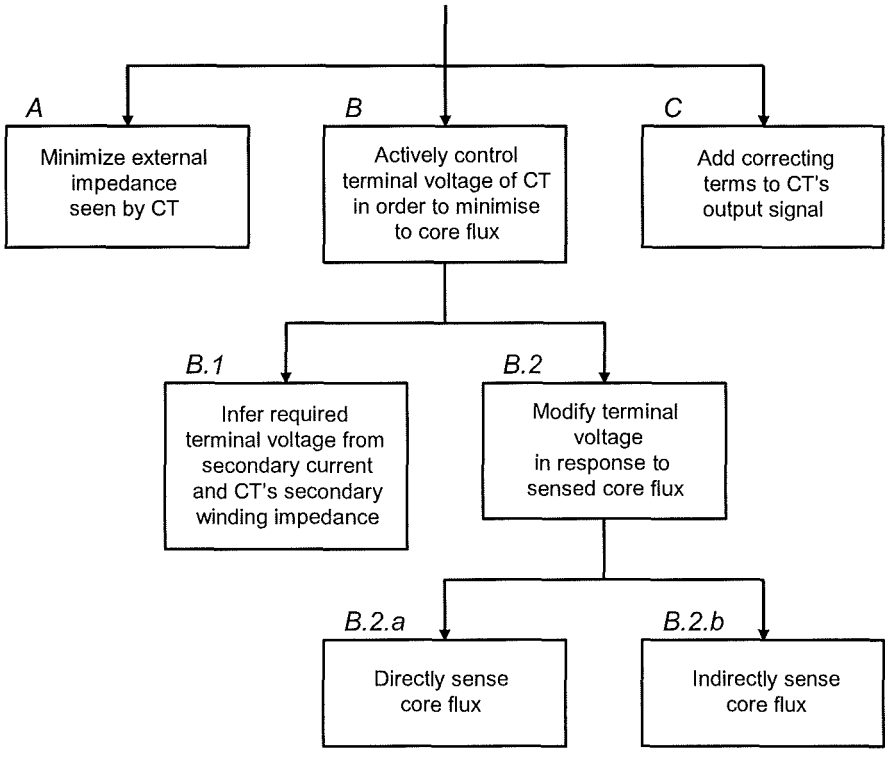


Figure 1.4. Classification of Methods for Minimizing Droop in the Signal Derived from a CT

1.4 Other CT Applications in Power Electronics

The use of the CT for current sensing and control in power converters is investigated here. However, CTs have been used in other electronics applications representing prior art of interest. These include regenerative base current supplies for the now virtually obsolete high-current bipolar junction transistor (BJT) [30, 31] and magnetrons [32].

Another application for the CT is in protecting the power semiconductor devices in inverters. Inverters are generally operated with average current control of their phase currents, particularly in high-performance applications where rotating machines are driven by implementing flux-vector control. Hall-effect devices are usually preferred for sensing the phase currents because of their inherent galvanic isolation and ability to operate with low-frequency and dc currents (for example, when zero-speed operation is required in a machine-drive application). However, local fast-acting over-current protection is normally incorporated within the power devices' gate driver circuits [33]. This is to protect the devices from failure should faults occur in the machine or the occurrence of simultaneous conduction (when the two devices in a voltage-sourced bridge-leg are erroneously turned on at the same time).

The IGBT is generally preferred as the power device in this application due to its low conduction losses at high voltage ratings. One technique for detecting over-currents is to monitor the collector-emitter voltage during the device's on-time and to trigger a latch to remove the gate drive signal if it becomes excessive. (This is similar to the technique in [9].) However, unlike the MOSFET, the *v-i* characteristic of the IGBT is approximated as a voltage sink in series with a relatively small slope resistance. Accurately setting the threshold trip current on the basis of the voltage observed across the power electrodes is therefore difficult with this technique. The CT, on the other hand, yields an output voltage proportional to the current being measured, making it useful for this application. Although galvanic isolation is not required here, as the inhibit signal is normally fed directly to the "high-side" section of the gate driver circuitry which is referenced to the IGBT's emitter potential, the combination

of low losses and high bandwidth nonetheless makes it attractive compared to the sense resistor.

A current-sensing IGBT structure for protecting against over-currents has been presented in [34]. This is similar to the current-sensing MOSFET in [6-8]. However, the commercial availability of these devices is low.

To directly measure the phase currents in a three-phase machine, three Hall-effect sensors may be used. Alternatively, to reduce the cost of these devices in a practical scheme, only two phase currents may be sensed with the current in the third phase being derived by means of Kirchoff's Current Law. To further reduce cost, the phase currents in a machine may be derived from a single current sensor located in the inverter's dc link conductor at the expense of additional processing circuitry [35].

Whilst it is current sensing that is addressed here, it is noted that the voltages in power converters may also be inferred from the sensed currents for control purposes [36]. The CT may therefore perform a dual function and negate the need for separate isolated voltage sensing elements.

1.5 Synchronous Rectification

Synchronous rectification (SR) is implemented in this thesis and is briefly discussed here. Figure 1.5 illustrates the principle behind SR [37]. Wherever a diode's forward voltage drop is problematic, an alternative arrangement is to replace it with a MOSFET. The MOSFET is turned on to allow it to conduct in reverse and turned off when biased in a forward direction to realize the blocking function of a diode.

Provided that the MOSFET has a sufficiently low $R_{DS(on)}$ value, conduction losses may be reduced. SR is frequently used in switched-mode power supplies with low output voltages where even a Schottky diode would incur a high voltage drop compared to the output voltage and hence reduced efficiency.

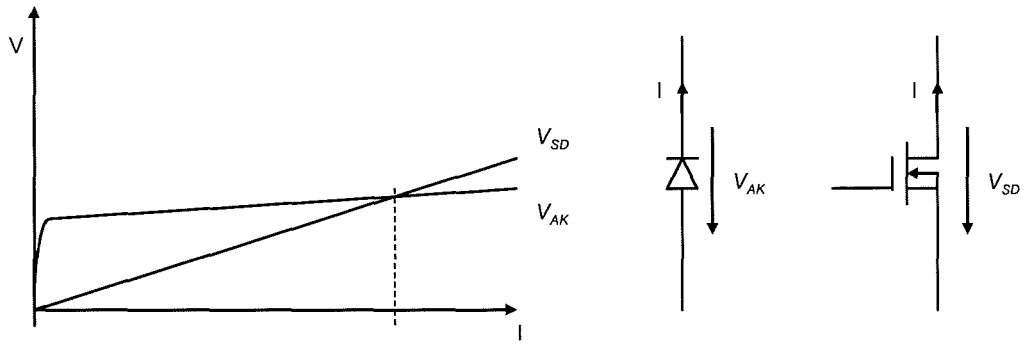


Figure 1.5. Principle of Synchronous Rectification

SR does, however, exhibit two principal drawbacks. Added complexity is usually introduced as circuitry is required to drive the SR MOSFET's gate terminal. Also, the transient behaviour of the MOSFET's intrinsic diode when regaining its blocking state at the end of a conduction period may be problematic. Difficulties include exacerbated turn-on losses in the complementary power semiconductor device due to the passage of recovery charge and the presence of electromagnetic interference (EMI) at the end of the recovery period when the diode regains its blocking properties [38].

Although other devices such as the BJT may be used for SR, the MOSFET is normally preferred due to its low on-state voltage drop, fast switching performance and the comparative ease with which its control electrode (the gate in this case) may be driven. In this thesis the application of SR in rectifying the output signal from a CT is investigated.

Techniques for deriving the drive signal for an SR device may be classified into three groups. In control-driven SR, the signal for the SR element is derived from that used to drive the main power device. In self-driven SR [39] a winding on a transformer or inductor is used to provide the SR MOSFET's gate-drive signal. Where the voltage appearing across an existing winding is at an appropriate amplitude it may be used directly. Otherwise, an auxiliary winding or a tapping taken from an existing winding is required. In current-driven SR, the current through the SR device is sensed, either

directly by means of a CT [40] or by sensing the voltage across its power electrodes [41, 42]. The resultant signal is then conditioned to provide a gate-drive signal for the SR device. Only control-driven SR is considered in this thesis. The principal advantage of the other two schemes, the incorporation of galvanic isolation, is not required from a CT's rectifier as this is realized by the CT itself.

Self-driven SR has another advantage in that the SR MOSFET's gate-drive signal is directly coupled to the rate-of-change in flux in a magnetic component. The rate of change in flux in the component is, in turn, directly related to the voltage applied to it by the action of power devices switching. Unlike control-driven SR where propagation delays through power devices have to be accounted for, the signal applied to the SR MOSFET therefore has near-perfect synchronization to the current changes at the power electrodes of the power circuit's devices. Self-driven SR does not therefore exhibit the same susceptibility to simultaneous conduction.

However, the problems of low efficiency, high losses and power device destruction resulting from simultaneous conduction are not applicable here, where a CT's output signal is being synchronously rectified. Furthermore, the inclusion of an auxiliary winding or tapping, required for all situations except where the winding voltage co-incides with that acceptable for driving the MOSFET's gate, adds increased complexity and expense. Also, the gate terminal of a MOSFET may typically only be driven over a maximum voltage ratio of three-to-one. That is, the ratio of the maximum safe voltage to the threshold voltage is three-to-one. The voltage range over which the power circuitry may operate is consequently constrained by this limitation.

Current-driven SR has the disadvantage that either an additional current sensing element or a voltage-sense amplifier is required, again increasing complexity and expense.

CHAPTER 2

REVIEW OF CURRENT TRANSFORMER CIRCUITS

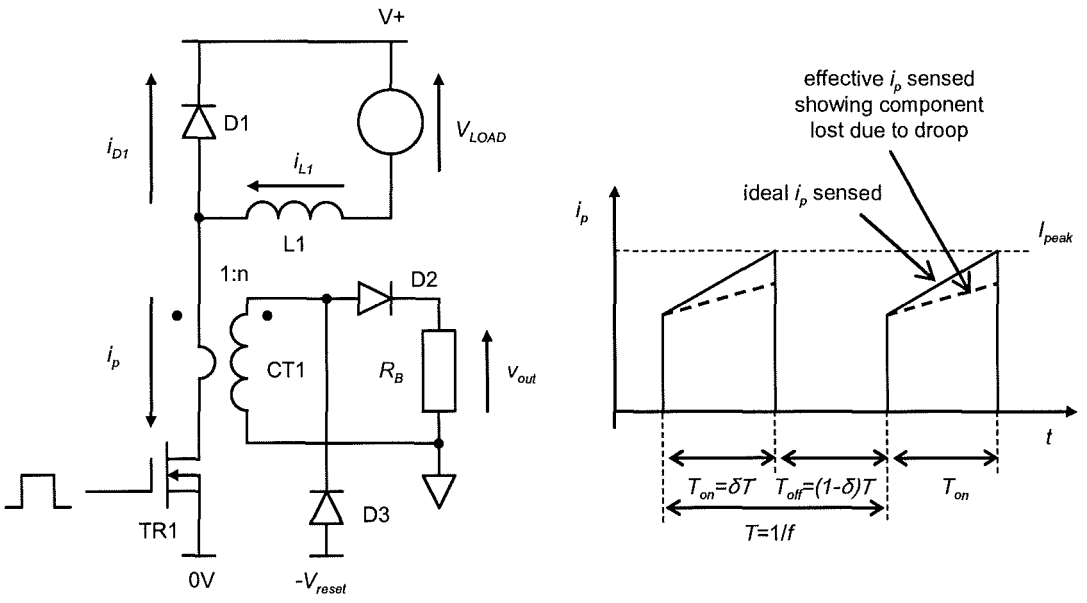
2.1 Introduction

Where the output signal from a CT has to be rectified for unidirectional current pulse (UCP) sensing [25, 43, 44], either diode rectification (DR) or synchronous rectification (SR) may be used. Both these options are discussed in this chapter. SR reduces distortion due to droop if the MOSFET has a sufficiently low on-state resistance. In addition, the duty factor at which the CT may operate before saturation of its core material occurs and accuracy is consequently reduced may be extended. However, for a given operating frequency, this is only achievable where the MOSFET's common-source output capacitance is sufficiently low as this capacitance combines with the CT's secondary magnetizing inductance to form a lightly damped resonant circuit, the oscillatory frequency of which defines the required reset time. Implementing SR may therefore increase the required reset time.

Three principle parameters of interest in evaluating the performance of a CT circuit are droop, maximum duty cycle and peak reset voltage. Droop is most frequently defined as the per-unit instantaneous drop in the sensed current present at the end of a rectangular current pulse. However, it may also be defined as the shortfall in the average current sensed over a switching period.

2.1.1 Unidirectional Current Pulse Sensing Using a CT

Figure 2.1(a) shows a CT used to sense the UCP conducted by the switch (TR1) in a buck converter. During TR1's on-time (T_{on}) the choke current (i_{L1}) flows through TR1 and the primary winding of CT1. CT's rectifier diode (D2) conducts its secondary current and, ideally, yields a signal (v_{out}) across the burden resistor (R_B) given by:



(a) Circuit Diagram (b) Waveforms

Figure 2.1. CT Sensing Unidirectional Current Pulse through Power Device

$$v_{out} = \frac{i_p R_B}{n} \tag{2.1}$$

where i_p is the current conducted by TR1 and n is the CT's turns ratio given by:

$$n = \frac{N_2}{N_1} \tag{2.2}$$

D3 may be included to connect the secondary winding of the CT across a defined voltage source, $-V_{reset}$, during the transistor's off-time (T_{off}), to reset the CT's core material. This is discussed in more detail later in this chapter.

Two principal problems arise with the CT. Firstly, as shown in an exaggerated and simplified form in Figure 2.1(b), distortion due to droop results as some of the primary current under measurement diverts away from the referred secondary winding and into the CT's magnetizing branch. (In accordance with convention, droop (D) is defined

here as the per-unit fall in the sensed current at the end of a rectangular current pulse [25, 43, 44].) Secondly, the maximum duty factor (δ_{max}) at which the power device operates has to be restricted to avoid saturation of the CT's core material.

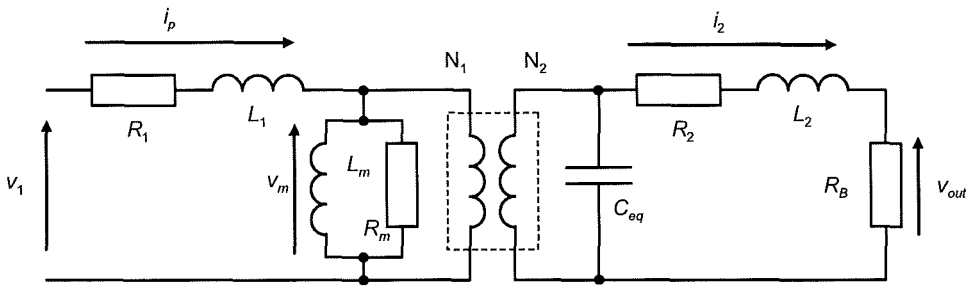
Droop is problematic as, in addition to impairing the accuracy of the average current measured, the triangular (ramp) component of the trapezoidal current measured in Figure 2.1(b) is reduced in magnitude with respect to the rectangular (step) component. Where the peak current is being sensed for control purposes, this effect tends to oppose the effect of the slope compensation necessary if sub-harmonic oscillation in the power converter's control system is to be avoided, as described in [44].

A restricted duty factor is problematic in various applications. In a buck converter a duty cycle near to 100 % may be desirable so that the converter can supply the required output voltage when the input voltage is low, that is, when a low "headroom" voltage is available. An example is in battery-powered applications where the required output voltage may be maintained for longer as the battery's terminal voltage falls with discharge.

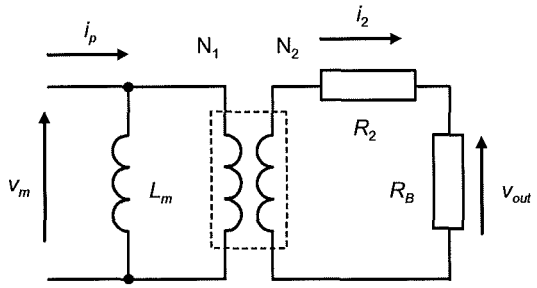
In the single-ended boost topology normally preferred for single-phase off-line power factor correction (shown in Figure 1.1) a power switch duty cycle up to 100 % is desirable when the input voltage is at zero in order to reduce crossover or "cusp" distortion. When a CT is used in series with the power switch, a compromise exists between avoiding this form of distortion and that resulting from CT saturation as the duty factor approaches 100 % [45].

2.1.2 CT Equivalent Circuits

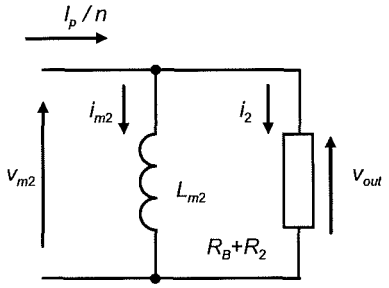
Figure 2.2(a) shows a transformer equivalent circuit. This is simplified here to give the circuit in Figure 2.2(b).



a) Conventional Transformer Equivalent Circuit



b) CT Simplified Equivalent Circuit



c) CT Simplified Equivalent Circuit with all Quantities Referred to Secondary Side

Figure 2.2. Transformer Equivalent Circuits

In addition to the ideal transformer, only the inductive component of the magnetizing branch (L_m) and the secondary winding resistance (R_2) are included. As the CT is fed from a current source (i_p) the primary winding resistance and leakage inductance (R_1 and L_1), both in any case small, are assumed not to affect the voltage (v_m) developed across the magnetizing branch. The flux excursion in a CT is normally very small and the resistive leg (R_m) of the magnetizing branch used to model core losses is often neglected. The secondary leakage inductance (L_2) is also often neglected in power converter applications as the CT is normally constructed with a toroidal core carrying an evenly spaced secondary winding.

Inter-turn and core-to-winding capacitances may be lumped and represented as an equivalent capacitance (C_{eq}) connected across the CT's secondary terminals. A high number of secondary turns (N_2) is desirable to reduce the amplitude of the secondary current. However, C_{eq} rises as N_2 is increased. Adverse consequences [46] are that the high-frequency performance of the CT is impaired and an increased reset time is required leading to a reduction in the duty factor at which the CT can operate.

It is noted that L_{m2} is given by:

$$L_{m2} = \left(\frac{N_2}{N_1}\right)^2 L_m \tag{2.3}$$

Ideally, the secondary current, i_2, in the load resistance is equal to the primary current, i_p, divided by n. However, as L_{m2} lies in parallel with the resistance formed by R_2 and R_B, it inevitably draws some of this current.

If i_p undergoes a step change from zero to I_p at $t = 0$, then i_2 decays according to:

$$i_2 = \left(\frac{N_1}{N_2}\right) I_p e^{\frac{-t}{\tau}} \tag{2.4}$$

where the circuit's time constant, τ, is given by:

$$\tau = \frac{L_{m2}}{R_2 + R_B} \tag{2.5}$$

R_2 may be neglected where it is much smaller than R_B. L_{m2} is given by:

$$L_{m2} = \frac{A_e \mu_0 \mu_r N_2^{\ 2}}{l_e} \tag{2.6}$$

The rate of decay of i_p can be lessened by reducing R_B which in turn increases τ. However, the voltage, v_{out}, developed across R_B by i_2 is now reduced and therefore has a smaller SNR.

Although the drop in current due to droop is exponential, if τ is much greater than T_{on} as is normally the case, then it may be regarded as linear. The per-unit droop (with all quantities referred to the secondary side) is therefore approximated as:

$$D = \frac{(R_2 + R_B)T_{on}}{L_{m2}} \tag{2.7}$$

2.1.3 dc Current Sensing

A limitation of the CT is that it cannot inherently sense non-return-to-zero dc currents such as the choke current (i_{L1}) in the converter shown in Figure 2.1(a) when it is operating in the continuous conduction mode (CCM).

However, methods are available for overcoming this limitation so that a single CT may be used directly in series with the choke to measure the current in it. These are described in this section.

2.1.3.1 Ancillary Circuitry for Core Material Resetting

Ancillary circuitry may be used to periodically reset the CT's core material [25, 47, 48]. Whilst the bandwidth of this arrangement may be satisfactory for average current control and sensing, it may be too low for effective peak current control or limiting for the purpose of switch protection. During the period when reset is taking place, measurement of the choke current is not possible. Accuracy may therefore be reduced as the current during the reset period has to be estimated.

2.1.3.2 Multi-vibrator Circuits

Another approach for dc current sensing is to incorporate the CT into a multi-vibrator circuit [49, 50]. This circuitry excites the secondary winding with an alternating voltage signal, the frequency of which is sufficiently low for the core material to become slightly saturated twice every cycle. That is, the flux density in it is made to approach $\pm B_{sat}$. When a dc primary current is applied, an asymmetrical ac flux excursion is now induced in the CT's core material. This effect is detected and a correcting secondary current is applied to restore the symmetry to the flux excursion. The average mmfs attributable to the primary and secondary currents have to cancel each other to yield zero average core flux. A burden resistor is normally used to develop a secondary voltage and this is given by Equation (2.1).

A variant of this technique uses two MOSFETs in conjunction with a CT to realise a simple multi-vibrator circuit [51]. However, a tertiary winding on the CT is required to drive the MOSFETs' gate terminals.

Although classified as a "CT" here, the use of multi-vibrator techniques may be classified with closed-loop Hall-effect sensors where a flux is detected and a restoring mmf is applied to drive the flux to zero. Effectively, the secondary winding acts as both a flux detector and also applies the compensating mmf.

High dc accuracy may be achieved using multi-vibrator circuits and a very simple CT construction may be used. However, the frequency response is low because of the need to remove the excitation signal from the circuit's output signal using a low-pass filter. The frequency of the excitation signal has to be low enough to swing the core's flux density through the material's linear range (from $+B_{sat}$ to $-B_{sat}$) to induce sufficient distortion to facilitate detection. The required frequency is proportional to the applied excitation voltage and inversely proportional to the flux swing, core effective area and number of secondary turns. When all these parameters assume practical values, a low excitation frequency is necessitated. The filter frequency has to be lower still, restricting the bandwidth of the output signal.

However, the asymmetrical flux excursion technique may be hybridized with a conventional CT to realize accurate high-bandwidth DC current transducers [52]. This system is relatively complex as three toroidal cores with associated windings and extensive processing circuitry is used. However, the cost and complexity is justified in some applications such as that in [52] where the currents in magnet drive circuitry for a particle accelerator have to be measured with high accuracy.

2.1.3.3 The Dual CT Circuit

As an alternative to the use of a single CT, the dual CT technique may be used [53] for dc current sensing. This is shown in Figure 2.3. A second CT is added to sense the current conducted by the power diode (D1) in Figure 2.1(a) and the CTs' outputs are added to yield the choke current (i_{L1}). The bandwidth achievable is such that peak current sensing as well as average current sensing may be implemented. Both the CTs are operating in the UCP sensing mode. Minimizing the droop and maximizing the duty factor that can be sensed by either or both may therefore be desirable.

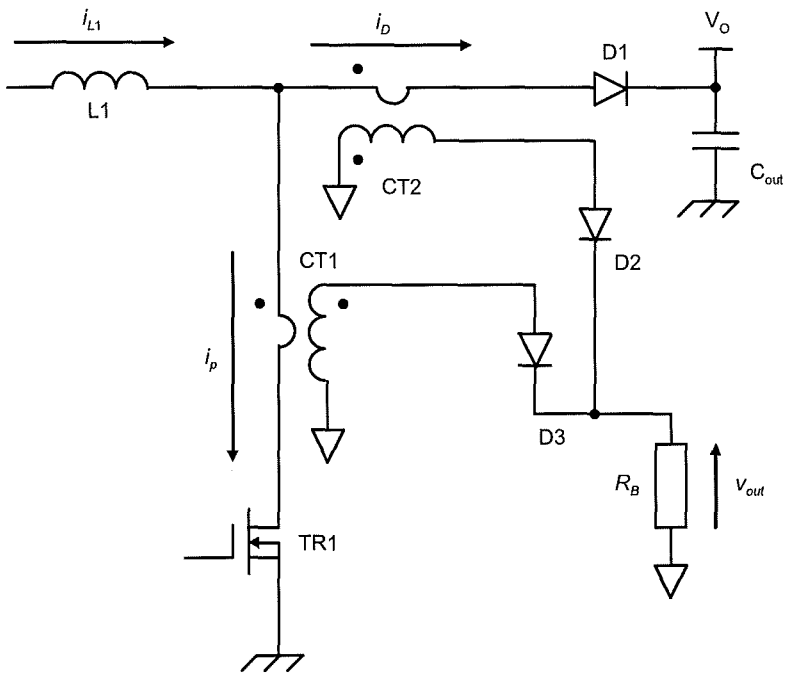


Figure 2.3. Dual CT Arrangement

A variant of the dual CT technique is described in [54] where the CTs are configured to sense pulse currents in both directions so that a bidirectional power converter can be controlled. An "integrated magnetics" approach is adopted in [54] to minimise the component count. Using this approach, the two CTs are assembled as one common component using a three-limbed magnetic core, the windings being configured so that the flux excursion produced by each CT has a minimal net effect on the other one.

The dual CT technique operates by adding the return-to-zero current pulses in a diode and power switch to obtain a resulting current elsewhere, normally in a power converter's input or output choke. A related technique is described in [55] where the two conductors carrying the power switch and diode currents in a power converter are led through the aperture of a single CT such that the currents in them tend to produce mmfs in opposite directions. The output is then conditioned to yield the choke current. However, low-pass filtering is required to extract the choke current and a compromise

has to be reached between having high dc accuracy and a high frequency response. This circuit is therefore unsuitable for peak current sensing.

One technique for sensing the average current in L1 without the use of a second CT uses a current synthesizer technique to estimate the choke current when TR1 is off. This is implemented in the PFC control IC described in [45]. A capacitor is charged up to a voltage proportional to the current in the power switch at the end of the current pulse. The capacitor is then discharged with a current proportional to the voltage across L1 during TR2's off-time. As this voltage has to be known or estimated, this is a complicating factor in applications where the control circuit has to be isolated from the power circuit. However, this voltage is generally sensed in any case for control purposes in the circuitry in [45]. In symmetrical isolated-output power converter topologies, the output choke current may be measured instantaneously using two CTs in the output rectifier circuit. Where instantaneous sensing is not required, the average choke current may be measured accurately using only one CT as the currents in each half of the rectifier circuit are virtually identical [56].

2.2 Rectifier and Load Arrangements

2.2.1 Current Pulse Sensing with Load Resistance and Diode Rectification

When the CT is used in the circuit in Figure 2.1(a), the voltage drop across the rectifier diode may be significant compared to that across the burden resistance. At power switch turn-off, the secondary magnetising current ($I_{m2(0)}$) is therefore given by:

$$I_{m2(0)} = \frac{\delta T}{L_{m2}}\left[V_f + \frac{i_p}{n}(R_2 + R_B)\right] \tag{2.8}$$

if it is assumed that the time constant of the circuit, given by Equation (2.5), is much greater than the pulse duration (δT). The droop is defined as:

$$D = \frac{nI_{m2(0)}}{i_p} \tag{2.9}$$

Putting Equation (2.8) into (2.9) and given that $T=1/f$ yields:

$$D = \frac{n\delta}{f \times i_p L_{m2}} \left[V_f + \frac{i_p}{n}(R_2 + R_B) \right] \tag{2.10}$$

Unlike the situation where the CT is used with a purely resistive load, as shown in Figure 2.2, the droop here is dependent on the magnitude of the current being sensed.

2.2.2 Current Pulse Sensing with Active Output Stage and Diode Rectification

Instead of connecting a burden resistance, R_B, across the output of the CT, as shown in Figure 2.1(a), the circuit in Figure 2.4(a) may be implemented [57]. The CT's secondary current flows into the node connected to the operational amplifier's inverting terminal. As the operational amplifier is connected in an inverting configuration it maintains this terminal at virtually the same potential as its non-inverting terminal which is connected to the zero-volt rail. The operational amplifier develops a voltage across R_F equal to i_2R_F. The polarity of the connection made to CT1 here is such that a positive output voltage is developed when the current pulse is present as this is generally more convenient for control purposes. If the voltage drop across D1 is neglected then each end of this winding is held at virtually the same potential by the feedback action of the operational amplifier, effectively short-circuiting it. The resistance seen in parallel with the magnetizing branch on the secondary side of the CT is now reduced from R_2+R_B to R_2. Consequently, τ is now increased from the value given in Equation (2.5) to:

$$\tau = \frac{L_{m2}}{R_2} \tag{2.11}$$

Although the resistance in parallel with the CT's magnetizing branch is now reduced from R_2+R_B to R_2, the forward voltage drop (V_f) from the rectifying diode (D1) still appears as shown in Figure 2.4(b).

If the voltage dropped across R_2 is small in comparison with that dropped across the diode then at power switch turn-off $I_{m2(0)}$ may be given by:

$$I_{m2(0)} = \frac{V_f \delta T}{L_{m2}} \tag{2.12}$$

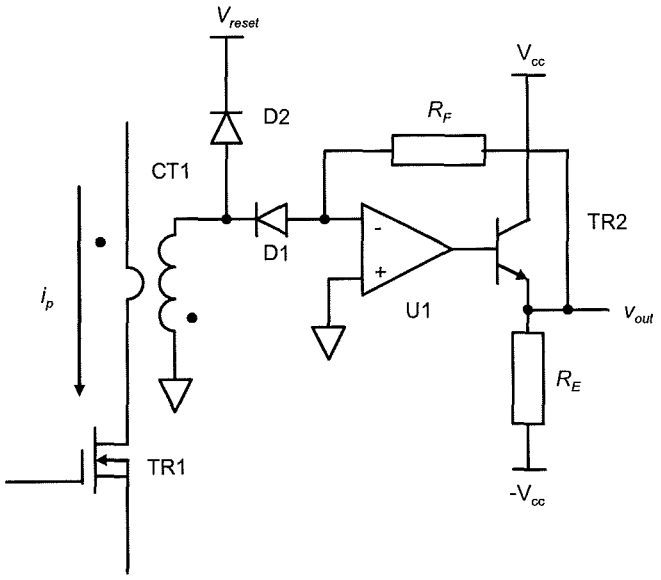
Putting this result into Equation (2.10) yields:

$$D = \frac{nV_f \delta}{f \times I_p L_{m2}} \tag{2.13}$$

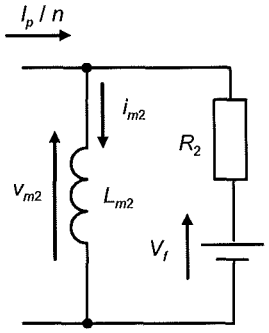
Again, unlike the situation where the CT is used with a load resistance, the droop here is now dependent on the magnitude of the current being sensed.

TR2 may be included to act as a Class-A amplifier to ensure that sufficient current may be driven through R_F where the operational amplifier's output is not able to source this current.

A resistor, R_E, is shown in the emitter of TR2. This is because the output voltage, v_{out}, may be required to go slightly negative during periods when the load current is zero in order to satisfy any offset voltage present at the operational amplifier's inputs. This resistor allows a negative voltage to appear and therefore prevents the operational amplifier's output from going to the negative rail when trying to source this voltage. The operational amplifier's transient response when TR1 is turned on and the load current is re-applied to the CT is therefore improved as its output voltage has to slew less before settling. (It is assumed here that R_2 is sufficient to allow the offset voltage to be developed with minimal current error. Where this is not the case, the CT may be ac-coupled to the operational amplifier [58].)



a) Circuit Realization



b) Equivalent Circuit from Figure 2.4(a) with all Quantities Referred to Secondary Side

Figure 2.4. Unidirectional Current Pulse Sensing with Active Load and Diode Rectification

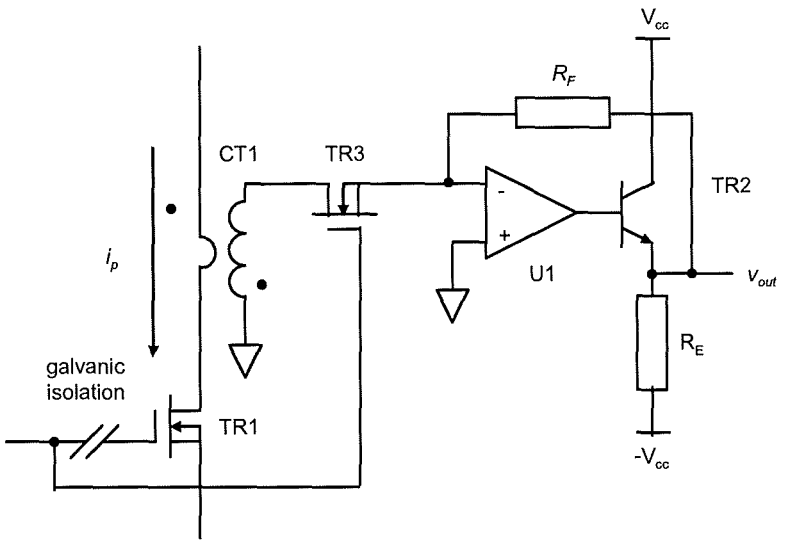
A drawback of using the active load compared to the passive load shown in Figure 2.1(b) is that, like the closed-loop Hall-effect sensor described in Section 1.3.4 and the multi-vibrator circuits described in Section 2.1.3.2, the CT's secondary current has to

be sourced by the power converter's low-voltage analogue circuitry. A further drawback is that the high-frequency performance of the operational amplifier may limit the response of the circuit to rapid current changes. Furthermore, the response of the operational amplifier to current pulses may be asymmetric. That is, the rise-time when a current pulse is applied may differ from the fall-time when it is removed. This is addressed in subsequent chapters and leads to some inaccuracy when sensing average currents.

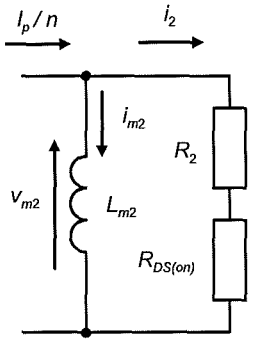
2.2.3 Current Pulse Sensing with Active Output Stage and Synchronous Rectification

The voltage drop across the rectifier diode may be reduced by the introduction of synchronous rectification (SR). The arrangement in Figure 2.4(a) is replicated in Figure 2.5(a) but, instead of a passive rectifying diode, a MOSFET (TR3) acting as a synchronous rectifier is used [59]. When the power device, TR1, is turned on TR3 is also turned on and its channel conducts in reverse. As shown in Figure 1.5, if the on-state channel resistance is sufficiently low, then the voltage developed across TR3's source-drain junction by the CT's secondary current is lower than that which would be incurred if it were to flow through a conventional passive diode. Again, the polarity of the connection made to CT1 is such that a positive output voltage is developed when the current pulse is present. As shown in Figure 2.5(a), where the signal used to drive TR1 is galvanically isolated before being applied to its gate, the signal prior to the isolation barrier may be used to drive TR3. One of the CT's principal advantages, the inherent galvanic isolation it provides, is therefore retained.

As outlined in Section 1.5, the control methods used for driving SR devices in power supplies may be classified as control-driven, self-driven or current driven, but only control-driven SR is considered here.



a) Circuit Realization



b) Equivalent Circuit from Figure 2.5(a) with all Quantities Referred to Secondary Side

Figure 2.5. Unidirectional Current Pulse Sensing with Active Load and Synchronous Rectification

Droop is calculated here using Equation (2.7) but with $R_{DS(on)}$ in place of R_B:

$$D = \frac{(R_2 + R_{DS(on)})T_{on}}{L_{m2}} \tag{2.14}$$

In terms of frequency and duty factor the droop is given by:

$$D = \frac{\delta(R_2 + R_{DS(on)})}{f \times L_{m2}} \tag{2.15}$$

Synchronous rectification can also be used in the dual CT arrangement. This is shown in Figure 2.6. By using an inverting logic gate (U2) the MOSFET rectifying the diode's CT output (TR4) is driven in anti-phase with the MOSFET rectifying the main switch's CT output (TR3).

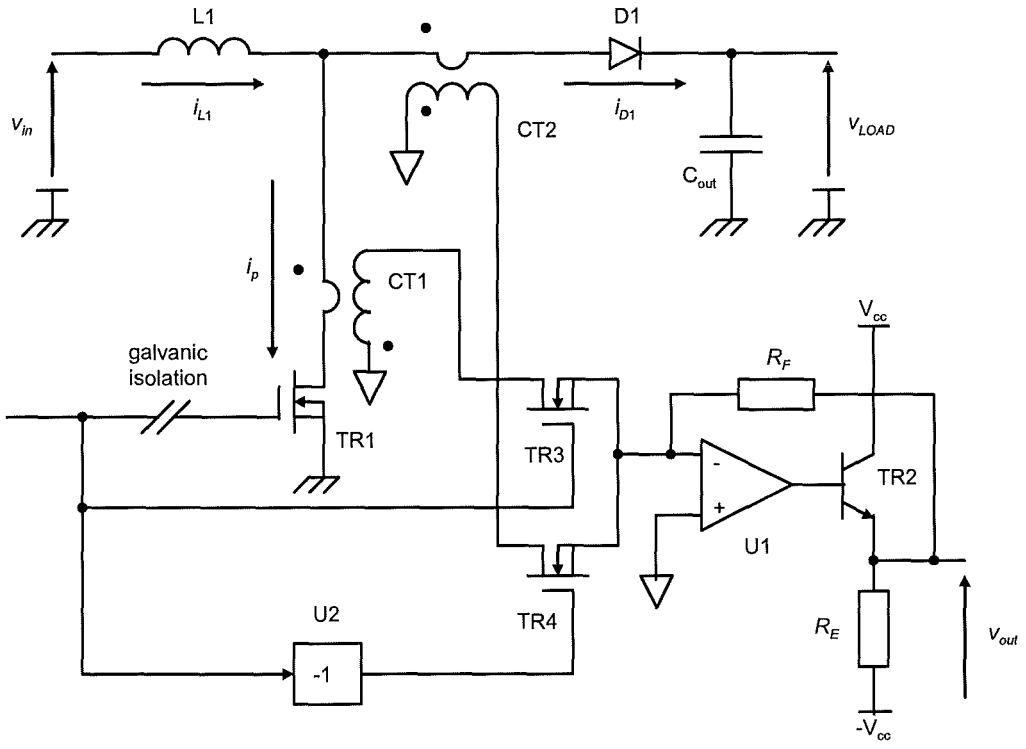


Figure 2.6. Dual CT Arrangement with Synchronous Rectification

Using an active stage and SR addresses droop attributable to the load resistance and rectifier diode respectively but the impedance of the CT still causes some voltage to be impressed across its magnetizing branch. In [60] both the resistive and inductive components of this voltage are minimized by introducing a compensating voltage dependent on the secondary current to the CT's secondary terminals. The application

addressed in [60] is for instrumentation-grade ac CTs used in mains-frequency applications where minimizing gain and phase errors is important. Another technique for enhancing the accuracy of ac CTs is described in [61] where droop and phase shift at low frequencies are compensated for by an analogue circuit which introduces compensating zeros and poles to cancel the error terms introduced by the CT's equivalent circuit. The feasibility of using a CT based around a small toroidal core with correcting circuitry to sense mains frequency (50 Hz) currents in an active power filter application is demonstrated in [61].

This approach is, however, not generally suited for use with the UCPT in power converter applications. This is because, although the fundamental frequency of the current waveform being sensed is generally fixed, it also has a changing series of harmonic terms as the width of the current pulse changes. In mains applications, the magnitudes of the harmonic terms relative to the fundamental are usually smaller. Another application where a CT is used with a corrected output signal based on the CT's known characteristics is in mains-frequency electronic integrating watt-meters [62] where digital, instead of analogue, circuitry performs the correction.

The error caused by the magnetizing current error can be corrected for by dropping the CT's turns ratio to account for the current components in L_m and R_m [63]. However, as described in [63], whereas L_m is linear, R_m is non-linear and varies with the primary current.

A problem addressed in both [62] and [63] is that the permeability of the material which defines L_m is subject to wide tolerances, as is the core loss characteristic which defines R_m. Furthermore, although a screening or set-on-test (SOT) approach may be taken to select components within narrow ranges, these quantities exhibit significant temperature dependencies.

2.3 CT Resetting Behaviour

2.3.1 Resetting into a Discrete Voltage Clamp Circuit

A maximum duty factor restriction is imposed upon the operation of a CT to avoid progressive ("staircase") saturation of its core material. Initially here, it is assumed that C_{eq} is negligible. If the positive and negative volt-second products appearing across the secondary winding of the CT during a switching cycle are not equal then the resultant dc voltage component will cause core saturation. Based on Faraday's Law:

$$v = N\frac{d\phi}{dt} \tag{2.16}$$

and with respect to the waveforms shown in Figure 2.7, it can be seen that if the CT is to be fully reset, that is, if the flux in the core is to be returned to zero during a switching cycle:

$$\int_0^{T_{on}} v_{m2}(t)dt + \int_{T_{on}}^{T} v_{m2}(t)dt = 0 \tag{2.17}$$

where the same winding is used for both fluxing and resetting the core and the voltage drops across the CT's series impedances are taken as negligible. To maintain the condition in Equation (2.17):

$$V_{forward}T_{on} \leq |V_{reset}|T_{off} \tag{2.18}$$

For simplicity here, the current pulse in the CT's primary winding is approximated as rectangular. $V_{forward}$, although described more accurately as a decaying exponential waveform, is shown in Figure 2.7 as a dc quantity for the purpose of assessing the maximum allowable duty factor as T_{on} is much smaller than τ, where τ is given by Equation (2.5).

As T_{on} and T_{off} are equal to δT and $(1\text{-}\delta)T$ respectively, then putting these results into Equation (2.18) and rearranging it gives:

$$\delta_{\max} = \frac{|V_{reset}|}{V_{forward} + |V_{reset}|} \tag{2.19}$$

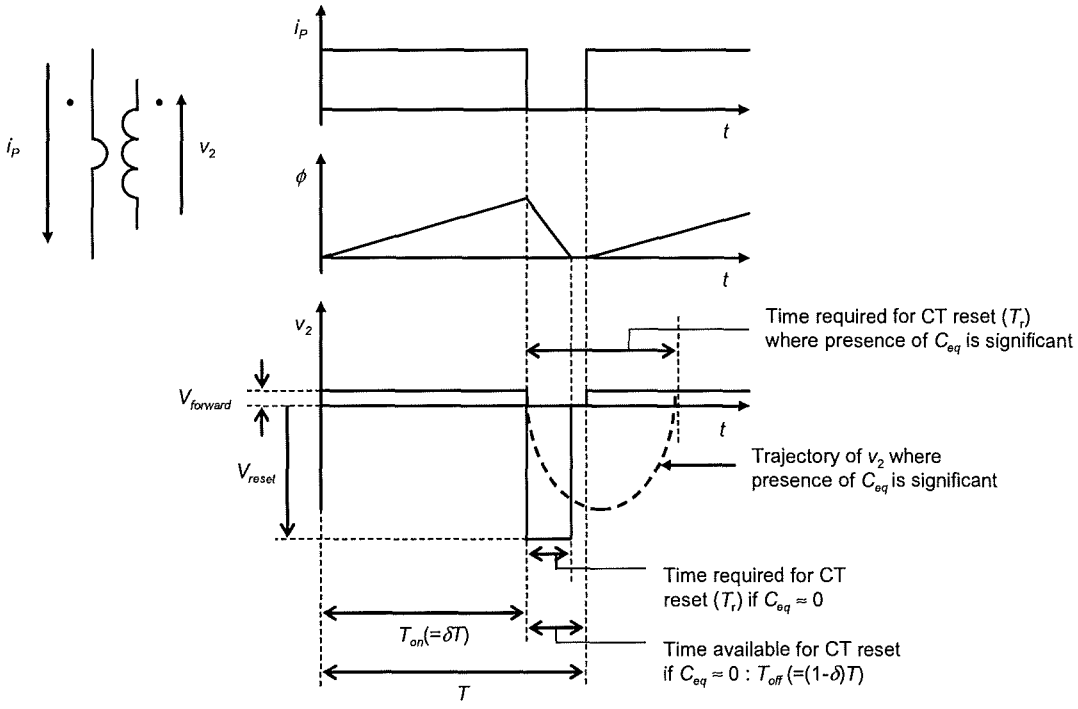


Figure 2.7. CT Reset Waveforms

From Equation (2.19) it can be seen that minimising $V_{forward}$ allows operation at a duty factor closer to 100 % for a given reset voltage (V_{reset}). A voltage rail between 5 and 15 V is typically available in a power control circuit. If a Schottky diode rectifier with a forward voltage drop of approximately 500 mV is used then a maximum duty factor of approximately 91 to 97 % is predicted from Equation (2.19) as the reset voltage is varied between 5 and 15 V. However, this estimate of the maximum duty factor does

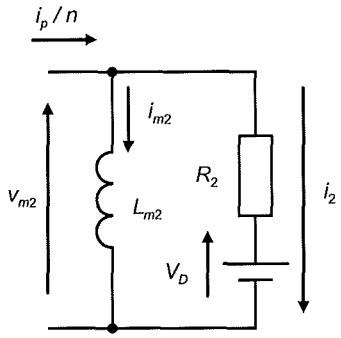
not account for the effect of the CT's parasitic capacitances during resetting. This is discussed in Section 2.3.2.

2.3.2 Natural Resetting into Stray Capacitances

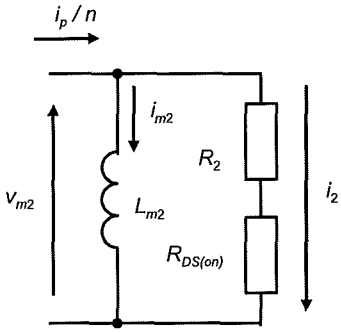
Instead of using a voltage sink to limit the voltage supported by the diode, the diode reset voltage may be unrestricted, and the CT may be reset by allowing it to resonate with the lumped capacitance of the CT and the diode or SR device. This is investigated in [53]. However, the rectifier has to be able to support the peak resetting voltage. Although a more sophisticated distributed model may be used as described in [64, 65], the capacitance here is assumed to be lumped.

Where this lumped parasitic inter-turn and winding-to-core capacitance (C_{eq}) is significant, the rectangular approximation of the CT's resetting behaviour shown in Figure 2.7 become inappropriate. As well as affecting the transient and high-frequency response of the CT, C_{eq} also presents a limitation on the minimum reset time required by the core. This is addressed in [53] and [59]. Figures 2.8(a) and 2.8(b) show the CT equivalent circuits referred to the secondary side during T_{on} for both diode rectification and SR respectively. C_{eq} is omitted in each of these circuits. Figure 2.8(c) shows the equivalent circuit during T_{off} for both DR and SR. An important point here is that, whilst it may limit the reset voltage, adding a reset clamp diode will extend the minimum reset time required. This is because it limits the rate at which the required volt-second product is accumulated.

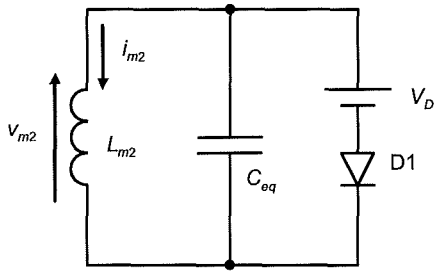
Although, as shown in Figure 2.8(c), the same topology is applicable during T_{off} for both DR and SR, C_{eq} is larger with SR due to the presence of the MOSFET's common-source output capacitance (C_{oss}). A perfect diode (D1) in series with an emf (V_f) is shown in parallel with C_{eq}. In the diode rectifier this represents the diode characteristic. In the SR arrangement it represents the MOSFET's intrinsic diode.



a) Equivalent Circuit from Figure 2.4(a) during T_{on}



b) Equivalent Circuit from Figure 2.5(a) during T_{on}



c) Equivalent Circuit from Figures 2.4(a) and 2.5(a) during T_{off}

Figure 2.8. Summary of CT Equivalent Circuits

The equivalent resistance representing the sum of the core material losses (R_m) which lies in parallel (R_{m2} when referred) with L_{m2} is neglected here. This is because it is much larger than the critical resistance (R_C) required in this location to cause significant damping. The circuit is therefore taken as only very lightly damped, that is:

$$R_{m2} >> R_C \tag{2.20}$$

where R_C is given by:

$$R_C = \frac{1}{2}\sqrt{\frac{L_{m2}}{C_{eq}}} \tag{2.21}$$

R_2, which lies in series with L_{m2}, is also neglected because, in this case, it is sufficiently small. Figure 2.9 shows the effect of C_{eq} on the reset voltage. If power switch turn-off takes place at $t = 0$ then $i_{m2}(t)$ is given by:

$$i_{m2}(t) = I_{m2(0)}\cos(\omega_r t) \tag{2.22}$$

over the interval from $t = 0$ to $t = \pi/\omega_r$ where ω_r is given by:

$$\omega_r = \frac{1}{\sqrt{L_{m2}C_{eq}}} \tag{2.23}$$

$v_2(t)$ lags the current by $\pi/2$ radians and is given by:

$$v_2(t) = I_{m2(0)}\sqrt{\frac{L_{m2}}{C_{eq}}}\sin(\omega_r t) \tag{2.24}$$

The peak voltage occurs when at $t = \pi/2\omega_r$ when $\sin\omega_r t = 1$ and is therefore:

$$v_2(pk) = I_{m2(0)}\sqrt{\frac{L_{m2}}{C_{eq}}} \tag{2.25}$$

D1 conducts again after the oscillation has completed a half-cycle (at $\omega_r t = \pi$ radians). It is noted that, in Figure 2.9, D1 ceases conducting before the current pulse is re-applied. However, both this and the situation where D1 is still conducting when the current pulse is re-applied are addressed in this thesis.

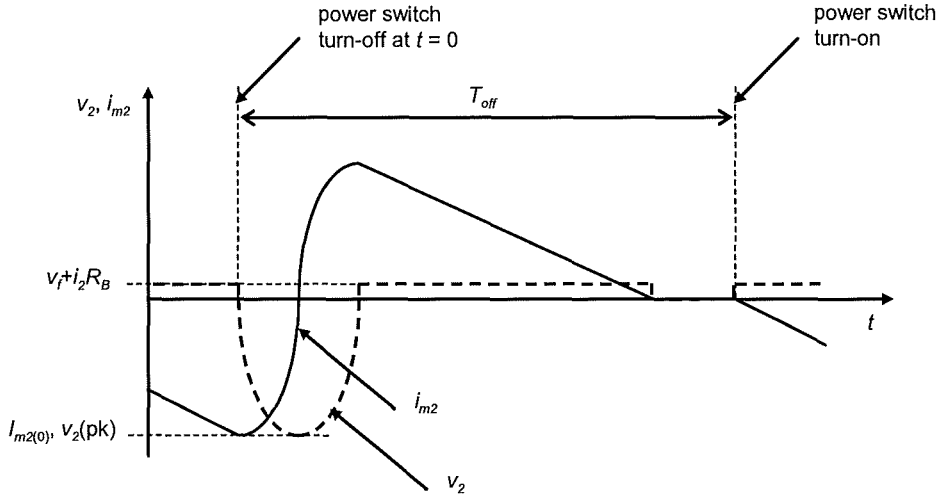


Figure 2.9. CT Reset Waveforms with Natural Resetting into Stray Capacitances

An active technique for resetting the core is presented in [66] where a tertiary winding on the CT is driven with a reset current pulse derived from a current source and synchronised to the operation of the power switch. This allows the CT to be driven at high duty factors.

2.3.2.1 Natural Resetting with Diode Rectification and Load Resistance

ω_r is given by Equation (2.23). In this case, $I_{m2(0)}$ is given by Equation (2.8). Putting this into Equation (2.25) gives:

$$v_2(pk) = \frac{\delta T}{\sqrt{L_{m2}C_{eq}}}\left[V_f + \frac{i_p}{n}(R_2 + R_B)\right] \tag{2.26}$$

The time required for reset (T_{reset}) that is, for $i_{m2}(t)$ to reach zero, is given by:

$$T_{reset} = \pi\sqrt{L_{m2}C_{eq}} \tag{2.27}$$

T_{reset} is a half of the CT's oscillatory period (T_r) and is independent of the magnitude of $I_{m2(0)}$ assuming that both L_{m2} and C_{eq} are linear. Given that $\delta_{max} = (T\text{-}T_{reset})/T$ and also that $T=1/f$ then the maximum duty factor, δ_{max}, is given by:

$$\delta_{\max} = 1 - f\pi\sqrt{L_{m2}C_{eq}} \tag{2.28}$$

2.3.2.2 Natural Resetting with Diode Rectification and Active Load

Again, ω_r is given by Equation (2.23) and $v_2(pk)$ is given by Equation (2.25). However, in this case $I_{m2(0)}$ is given by Equation (2.12). This is put into Equation (2.25) to yield:

$$v_2(pk) = \frac{\delta \times V_f}{f\sqrt{L_{m2}C_{eq}}} \tag{2.29}$$

T_{reset}, and the maximum duty factor are again given by Equations (2.27) and (2.28).

2.3.2.3 Natural Resetting with Synchronous Rectification and Active Load

The CT's resetting behaviour is reconsidered here with SR. The resetting voltage appearing is again calculated using Equation (2.25). However, in the case of SR, $I_{m2(0)}$ is given by:

$$I_{m2(0)} = \frac{\delta \times I_p (R_2 + R_{DS(on)})}{nfL_{m2}} \tag{2.30}$$

Putting this result into Equation (2.25) yields:

$$v_2(pk) = \frac{\delta \times I_p (R_2 + R_{DS(on)})}{nf\sqrt{L_{m2}(C_{eq} + C_{oss})}} \tag{2.31}$$

given that C_{eq} is now augmented by C_{oss}. The maximum duty factor is now given by:

$$\delta_{\max} = 1 - f\pi\sqrt{L_{m2}(C_{eq} + C_{oss})} \tag{2.32}$$

2.4 Summary of Alternative Rectifier and Load Arrangements

To summarize, the effects of DR and SR arrangements on the desired CT parameters are shown in Table 2.1. Maximising δ_{max} and minimising droop and $v_2(pk)$ are desired. The peak voltage ($v_2(pk)$) appearing across the rectifier is of interest as it has a bearing on whether a Schottky diode is used in place of a *p-n* diode. Whilst the Schottky diode cannot withstand as high a peak voltage as the *p-n* diode, it is noted that $v_2(pk)$ is dependent on the diode's forward voltage drop which is lower in the case of the Schottky diode.

A low magnetizing inductance allows δ_{max} to be increased. However, both droop and $v_2(pk)$ are exacerbated. Different expressions are used with DR and SR for calculating droop and the peak reset voltage. The same expression is used for calculating δ_{max} in

both DR and SR cases. However, with SR, C_{eq} is now larger. As described in [59], when SR is introduced C_{eq} is augmented by C_{oss}. This latter capacitance is non-linear and falls with applied voltage.

Several corollaries [67] result when a high-permeability MnZn material is used, that is, one with a high ratio of Zinc to Manganese in its active material. These are relatively high core losses, a low saturation flux density (B_{sat}) and a low Curie Temperature (T_C). The core losses and the consequent temperature rise are not normally problematic in CT applications as, in practice, the flux density excursion is restricted to a very low level. However, maximising T_C is desirable for operation in high ambient temperatures. Examples include automotive applications where "under-hood" and "on-engine" temperatures may be rated at 125 °C and 140 °C respectively [68]. This necessitates some reduction in the material permeability.

A feature of the ring core shape when implemented with a ferrite material is that the ratios of its dimensions are relatively fixed and different core aspect ratios are not compared here. Varying the outer diameter (d_o) and height (h) significantly from their typical proportions with respect to the inner diameter (d_i), for example, $d_o/d_i/h$ = 9/6/3 for a Ferroxcube TN9/6/3 ring core, is deemed impractical. This is due to manufacturing and other practical considerations such as the brittleness of ferrite materials and the need to avoid breakages.

In a typical off-line power converter currents of between 1 A and 10 A may be sensed by a CT. d_i may therefore be made small without exceeding the allowable current density, J, in either the primary or secondary conductors. J is typically between 5×10^{-6} and 10×10^{-6} A/m^2 for a physically small component, depending on factors such as the ambient temperature, allowable temperature rise, orientation and cooling regime. However, automated winding of such physically small components may be rendered more difficult and robustness may be a more important consideration in defining the cross-sectional area of the secondary conductor.

Parameter	Diode rectification with burden resistance	Diode rectification with active load	Synchronous rectification with active load
δ_{max}	$1-f\pi\sqrt{L_{m2}C_{eq}}$		$1-f\pi\sqrt{L_{m2}(C_{eq}+C_{oss})}$
D	$\frac{n\delta}{fi_pL_{m2}}\left[V_f+\frac{i_p}{n}(R_2+R_B)\right]$	$\frac{nV_f\delta}{fI_pL_{m2}}$	$\frac{\delta(R_2+R_{DS(on)})}{fL_{m2}}$
$v_2(pk)$	$\frac{\delta}{f\sqrt{L_{m2}C_{eq}}}\left[V_f+\frac{i_p}{n}(R_2+R_B)\right]$	$\frac{\delta V_f}{f\sqrt{L_{m2}C_{eq}}}$	$\frac{\delta I_p(R_2+R_{DS(on)})}{nf\sqrt{L_{m2}(C_{eq}+C_{oss})}}$

Table 2.1. Summary of CT Performance Parameters for Different Load Arrangements

2.5 Average Current Droop and Resonant Operation of the CT

If the energy in the CT's core is completely dissipated during the reset interval, the average current droop (D_{ave}) may be calculated by dividing the peak current droop by 2. In the DR case, D_{ave} is given by:

$$D_{ave}=\frac{nV_f\delta}{2fL_{m2}I_p} \tag{2.33}$$

In the SR case, D_{ave} is given by:

$$D_{ave}=\frac{\delta(R_2+R_{DS(on)})}{2f\times L_{m2}} \tag{2.34}$$

However, without a discrete reset voltage clamp, the behaviour of the CT during reset is resonant. It is noted in Section 2.3 where resonant resetting is described that, after a half resonant period has elapsed, the magnetizing current flows into the rectifier diode when the current pulse is removed. The effect of this on both average and peak current droop is investigated in more detail in subsequent chapters.

CHAPTER 3

THE UNIDIRECTIONAL CURRENT PULSE TRANSFORMER WITH DIODE RECTIFICATION AND NATURAL RESETTING

3.1 Introduction

The objective in this chapter is to investigate and quantify the average current droop in a UCPT when used with diode rectification, an active load and natural resetting, as described in Section 2.3. During a current pulse, some current diverts into the CT's magnetizing branch, storing energy. However, when the current pulse ends this energy is dissipated either in the form of losses in the CT or in external circuitry. In addition to acting according to the same principle as a forward transformer, the CT also effectively acts as if it were operating within a flyback (effectively an isolated-output buck-boost) converter. Three distinct operating modes are identified and investigated here. These are the discontinuous magnetizing current mode (DMCM), continuous magnetizing current mode (CMCM) and discontinuous secondary current mode (DSCM).

Being able to sense average currents in a power converter accurately despite the presence of a high peak current droop is useful, as in many applications average current control may be adequate or even advantageous [69] when compared to peak current control.

3.2 Theory of Resonant CT Operation with Lossless Core Material

Figure 3.1 shows a current pulse being applied to a CT in the circuit in Figure 2.4(a). The magnetizing current (i_{m2}) ramps up during the pulse and subtracts from the secondary terminal current, i_2. When the pulse is removed, a half oscillation occurs, the period of which is determined by L_{m2} and C_{eq}. At $t = \pi/\omega_r$ the voltage, v_2, across

the CT's secondary terminals changes direction and i_{m2} flows into the diode which clamps v_2. It can be seen that some of the magnetizing current-time product lost during the pulse's on-time is returned to the CT's output terminals during its off-time. The average current droop may therefore be substantially less that predicted from Equations (2.33) and (2.34).

In the centre waveforms, i_{m2} has decayed to zero, after an interval t_c, before the current pulse is re-applied. This is referred to here as the discontinuous magnetizing current mode. The lower waveforms show a situation where i_{m2} has not reached zero prior to the re-application of the current pulse. This is referred to here as the continuous magnetizing current mode.

Although the core flux passes through zero in the continuous mode, the term "discontinuous" is used here to refer to a state where the core flux settles at zero for a finite period.

V_{f1} is the rectifier diode's voltage drop seen during T_{on}. V_{f2} is the voltage drop seen when the core flux has reversed and i_{m2} is decaying linearly. Where diode rectification is used, V_{f1} is invariably greater than V_{f2}. This is because during T_{on}, the current in the rectifier diode comprises the referred primary current less i_{m2} whereas during T_{off} only the decaying i_{m2} flows. As i_{m2} is normally much less than i_2, typically by a factor of at least ten or more, the diode is operating at a significantly different point on its *v-i* characteristic. It is noted that V_{f1} is the external voltage drop, but the voltage impressed across the CT's magnetizing branch is the sum of this voltage and the voltage developed across R_2 by i_2. However, this latter voltage drop may be small enough compared to V_{f1} to be neglected. It is also assumed that the voltage drop over the CT's secondary leakage inductance is negligible.

In the lowest set of waveforms in Figure 3.1, the ratio of V_{f1} to V_{f2} is exaggerated to be much greater than that likely to be encountered in a practical circuit.

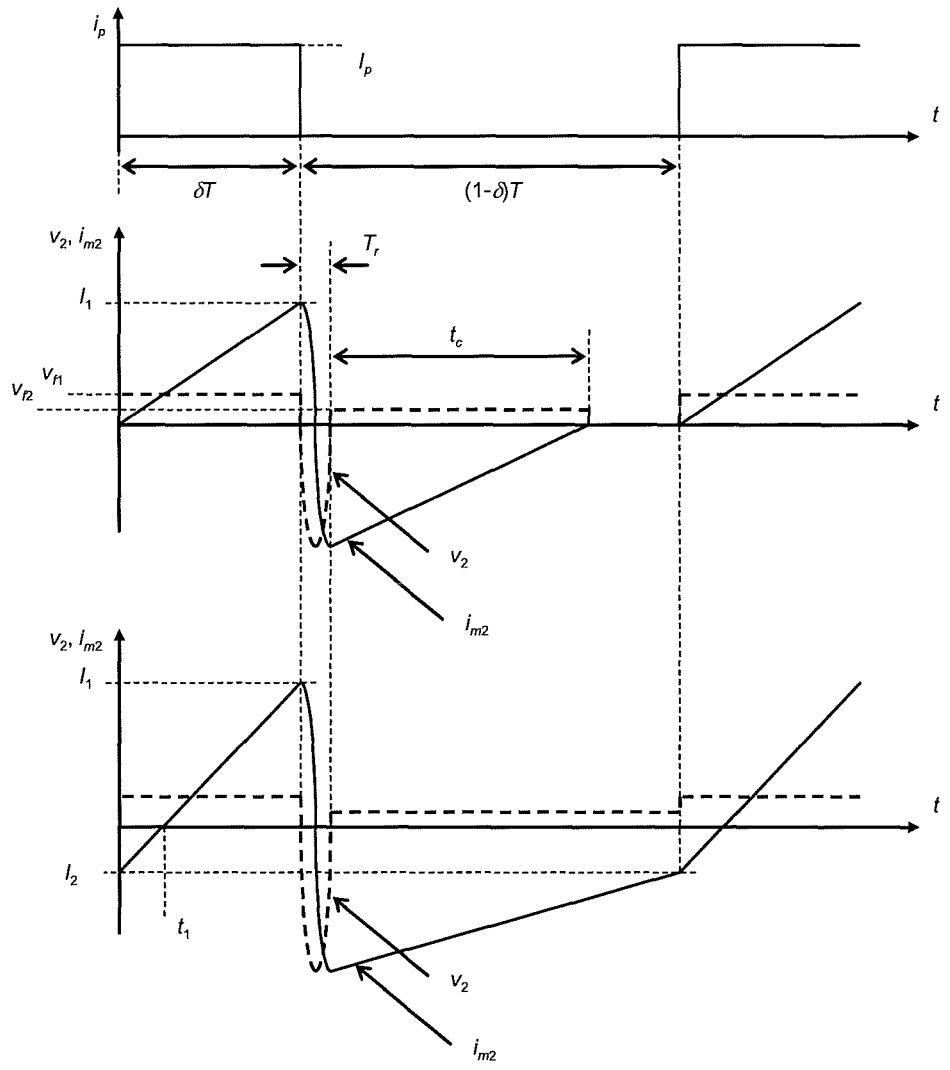


Figure 3.1. CT Magnetizing Current in Discontinuous and Continuous Modes

In considering the effect of the net i_{m2} over a switching period on average current droop, Figure 3.1 is simplified here to give Figure 3.2 where the oscillatory period is neglected and the change in direction of i_{m2} is taken as occurring instantaneously.

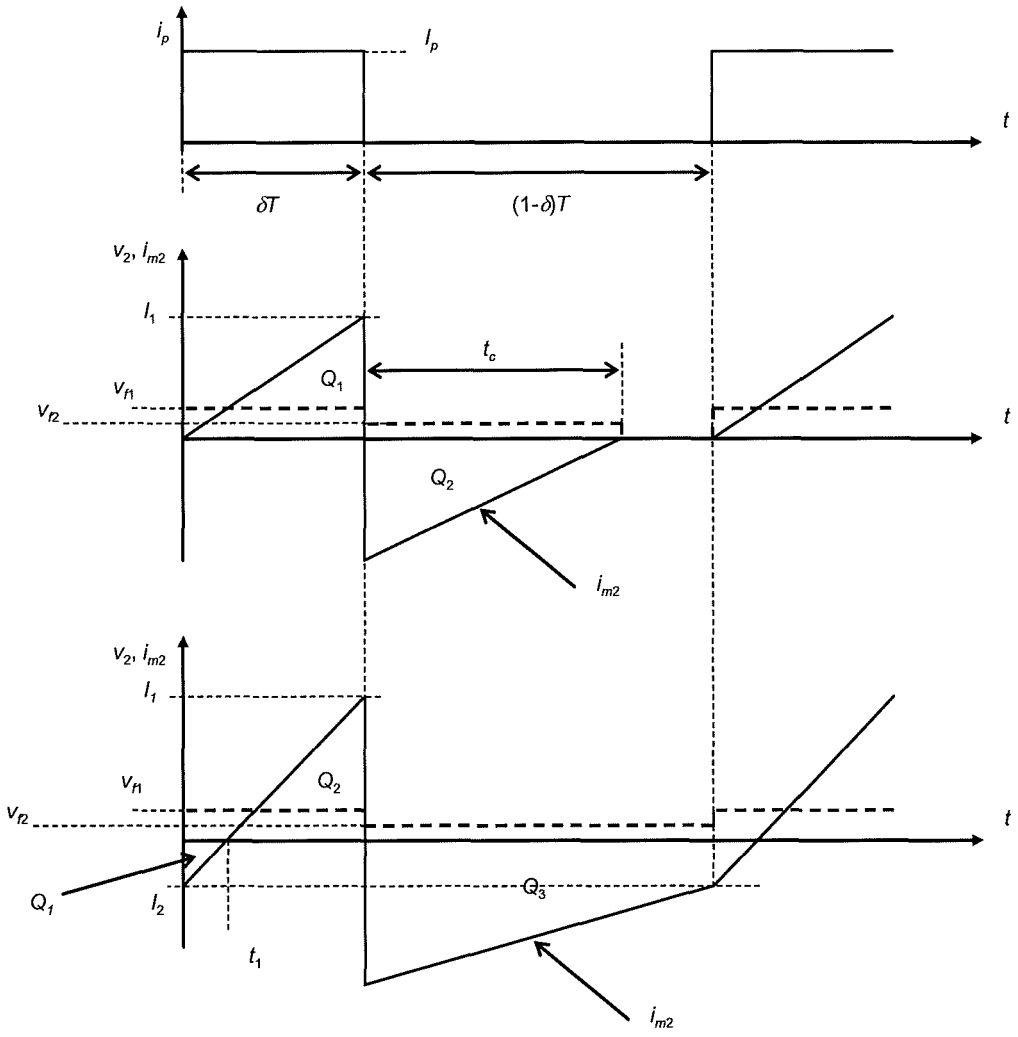


Figure 3.2. Waveforms from Circuit in Figure 3.1 with Oscillatory Period Omitted for Simplicity

For the discontinuous operating mode, I_1 is given by:

$$I_1 = \frac{V_{f1}\delta T}{L_{m2}} \tag{3.1}$$

For the continuous operating mode, I_1 and I_2 may be found from:

$$I_1 = I_2 + \frac{V_{f1}\delta T}{L_{m2}} \tag{3.2}$$

and:

$$I_2 = -I_1 + \frac{V_{f2}(1-\delta)T}{L_{m2}} \tag{3.3}$$

provided that T_r is small compared to T.

V_{f1} and V_{f2} may be expressed as a ratio of each other:

$$k_v = \frac{V_{f1}}{V_{f2}} \tag{3.4}$$

Combining Equations (3.2) and (3.3) and expressing V_{f2} as the ratio of V_{f1} given in Equation (3.4) yields:

$$I_1 = \frac{V_{f1}T}{2L_{m2}}\left(\frac{1-\delta}{k_v} + \delta\right) \tag{3.5}$$

and also:

$$I_2 = \frac{V_{f1}T}{2L_{m2}}\left(\frac{1-\delta}{k_v} - \delta\right) \tag{3.6}$$

It is noted that where k_v is equal to one, then I_1 is simply given by:

$$I_1 = \frac{V_{f1}T}{2L_{m2}} \tag{3.7}$$

For operation at the boundary between a continuous and a discontinuous magnetizing current (where $I_2 = 0$) then:

$$\delta = \delta_{TH} = \frac{1}{k_v + 1} \tag{3.8}$$

where δ_{TH} is the threshold duty factor. Combining Equations (3.1) and (3.7) and taking k_v as 1, Figure 3.3 shows the peak value of i_{m2} reached during a switching cycle plotted against duty factor. Also shown is the peak core flux excursion (φ_{pk}) which is proportional to this current.

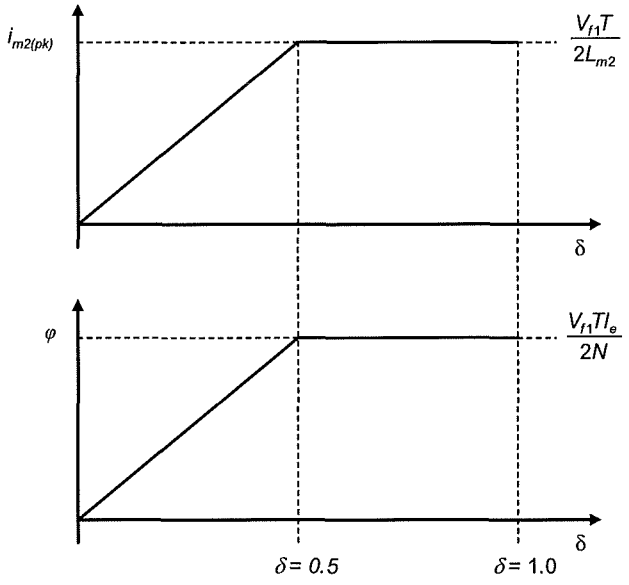


Figure 3.3. Peak Magnetizing Current and Core Flux Excursion Plotted against Duty Factor for $k_v = 1$

3.3 Effect of Net Magnetizing Current on Average Current Droop

3.3.1 Average Current Droop with Discontinuous Magnetizing Current and Lossless Core Material

The net i_{m2} drawn from the CT's output current and averaged over one switching cycle is calculated by summing the enclosed areas shown in Figure 3.2 and dividing by T, the waveform's period:

$$I_{m2(ave)} = \frac{Q_1 - Q_2}{T} \tag{3.9}$$

It is noted that as i_{m2} during the interval from δT to t_c is negative then Q_2 also becomes negative, thereby reducing $I_{m2(ave)}$. Q_1 is given by:

$$Q_1 = \frac{\delta^2 T^2 V_{f1}}{2L_{m2}} \tag{3.10}$$

Q_2 is given by:

$$Q_2 = \frac{I_1 t_c}{2} \tag{3.11}$$

where t_c is given by:

$$t_c = \frac{I_1 L_{m2}}{V_{f2}} \tag{3.12}$$

Putting Equation (3.12) into (3.11) and putting in the value for I_1 from Equation (3.1) into the result yields:

$$Q_2 = \frac{k_v V_{f1} \delta^2 T^2}{2L_{m2}} \tag{3.13}$$

Putting Equations (3.12) and (3.13) into (3.9) gives:

$$I_{m2(ave)} = \frac{\delta^2 T V_{f1}}{2L_{m2}}(1 - k_v) \tag{3.14}$$

It can be seen from Equation (3.14) that if k_v equals one then no droop results and if k_v exceeds one then negative droop may result. That is, the current-time product (charge)

returned into node at the operational amplifier's inverting input terminal may exceed the current-time product lost during the current pulse under measurement.

3.3.2 Average Current Droop with Continuous Magnetizing Current and Lossless Core Material

Again, i_{m2} averaged over one switching cycle is calculated by summing the applicable enclosed areas shown in Figure 3.2 and dividing by the waveform's period:

$$I_{m2(ave)} = \frac{-Q_1 + Q_2 - Q_3}{T} \tag{3.15}$$

Q_1 is given by the area under the triangle:

$$Q_1 = \frac{1}{2} | I_2 | t_1 \tag{3.16}$$

where $|I_2|$ is the magnitude of I_2, given by:

$$| I_2 | = \frac{V_{f1} T}{2 L_{m2}} \left(\frac{\delta - 1}{k_v} + \delta \right) \tag{3.17}$$

and where the interval t_1 is given by:

$$t_1 = \frac{| I_2 | L_{m2}}{V_{f1}} \tag{3.18}$$

Putting Equation (3.18) and then Equation (3.17) into Equation (3.16) gives:

$$Q_1 = \frac{V_{f1} T^2}{8 L_{m2}} \left(\frac{\delta - 1}{k_v} + \delta \right)^2 \tag{3.19}$$

Q_2 is given by the area under the triangle:

$$Q_2 = \frac{1}{2} I_1 (\delta T - t_1) \tag{3.20}$$

Putting Equation (3.5) and then (3.18) into Equation (3.20) gives:

$$Q_2 = \frac{V_{f1} T^2}{8 L_{m2}} \left(\frac{1-\delta}{k_v} + \delta \right)^2 \tag{3.21}$$

Q_3 is given by:

$$Q_3 = (1 - \delta) T \left(\frac{I_1 + |I_2|}{2} \right) \tag{3.22}$$

Putting Equations (3.5) and (3.6) into Equation (3.22) gives:

$$Q_3 = \frac{V_{f1} T^2}{2 L_{m2}} (\delta - \delta^2) \tag{3.23}$$

Finally, Equations (3.19), (3.21) and (3.23) are put back into Equation (3.15) to yield $I_{m2(ave)}$:

$$I_{m2\,(ave)} = \frac{V_{f1} T}{2 L_{m2}} \left[(\delta - \delta^2) \left(\frac{1}{k_v} - 1 \right) \right] \tag{3.24}$$

Figure 3.4 shows the normalized average magnetizing current drawn against duty factor for k_v = 1.1 and 1.2. It is noted that this is always negative. Equation (3.14) is used to calculate $I_{m2(ave)}$ for the DMCM mode and Equation (3.24) is used to calculate $I_{m2(ave)}$ for the CMCM mode.

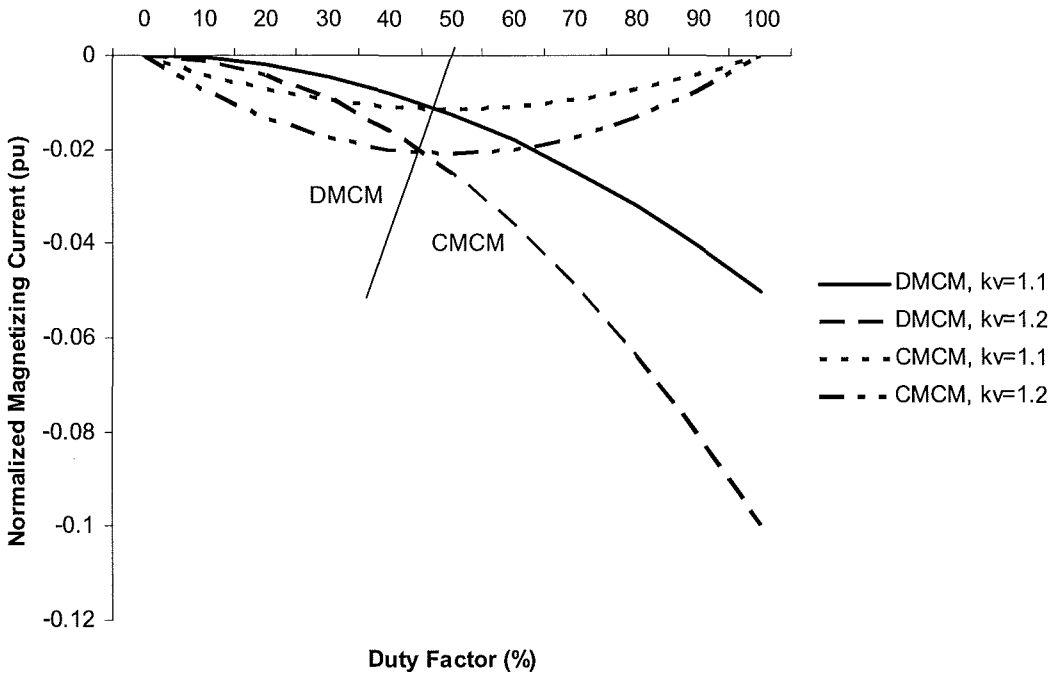


Figure 3.4. Normalized Average Magnetizing Current against Duty Factor for $k_v = 1.1$ and 1.2

The threshold duty factor, δ_{TH}, given by Equation (3.8), where the change from discontinuous to continuous modes takes place, is marked on Figure 3.4.

3.4 Operation in Discontinuous Secondary Current Mode with Lossless CT Core Material

As the value of the current is progressively reduced or the pulse length is increased, a point is reached where the current under measurement is entirely diverted into the CT's magnetizing branch before the end of the pulse. The CT's secondary current now becomes discontinuous, that is, the DSCM mode is entered and the peak current droop is 100 %. This mode of operation is illustrated in Figure 3.5 and occurs at a duty factor (δ_1) given by:

$$\delta_1 = \frac{I_p L_{m2}}{n V_f T} \tag{3.25}$$

The difference between V_{f1} and V_{f2} is neglected here as the effect on droop due to entering the DSCM mode is taken as being dominant. Therefore, $V_f = V_{f1} = V_{f2}$. Above δ_1 the measured current does not change because no information is available from the CT as its core flux is no longer changing. The average current droop for duty factors above δ_1 is given by:

$$D_{(ave)} = \left. \frac{\delta - \delta_1}{\delta} \right|_{\delta > \delta_1} \tag{3.26}$$

To avoid DSCM operation, L_{m2} has to be sufficiently large such that δ_1 is larger than the worst-case duty factor encountered for a given current being sensed.

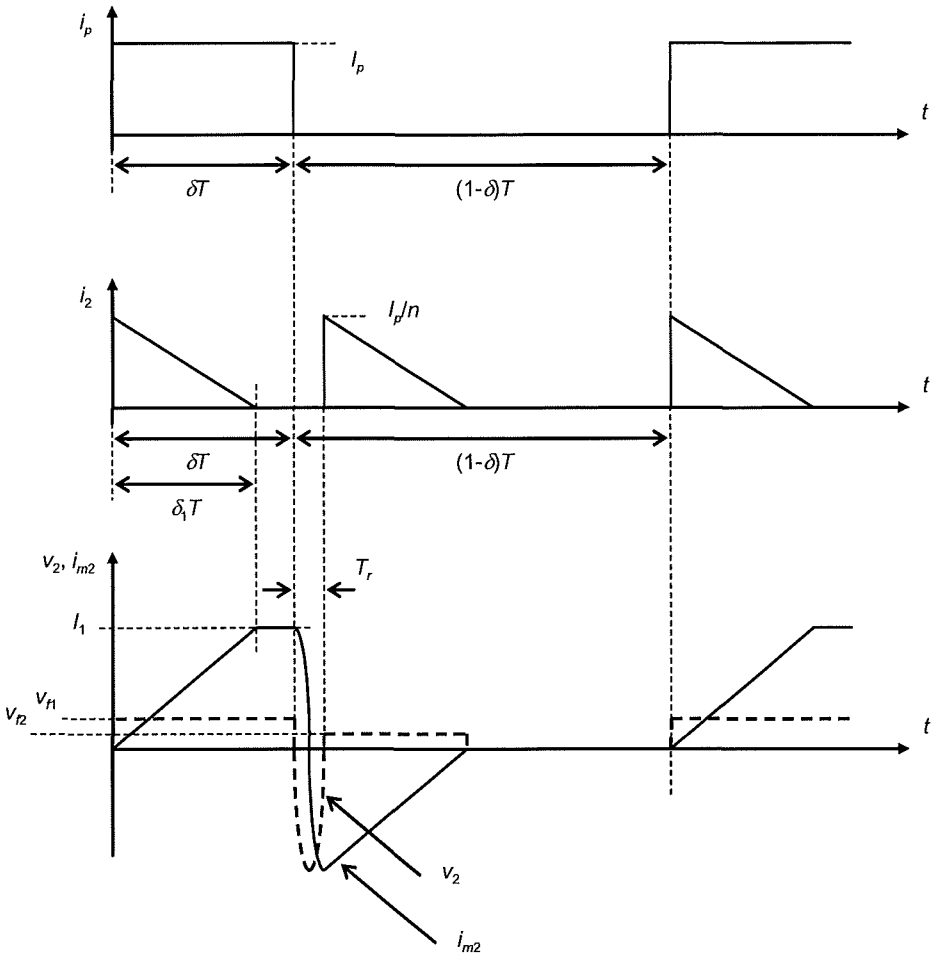


Figure 3.5. CT Waveforms in Discontinuous Secondary Current Mode

However, the average droop given by Equation (3.26) is only appropriate up to the point where the current pulse is re-applied after the resonant magnetizing current from the previous pulse has reached zero. This mode of operation is shown in Figure 3.6. The duty factor (δ_2) at which this occurs is given by:

$$(1-\delta_2)T = \frac{I_p L_{m2}}{nV_f} \tag{3.27}$$

provided that T_r is small compared to the switching period (T). Equation (3.27) may be rearranged to give:

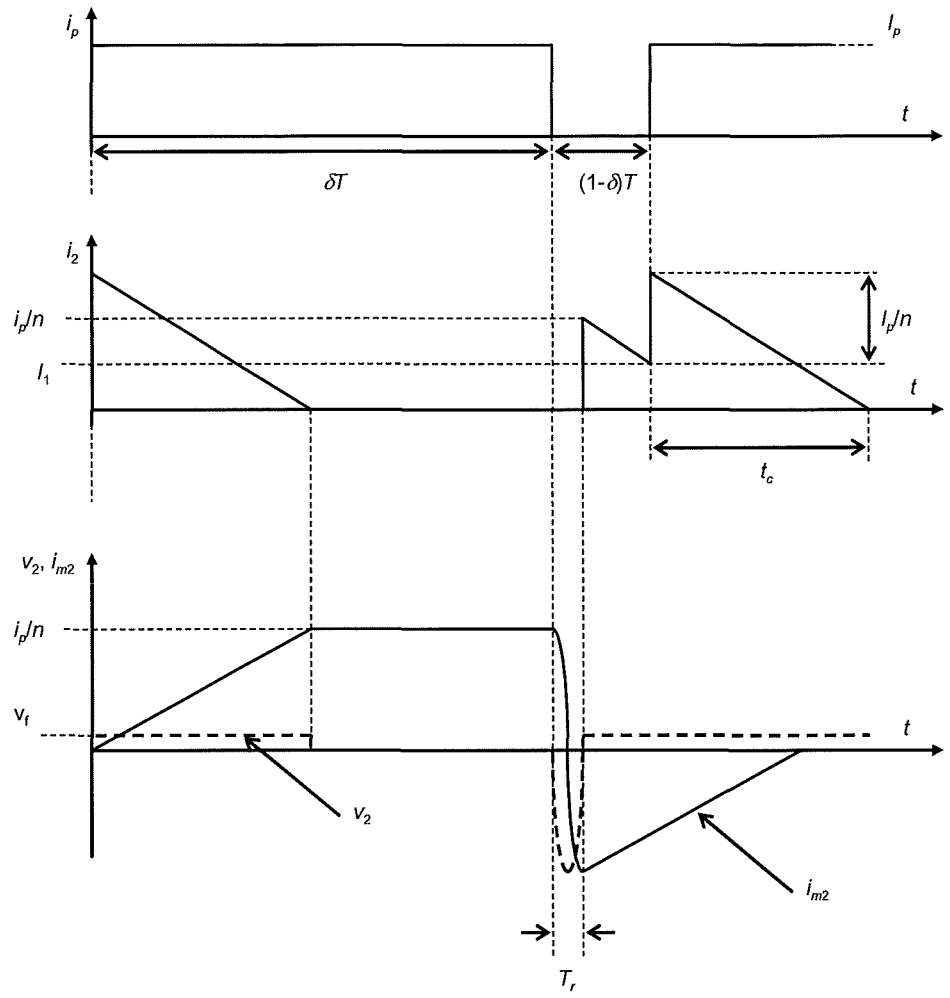


Figure 3.6. DSCM Operation with Current Pulse Re-applied before Decaying Magnetizing Current from Previous Pulse has Reached Zero

$$\delta_2 = 1 - \frac{I_p L_{m2}}{n V_f T} \tag{3.28}$$

This can be expressed in terms of δ_1:

$$\delta_2 = 1 - \delta_1 \tag{3.29}$$

The droop in this region is calculated by equating ampere-time products as follows:

The ideal output is given by:

$$Q_i = \delta T\left(\frac{I_p}{n}\right) \tag{3.30}$$

The actual output is given by adding the trapezium and triangle in Figure 3.6:

$$Q_{actual} = \frac{1}{2}(1-\delta)T\left(\frac{I_p}{n}+I_1\right)+\frac{1}{2}t_c\left(\frac{I_p}{n}+I_1\right) \tag{3.31}$$

This simplifies to:

$$Q_{actual} = \frac{1}{2}\left(\frac{I_p}{n}+I_1\right)[(1-\delta)T+t_c] \tag{3.32}$$

I_1 and t_c are given by:

$$I_1 = \frac{I_p}{n}-\frac{V_f(1-\delta)T}{L_{m2}} \tag{3.33}$$

and:

$$t_c = \left(I_1+\frac{I_p}{n}\right)\frac{L_{m2}}{V_f} \tag{3.34}$$

Combining Equations (3.33) and (3.34) and putting the result into Equation (3.32) gives:

$$Q_{actual} = \frac{2{I_p}^2 L_{m2}}{n^2 V_f}-\frac{I_p}{n}(1-\delta)T \tag{3.35}$$

The average current droop, D_{ave}, is given by:

$$D_{ave} = \frac{Q_i - Q_{actual}}{Q_i} \tag{3.36}$$

Putting Equations (3.30) and (3.35) into Equation (3.36) and rearranging it gives:

$$D_{ave} = \frac{1}{\delta} - \frac{2I_p L_{m2}}{T\delta \times nV_f} \tag{3.37}$$

This can also be expressed in terms of δ_1:

$$D_{ave} = \frac{1}{\delta} - \frac{2\delta_1}{\delta} \tag{3.38}$$

Figure 3.7 shows D_{ave} calculated against duty factor for DSCM operation for different primary currents and hence, from Equations (3.36) and (3.38), different values of δ_1. All quantities are normalized to one.

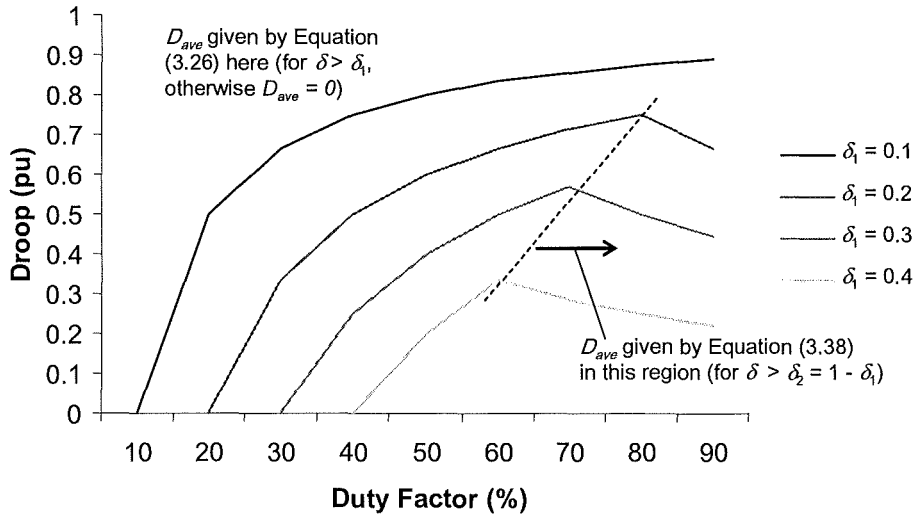


Figure 3.7. Average Current Droop against Duty Factor in Discontinuous Secondary Current Mode

Although, as shown in Figure 3.8, increasing μ_r, and hence L_{m2}, avoids the secondary current becoming discontinuous, a drawback is that the maximum allowable duty factor is reduced as the reset period required is increased. Combining Equations (2.28) and (3.25), the boundary condition beyond which distortion due to either the maximum duty factor limitation or DSCM operation is unavoidable for a given core shape is given by the relationship:

$$I_p = f\pi^2 n^2 V_f C_{eq}\left(\frac{\delta}{(1-\delta)^2}\right) \tag{3.39}$$

C_{eq} is taken as being a function of the core's shape and the secondary winding turns number and configuration. In this section droop attributable to k_v not being equal to one and to core losses has been neglected, as, for most duty factors, the effect of a discontinuous secondary current is dominant.

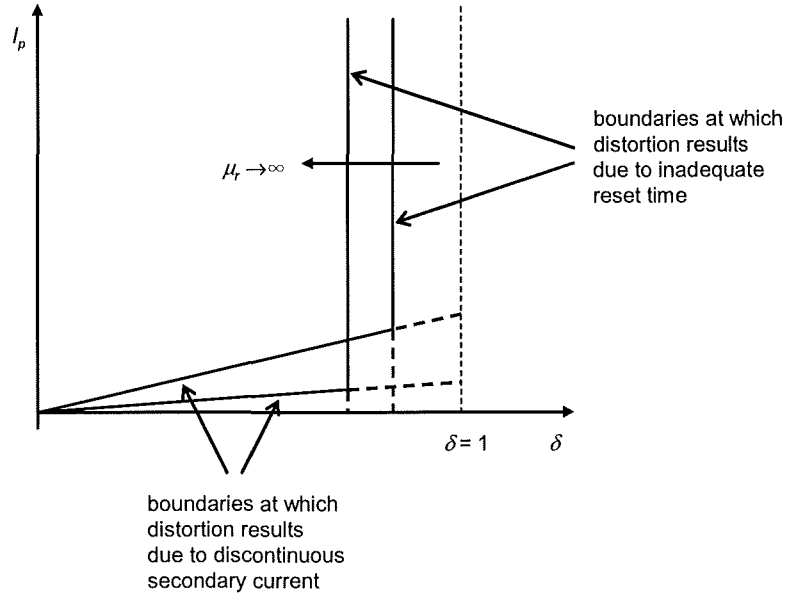
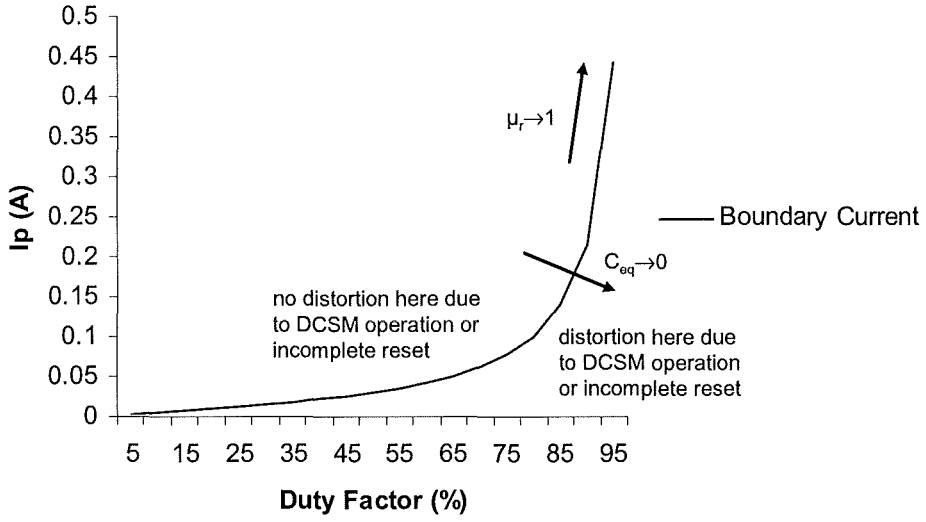


Figure 3.8. Boundaries at which Distortion Results from Insufficient Reset Time and Onset of Discontinuous Secondary Current for Varying CT Core Material Permeability

Using Equation (3.39), Figure 3.9 shows the boundary condition where distortion attributable to either DSCM operation or incomplete reset results for a CT circuit with the notional parameters C_{eq} = 20 pF, n = 120, V_f = 0.8 V operating at 20 kHz.



3.9. Boundary Condition at which Distortion Attributable to either Onset of DSCM Operation or Incomplete Reset Results for a CT Circuit with Notional Parameters

3.5 Effect of Core Losses in the CT on Average Current Droop

In Sections 3.2 to 3.4, losses in the CT have not been accounted for. Three approaches may be taken in anticipating D_{ave}. Firstly, the theory in Section 3.3 may be applied where droop is calculated in terms of k_v and δ and losses are assumed to be negligible. Secondly, the droop attributable to variations in k_v and δ may be neglected and the droop resulting from core losses may be taken as dominant. Thirdly, both the above factors may be combined. The second approach is taken here.

The Steinmetz equation takes account of the hysteresis and eddy current losses in a magnetic material separately:

$$P_v = C_h f B_{ac}^{\ a} + C_e f^2 B_{ac}^{\ 2} \tag{3.40}$$

where B_{ac} is the peak flux density excursion and C_h and C_e are the coefficients of hysteresis loss and eddy current loss respectively. However, information from ferrite core manufacturers is generally expressed in the simplified form [70] in Equation (3.41):

$$P_v = k_1 f^a B_{ac}{}^d \tag{3.41}$$

where k_1, a and d are constants. (The loss may also be estimated by using the manufacturer's graphs of loss per unit volume for various combinations of B_{ac} and f, for example, in [71]. However, these graphs do not give detailed data for the combination of B_{ac} and f used here.) The core's power loss (W_{core}) is:

$$W_{core} = P_v V_e \tag{3.42}$$

where V_e is the core's effective volume. Therefore:

$$W_{core} = V_e k_1 f^a B_{ac}{}^d \tag{3.43}$$

At a given frequency, the core loss may be expressed as:

$$W_{core} = k_2 B_{ac}{}^d \tag{3.44}$$

if $V_e k_1 f^a$ are expressed as the constant, k_2.

Up to δ_{TH}, B_{ac} is directly proportional to δ. Therefore, for $\delta \leq \delta_{TH}$, Equation (3.44) may be written as:

$$W_{core} = k_3 \delta^d \tag{3.45}$$

and above δ_{TH} the core losses remain fixed at this level.

The power output from the CT is $W = V_f \times i_{2(ave)}$ where $i_{2(ave)}$ is the CT's average secondary terminal current. Therefore, for $k_v \approx 1$, the core loss is directly manifested as a shortfall in the average sensed current.

The factor 'd' here is approximated as "2" here. However, it is noted that the flux excursion has a considerable harmonic content and a more complete method of assessing losses is given in [72].

3.6 Experimentation

3.6.1 Experimental Arrangements

The theory presented in Section 3.5 was evaluated using a boost converter circuit and CT with diode rectification and an active load as shown in Figure 3.10. For experimental purposes this has the advantage that, unlike the buck converter, the choke current may be set by the power supply operating in constant output current mode and does not change with duty factor. In a buck converter, a feedback loop would be required to adjust the output voltage from the power supply to maintain a constant choke current. A low-pass filter formed by *R1* and *C1* was used at the emitter of TR2 to allow $v_{out(ave)}$ to be observed. Two CT cores were used in the test circuit. Both were in the TN9/6/3 shape manufactured by Ferroxcube. One was in the 3F3 material grade and the other was in the 3E25 grade.

The average output voltage ideally expected is given by:

$$v_{out(ave)} = \frac{\delta \times i_{L1(ave)} R_F}{n} \tag{3.46}$$

provided that i_{L1} is continuous.

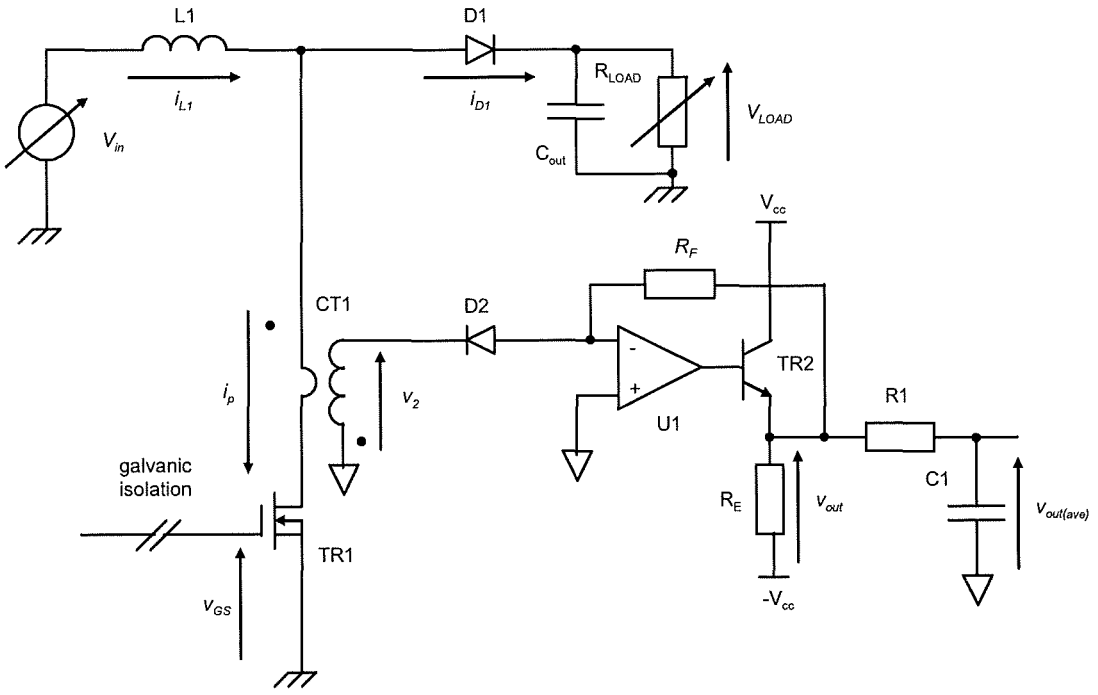


Figure 3.10. Converter Circuit Used for Experimentation with Diode Rectification

An IRF1010E MOSFET was used in location TR1 and a 43CTQ100 Schottky diode was used in location D1. Using a MOSFET avoids the effects of "tail" currents at turn-off which are exhibited by some other power semiconductor devices, for example, the IGBT. A Schottky diode was used to avoid the effects of diode reverse recovery current which would be present if a *p-n* junction diode were to be used. This current would be expected to cause some error, particularly at high frequencies. However, some transient reverse current flow is still expected due to junction capacitances. D2 is a 1N4148 *p-n* signal diode. A Schottky diode may be preferred here due to the lower forward voltage exhibited. However, a *p-n* diode was used as the higher forward voltage drop is useful in accentuating droop for experimental purposes. An LEM LA 100-P Hall-effect sensor was used to calibrate the average choke current ($i_{L1(ave)}$).

The principal data from the circuit in Figure 3.10 are listed in Table 3.1.

Operational amplifier feedback resistance (R_F) (Ω)	120
Emitter resistance (R_E) (kΩ)	10
Operational amplifier type	NE5534AP [73]
Rectifier diode (D2)	1N4148
Bipolar npn transistor used in location TR2	ZTX651
Supply rail voltages (V_{cc} and $-V_{cc}$) (V)	± 15
R1 (kΩ)	10
C1 (nF)	3.3

Table 3.1. Experimental Circuit Parameters

The corner frequency of the low-pass filter (*R1* and *C1*) is set at 4.8 kHz. The CTs' data are listed in Table 3.2. The small-signal secondary magnetizing inductances of the CTs (L_{m2}) were measured using a Philips PM 6303 RCL meter at a measurement frequency of 1 kHz. The experimentally derived value of the permeability was calculated from:

$$\mu_r = \frac{L_{m2} l_e}{\mu_0 N_2^{\,2} A_e} \tag{3.47}$$

where l_e and A_e are given as 22.9 mm and 4.44 mm^2 respectively from the manufacturer's data in [71].

As the turns ratio (n) is 120 and the feedback resistance (R_F) is 120 Ω then a gain of 1 V/A is expected. Details of the CTs assembled for testing are listed in Table 3.2.

The resistances of the CTs' secondary windings (R_2) were measured using the four-wire technique with an instrument uncertainty of ±2 %. At the rated primary current of 5 A and given that n = 120 and R_2 = 0.89 Ω in each case, the voltage drop across the secondary winding is calculated at 37 mV. This is small in comparison to the forward voltage drop of approximately 0.8 V across the rectifier diode [74].

The 3F3 and 3E25 material grades are representative of the typical trade-off between permeability and core losses detailed in [71]. In relative terms, the 3F3 grade has a

high Curie temperature and a low permeability whereas, conversely, the 3E25 grade has a low Curie temperature and a high permeability.

Core shape		TN9/6/3
CT primary winding configuration		Single conductor passed through core aperture
CT secondary winding configuration		120 turns of 0.2 mm diameter copper wire wound evenly around core circumference to minimize leakage inductance
CT using 3F3 material	T_C (°C)	200
	Measured value of L_{m2} at approximately 20 °C (mH)	11.0
	μ_r calculated from measured L_{m2}	3134
	Measured value of R_2 at approximately 20 °C (Ω)	0.89
CT using 3E25 material	T_C (°C)	125
	Measured value of L_{m2} at approximately 20°C (mH)	24.7
	μ_r calculated from measured L_{m2}	7038
	Measured value of R_2 at approximately 20 °C (Ω)	0.89

Table 3.2. Parameters of CTs under Test

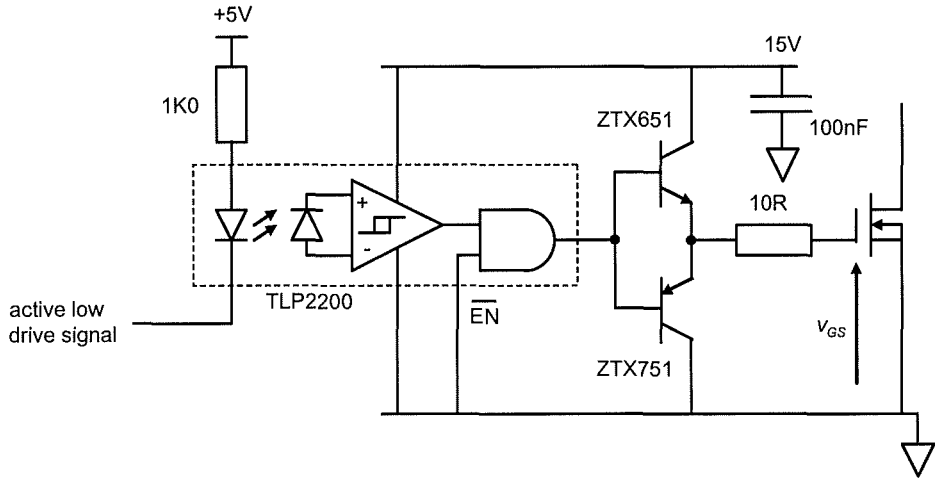


Figure 3.11. Gate Driver Circuit with Optical Isolation

Some practical points are noted. C_{eq} is particularly sensitive to end-winding effects, that is, the proximity of the winding tails. The position of the tails is therefore disturbed as little as possible during experimentation to ensure repeatability. The oscilloscope probe used to observe v_2 was left permanently in place during all measurements to avoid changes to C_{eq} attributable to the probe's capacitance. The CTs evaluated here are not varnish-impregnated, as is normally the case for production purposes. The presence of varnish increases the stray capacitance associated with the CT as the permittivity of varnish is invariably significantly greater than that of air. The winding had multiple layers and no attempt was made to keep the ends physically distanced. This arrangement leads to a relatively high capacitance.

The switching frequency was set at 20 kHz. Although higher frequencies are generally used for switched mode power conversion, 20 kHz was selected as, for the particular CTs used here, this allows operation at a high duty factor (approximately 95 %) prior to incomplete reset resulting. Also, operational amplifier parameters such as slew rate and frequency response assume less importance.

In addition to the dc component, the current waveform conducted by the CT has ac components present at integer multiples of 20 kHz. However, the skin effect is treated as negligible here. This is justified as follows. The skin depth (d_s) is given by:

$$d_s = \sqrt{\frac{\rho}{\pi \times f \mu_0}} \tag{3.48}$$

where ρ is the resistivity of the conductor material, in this case copper. Equation (3.48) rearranges to give:

$$f = \frac{\rho}{\pi \times \mu_0 d_s^{\,2}} \tag{3.49}$$

Taking the resistivity of copper as 17.1×10^{-9} Ωm at 20 °C and d_s as 0.1 mm, that is, the same as the radius of the conductor, then f is calculated as 433 kHz. The skin

effect is therefore not expected to be significant as the fundamental frequency here is 20 kHz.

During experimentation the value of i_{m2} and the consequent state of the core flux is inferred from either the missing sensed load current or the time integral of the voltage at the terminals (according to Faraday's Law).

A photograph of the test circuit is shown in Figure 3.12.

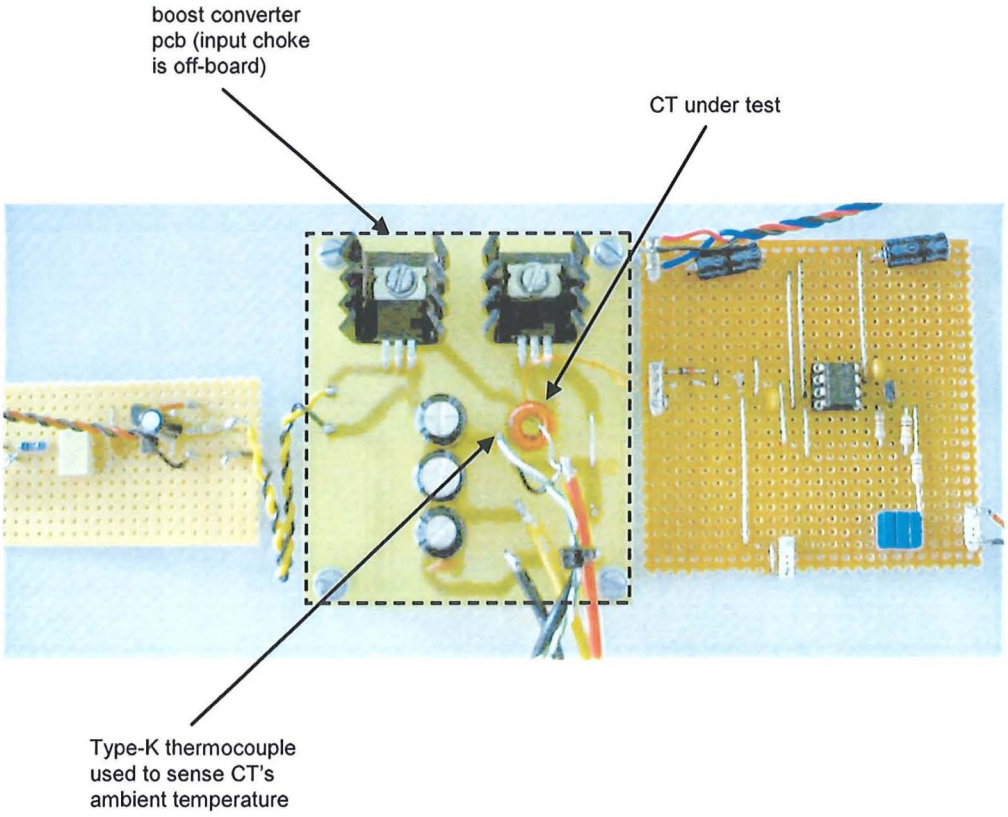


Figure 3.12. Photograph of Test Circuit

3.6.2 Experimental Results

Figures 3.13, 3.14 and 3.15 show exemplifying waveforms from the circuit in Figures 3.10 and 3.12 when it is operating in the CMCM mode. The average value of i_{L1} is set at 5 A and δ is set at 33 %.

The values of $L1$, V_{in} and V_{out} are selected here such that they allow a visible rate of current change during the period of the switching waveform.

In Figure 3.13, the MOSFET's drive signal (v_{GS}) is shown for reference purposes. Also shown are CT's secondary terminal voltage (v_2), the choke current (i_{L1}) which is sensed using a high-bandwidth (50 MHz) dc current probe, and the instantaneous output voltage at the emitter of TR2 (v_{out}).

Figure 3.14 shows v_2 in greater detail. It can be seen that v_2 adopts two different voltage levels, V_{f1} during T_{on} and V_{f2} during T_{off}. The end of conduction, where v_{out} reaches zero, is also characterized by an oscillation in v_2 having a peak amplitude approximately equal to that of the rectifier diode's forward voltage drop. The oscillation is at the same frequency seen during the period T_r as L_{m2} again resonates with C_{eq}. This frequency is measured at approximately 300 kHz. As expected, the duration of t_c exceeds that of T_{on} as k_v is greater than 1.

Figure 3.15 shows i_{L1} and v_{out} in greater detail. v_{out} is characterized by several phases. During T_{on}, it is essentially proportional to i_p, less a component attributable to droop. At $t = T_{on}$, it drops to zero for the interval T_r when i_{m2} reverses direction due to the resonant action of L_{m2} and C_{eq}. It then rises as i_{m2} decays through D2, and then reaches zero when i_{m2} has commutated.

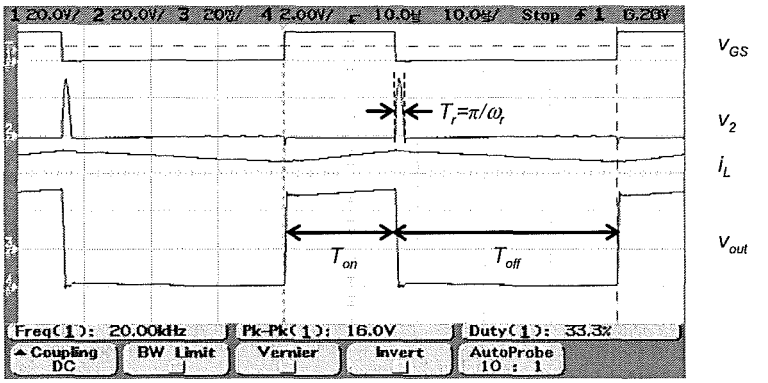


Figure 3.13. Waveforms in Discontinuous Magnetizing Current Mode (v_{GS} = 20 V/div, v_2 = 20 V/div, i_{L1} = 2 A/div, v_{out} = 2 V/div, Time Scale: 10 µs/div)

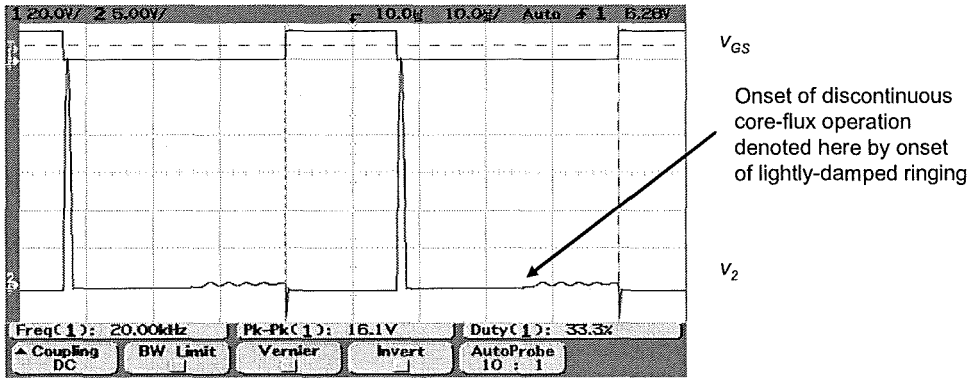


Figure 3.14. Waveform v_2 in Discontinuous Magnetizing Current Mode Shown in Greater Detail (v_{GS} =20 V/div, v_2 =5 V/div, Time Scale: 10 µs/div)

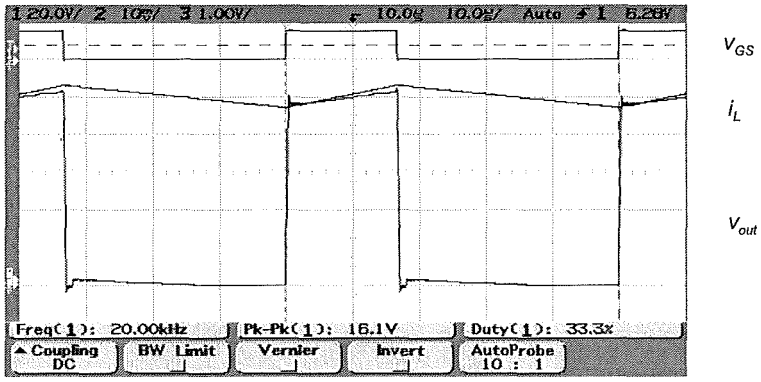


Figure 3.15. Waveforms i_{L1} and v_{out} in Discontinuous Magnetizing Current Mode Shown in Greater Detail (v_{GS} = 20 V/div, i_{L1} = 1 A/div, v_{out} = 1 V/div, Time Scale: 10 µs/div)

Figures 3.16, 3.17 and 3.18 show exemplifying waveforms from the circuit in Figures 3.10 and 3.12 when it is operating in the CMCM mode. Again, the average value of i_{L1} is 5 A and the switching frequency is 20kHz. However, δ is set at 67 % here.

Figure 3.16 shows the MOSFET's gate drive signal (v_{GS}) for reference purposes, the CT's secondary terminal voltage (v_2), the choke current (i_{L1}) and the instantaneous output voltage at the emitter of TR2 (v_{out}).

Figure 3.17 shows v_2 in greater detail and Figure 3.18 shows i_{L1} and v_{out} in greater detail. It can be seen that the effective peak current droop is exacerbated as described in Section 3.2.

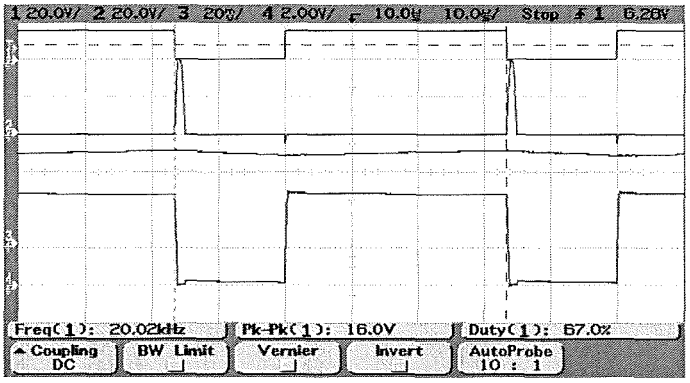


Figure 3.16. Waveforms in Continuous Magnetizing Current Mode (v_{GS} = 20 V/div, v_2 = 20 V/div, i_{L1} = 2 A/div, v_{out} = 2 V/div, Time Scale: 10 µs/div)

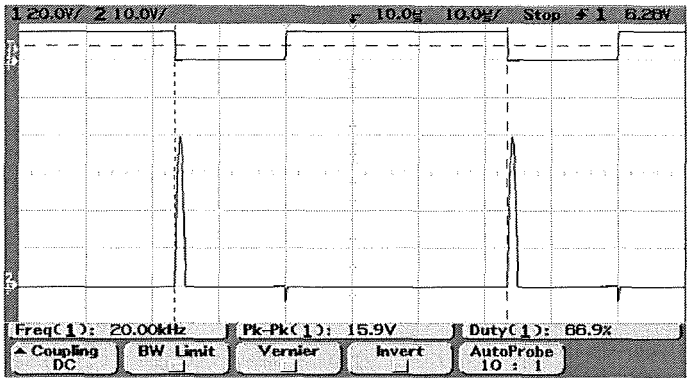


Figure 3.17. Waveform v_2 in Continuous Magnetizing Current Mode Shown in Greater Detail (v_{GS} = 20 V/div, v_2 = 10 V/div, Time Scale: 10 µs/div)

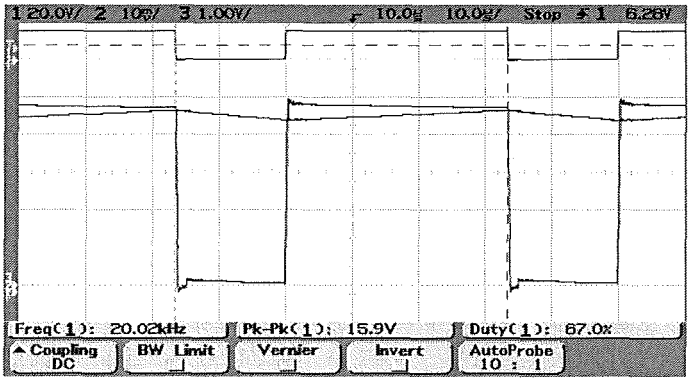


Figure 3.18. Waveforms i_{L1} and v_{out} in Continuous Magnetizing Current Mode Shown in Greater Detail (v_{GS} = 20 V/div, i_{L1} = 1 A/div, v_{out} = 1 V/div, Time Scale: 10 µs/div)

In Figures 3.13 to 3.18 inclusive the permutation of input and output voltages and the choke inductance are set to allow a discernible di/dt over a switching cycle for illustrative purposes. However, for subsequent measurements the choke size is now increased so that less than 5 % current ripple is now present.

Figures 3.19, 3.20 and 3.21 show $v_{out(ave)}$ for average choke currents (i_{L1}) of 5 A, 3 A and 1 A respectively with a TN9/6/3 core shape using 3F3 core material. The output voltage ideally obtained is also plotted on these figures. It can be seen that the per-unit error present increases as the current under measurement is decreased. This is expected as the magnitude of the magnetizing current in a diode-rectified CT upon which error depends is essentially independent of the magnitude of the current being measured.

It can also be seen, particularly from Figure 3.21, that a change in the trajectory in the measured sensed current is evident at the duty factor where the transition from DMCM to CMCM core flux operation occurs (δ_{TH}).

Figures 3.21, 3.22 and 3.23 show $v_{out(ave)}$ for average choke currents (i_{L1}) of 5 A, 3 A and 1 A respectively with TN9/6/3 core shape in 3E25 material.

At 95 % duty factor some distortion is evident as insufficient reset time is available with either core type for the reset half-oscillation to fully elapse.

Because the absolute droop is primarily dependant on the rectifier's forward voltage drop here, the per-unit droop becomes greater at lower currents.

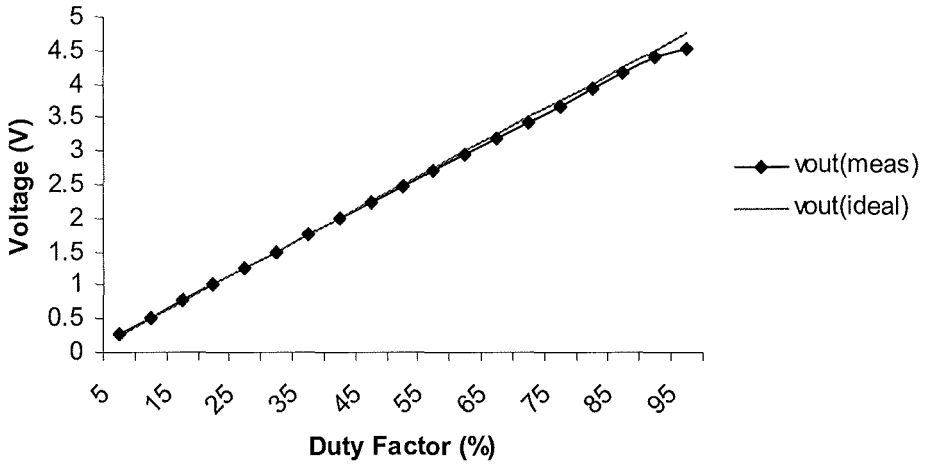


Figure 3.19. Measured and Ideal $v_{out(ave)}$ Plotted against Duty Factor (3F3 Core Material, i_{L1} = 5 A)

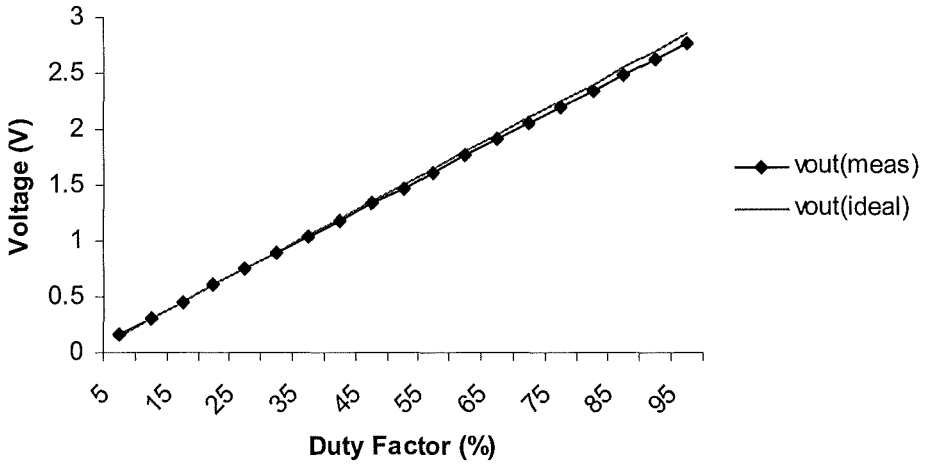


Figure 3.20. Measured and Ideal $v_{out(ave)}$ Plotted against Duty Factor (3F3 Core Material , i_{L1} = 3 A)

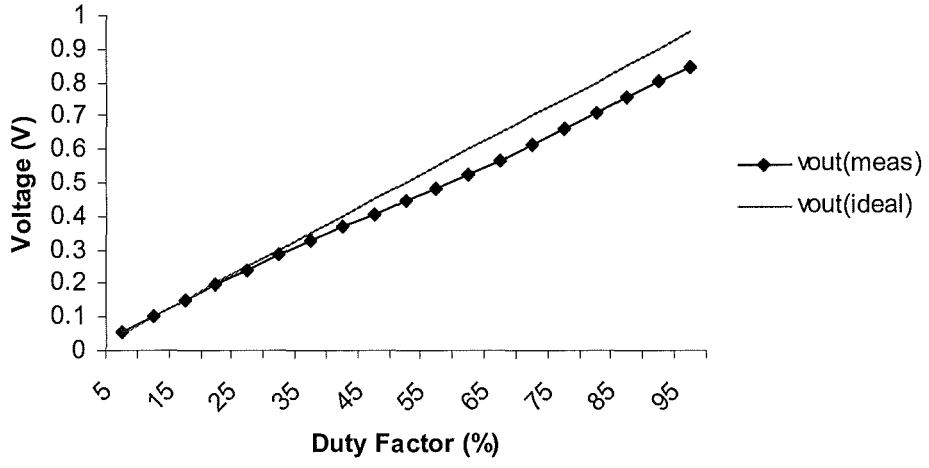


Figure 3.21. Measured and Ideal $v_{out(ave)}$ Plotted against Duty Factor (3F3 Core Material, i_{L1} = 1 A)

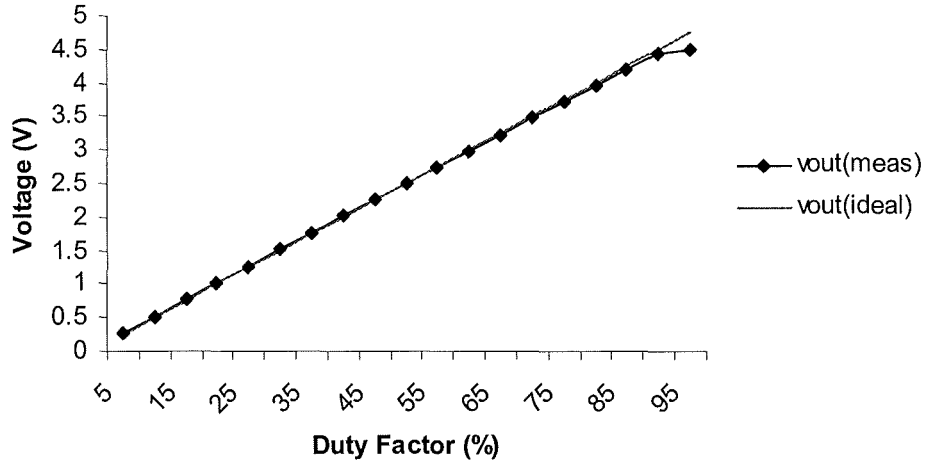


Figure 3.22. Measured and Ideal $v_{out(ave)}$ Plotted against Duty Factor (3E25 Core Material, i_{L1} = 5 A)

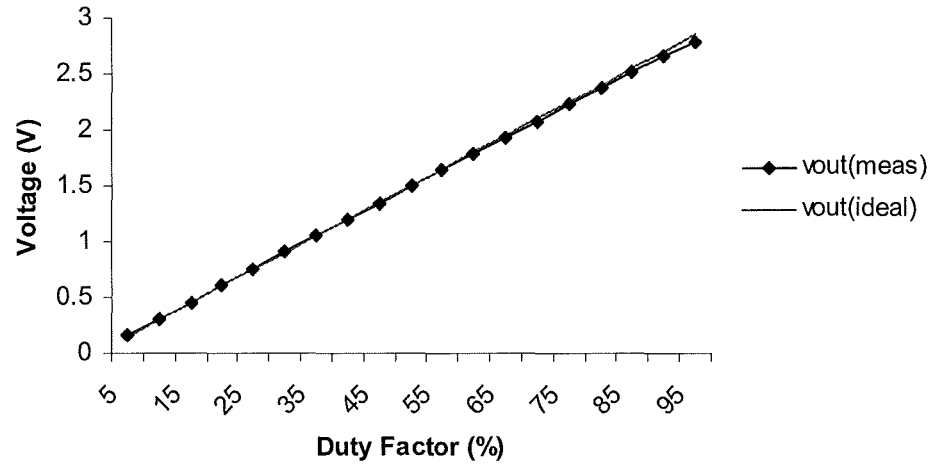


Figure 3.23. Measured and Ideal $v_{out(ave)}$ Plotted against Duty Factor (3E25 Core Material, i_{L1} = 3 A)

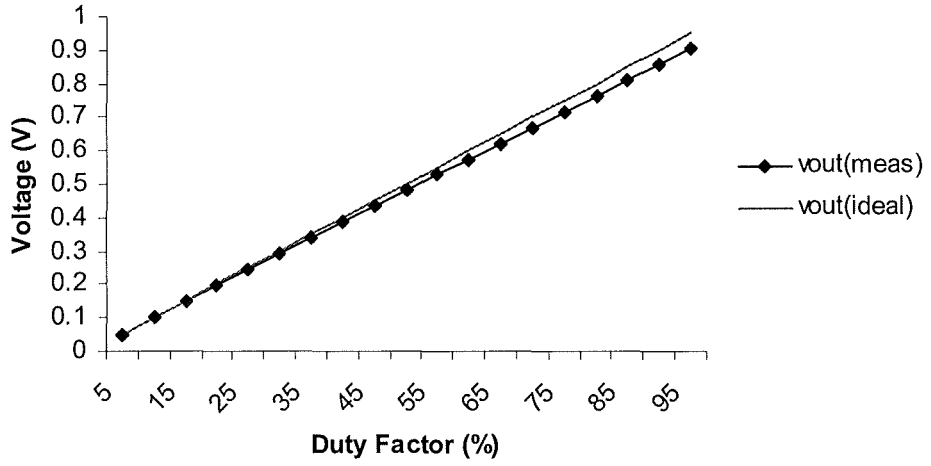


Figure 3.24. Measured and Ideal $v_{out(ave)}$ Plotted against Duty Factor (3E25 Core Material, i_{L1} = 1 A)

Figures 3.25 and 3.26 again show the data from Figures 3.21 and 3.24 respectively, but with the predicted sensed currents for a lossless CT core used without resonant energy recovery added.

The output voltage for this condition is calculated from:

$$v_{out} = v_{out(ideal)}\left(1 - \frac{nV_f\delta}{2f \times L_{m2}I_p}\right) \tag{3.50}$$

V_f is taken as 0.8 V and L_{m2} for the 3F3 and 3E25 materials are the values given in Table 3.2.

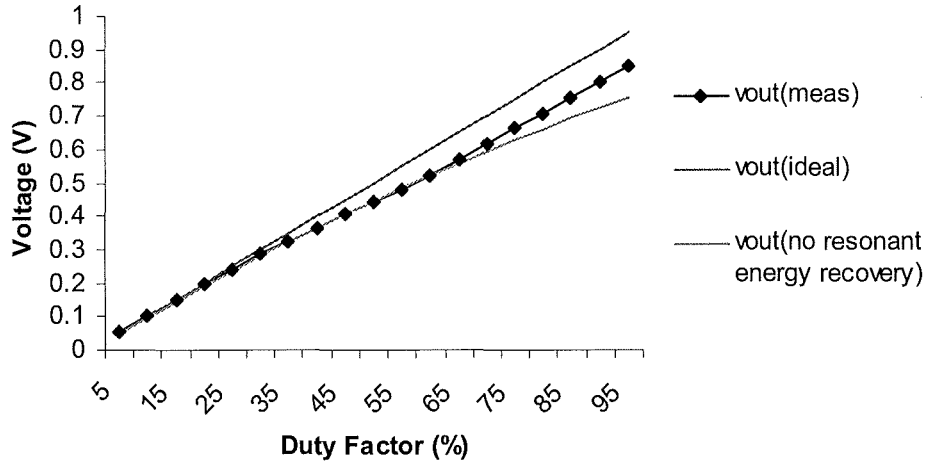


Figure 3.25. Measured and Ideal $v_{out(ave)}$ Plotted against Duty Factor with Predicted Sensed Current without Resonant Operation Superimposed (3F3 Core Material, i_{L1} = 1 A)

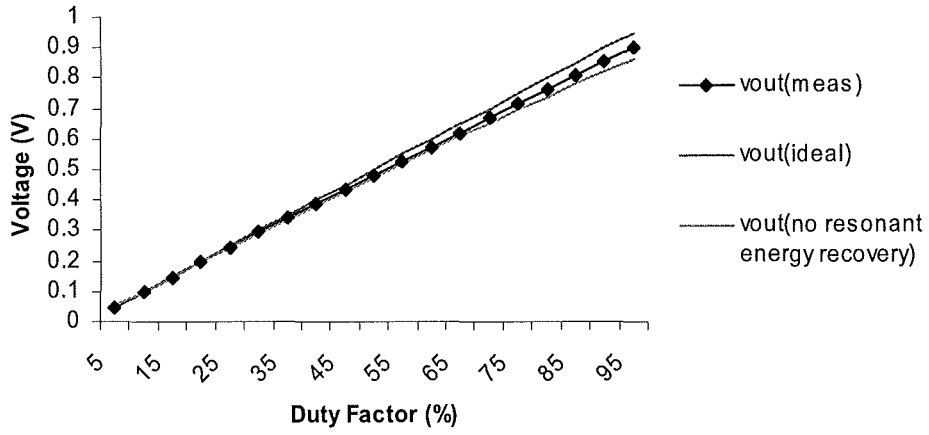


Figure 3.26. Measured and Ideal $v_{out(ave)}$ Plotted against Duty Factor with Predicted Sensed Current without Resonant Operation Superimposed (3E25 Core Material, i_{L1} = 1 A)

Figure 3.27 shows the absolute average voltage droop against duty factor for load currents between 1 and 5 A in 1 A increments. The results in Figure 3.27 and all subsequent results in this chapter are taken with the CT variant in 3F3 core material described in Table 3.2. It can be seen that the value of droop is essentially independent of the magnitude of the sensed current. It is noted that some offset error is expected in these readings as the droop is calculated by subtracting the measured current from the

set current. The current is set using instrumentation with a resolution of 1 % at the lowest current and therefore a consequent (larger) per-unit error may appear in the droop calculated in this way. At 95 % duty factor some of the error readings are shown to deviate as the reset half-oscillation is not completed.

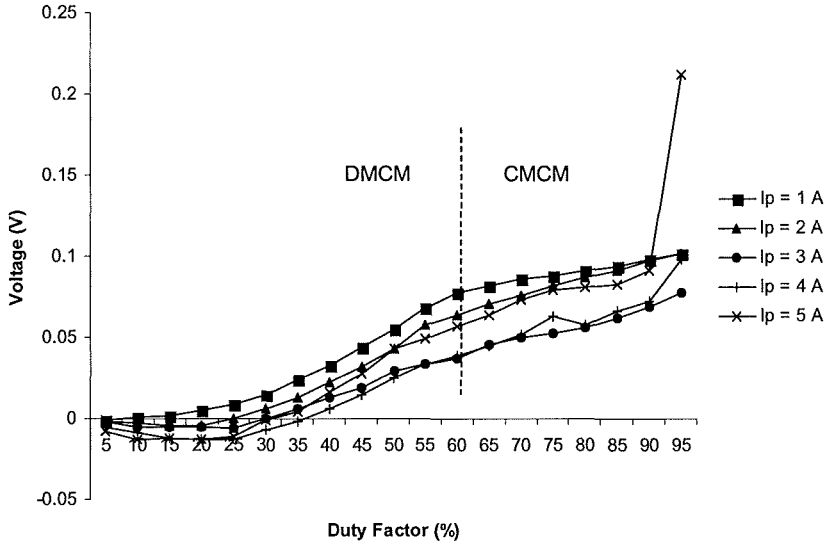


Figure 3.27. Absolute Droop Expressed as Shortfall in $v_{out(ave)}$ against Duty Factor for Currents from 1 to 5 A

As the CT's core losses are proportional to δ^2 below δ_{TH}, then as δ approaches zero the theory in Equation (3.12) is expected to become applicable where the droop becomes negative. This is consistent with the results in Figure 3.27.

3.6.3 Experimental Results at Low Primary Currents

In the diode-rectified CT, the magnetizing current's peak magnitude is essentially independent of the load current magnitude. In order to evaluate the behaviour of the magnetizing current more accurately, the current under measurement is now reduced to accentuate the magnitude of i_{m2} with respect to i_{L1}. Subsequent measurements are

taken at less than 1 A. To enhance the resolution of the sensed current, the value of R_F is changed to 1.2 kΩ to yield an expected output of 10 V/A.

Figure 3.28 shows exemplifying waveforms when operating with 100 % peak current droop. The switching frequency is 20 kHz and i_{L1} is 100 mA. As with the situation where the magnetizing current reaches zero during discontinuous operation, the point at which 100 % peak current droop occurs is marked by the onset of an oscillation in v_2. The height of the voltage triangle immediately after the reset half-resonant period is less than that when the current pulse under measurement is applied. Also, some curvature is seen in the triangles' decaying slopes. Both these observations are attributed to the presence of the CT's core losses.

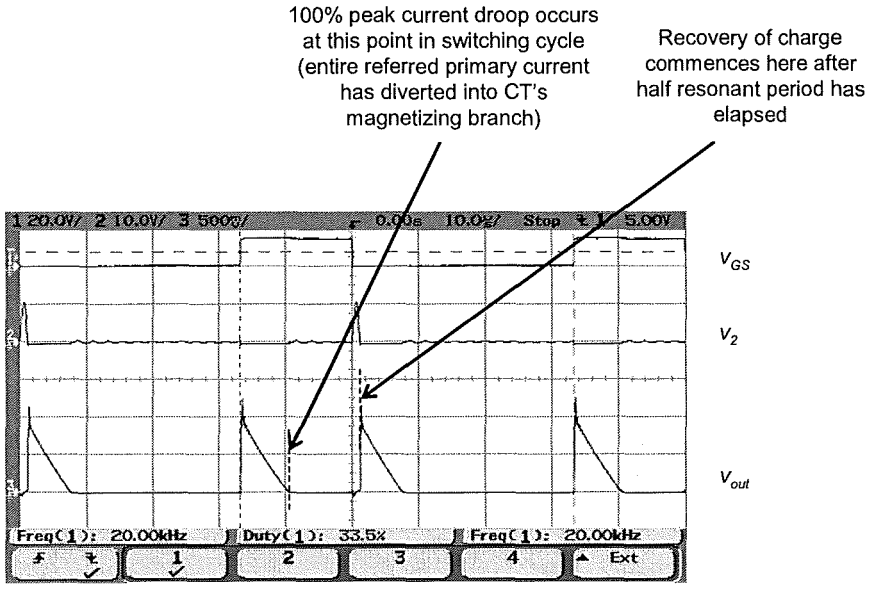


Figure 3.28. Waveforms with Discontinuous Secondary Current (v_{GS} = 20 V/div, v_2 = 5 V/div, v_{out} = 500mV/div, Time Scale: 10 μs/div)

Figure 3.29 shows exemplifying waveforms when operating with 100% peak current droop and with the current pulse re-applied prior to commutation of the magnetizing current.

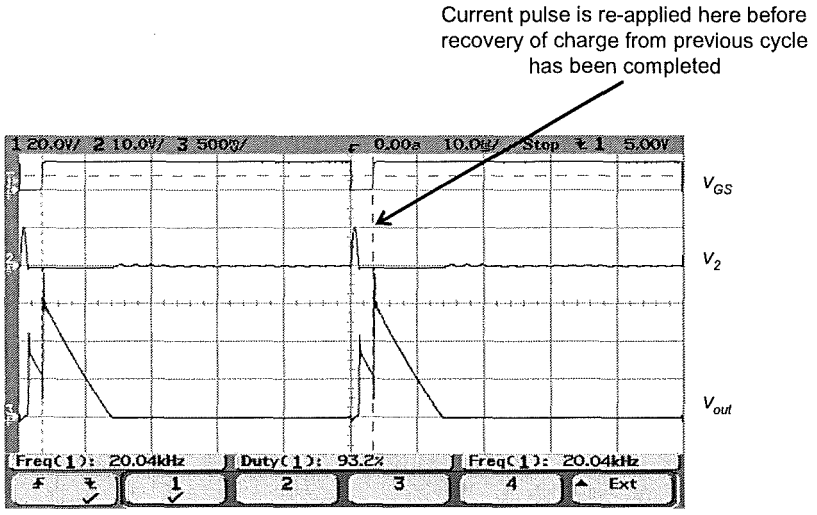


Figure 3.29. Waveforms with Discontinuous Secondary Current and with Current Pulse Re-applied Prior to Commutation of Magnetizing Current (v_{GS} = 20V/div, v_2 = 5 V/div, v_{out} = 500 mV/div, Time Scale: 10 μs/div)

Figure 3.30 shows the measured and ideal v_{out} against δ for primary currents of 100 mA, 300 mA and 500 mA. The current against duty factor boundary at which the peak current droop reaches 100 % is marked. This is calculated with Equation (3.25) and with L_{m2} taken as 11.0 mH. V_{f1} is taken as 0.8 V.

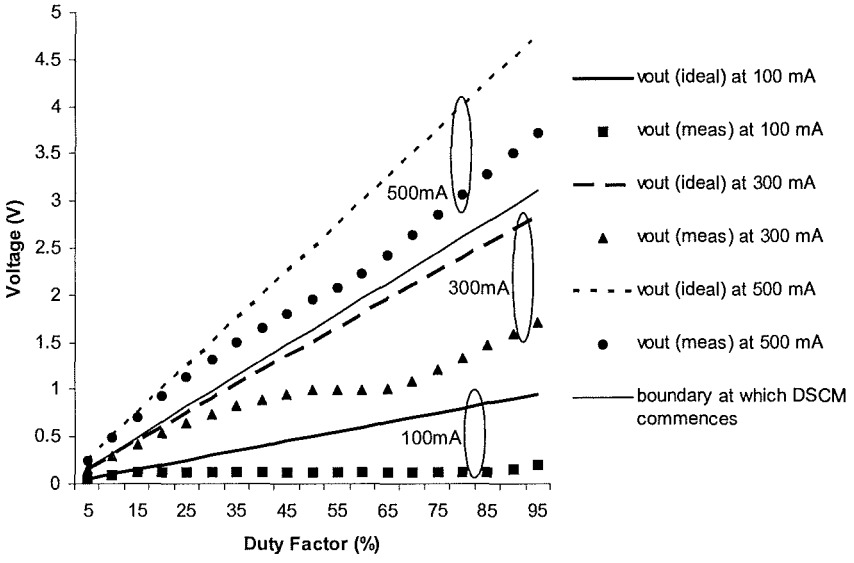


Figure 3.30. Measured and Ideal v_{out} Plotted against Duty Factor (i_{L1} = 100 mA, 300 mA and 500 mA)

In Figure 3.30, it can be seen that the measured currents exhibiting plateaus centred around a duty factor of approximately 50 % lie below this boundary where the ratio of δ to I_p is too high to sustain continuous conduction in the CT's secondary winding.

3.6.4 Comparison of Experimental Results with Theory

Figure 3.31 shows the sensed and ideal currents against duty factor for a primary current of 500 mA. It can be seen that the change from CMCM to DMCM operation occurs at a duty factor of approximately 60 %. Where losses are significant, a higher threshold duty factor than that predicted by Equation (3.8) is applicable. As mentioned in Section 3.5, a shortfall in output current, and hence output voltage, is proportional to the core losses, and hence the peak core flux excursion to the appropriate power. Vout is therefore also proportional to the losses. Therefore, if losses are proportional to B_{ac}^2:

$$k_4 = \frac{v_{out(ideal)} - v_{out(meas)}}{\delta^2} \tag{3.51}$$

where k_4 is determined here from $v_{out(meas)}$ at the threshold duty factor (δ_{TH}). The predicted value of $v_{out(ave)}$ is shown where v_{out} is derived from Equation (3.51) for values of δ below δ_{TH} and the absolute droop above δ_{TH} is held constant at that measured at δ_{TH}.

Using the correction algorithm given, it can nonetheless be seen that an increasing deviation takes place as δ is raised from δ_{TH} towards one. This is attributed to the observation that, as δ rises, the magnitude of the average voltage impressed across L_{m2} increases slightly. That is, whilst the primary winding of the CT is conducting during the period δT, the voltage across L_{m2} is $V_{f2} + I_2R_2$, whereas when the pulse is not present during the period $(1 - \delta)T$, this voltage is V_{f1}.

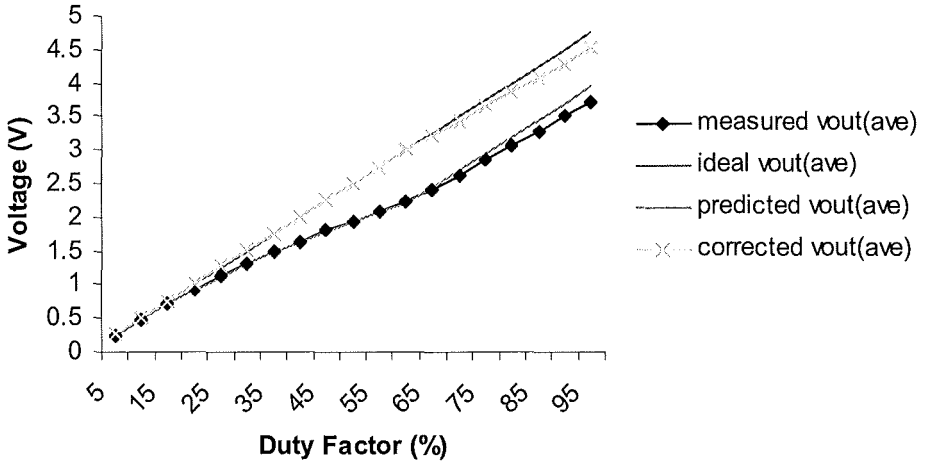


Figure 3.31. Introduction of Piece-Wise Compensation Scheme to CT Output Signal (i_{L1} = 500 mA)

Figure 3.32 shows the error at 5A current from Figure 3.18 with the error after compensation superimposed. The correction coefficient (k_4) is that taken from the measured error at 500 mA. As with the results shown in Figure 3.25, this is to demonstrate that the flux swing and consequent losses are essentially independent of the magnitude of the current being sensed.

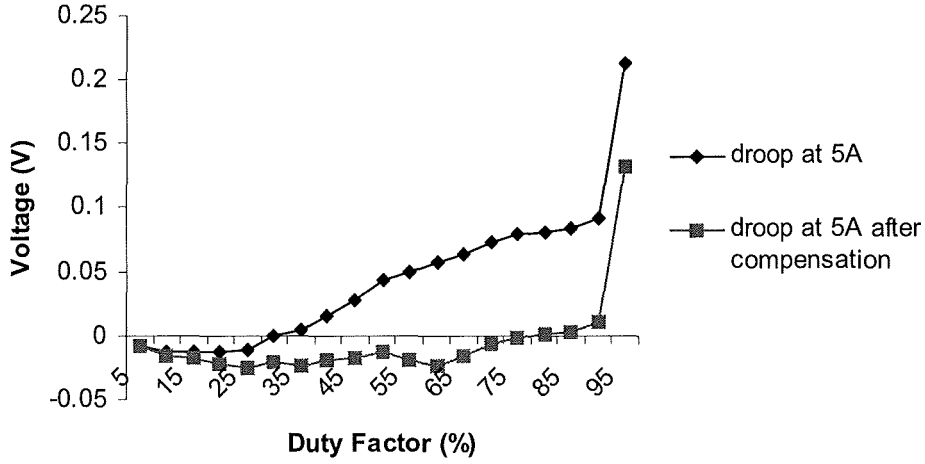


Figure 3.32. Error at 5 A Current Before and After Compensation with Correction Coefficient Derived from Reading at 500 mA

3.6.5 Relation of Average Current Droop to Core Material Loss Data

The CT's core flux density swing is given by:

$$\Delta B = \frac{\delta \times TV_f}{NA_e} \tag{3.52}$$

At a frequency of 20 kHz the waveform's period, T, is 50 μs. Other parameters are: V_f = 0.8 V, N_2 = 120 and A_e = 4.44 mm^2. At the threshold duty factor of approximately 50 % (where the full flux swing is nearly reached, as shown in Figure 3.3) the peak flux excursion, B_{ac}, is calculated from Equation (3.52) at 73 mT.

k_1, a and d are given in [70] as 1.5×10^{-6}, 1.3 and 2.5 respectively where f is entered in kHz and B_{ac} is entered in mT. This gives a specific loss of 3.355 mW/cm^3 here. As the core used has a volume of 0.102 cm^3 then the resultant loss is 0.342 mW. In the data presented in Figure 3.30, the output voltage measured at I_p = 500 mA and δ = 50 % is 1.944 V compared to an ideal of 2.5 V. Given that R_F = 1.2 kΩ, then this represents a shortfall in the measured current of 0.463 mA. As V_f = 0.8V then this represents a power loss of 0.371 mW. There is therefore approximate agreement between the power loss inferred from the shortfall in the sensed current and the calculated core loss.

3.7 An Enhanced Loss Algorithm

Although losses were taken as being fixed above δ_{TH}, it can, however, be seen that a small, approximately linear (ramp-on-a-step) rise is evident.

Where enhanced accuracy is required, a straight-line loss approximation dependent on the duty factor is deemed appropriate above δ_{TH} at the expense of a slightly more complex algorithm. The approximation is justified as follows. With respect to Figure 3.33, the average voltage ($v_{2(ave)}$) impressed across L_{m2} over a switching cycle is given by:

$$v_{2(ave)} = \delta V_{f1} + (1-\delta)V_{f2} \tag{3.53}$$

As $V_{f1} = k_v V_{f2}$ then:

$$v_{2(ave)} = V_{f2}[1 + (k_v - 1)\delta] \tag{3.54}$$

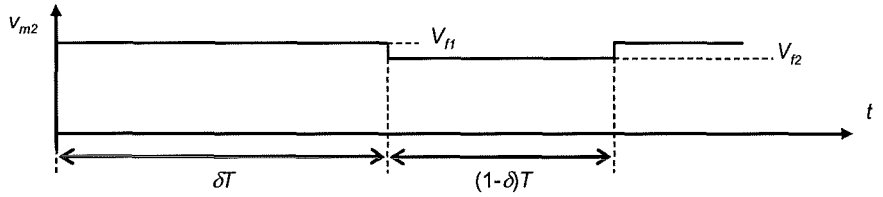


Figure 3.33. Voltage Impressed across CT's Magnetizing Branch over a Switching Cycle for $\delta > \delta_{TH}$ (CMCM Operation)

ϕ_{pk} is proportional to $v_{2(ave)}$ and the losses are in turn proportional to ϕ_{pk}^2 and hence $v_{2(ave)}^2$. Expressing this with a lumped constant, k, then:

$$P_v = k[1 + (k_v - 1)\delta]^2 \tag{3.55}$$

This expands to give:

$$P_v = k\left[1 + 2(k_v - 1)\delta + (k_v - 1)^2 \delta^2\right] \tag{3.56}$$

Given that k_v is only slightly greater than one, then Equation (3.56) may be simplified to give:

$$P_v \approx k[1 + 2(k_v - 1)\delta] \tag{3.57}$$

Therefore, above δ_{TH}, the increase in P_v as δ approaches one, and hence the droop, may be approximated as directly proportional to the duty factor multiplied by a constant, in this case, $2k(k_v\text{-}1)$. For values of δ above δ_{TH}, the droop is now given by:

$$D_{ave} = k_4 \delta_{TH}^{\ 2} + k_5 (\delta - \delta_{TH}) \tag{3.58}$$

where k_5 is an empirically determined constant. Figure 3.34 shows the results from Figure 3.30, but with the enhanced algorithm described in Equation (3.58) used to correct the sensed current. It can be seen that the agreement is improved.

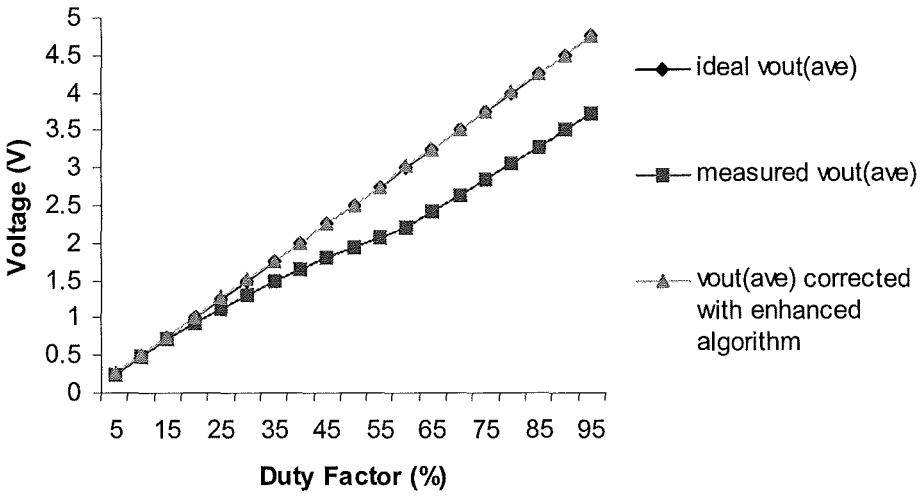


Figure 3.34. Effect of Enhanced Compensation Algorithm Applied to CT Output Signal (i_{L1} = 500 mA)

3.8 Thermal Effects

The measurements taken in this chapter are performed at room temperature, that is, at approximately 20 °C. The CT normally exhibits a very low temperature rise above ambient. However, the ambient temperature may be high in some applications, for example, in automotive power converters. The proximity of other components

dissipating heat, for example, power transformers and semiconductors may also lead to the CT operating at an elevated temperature.

Most ferrite materials have a negative core loss temperature coefficient at room temperature which progressively reduces in magnitude as the temperature increases and then becomes positive at typically 80 to 120 °C. Exemplifying measurements of the droop obtained from the circuitry in Figures 3.10-3.12 as the CT's temperature is varied are given in Appendix 3.

The flux excursion in the CT is primarily defined by the rectifier diode's forward voltage drop which is also temperature dependent, normally having a negative thermal coefficient. The diode's *v-i* characteristic is also, in any case, normally subject to broad tolerances.

3.9 Summary of Chapter

In a UCPT used with diode rectification, core losses are shown to predominately influence the theoretically predicted average current droop. Provided that the current pulse being measured does not entirely divert into the CT's magnetizing branch, simple algorithms have been shown to be appropriate for substantially correcting the sensed current to allow for core losses.

The correction algorithms may be applied to allow the use of a lower-permeability material with a higher Curie temperature, whilst still maintaining high accuracy. However, with ferrite core materials, a limitation arises if accuracy is to be obtained over a wide operating range as the losses are temperature-dependent. Difficulties include obtaining both accurate core loss data and information on the tolerances of that data for ferrite materials operating at low flux excursions.

CHAPTER 4

DIODE RECTIFICATION IN THE DUAL CURRENT TRANSFORMER ARRANGEMENT WITH NATURAL RESETTING

4.1 Introduction

The dual CT technique may be used with either diode rectification or synchronous rectification as shown in Figures 2.3 and 2.6 respectively. Although, as described in [45], a current synthesizer circuit may be used instead of a second CT, there are some circumstances where a second CT may be necessary, for example, where the requisite input or output voltages are not known for the purpose of estimating the required rate of change of current. The suitability of the core loss correction algorithms given in Chapter 3 when applied to the dual CT circuit with diode rectification is investigated in this chapter.

4.2 Application of Core Loss Correction Algorithms to the Dual CT Arrangement with Diode Rectification

With respect to the dual CT arrangement shown in Figure 2.3 and the top set of graphs in Figure 4.1, it can be seen that the total average current sensed is ideally independent of the duty factor of the signal driving TR1. However, with diode rectification and with R_B replaced by an active stage and therefore equal to zero, the flux swing in each transformer is approximated by the second from top set of graphs. Resultant losses in each CT's core are shown in the second from bottom graph. As described in Chapter 3, this is proportional to the droop where k_v is approximated as one. The bottom set of graphs shows the aggregate core losses.

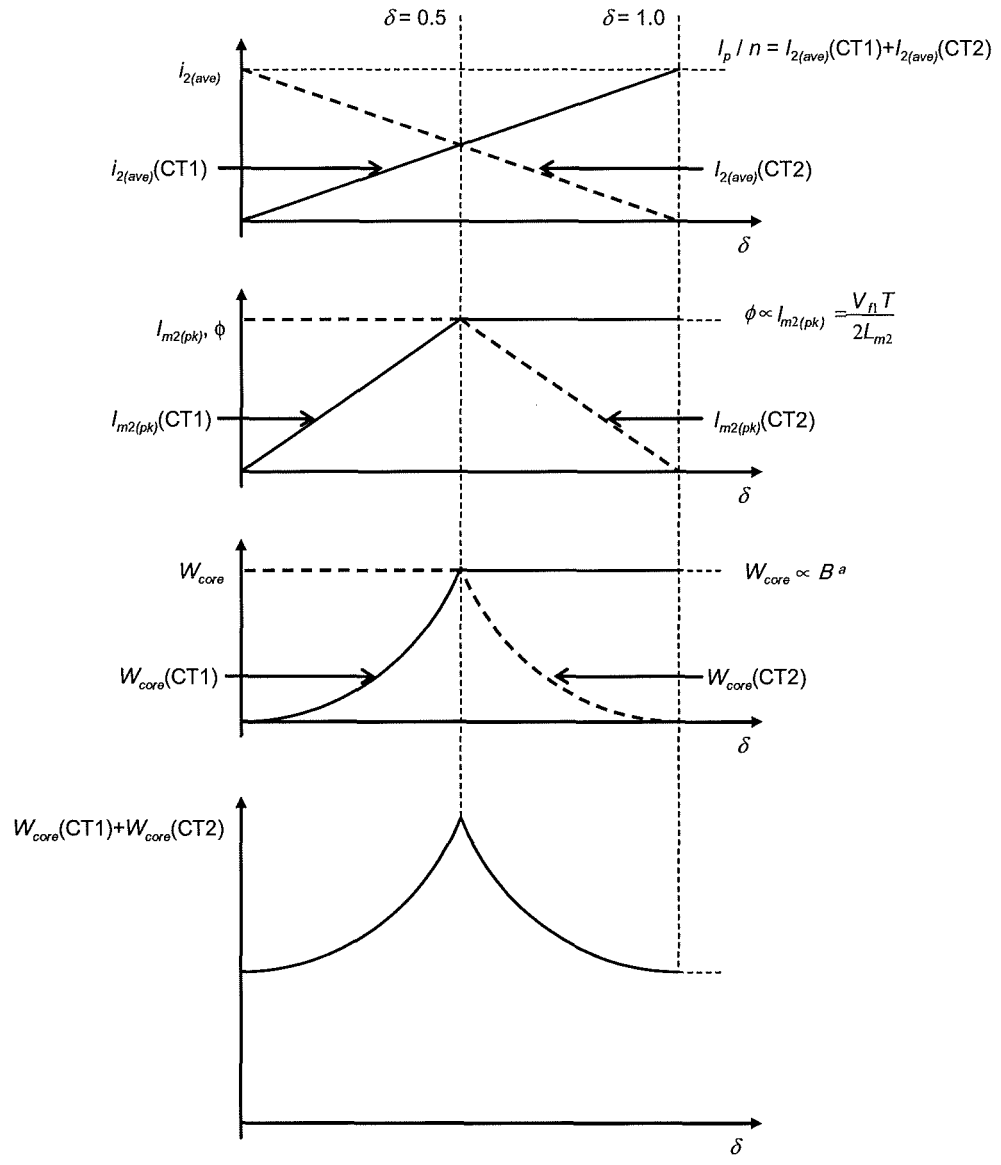


Figure 4.1. Idealized Graphs of Average Currents Sensed, Flux Density Swings and Expected Core Losses Plotted against Duty Factor for CTs in Dual CT Arrangement with Diode Rectification

As described in Chapter 3, losses in the CT (expressed as a current) are given by the formulae which are repeated here. Below the threshold duty factor, δ_{TH}, losses are:

$$i_{loss} = k_4 \left(\frac{\delta}{100} \right)^2 \Bigg|_{\delta \le \delta_{TH}} \tag{4.1}$$

where δ is expressed as a percentage. Also, above δ_{TH}, losses are given by:

$$i_{loss} = k_4 \left(\frac{\delta_{TH}}{100} \right)^2 \Bigg|_{\delta \geq \delta_{TH}} \tag{4.2}$$

The constants k_4 and δ_{TH} were empirically determined as being 2.224 and 60 % respectively in Chapter 3. The duty factor at which CT2 operates is 1-δ where δ is the duty factor at which TR1 is driven. Losses in CT1, CT2 and the total CT losses are shown in Figure 4.2. As δ_{TH} is greater than 50 %, two relatively shallow peaks are present instead of the single peak shown in Figure 4.1.

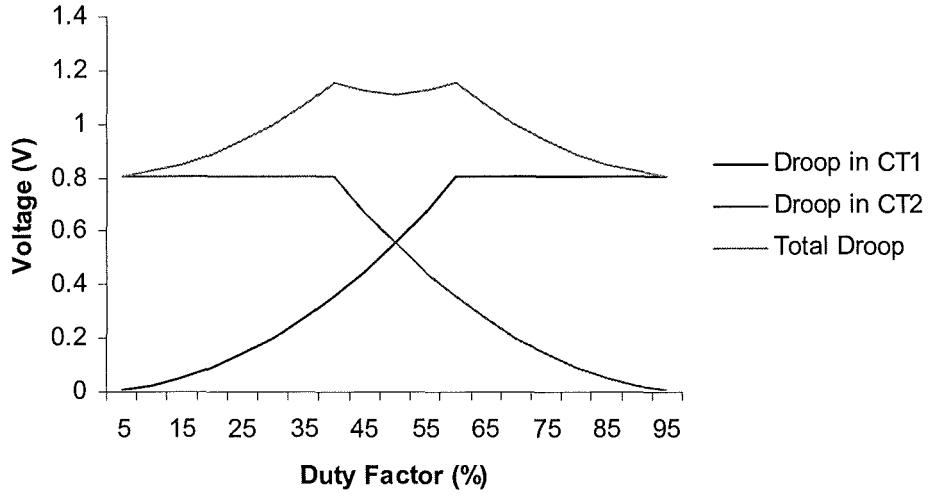


Figure 4.2. Expected Droop in CT1 and CT2 and Total Droop Plotted against Duty Factor

Figure 4.3 shows the expected droop where the enhanced compensation scheme is applied and, above δ_{TH}, the droop is now given by:

$$i_{loss} = k \left(\frac{\delta_{TH}}{100} \right)^2 + k_5 \left(\frac{\delta - \delta_{TH}}{100} \right) \Bigg|_{\delta \geq \delta_{TH}} \tag{4.3}$$

where k_5 is the constant empirically determined in Section 3.7 of Chapter 3.

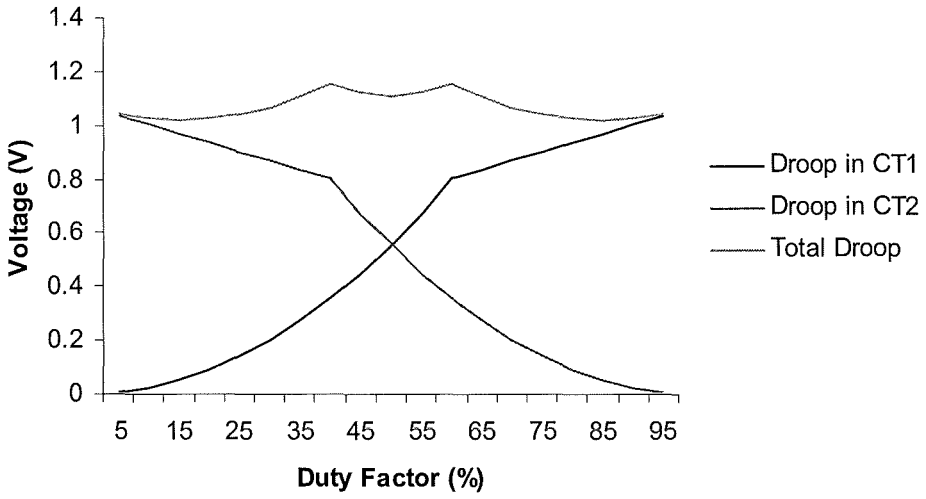


Figure 4.3. Expected Droop in CT1 and CT2 and Total Droop Plotted against Duty Factor with Enhanced Compensation Scheme Applied

4.3 Effect of Inclusion of Second CT on Current Slope Sensed during Power Device's On-Time

Where the dual CT arrangement is used with resonant resetting, the instantaneous output voltage (v_{out}) is comprised of two components. Firstly, a voltage proportional to the current under measurement less the component lost due to peak droop is present. Secondly, a component attributable to the resetting action of the complementary CT is present.

4.4 Experimentation

4.4.1 Experimental Arrangements

Droop with the dual CT arrangement was evaluated using the circuit shown in Figure 4.4. This is identical to the circuit in Figure 3.10, but with CT2 and D3 incorporated. CT2 is constructed identically to CT1, as summarized in Table 3.2.

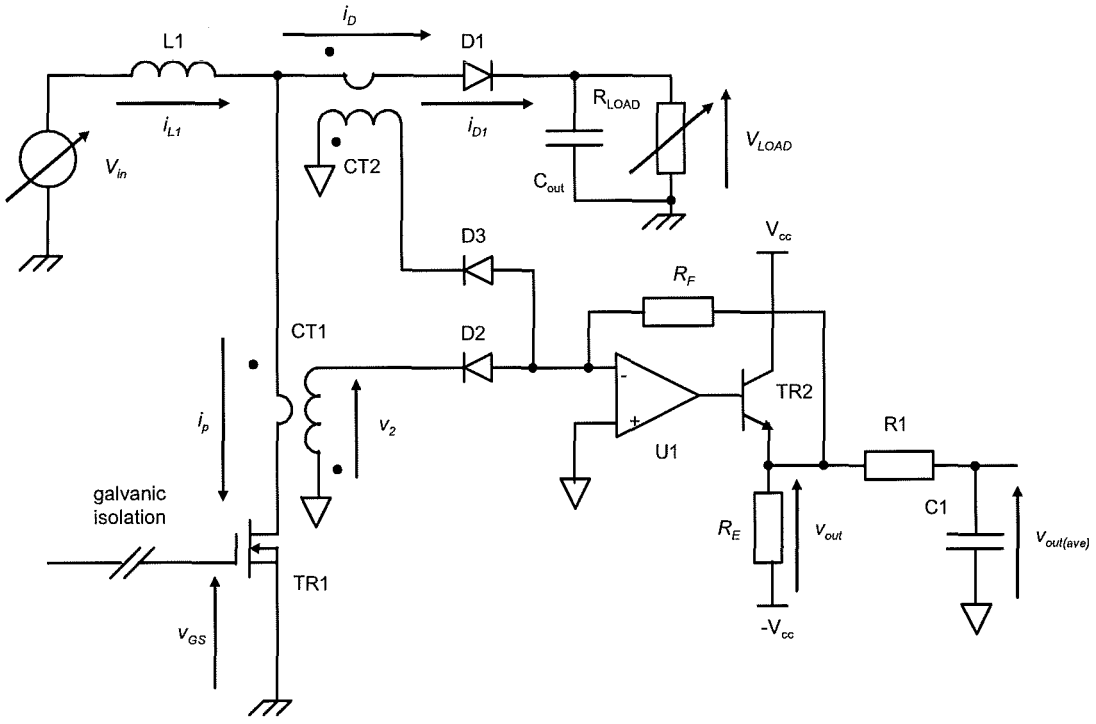


Figure 4.4. Converter Circuit Used for Experimentation with Diode Rectification in Dual CT Arrangement

4.4.2 Exemplifying Circuit Waveforms

Figure 4.5 shows exemplifying waveforms from the circuit in Figure 4.4 for $i_{L1(ave)} = 5$ A and $\delta = 50$ %. The values of $L1$, V_{in} and V_{LOAD} are selected here such that they allow

a visible rate of current change over the period of the switching waveform. The magnetizing currents in both CT1 and CT2 are continuous.

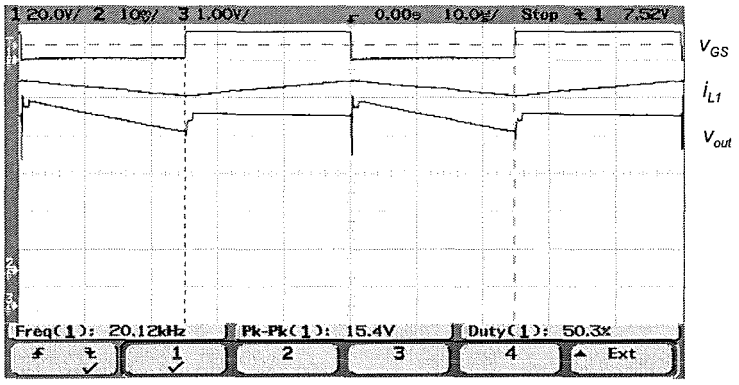


Figure 4.5. Exemplifying Waveforms from Dual CT Circuit with Diode Rectification and 50 % Duty Factor ($i_{L1(ave)}$ = 5 A) (v_{GS} = 20 V/div, i_{L1} = 1 A/div, v_{out} = 1 V/div, Time Scale: 10 μs/div)

From Figure 4.5 it is seen that the output voltage, v_{out}, during T_{on} is stepped as the decaying magnetizing current from the complementary CT is applied shortly after turn-on when the reset half-oscillation has elapsed. This may render peak current control problematic. Leading edge blanking (LEB) is normally incorporated [44] in peak current control schemes to mask the effect of the power diode's reverse recovery current and other transients at switch turn-on. However, T_r may exceed the length of these transients which are typically of 200-300 ns duration. The LEB time may be adjusted to exceed T_{reset} and provide smooth control, but this may be at the expense of an increased minimum power device on-time and some loss of device protection.

Figure 4.6 shows operation at a duty factor of 66 %. The magnetizing current in CT2, i_{m2}(CT2), is now discontinuous. As discussed in Section 4.3, this current affects the circuit's instantaneous output voltage (v_{out}). It can therefore be seen that the slope in v_{out} undergoes a change in trajectory when i_{m2}(CT2) commutates. This is shown in greater detail in Figure 4.7.

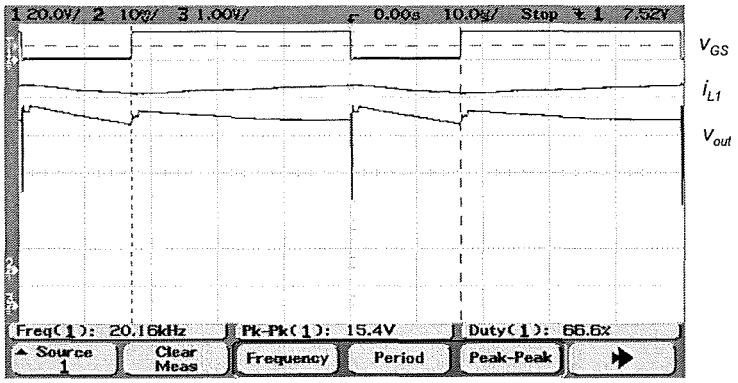


Figure 4.6. Exemplifying Waveforms from Dual CT Circuit with Diode Rectification and δ Set so that Magnetizing Current in CT2 is Discontinuous ($i_{L1(ave)}$ = 5 A) (v_{GS} = 20 V/div, i_{L1} = 1 A/div, v_{out} = 1 V/div, Time Scale: 10 μs/div)

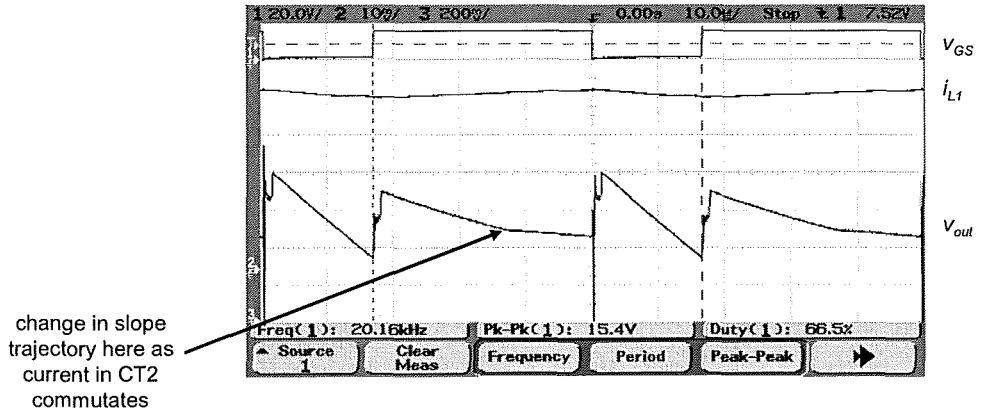


Figure 4.7. Waveforms from Figure 4.5 with v_{out} Shown in Greater Detail (v_{GS} = 20V/div, i_{L1} = 1 A/div, v_{out} = 200 mV/div, Time Scale: 10 μs/div)

The abrupt change in slope magnitude may, again, present a difficulty where the CT in series with the power switch is being used in a peak current control loop as well as acting as one of the two CTs in an average current measurement scheme. This is because slope compensation is normally incorporated to avoid sub-harmonic oscillations at duty factors above 50 % and to provide input voltage feed-forward. With effectively two slopes, a compromise is necessary where the current change due to the termination in the complementary CT's magnetizing current is significant. If the

magnetizing current is relatively high and the slope compensation is to be ideal (that is, providing 100 % feed-forward under all conditions) then a current synthesizer circuit may be preferred instead of a second CT for deriving the average current. Superimposition of the diode's detected current onto the transistor's detected current is therefore avoided. Alternatively, separate operational amplifiers may be used to detect the outputs from the CTs.

In Figures 4.5 to 4.7 the permutation of input and output voltages and the choke inductance are set to allow a discernible di/dt over a switching cycle for illustrative purposes. However, as in Chapter 3, for all subsequent measurements the choke size is now increased so that less than 5 % peak-to-peak current ripple is now present.

4.4.3 Experimental Results

Figure 4.8 shows readings of the average current droop against duty factor from the circuit in Figure 5.4 for $i_{L1(ave)}$ = 500 mA. The droop is calculated by subtracting the reading ($v_{out(ave)}$) from the expected output of 5 V. R_F is 1.2 kΩ here to enhance resolution and give the expected output of 5 V. Although the nominal core type and construction of CT2 is identical to that of CT1, no attempt is made to ensure that the core losses are identical. The curve giving the expected droop derived from the enhanced algorithm described by Equations (4.1) and (4.3) is also shown.

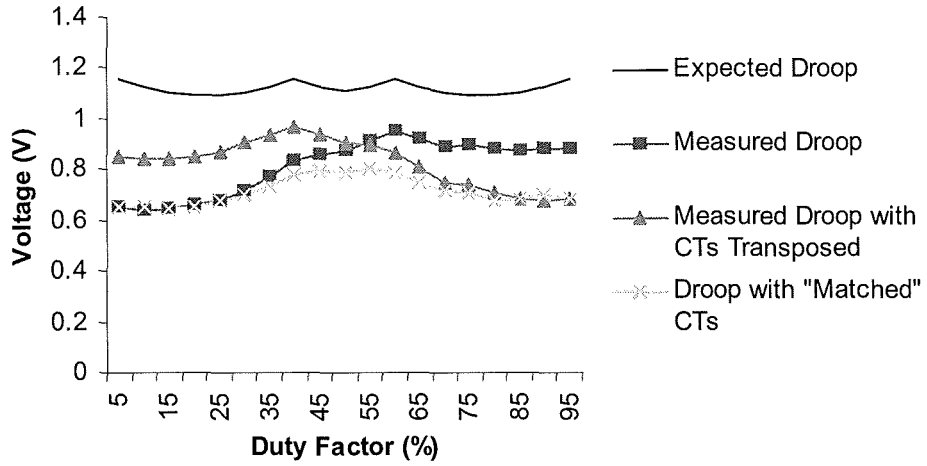


Figure 4.8. Expected and Measured Droop Using the Dual CT Arrangement with Diode Rectification ($i_{L1(ave)}$ = 500 mA)

It can be seen from Figure 4.8 that the agreement between the predicted and measured curves is relatively poor. Two factors are noted. Firstly, the loss disagrees with that given. Secondly, an asymmetry about δ = 50 % is observed. This is attributed to a mismatch between the CTs' core losses. This is verified by transposing them to yield the curve shown which shows reverse repeatability about δ = 50 %.

A third curve is now obtained using two experimentally matched cores. It can be seen that the symmetry of the losses about δ = 50 % is now improved.

4.4.4 Discussion of Experimental Results

It is concluded from the experimental results that to minimize droop, accurate information on core losses and their tolerances is required. However, even in the absence of this information, although applying a piecewise square-law and fixed-term core loss correction algorithm may be appropriate, a substantial reduction in droop may be achieved by simply adding in a fixed offset term throughout.

4.5 Summary of Chapter

Average current droop in the dual CT circuit with diode rectification has been evaluated. To minimize droop, accurate information on core losses and their tolerances is required. However, although applying a piecewise power-law and linear-term core loss correction algorithm to each CT may be appropriate, a substantial reduction in droop over the entire duty factor range may be achieved by simply adding in a fixed offset term throughout.

A drawback with using diode rectification in the dual CT circuit is that the current slope detected during the power switch's on-time has discontinuities imposed upon it by the action of the complementary CT. In both DMCM and CMCM operation, a step is imposed due to the application of the decaying magnetizing current in the complementary (diode) CT after the interval T_{reset}. In the DCMC mode a second step is introduced by the commutation of this current. This may prove a difficulty where the CT in series with the power switch is being used in a peak current control loop as well as acting as one of the two CTs in an average current measurement scheme.

CHAPTER 5

THE UNIDIRECTIONAL CURRENT PULSE TRANSFORMER WITH SYNCHRONOUS RECTIFICATION AND NATURAL RESETTING

5.1 Synchronous Rectification with Discrete MOSFET

As described in Chapter 2, synchronous rectification may be used instead of diode rectification with a UCPT. In [59] the droop is experimentally compared with that resulting with DR and a reset voltage circuit in place. However, in this chapter factors influencing the droop with SR are investigated in further detail. For a given CT, there are some significant differences when SR is compared with DR. The period of the reset voltage half-oscillation occurring when the current pulse ends is longer as the MOSFET's inter-terminal capacitance now augments that of the CT as described in [59] and Chapter 2. The peak amplitude of the half-oscillation is also lower due to both the presence of this capacitance and the lower magnetizing current when the current pulse is terminated. The minimum reset period is longer, an exception being where otherwise a voltage clamping diode would be used with DR to limit the peak reset voltage.

As shown in Figure 5.1, with DR V_{f2} is invariably greater than V_{f1} as, after the half-oscillation at turn-off, the magnetizing current passes through the MOSFET's intrinsic anti-parallel diode during T_{off}. The CMCM mode now commences at a much higher duty factor and operation is almost entirely in the DCMC mode. (V_{f1} is now given by $V_{f1} = i_2(R_2 + R_{DS(on)})$ and V_{f2} is the forward voltage drop across the SR MOSFET's intrinsic diode. The constant k_v is consequently smaller and primarily current-dependent.)

At the boundary condition where the core flux becomes continuous then $t_c = (1\text{-}\delta)T$. Therefore, from Equations (3.4) and (3.8):

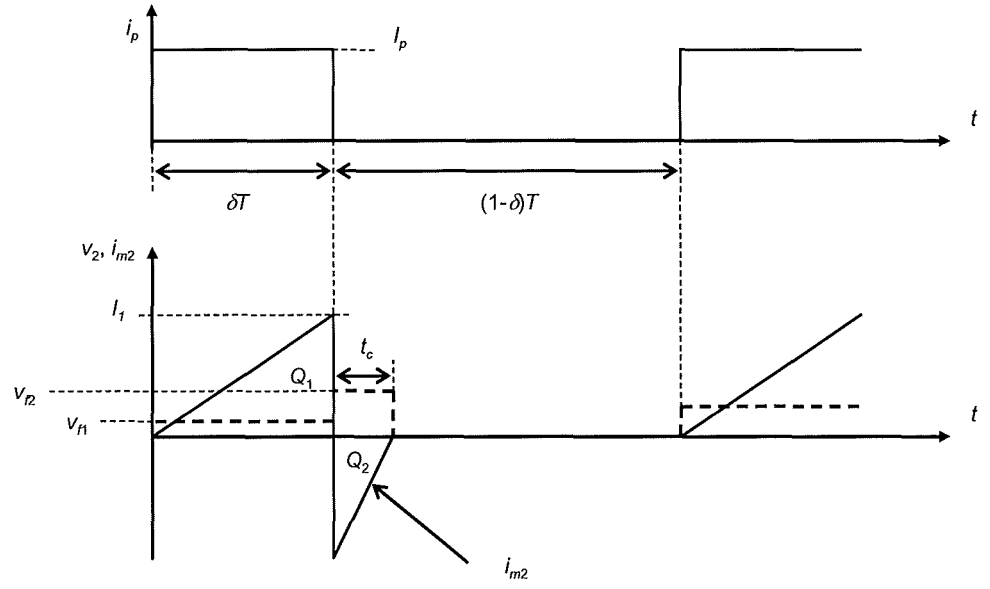


Figure 5.1. CT Magnetizing Current with Synchronous Rectification

$$\delta_{TH} = \frac{V_{f2}}{\left(\frac{i_P\left(R_w + R_{DS(on)}\right)}{n}\right) + V_{f2}} \tag{5.1}$$

Therefore, if V_{f1} is low compared to V_{f2} then δ_{TH} is close to one. However, due to the presence of C_{oss} when an SR MOSFET is used, T_r is more significant. In this case, at the onset of continuous conduction t_c may be obtained from:

$$T = \delta T + T_r + t_c \tag{5.2}$$

This rearranges to give:

$$t_c = T - \delta T - T_r \tag{5.3}$$

Putting Equation (5.1) into Equation (5.4) and rearranging gives:

$$\delta_{TH} = \frac{T - T_r}{\left(\frac{Ti_p\left(R_2 + R_{DS(on)}\right)}{nV_{f2}}\right) + T} \tag{5.4}$$

In the DR case the effect of the resonating current in the CT after the diode has ceased conducting in the forward direction during T_{off} is taken to be negligible. The peak voltage is insufficient to make the diode conduct again. However, with SR a capacitive route is provided for this current to flow into the operational amplifier's input and consequently affect its output voltage. For a lossless core material, negative droop is expected with DR. Measurements in Chapter 3 show that this is the case where the core flux excursion and consequent losses are low, although it is shown that for certain practical current levels positive droop is expected due to core losses in the CT. With SR, although for a given CT the core flux excursion is less, the droop is expected to be positive at all combinations of frequency, current and duty factor due to k_v being less than one.

5.1.1 Categorization of Synchronous Rectification Topologies for Use with the CT

Where the output from a CT is to be synchronously rectified, several topologies may be implemented other than that shown in Figures 2.5a and 2.6 and presented in [59]. The possible permutations with both N- and P-channel MOSFETS are categorized here. The junction field effect transistor (JFET) is not considered due to its $R_{DS(on)}$ rating being too high for this application.

5.1.2 Synchronous Rectifier Topologies with N-Channel MOSFET

Figure 5.2 shows the possible topological permutations where an N-channel MOSFET is used for SR. In each case the dotted end of the CT secondary winding goes positive when a current pulse is applied. The properties of the arrangements in Figure 5.1 are

tabulated in Table 5.1. Several criteria are applicable when selecting a topology. Whether the output voltage is negative or positive is of interest here as most commercially available power control ICs operate from a single rail and a positive output voltage from the operational amplifier is preferred. Referencing the MOSFET's gate signal to "zero" volts is also preferred as this is normally the reference voltage for the power device drive signal produced by the IC.

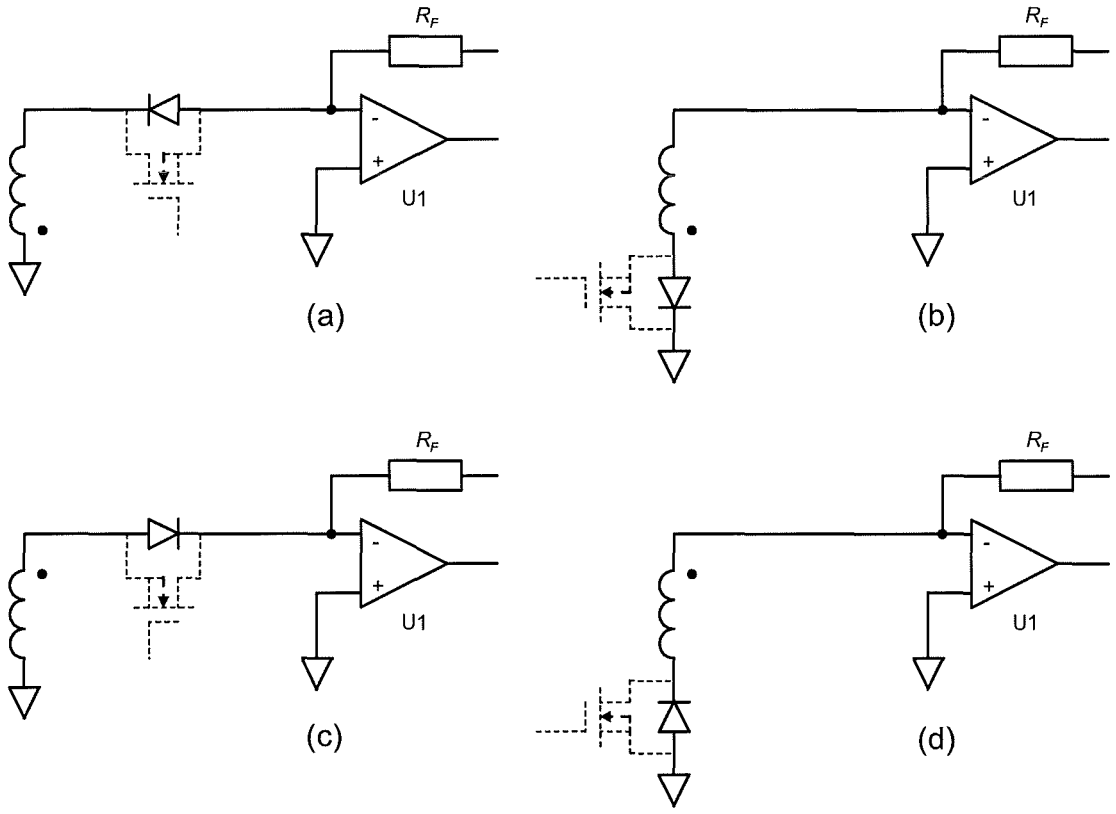


Figure 5.2. Topologies for UCPT with Synchronous Rectification using N-Channel MOSFET

The requirement for gate-drive level-shift circuitry is therefore avoided. Another criterion is that, for improved accuracy, it is desirable that the return path for the MOSFET'S transient gate-drive current is not common with the CT's secondary current flowing into the operational amplifier's non-inverting terminal.

Topology	Operational amplifier output voltage polarity	Non-changing reference electrode (MOSFET source) potential held at 0V?	Undesired output voltage developed by gate charging current?
(a)	Positive	Yes	Yes
(b)	Positive	No	No
(c)	Negative	No	No
(d)	Negative	Yes	No

Table 5.1. Properties of Topologies for UCPT with Synchronous Rectification using N-Channel MOSFET

With reference to Table 5.1, it can be seen that no ideal combination of parameters is available, that is, a positive output voltage, a non-floating reference electrode voltage and no undesired output voltage developed by the MOSFET's gate charging current.

5.1.3 Synchronous Rectifier Topologies with P-Channel MOSFET

Figure 5.3 shows the possible topological permutations where a P-channel MOSFET is used for SR. (Again, in each case the dotted end of the CT secondary winding goes positive when a current pulse is applied.) The P-channel MOSFET presents two disadvantages in this application. Its $R_{DS(on)}$ rating for a given die area and voltage rating is approximately 2.5 times that of an equivalent N-channel MOSFET due to the lower mobility of the carriers (holes) compared to electrons. Also, a negative gate voltage is required to turn the device on[1].

[1] The main application for the P-channel MOSFET in power electronics is at low power levels where it acts as a switch referenced to a positive supply rail. The negative gate voltage requirement is useful in these applications as the requirement for level-shifting circuitry for driving the gate is avoided and this may outweigh the disadvantage of its higher on-state resistance.

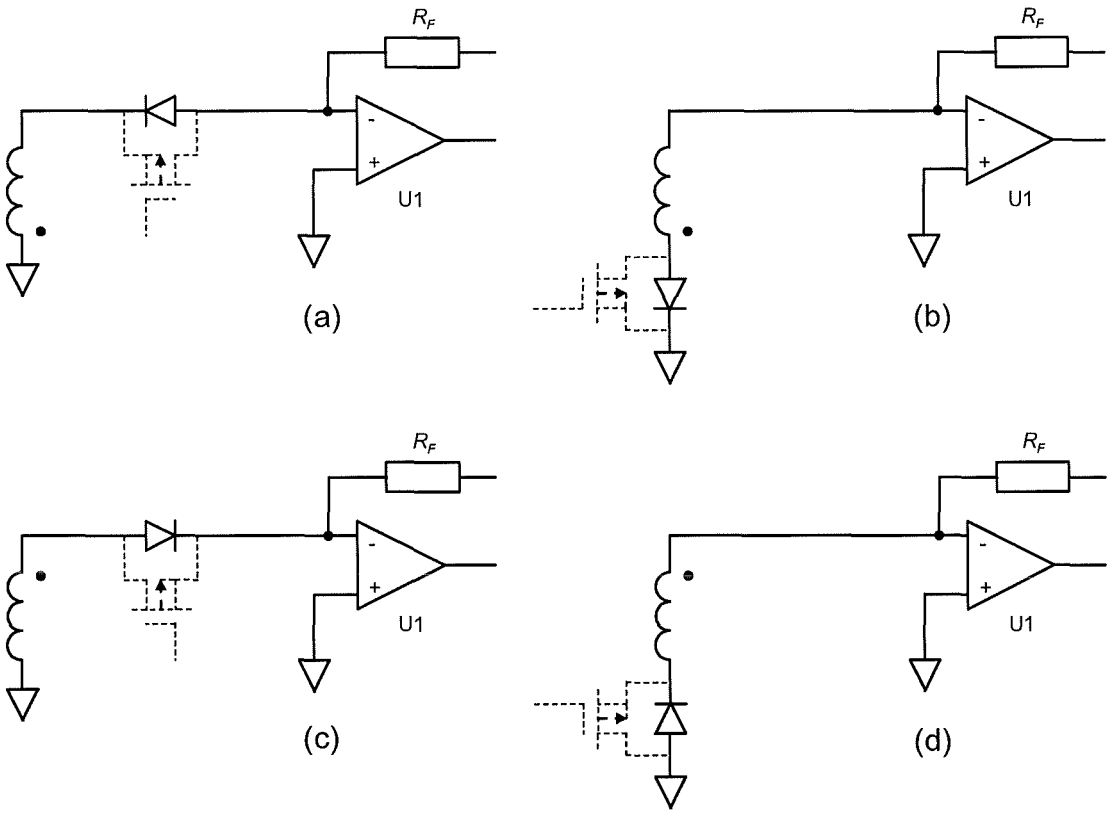


Figure 5.3. Topologies for UCPT with Synchronous Rectification using P-Channel MOSFET

The properties of the arrangements in Figure 5.3 are tabulated in Table 5.2. It can again be seen that no ideal combination of parameters is available.

Topology	Operational amplifier output voltage polarity	Non-changing reference electrode (MOSFET source) potential held at 0V?	Undesired output voltage developed by gate charging current?
(a)	Positive	No	No
(b)	Positive	Yes	No
(c)	Negative	Yes	Yes
(d)	Negative	No	No

Table 5.2. Properties of Topologies for UCPT with Synchronous Rectification using P-Channel MOSFET

5.1.4 Experimentation with Discrete MOSFET SR

5.1.4.1 Experimental Arrangements

Figure 5.4 shows the experimental circuit used. This is identical to that in Figure 3.10, but with the rectifier diode replaced with an N-channel MOSFET (TR3) acting as the SR device.

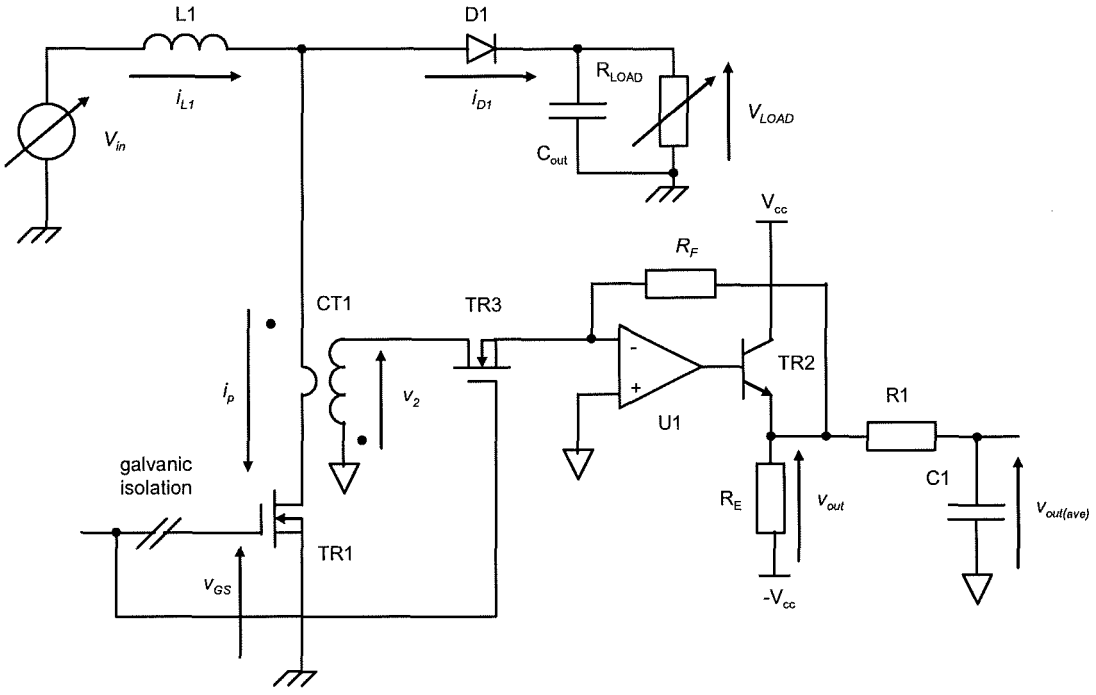


Figure 5.4. Converter Circuit Used for Experimentation with Synchronous Rectification Implemented with Discrete MOSFET

TR3 is a Zetex ZVN4306A device and its principal parameters of interest here are given in Table 5.3. The CT used throughout the experimentation here is the variant in 3F3 core material described in Table 3.2. The same physical core was used so that DR and SR could be directly compared without the effects of variations in the core characteristics.

V_{DS}	60	V	V_{GS} = 0 V, I_D = 1 mA
$R_{DS(on)}$ (maximum)	450	mΩ	V_{GS} = 5 V, I_D = 1.5 A
$V_{GS(th)}$	1.3-3.0	V	V_{GS} = V_{DS}, I_D = 1 mA
C_{oss}	140	pF	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz
C_{iss}	350	pF	

Table 5.3. SR MOSFET Principal Parameters of Interest

5.1.4.2 Estimate of Effect of CT Core Losses with Synchronous Rectification

The peak flux density excursion, B, is:

$$B = \frac{NI_{m2(0)}\mu_0\mu_r}{l_e} \tag{5.5}$$

Putting Equation (2.30) into Equation (5.5) yields:

$$B = \frac{I_p(R_2 + R_{SR})\delta T}{N_2{}^2 A_e} \tag{5.6}$$

as $n = N_2$, that is, N_1 has one turn here.

At I_p = 5 A, R_2 = 0.89 Ω, $R_{SR} = R_{DS(on)}$ = 0.45 Ω, a duty factor of 100 % and f = 20 kHz (T = 50 μs) then the maximum core flux excursion is calculated as 5.2 mT. The effect of core material losses is therefore predicted to be very small.

5.1.4.3 Synchronous Rectifier MOSFET Gate Charge Effects

Before proceeding with obtaining results, the practical issue of driving the SR MOSFET's gate is addressed. The arrangement in Figure 5.5 is that shown in configuration (a) in Figure 5.2 where the return connection to the gate terminal is made via the signal ground voltage rail. As shown in Figure 5.5, the gate charging

current (i_G) supplied to the MOSFET is therefore injected into the node connected to the operational amplifier's inverting terminal and consequently develops an unwanted transient output voltage as it is routed through R_F.

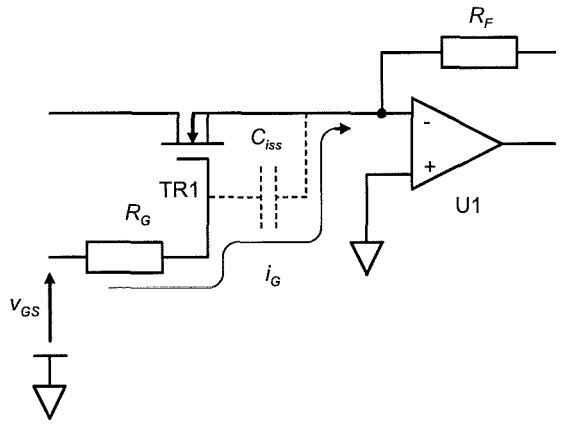


Figure 5.5. Route Taken by SR MOSFET Gate Charging Current

When SR is used with the dual CT arrangement where two MOSFETs are driven with complementary gate signals, as shown in Figure 2.6, some reduction of the unwanted signals results as the gate charging current of one MOSFET is cancelled by the discharging current of the other. This is shown in Figure 5.6. However, it is not expected that the unwanted signals may be entirely eliminated due to the non-linearity of the MOSFETs' input capacitances.

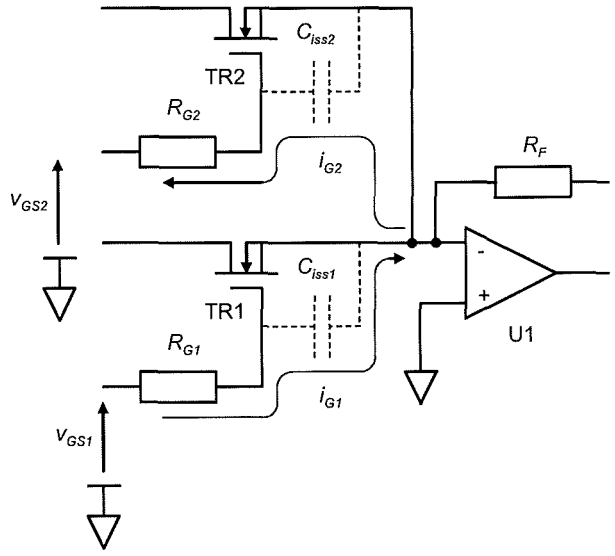


Figure 5.6. Routes Taken by SR MOSFET Gate Charging Currents in Dual CT Arrangement

Figure 5.7 shows waveforms from the circuit in Figure 5.5 with a gate resistance of 100 Ω used to limit i_G. The choke current is 500 mA and R_F = 1.2 kΩ. The upper trace shows the gate voltage (5 V in the on-state) applied to the power MOSFET, the centre trace shows the gate voltage applied to TR3 and the lower trace shows v_{out}. It can be seen that disturbances result on the output voltage at turn-on and turn-off.

The maximum gate-source voltage allowable with the ZVN4306A device is specified as being within ±20 V. However, this is a logic-level device and is designed to be satisfactorily operated from a 5 V drive signal. Although the channel resistance becomes lower as the voltage is increased above the threshold voltage, the gate charge required rises disproportionately with respect to the improvement in conductivity.

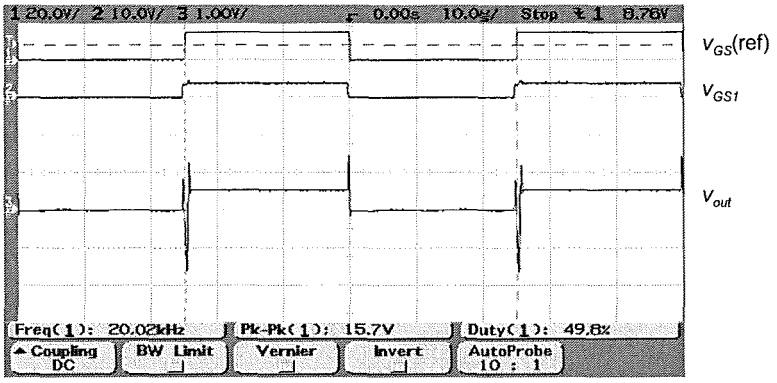


Figure 5.7. Waveforms with $v_{GS(on)}$ = 5 V, R_G = 100 Ω (i_{L1} = 500 mA) (v_{GS} = 20 V/div, v_{GS1} = 10 V/div, v_{out} = 1 V/div, Time Scale: 10 µs/div)

Figure 5.8 shows waveforms, again from the circuit in Figure 5.5, but with the gate resistance now increased to 1 kΩ. The disturbances on the output voltage are now less severe. However, as can be seen, transient exponential terms are added to the measured current at turn-on and turn-off.

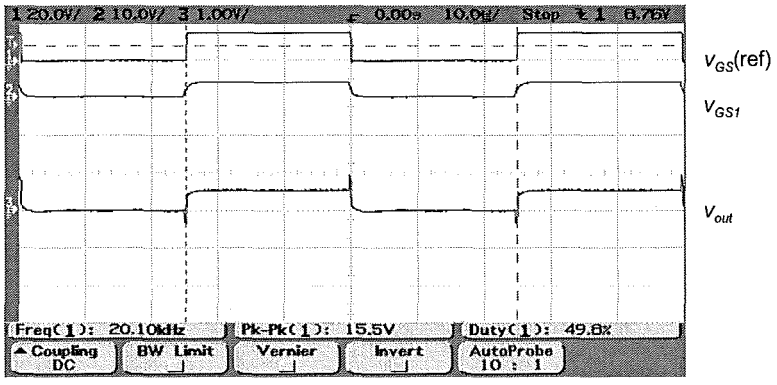


Figure 5.8. Waveforms with $v_{GS(on)}$ = 5 V, R_G = 1 kΩ (i_{L1} = 500 mA) (v_{GS} = 20 V/div, v_{GS1} = 10 V/div, v_{out} = 1 V/div, Time Scale: 10 µs/div)

Figure 5.9 shows the voltage obtained from the circuit in Figure 5.6 where the second MOSFET is added in position TR2 and driven with a complementary signal. Its drain terminal is short-circuited to its source terminal. Both R_{G1} and R_{G2} are 100 Ω. A 74AC

series logic gate is used as the inverter. This logic series has a propagation delay of approximately 4 ns so minimal timing skew is imposed between the two gate signals.

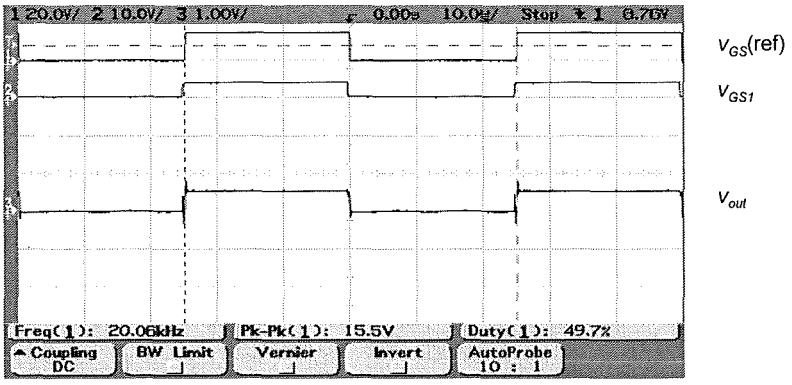


Figure 5.9. Waveforms with $v_{GS(on)}$ = 5 V and Complementary MOSFET in Place with $R_{G1} = R_{G2}$ = 100 Ω (i_{L1} = 500 mA) (v_{GS} = 20V/div, v_{GS1} = 10V/div, v_{out} = 1 V/div, Time Scale: 10 µs/div)

In order to minimize the effect of the passage of gate charge, all subsequent experimental readings are taken with R_G = 1 kΩ.

However, where the CT is used in a peak current control scheme a disturbance is not necessarily problematic when the current pulse is applied. This is because of the leading edge blanking described in [44] and discussed in Section 4.4.2. The current is also not monitored during the switch's off-time so, for peak current control purposes, the disturbance at turn-off is also not necessarily problematic. The $R_{DS(on)}$ value given in Table 5.3 is the manufacturer's quoted maximum value. However, for experimental purposes, the actual value was measured at 0.37 Ω for $V_{GS(on)}$ = 5 V and I_D = 100 mA when at room temperature.

5.1.4.4 Experimental Results with Discrete MOSFET SR

Figures 5.10, 5.11 and 5.12 show exemplifying waveforms at I_{L1} = 5 A. The switching frequency is 20 kHz and the duty factor is set at 50 %.

It is noted that, due to the propagation delay introduced by the galvanic isolation element in Figure 5.4, the gate signal applied to the power MOSFET (TR1) lags behind that applied to the TR3 by approximately 300 ns at both turn-on and turn-off. The oscillatory frequency is measured at 91 kHz. It can be seen from Figure 5.12 that, when compared to Figures 3.15 and 3.18 where diode rectification is used, the peak current droop is now reduced.

Some observations are made with respect to Figures 5.10, 5.11 and 5.12. Operation here is discontinuous. During the power switch's off-time the same three phases are evident as when DR is used. Firstly, the half-oscillation takes place. Secondly, the diode (in this case the SR MOSFET's intrinsic diode) conducts and thirdly, there is an oscillation with a peak magnitude of approximately 0.8 V when the diode ceases to conduct. The volt-second product appearing across the diode when resetting appears to be greater than the volt-second product appearing when the pulse is applied. However, this is expected because, as the voltage dropped across the SR MOSFET's on-state resistance (0.37 Ω) is low compared to the CT's secondary winding resistance (R_2 = 0.89 Ω), then most of the voltage drop impressed across the CT's magnetizing branch is internal to the CT.

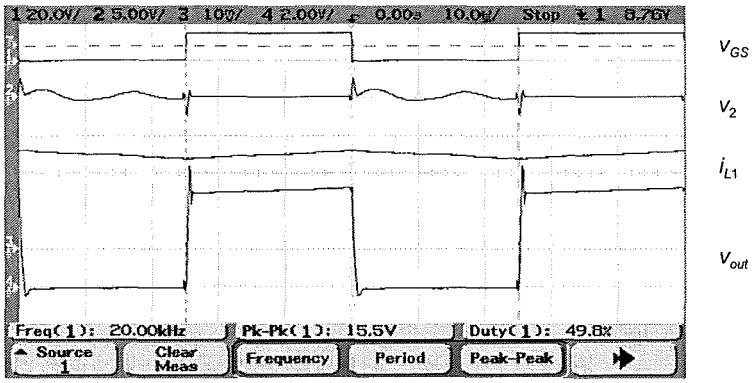


Figure 5.10. Waveforms at 50% Duty Factor with SR (I_{L1}= 5 A) (v_{GS} = 20 V/div, v_2 = 5 V/div, i_{L1} = 2 A/div, v_{out} = 2 V/div, Time Scale: 10 µs/div)

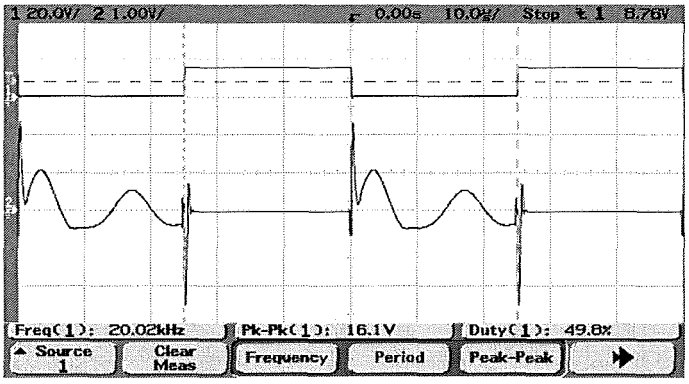


Figure 5.11. v_2 Shown in Greater Detail (v_{GS} = 20 V/div, v_2 = 5 V/div, Time Scale: 10 µs/div)

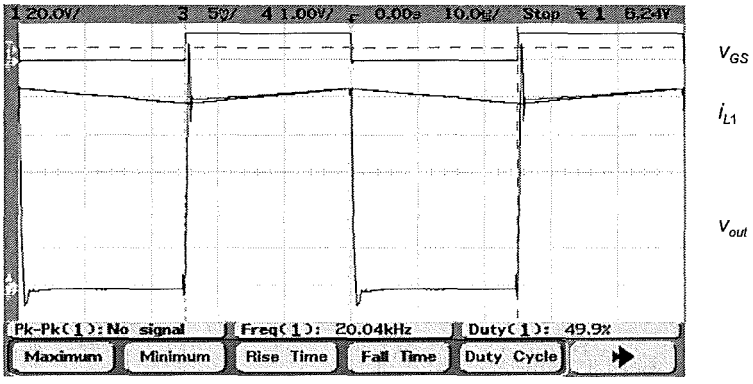


Figure 5.12. Waveforms i_{L1} and v_{out} Shown in Greater Detail (v_{GS} = 20 V/div, i_{L1} = 2 A/div, v_{out} = 1 V/div, Time Scale: 10 µs/div)

In previous figures the permutation of input and output voltages and the choke inductance are set to allow a discernible di/dt over a switching cycle for illustrative purposes. However, for subsequent measurements the choke size is now increased so that less than 1 % current ripple is now present.

Figures 5.13, 5.14 and 5.15 show the measured and ideal sensed output voltages against δ for currents of 5 A, 3 A and 1 A respectively. It is seen that the maximum duty factor attainable prior to incomplete reset causing droop is, as expected, lower than that with DR. Putting the values of R_2 and L_{m2} in Table 3.2 and the value of $R_{DS(on)}$ measured here (0.37 Ω) into Equation (2.34) gives an expected D_{ave} of:

$$D_{ave} = \delta \times 2.9 \times 10^{-3} \tag{5.7}$$

assuming that the current-time product recovered from the CT during T_{off} is negligible, that is, V_{f2} is much greater than V_{f1}. Figure 5.16 shows the measured droop for choke currents of 5 A, 3 A and 1 A and the predicted droop from Equation (5.7).

Figure 5.17 shows the absolute measured droop (expressed as the shortfall in $v_{out(ave)}$) for choke currents of 5 A, 3 A and 1 A. It can be seen that the droop is dominated by the oscillatory behaviour of the circuit during the switch's off-time.

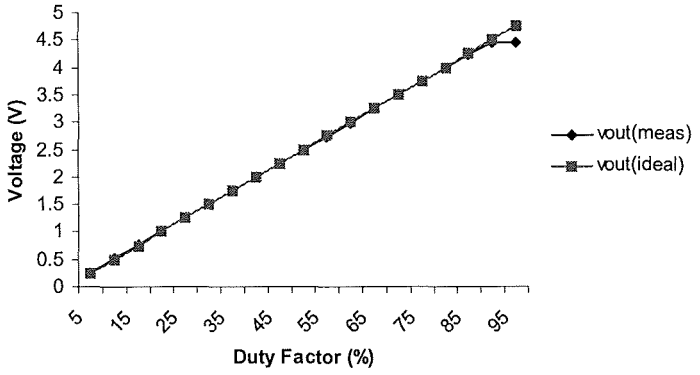


Figure 5.13. Measured and Ideal $v_{out(ave)}$ against Duty Factor

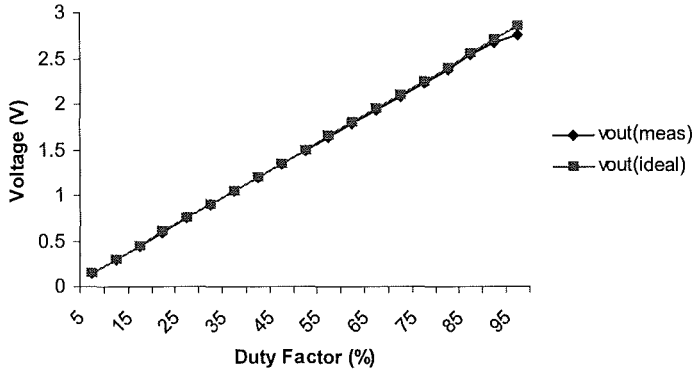


Figure 5.14. Measured and Ideal $v_{out(ave)}$ against Duty Factor

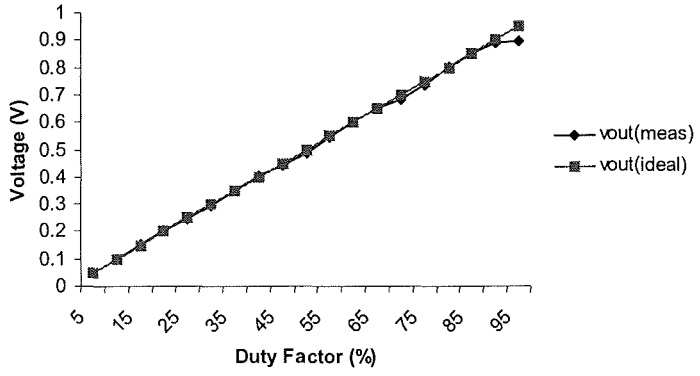


Figure 5.15. Measured and Ideal $v_{out(ave)}$ against Duty Factor

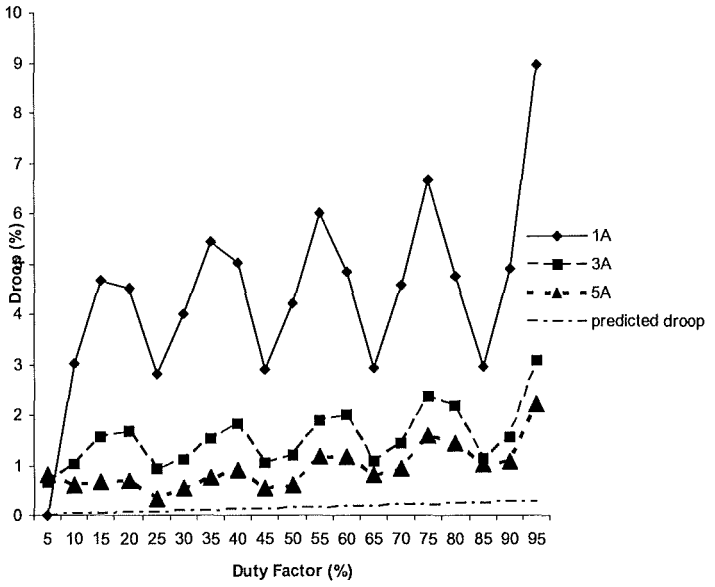


Figure 5.16. Droop against Duty Factor for i_{L1} = 5 A, 3 A and 1 A with Calculated Droop also Shown

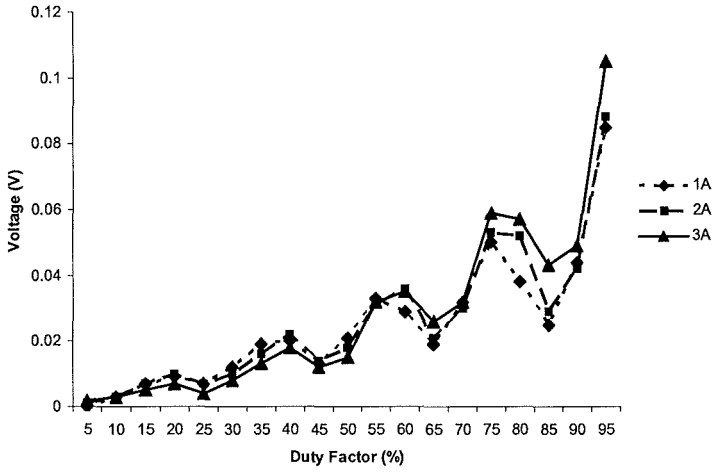


Figure 5.17. Absolute Droop Expressed as Shortfall in $v_{out(ave)}$ against Duty Factor for i_{L1} = 5 A, 3 A and 1 A

Figure 5.18 shows a more complete circuit representation of the MOSFET. The MOSFET's inter-terminal capacitance, in addition to lengthening the required minimum reset time presents an additional disadvantage in this application. As one end of this capacitance is connected not to the zero voltage rail but to the virtual

ground at the operational amplifier's inverting terminal, most of the resonating magnetizing current flows through R_F, developing a consequent voltage.

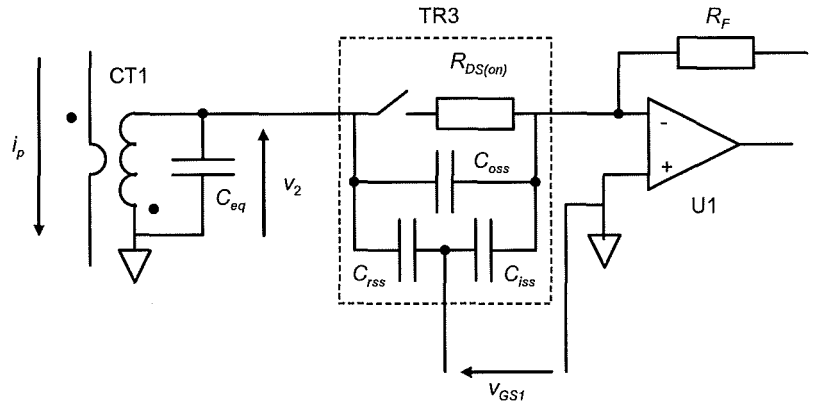


Figure 5.18. More Complete Representation of the MOSFET in CT Rectifier Application

5.2 Synchronous Rectification with Analogue Switch

5.2.1 Experimental Circuit

Figure 5.19 shows the circuit from Figure 5.4, but using a Texas Instruments TS5A3159 analogue switch [75] instead of a discrete MOSFET as the SR element.

Figure 5.20 shows (gate) waveforms for comparison with those from Figures 5.5-5.7. Figure 5.21 shows the average current droop for I_{L1} = 5 A, 3 A and 1 A for comparison with the values in Figure 5.16. The estimated droop is also shown, again calculated from Equation 2.35, but with $R_{DS(on)}$ taken as 1.1 Ω from the data in [75]. It is noted that the resonant frequency of the oscillation at turn-off is approximately 310 kHz, that is, similar to that measured with diode rectification in Chapter 3. The effect of capacitive loading is therefore minimal. Over the range of currents and pulse lengths measured here, the peak reset voltage is such that it does not exceed the analogue switch's maximum input voltage.

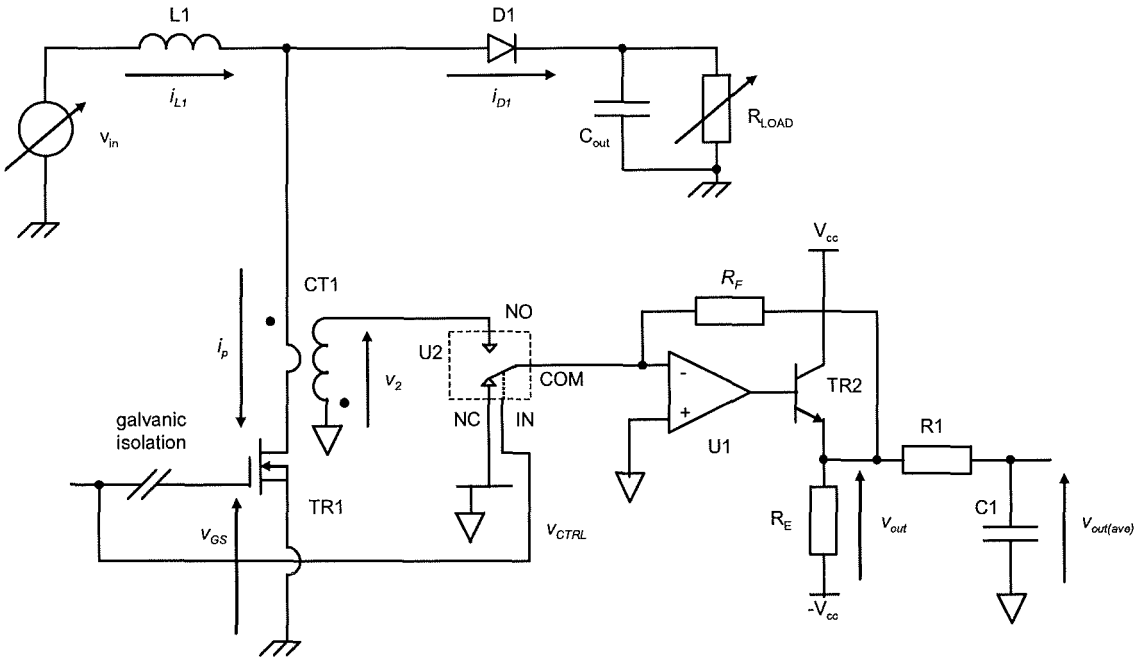


Figure 5.19. Converter Circuit Used for Experimentation with Synchronous Rectification Implemented with Analogue Switch

5.2.2 Experimental Results with Analogue Switch SR

Figure 5.20 shows the measured droop with analogue switch SR. The negative droop in Figure 5.20 is attributed to an asymmetry in the rise and fall times of the operational amplifier's output voltage when the current pulse is applied and removed, as discussed in Section 2.2.2. The rise and fall times of the current pulse and voltage gain of the amplifier are set such that v_{out} is limited by the slew rates. From Figure 5.21, a volt-second difference of approximately 0.5 μVs is imposed. The fall-time is found to be essentially independent of current magnitude and therefore the effect on droop is also fundamentally independent of current magnitude. It is noted here that the operational amplifier is driven with a large signal when the current pulse is applied and a small signal when it is removed. To illustrate the importance of the operational amplifier's performance here, Figure 5.22 shows the effect on v_{out} of using an alternative operational amplifier (the OPA134PA type) with a slower response upon current pulse removal.

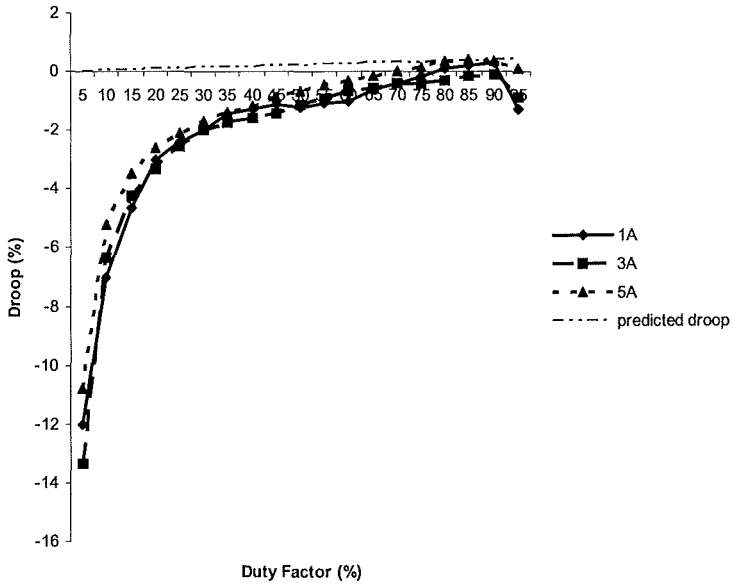


Figure 5.20. Droop against Duty Factor for i_{L1} = 5 A, 3 A and 1 A with Calculated Droop also Shown (Analogue Switch SR)

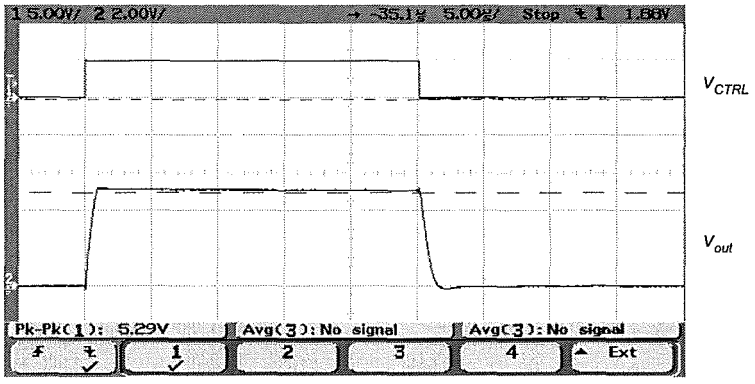


Figure 5.21. Control and v_{out} Waveforms with NE5534AP Operational Amplifier (v_{CTRL} = 5 V/div, v_{out} = 2 V/div, v_{out} = 1 V/div, Time Scale: 5 µs/div)

Figure 5.22. Control and v_{out} Waveforms with OPA134PA Operational Amplifier (v_{CTRL} = 5 V/div, v_{out} = 2 V/div, v_{out} = 1 V/div, Time Scale: 5 µs/div)

Returning to Figure 5.21, Figures 5.23 and 5.24 show the transient waveforms at I_{L1} = 5 A and 1 A respectively in greater detail.

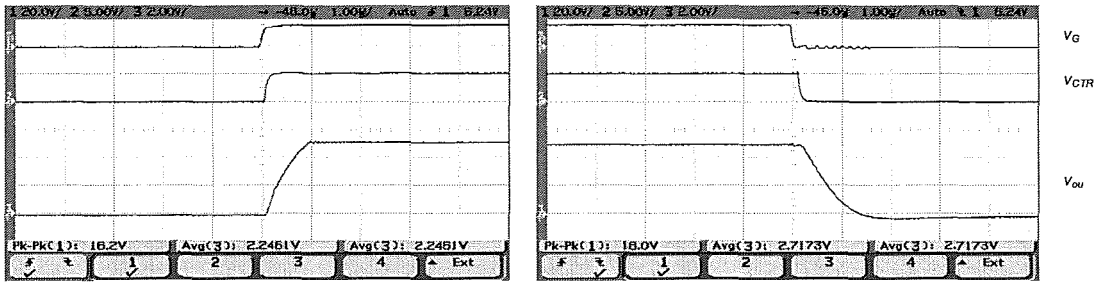


Figure 23. Transient Waveforms in Greater Detail at I_{L1} = 5 A with NE5534AP Operational Amplifier (v_{GS} = 20 V/div, v_{CTRL} = 5 V/div, v_{out} = 1 V/div, Time Scale: 1 µs/div)

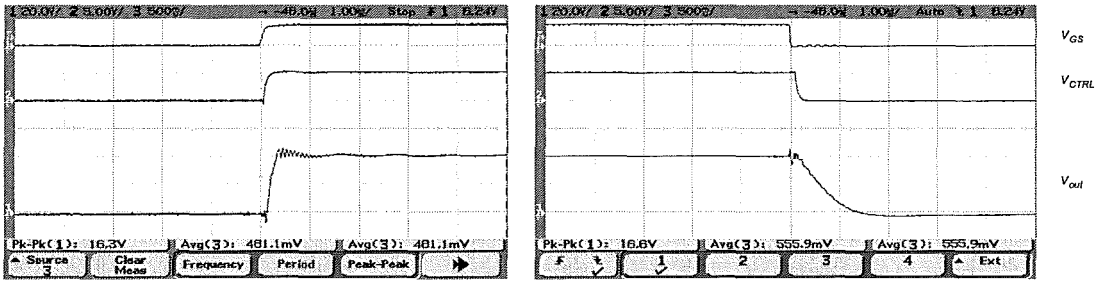


Figure 24. Transient Waveforms in Greater Detail at I_{L1} = 1 A with NE5534AP Operational Amplifier (v_{GS} = 20 V/div, v_{CTRL} = 5 V/div, v_{out} = 500 mV/div, Time Scale: 1 µs/div)

5.3 Discussion of Experimental Results and Summary of Chapter

Either a discrete MOSFET or an analogue switch may be used for SR. The following observations are made:

1. Where a MOSFET is used, driving its control (gate) terminal is not a trivial consideration. Transient interference results. This, and the excitation of the LC circuit formed by L_{m2} and C_{eq} both impair accuracy.
2. An analogue switch may therefore be preferred. It is noted that this device is intended for signal routing. As such, it is optimized to minimize "crosstalk" between the signal at the control terminal and signal being routed. Also, inter-terminal capacitances are low to reduce signal degradation. This has the dual benefit here of minimizing oscillations and allowing operation at a duty factor approximately equal to that with DR.
3. The transient performance of the operational amplifier remains a limiting factor in determining the accuracy of the CT circuit.

CHAPTER 6

APPLICATION OF RESET VOLTAGE FEEDBACK FOR DROOP MINIMIZATION IN THE UNIDIRECTIONAL CURRENT PULSE TRANSFORMER

6.1 Introduction

A technique for minimizing the peak current droop in the signal derived from a UCPT is investigated in this chapter. This is achieved by applying a correcting voltage in series with the CT's output terminals when a current pulse is present. The magnitude of the correcting voltage is based on the resetting voltage sensed during the power converter's previous switching cycles. An experimental circuit is implemented to investigate the technique's effect on both peak and average current droop. A passive diode rectifier and resistive load is used. Results are compared with a circuit simulation.

6.2 Operating Principle

The technique investigated here may be loosely grouped with those techniques where the CT's core flux is sensed and its secondary terminal voltage is modified in response to minimize the flux. Such techniques may be further sub-divided into those where the flux is sensed directly by a detector element placed in the magnetic circuit, for example, in [11] and [14] and those where it is inferred indirectly, for example, in [29] where the rate of change of flux is sensed. The technique here may be grouped in the latter sub-division as the core flux is also sensed indirectly by measuring another quantity in this case, the CT's reset voltage. In [29], as shown in Figure 6.1(a), a tertiary winding on the CT is used to provide a voltage proportional to the rate of change of flux present in the core (v_{N3}). Alternatively, as shown in Figure 6.1(b), a Hall-plate may be used to directly sense the core flux and produce a proportional

voltage (v_{HE}). In either case, this voltage is amplified as by A1 to yield a correcting voltage (v_c) which is applied in series with the CT's secondary terminal voltage. As shown in Figure 6.2, the emf across the CT's magnetizing branch is therefore reduced, in turn reducing the peak current droop.

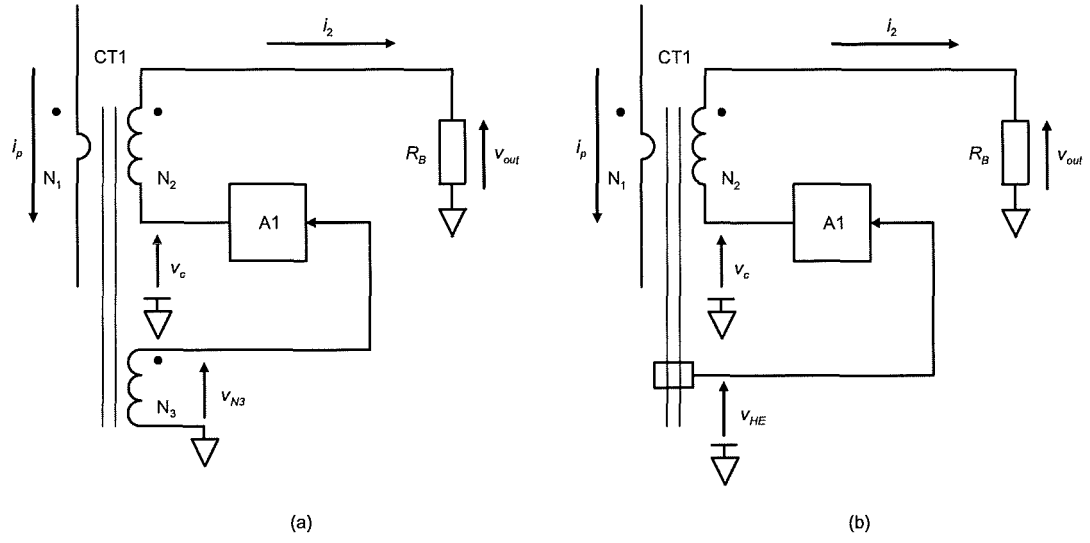


Figure 6.1. Circuits for Correcting CT Secondary Terminal Voltage in Response to Rate of Core Flux Change Detected with (a) Tertiary Winding and (b) Flux Detected Using Hall-Plate

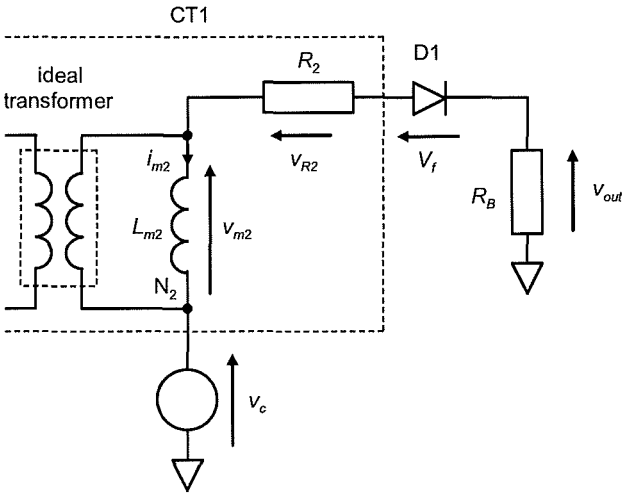


Figure 6.2. Equivalent Circuit during Current Pulse with Correcting Voltage Applied to CT's Secondary Winding

The principal advantage of the technique here compared to those in Figure 6.1 is that the CT's construction is not modified. Figure 6.3 shows a functional block diagram outlining the technique investigated here and Figure 6.4 shows the principal idealized waveforms. TR1 is the switching device in a power converter and CT1 is in series with it acting as a UCPT. D1 is the CT's rectifier diode and R_B is the burden resistance. If a voltage clamp circuit is not used, at TR1 turn-off a sinusoidal half-wave oscillation occurs as shown in Figures 2.7 and 2.9. In the conventional diode rectifier and load resistance circuit shown in Figure 2.1(a) the peak secondary voltage ($v_2(pk)$) appearing at CT reset is given by Equation (2.26) which is repeated here:

$$v_2(pk) = -\frac{\delta T}{\sqrt{L_{m2}C_{eq}}}\left[V_f + \frac{I_p}{n}(R_2 + R_B)\right] \tag{6.1}$$

It can be seen that $v_2(pk)$ is dependent on the magnetising current and the consequent core flux at switch turn-off.

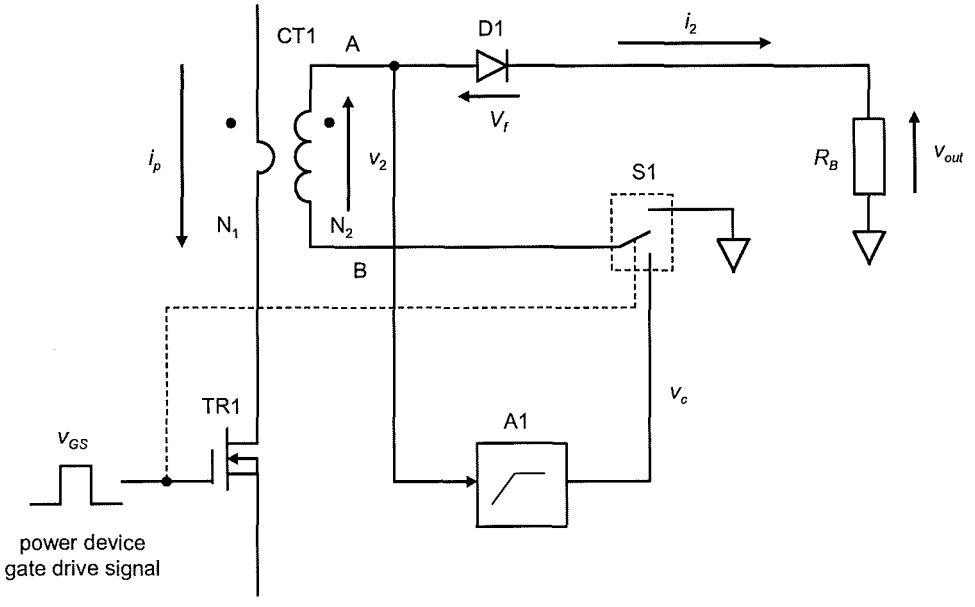


Figure 6.3. Functional Block Diagram of Reset Voltage Feedback Scheme

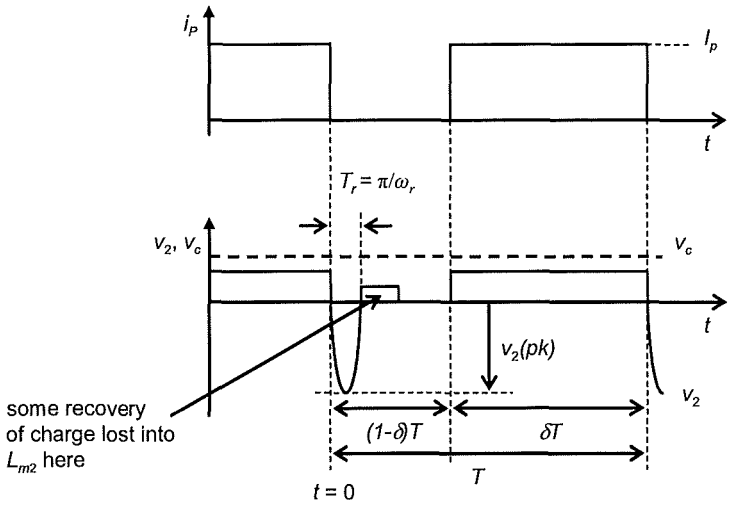


Figure 6.4. Idealized Waveforms Showing Operation of Reset Voltage Feedback Scheme

This effect is exploited here to minimise droop. The switch shown in Figure 6.3 (S1) is controlled by the same signal driving TR1. During TR1's off period end "B" of N_2 is connected to the zero voltage rail. During TR1's on-period end "B" of N_2 is connected to the output of the amplifier A1.

At TR1 turn-off the negative-going reset voltage is applied to A1 (which is an inverting amplifier) and low-pass filtered to give a voltage, v_c.

If the loading effect of the amplifier is negligible, then the voltage v_2 at the amplifier's input over the period from $t = 0$ to $t = \pi/\omega_r$ is given by:

$$v_2(t) = -\frac{\delta T}{\sqrt{L_{m2}C_{eq}}}\left[V_f + \frac{I_p}{n}(R_2 + R_B)\right]\sin(\omega_r t)\Big|_{0 \le t \le \frac{\pi}{\omega_r}} \qquad (6.2)$$

where ω_r is the resonant frequency of the circuit formed by L_{m2} and C_{eq}. As the voltage seen by A1 is approximately zero for the rest of the switching cycle then the average voltage is given by:

$$v_2(ave) = -\frac{1}{T}\int_0^{\frac{\pi}{\omega_r}} \frac{\delta T}{\sqrt{L_{m2}C_{eq}}}\left[V_f + \frac{I_p}{n}(R_2 + R_B)\right]\sin(\omega_r t)dt \tag{6.3}$$

This integrates to give:

$$v_2(ave) = -2\delta\left[V_f + \frac{I_p}{n}(R_2 + R_B)\right] \tag{6.4}$$

Alternatively, this result may be deduced from the observation that, as the current is returned to zero halfway through the reset half-oscillation, then the average reset voltage must be twice the average voltage applied across the CT's magnetizing branch during T_{on}. Due to the inversion introduced by A1, when the power device is next turned on and v_c is applied to end "B" of N_2, the polarity of v_c is such that it opposes the voltage impressed across L_{m2} by the sum of the voltage drops across R_B, D1 and R_2. v_2 is therefore now given by:

$$v_2 = V_f + i_2 R_B - v_c \tag{6.5}$$

However, v_2 is the CT's terminal voltage and the voltage across L_{m2} (v_{m2}) is given by:

$$v_{m2} = V_f + i_2(R_B + R_2) - v_c \tag{6.6}$$

The magnetizing current drawn by L_{m2} is therefore reduced. Again, if the loading effect presented by A1 is negligible, the peak reset voltage is now given by:

$$v_2(pk) = -\frac{\delta T}{\sqrt{L_{m2}C_{eq}}}\left[V_f + \frac{I_p}{n}(R_2 + R_B) - v_c\right] \tag{6.7}$$

and the average reset voltage is now given by:

$$v_2(ave) = -2\delta\left[V_f + \frac{I_p}{n}(R_2 + R_B) - v_c\right] \tag{6.8}$$

v_c is given by:

$$v_c = k_A(s)v_2(ave) \tag{6.9}$$

where $k_A(s)$ is the gain of A1 which only acts on the negative-going part of the input signal.

The greater the average reset voltage occurring, the greater is the correcting voltage (v_c) applied to the loop encircling L_{m2}.

Unlike the technique in [29], the voltage across L_{m2} is not controlled instantaneously in response to the rate of change of core flux but is based on the magnitude of the magnetizing current indirectly detected at the end of previous current pulses. Disadvantages with this technique are that abrupt deviations in current magnitude between successive current pulses are not readily catered for and that the correction voltage is a fixed magnitude which cannot change to account for changes in current magnitude during the pulse. Also, long "one-off" pulses cannot be catered for. However, in many switched mode applications abrupt changes in current magnitude do not present a difficulty as soft starting is incorporated into the control circuit thereby limiting the rates of change. Also, changes during steady-state operation are typically small.

The principle advantage with this technique compared with that in [29] is that the CT does not have to carry an auxiliary winding. All of the correction circuitry may be incorporated within TR1's control circuitry as the only control signal required is that used to drive the power device. The technique is therefore more cost-effective for switched mode power converter applications.

6.3 Implementation of Circuit and Experimental Results

6.3.1 Implementation

The circuit in Figure 6.5 was used to evaluate the technique. The power device (TR1) is operated in the same boost converter circuit shown in Figure 3.10 where TR1 is a MOSFET and the power diode is a Schottky type. The permutation of input voltage, output voltage and choke inductance is such that the ripple component of the current is less than 1 % and the current pulses conducted by TR1 are therefore regarded as rectangular. U2 is a Texas Instruments TS5A3159 analogue switch, as described in [75], and is used to realise the function of S1 in Figure 6.3. D3 is included to prevent the operational amplifier (U1) applying an out-of-specification negative voltage to U2 when the current in CT1 is zero or so low that the error voltage does not overcome any offset terms present.

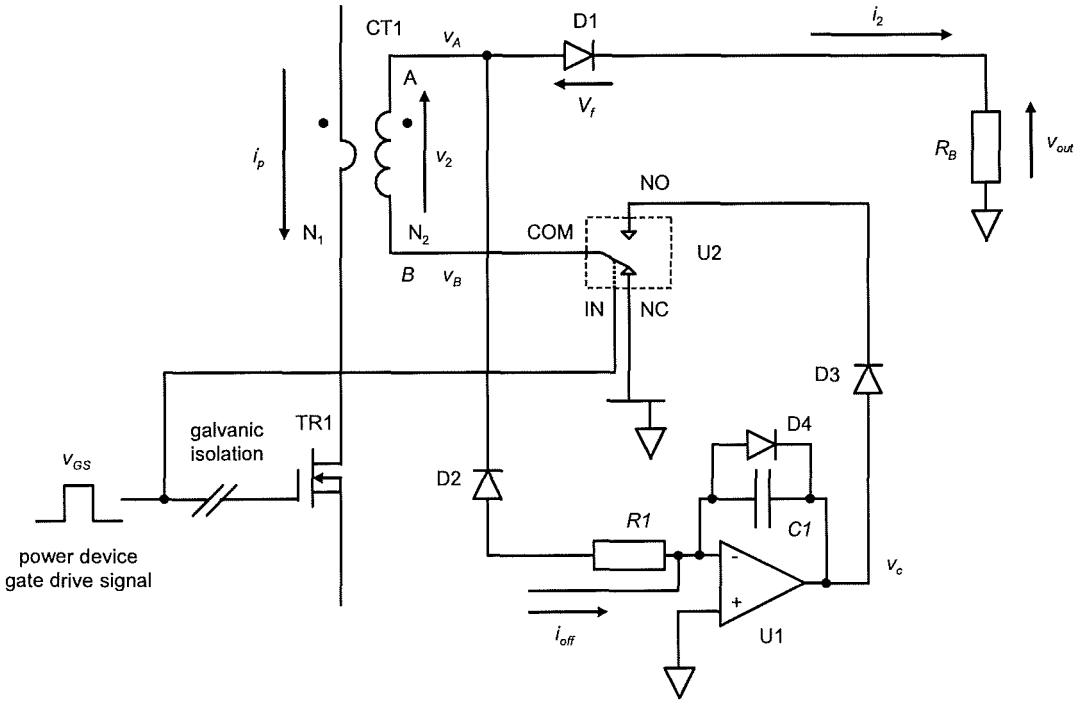


Figure 6.5. Implementation of Reset Voltage Feedback Scheme

D4 prevents the operational amplifier's output from saturating at the negative rail in the quiescent state, yielding a faster response when current pulses are applied. (D3 is still included as the forward voltage drop of D4 exceeds the maximum allowable negative voltage at the input to U2.)

The CT used is the variant in 3F3 core material described in Table 3.2 to enable direct comparisons to be made with the circuit with diode rectification and an active load. R_B is 12 Ω giving an expected gain of 100 mV/A. The TS5A3159 device has a maximum supply voltage of 5 V and the circuit's supply voltage was set at ± 5 V to allow U1 to be supplied from the same positive supply voltage rail. The principal component data are listed in Table 6.1. The gain of U1 is integral here. This control method has the advantage that, for a low-frequency error term, the steady-state error is virtually eliminated.

R1 was set at 100 kΩ so that the damping effect on the RLC circuit it forms with L_{m2} and C_{eq} is minimized. That is, the loading effect of the amplifier can be taken as very small. This was verified by running the circuit open-loop with *R1* in and then out of circuit. With *R1* out of circuit the resonant frequency of the reset transient voltage is measured at 365 kHz with a peak value of -37.2 V. With *R1* in circuit these values are measured at 343 kHz and -32.5 V respectively. Minimizing the damping effect and consequent reduction in the resonant frequency is desirable as the increase in the reset time is in turn minimized. Although a second operational amplifier may be used to buffer v_2, a difficulty is that the signal applied would have to be attenuated or clamped to prevent over-voltages at its input terminals. The arrangement here is therefore implemented for simplicity.

R1	100 kΩ
C1	1.0 nF
D2,3,4	1N4148
U1	NE5534A
U2	TS5A3159

Table 6.1. Component Data

It is noted that, in a practical scheme where integral control is used, some offset input current (shown as i_{off} in Figure 6.5) is necessary at the operational amplifier's inverting terminal to allow for its worst-case input offset voltage. This is needed because, if a positive offset voltage is present between the operational amplifier's input terminals, saturation of the feedback loop will be present at start-up. This results in U1's output voltage saturating at the positive supply rail voltage in the quiescent state ($\delta I_p \approx 0$) and sourcing an excessive current through the loop formed by U2, N2, D1 and R_B.

The galvanic isolation circuit shown in Figure 6.5 is that shown in Figure 3.11 with one change made. R_G is now 100 Ω instead of 10 Ω. This resistance was made larger as the interference resulting from transient effects at TR1 turn-off was otherwise found to affect correct operation of the integrator.

An analogue switch is used here, although an alternative circuit realisation using a discrete MOSFET is described in Appendix 4. With the exception of U2, leaded through-hole components are used in the circuit in Figure 6.5. However, a photograph of the circuit assembled in surface mount technology throughout is shown in Appendix 5.

6.3.2 Exemplifying Circuit Waveforms

Exemplifying circuit waveforms are shown in this section. Figure 6.6 shows oscillograms of i_p, v_{out} and v_A where the circuitry in Figure 6.5 is omitted and i_p is sensed using the conventional rectifier diode and load resistor arrangement as shown in Figure 2.1(a). The power device switching frequency is 20 kHz and the primary current is 5 A at a duty factor of 50 %. i_p is sensed for reference purposes using a high-bandwidth (50 MHz) dc current probe. As is the case with the measurements in Chapter 3, during the pulse off-time some recovery of the current-time product lost to droop during the on-time can be seen in the trace of v_{out} after the half-sinusoidal resonant resetting period has elapsed.

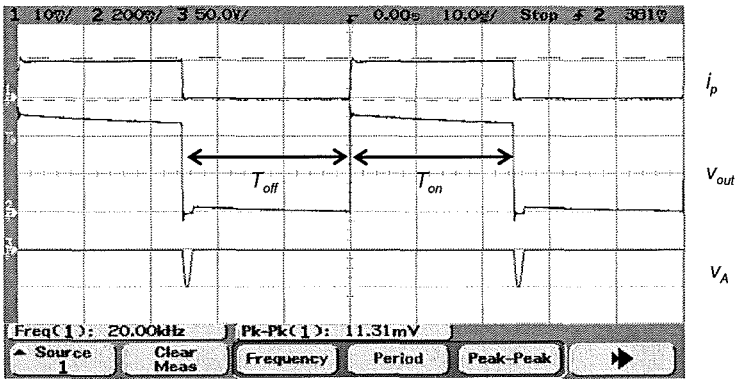


Figure 6.6. i_p, v_{out} and v_A in Conventional Arrangement (i_p = 5 A/div, v_{out} = 100 mV/div, v_A = 50 V/div, Time Scale: 10 μs/div)

The modified scheme shown in Figure 6.5 is now introduced. Figure 6.7 shows the oscillograms. It can be seen that both the peak current droop and the peak reset voltage are reduced. (Note that different scaling by a factor of 5 is used for v_A in Figures 6.6 and 6.7.) As expected, during the pulse off-time the current-time product returned to v_{out} is less due to the smaller current now forced into L_{m2}. Although the duty factor is 50 %, operation is well within the DMCM mode here. The reset voltage transient is not entirely eliminated due to the offset current supplied to the operational amplifier.

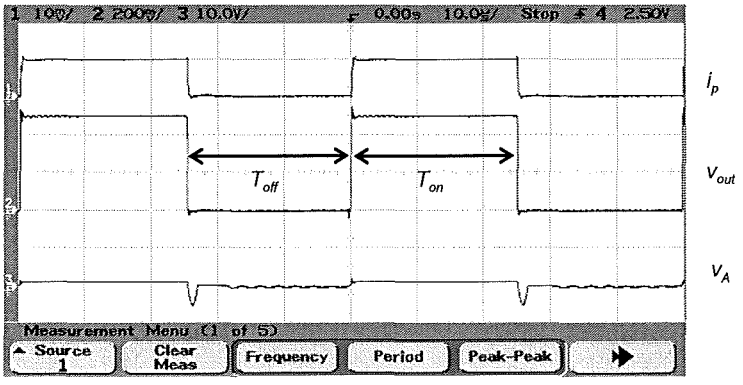


Figure 6.7. i_p, v_{out} and v_A in Modified Arrangement with Integral Feedback (i_p = 5 A/div, v_{out} =100 mV/div, v_A = 10 V/div, Time Scale: 10 μs/div)

Peak current droop is measured at 8.5 % using the conventional arrangement and is found to be negligible using the modified arrangement from the respective waveform data collected in Figures 6.6 and 6.7. (However, up to 1 % rise in the applied current pulse is allowed so some droop may be present.) The former figure of 8.5 % is in approximate agreement with the calculated peak current droop of 6.8 % which is given by:

$$D = \frac{I_{m2(0)}}{i_2} \tag{6.10}$$

where $I_{m2(0)}$ is given by Equation (2.8) and i_2 is the ideal secondary current. V_f is taken as 0.8 V and L_{m2} and R_2 are the values given in Table 3.2. Putting these values into Equation (2.8) and then putting this result into Equation (6.10) gives a droop of 7.8 %.

Figure 6.8 shows the principle waveforms from the circuit in Figure 6.5, including that of v_B.

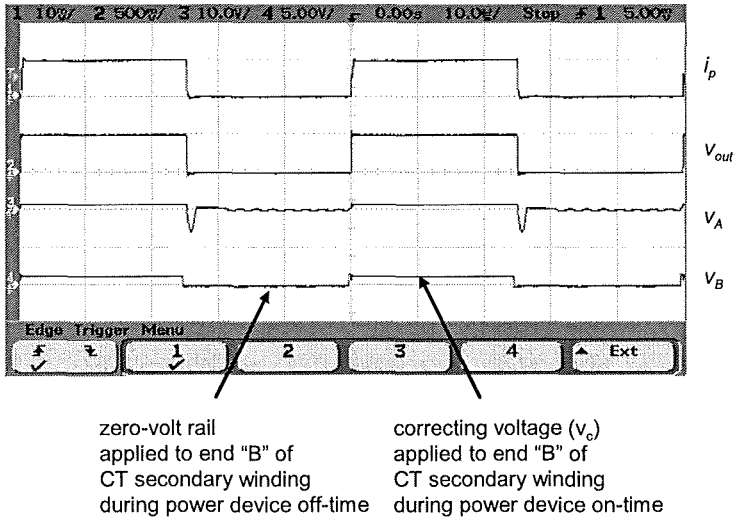


Figure 6.8. Principle Waveforms from Modified Arrangement with Integral Feedback (i_p = 5 A/div, v_{out} = 500 mV/div, v_A = 10 V/div, v_B = 5 V/div, Time Scale: 10 μs/div)

6.3.3 Comparison of Average Current Droop with Conventional Diode Rectifier and Load Resistor Circuit

Figure 6.9 shows the average current droop plotted against duty factor measured using the 12 Ω load resistor connected in the normal way (as shown in Figure 2.1a) and also the droop from the modified circuit with solely integral control implemented. The output voltage across R_B is low-pass filtered using the same RC circuit used in previous chapters where R = 10 kΩ and C = 3.3 nF, giving a corner frequency of 4.8 kHz. Some observations are made. Average current droop is very low over the entire duty factor range with the modified scheme introduced. Also, with the conventional scheme, the piecewise correction algorithm described in Chapter 3 is not so applicable here. This is expected, as the load here is a combination of a voltage sink (the rectifier diode) and resistance (the load resistor), whereas in Chapter 3, the load is more readily represented as a zero-impedance voltage sink.

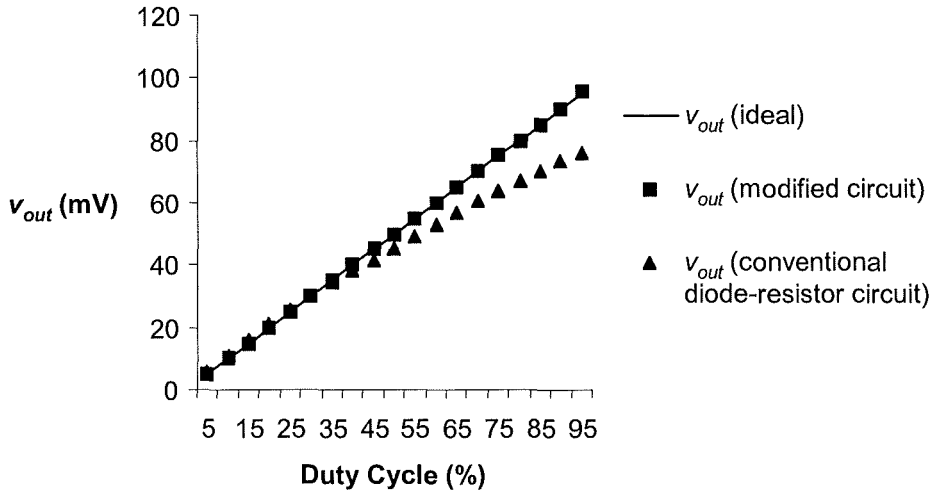


Figure 6.9. Average Output Voltage against Duty Factor with Conventional Diode and Load Resistor Arrangement and with CT Circuit Incorporating Reset Voltage Feedback (i_{L1} = 1 A)

6.3.4 Operation at Low Primary Currents

The discontinuous secondary current mode (DSCM) is described in Chapter 3 where the CT is operated with diode rectification and an active load. Figure 3.30 shows the boundary combination of primary current and duty factor at which this condition and the consequent exacerbated distortion occur with experimental readings superimposed.

The circuit in Figure 6.5 was tested at the same primary currents of 100 mA, 300 mA and 500 mA shown in Figure 3.30. A potentiometer was adjusted to set i_{off} such that the offset error developed by the operational amplifier resulted in v_2(pk) being set at approximately -2 V. The same CT was used for consistency and the results are shown in Figure 6.10.

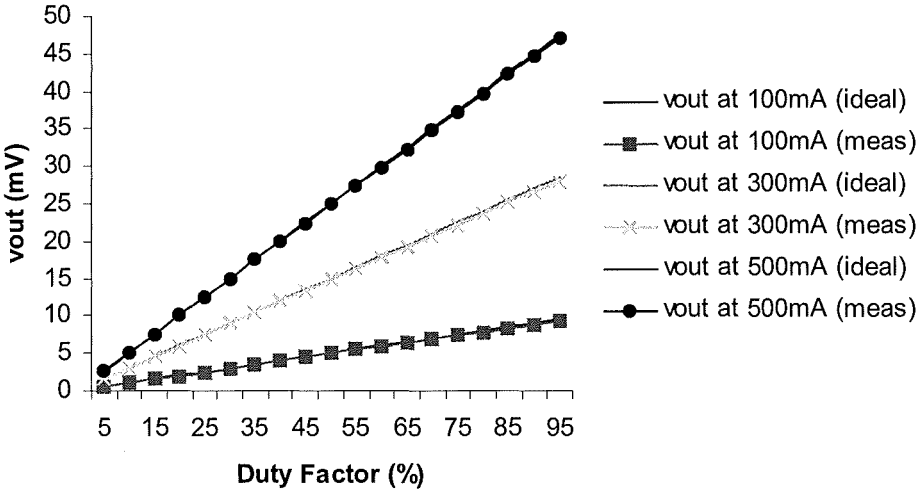


Figure 6.10. Average Output Voltage against Duty Factor Obtained from CT Circuit Incorporating Reset Voltage Feedback at Low Primary Currents

Again, it can be seen that the steady-state error in the current sensed is virtually eliminated, as is the problem of operation in the DSCM mode.

6.4 Circuit Simulation

The circuit may be treated as continuous by averaging quantities over a switching cycle. This approach is shown in block diagram form in Figure 6.11, where it is assumed that the circuit's time constants are large compared to the period of the waveform being measured.

However, where the bandwidth of A1 is high compared to that of the switching frequency, the circuit in Figure 6.11 is no longer adequate. Therefore, to more fully investigate the instantaneous behaviour of the circuit, in particular, cycle-by-cycle variations, a simulation model was prepared for the circuit in Figure 6.5 using Simulink [76]. This is shown in Figure 6.12.

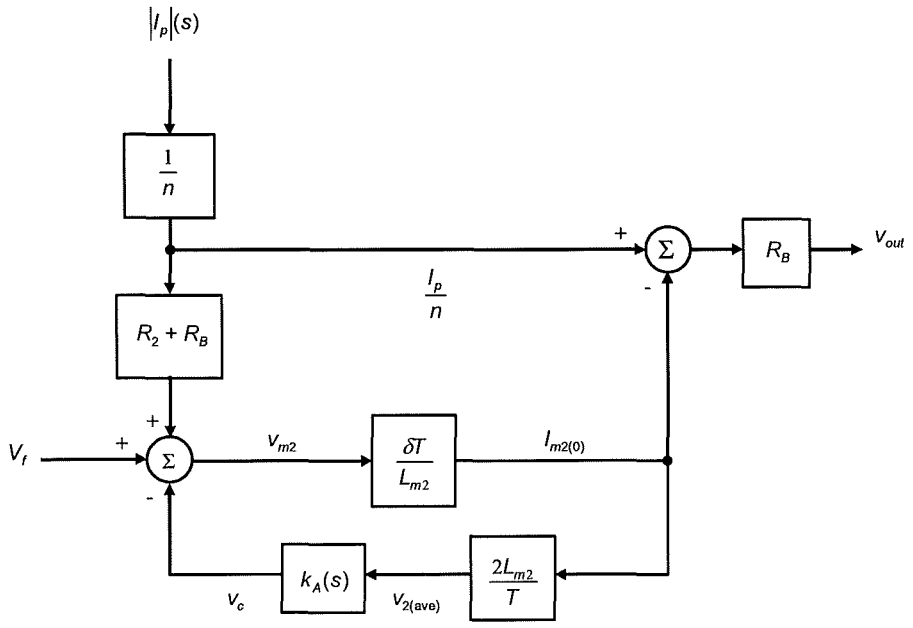


Figure 6.11. Block Diagram Showing Continuous Approximation of Circuit Operation when Sensing Rectangular Current Pulses

In Figure 6.12, switches 1 and 2 respectively emulate the effect of the application and removal of the primary current pulse. When the current pulse is present, the voltage given by Equation (6.6) is applied to the CT's magnetizing branch (L_{m2}) by "switch 1". When the current pulse is removed, the resonant circuit formed by C_{eq} is connected by "switch 2". "integrator 3" and "Fcn" represent the integral feedback gain (k_A(s)) realized by U1 in Figure 6.5. The "offset" input is included to assess the effects of worst-case offset terms and an output saturation limit is imposed to represent the finite rail voltage available.

"integrator 1" and "integrator 2" are both reset at the application of the pulse and at the completion of the half resonant resetting cycle. That is, i_{m2} and v_2 in the resonant circuit formed by L_{m2} and C_{eq} are both forced to zero at these instants.

The experimental conditions were replicated and the data in Table 3.2 were used in the simulation. VD1 is the forward voltage drop of the rectifier diode (D1 in Figure 6.5) and VD3 is the voltage drop of the blocking diode (D3 in Figure 6.5). Both VD1 and VD3 are entered as 0.8 V, the value measured at 40 mA. The forward voltage drop of D2 is neglected.

L_{m2} is not entered directly but is calculated (in block "f(u)") from the core dimensions and material characteristics so the effects of varying these parameters may be readily assessed. C_{eq} is entered as 17 pF, the value calculated from the measured unloaded resonant frequency of 365 kHz and the measured value of L_{m2} in Table 3.2.

The droop when feeding a resistive load via a rectifier diode has both linear and exponential components and these are accounted for as such in the simulation. However, it is noted in Chapter 2 that the exponential component may be treated as linear if T_{on} is much shorter than τ and this accuracy is not expected to be strictly necessary.

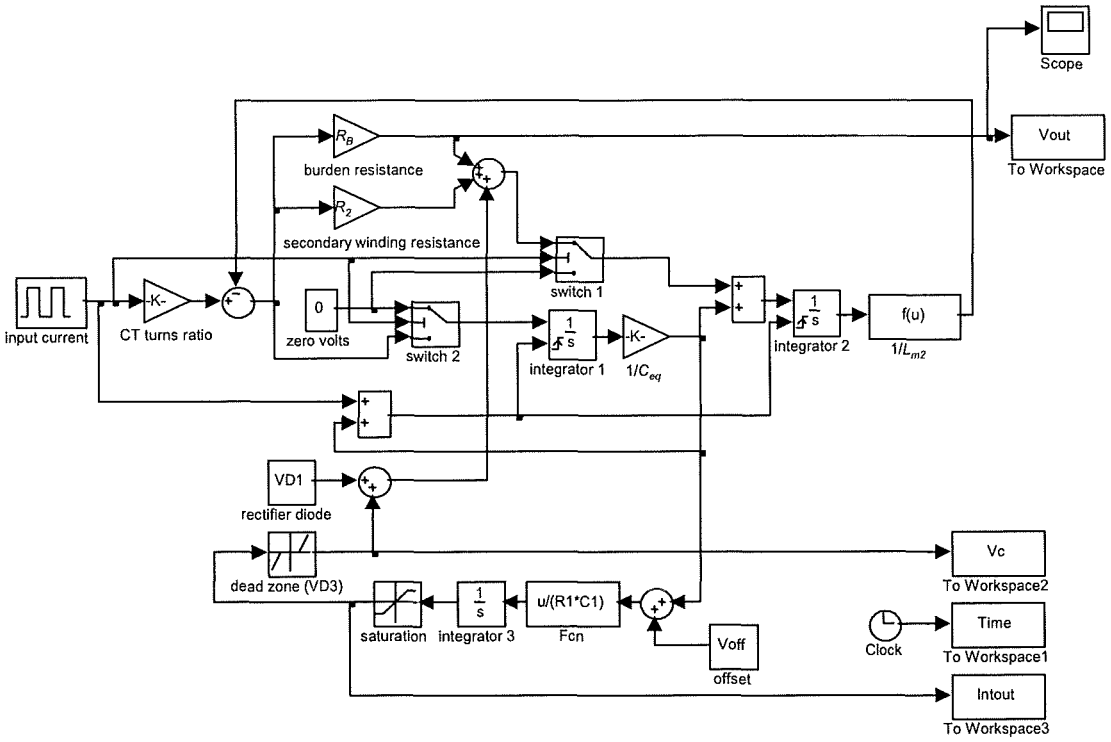


Figure 6.12. Simulink Model of CT Circuit with Reset Voltage Feedback

Figure 6.13 shows the simulated steady-state output voltage for I_p = 5 A at a duty factor of 50 % with the correction circuitry omitted. Droop is measured at 7.2 %, in approximate agreement with that measured in Figure 6.6 and calculated in Section 6.3.2.

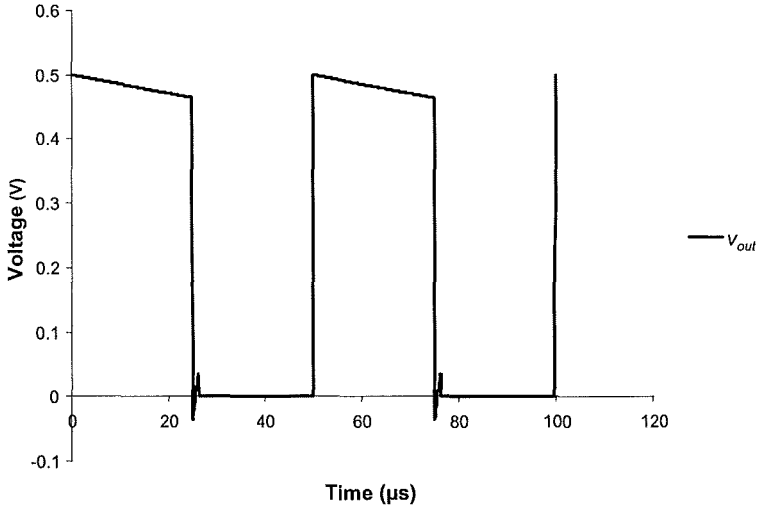


Figure 6.13. Steady-State Output Voltage Modelled in Simulink with Correction Circuitry Omitted (I_p = 5 A, δ = 50 %)

Figure 6.14 shows the simulated steady-state output voltage with the correction circuitry included. Droop is measured at virtually zero, in agreement with that measured in Figure 6.7.

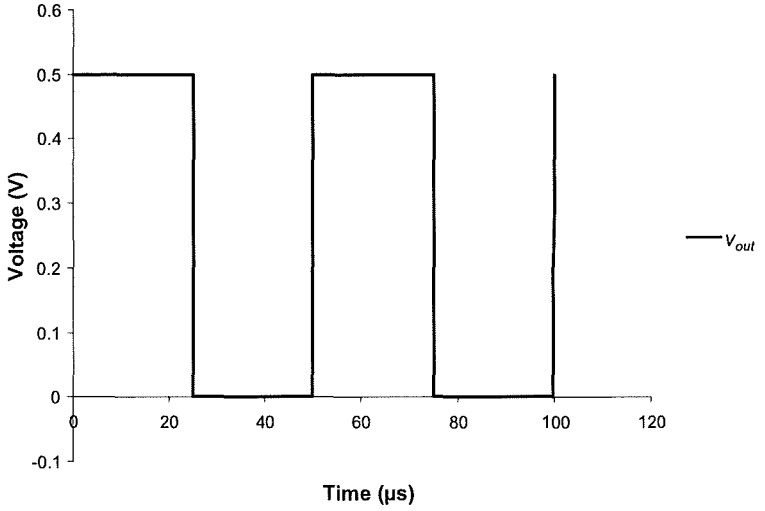


Figure 6.14. Steady-State Output Voltage Modelled in Simulink with Correction Circuitry Incorporated (I_p = 5 A, δ = 50 %)

Figure 6.15 shows the modelled transient output voltage and correcting voltage (v_c) and integrator output voltage (Intout) in response to a step application of a rectangular current pulse train modelled with the correction circuitry incorporated. I_p is 5 A and δ is 50 %. Figure 6.16 shows the same simulation but with $\delta = 90$ %. Although positive in the circuits in Figures 6.3 and 6.5, v_c is shown as a negative-going quantity here as it opposes the other voltage drops impressed across L_{m2}. Also, the initial condition of the integrator is arbitrarily set at 1 V. From Figures 6.15 and 6.16, it can be seen that, the steady-state correcting voltage is independent of δ although with higher values of δ it is approached more rapidly.

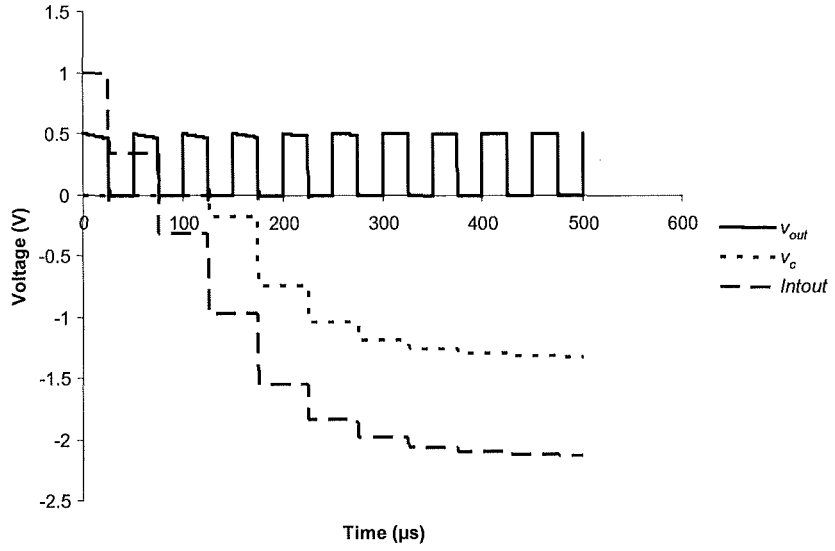


Figure 6.15. Modelled Transient Response to Step Application of Current Pulse Train with Correction Circuitry Incorporated (I_p = 5 A, δ= 50 %)

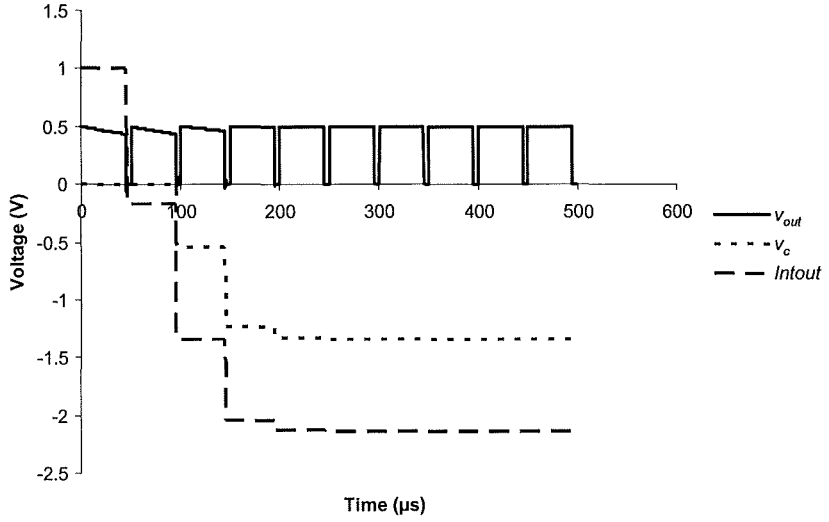


Figure 6.16. Modelled Transient Response to Step Application of Current Pulse Train with Correction Circuitry Incorporated (I_p = 5 A, δ= 90 %)

From Figures 6.15 and 6.16, it can be seen that, the steady-state correcting voltage is independent of δ although with higher values of δ it is approached more rapidly.

6.5 Performance with Non-Rectangular Current Pulses

6.5.1 Theory

So far, only rectangular current pulses have been addressed. However, in a practical power converter in the continuous conduction mode the waveform is more accurately treated as a ramp-on-a-step and in the discontinuous conduction mode the waveform becomes triangular. Where v_c is a steady value during a current pulse, an important difference between rectangular and non-rectangular cases is that, in the latter case, some flux excursion takes place during a current pulse in the steady-state. The circuit is represented in Figure 6.17 where R_T is the sum of R_2 and R_B. Two disadvantages are incurred with triangular waveforms. Firstly, the inaccuracy of the average current measurement increases. Negative droop is incurred: that is, v_{out} is an overestimate. Secondly, although not definable as peak current droop in the normal way defined in [25, 43, 44], the slope of the current waveform is reduced at the peak current value.

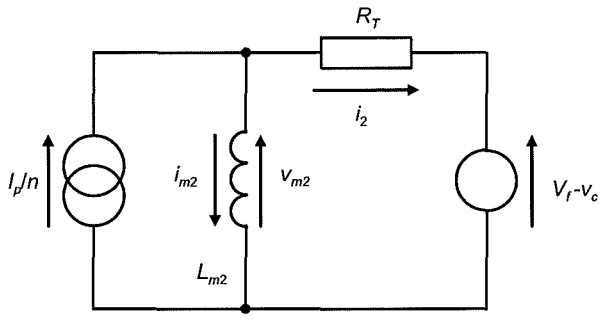


Figure 6.17. Equivalent Circuit for Evaluating Steady-state Performance with Non-Rectangular Current Pulses

With respect to Figure 6.17, for a triangular current waveform where $i_p/n = At$, then i_{m2} is given by:

$$i_{m2} = A\left[t - \tau\left(1 - e^{-t/\tau}\right)\right] - \frac{v_c - V_f}{R_T}\left(1 - e^{-t/\tau}\right) \tag{6.11}$$

If $i_{m2} = 0$ at the end of a pulse of duration δT then, by substituting these values into Equation (6.11) and rearranging, v_c is given by:

$$v_c = R_T A\left(\frac{\delta T}{1 - e^{-\delta T/\tau}} - \tau\right) + V_f \tag{6.12}$$

Substituting this result back into Equation (6.11) gives:

$$i_{m2} = At - A\delta T\frac{\left(1 - e^{-t/\tau}\right)}{\left(1 - e^{-\delta T/\tau}\right)} \tag{6.13}$$

This is integrated over the interval from $t = 0$ to $t = \delta T$ to yield the magnetizing charge drawn during a switching cycle:

$$\int_0^{t_p} i_{m2}\,dt = \frac{A\delta^2 T^2}{2} - A\delta T\left(\frac{\delta T + \tau e^{-\delta T/\tau} + \tau}{1 - e^{-\delta T/\tau}}\right) \tag{6.14}$$

The average magnetizing current drawn may be obtained by dividing this result by the waveform's period:

$$i_{m2(ave)} = \frac{A\delta^2 T}{2} - A\delta\left(\frac{\delta T + \tau e^{-\delta T/\tau} + \tau}{1 - e^{-\delta T/\tau}}\right) \tag{6.15}$$

The instantaneous value of v_{out} during T_{on}, may be calculated from:

$$v_{out} = R_B\left(\frac{i_p}{n} - i_{m2}\right) \tag{6.16}$$

where i_{m2} for a triangular waveform is given by Equation (6.13).

6.5.2 Experimental Readings with Triangular Current Waveform

Figure 6.18 shows waveforms from the conventional diode-resistor circuit in Figure 2.1 (that is, without reset voltage feedback) when sensing a triangular current waveform of 5 A peak value at 50 % duty factor. As with the result shown in Figure 6.6, significant charge recovery takes place after the interval T_r has elapsed.

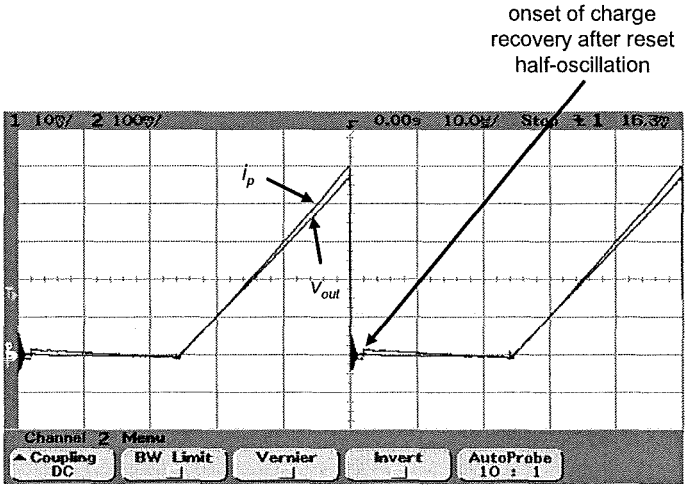


Figure 6.18. i_p and v_{out} in Conventional Arrangement when Sensing Triangular Current Pulse at 20 kHz (i_p = 1 A/div, v_{out} = 100 mV/div, Time Scale: 10 μs/div)

Figure 6.19 shows waveforms from the circuit in Figure 6.5 (with reset voltage feedback) when sensing a triangular current waveform of 5 A peak value at 50 % duty factor.

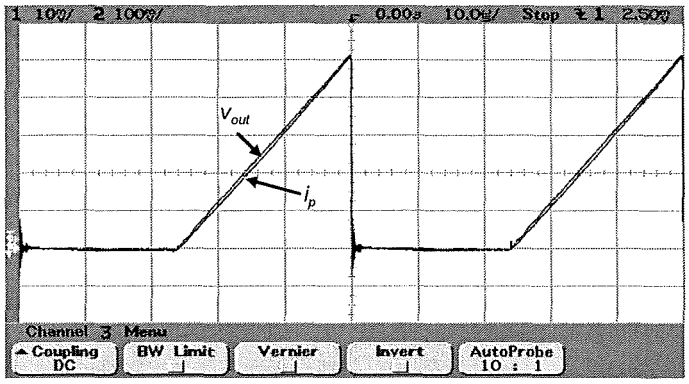


Figure 6.19. i_p and v_{out} in Modified Arrangement with Integral Feedback when Sensing Triangular Current Pulse at 20 kHz (i_p = 1 A/div, v_{out} = 100 mV/div, Time Scale: 10 µs/div)

Some divergence between i_p and v_{out} is seen in Figure 6.19. Figure 6.20 shows i_p and v_{out} with the switching frequency now reduced to 4 kHz and δ increased to 75 % to accentuate the expected distortion for comparison with that predicted using Equation (6.16).

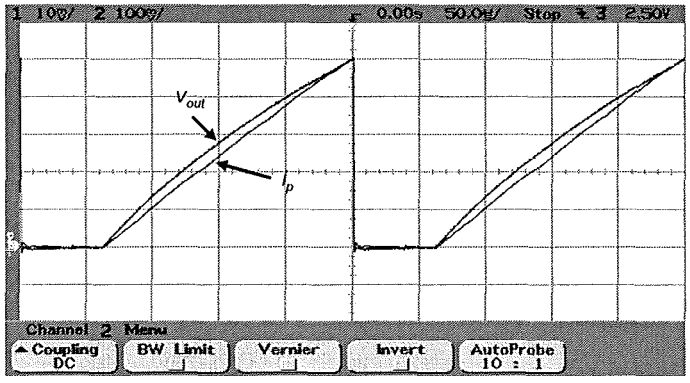


Figure 6.20. i_p and v_{out} in Modified Arrangement with Integral Feedback when Sensing Triangular Current Pulse at 4 kHz and δ = 75 % (i_p = 1 A/div, v_{out} = 100 mV/div, Time Scale: 50 µs/div)

For comparison, Figure 6.21 shows the same traces as in Figure 6.20, but with the CT variant in 3E25 core material described in Table 3.2.

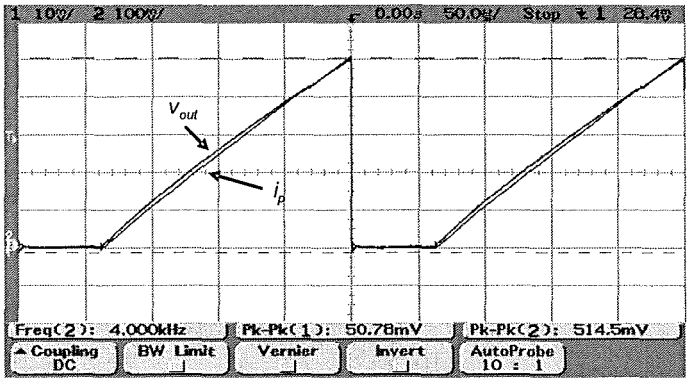


Figure 6.21. i_p and v_{out} in Modified Arrangement with Integral Feedback when Sensing Triangular Current Pulse at 4 kHz and δ = 75 %, 3E25 CT Core Material (i_p = 1 A/div, v_{out} = 100 mV/div, Time Scale: 50 μs/div)

6.5.3 Comparison with Theory

Figure 6.22 shows the data for v_{out} collected from Figure 6.20 with the calculated value using Equation (6.16) superimposed. In the calculation, L_{m2} = 11.0 mH, $R_T = R_B + R_2$ = 12.89 Ω and I_p/n = 1667 A/s.

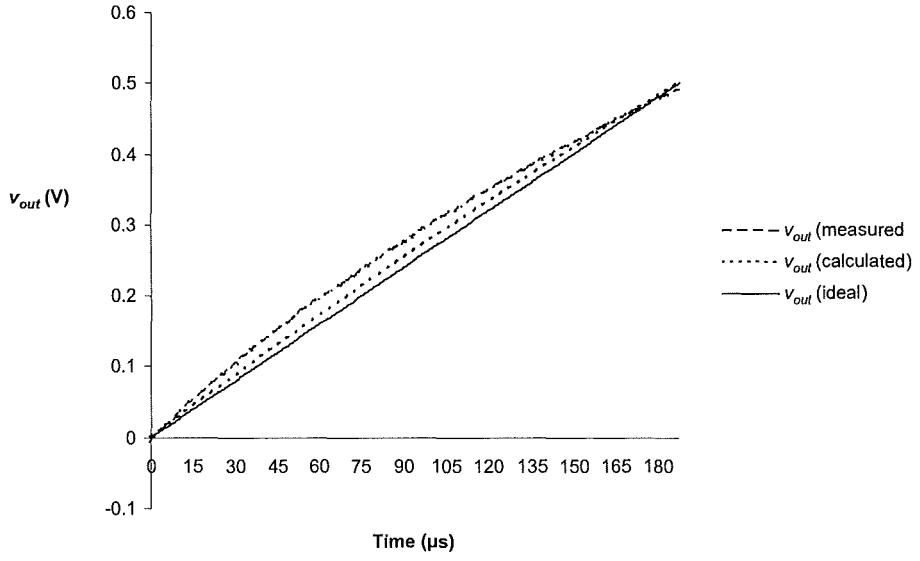


Figure 6.22. Measured and Calculated Readings with Triangular Current Pulse and 3F3 Core Material (I_p = 5 A, f = 4 kHz and δ = 75 %)

6.6 Discussion and Summary of Chapter

A technique has been described and demonstrated for reducing droop in the output signal from a UCPT. The CT's construction is not modified here. Instead, its secondary terminal voltage is adjusted during a current pulse in response to the resetting voltage sensed during previous switching cycles. Largely arbitrary component values have been used and the results have been compared with a circuit simulation with good agreement.

Unlike the scheme in Chapter 3, the peak current droop is largely eliminated here and this in turn implies a reduced D_{ave}.

Although it is shown in Chapter 3 that the operation of the CT is inherently resonant and a proportion of the current-time product lost due to peak current droop is returned, thereby alleviating D_{ave}, the CT's core losses and the ratio of V_{f1} to V_{f2} have to be known if high accuracy is to be attained. These issues are less problematic with reset voltage feedback. However, with this scheme, it is noted that where the peak current droop is not entirely eliminated, some recovery of the (now much smaller) current-time product lost during the current pulse still takes place, thus further minimizing D_{ave}. It is also noted that complete elimination of the peak current droop is not feasible due to the need to cater for worst-case offsets in the amplifier. However, the much smaller core flux swing also implies that the lossless approach may be more relevant in estimating D_{ave} and the offset term left in may be countered by the effective return of energy into the CT's output load.

Given that a minimum voltage drop is known to be incurred by the rectifier diode (at the very least, approximately 0.45 V where a Schottky diode is used), then this can be fed forward. However, feed-forward is omitted for simplicity here. It is, however, noted that, when detecting rectangular current pulses, the steady-state error due to droop is virtually eliminated using integral control without it being necessary to know the values of V_f or R_B.

When detecting triangular current pulses, complete elimination of average current droop is not achieved and worsening negative droop results as the circuit's time constant approaches the period of the switching waveform.

Several practical considerations are noted:

1. During the period when the integrator is measuring the CT's resetting voltage, a comparatively high level of ambient interference is also present in the circuit due to the transient effects of the power switch turning off. Two approaches may be taken to counter this. Firstly, the circuit's susceptibility to interference may be minimised by measures such as slowing down the rate at which power devices switch and implementing appropriate routing of conductors. Secondly, an offset term may be added to cancel the effect of any net dc voltage induced at the amplifier's input by the transient interference. (An offset term is required in any case to allow for the worst-case amplifier input offset voltage.)
2. The equivalent capacitance between the anode of the reverse voltage sense diode (D3 in Figure 6.5) and the zero voltage rail leads to some peak detector action taking place. Ideally the voltage at this point tracks the voltage, v_A, in Figure 6.6. However, it decays at a slightly slower rate due to this capacitance combining with *R1*. The volt-second product predicted in Equation (6.8) is therefore expected to be a slight underestimate.
3. A further practical consideration is found to be that timing skews between the current transitions in the CT and the control signal driving the analogue switch may exacerbate distortion when sensing current waveforms with ramp components.

CHAPTER 7

APPLICATION OF SWITCHED-MODE CIRCUITRY FOR SUPPLYING CORRECTING VOLTAGE TO THE UNIDIRECTIONAL CURRENT PULSE TRANSFORMER WITH RESET VOLTAGE FEEDBACK

7.1 Introduction

The droop reduction scheme described in Chapter 6 applies a correcting voltage to the CT's secondary terminals by dropping the supply voltage across a linear regulator. U1 performs this function in the circuit realised in Figure 6.5. The power dissipation, however, is not necessarily trivial. Considering the circuitry in Figure 6.5, the following permutation of parameters is taken as an example: V_{DD} (the supply voltage) = 12V, n = 120, I_p = 5A, δ = 95 % and v_{out}/i_p = 100 mV/A, implying that R_B is 12 Ω. At these conditions, and with V_f taken as 0.8 V, the power dissipated in the circuit is 475 mW of which 424 mW is lost in the linear regulator. Significant additional capacity is thus required from the control circuitry's power supply. Apart from the problem of providing the extra power drawn, cooling of the series regulator element has to be addressed, particularly if the circuit is to be integrated with existing control circuitry.

The CT may be wound with an increased number of secondary turns to reduce circuit losses by reducing the rail current drawn for a given primary current. However, this has the drawbacks described in Section 2.1.2: the frequency response of the CT is reduced due to the increased inter-winding capacitance introduced into its equivalent circuit and the required reset time is increased. A practical issue is that a high secondary turns number implies a low secondary conductor csa leading to termination difficulties. A large headroom voltage is desirable where the secondary voltage varies.

The feasibility of using switched-mode circuitry to reduce this power consumption is therefore investigated in this chapter.

7.2 Proposed Technique

Figure 7.1 outlines the proposed technique. During T_{off}, end "B" of N_2 on the CT is held at 0 V by S2 and, as described in Chapter 6, an error voltage is derived from the reset voltage by A1. During T_{on}, however, the error voltage is not simply directly applied to end "B" as before, thus making A1 act as a linear regulator. Instead, v_c is compared with a high-frequency reference waveform, v_{REF}, by a comparator, COMP1 to produce a PWM signal, v_{PWM}. An AND gate, U1, enables this signal to control S1 and S2 such that S1 acts as the power switch and S2 acts as the synchronous rectifier diode in a buck converter circuit. Ideally, the PWM frequency is high compared to that at which the main power device (TR1) operates so that it introduces a minimal ripple current onto the CT's output signal.

Normally the implementation of switched-mode circuitry is relatively expensive due to the need to include a passive component (a choke in the case of a voltage-sourced power converter). However, this is not problematic in the topology here as the CT's secondary inductance acts as the choke.

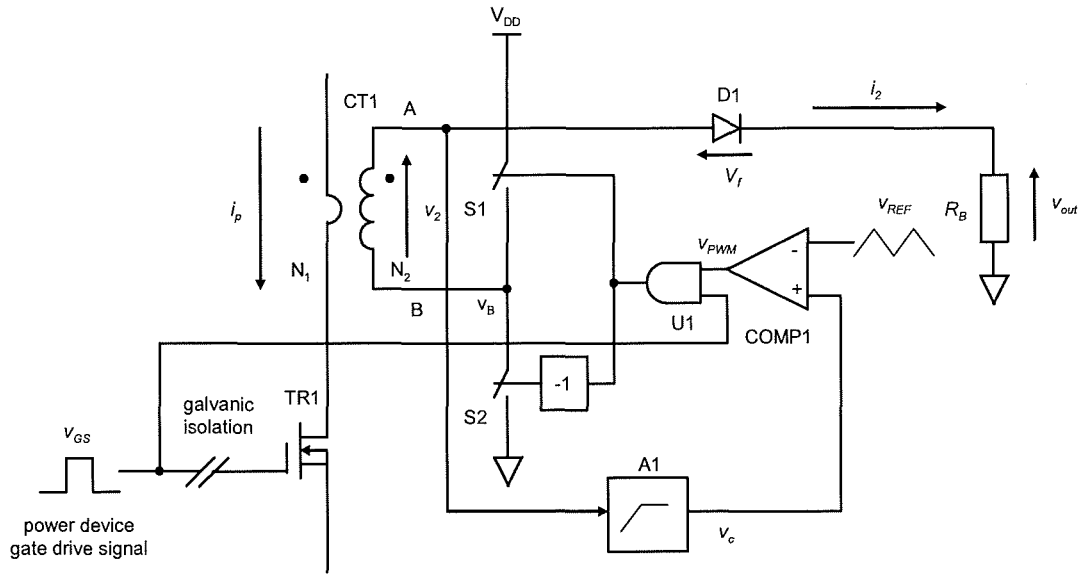


Figure 7.1. Outline of Proposed Switched-Mode Circuit for Applying Compensating Voltage to CT Secondary Winding

7.3 Implementation of Circuit and Experimental Results

7.3.1 Implementation

Figure 7.2 shows the experimental implementation of the circuit in Figure 7.1. 200 kHz was selected as the correcting PWM frequency. This is greater by a factor of 10 than the power converter switching frequency of 20 kHz. V_{REF} was a triangle wave set at 3 V peak-to-peak, with a 3 V positive offset voltage superimposed. An IR4427 gate driver IC (U2) was used to realise the functions of S1 and S2 in Figure 7.1. This is a dual-channel device that uses MOSFETs as the output transistors. Both channels are connected in parallel to minimise the resultant output resistance. The function of U1 in Figure 7.1 is realised using D3 (1N4148) to make a "wired-AND" connection between the output of COMP1 and the gate drive signal applied to TR1. The pull-up resistor, *R2*, is 2.2 kΩ to yield an acceptable rise-time. Unlike the circuit in Figure 6.5, the circuit here was designed to operate from a single rail supply voltage (V_{DD}), set at

12V here. A1 is an MC33171PG single-rail operational amplifier. However, the non-inverting terminal was held at approximately 0.8 V above the 0 V rail to avoid it attempting to operate with input voltages outside the supply rail voltages. Otherwise, details are the same as those for the circuit in Figure 6.5. That is, $R1$ = 100 kΩ, $C1$ = 1 nF, R_B = 12 Ω and D1 = D2 = 1N4148. CT1 is the device in 3F3 material specified in Table 3.1.

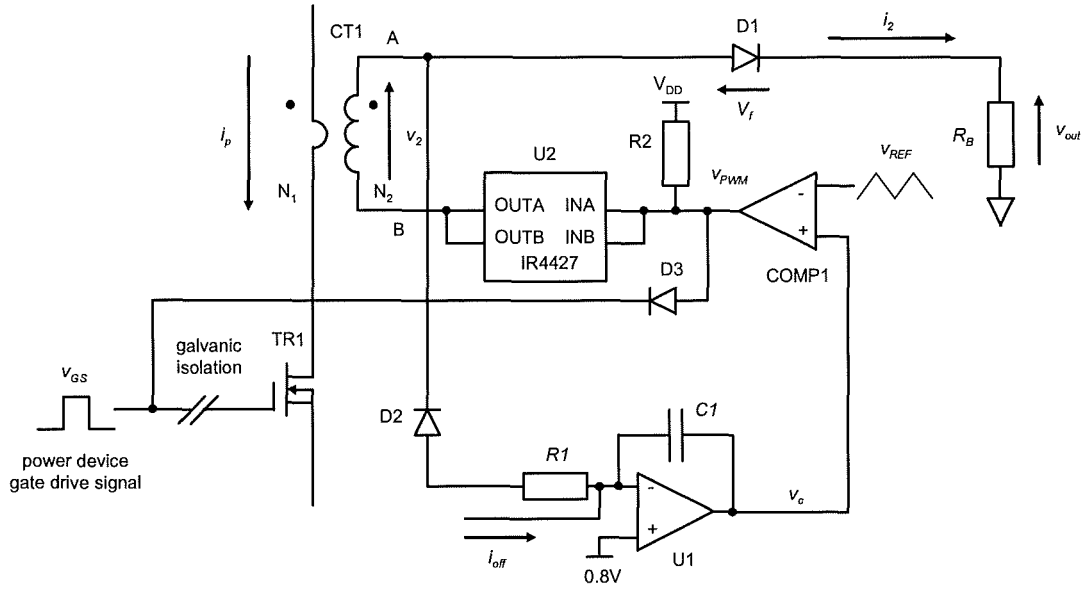


Figure 7.2. Implementation of Switched-Mode Circuit for Applying Compensating Voltage to CT Secondary Winding

Neglecting quiescent losses, the loss in the linear scheme is

$$W_T = \frac{\delta \times I_p V_{DD}}{n} \tag{7.1}$$

and losses in an ideal switched-mode scheme are:

$$W_T = \delta\left[\frac{I_p V_f}{n} + \left(\frac{I_p}{n}\right)^2 R_B\right] \tag{7.2}$$

However, a practical switched-mode scheme exhibits some losses. These include conduction and switching losses in the driver stage as well as quiescent losses.

7.3.2 Exemplifying Circuit Waveforms

Figure 7.3 shows exemplifying waveforms from the circuit in Figure 7.2 at I_p = 5 A and δ = 50 %. When compared with the waveforms from the uncompensated and linear schemes in Figures 6.6 and 6.7 respectively, it can be seen that droop is also reduced using the switched-mode arrangement. However, a ripple voltage is superimposed onto the signal ideally obtained. Transient voltages are also superimposed onto the ideal signal when the driver IC switches. This is shown in more detail in Figure 7.4. It is noted that the switching voltage transitions (dv/dts) produced by the driver IC are very rapid and that C_{eq} provides a route for the dv/dts applied at end "B" of N2 to inject currents through R_B.

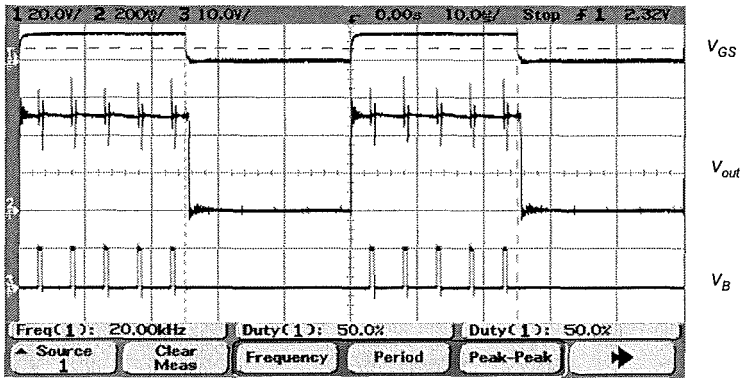


Figure 7.3. v_{GS}, v_{out} and v_A in Modified Arrangement with Integral Feedback and Switched-Mode Correction Stage (I_p = 5A, δ= 50%) (v_{GS} = 20V/div, v_{out} = 100 mV/div, v_B = 10 V/div, Time Scale: 10 µs/div)

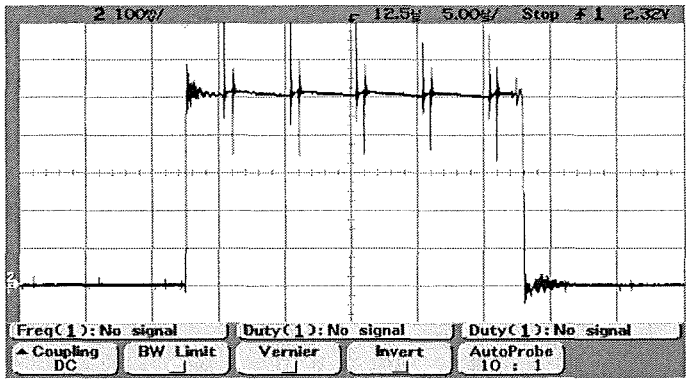


Figure 7.4. Detailed View of v_{out} (v_{out} = 100 mV/div, Time Scale: 5 µs/div)

7.3.3 Comparison of Average Current Droop with Conventional Diode and Burden Resistor Circuit

Figure 7.5 shows the sensed average current plotted against duty factor for I_{L1} = 1 A to allow a comparison with the results from the linear technique given in Figure 6.9. Again, the current sensed with the unassisted conventional diode and resistor arrangement is shown. Also as before, the output voltage is filtered using a low-pass RC circuit where R = 10 kΩ and C = 3.3 nF giving a corner frequency of 4.8 kHz.

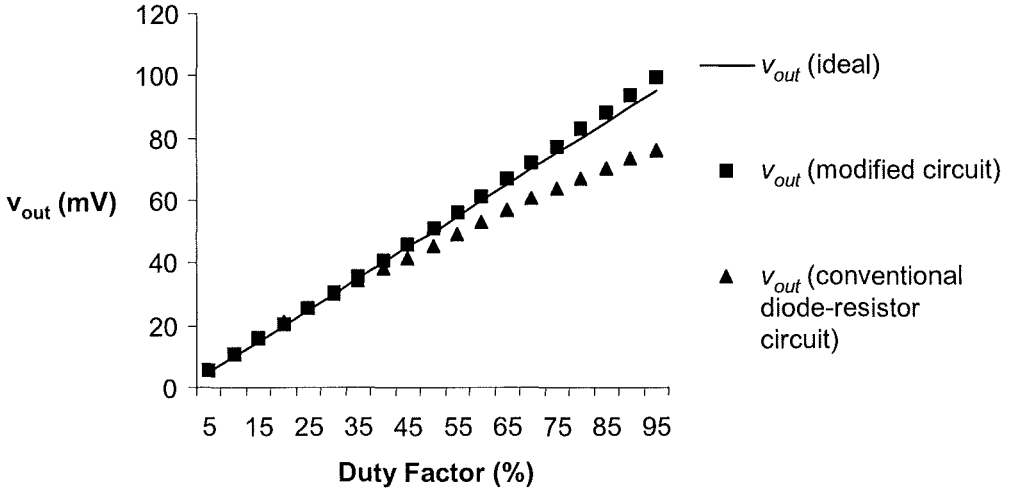


Figure 7.5. Average Output Voltage Plotted against Duty Factor with Switched-Mode Correction Stage (I_{L1} = 1 A)

7.3.4 Comparison of Measured Losses against Estimated Losses

The losses against duty factor for I_{L1} = 5 A are shown in Figure 7.6 and are inferred from the current drawn from the supply voltage rail. The losses calculated in Equations 7.1 and 7.2 for the linear and ideal switched-mode circuits respectively are also shown for comparison. No particular attempt has been made to minimize quiescent losses here and the loss exhibits the consequent fixed term seen. However, when this fixed term (137 mW) is subtracted from the power drawn when the circuit is active, it can be seen that the dynamic losses (that is, principally the switching losses in the IR4427 IC) are very low.

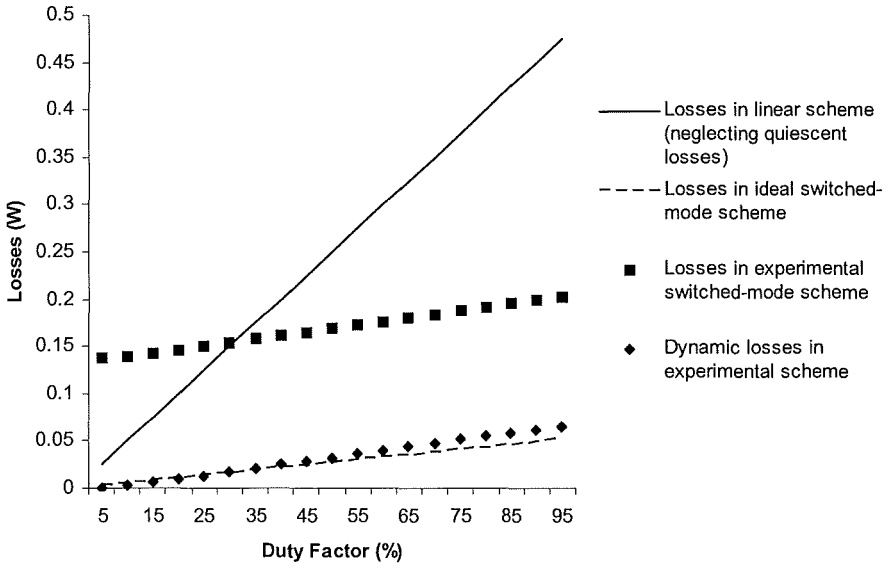


Figure 7.6. Comparison of Measured Losses in Ideal Switched-Mode (100% Efficient) Circuit and Linear Circuit Plotted against Duty Factor (I_{L1} = 5 A)

7.4 Circuit Simulation

The circuit was simulated using the Simulink simulation shown in Figure 7.7. A simulation is carried out again here to investigate the effect on the output voltage across V_B caused by applying a PWM signal to N2. "switch 3" represents the stage

formed by the IR4427 device and applies 0 V or 12 V to end "B" of CT1's secondary winding in response to the PWM signal produced by the comparator stage.

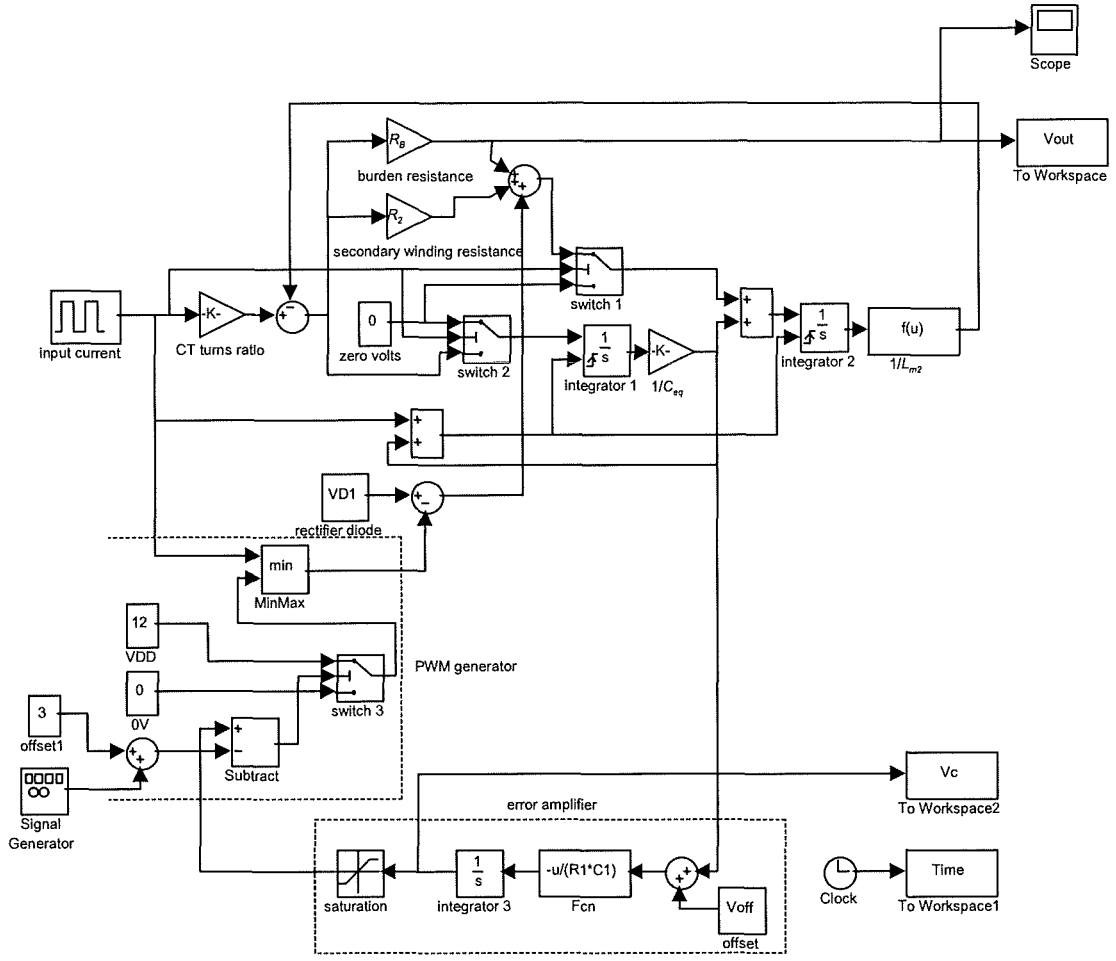


Figure 7.7. Simulink Model of CT Circuit with Switched-Mode Reset Voltage Feedback

Figure 7.8 shows the simulated steady-state output voltage with the correction circuitry included for comparison with the waveforms in Figures 7.3 and 7.4. Droop is measured at virtually zero. However, the ripple component introduced by the correction circuitry can be seen.

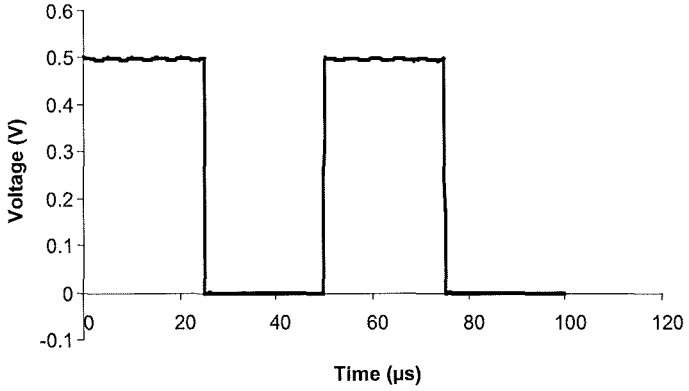


Figure 7.8. Steady-State Output Voltage Modelled in Simulink with Switched-Mode Correction Circuitry Incorporated (I_p = 5 A, δ= 50 %)

7.5 Discussion and Summary of Chapter

The feasibility of using a switched-mode stage to provide a compensating voltage has been demonstrated. Losses in the compensating circuit are reduced except at low duty factors where fixed losses dominate. However, a ripple voltage is superimposed onto the signal under measurement. Although, as in any switched-mode scheme, the ripple current may be minimised by operating at a higher PWM frequency, transient voltages are introduced by the switching action of the PWM controller. Apart from the effect on the waveform being measured, another potential source of unwanted EMI is introduced.

CHAPTER 8

CONCLUSIONS

8.1 Principal Findings

8.1.1 Diode Rectification

Operation of the current pulse transformer with diode rectification, an active load realized using an inverting operational amplifier circuit and natural resetting has been investigated. Compared to synchronous rectification, both average and peak current droop are relatively high. Three modes of operation have been identified and described. These are the discontinuous magnetizing current, continuous magnetizing current and discontinuous secondary current modes. It is found that, at relatively high core flux excursions, the error in the average output signal obtained is predominantly defined by the core losses in the CT. A simple piecewise correction algorithm which is a function of duty factor is shown to be appropriate for correcting the error due to droop provided that the discontinuous secondary current mode is avoided. A further enhancement is introduced using a square-law and ramp-on-a-step algorithm which provides good accuracy.

The dual CT circuit with DR and an active load is also investigated. It is found that a simpler correction algorithm based on the addition of a fixed offset term irrespective of duty factor may be appropriate. It is found that slope compensation may be complicated in this circuit.

Although the influence of core losses is described, three difficulties to the successful implementation of the correction schemes based on compensation for core losses are identified.

Firstly, data on ferrite losses at low levels of flux density excursion are not readily available. In any case, this data is subject to wide tolerances.

Secondly, the core losses exhibit a significant temperature coefficient. Whereas the first difficulty may be addressed by means of a trimming or "set-on-test" operation, this latter problem is more difficult to address. Although the ambient temperature or that of the CT itself could be sensed, and compensation adjusted in response, this would tend to negate two of the CT's principal advantages, its simplicity and low cost. Nonetheless, the worst-case distortion from a CT may be estimated by accounting for the worst-case combination of core losses and ambient temperature.

Thirdly, if the positive and negative-going slew rates of the operational amplifier are mis-matched, then average current droop is affected, particularly at low duty factors and high frequencies.

8.1.2 Synchronous Rectification

Resonant operating modes of the current pulse transformer when used with synchronous rectification and an active load realized using an operational amplifier are investigated.

8.1.2.1 Synchronous Rectification with Discrete MOSFET

The practical issue of driving the SR MOSFET's gate terminal is addressed as it is found that this is non-trivial if distortion is to be minimized. Compared to diode rectification, both the average and peak current droop are relatively low. However, the theoretically anticipated improvement is not attained. Sources of inaccuracy identified are attributable to the gate charging current being injected into the operational amplifier's input node and the interaction ("ringing") of the MOSFET's inter-terminal capacitances with the CT's magnetizing inductance.

8.1.2.2 Synchronous Rectification with Analogue Switch

Improved results were obtained using a commercially available analogue switch in that both the unwanted signals injected via the control terminal and ringing due to inter-terminal capacitances cause less inaccuracy. However, the performance of this arrangement is still affected by mismatches in the operational amplifier positive and negative-going slew rates. As with DR, this becomes particularly significant at low duty factors

For maximum accuracy, whether DR or SR is used, an operational amplifier with an accurate transient response is required. The operational amplifier will normally act in a slew rate limited mode. For average current sensing of rectangular current waveforms, this does not necessarily introduce inaccuracy provided the positive and negative-going slew rates are identical. However, the degree of symmetry is not normally specified by manufacturers. During the experimental work considerable asymmetry was found to exist between operational amplifiers of the same type number.

8.1.3 Reset Voltage Feedback

8.1.3.1 Reset Voltage Feedback with Linear Correction Stage

A further technique, reset voltage feedback, has been investigated for addressing droop in the UCPT. Its secondary terminal voltage is adjusted during a current pulse in response to the peak resetting voltage sensed during previous switching cycles. Arbitrary component values have been used to evaluate the technique and experimental results have been compared with simulated results.

Reset voltage feedback is shown to be effective. However, it performs best when sensing a rectangular primary waveform without abrupt changes in magnitude and duty factor. The CT's core flux excursion is very small and, consequently, the error

due to core losses is also very small. The problem of discontinuous secondary current operation is virtually eliminated when operating at permutations of low current and high duty factor. With a triangular component in a current pulse, some core excitation is incurred, as is some (negative) average current droop.

Advantages are that a very low steady-state error in the average current sensed is attained and the threshold at which the secondary current becomes discontinuous is lowered. However, as with any feedback scheme, a compromise is needed between maximizing transient performance and retaining stability. Also, being a scheme with a repetitive discrete behaviour, there is the potential for sub-harmonic oscillations. With ramp current waveforms, complete elimination of droop is not achieved using reset voltage feedback and some negative average current droop is incurred. Although not definable as peak current droop in the normal way, distortion of the instantaneous current sensed is also present with ramp waveforms. Both these forms of droop may be minimized by ensuring that the CT's time constant is large compared to the pulse length, and ideally using a rectifier diode with a "flat" *v-i* characteristic.

An attractive feature of reset voltage feedback when compared to DR and SR is that the transient response of the operational amplifier is less important as its output does not have to slew at a significant rate.

8.1.3.2 Reset Voltage Feedback with Switched-Mode Correction Stage

The reset voltage scheme has also been implemented using a switched-mode stage. It has been shown that this can yield an improvement in efficiency. However, a ripple current component is added to the sensed current, as well as transient switching noise attributable to the operation of the switched-mode circuitry. Also, efficiency is only improved if the saving in dissipative losses incurred in the linear stage are not offset by standby losses. A feature is that, ideally, the comparator is capable of high-frequency operation (eg., at 1 MHz if it is to operate at ten times a typical PWM

frequency of 100kHz). It should also exhibit low power consumption. However, these tend to be conflicting properties in a practical comparator design.

8.2 Classification of Work Done against Existing Techniques

To put the work in this thesis into context with respect to the discussions in Section 1.3.6, Table 8.1 tabulates it against the techniques shown in Figure 1.4 and also selected references exemplifying the prior art.

<table>
<tr><th colspan="3">Technique (as categorized in Figure 1.4)</th><th>References Exemplifying Prior Art</th><th>Work in Thesis</th></tr>
<tr><td colspan="3"></td><td></td><td></td></tr>
<tr><td>A. Minimise external secondary impedance seen by CT</td><td colspan="2"></td><td>[57, 59]</td><td>Chapter 5: synchronous rectification</td></tr>
<tr><td rowspan="3">B. Actively control terminal voltage of CT in order to minimise core flux</td><td colspan="2">B.1. Infer required terminal voltage from secondary current and CT's secondary winding impedance</td><td>[60]</td><td>-</td></tr>
<tr><td rowspan="2">B.2. Modify terminal voltage in response to sensed core flux</td><td>B.2.a. Directly sense core flux</td><td>[11, 12, 14]</td><td>-</td></tr>
<tr><td>B.2.b. Indirectly sense core flux</td><td>[29]</td><td>Chapters 6 and 7: reset voltage sensing</td></tr>
<tr><td>C. Add correcting terms to CT's output signal</td><td colspan="2"></td><td>[61, 62]</td><td>Chapters 3 and 4: diode rectification</td></tr>
</table>

Table 8.1. Classification of Approaches to Reducing Distortion in Signal Derived from a CT

8.3 Suggested Further Work

It is suggested that the topics described below may merit further investigation.

1. The relationship between the lossless and "lossy" models for CT behaviour with DR may be investigated to develop a more comprehensive model. As the CT's peak flux excursion approaches zero at high frequencies and low duty

factors, then the lossless model becomes more appropriate. A combined model may therefore be developed. It is noted that the equipment used for measuring currents, voltages and resistances in this thesis has typical accuracies of between 0.1 % and 1 %. Further experimentation with more accurate instrumentation may therefore be useful.

2. Standard commercial MnZn ferrite core materials have been used. These exhibit low core losses. However, more important criteria in CT circuits where droop correction algorithms are applied may include the tolerancing of the core losses and their temperature dependencies. Alternative materials may therefore be investigated.
3. A practical compensation scheme may be realised using either traditional analogue or digital PWM control circuitry as exemplified in [77].
4. Optimization of the CT's design specifically for use with active DR and SR schemes may yield an improved performance. System inputs may be regarded as current magnitude, frequency and duty factor. Outputs may be regarded as both peak and average current droop, maximum allowable duty factor and the restriction on the current magnitude and duty factor combination which must be met if the discontinuous secondary current mode is to be avoided. Elements influencing the process may be regarded as the magnetizing inductance, secondary winding resistance, equivalent capacitance and the core losses. The inter-relationships between these elements may be investigated and optimized.
5. In the reset voltage feedback schemes used for droop reduction, further work may include enhancing the circuit simulations, quantifying stability issues and optimizing component values. Feed-forward may be introduced to account for a proportion of the forward voltage drop across the rectifier diode. An improved practical realization of the switched-mode circuitry may be implemented to further improve efficiency.
6. The switched-mode arrangement has been applied to the CT with reset voltage feedback. This feedback method is loosely classed here with the use of a flux sense winding, another way of indirectly sensing core flux to allow a compensating voltage to be applied. This latter method was not considered in

the thesis as it involves complicating the CT's construction. However, it also may be suitable for operation with a switched-mode stage.

7. Hybrid permutations of the circuitry studied in this thesis may be investigated. For example, a CT may be used with either a passive or an active load, diode or synchronous rectification and with or without reset voltage. Also, the dual CT circuit may be used with different circuit permutations for each CT.
8. Operation of the CT arrangements presented in this thesis at both higher and lower frequencies may be investigated.

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APPENDIX 1

PUBLICATIONS BASED ON WORK CARRIED OUT FOR THE THESIS

The following principle papers based on the work carried out for this thesis have been published:

1. N. McNeill, N. K. Gupta, S. G. Burrow, D. Holliday and P. H. Mellor, "Application of Reset Voltage Feedback for Droop Minimization in the Unidirectional Current Pulse Transformer", IEEE Transactions on Power Electronics, Vol. 23, No. 2, pp. 591-599, March 2008
2. N. McNeill and N. K. Gupta, "Assessment of the Error in the Average Current Sensed by the Unidirectional Current Pulse Transformer", IET Circuits, Devices & Systems, Vol. 2, Issue 2, pp. 265-276, April 2008

APPENDIX 2

DROOP MEASUREMENTS FROM THE CURRENT TRANSFORMER WITH DIODE RECTIFICATION AT VARYING FREQUENCIES

A2.1 Introduction

In Chapter 3 it is shown that, at low frequencies, the average current droop (D_{ave}) in the signal derived from a CT used with DR is primarily dependent on losses in the CT's core material.

A2.2 Results

The circuitry in Figures 3.10, 3.11 and 3.12 is used again with the CT in 3F3 core material detailed in Table 3.2. I_{L1} is set at 1 A. Figure A2.1 shows the droop at frequencies of 10 kHz, 20 kHz, 50 kHz and 100 kHz. It can be seen that the core flux compensation algorithm becomes less appropriate as the operating frequency is raised. An increasing offset at $\delta \approx 0$ is evident as the frequency rises. With respect to Figure 3.27 where the absolute droop tends to zero at $\delta = 0$, two observations are made:

1. Firstly, the offset worsening as the frequency increases is attributable to the increased effect of the operational amplifier's asymmetrical rise and fall times, as discussed in Sections 2.2.2 and 5.2.2.
2. Secondly, the diode, operational amplifier and feedback resistor, although having the same specification, are all physically different components here.

It is further noted that the maximum allowable duty factor given by Equation (2.28) applies, where the duty factor at which incomplete reset results becomes lower as the frequency rises.

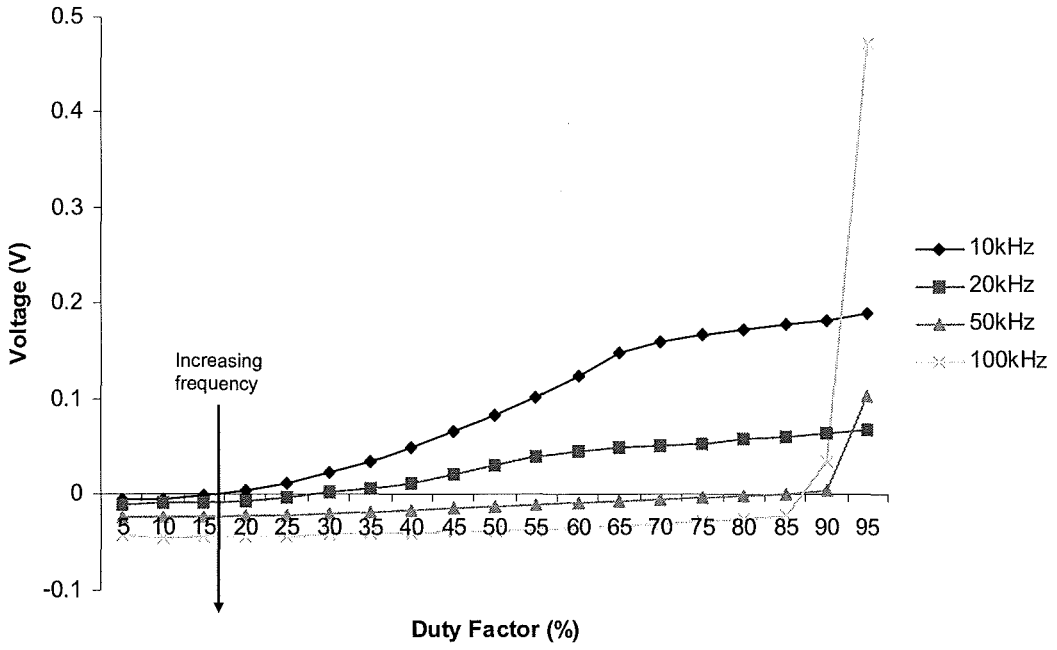

Figure A2.1. Absolute Droop at 10 kHz, 20 kHz, 50 kHz and 100 kHz (i_{L1} = 1 A)

APPENDIX 3

MEASUREMENTS OF THE EFFECT OF CORE TEMPERATURE ON AVERAGE CURRENT DROOP FROM THE CURRENT TRANSFORMER WITH DIODE RECTIFICATION

A3.1 Introduction

In Chapter 3 it is shown that, at low frequencies, the average current droop (D_{ave}) in the signal derived from a CT used with DR is primarily dependent on losses in the CT's core material. Where this material is a ferrite type, its temperature therefore influences D_{ave} as the losses in these materials are in turn strongly temperature dependent. Measurements of the temperature dependency of the error in the CT's output are given in this appendix.

A3.2 Experimental Arrangements

The circuitry in Figures 3.10, 3.11 and 3.12 is used again. However, the ambient temperature seen by the CT is varied by putting the printed circuit board it is mounted on (shown in Figure 3.12) into an enclosure and varying the internal temperature by means of a fan-cooled resistor. The ratio of power dissipation to surface area of the CT is very low, so the CT's core material temperature in the steady-state is close to ambient. (An infra-red temperature probe was used to measured the surface temperature of the CT as being approximately 1 °C above ambient when operating.) A type-K thermocouple is used to monitor the air temperature within the enclosure. The thermocouple's junction is located in air approximately 5 mm away from the CT (as shown in Figure 3.12).

The CT used is the 3F3 variant specified in Table 3.2.

Two complicating factors exist. Firstly, the rectifier diode's forward voltage drop is generally temperature dependent, having a negative coefficient in the case of the pn type (as used here). Secondly, the resistance of the secondary winding, R_2, has a temperature coefficient of 0.4 %/°C. However, the diode's forward voltage drop is only slightly affected by its temperature. In any case, for experimentation, the diode is outside the heated enclosure and is therefore at room temperature (between 20 °C and 25 °C) during experimentation. Also, the voltage drop across R_2 is low and the voltage impressed across L_{m2} is dominated by the diode's forward voltage drop.

A3.3 Results

The output from the CT was measured at between 20 °C and 100 °C inclusive in 20 °C increments. Figure A1.1 shows the sensed current (in the form of $v_{out(ave)}$) plotted against duty factor for I_p = 500 mA at 20 °C and 40 °C.

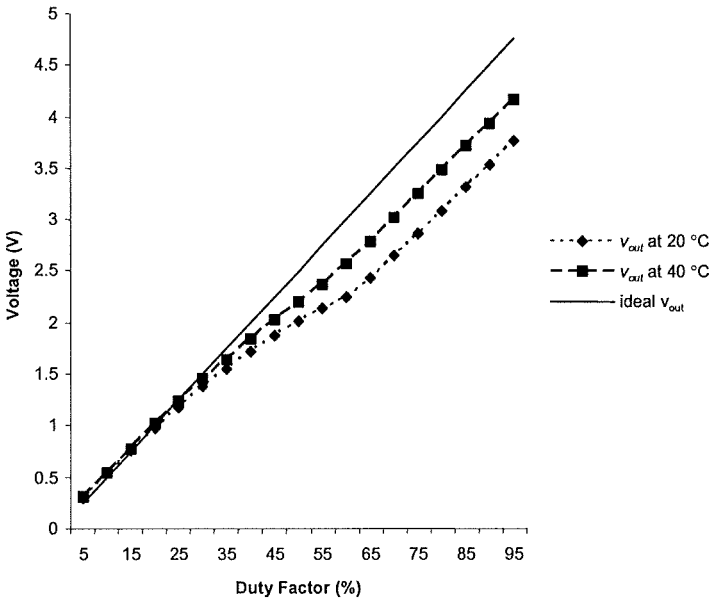

Figure A3.1. Output Voltage against Duty Factor for Varying Temperatures at I_p = 500 mA

Figure A3.2 shows the absolute error in the sensed current against duty factor for I_p = 500 mA at all five measurement temperatures, from 20 °C to 100 °C inclusive.

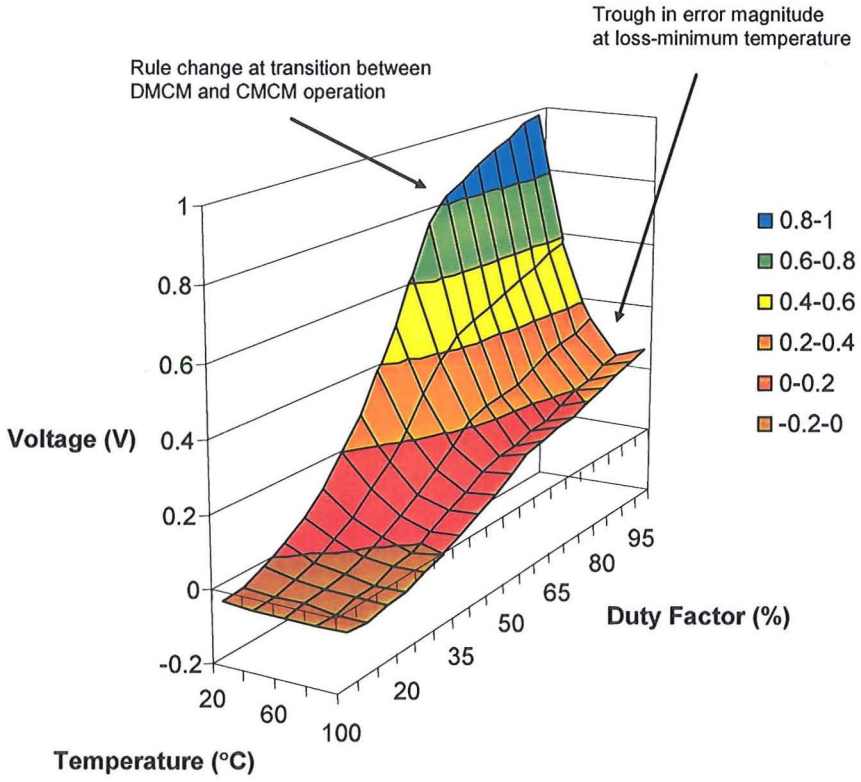

Figure A3.2. Absolute Droop against Duty Factor and Temperature at I_p = 500 mA

For clarity, Figure A3.3 shows the error at δ = 90 % at the different temperatures. (The measurements are taken at δ = 90 % as, at 95 %, the duration of the reset transient is only slightly less than the available off-time. This therefore ensures that droop attributable to incomplete reset is not incurred.) As expected, the curve is similar to the curves of core loss against temperature given by the core manufacturer in [71]. The data in [71] is shown as graphs of losses against temperature for four permutations of frequency and flux density excursion and no formulae are provided.

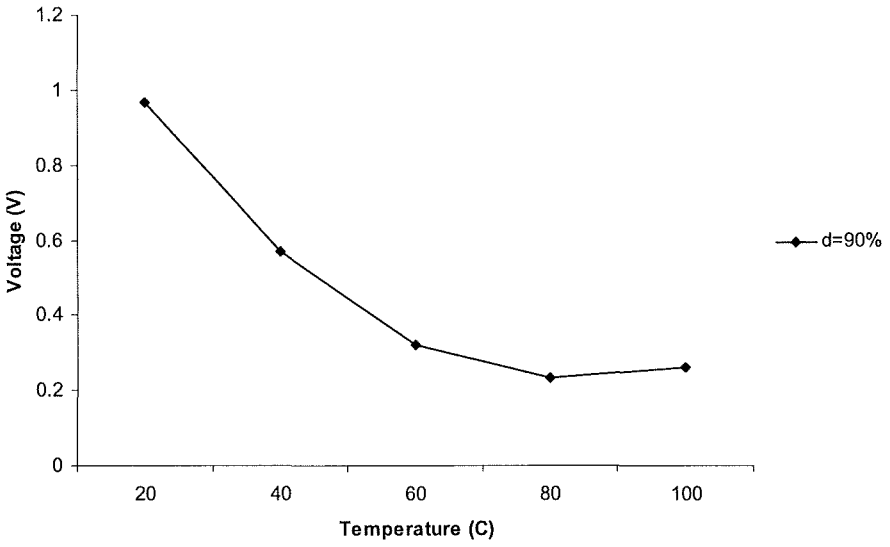

Figure A3.3. Absolute Droop against Temperature at $\delta = 90$ %

APPENDIX 4

ALTERNATIVE IMPLEMENTATION OF LINEAR RESET VOLTAGE FEEDBACK SCHEME USING DISCRETE MOSFET

In the linear realization of the reset voltage feedback technique in Chapter 6, an analogue switch is used to connect the end of the CT's winding alternately to zero volts and to the correcting voltage. The correcting voltage is derived from an operational amplifier which acts as a linear regulator. However, as with the synchronous rectification arrangements investigated in Chapter 5, a discrete MOSFET may also be used as the switch. This is described here.

Figure A4.1 shows an N-channel MOSFET, TR2, acting as the analogue switch (S2) in Figure 6.3. During T_{off} U1 detects the reset voltage transient and low-pass filters it as described in Chapter 6. TR2 is off during this period as its gate is held low by v_{GS} by means of D4. Although the node at "v_B" is not firmly connected to ground, the lumped capacitance between this node and ground allows only a relatively small voltage excursion at this point during T_{off}. When v_{GS} goes high, turning TR1 on, R2 pulls the voltage at the gate of TR2 up to v_c plus the forward voltage drop of D5 (V_f). TR2 operates in the (linear) source-follower mode and applies the correcting voltage to N2. During T_{off}, v_B is therefore given by:

$$v_B = v_c + V_f - V_{GS(th)} \tag{A4.1}$$

where $V_{GS(th)}$ is the gate-source threshold voltage of TR2.

Two points are noted:

1. As with the schemes in Chapter 5 where discrete MOSFETs are used for SR, the reset interval is increased due to the effect of introducing the MOSFET's inter-terminal capacitances across the CT's secondary winding terminals.

2. In addition to acting as the analogue switch, the MOSFET, and not the operational amplifier, acts as the linear regulator here in that it is the power dissipating element.

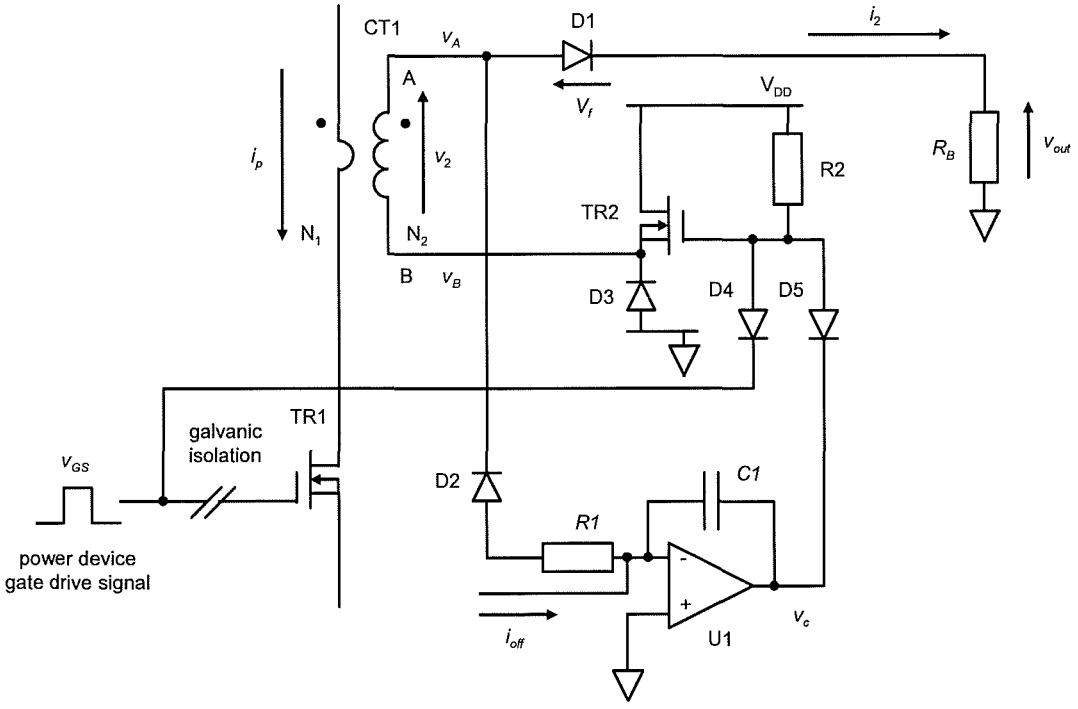

Figure A4.1. Alternative Implementation of Linear Reset Voltage Feedback Scheme Using Discrete MOSFET

APPENDIX 5

LINEAR RESET VOLTAGE FEEDBACK SCHEME REALIZED IN SURFACE-MOUNT TECHNOLOGY

Figure A5.1 shows the circuit in Figure 6.5 replicated in surface-mount packaging. The diode pairs D1/D2 and D3/D4 are realized using BAV99 dual anode-to-cathode packages. Ceramic decoupling capacitors are included across the 0 V to + 5V and 0 V to –5 V rails and a potentiometer is included to allow the easy adjustment of i_{off}. Figure A5.2 shows a more detailed view of the correction circuitry.

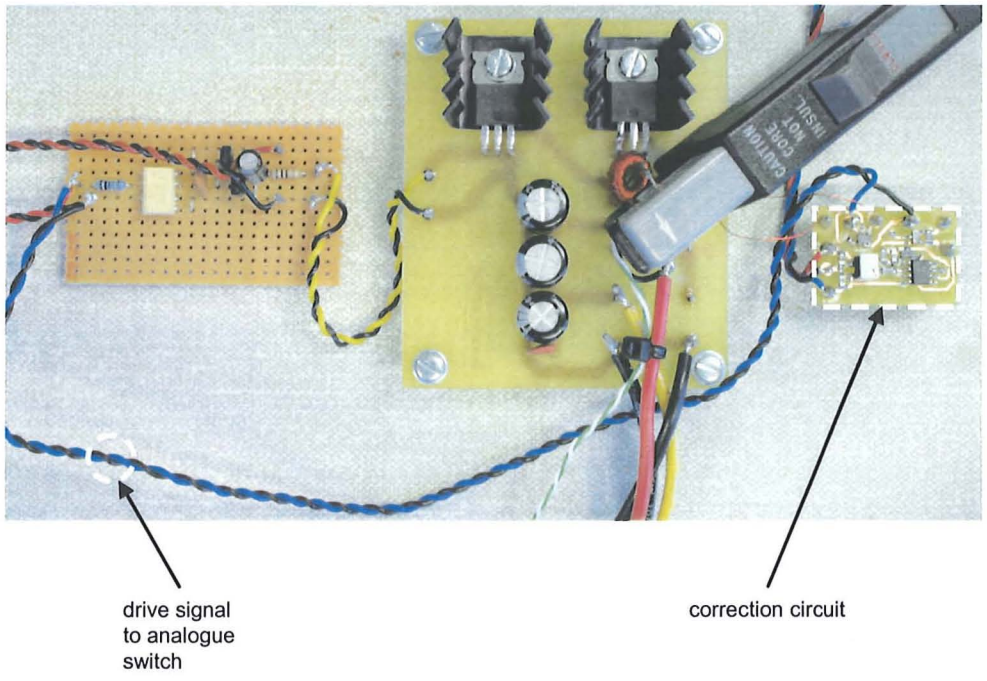

Figure A5.1. Photograph of Test Circuit showing Linear Reset Voltage Feedback Circuit Assembled in Surface-Mount Packaging

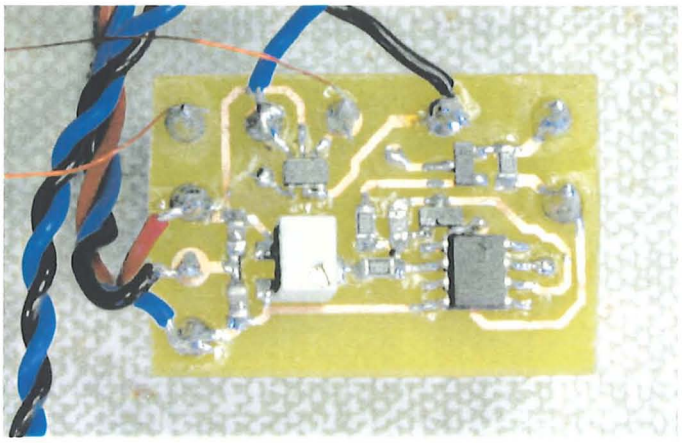

Figure A5.2. Correction Circuitry shown in Greater Detail