Voltage Balancing Sorting Algorithm with Reduced Switching Frequency for Modular Multilevel Converters

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Abstract

Over the last decade, Modular Multilevel Converters (MMCs) have been developed for medium- to high-voltage applications. They exhibit distinct features such as modularity, scalability, high degrees of redundancy and high-quality output voltage with the superior harmonic performance that reduces the requirement for filters. These features are unique to MMCs, thereby giving them a competitive advantage as an industrial solution over other voltage source multilevel converters.

However, there are challenges associated with such converters when numerous sub-modules (SMs) are considered. The issues involved include voltage-balancing of the distributed SM, circulating current suppression, reliability, and increased complexity in the circuit configuration.

The focus of this research is the voltage balancing of SMs. The most common and effective method of voltage-balancing is based on the well-known sorting algorithm, which results in higher switching frequency compared to other methods. This leads to substantially higher switching losses and hence lower efficiency, particularly when there are high numbers of SMs. Furthermore, the increased execution and calculation time leads to high computational complexity when the number of SM is high.

This thesis proposes three new voltage balancing schemes to reduce the unnecessary switching events which are typically generated by the conventional sorting algorithm (CSA) and to reduce computational complexity:

1. The Index Selection Algorithm (ISA) is based on a constraint band of permissible voltage ripples and existing gate signals to offer three index options. This technique selects the optimum choice based on the number of SMs contained in the band.

2. The Hybrid Heap Sorting Algorithm (HSA) replaces the CSA with the heap sorting

algorithm. With this technique, the computational complexity is significantly decreased.

3. The Priority-based Sorting Algorithm (PSA) clusters the SMs of converter into different priority groups according to a pre-defined voltage ripple range along with the gate signal information of the previous sampling period. It helps to reduce the switching frequency by only selecting the necessary priority groups to be involved in the sorting stage. Another benefit of this scheme is its flexibility and great dynamic response to different pre-defined range.

All the proposed algorithms produce fewer switching events and incur a lower computational cost, resulting in higher efficiency without detriment to the quality of the output waveform.

The proposed voltage balancing schemes are tested using 4- and 22- level MMC models which were built using MATLAB/Simulink to investigate their performance. The converter performance is also validated for a small-scale 4-level MMC that was designed, built, and tested in the laboratory. The validation shows that the proposed algorithms clearly reduce the number of switching events. In addition, the algorithm can be easily incorporated without requiring hardware modifications.

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List of Symbols

$\boldsymbol{B}$	Index of conventional sorting algorithm
$\boldsymbol{C1\text{-}C6}$	6 Priorities of PSA
C	Sub-module capacitance
$cos\emptyset$	Power factor
C_{SM}	Capacitance of SM
D_p	Possibility for a SM to change its state
E_{on}	Turn-on energy
E_{off}	Turn-off energy
E_{rec}	Reverse recovery energy
$\boldsymbol{F}$	Index of virtual sorting algorithm
f	Output frequency
f_C	Carrier frequency
f_{sample}	Sampling frequency
$g_{(i,j)}$	Gate signal of SMs
i_{arm}	Arm current
i_{circ}	Circulating current
$i^*_{circ\_ac}$	Reference circulating current
I_C	Current flows through the capacitor

I_F	Forward current of diode
i_N	Lower arm current
i_P	Upper arm current
i_u	Line current
I_{2f}	Peak value of double fundamental frequency of circulating current
K	The number of the group for high number SMs.
k	Current factor
L	Arm inductance
L_L	Load inductance
m_i	Modulation index
N	Number of the SMs in the arm
N'	Number of SMs need to be switched-on at one sampling period
n_K	Distributed required inserted number of SMs for sub-groups
n_{low}	Estimated required inserted number of SMs for lower arm
n_{up}	Estimated required inserted number of SMs for upper arm
O	Time complexity of algorithm
P_{con}	Conduction loss
P_{on}	Turn-on loss
P_{off}	Turn-off loss
P_s	Apparent power

P_{sw}	Switching loss
P_{total}	Total loss
R	Arm resistor
$\boldsymbol{R}$	Index of previous sampling period
R_1	Resistance of the ‘light’ mode
R_2	Resistance of the ‘heavy’ mode
R_{ESR}	Resistance of ESR
R_L	Load resistance
S	Switching states of SM
$\boldsymbol{S_1}$	Upper switch
$\boldsymbol{S_2}$	Lower switch
S_P	Switching pulses within one fundamental period
T	Fundamental period
T_0	The number of sorting time of CSA
T_1	The number of sorting time of ISA
T_2	The number of sorting time of HSA
T_2^{worst}	Comparison made by heap sorting for the wort case
$T_2^{worst''}$	Comparison made by HSA for the wort case
T_3	The number of sorting time of PSA
T_s	Sampled time
T_ω	Window width of MAF

U_c	DC component of capacitor voltage
u_{diff}	Inner unbalanced voltage
u_N	Average lower arm capacitor voltage
u_P	Average upper arm capacitor voltage
v_{avg}	Ideal average voltage of the arm
V_{Au}^*	Reference value of energy average control
V_{Bu}^*	Reference value of voltage balancing control
V_C	Voltage across the SM capacitor
V_C':	Virtual voltage across the capacitor
V_C^*	Ideal capacitor voltage
V_{cap}	Inner capacitance
V_{CE}	Collector-emitter block voltage of IGBT
V_{DC}	DC source voltage
V_F	Forward voltage of diode
V_N	Lower arm voltage
V_P	Upper arm voltage
V_{ref}	Reference capacitor voltage value
$\boldsymbol{v_{SM}}$	Measured voltage of the SM
$\mathbf{X}$	Value of pre-set ripple range
$\mathbf{Y}_{\boldsymbol{max}}$	The max level of heap tree map
α	Coefficient for SMs outside the range

$\delta V_{C,pp}$	Peak-to-peak acceptable ripple voltage
Δn	Changed number of required inserted SMs
θ	Phase shift between two adjacent carriers
σ	Capacitor variation range
ω_0	Fundamental frequency
$[n/K]$	Integer part of n/K
$\boldsymbol{B}$	Index of conventional sorting algorithm

List of Abbreviations

AC	Alternating current
ADC	Analogue to digital converter
AEP	Available estimation period
ANN	Artificial neural network
APOD	Alternative phase opposition disposition
BPF	Band-pass filters
CCS	Code composer studio
CHB	Cascaded H-bridge
CSA	Conventional sorting algorithm
CT	Comparison time
DC	Direct current
DSP	Digital signal processor
ESR	Equivalent series resistor
EP	Energy power ratio
FACTS	Flexible AC transmission systems
FAP	Fast affine projection algorithm
FCC	Flying capacitor converter
FFT	Fast Fourier transform

FPGA	Field programmable gate arrays
HPF	High-pass filter
HSA	Hybrid heap sorting algorithm
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
ISA	Index-based sorting algorithm
LCC	Line-commutated converter
LSPWM	Level-shift PWM
MAF	Moving average filter
MMC	Modular multilevel converter
MOSFET	Metal-oxide semiconductor field-effect transistor
HMC	Hybrid multilevel converter
LMS	Least means square algorithm
NLM	Nearest level modulation
NPC	Neutral point clamped converter
PSC-PWM	Phase-shifted carrier PWM
PSPWM	Phase-shift PWM
PWM	Pulse width modulation
PD	Phase disposition
PFM	Prime factorisation method
POD	Phase opposition disposition

PSA	Priority-based sorting algorithm
RLS	Recursive least square algorithm
SHE	Selective harmonic elimination
SM	Sub-module
SMO	Sliding mode observer
SVM	Space vector modulation
STACOM	Static synchronous compensator
TB	Tolerance band
THD	Total harmonic distortion
VSC	Voltage source converter

Chapter 1.Introduction

1.1 Background

Renewable energy sources such as solar and wind power have attracted close attention over the past two decades as environmental deterioration challenges the survival of humankind. However, due to its complex nature, the collection and delivery of renewable energy is a critical and problematic issue. According to the latest REN21 Renewable Global Status Report (GSR2019) [1], renewable energy will provide over 26% of global power energy generation in 2019. Given the rapid development of renewable energy, the requirement for advanced power electronics technologies has increased accordingly. The growing demand for renewable energy has also intensified the requirements of the reliability and quality of power grid interconnection and transmission. Therefore, High Voltage Direct Current (HVDC) is considered to be the core modern solution addressing these problems, connecting renewable energy sources to consumers with high power quality and minimal transmission losses.

The development of HVDC has involved several phases. In the beginning, the traditional two-level topology line-commutated converters (LCC)-based HVDC was considered to be an effective and efficient solution when dealing with the integration of renewable energy into the power system. However, the weakness of reactive power control and uncontrollable power devices limited its application. Thanks to the rapid development of the power devices such as Insulated-Gate Bipolar Transistors (IGBTs) and DC circuit breakers, the VSC-HVDC topology proposed by Boon-Teck Aoi in 1990 [2] was introduced to replace the LCC-HVDC for long-distance power transmission. The controllability and flexibility of the VSC-HVDC helped to improve the control of active and reactive power and to reduce the stress on semiconductors due to its better switching distribution [3]. The main disadvantage of this topology is the requirement for a high volume of filters on the AC sides due to the high total harmonic distortion (THD) [3]. Nowadays, the VSC-HVDC has become the backbone of multi-terminal DC grids

and super grid [4], and numerous VSC-HVDC grid projects have been planned, such as the European super grid and GRID 2030 in the USA. Meanwhile, the traditional two-level VSC-HVDC requires thousands of press-pack IGBTs, which results in high switching stress, high EMI, high harmonics and high power losses [5]. Therefore, designing the new converter topologies with higher-level output to overcome such problems is becoming a significant concern.

Multilevel converters were implemented with VSC-HVDCs to generate staircase waveforms via output voltage levels in attempting to approach sinusoidal waveforms. Theoretically, more voltage levels should mean more steps in the waveform to become closer to a sinusoidal shape. Therefore, there will be fewer output total harmonics distortion (THD). However, component volume and control complexity make it less cost-effective to apply multilevel converters in real applications. There are three main types multilevel converters, which are classified according to topology [3]:

1. Neutral-point clamped converter (NPC)[6],
2. Flying capacitor converter (FCC)[7, 8],
3. Cascaded H-bridge converter (CHB)[9].

The configurations of the above topologies are illustrated in Figure 1.1. NPCs and FCCs consist of numerous diodes and capacitors and can achieve variable voltage levels by controlling the states of the semiconductors. However, the quantity of these components rises significantly as the levels increase. The CHB topology requires a separate DC source, *E*, for each SM, so the problem of voltage balancing is negligible. However, these DC sources require transformers and rectifiers which increase the volume and cost of the H-bridge SMs. The modular multilevel converter (MMC) was introduced to overcome these disadvantages. For the past decade, the MMC topology has been widely used and is considered to be the most suitable topology for medium- and high-level voltage applications.

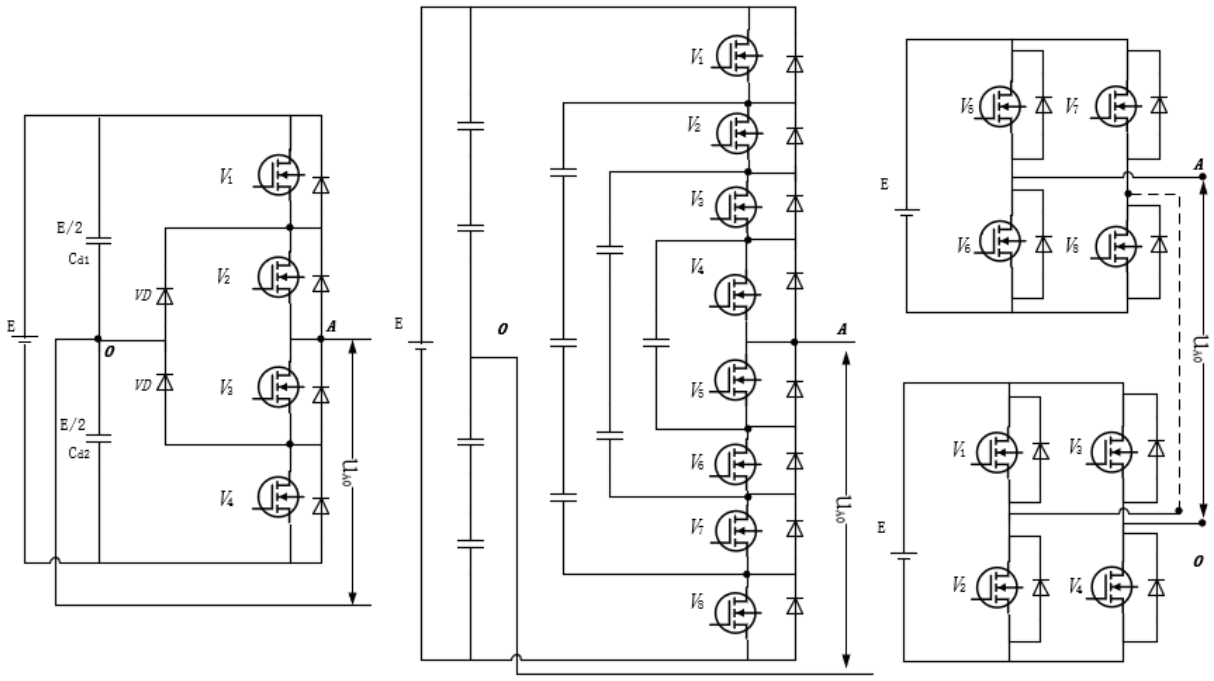


Figure 1.1 Conventional multilevel topologies: (a)NPC. (b)FCC. (c)CHB.

The classification of multilevel converters is depicted in Figure 1.2, along with some new proposed topologies which were based on the multilevel concept, such as the hybrid multilevel converter (HMC) [10, 11]. Multilevel converters have fewer harmonics and low switching frequency compared to traditional converters [5].

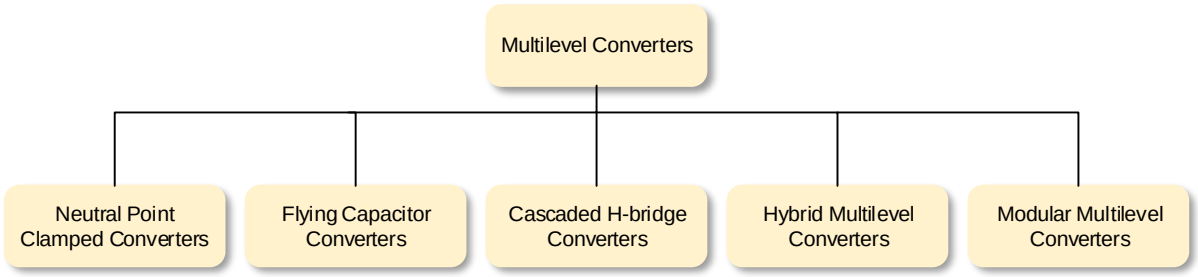


Figure 1.2 Classification of multilevel converters.

Since its introduction by Marquart and Lesnicar in 2003, the MMC has developed drastically and has already become the more competitive choice over LCCs and VSCs for past decades [12]. Compared to the NPC and FCC, the requirements for diodes and capacitors was decreased significantly, while compared in the CHB, an SM does not need a separate DC source, which leads to less component volume. The key advantages of MMCs over conventional VSC

converters for HVDC are as follows:

- The modularised system has good scalability and flexibility, which is beneficial for industrial design and redundancy control.
- Higher number of voltage levels help in reducing the voltage stress $\mathrm{d}u/\mathrm{d}t$, where a larger number of stairs is applied for the output AC waveform. Therefore, the voltage variation between two consecutive voltage stairs is lower compared to others with a fewer number of stairs with the same rated voltage level.
- Less harmonic distortion on the AC output side when the number of SMs is high means that there is less dependence on circuit filters.
- Appropriate control algorithms help to lower the switching frequency, reduce switching losses and increase power efficiency [13].
- The MMC can control the DC-link voltage, thus no DC-link capacitor or filters are required at the DC-bus, thereby reducing total volume and cost [14].
- Fast dynamic control under both transient and fault conditions [15].

However, there are also several disadvantages associated with MMCs which cannot be disregarded, including:

- The high number of SMs which necessitate a greater volume of components.
- The unbalanced voltage between each SM and the phase arms and phase legs leads to huge energy imbalances [16].
- The control methods required to balance the voltage between each SMs are relatively complicated in comparison to other approaches.

Overall, the MMC is an advanced topology with complex operation due to its multiple SM structure. There still numerous problems in terms of operation and control, which need to be addressed. This thesis investigates some of the problems of MMCs and proposes feasible solutions.

The most common application of an MMC system is for a power system, which starts with

the conversion of AC/DC for a Flexible AC Transmission System (FACTS). Then, the application of MMC is expanded to the HVDC power transmission and STATCOMs [17]. With its attractive features of high reliability and low maintenance costs compared to other multilevel converters, the implementation of MMC for power transmission appears to be favourable. Several major projects have been successfully completed using it, such as the Trans Bay project in the US [18], INFLFE in France and Spain, and Amprion GmbH and Transnet BW GmbH in Germany [19]. Research into MMC-HVDC has applied hundreds of SMs per arm to guarantee effectiveness [20]. MMC-HVDC has been widely applied and power loss reduction is one of its most attractive points for commercial design [21]. The MMC is also suitable for high-voltage DC/DC converters due to its flexibility and the fact that energy can flow in both directions. The MMC is also suitable for grid connection [22] and transformer-less inverters [23]. Energy storage for photovoltaic systems is another potential area where independent control of each energy storage module can be achieved.

Furthermore, the MMC can be used for other specialised applications, such as medium-voltage variable-speed drives [23-25]. Compared to the traditional H-bridge inverter, the MMC has better power transmission efficiency, but the capacitor voltage suffers from higher ripples, when electrical machines work at lower frequency modes, this requires further investigation. Similarly with the rail traction systems discussed elsewhere in[26], various problems remain to be resolved. Considerable effort has been devoted to determining the characteristics of MMCs, and great progress has been made in terms of topology, modulation and control methods, grid connection, reliability and industrial applications.

1.2 Research Motivations

Although the MMC has tremendous advantages compared to other multilevel converters topologies and has been widely applied for medium- to high-power conditions, there are still many problems that need to be resolved. The first and primary issue is its control complexity, since the series connection of submodules (SMs), unbalancing problems and reliability issues can be critical because any fault inside one SM has the potential to damage the whole system.

Therefore, enhanced control algorithms are essential. Secondly, although the MMC topology has lower switching frequency compared to other converter topologies, the high number of SMs means that the power losses accumulate, and so further to reducing the switching frequency remains an important topic. Thirdly, the modular structure makes it difficult to monitor the components inside the module, which necessitates hierarchical condition monitoring methods [27, 28].

Finally, execution time and calculation effort increase rapidly when numbers of SMs are high, thereby leading to significant computational complexity. With the development of processor technology, the latest processor from ABB HVDC Light [29] can deal with 8 million floating-point operations per 5 μs. However, the processor is also responsible for unit communication and component protection control, and the whole HVDC process will become a fully digitalised system. Also, operational control requires extra computational resources for the redundancy maintenance. Therefore, huge processing resources are required, and computational complexity involved is still very high. The purpose of this thesis is to assess and attempt to resolve these issues. The evaluation of computational complexity can be simplified by measuring the comparison times (CTs) of the algorithm. Here the term 'CT' refers how many times of the 'comparison' commands are executed every sampling period.

1.3 Research Objectives

The objectives of this thesis are as follows:

1. To investigate the relevant literatures and review the latest technologies related to MMCs, and evaluate the likely directions of future development.
2. To conduct a comprehensive analysis of MMCs, including their principles, operation, challenges and up-to-date solutions.
3. To propose novel voltage balancing approaches for SM capacitors with reduced switching frequency and computational complexity.

The proposed approaches are tested using MATLAB/Simulink and a scaled-down

hardware prototype. In doing so, this research strives to verify the effectiveness of the proposed techniques and to evaluate their potential for future application.

1.4 Verification Tools

All the present work and related analysis are based on the detailed simulation and experimental results. The simulation results were generated using MATLAB/Simulink/SIMPOWER (2017b version). The experimental process (see chapter 6) was conducted using a TMS320F28335 microcontroller from the Texas Instruments Semiconductor Manufacturing Company (TI), and the results are shown on display of a TEKTRONIX MDO3014 Mixed Domain Oscilloscope. The proposed methods were processed using MATLAB tools and its C code support packages to convert the algorithms and simulation circuits into a C code package. Then, the parameters can be tuned using the package to achieve better performance. Subsequently, the code was then uploaded to the digital signal processor (DSP) using TI's Code Composer Studio (CCS5.5) development tool packages. Further details of the practical validation work are provided in chapter 7, which presents the results for a scaled-down 4-level MMC system.

1.5 Thesis Contributions

This thesis focuses on improving the sorting algorithm in terms of the reduction of switching frequency and computational complexity without compromising its advantages of capacitor ripple control and quick dynamic response. The main contributions of the work are summarised as follows:

1. The reason for the generation of high unnecessary switching frequency is investigated. The range-based index selection method is proposed to eliminate it, with an advanced index arrangement to avoid unnecessary switching events without compromising output quality.

2. The sorting algorithm family is reviewed to identify different algorithms that could replace the bubble sorting algorithm. Heap sorting is selected due to its high efficiency in reducing computational complexity. This thesis helps to make adjustments to heap sorting to make it suitable for the voltage balancing of an MMC.

3. A novel priority-based algorithm is proposed which decreases the switching frequency by reducing the number of SMs involved in the switching events. Meanwhile, a smaller number of involving SMs can substantially reduce the comparison operations by the processor, and lead to less computational complexity. This algorithm is also flexible since priority is classified based on an acceptable range, and the ripple is controllable and varies according to different applications. Besides, the algorithm is also suitable for MMCs with high numbers of SMs, and therefore it is suitable for real cases.

4. A capacitance estimation scheme based on the proposed PSA is introduced which involves no extra hardware and does not affect output performance. Its feasibility is verified through simulation.

1.6 Layout of the Thesis

Chapter 2 first introduces the structure, principles of operation and mathematical descriptions of the MMC. Then, the operational states of SMs are investigated in detail, and modulation techniques are demonstrated. The primary challenges associated with MMCs are introduced, including parameter selection, reliability issues, circulating current suppression and voltage balancing methods. Among all of the challenges, voltage balancing is the most important, and sorting algorithm has been widely used due to its high efficiency, effectiveness in limiting capacitor voltage ripple and ease of implementation.

Chapter 3 focuses on the sorting algorithm and provides an up-to-date literature review. The sorting algorithm itself produces unnecessary switching that is not desirable in an MMC. The ideal performance of the optimisation method used by the sorting algorithm should achieve three aims: low switching frequency, low complexity and good quality. Therefore, stronger approaches to improve sorting algorithms are essential. Recent studies have made several attempts to improve the performance of sorting algorithms and are evaluated in this chapter.

Chapter 4 first investigates the reason for the generation of high number of switching events by sorting algorithms. Then, it presents an index selection concept which provides several options during every sampling period to avoid unnecessary switching events during

sorting. The use of this approach means that SMs within the nominated ripple range are less likely to change their states, and SMs outside the ripple range converge to the reference value more rapidly.

Chapter 5 attempts to identify new sorting algorithm to replace the conventional algorithm. The heap sorting algorithm is deemed to be particularly suitable for MMC voltage balancing. Due to its complete binary heap tree, not all of the nodes inside the tree need to be involved in the comparison process, which helps in reducing the computational complexity. Be, heap sorting is compatible with switching frequency reduction methods for further optimisation.

Chapter 6 introduces the proposed method based on pre-defined priority groups. It defines a pre-defined range for classification before the sorting process, and then a new set of priority group selection rules is applied to overcome the disadvantages associated with the CSA. This scheme minimises the number of SMs involved in the sorting process. During the simulation, all of the proposed schemes are verified and compared via a simulation model, which demonstrates their potential.

Chapter 7 presents the validation of the proposed methods based on practical experimental work. Detailed descriptions of each component of the prototype in the experiment are provided, and the selection of components and parameters is explained. The validation work was carried out primarily to test the performance of switching frequency reduction of proposed methods, and all the proposed methods are successfully validated.

Chapter 8 proposes an application of the switching reduction control scheme, which can provide a long ON-STATE period. The SMs are shown to be unlikely to change their states when they are inside the pre-set range. This proposed control scheme enables the application of a fast and accurate online estimation method called fast affine projection (FAP) to monitor the parameters of SM capacitors. The verification work is conducted via simulation.

Chapter 9 presents the conclusions from all of the theoretical, simulation and practical work. The contributions of this study are then detailed. Finally, the potential directions for further research are summarised.

Chapter 2. Structure, Operation, Modulation and Challenges Associated with MMC

2.1 Introduction

This chapter describes the structure, operation, modulation techniques, characteristics, and application of MMCs. As one of the multilevel structures for VSC with the development of power electronics, the MMC structure has great advantages over others. This chapter begins with operation models of the MMC, and a mathematical model for the MMC is then built for analysis. A comparison of the different modulation techniques is made, and they are classified into three groups according to the switching frequency involved. Finally, the applications of MMC up to now and in the future are presented. The main challenges in MMC design and previous studies of these challenges are then discussed in this chapter. They include voltage balancing, circulating current suppression and parameter selection. Among all of the challenges, voltage balancing is the most important. This chapter summarises the existing voltage balancing methods and, based on a comparison of methods, provides an analysis of reason for implementing the sorting algorithm to balance the capacitor voltage.

2.2 Principle and Basic Operation of MMC

The half-bridge structure is the most commonly used SM structure for MMCs, as depicted in Figure 2.1. The converter normally consists of three phase legs, each of which is divided into two arms, the upper arm and lower arm (in this study, only single-phase MMC is investigated for better illustration) [30]. Each arm contains an identical number of cascaded submodules (SMs) which are connected in series, and an arm inductor L. The SM typically utilises the half-bridge structure rather than the full-bridge structure [31]. The half-bridge structure consists two complementary power switches and a capacitor for building up the voltage to desired output waveform.

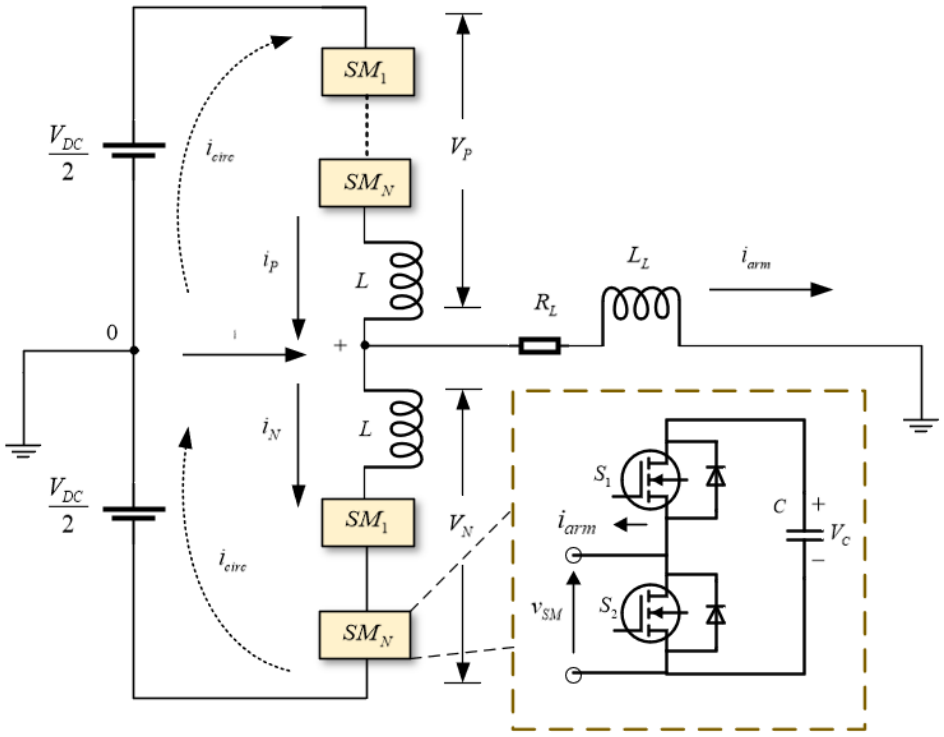


Figure 2.1 The structure of single-phase MMC with its SM.

However, the half-bridge structure cannot suppress DC-side fault current, and thus the full-bridge configuration has been discussed as an alternative [32] and the basic structure of both structures are shown in Figure 2.2. Compared to the half-bridge structure, the full-bridge SM can effectively block the DC-side short current, besides which it provides higher flexibility and the ability to generate more output levels with the same number of SMs. However, this structure requires more semiconductors, which increases both losses and the control complexity. Therefore, it is a less cost-effective choice. The half-bridge structure is normally selected for the SM [33], and the half-bridge and full-bridge configuration are compared in detail elsewhere [31], and it has been conducted that the half-bridge is more suitable in terms of switching losses and control complexity.

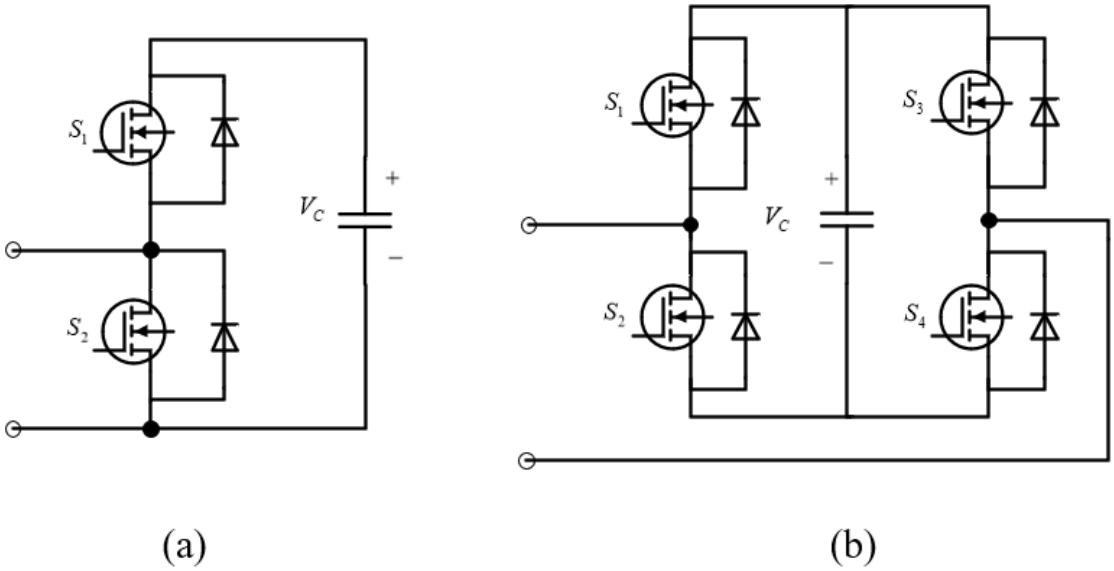


Figure 2.2 The SM structure of (a) Half-bridge MMC. (b) Full-bridge MMC.

Therefore, in this thesis, the half-bridge structure is selected for the MMC. In Figure 2.3, switches S_1 and S_2 are complementary IGBTs (MOSFETs). The red line represents the current flow and the arrow shows the direction of the arm current. The output voltage of the SM is either V_C or 0 based on the manipulation of the switching states of S_1 and S_2. Normally, the signal of the upper switch S_1 represents the gate signal of the whole SM.

When the upper switch S_1 is conducting and the upper switch S_2 is bypassed accordingly, the SM voltage v_{SM} is the voltage across the capacitor. Consequently, the arm current I_{arm} is charging or discharging the capacitor based on the current direction, as shown in diagrams (a) and (b) in Figure 2.3. These two states of the SM are defined as inserted. Conversely, when the SM is defined as in the bypassed states, the capacitor is isolated from the circuit so that the output voltage v_{SM} is equal to 0 as shown in diagrams (c) and (d) of Figure 2.3. These two states of SMs are defined as bypassed, where the voltage across the capacitor maintains the same level. The arm current i_{arm} is no longer charging or discharging the capacitor, and instead it flows through the switch S_2 or diode D_2. Besides, two fault states exist when both switches are switched off simultaneously, where both semiconductors and capacitor are blocking the current in either direction. The fault states are normally requires for the redundancy control of the MMC, and the SMs are isolated from the circuits if they are recognized as faulty. These

conditions normally arise due to the failure of SMs and can be viewed as short-circuits in the analysis. Details regarding all four basic switching states and two fault states are provided below in Table 2-I for clarity.

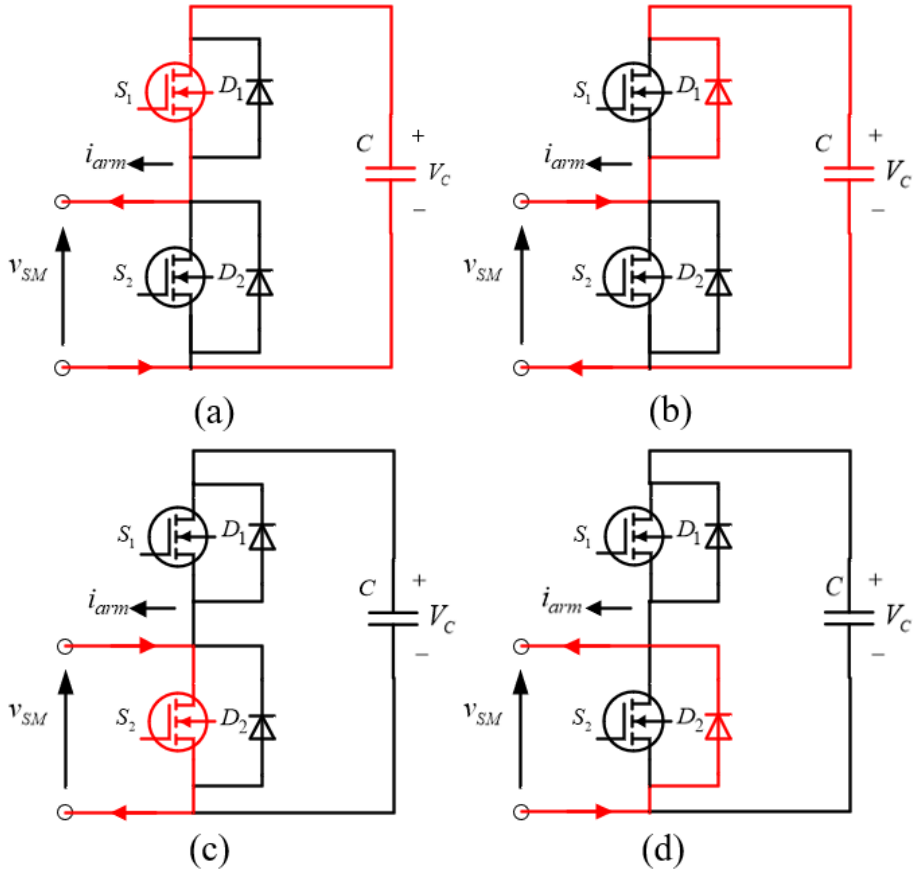


Figure 2.3 Four basic switching states under normal operation.

Table 2-I Switching states of SMs.

S_1	S_2	v_{SM}	Current Direction	Capacitor State
ON	OFF	Vc	I_{arm}>0	Charging
ON	OFF	Vc	I_{arm}<0	Discharging
OFF	ON	0	I_{arm}>0	Bypassed
OFF	ON	0	I_{arm}<0	Bypassed
OFF	OFF	Vc	No Current	Isolated
OFF	OFF	0	No Current	Isolated

Depending on the topology of the MMC, the phase output voltage is generated by selecting the switching states of each SM of the phase leg [34]. Each SM contributes to one level of the output. By applying the appropriate control method, the output voltage can approach a sinusoidal AC waveform in ideal cases. At every sampling period, the total number of inserted SMs within one phase leg is maintained at *N* to ensure that the level of output does not exceed the limit.

2.3 Mathematical Model of MMC

A circuits diagram of a single-phase MMC with a half-bridge SM structure is depicted in Figure 2.1. The DC source can be divided into two identical parts with same value, $\frac{V_{DC}}{2}$, while the AC side is connected to an RL load, R_L and L_L. The mathematical model of the MMC developed in this section depends on the analysis in previous studies [35, 36]. The equations developed in this chapter are designed for a three-phase MMC.

Assuming the i_{uj} represents the line current of phase j $(j = a, b, c)$, i_{Pj} and i_{Nj} are the upper arm current and lower arm current of phase j respectively. The arm inductors are represented as L so the arm voltage of phase j is given by:

$$V_{Pj} = \sum_{i=1}^{N} S_{Pj} \cdot u_{Pj} + L\frac{di_{Pj}}{dt} \quad ,j = a, b, c \tag{2.1}$$

$$V_{Nj} = \sum_{i=1}^{N} S_{Nj} \cdot u_{Nj} + L\frac{di_{Nj}}{dt} \tag{2.2}$$

where V_{Pj} and V_{Nj} are the voltages of the upper and lower arms of phase j respectively. The u_{Pj} and u_{Nj} are the average capacitor voltages of the upper or lower arm voltage of phase j respectively. The S_{Pj} and S_{Nj} are the switching states of SMs on upper arm or lower arm of phase j and are expressed by:

$$S_j = \begin{cases} 0 & (The\ SM\ is\ switched\ off) \\ 1 & (The\ SM\ is\ switched\ on) \end{cases} \tag{2.3}$$

where u_j is the output voltage of the AC side of phase j. Considering the above equations, the voltage of the DC side and the AC side are given by:

$$V_{Pj} + V_{Nj} = V_{DC} \tag{2.6}$$

$$u_j = \frac{V_{Nj} - V_{Pj}}{2} \tag{2.7}$$

he upper arm current and lower arm current of phase j, are defined as i_{Pj} and i_{Nj}, and are expressed by:

$$i_{Pj} = i_{circj} + \frac{i_{uj}}{2} \tag{2.8}$$

$$i_{Nj} = i_{circj} - \frac{i_{uj}}{2} \tag{2.9}$$

where the i_{uj} and i_{circj} represents the output current and circulating current of phase j respectively, and are defined as:

$$i_{circj} = \frac{i_{Pj} + i_{Nj}}{2} \tag{2.10}$$

$$i_{uj} = \frac{i_{Pj} - i_{Nj}}{2} \tag{2.11}$$

Rearranging the above equations, the dynamic behaviours of MMC are described as:

$$u_j = \frac{V_{Pj} - V_{Nj}}{2} - \left(\frac{L}{2} + L_L\right)\frac{di_{uj}}{dt} - \frac{R_L}{2} i_{uj} \tag{2.12}$$

$$\frac{V_{DC}}{2} - \frac{V_{Pj} + V_{Nj}}{2} = L\frac{di_{circj}}{dt} + R_L i_{circj} = u_{diffj} \tag{2.13}$$

where u_{diffj} is the inner unbalance voltage and is generated by the difference between the two arms of phase j which control the inner dynamic performance. Equation 2.12 and 2.13 demonstrates that the AC side voltage is controllable based on the upper and lower arm voltages[27]. The relationship between the circulating current, arm current and output current is presented through Equation 2.10 and 2.11 [37].

2.4 Modulation Techniques of MMC

As a critical procedure for maintaining the MMCs' operation, modulation techniques establish quality of the output voltage waveform by ascertaining the state of each SM that is to be inserted and bypassed. Also, pulse-width modulation (PWM) has a significant impact on the harmonic performance of the output. Thus, the voltage required for the operation of the converter can be determined depending on the modulation technique used.

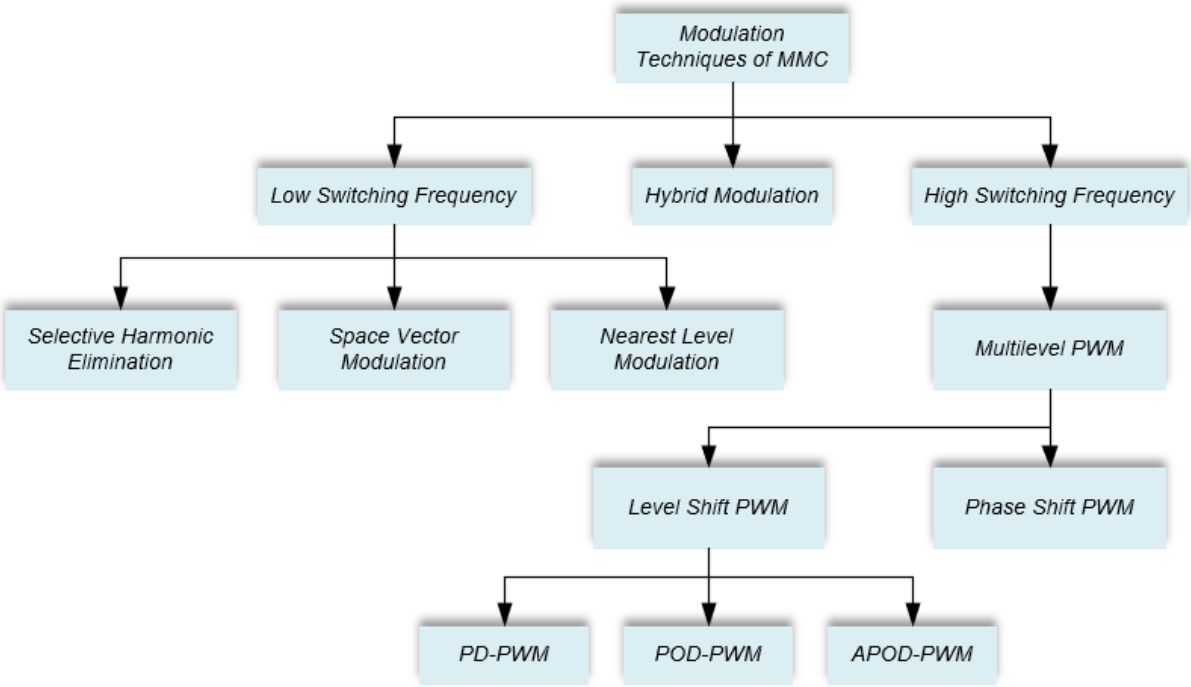


Figure 2.4 Classification of MMC modulation techniques.

The normal modulation techniques generate the N+1 type modulation signal for the MMC where the carriers of the upper and lower arms have the same phase angles. However, when turning the carrier of the lower arm over 180 degrees, the modulation techniques generate 2N+1 type modulation signal, which is referred to as interleaving [28]. The interleaving modulation technique is designed to increase the voltage level, but the complexity of the control method involved is high. Thus, there is extra distortion in the system, which makes the interleaving technique not the first choice for normal applications. Therefore, in this chapter, only non-interleaving modulation techniques are discussed in detail which are suitable for generic conditions.

Several different kinds of modulation technique have been proposed over the decades. This section gives a brief introduction and classification to some of the most commonly used. As illustrated in Figure 2.4, there are three categories of such techniques according to their switching frequency level: low, high and hybrid switching frequency [38].

2.4.1 Low switching frequency modulation techniques

The main low switching frequency modulation techniques include selective harmonic elimination (SHE), nearest level modulation (NLM) and space vector PWM (SVPWM) [39]. Among these, SVPWM gives a great reduction in total harmonic distortion (THD). It is simple to implement with voltages in low-level situations, especially for two-level VSCs [40, 41]. However, substantial computational costs accrue when the numbers of redundant vectors rise as a consequence of increasing voltage level [42].

SHE is another low switching frequency modulation technique which cancels out specific harmonics of the output voltage waveform [43]. SHE is used to achieving switching of a pre-defined moment and has a good total harmonic distortion (THD) performance but the computational burden is increased significantly[38, 44]. Modulation techniques for MMCs of fundamental switching frequency have been proposed elsewhere [45].

The most direct method is Nearest Level Modulation (NLM), which is mostly used for the MMCs with high numbers of SMs[7, 46, 47]. These methods rely on the function *round(x)* to estimate the required inserted number. There are several ways to set the estimate of numbers of required inserted SMs $n_{up/low}$ of the upper or lower arms. A simple way is:

$$n_{up/low} = round\ (x) = round\left(\frac{v_{avg}}{v_{sm}}\right) \tag{2.14}$$

where v_{avg} is the ideal average value of the upper or lower arm. Due to its simplicity, NLM is typically employed under conditions where the output voltage has more voltage level but demonstrates higher harmonics than other modulation techniques. Based on a previous analysis [46], NLM has larger THD and harmonics when the voltage level is low, consequently restricting its application.

2.4.2 High switching frequency modulation techniques

The main high switching frequency modulation techniques are carrier-based switching algorithms. Carrier-based algorithms can be classified as level-shift PWM (LSPWM) and phase-shift PWM (PSPWM) based on the distribution of the carrier waveform [48]. Whilst the high switching frequency generates greater power losses than other methods, these carrier-based techniques are nevertheless widely applied in MMC systems due firstly to their compatibility with the modularised model, and secondly because there is no significant increase in computational costs when high number of SM is applied. Additionally, they are easy to implement with the sorting algorithm. Moreover, the drawbacks of high switching frequency can be overcome using some of the recently proposed optimisation methods discussed further in the next chapter.

PSPWM is used to compare the variable sinusoidal reference waveform with carriers to determine the gate signals of all SMs. The reference waveform of each SM has a fixed phase variation with the adjacent one. Regardless of the reference phase angle, the carriers of each SM are identical, meaning that there are similar switching frequencies and power losses for each SMs are close. Consequently, the imbalanced voltage between the SM capacitors is minimal compared to when other techniques are used. Moreover, THD performance is good, making PSPWM one of the most commonly applied techniques for MMCs. The principle of PSPWM is illustrated in Figure 2.5. An $N+1$ level MMC requires N sets of independent pulse width modulation (PWM) signals to drive N SMs. The phase shift between two adjacent carrier signals is given by:

$$\theta = 2\pi/N \tag{2.15}$$

Similarly, for the $2N+1$ level MMC, the phase shift becomes:

$$\theta = \pi/N \tag{2.16}$$

With LSPWM is the carriers are at the same magnitude, but evenly and symmetrically displaced across the zero axis, as illustrated in Figure 2.6. LSPWM can be further classified

depending on the relationship between the phase angle of carriers into: phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) [28], where the selected carriers are designed to inverse their phase so as to achieve different required inserted numbers for the MMC. These methods can all help reducing the harmonics for various applications of MMC. However, due to the nature of LSPWM, the carrier distribution becomes uneven, which leads to unequal switching events across SMs, thereby distorts the power balance between them.

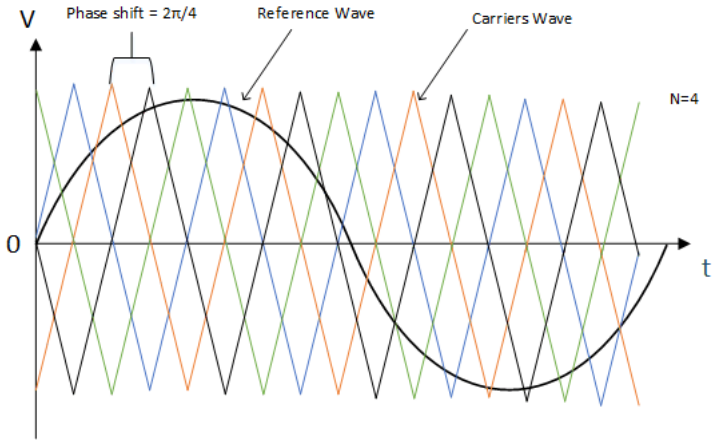


Figure 2.5 PSPWM modulation technique.

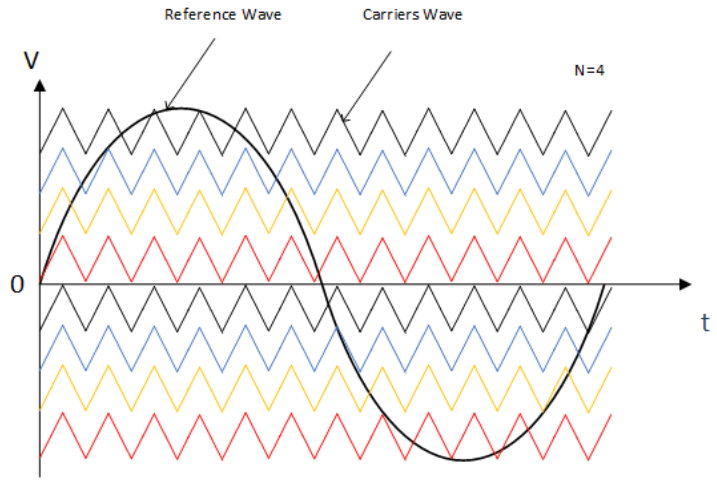


Figure 2.6 LSPWM modulation technique.

2.4.3 Hybrid modulation techniques

Considering the advantages and disadvantages of both low-frequency and high-frequency modulation, some hybrid modulation techniques have been proposed. The traditional NLM

improvement is illustrated elsewhere [39]. A method with improved PSPWM for the high-frequency current component has been proposed where NLM still being applied to the low-frequency component [49]. With the introduction of the hysteresis loop to NLM modulation, the NLM error can be complied [50, 51]. The aim is to make the MMC operate at different switching frequencies based on the NLM modulation errors. Overall, these methods are yet to become the most suitable choice for MMC applications.

2.5 Challenges Associated with MMCs

Since the MMC has been the most popular power converters topology compared to traditional multilevel converters for medium- to high-power applications, enormous efforts have been undertaken to improve its performance. Saeedifard discusses the basic operation and the control of MMC based on schematic diagram and mathematical analysis [30], and compares it with other multilevel converters to demonstrate its superiority. The features and operations involved are mentioned elsewhere in Chapter 2. According to previews research, there are various technical challenges associated with MMCs, particularly in terms of high power and the high numbers of SMs in the systems. The primary challenges which have been identified are as follows:

1. Parameter design and selection, which chiefly refers to the analysis of arm inductance and SM capacitance, where the mathematical models for the parameter selection are proposed [34, 52]. Moreover, the insulation level for the design of MMC must be taken into consideration that select parameters to meet the requirement of the insulation withstand level, based on the worst-case voltage level.

2. New topologies based on modular designs, including full-bridge and hybrid SMs. The full-bridge configuration is discussed in [32], and compared it with half-bridge configuration in detail [31]. The half-bridge is more popular because of the lower control complexity and computational cost. A new dual-SM structure has been introduced , which provides the ability to block the DC fault current [15].

3. Voltage balancing issues include the voltage between each SM, the phase arms and phase

legs. Different methods to tackle this have diverse effects in terms of capacitor ripple and balancing effects [30, 53-56], as discussed in the next chapter.

4. Current control, which mainly focuses on circulating current suppression. The circulating current circulates around the phase legs and this consequently increases voltage ripples and power losses.

5. Reliability issues, where fault tolerance, redundancy control and component condition monitoring are key points. Typically, problems arise in the series connections of SMs for high-level MMCs, since even the most minor error occurring inside one SM can result in catastrophic failure. A method for the detection of fault semiconductor is proposed [42, 57]. An SM capacitor bank is built, and compared to the traditional SM capacitor[58]. A reliability model has been built for the calculation [59], and other studies have focused on the condition monitoring of the SM capacitor with signal injection to the reference signal of PWM [60, 61].

6. Cost issues. Unavoidable costs include the cost of constructing the system, and the computational costs. With the developments in power electronics, the cost of components has been decreasing over time, but the computational complexity for control methods remains a substantial challenge. One study [56] relies on changing the sampling period to reduce the complexity, whilst another [42] introduces a sensor-less algorithm to reduce the number of current sensors in the system. Moreover, the number of voltage sensors can be reduced by implementing the state observers, and consequently reduce the computational cost [62].

2.5.1 Parameter selection

In order to enhance MMC design, the parameter selection is very important. Among the components of the MMC system, the arm inductor and SM capacitor are the most important. As mentioned above, even though various studies have achieved a reduction in the circulating current and balanced the voltage, these solutions all increase the computational complexity of the system due to the need for the extra measurements and controllers. Therefore, the

appropriate parameter selection helps in reducing the AC component of the circulating current and voltage ripples from the outset, and this eventually helps to improve the performance of the system [52].

The SM capacitor is an energy storage capacitor that helps in reducing the voltage ripples across it, when larger capacitors are more effective in storing energy and reducing fluctuation ripple[34]. However, the larger size requires components with large volume and cost. For the three-phase MMC, the SM capacitor is determined as follows:

$$C_{SM} = \frac{1}{3NmV_C\delta V_{C,pp}\omega\cos\emptyset}\left(1-(\frac{m\cos\emptyset}{2})^2\right)^{\frac{3}{2}} \tag{2.18}$$

where N is the number of SMs in one phase arm and can also be viewed as the total number of SMs at a specific sampling point, $\delta V_{C,pp}$ is the permissible peak-to-peak ripple magnitude for SM capacitor voltage. The arm inductor helps limit the faulty current across the arm as well as reducing the high-frequency harmonics. It can also block DC-side short circuits and make the current manageable through the use of appropriate control methods[63, 64]. Meanwhile, the circulating current can also be suppressed by increasing the value of the inductor, as in capacitance selection, although volume and cost implications must be taken into consideration:

$$L = \frac{1}{8\omega_0^2 \cdot C_{SM} \cdot U_c}\left(\frac{P_S}{3I_{2f}} + V_{DC}\right) \tag{2.19}$$

where U_c is the DC component of capacitor voltage, P_s is defined as the apparent power, ω_0 is the fundamental frequency of the MMC and I_{2f} is the peak value of the double fundamental frequency of the circulating current [65].

2.5.2 Component reliability

The proper operation of the system relies on the correct condition of every single power electronics device, and this is especially true for the MMC system where the SMs are connected in series. Therefore reliability issues in MMCs pose another big challenge. A fault in any of these vulnerable devices (MOSFETs, IGBTs, diodes, capacitors, etc.) could lead to distortion, failure and even system shutdown.

There are four basic categories of reliability issues with MMCs:

1. Reliability assessment,
2. Fault detection,
3. Health monitoring,
4. Fault tolerance.

The first step concerns how to evaluate the reliability, and description of system reliability include serval terms such as failure rate, mean time to failure, mean time to repair, and availability [66]. The reliability function is denoted as $R(t)$, which represents the probability that an item or device will perform the required functions under normal operation within an intended period of time. Several examples have been provided elsewhere of how to calculate the reliability model based on multilevel converters [59]. A model of The reliability assessment for MMCs has been presented, where reliability model of different SM arrangements are built and also the redundancy of SM is taken into account [67]. Reliability has been evaluated based on mathematical modelling considering both IGBTs and the capacitors of SMs [68].

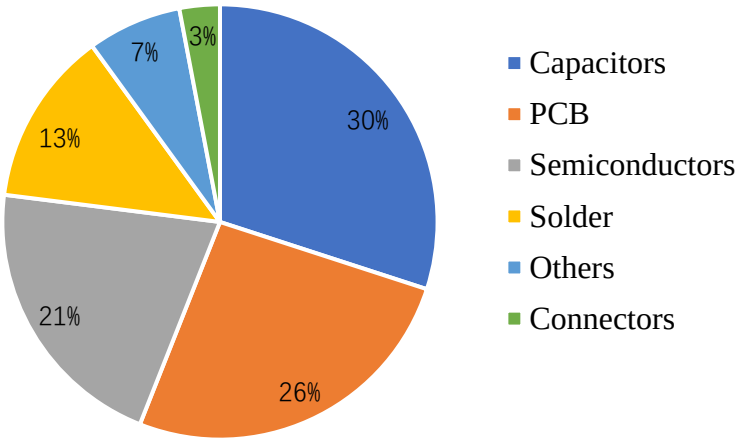


Figure 2.7 Failure rate of power electronics devices [69].

Figure 2.7 depicts the rate of failures of power electronics devices. This is clear that semiconductors and capacitors are highly likely to fail, particularly in MMCs, due to the nature

of their modular design.

A fault detection method for IGBTs with extra hardware implementation has been introduced [70, 71] where the collector current or gate voltage is the criterion that indicates the location of the fault. Several novel fault detection methods [57, 72-74] apply diverse approaches such as artificial neural network (ANN) and sliding mode observer (SMO) for SM fault detection. The voltage or current of the next sampling period can be predicted and compared with the measured values and then the conditions of semiconductors can be evaluated based on specific criterion [75].

The capacitor is a passive component which deteriorates over time and its capacitance and equivalent series resistance (ESR) gradually change [76]. Especially in electrolytic capacitors, this degradation is the main reason for component failure. At a certain point of degradation, the capacitor begins to malfunction, resulting increased capacitor voltage ripples [69]. In the conventional methods the voltage and current ripple are measured directly, and subsequently, the capacitance and ESR are calculated depending on the dominant frequency region of impedance [77], which requires additional filters. In a previous study[78], an AC signal was injected to the reference PWM and a digital band-pass filter was employed for signal extraction for a DC-link capacitor, after which the capacitance was calculated using the recursive least square (RLS) algorithm. A similar approach has been utilised for MMC sub-modules [79], where the same method was applied for a different application. A mechanism for redundancy control of the MMC has been introduced [80], which is applied after detecting faulty sub-modules. Methods of fault tolerance control of redundancy SMs have been presented [54, 57, 72].

2.5.3 Circulating current limitation

Circulating current is an actually not real current, and is defined as the current which circulates within the phase which is generated by the inner difference in voltage between phase units [13]. From Equations 2.10 and 2.11, it can be seen that the circulating current has no relationship to the AC or DC side voltage and is only determined according to the DC-link and arm voltages.

It has been pointed out that the second-order harmonic is the dominant component of the circulating current [81, 82], and the negative sequence components have frequencies twice those of the fundamental one, which leads to extra power losses. As a fictitious variable, it cannot be measured directly but is defined in Equation 2.10, and so its value is based on the upper and lower arm currents. Then according to Equation 2.13, it does not affect either the voltages or currents of either side [16]. From Equations 2.8 and 2.9, the circulating current is an additional component of the arm current which flows through each SM and resulting in extra voltage ripple [16]. Excessive power losses arise due to these extra voltage ripples, and so makes it is critical to introduce an additional control scheme to limit these extra ripples.

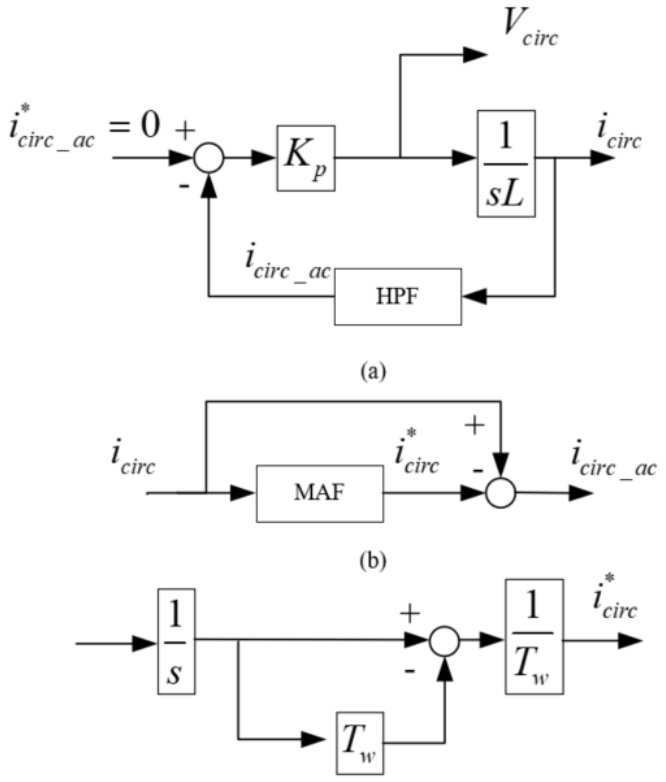


Figure 2.8 AC component elimination of circulating current by HPF/MAF [13].

The circulating current can be divided into two components: the AC component and the DC component. The purpose of the DC component is to help maintain the SM voltage at the reference value. The AC component is generated by the variation voltage between the upper and lower arms due to voltage oscillations in the cell capacitors, which consequently reduces the ripples but produces extra losses [13]. Several techniques for the suppression of circulating

current have been proposed [13, 36], as depicted in Figure 2.8. Firstly, for the elimination of the AC component a high-pass filter (HPF) is introduced to separate the AC component i_{circ} from the DC component, where the ideal AC component of the circulating current $i^*_{circ\_ac}$ is set to 0. The HPF can be replaced by one moving average filter (MAF) where T_ω is the window width of the MAF which is adjusted to 1/*f*, with *f* being the frequency of the output waveform, The reference AC component is set to the ideal zero to eliminate the oscillations in the circulating current.

As in the above analysis, the cascaded topology of the MMC applies the SM capacitor as the voltage source of the SMs, which differs from the situation in traditional 2-level and 3-level converters in terms of energy storage. Therefore, it is important to maintain the value of circulating current at an acceptable level, or even to further reduce it during the MMC's operation. The circulating current has been modelled and analysed elsewhere [36, 81]. The most and direct straightforward method of limiting the circulating current is to increase the arm inductance, but this will cause the system to become bulkier due to the greater volume of large inductors [36]. Indirect methods have been proposed [65, 83, 84] which apply a PI controller with the d-q frame transformation to eliminate the circulating current. The AC components can be eliminated based on the paralleled multi-frequency PR controllers to filter the current signals out of the particular frequency range [35]. The circulating current in the three-phase MMC can be transformed to the double-line frequency rotational frame, and then the second harmonic is eliminated [36, 85].

2.5.4 Voltage Balancing

Voltage balancing issues are deemed to be the most significant challenge, as for MMC the entire operation relies on it being accurate. Furthermore, it has a strong link to the other challenge associated with these systems. The objective of voltage balancing control in the MMC is to maintain the SM capacitor voltage at a level can be fluctuating around the value of V_{DC}/N. Based on the modulation techniques involved, the numbers inserted have three conditions: +1, -1, and remaining unchanged, where +1 and -1 mean that at least one SM needs to change its

state. The voltage balancing methods are designed to determine SMs to be either inserted or bypassed. Without properly balancing the capacitor voltage, a high circulating current might be flown through the arms, resulting in increased power losses and improper operation of the converter [36].

The open-loop control method is a scheme that modifies the PWM gate signals of the MMC switches. A previous study [86] has introduced a method that derives the pulse pattern of the gate signal directly under the fundamental switching frequency, and then applies it with the selective harmonic elimination PWM(SHEPWM) technique. The theory of the process has been explained [48, 49] whereby re-distributing the carrier waveform via the high-frequency components of the PSC-PWM of the arm current mean that the sorting algorithm is responsible for the reassignment of PWM signals. In other words, the driving pulses of semiconductors are allocated according to their contribution to the subsequent charges of the capacitors during every fundamental period. These methods require independent control adjustments for each SM, which results in greater computational complexity for MMCs with high number of SMs. However, system efficiency is decreased since the circulating current is higher under high-frequency conditions. As shown in Figure 2.9, the gate signal index is sorted in both ascendingly and descending sequences, and is then selected depending on the specific conditions involved, before the specific index is finally assigned to the SM to generate the gate signal, $g_{(i,j)}$, for the i-th SM of phase j.

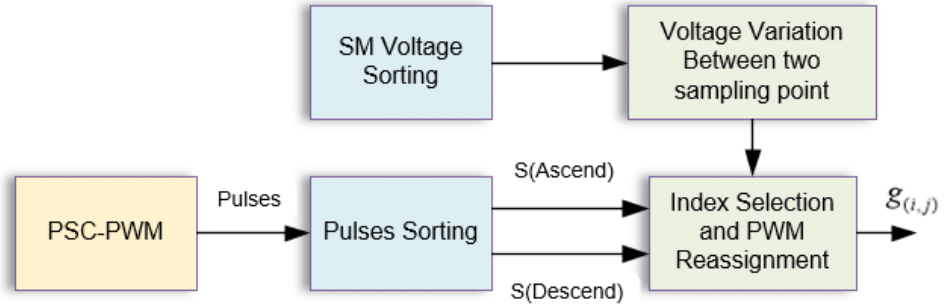


Figure 2.9 The diagram of open-loop control of carrier waveform redistribution[48].

The closed-loop control method was first introduced by Hagiwara [87, 88]. This type of control loop is based on two closed loops according to the PSPWM. The inner loop is the

average voltage control loop and the outer loop is the voltage balancing control loop, where V_C^* is the ideal average capacitor voltage value which is set to $\frac{V_{DC}}{N}$. The two control loops are both controlled by the PI controller, which implements various components of arm current to balance the energy, including the energy between the arms and SMs. The equivalent switching frequency is $2N \cdot f_C$, which is suitable for MMCs with fewer SMs.

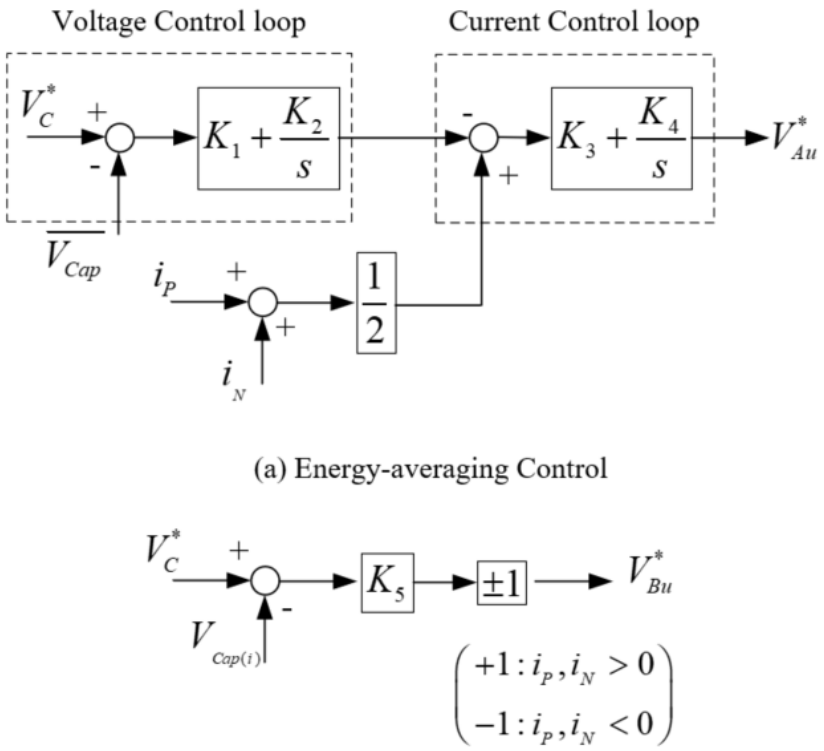


Figure 2.10 Diagram of closed-loop control[87, 88].

However, for MMCs with high numbers of SMs, the problem of high switching frequency continues to generate additional power losses. The primary disadvantages of this method are that each SM requires separated control loops and controllers, which clearly increases the degree of complexity when dealing with high numbers of SMs, and also there is a significant issue concerning the adjustment of PI for different control loops and SMs. The diagram of the proposed method is shown in Figure 2.10, where V_{Au}^* and V_{Bu}^* are the reference values of energy-average control and voltage balancing control respectively, and these are controlled and unified further to generate the control reference signals of every single SMs. In addition,

synchronising the clocks between different SMs is another serious challenge.

Predictive control is another direction which can be taken for voltage balancing. The amplitude of the capacitor voltage can be predicted for the coming sampling period, especially for MMC with low switching frequencies[21]. Determine the possibility of the SM changing its state varies depending on prediction of the SM voltage or the charge stored in the SM for the next control period or sampling period, which can be made by comparing the estimated maximum ripple value with a pre-set ripple value. Kamran has also proposed a predictive sorting [21], which calculates the inserted index based on the predictive value for the next sampling point, then based on the current and required number N to select the appropriate SMs to be inserted. The voltage boundaries comparison prior to the switching SMs selection has been introduced [56]. If the voltage of the next sampling point exceeds a specific boundary value, this switching event will be rejected, and the switching states will remain the same. Another method is to predict the charge stored in the SM of the next sampling point to determine the switching states [89]. The cost function has been applied to regulate the SM voltage according to a pre-set judgement condition [90].

The model of predictive control has been investigated further , by applying the weighting factors to configure the cost function [91]. The cost function is minimised by dividing it into three types related to AC current, circulating current and SM capacitor voltage. The reduction in switching states is subsequently combined to achieve the overall reduction in switching states. With regards to industrial use, the efficiency and effectiveness of these methods are still debatable. Firstly, capacitor degradation is not taken into consideration, which results in incorrect predictions; and secondly, the implementation of the cost function to calculate every SM at every sampling point brings an extra computational burden. However, this kind of method does provide another promising direction for future study.

There also exists a variety of control strategies regarding the voltage balancing of MMCs, and in this chapter, only some iconic methods are reviewed. A dynamic control method has been introduced based on feedback frequency, where a real-time adjusted factor is applied to the SMs,

which and then sorted using the adjusted factor [92]. Alternatively, a stored energy sorting has been introduced, which calculates the energy depending on the capacitor voltage as the reference signals, and then a closed loop is built up to balance each of the SM [93]. A phase-shifted carrier PWM (PSC-PWM)-based voltage balancing scheme has been proposed [94] which compares each SM's voltage with the average voltage of the arm and accordingly re-assigns the carrier waveforms of the SMs. This method allows the SMs with lower voltage to be switched-on for longer durations, whereas the switch-on period is shorter for higher voltage SMs. These methods help to reduce the switching frequency to some extent, but require individual controllers for each SM, which may lead to increased computational complexity when the number of SMs exceeds 200.

Overall, voltage balancing methods can be divided into two major categories of sorting-based methods and mon-sorting methods. Sorting-based algorithms are considered to be the most simple and effective for MMCs[30] as they exhibit very good performances in terms of average voltage regulation and voltage balancing between SMs. However, their primary disadvantage is that they generate large amount of unnecessary switching events. The core concept of this method is to switch on the SMs with the lowest voltage during the charging period, and SMs with the highest voltage during the discharging period. The voltages of the SMs are measured and sorted for every control period. In non-sorting related methods, each SM has an independent controller that helps to maintain the voltage ripples. This chapter mainly reviews the non-sorting control methods, whereas the next chapter focuses on the sorting-based methods.

2.6 Chapter Summary

This chapter first provides a brief review of the control and operation of MMCs. Subsequently, a comprehensive analysis is presented of the challenges associated with MMCs. Many studies have focused on overcoming the challenges, and there are reviewed in this chapter. Amongst all of the challenges, voltage balancing is the most important as it directly affects the output waveform quality and can affect other areas such as circulating current. Nowadays, one of the

most popular voltage balancing algorithms is the sorting algorithm due to its simplicity, good compatibility and ability to reduce the capacitor voltage ripple. Meanwhile, there are also some well-known non-sorting methods. Finally, the potential application areas of MMCs are briefly introduced in this chapter. For MMCs, the best approach to the identification of a control method that is both highly effective and incurs low costs has yet to be comprehensively investigated.

Chapter 3. Literature Review of Sorting Algorithms

3.1 Introduction

This chapter presents a comprehensive up to date literature review of sorting algorithms. The chapter commences with an in-depth analysis of the characteristics of the conventional sorting algorithm. Then, the implementation of this algorithm is briefly described in terms of both the modulation and selection stage of voltage balancing. Issues relevant to the of the sorting algorithm for voltage balancing are then addressed, where the nature of the algorithm with the associated high switching frequency and computational complexity creates problems for the operation of the MMC system.

Several solutions are available to overcome these problems, thereby improving the sorting algorithm, and these are reviewed in this chapter. One solution is to focus on improving the sorting algorithm itself, since the conventional sorting algorithm also known as bubble sorting is only one particular type of sorting algorithm. Therefore, the potential approaches which could be used to modify the sorting sequences in order to minimise the switching frequency and computational costs need to be identified. Another solution concentrates on the reduction of the numbers of the switching events based on only applying the sorting algorithm for selected SMs, since if there are fewer sorting events, then the switching frequency will be lower. Finally, MMC applications and potential future research directions are summarised in this chapter.

3.2 Principle of the Sorting Algorithm

The sorting algorithm is still one of the most widely used techniques employed for voltage balancing. The sorting process is explained in detail elsewhere [30, 95], and a flowchart of the conventional sorting algorithm is depicted in Figure 3.1. Due to the increased unnecessary switching generated by sorting algorithm, it has become the primary concern for its use in voltage balancing, particularly when the number of SMs is high. Since the comparison and execution times between SM are increased exponentially with the number of SMs, this also

leads to extra computational complexity. Hence, to resolve these issues it is essential to improve the performance of the sorting algorithm. Much existing research focuses on this area and proposes means of achieving enhanced balancing performance.

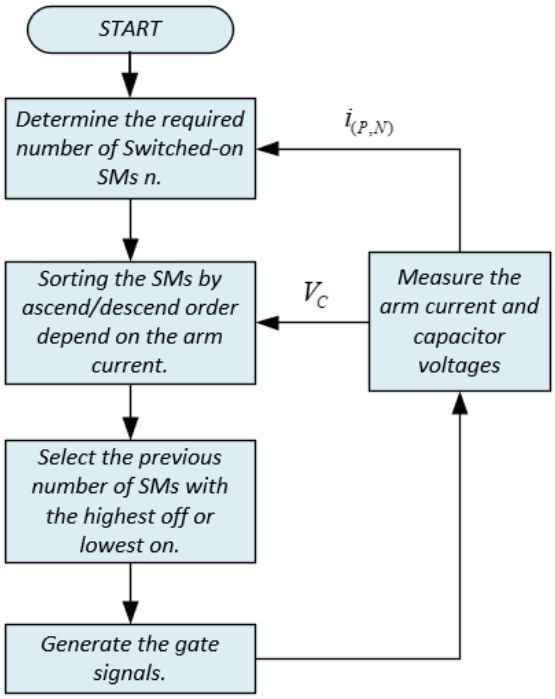


Figure 3.1 Flowchart of the conventional sorting algorithm

The conventional sorting algorithm or so-called bubble sorting algorithm was first described by Saeedifard [30]. Since then, it has attracted enormous interest, and many methods have been proposed to improve its performance. The basic concept of the bubble sorting algorithm is to select the specific SMs to be inserted or bypassed depending on the direction of the arm current. According to Figure 3.2, the operation of the sorting algorithm can be divided into two steps:

1. Determining the required number of SMs to be inserted n using modulation techniques. The main modulation methods are phase-shift PWM (PSPWM), level-shift PWM (LSPWM) and nearest level control (NLC). For LSPWM and PSPWM, the sum of the required inserted number of the upper and lower arms is equal to the total number of SMs in one arm *N*.

$$n_{up} + n_{low} = N \tag{3.1}$$

The level of output is determined by the required inserted number for the upper and lower arms, since the upper arm number contributes to negative levels of the output, and the lower arm number contribute to the positive levels.

2. The second step is the selection step. Based on step one, the output level has been determined by the modulation methods before actual balancing the capacitor voltage of the SMs. The algorithm generates the gate signals of SMs while the total numbers of the inserted signals are determined by the modulation signals, and this represents the biggest difference from other converter control methods. If the arm current is positive, the capacitor voltage of the inserted SMs are thereby increases, and then the n SMs with the lowest voltage will be switched on and the rest will be switched off. Conversely, if the arm current is negative, the algorithm will select the n SMs with the highest voltages to be switched on and the rest to be switched off.

Inspired by the above two steps, voltage balancing control methods can be divided into two widely recognised stages: the modulation stage and the SM selection stage. Improvement can be implemented either during the modulation stage or the SM selection stage.

The modulation stage differs from open-loop control as it does not re-assign the PWM waveform of the SMs. Instead, it calculates the required inserted number in different ways using several sampling periods which slows down the SM selection stage. Another solution based on these two stages has been proposed which referred as the fundamental-frequency balancing method [56]. It only calls for the information of required numbers of changes Δn only during the specific phase angles such as 90 and 180 degrees. The general concept is presented in Figure 3.2. During the modulation stage, the measured capacitor voltages of phase *j* are stored prior to sorting, and subsequently the index list is generated. This list varies depending on the sampling frequency. The index list is then sent to the sorting stage to obtain the gate signal, $g_{(i,j)}$. This method slows down the rate of change of the Δn to reduce the switching frequency, but the longer sampling intervals increase the voltage fluctuation. Also, the dynamic response performance is reduced because some key modulation information has a high possibility to be

ignored. In addition, a hybrid strategy that predicts the value of the next sampling period is introduced, which requires an extra prediction procedure prior to voltage balancing, hence increasing the computational complexity.

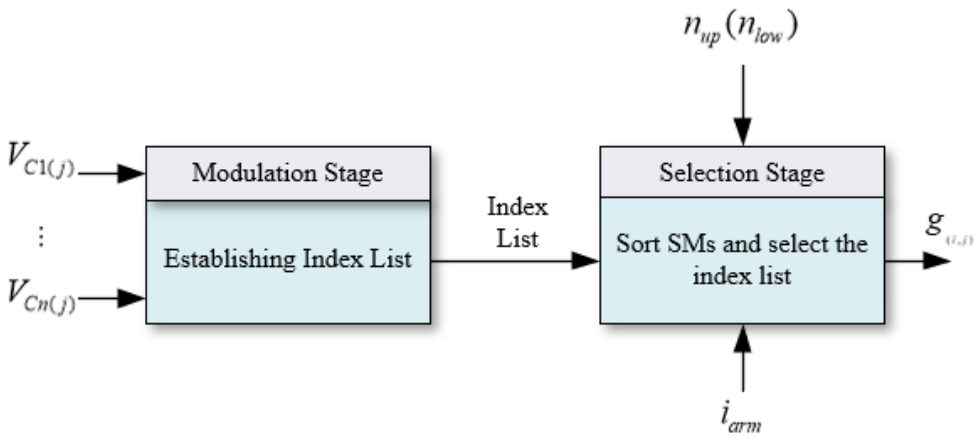


Figure 3.2 General framework of two stage method proposed by[56].

3.3 Sorting Algorithm Optimisation

The conventional sorting algorithm (CSA) has been recognised as ease of implementation, which is simple and has good compatibility with most modulation methods. However, the sorting of all SMs in every sampling period results in many unnecessary switching events, which leads to a very high effective switching frequency, and therefore higher power losses. Studies aiming to improve it can be classified into two categories. The first is based on complexity reduction, aiming to reduce the computational costs to increase the operation speed of the algorithm. The second category attempts to reduce the switching frequency through an optimal arrangement of distribution of the switching events.

3.3.1 Reduction of the computational cost of sorting algorithms

The sorting algorithm requires a long execution time when dealing with high number of SMs because the calculations required for the algorithm increases exponentially. Nowadays, the most advanced processor can deal with up to 4000 SMs simultaneously in a fixed 20kHz sampling period. However, for real MMC projects, the processor is also responsible for many other tasks, which may lead to insufficient processor resources for the system. The motivation for reducing

computational complexity because in high-frequency applications, the available execution time is very limited, and so reducing the computational complexity is extremely important. Secondly, for high number of SMs, an algorithm involving less computational complexity requires fewer processor unit, regardless of the limitation of the processor PWM channels, thereby leading to reduction in manufacturing cost in real projects.

The most popular methods to reduce the computational complexity are based on the grouping-up concept, which reduces the numbers of SMs involved in the control algorithm. Then the calculation and comparison will be distributed into groups. The Prime Factorisation Method (PFM) was introduced to group the SMs level by level until the final groups only contain 2 to 3 SMs to sort the sequences, after which the elements within the final groups are sorted [96]. This method reduces the comparison times (CT) but cannot increase the quality of the output waveform. The voltage balancing arrangement of PFM is illustrated in Figure 3.3. The Shell Algorithm has also been proposed to replace the conventional bubble sorting algorithm [97], and this has less steps for the sorting, which subsequently helps increasing the sorting efficiency. However, the shell algorithm is not as stable as CSA, which causes difficulties in voltage balancing.

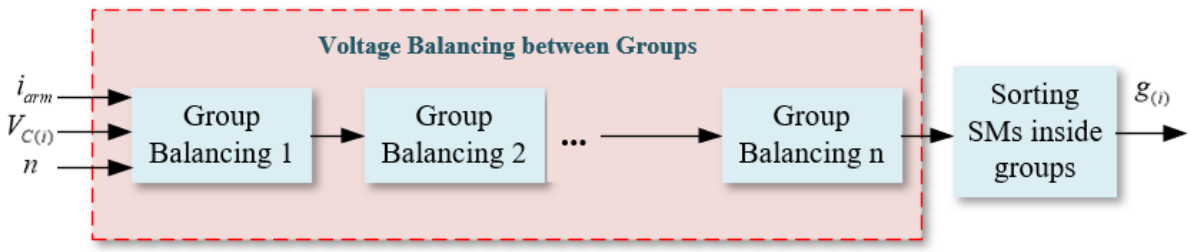


Figure 3.3 Flowchart of group sorting control[96].

The SMs can also be assembled evenly into several groups, and then the required inserted number n is individually assigned to determine the gate signals [98]. However, its effectiveness requires further experimental validation. A quick sorting algorithm has been introduced for MMC voltage balancing after the SMs have been divided into inserted and bypassed groups [99]. This quick sorting algorithm has good efficiency and less complexity, but the increased

ripples limit its application and it still requires further investigation.

A complexity reduction method is proposed, which introduces a multi-layer controller scheme, where another controller layer is inserted between the main and separated SM controllers [100]. This additional controller is a called value controller which is responsible for 6 SMs, so that the control information can be distributed into three controller layers, and the main diagram is shown in Figure 3.4. This scheme not only reduces the complexity of the control of the MMC, but also limits the usage of communication wires. However, synchronisation between different controllers requires significant effort, and the system does not support reductions in switching frequency.

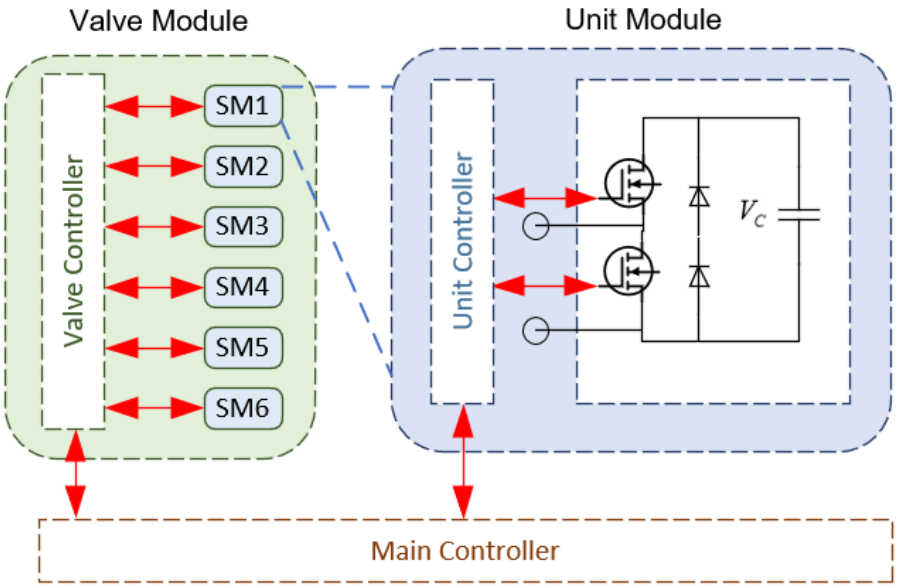


Figure 3.4 Diagram of the multi-layer controller scheme.

3.3.2 *Reductions in the switching frequency of sorting algorithms*

The second category aims to reduce the switching frequency, since switching losses remain a big challenge for power devices with the MMC topology. The core concept is to avoid extra sorting actions by a better arrangement of sorting events distribution. The primary objective of the CSA is to minimise variations in voltage variations between SMs. This essentially makes the capacitor voltage identical or very close to each other in every sampling period. However, for voltage balancing, the main purpose is to maintain voltage ripples within a certain range, and an identical voltage is not necessary. Therefore, the implementation of CSA will lead to

unnecessary switching caused by this additional action. Several studies have proposed strategies for the selection and distribution of switching events to avoid unnecessary switching actions, thus eventually reducing the switching frequency.

Compared to the CSA which is straightforward, a new variable is introduced to the sorting stage has been implemented [36]. The SMs are selected not only according to the measured values of the arm current and capacitor voltage, but also the switching states of SMs in the previous sampling period. The SMs in inserted states maintain their previous signals, whilst the SMs with previously bypassed states are considered to change their states in the current sampling period. Switching occurs only when the required inserted number n changes, which is referred as Δn where its accuracy relies heavily on the modulation signals. A diagram of the proposed technique is depicted in Figure 3.5, the selection of switching strategies is conducted according to the number Δn. However, this method helps to reduce switching frequency, it is not applicable for low carrier frequencies due to higher voltage ripple involved.

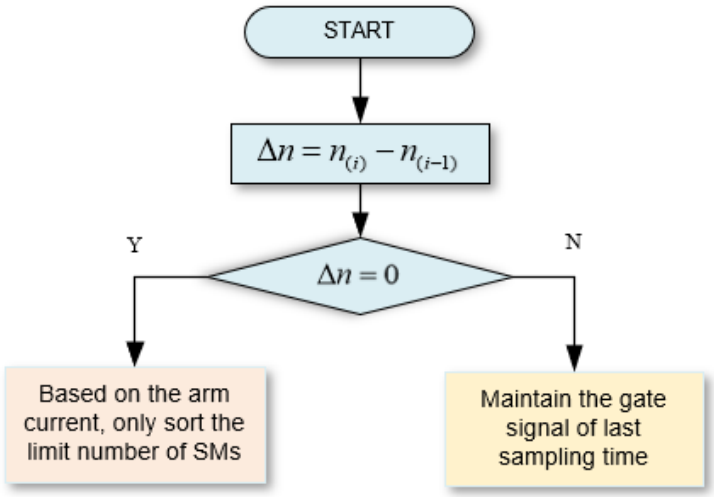


Figure 3.5 Diagram of reduced switching frequency method [20].

The maintaining factors method introduces to balance the virtual capacitor voltage, where the measured voltage value of SMs are multiplied by different factors [53]. Then, the sorting process is based on virtual capacitor voltages. A diagram of this method is illustrated in Figure 3.6, where SMs with higher or lower values are multiplied by the higher factors to ensure that they have a greater possibility of being involved in the switching; thus convergence to the

desired voltage value is faster. The higher factors it selected, the greater the resulting ripple and variation between SMs, but a lower switching frequency it is achieved. A similar idea has been proposed, where the virtual voltage is assigned by adding an offset to the capacitor voltage based on the PSPWM modulation signal [95]. The purpose of virtual voltage sorting is to define the SMs with distorted voltage as they have a higher value which results in more frequent voltage changes. Broadly speaking, the core concept is to increase the probability of the SMs maintaining their original states. This concept helps SMs with higher or lower values to have a high probability of changing states, thus reducing unnecessary switching events. However, this requires extra calculations of virtual voltages prior to achieving balancing, and furthermore, each SM must be compared to all others in every sampling period which increases the demand for computational resources.

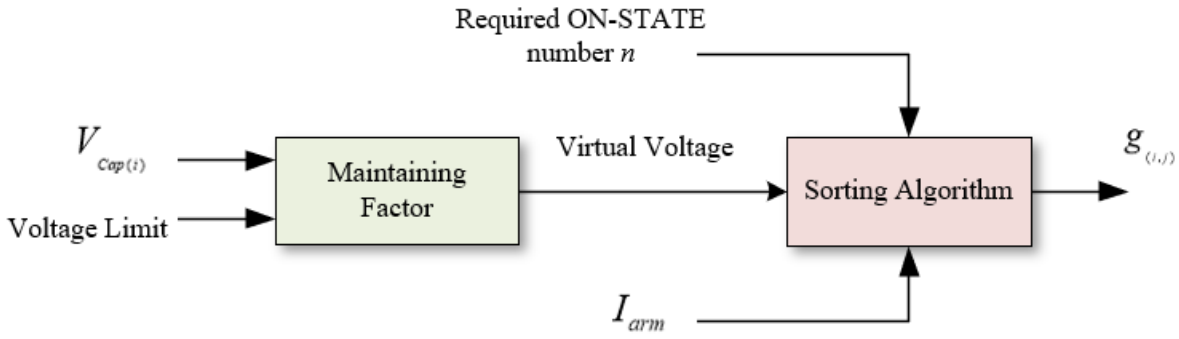


Figure 3.6 The diagram of virtual capacitor voltage method [53].

For the purpose of the simplification of the sorting algorithm, a dual sorting algorithm has been presented [101] which is a sensor-less method that sorts the increment of the voltage of each SM instead of the arm current. Then it re-allocates gate signals with the help of traditional capacitor voltage sorting for PSPWM. This method has the ability to reduce the switching frequency, but the incremental calculations and sorting brings extra computational burden to the system.

The above methods are fundamentally based on the CSA, which itself continues to produce extra switching actions and increased computational complexity. A grouping idea for the control strategy has been implemented by dividing the SMs into several groups according to different

criteria [98]. Therefore, the algorithm no longer needs to sort each SM in every sampling period, but rather the sorting actions only occur in certain groups. In this method, N SMs are evenly divided into $N/2$ groups and a serial number is assigned to each group. The serial number only changes when the measured deviation voltage exceeds the limit, and then only the groups with changed serial numbers must switch their states. A new group-up method that has been applied to group-up the SMs evenly into several groups, and uses conventional sorting to sort the groups [96]. Then, the groups with the highest or lowest values go to the second stage of sorting. This helps to limit the sorting to within one or two groups, and subsequently only two or three sets of SMs are sorted instead of high number of SMs. This method can reduce computational complexity and cost significantly, since the computational complexity of sorting algorithm increases exponentially with the number of SMs.

The group-up idea has been further applied by using a reference tolerance band which is referred to as the extremist voltage ripple range [21]. The SMs only change their state when their voltage reaches the boundaries of the band. This method has large ripple compared to CSA, and thus the voltage difference between arms increases which leads to high circulating current. Another grouping idea has been proposed which sorts the upper and lower arm groups together, then employing a cost function to determine the optimum combinations [92]. This computational cost is based on the number of groups T, and then T times the value of the cost function is calculated to evaluate the minimum group combination.

3.3.3 Hybrid improvement for sorting algorithms

The improvement of sorting not only relies on reducing switching frequency, but also decreases the computational complexity. Mathematical models for computational complexity reduction have been provided where an optimised sorting algorithm is applied [96, 97]. A method has been proposed for makes use of the characteristics of the field programmable gate array (FPGA), along with a new set of SM selecting rules [102], which manages to sort the SMs in parallel to reduce computational complexity. Another FPGA method has been suggested , where the SMs are grouped in each sampling period and extra switching events are reduced, which make full

use of the characteristics of FPGA that controls the gates simultaneously, thus decreasing both the time complexity and the switching frequency [103]. The hybrid method creates a state decision optimisation model using the Taboo Search Hard Optimisation Algorithm [104]. It searches for the optimised objective conditions in every sampling period to reduce the computational complexity; however, the reduction of switching frequency is not very effective. Therefore, the demands still exist for better designs of voltage balancing methods.

3.4 Comparison of Major Voltage Balancing Methods

A comparison of the main voltage balancing control methods is listed in Table 3-I, where computational complexity, ripple performance, sorting and reduction in switching frequency are highlighted.

Table 3-I Comparison between the main control methods of MMC.

Methods	Computational Complexity	Capacitor Ripple	Is Sorting Algorithm Applied?	Switching Frequency Reduction
Reduced-switching frequency[36].	Medium	Medium	YES	Very High
Closed-loop control[87, 88]	High	Low	NO	Medium
Factor balance[53]	High	Medium	YES	High
Slow-rate Strategy[56]	Medium	High	YES/NO	Medium
Hybrid strategy[56]	High	Varies	YES	Medium
Fundamental-Frequency strategy[56]	Low	High	NO	Low
Predictive Controller Based Method[105]	Reduce the execution time	High	NO	Low
Tolerance Band[21]	High	Varies	YES	High
Modified Method[55]	Medium	High	YES	Medium
Fundamental Frequency Sorting Algorithm[101]	Medium	Medium	NO	High
A novel sorting[98]	Medium	Medium	YES	High

From the table, the sorting algorithm has been applied in most of the control methods during the SM selection stage due to its effectiveness and ease of implementation. It can be concluded that the effectiveness of the switching frequency reduction varies from very low to very high depending on the methods employed, but most methods proposed so far are unsuccessful in reducing computational complexity.

3.5 Chapter Summary

This chapter has provided a comprehensive review of the voltage balancing control of MMCs, particularly focusing on methods related to sorting algorithms which have advantages such as cost-effectiveness and ease of implementation in the voltage balancing. However, the excessive unnecessary switching is the primary concern with the conventional sorting algorithm due to the massive extra power losses involved. Furthermore, the issue of computational complexity where there are high numbers of SMs cannot be disregarded since the sorting process itself creates a large computational burden for the processor. Numerous studies which aim to improve the performance of the conventional algorithm have been reviewed and classified, and some effective ideas have been analysed. The solutions offered can be divided into two main categories, and some of them have shown good progress and outcomes in improving the sorting algorithm. However, the problems of high switching frequency and computational complexity are yet to be fully addressed. This situation necessitates greater efforts and more comprehensive research into sorting algorithms.

Chapter 4. Range-based Index Selection Scheme

4.1 Introduction

This chapter begins by analysing the conventional bubble sorting algorithm, and its advantages and disadvantages are evaluated. Then, based on the analysis, the causes of unnecessary switching are investigated. In order to overcome the problems of conventional bubble sorting, a method called the Index Selection Method is introduced, which determine the gate signals by selecting the index based on different conditions. The index is defined a one-dimensional binary matrix, where the element '1' means to switch on the corresponding SM and '0' means to switch it off. This selection process is designed mainly to reduce the frequency of switching.

There are three options: maintain the existing gate signals, conventional SM voltage sorting, and virtual voltage sorting with the use of coefficients. The conditions are determined according to the defined ripple tolerance band, and the selection is based on the number of SMs that are within the tolerance band. This is comprehensively analysed in this chapter. In addition, the pre-defined tolerance band is also suitable for virtual voltage sorting. Finally, the proposed technique and its effectiveness in switching reduction is validated using MATLAB/Simulink.

4.2 Conventional Sorting Algorithms

SM balancing is the primary used technique in the MMC control system. In an ideal situation, the parameters of the SMs would be identical and the capacitor voltages of all the SMs would be maintained at V_{DC}/N without any extra balancing method being required. However, due to the nature of MMCs, there will be unbalanced voltages between SMs, and hence the quality of the output waveform is inevitably distorted. Voltage balancing control, in other words, is a method of re-distributing the total energy inside the arm. Compared with the traditional VSC topology, each SM requires a separate carrier waveform which results in limitations when the number of SMs is very high.

The fundamentals and flowchart of the conventional sorting algorithm (CSA) have been presented in Chapter 3. This chapter analyses the causes of unnecessary switching and describes the desired control method. These switching events occur in every sampling period, generating switching losses and causing harmonic distortion. Ripple voltage regulation is another critical issue when selecting an appropriate voltage balancing method for the system. The ideal voltage balancing method should maintain the voltage at a specific value with minimum ripple with the lowest switching losses. In addition, the optimum design of a voltage balancing method should take the computational complexity involved into consideration.

4.2.1 Expectations of voltage balancing methods

According to the analysis in previous chapters, an effective design for a voltage balancing method should encompass the following characteristics:

1. Low switching frequency, and lower switching losses.
2. Low computational complexity, leading to a low computational burden for processing.
3. Good ripple performance and output waveform quality.

Meanwhile, the switching frequency of SMs can be divided into necessary switching and unnecessary switching. The frequency of unnecessary switching has an impact on fluctuations in capacitor voltage, which is undesirable. The basic concept of the bubble sorting algorithm is to select SMs with the highest or lowest values to be inserted or bypassed depending on the direction of the arm current, resulting in an equal voltage level being achieved in the SMs. The CSA generates the required signals that directly control the gate signals of power switches in SMs. The numbers of inserted signals and bypassed signals are determined by the modulation signals, and this represents the biggest difference in comparison to other converter control methods. The CSA is popular among all types of MMC control because it only requires the information of instantaneous voltage current of SMs, which means that it is simple and has good compatibility with most modulation methods. However, sorting all SMs during every sampling period results in many unnecessary switching events, which leads to a very high

effective switching frequency and therefore higher power losses.

4.2.2 Investigation of unnecessary switching

Although the bubble sorting can effectively balance the capacitor voltage between SM with low harmonic distortion, the main problem is the computational complexity it entails. Bubble sorting compares each SM with all others in every sampling period. In other words, the SMs are constantly involved with switching events at every period, and so unnecessary switching is generated during the bubble sorting process. Furthermore, there is a positive correlation between increased switching and higher switching losses. In a practical project, where numbers of SMs are very high, this cannot be disregarded. Therefore, the primary target in optimising the sorting algorithm is to avoid the unnecessary switching.

Unnecessary switching events are demonstrated in Figure 4.1 (a), where an illustrative example of an MMC with 3 SMs per arm is presented, and the modulation method provides information about the required inserted number n which is equal to 1 for the next 5 sampling periods under the condition of positive arm current. For CSA, SM2 and SM3 with similar voltage levels will change their switching states alternately until they reach the desired value. Most of those switching events are unnecessary switching events. Since the purpose of the control method is to balance the SMs so that they fluctuate within the pre-defined range, the only necessary event in this condition is to switch on the SM with the lowest value regardless of the voltage levels of adjacent SMs. Therefore, in this case, there are 4 switching pulses for SM2 and SM3 in total, but three of them merely maintain them at same value. In conclusion, the objective of reducing unnecessary switching events mainly relies on providing flexibility to SMs to allow them to fluctuate within an acceptable range instead of all kept at an identical value. The Figure 4.1 (b) illustrates a possible solution to avoid such unnecessary switching events, where the SM with the lowest voltage is kept inserted until voltage level reaches a certain value for the next 5 sampling periods. Since the other SMs are bypassed in the same period, therefore the total switching event in this case is only 1 pulse, and the other 4 unnecessary pulses are eliminated. A simple comparison with Figure 4.1 (a) shows that one can

easily see that there an 80% reduction in switching event.

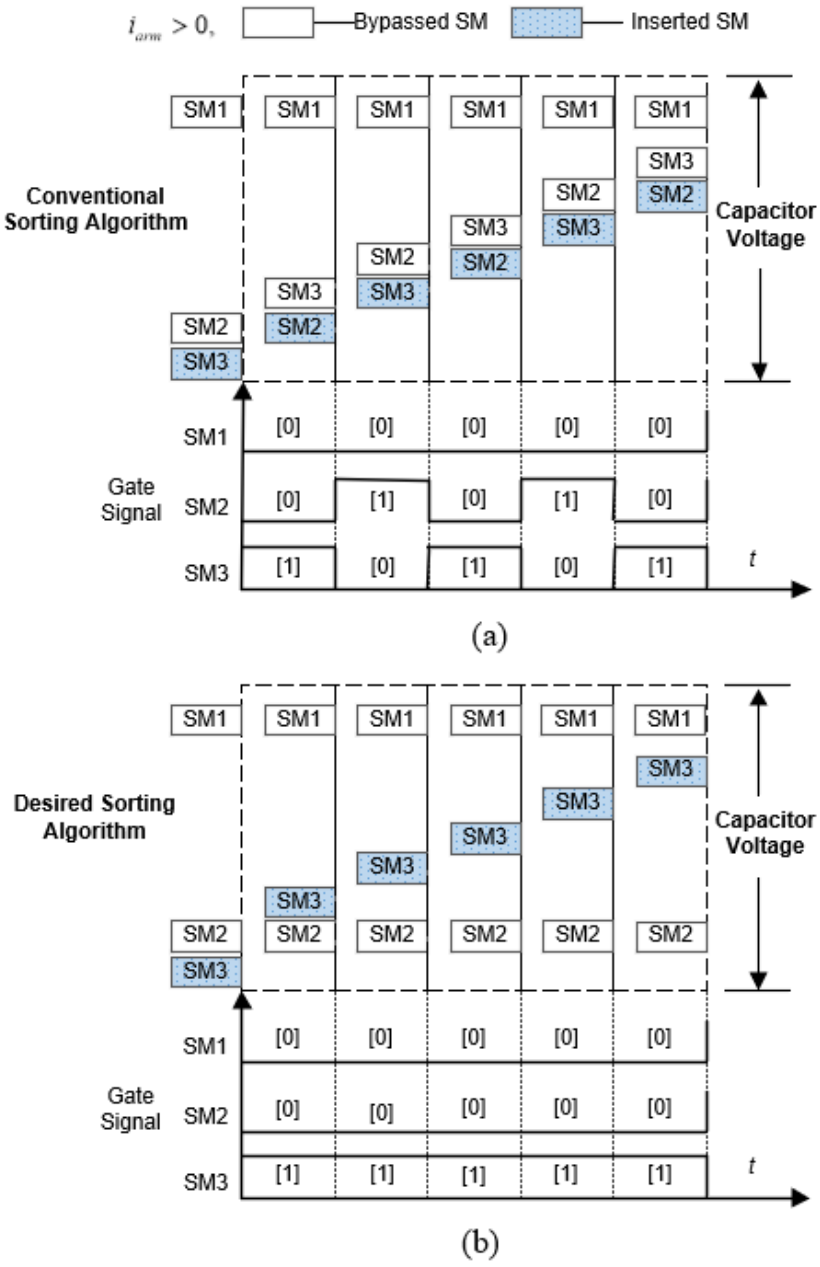


Figure 4.1. (a) One condition of the origin of unnecessary switching events. (b) Same condition with the desired control scheme.

However, if the SM maintains it inserted state for too long time, this will result in increased ripple voltage as well as the conduction loss. Meanwhile, the approach used to reduce unnecessary switching means identifying the SMs which are not involved in sorting actions. Therefore, the purpose of improving the sorting algorithm is to achieve a better switching arrangement with the similar output quality.

4.2.3 Complexity of CSA

In conventional bubble sorting with *N* sub-modules, the comparisons required for sorting will be N^2, which produces numerous useless iterations during operation. When CSA is employed with *N* SMs, clearly extra calculation is required to perform the sorting. This produces numerous useless comparison iterations during the operation. Therefore, the number of comparisons executed by the processor in one sampling period is[96]:

$$T_0 = 1 + 2 + 3 + \cdots + N = N(N-1)/2 \tag{4.1}$$

where T_0 is the comparison time of the conventional sorting algorithm. Comparison time is defined as the total number of times that the value two adjacent SMs are compared during the process of sorting of all SMs in one arm. According to Equation 4.1, the system will sort each SM in every sampling step. In this thesis, the computational complexity is simplified and evaluated by comparison time (CT), and the computational complexity becomes huge when the number of SMs is high. An improved sorting algorithm is introduced in this chapter for the purpose of reducing the computational complexity and switching frequency.

4.3 Introduction to the Index-based Sorting Algorithm

This chapter proposes a new control method based on the sorting algorithm called the Range-based Index Selection Method (ISA). For the purpose of the reduction of switching frequency, this method applies a different rule during the SM selection stage. The algorithm is applied after the required inserted number *n* is determined by modulation techniques, and a pre-defined tolerance band (TB) is set before SM selection. Meanwhile, this pre-defined TB, also called the ripple TB, is defined as **X** and limits the capacitor voltage within an acceptable range of value, thus helps to improve the performance of voltage balancing. **X** is set normally from 5% to 10% of the reference value depending on the application. The proposed ISA measures the instantaneous value of capacitor voltage $V_c(t)$, and arm current $i_{arm}(t)$, as the key parameters for voltage balancing, which is the same as with the CSA.

Additionally, the change of the size of *n* from the modulation stage between two

consecutive sampling periods is referred as Δn, and the number of SMs within the range **X** are considered as the conditions for selection. Finally, the index of the previous sampling period ***R***, the index from the conventional sorting algorithm ***B***, and the index from the virtual sorting algorithm ***F*** are taken into account as index choices. The main purposes of this approach are:

1. To maintain the SMs within the TB so as to retain their gate signal as far as possible.
2. To cause the SMs outside the TB to converge to the TB faster than the case with the CSA.

The former purpose helps to reduce the number of unnecessary switching actions, whilst latter focusing on capacitor voltage ripples and improving dynamic performance.

4.4 Index Determination and Selection

The first step is to compare the SM voltages within the required range, to classify them in three categories:

- **Q1** if the voltage of the SM is below the lower boundary of the range,
- **Q2** if the voltage of the SM is within the range,
- **Q3** if the voltage of the SM is above the upper boundary of the range.

The second step is to update the index of the previous sampling period ***R***. The algorithm implements the gate signal ***G*** of the previous sampling period, and replaces the ***R*** of the current sampling period with ***G***. This process is executed continuously and the only computational resources it requires involves data storage.

The third step is to define the index ***B***, where the normal sorting algorithm is applied to determine the gate signal index. The algorithm does not need to calculate ***B*** prior to commencing selection.

Finally, the defined range **X** helps to determine the index ***F*** as well as the virtual sorting algorithm mentioned in Chapter 2. The proposed ISA only marks the SMs outside the boundaries of **X** with the coefficient α, which is similar to a previous study [53], and the ISA is simpler and easier to implement, because it ignores the states in the previous sampling period.

The purpose of the ISA is to force the SMs within the **X** to become less 'active', because some small capacitor voltage fluctuations are acceptable in the MMC system, and the SMs outside the **X** to converge to the permissible ripple range rapidly. The principle of the determination of index ***F*** is illustrated in Table 4-I.

Table 4-I Determination of Index ***F*** for ISA.

Steps	Actions
1. Charging/discharging process judgement	$I_{arm} \geq 0$, Charging process $I_{arm} < 0$, Discharging process
2. If charging, apply the coefficient to SMs outside **Q1**	For i from **Q2** and **Q3** $V_C'(i) = V_C(i) \cdot \alpha$
3. If discharging, apply the coefficient to SMs within **Q3**	For j from **Q3** $V_C'(j) = V_C(j) \cdot \alpha$
4. Depending on the required inserted number n, sort $V_C'(i)$ to obtain index ***F***	Switch on first *n* SMs: If charging, sort ascending. If discharging, sort descending.

The concept of the ISA is to select the best index choice for voltage balancing in every sampling period. The coefficient α is used to describe the ability of an existing SM to maintain its switching state. The higher the value of α, the more involvement with sorting and the faster sped to converge to the permissible ripple range. Normally, α is set at between 1 to 1.1 to ensure that it will not cause the voltage ripple to exceed the limit. After determining all three potential indexes, one out of the three choices is selected as the final index for the gate signal, depending on different conditions. In addition, the selected index for the current sampling period will be treated as the index ***R*** for the next sampling period. Overall, the proposed technique aims to reduce switching frequency, and so those SMs which are within **X** should have less possibility to change their states. The detailed steps in the ISA procedure are

demonstrated below.

1. If the number of elements inside **Q2=*N***, i.e. If all the SMs are inside the **X**, all of the SMs tend to maintain their states when $\Delta n = 0$. So, the index ***R*** is applied to keep all the SMs within the TB.

2. If the number of elements inside **Q2=0**, i.e. all the SMs are outside **X**, the gate signal index is updated with Index ***B***, which essentially the CSA is taking the responsibility of voltage balancing.

3. If the number of elements inside **Q2** is between 0 and *N*, the gate signal index is updated with the Index ***F*** to balance the SMs. Thus, the SMs with extreme values will have higher convergence speed towards **X**, whereas the SMs inside **X** have higher possibility to maintain their existing states.

The process for producing indexes in the ISA is shown in Figure 4.2. Taking a 4-level MMC during the charging period as an example, at the sampling period ***t***, three different situations are depicted on the left-hand side of the graphic. If *n*=0 this implies that the required inserted number is kept at *n.* So, the index ***R*** of (***t+1***) is maintained at its index of ***t***, while the index ***B*** and ***F*** use conventional sorting to identify the lowest *n* SMs to be switched on. Thus, the selections of indexes for ISA are generated, and the final stage is to choose one of them to be the gate signal index.

Therefore, the function of index ***B*** is to inherit the ability of the CSA to achieve good capacitor voltage balancing and a quick dynamic response, whilst index ***R*** helps to avoid unnecessary switching events and index ***F*** is responsible for ensuring that the SMs remain within the acceptable voltage range.

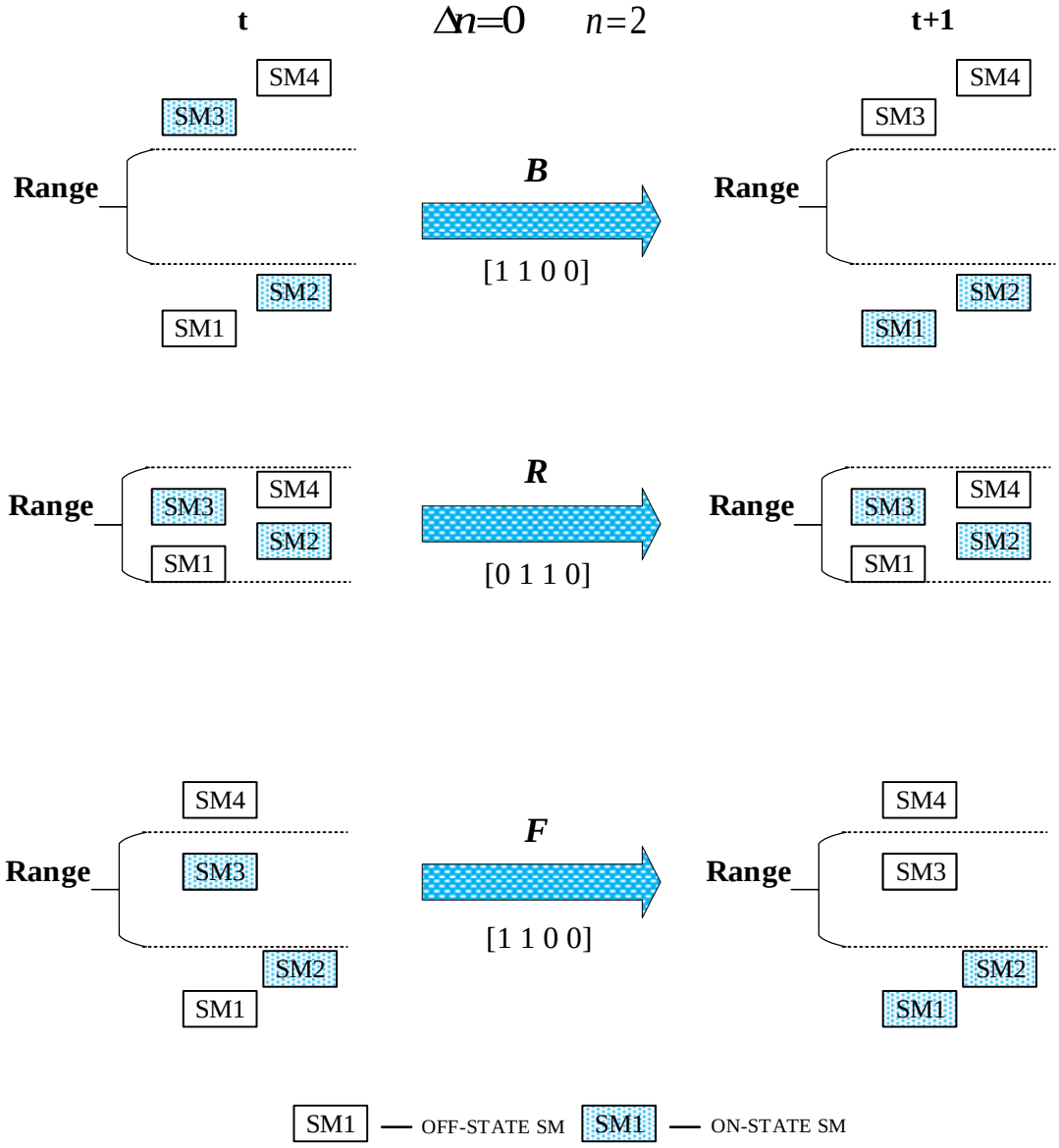


Figure 4.2 Indexes generation of Range-based ISA.

4.5 Characteristic of ISA

A flowchart of the proposed range-based ISA is depicted in Figure 4.3 This concept partly reduces the switching frequency in two main ways. Firstly, the usage of the sorting algorithm is reduced while Δn=0, and secondly is the virtual voltage sorting sacrifice the total uniformity of capacitor voltage, instead of allowing a small ripple to trade off against the reduction in switching frequency.

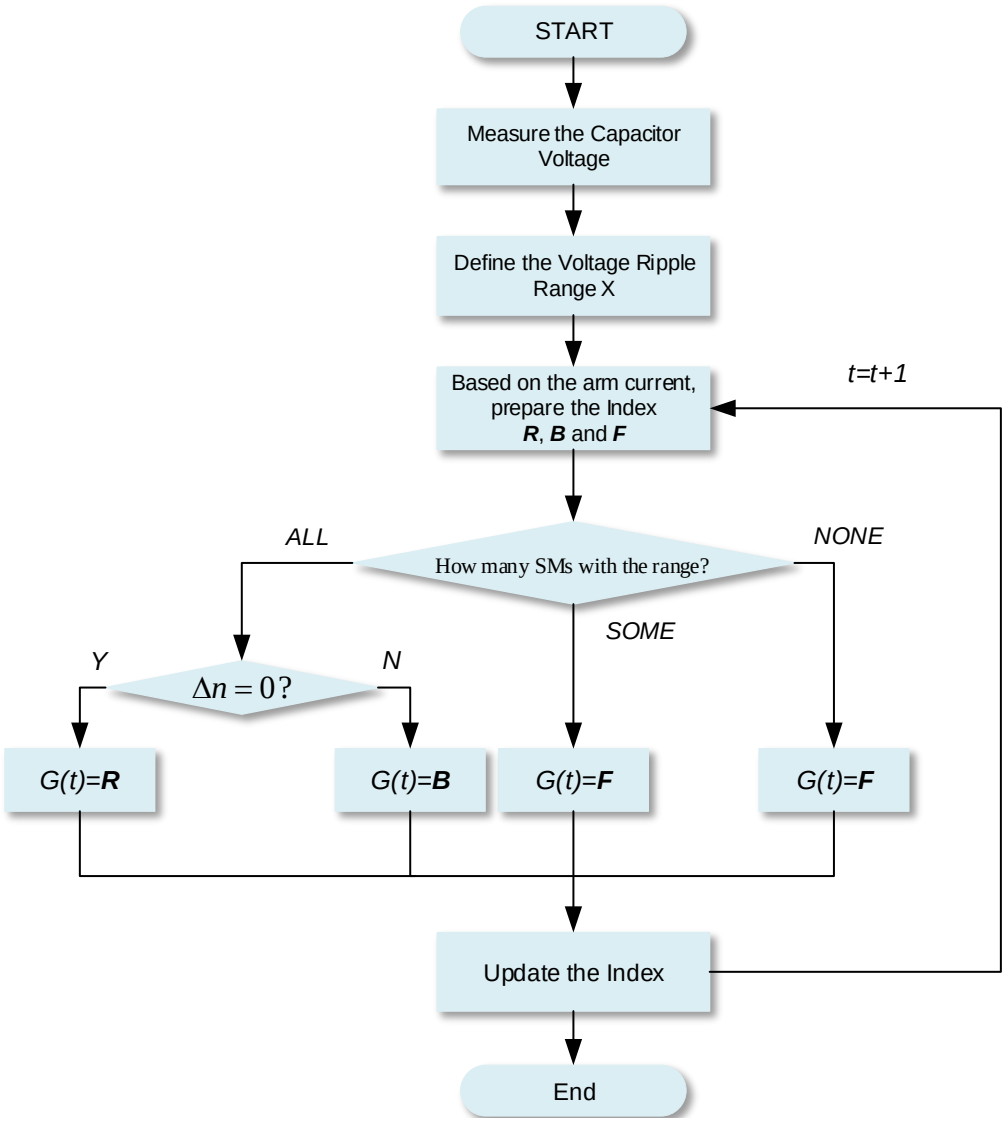


Figure 4.3 Flowchart of proposed ISA.

In contrast to the CSA, the sorting algorithm in this context is not currently widely utilised. Instead, it is used depending on the number matrix required. If the average possibility of a switching event occurring across a certain sampling period is D_p, it means that in each sampling period, the SM has D_p possibility of changing its switching state. For an MMC system, the carrier frequency is usually below 3 kHz. Events of changing state only happen when the carrier waveform is equal to the reference waveform, otherwise there is no change to the gate signal, and therefore it is obvious that $D_p \ll 1$. Thus, the sorting time for ISA becomes:

$$T_1 = D_p(1 + 2 + 3 + \cdots + N) = D_p \cdot N(N-1)/2 \tag{4.2}$$

where T_1 is the sorting time of ISA. Compared with the CSA, the relationship between the CT

of CSA and ISA can be easily derived.

$$T_0 \gg T_1 \tag{4.3}$$

This proves that the effectiveness of the proposed ISA as its computational complexity is lower than that of the CSA. Additionally, for a system which is not very sensitive, the required number matrix can be set using an average value every 5 (or more) sampling periods to further improve effectiveness in reducing switching frequency. The comparison of CT for the ISA and CSA is illustrated in Figure 4.4, where the D_p is set to 0.4. From Equation 4.4 and this diagram, the reduction of the CT that the ISA is heavily dependent on the value of D_p, which means that it relies on the modulation methods.

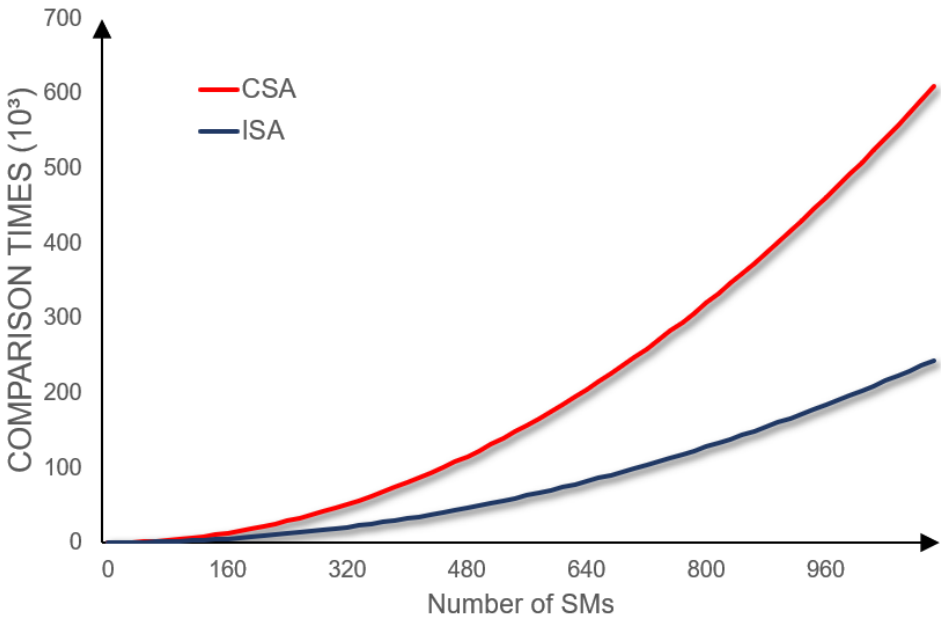


Figure 4.4 Comparison of computational complexity between ISA and CSA.

Due to the employment of sorting and virtual sorting algorithms, the options proposed in this chapter have strong voltage balancing capabilities. Meanwhile, these index choices could be replaced by other existing methods; for instance, the RSF method mentioned elsewhere [36] which is more effective in reducing the switching frequency, or tolerance-band control methods [21]. Both are focusing on the less usage of CSA but produce larger capacitor voltage fluctuation.

4.6 Simulation Results

Simulation studies have been carried out using the MATLAB/Simulink software package based on a 4-level single-phase MMC model. The simulation circuit is built based on Figure 2.1. The main system parameters used in the simulation are listed in Table 4-II. The sampling frequency f_{sample}=20, and the value of arm inductance and SM capacitance are selected based on Equations 2.17 and 2.18. The feasibility of the proposed ISA is demonstrated for a single-phase MMC with 3 SMs per arm.

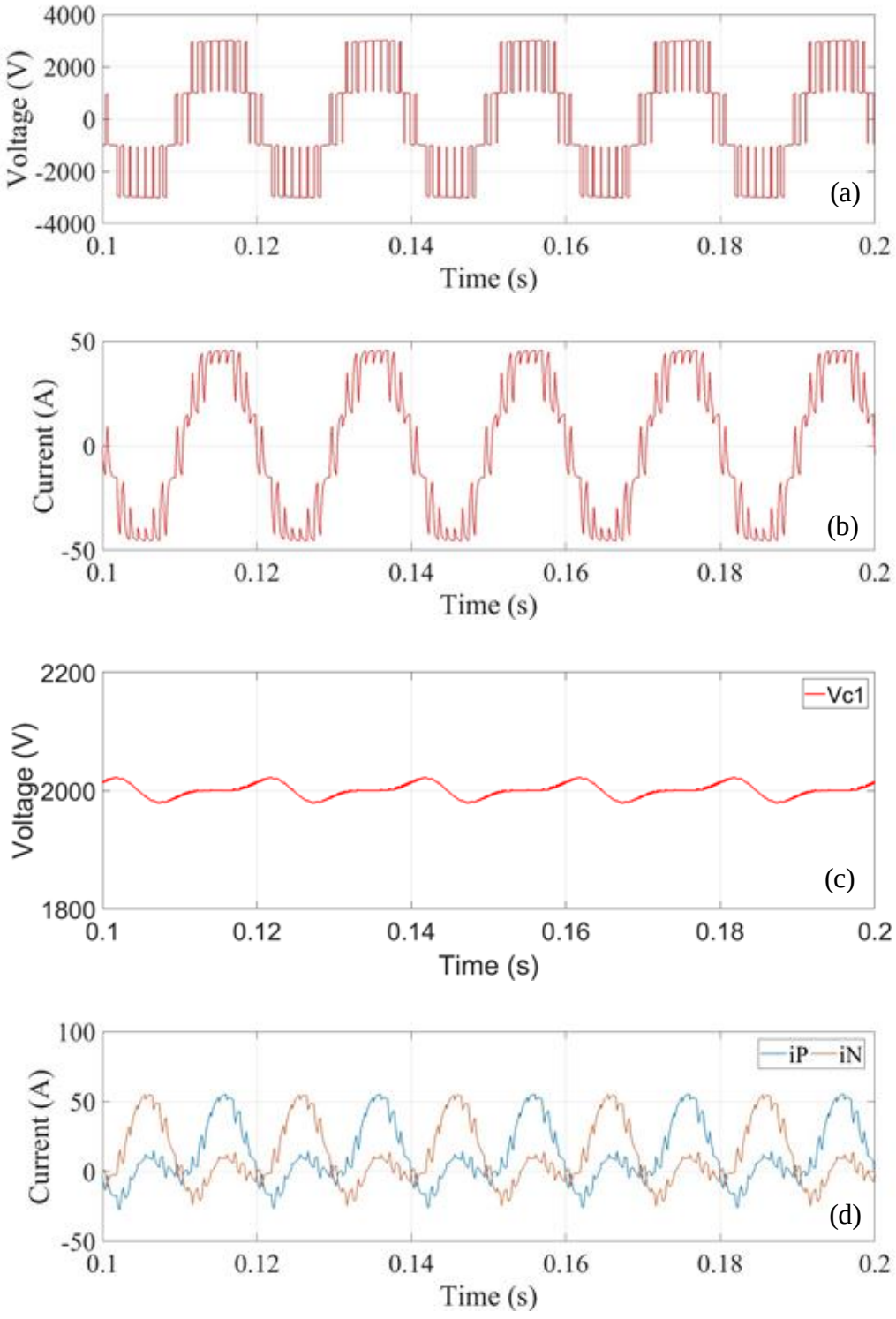
Table 4-II Parameters of Simulation.

Parameter	**Value**
Modulation index (m_i)	1.0
Switching frequency (f_c)	1 kHz
Output frequency (f)	50 Hz
DC source voltage (V_{DC})	6000 V
Arm inductance (L)	3.0 mH
Load inductance (L_L)	4.0 mH
Load resistance (R_L)	68 Ω
SM capacitance (C)	2.0 mF
SM resistance (R_{ESR})	0.1 Ω

4.6.1 Steady-state operation condition of CSA and ISA

The performance of the conventional sorting algorithm and proposed ISA are expressed in Figure 4.5 to Figure 4.6, and they have effectively balanced the voltage of the SMs. From Figure 4.6, the proposed ISA does not have a negative impact on the output voltage which means it won't sacrifice the performance of the system to achieve the switching frequency reduction. When comparing Figure 4.6 (a) and Figure 4.6 (b) with Figure 4.5, there is no substantial difference in the capacitor voltage or current, and all have strong staircase waveforms. In Figure 4.5 (c) and Figure 4.6 (c), the value of voltage variations is close. They all have small oscillations around the reference value of 2000V. Figure 4.6 (d) and Figure 4.6 (e) depict the

current performance, again the ISA does not significantly change the performance compared to Figure 4.5 (d) and (e).



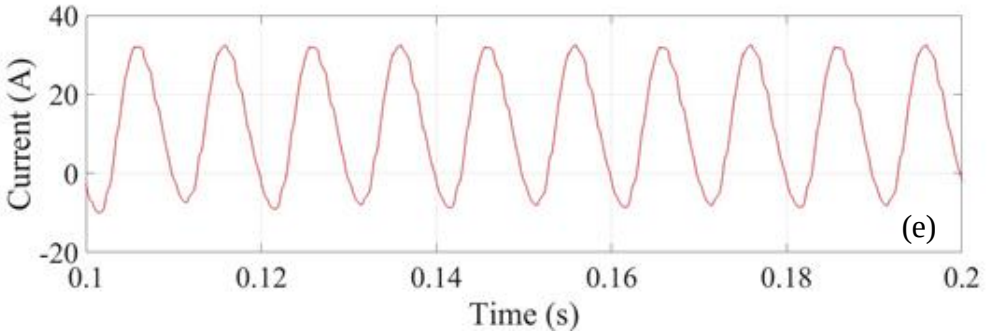
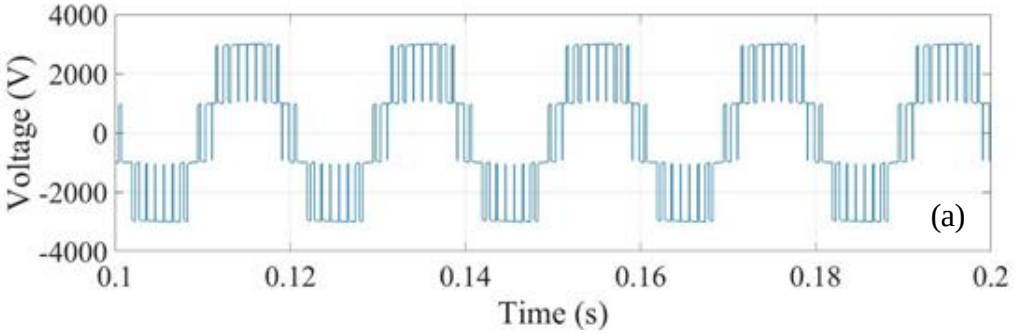
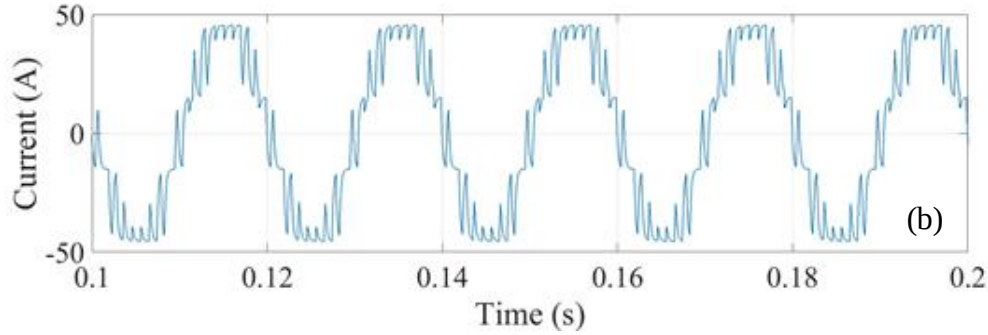
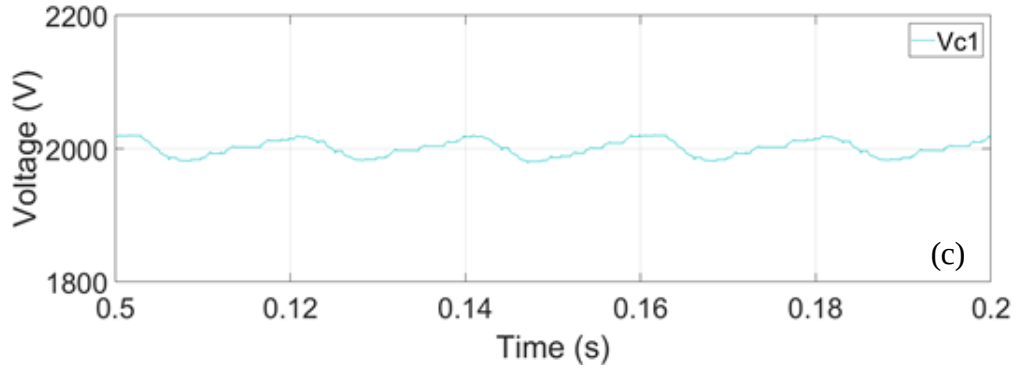


Figure 4.5 Simulation results of conventional sorting algorithm. (a) Output load voltage. (b) Output load current. (c) Voltage across C1. (d) Upper arm and lower arm current. (e) Circulating current.







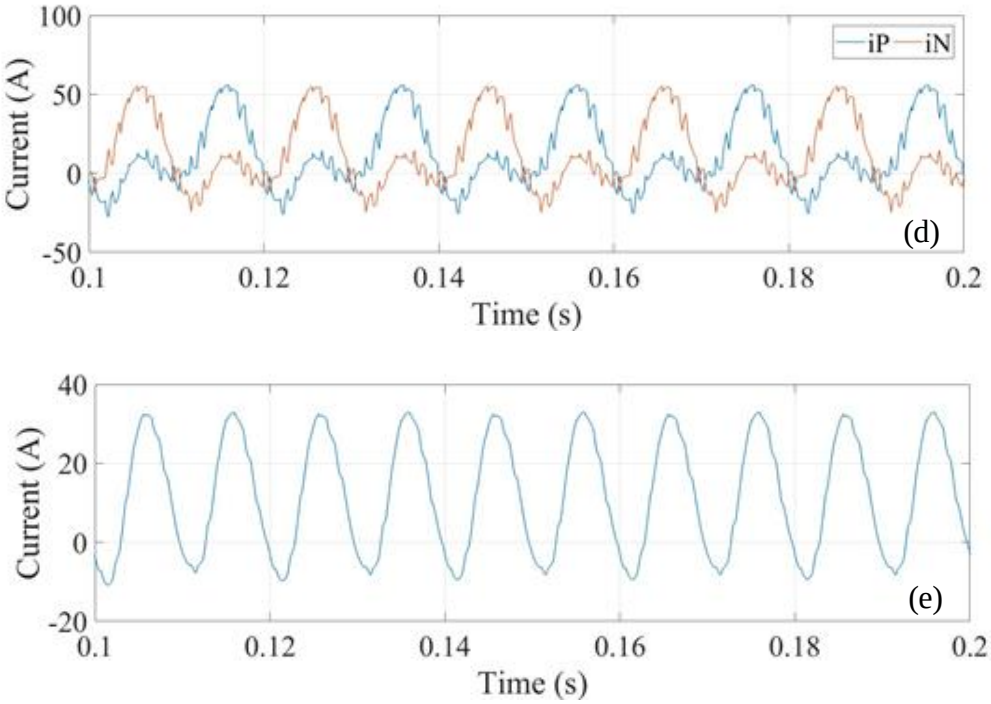


Figure 4.6 Simulation results of ISA. (a) Output load voltage. (b) Output load current. (c) Voltage across C1. (d) Upper arm and lower arm current. (e)Circulating current.

Figure 4.7 compares the difference between CSA and ISA in terms of the gate signal for all the upper arm SMs. The ISA shown in (b) has clearly fewer switching events than the CSA shown in (a) over the same period. Figure 4.9 demonstrates the switching events and the average switching frequency of ISA within 0.1s of SM1. The simulation counts the rising edge of the gate pulses. Comparison between Figure 4.8 and Figure 4.9, clearly indicates that ISA has better efficiency in terms of frequency reduction, which reduce the average switching frequency from 3350 Hz to 510 Hz, over the CSA. Overall, the effectiveness of switching frequency reduction has been proved by the results.

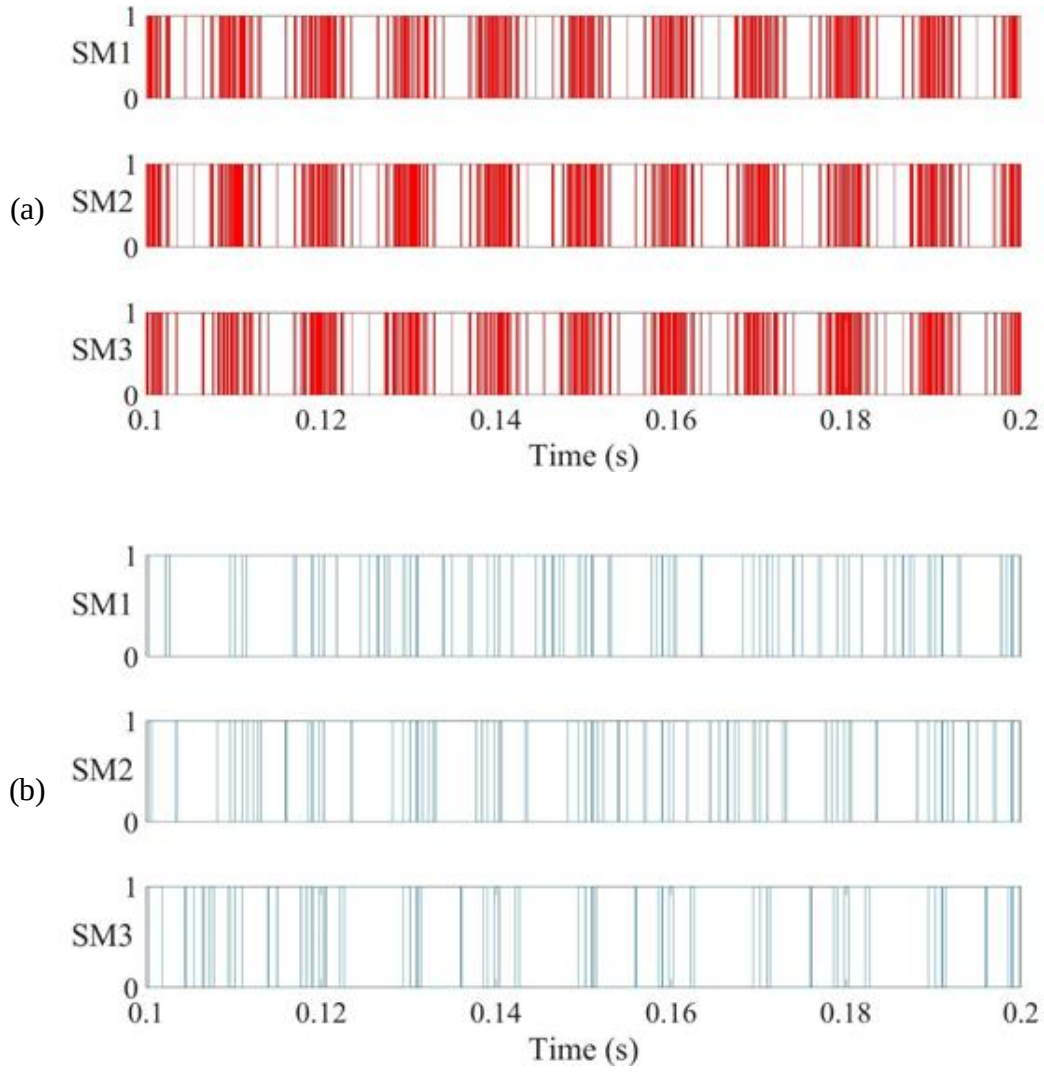


Figure 4.7 Simulation results of gate signal for upper arm SMs with different voltage balancing algorithms. (a) CSA. (b) ISA.

Figure 4.10 compares the difference between CSA and ISA in terms of capacitor voltage ripple. It is obvious that Figure 4.10 (b) from ISA has more flexibility, which means the capacitor voltages are no longer required to maintained identical, instead the variation becomes larger as long as they are inside the pre-defined range, compared to CSA from the Figure 4.10 (a). The capacitor voltage ripples of CSA are identical and fluctuate around the reference value $V_{ref} = V_{DC}/N$=2000V. The capacitor voltages of ISA have a slight variation from each other, but the variation is smaller than the fluctuation range of CSA. Figure 4.11 shows the harmonic distribution with the help of Fast Fourier Transform (FFT) of CSA and ISA during the steady-state. From the figure, the THD of ISA is not changed significantly from CSA.

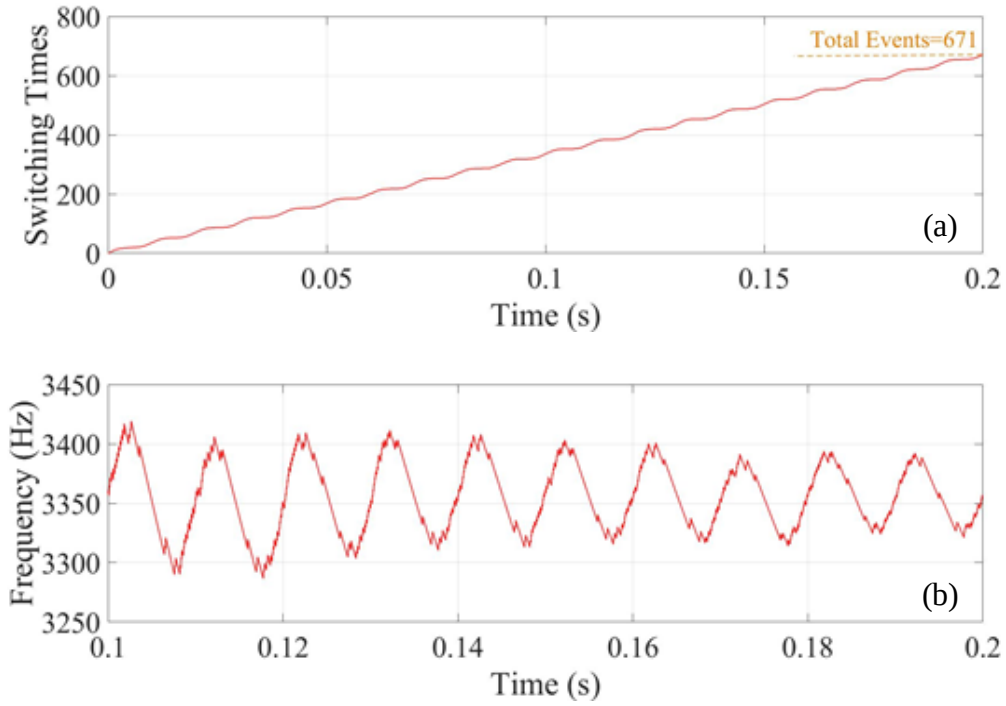


Figure 4.8 Switching condition of SM1 based on CSA. (a)Switching events. (b)Average switching frequency.

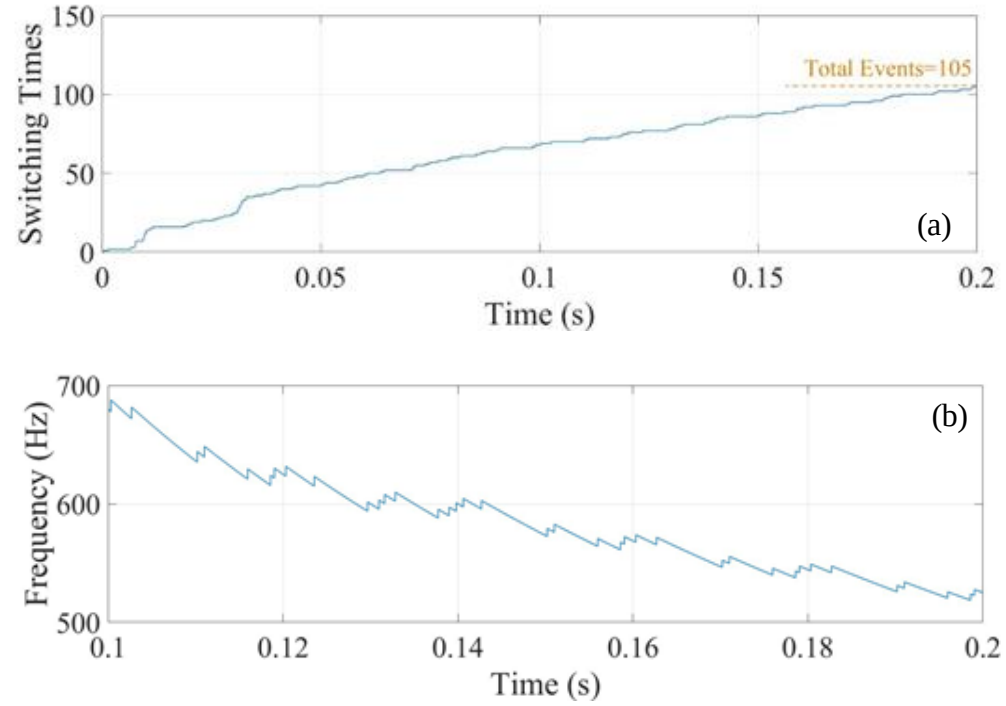


Figure 4.9 Switching condition of SM1 based on ISA. (a)Switching events. (b)Average switching frequency.

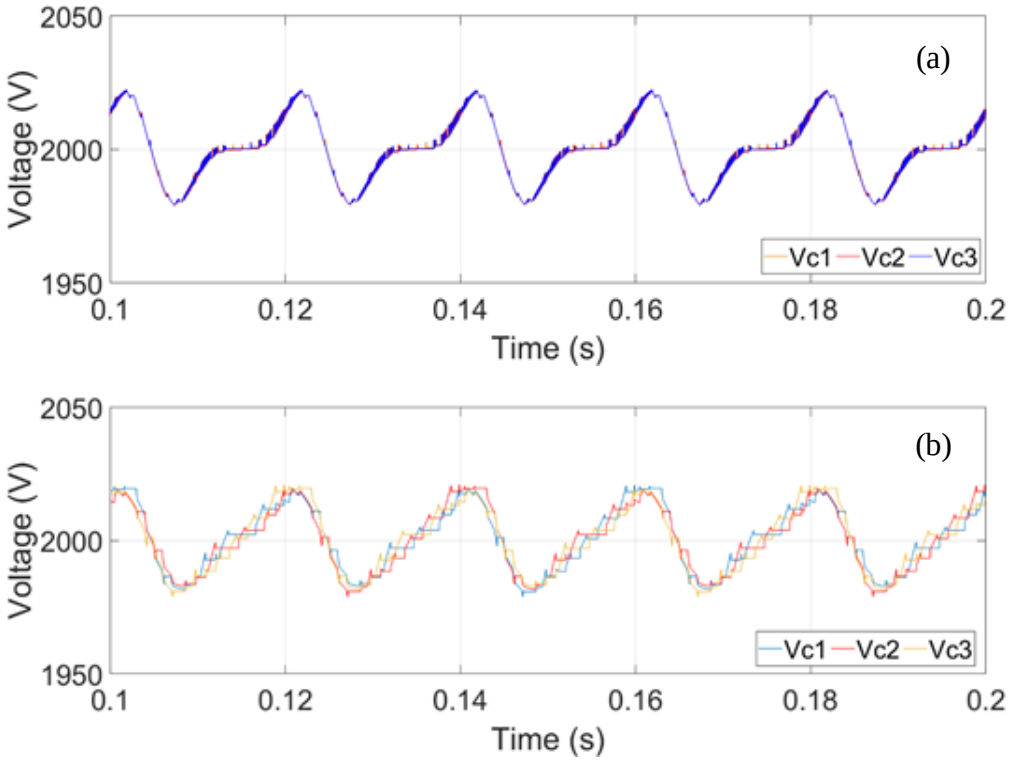
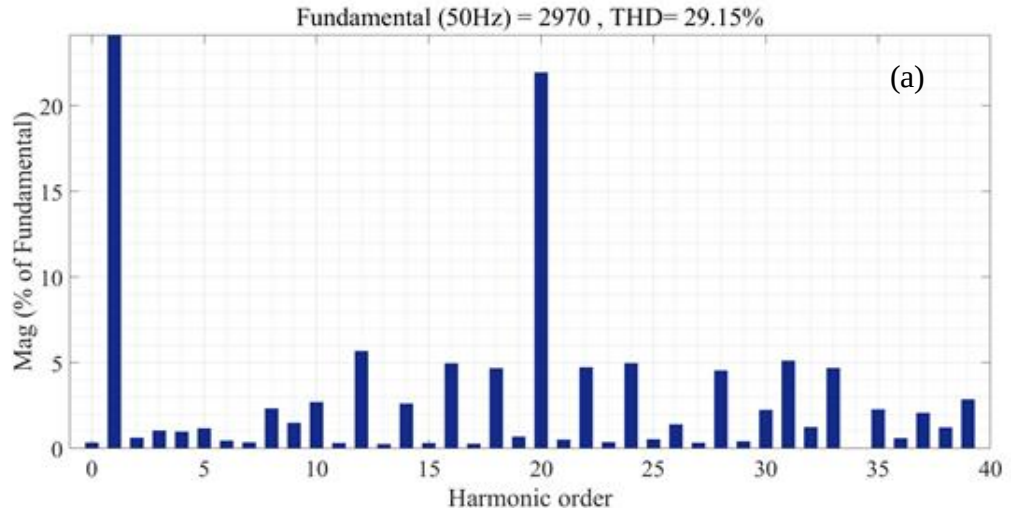


Figure 4.10 Capacitor voltage ripple performance comparison of upper arm. (a) CSA. (b)ISA.



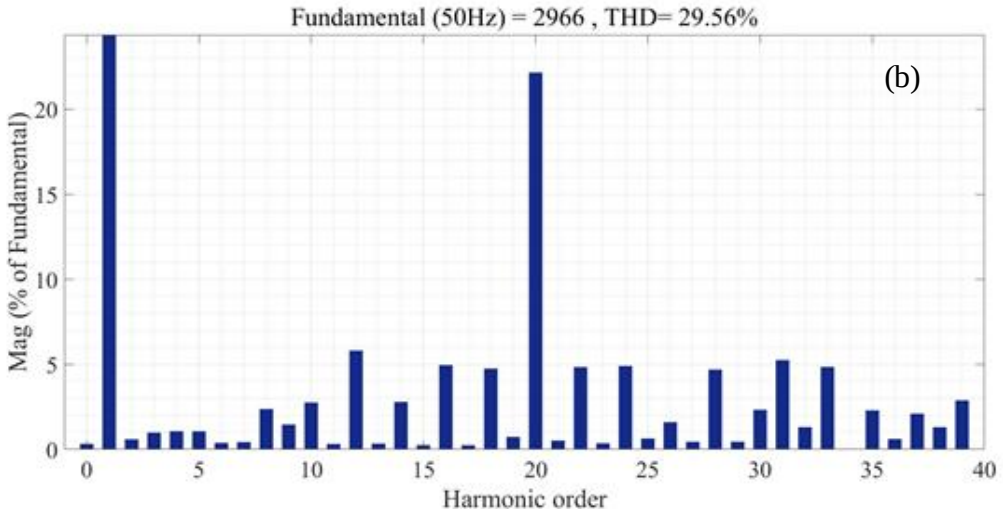


Figure 4.11. Output voltage harmonic performance. (a) CSA. (b) ISA.

4.6.2 Performance during a step change of DC side

The MMC topology is highly compatible with renewable energy such as PV and wind turbine, which produce unstable sources. Also, as in MMC-HVDC back-to-back system, the failure of the DC-link capacitor is a common failure type of the system. Overall, the dynamic response to the step change of DC source is important. The dynamic response of the proposed ISA is tested by applying a step change in the DC side at t=0.4. The DC source loses 50% of its original value and drops from 6000V to 3000V. Comparison is made between the CSA and ISA based on the output voltage, output current and the capacitor voltage.

It can be seen from Figure 4.12 (c), the capacitor voltage of CSA is able to balance again at V_{DC}/N =1000V less than 0.1s. The results depicted in Figure 4.13 of ISA are very close to the results in Figure 4.12, there exists a ripple during the transient period for ISA, but the overall performance is as good as CSA. According to the theory, CSA should have the best dynamic response because it alters the states of SMs every single sampling period. The simulation results prove the theory and the effectiveness of both CSA and ISA under the step change condition.

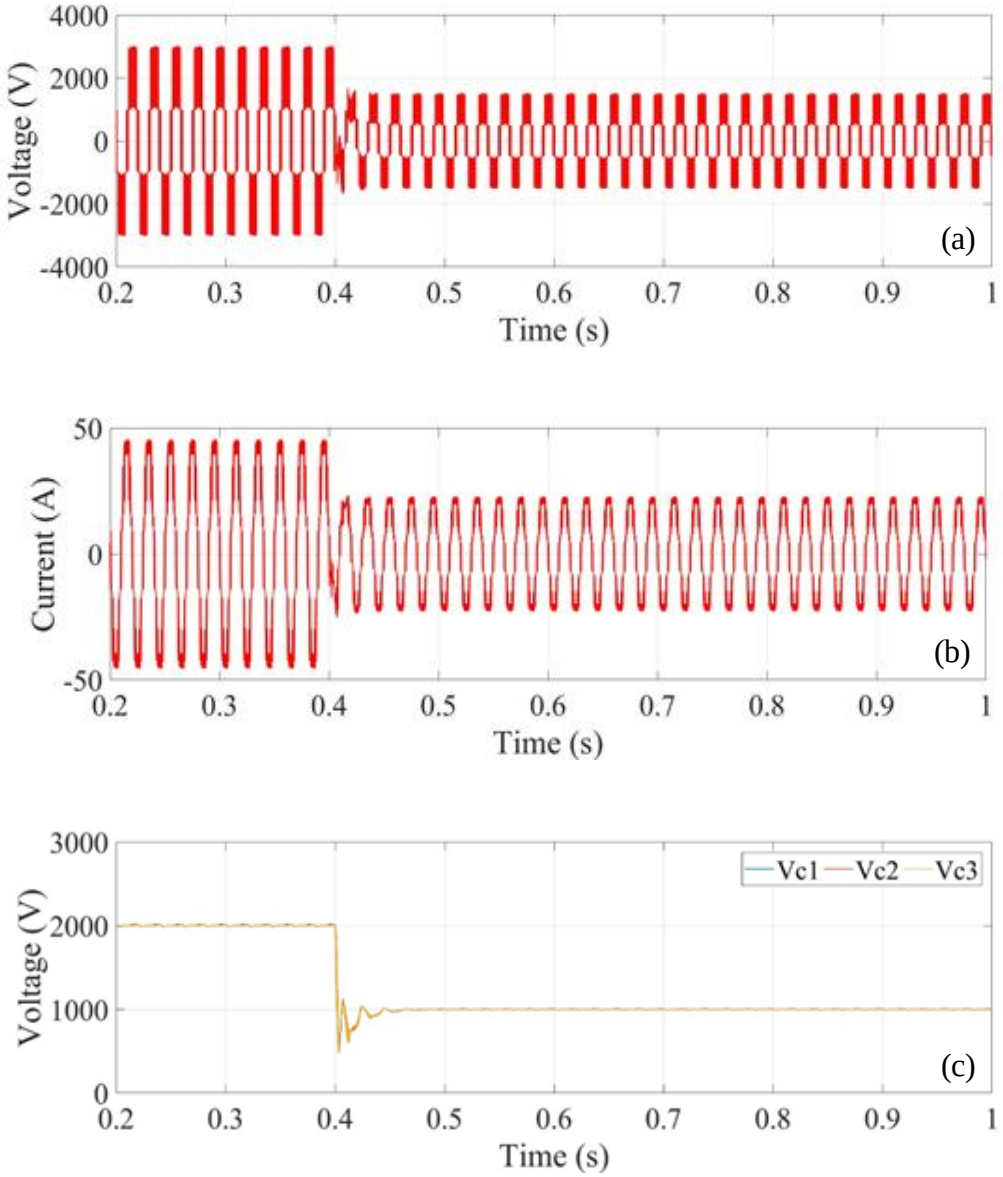


Figure 4.12 Simulation results for DC step change under CSA scheme. (a) Output load voltage. (b) Output load Current. (c) Capacitor voltage of upper arm.

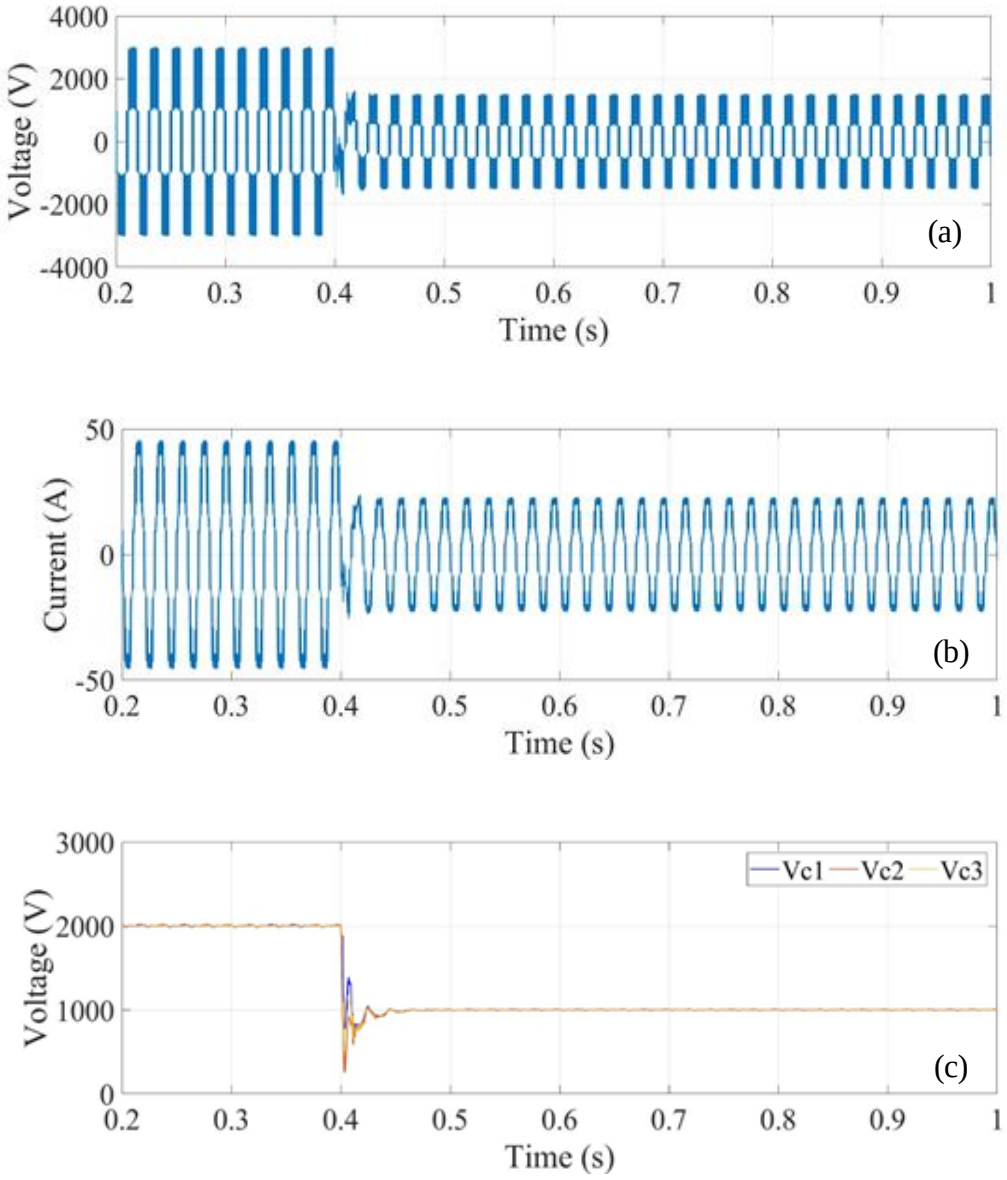


Figure 4.13 Simulation results for DC step change under ISA scheme. (a) Output load voltage. (b) Output load Current. (c) Capacitor voltage of upper arm.

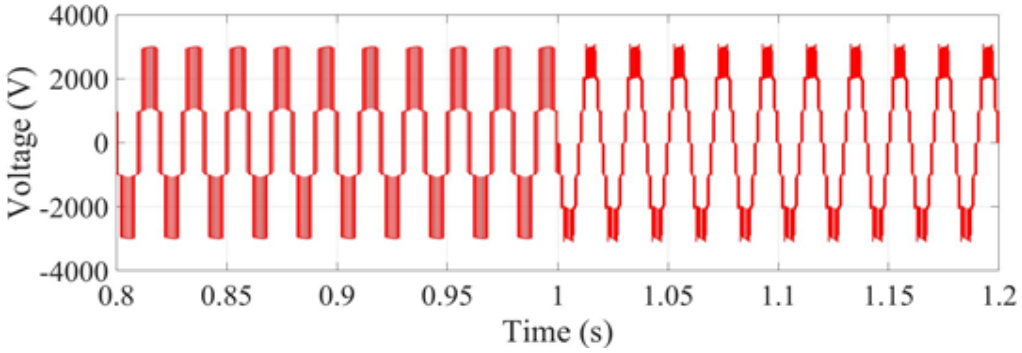
4.6.3 Implementation of Interleaving

Figure 4.14 shows the response of CSA after the interleaving modulation scheme applied for the upper arm at t=1s. The expectation of the output level is altered from 4-level to 7-level. From Figure 4.14 (a), the output level transferred very fast and have a significant impact on the output load current on Figure 4.14 (b). The current waveform is smoother compared to a 4-level scheme which means it has the potential to reduce the size of the filter. Figure 4.14 (c) and (d)

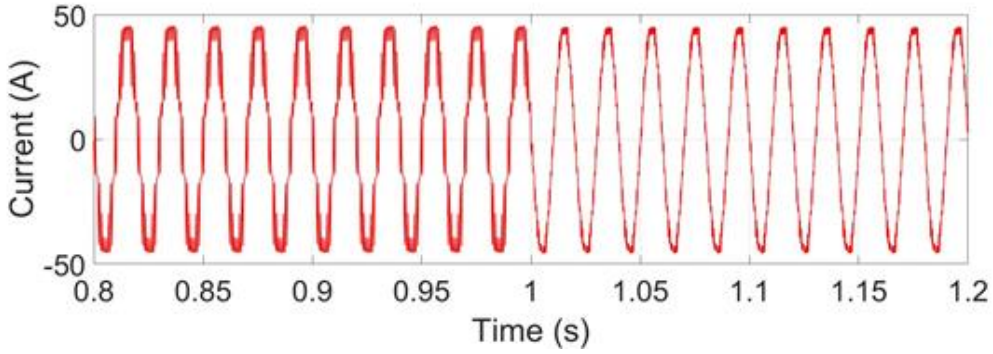
reflect the capacitor voltage ripples, the fluctuation range increased from 1% to 5% because the circulating current is increased from 50A to 200A. That is the drawback of the interleaving modulation scheme, to increase the distortion and make the system unstable.

Figure 4.15 depicts the response of ISA after the interleaving modulation scheme applied for the upper arm at t=1s. Compared to the CSA, the output dynamic response of them are similar according to Figure 4.15 (a) and (b). It can be seen from Figure 4.15 (c) and (d), the voltage variation and circulating current of ISA is smaller than CSA, which shows the ISA improved the performance of the sorting algorithm.

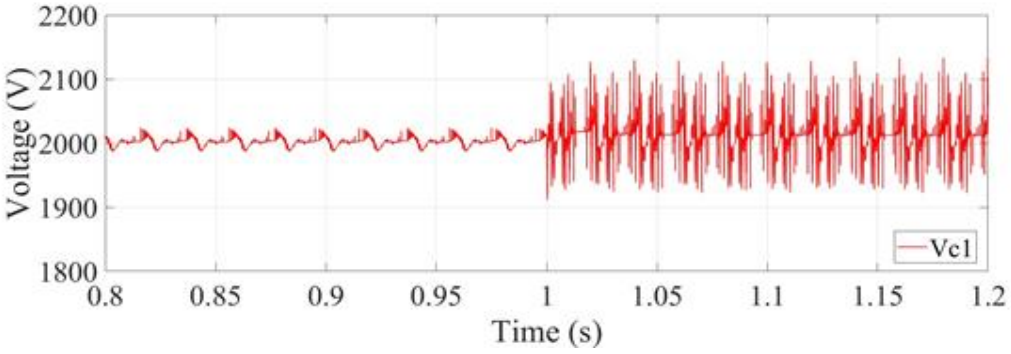
(a)



(b)



(c)



(d)

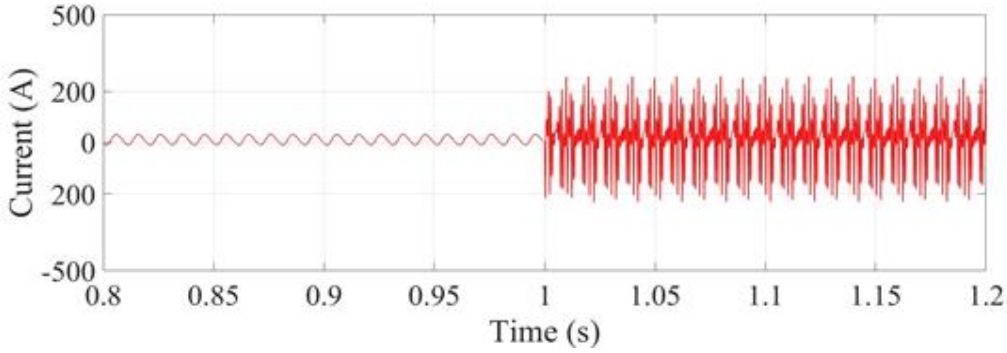
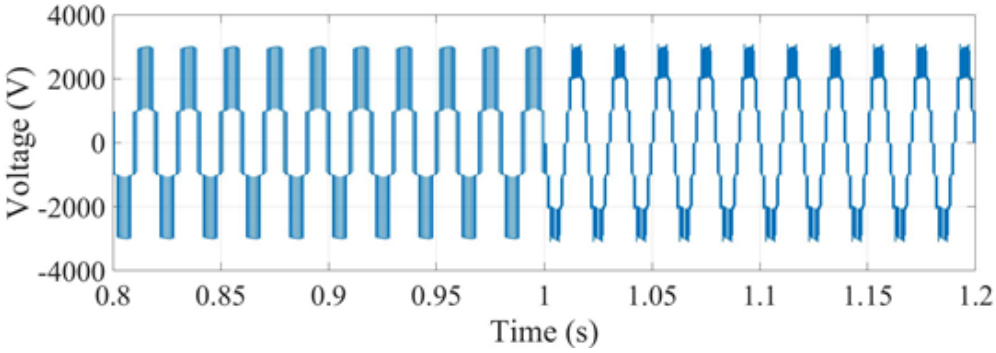
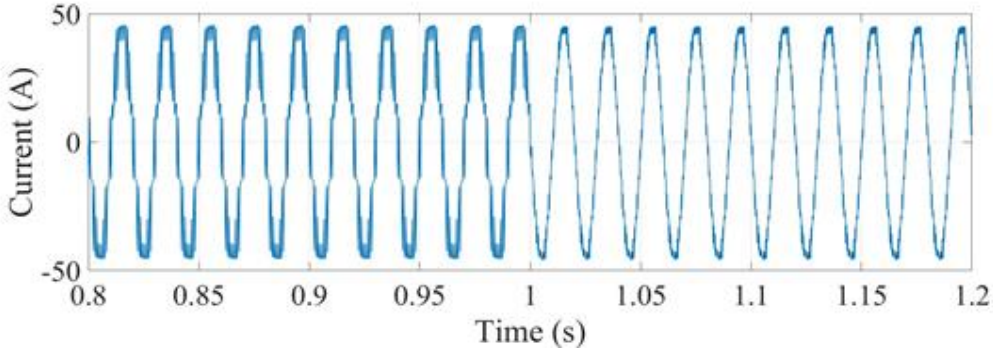


Figure 4.14 Simulation results for applying interleaving modulation scheme 4-level MMC with CSA (a) Output load voltage. (b) Output load Current. (c) Capacitor ripple voltage of SM1. (d) Circulating current.

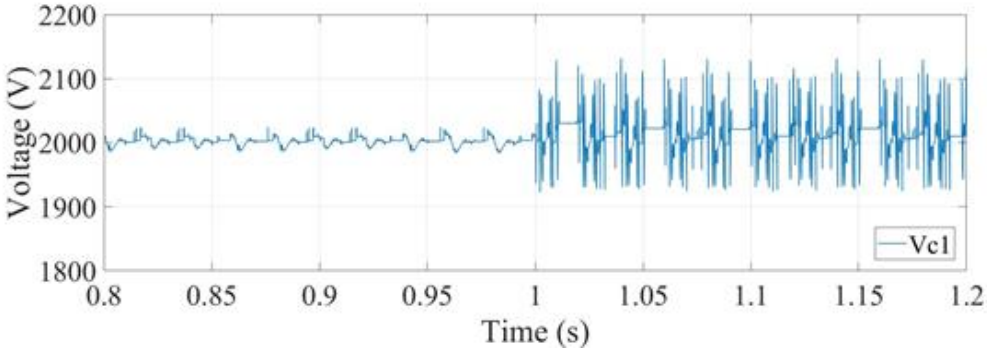
(a)



(b)



(c)



(d)

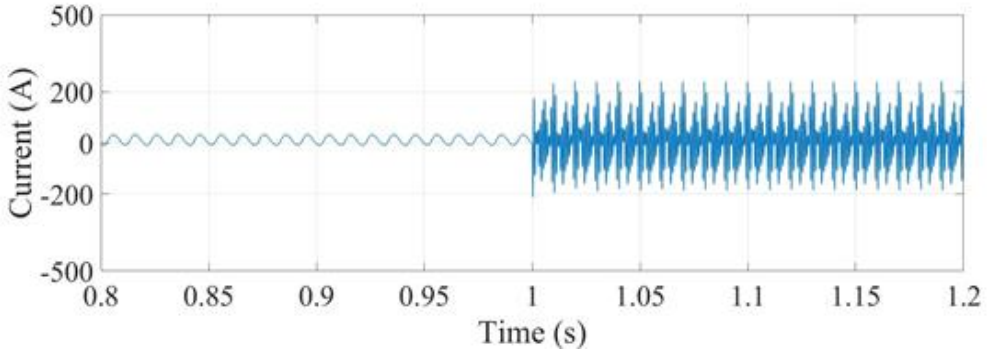


Figure 4.15 Simulation results for applying interleaving modulation scheme 4-level MMC with ISA (a) Output load voltage. (b) Output load Current. (c) Capacitor ripple voltage of SM1. (d) Circulating current.

4.7 Chapter Summary

This chapter reviews the principles and features of the CSA and investigates the cause of unnecessary switching events. The ISA is proposed and explained in order to reduce the switching frequency. The ISA essentially provides several options for the final gate signal index and reduces the switching frequency by allowing the capacitor voltage to fluctuate slightly within an acceptable pre-defined range. The SMs with voltages outside that range should have faster convergence speed toward the range with the help of a coefficient which multiplies the measured voltage values. The simulation results of the ISA indicated that the capacitor voltages do not continue to track each other's values in every sampling period. Instead, their values vary slightly within a 1% range which is acceptable. Meanwhile, the switching frequency was substantially decreased without compromising overall performance in terms of THD, ripple and output level. Also, the dynamic response of both CSA and ISA were also tested and compared in the simulation, and the results indicate that the ISA has a similar dynamic response to that of the CSA. However, the method still sorts all the SMs most of the time, and so the problem of computational complexity remains to be resolved and requires further effort.

Chapter 5. The Hybrid Heap Sorting Strategy

5.1 Introduction

This chapter proposes another solution for the improvement of the sorting algorithm for MMCs. The heap sorting algorithm is introduced and applied to replace the conventional bubble sorting algorithm. The objective of the proposed scheme is to decrease both the switching frequency and computational complexity.

This chapter commences with an introduction to the heap sorting algorithm, explaining its superiority in terms of lower complexity compared to the conventional bubble sorting algorithm. A brief comparison of all the main sorting algorithms is then conducted. This heap sorting algorithm applied to the MMC still produces the gate signal directly, but its application differs slightly from that of bubble sorting due to its special characteristics. The heap sorting algorithm can then be tuned to make it suitable for MMC applications.

The reduction of computational complexity associated with heap sorting has already been extensively proven and detailed in numerous studies [106-108], and therefore it is not necessary for this study to cover the same ground. This chapter illustrates the operation of heap sorting using simple graphs to explain how it reduces computational complexity. As one stable algorithm in the sorting family, its mode of gate signal control is no different from other examples, signifying that it produces gate signals every sampling period and thus the switching frequency remains high. This chapter combines the heap sorting algorithm with a proposed switching reduction technique elsewhere [65] to overcome such problems.

5.2 Principles and Operation of the Heap Sorting Algorithm

As explained in Chapters 3 and 4, the conventional bubble sorting algorithm not only increases switching frequency, but also significantly increases the computational complexity, since all of the SMs are involved in the comparison process. In the initial introduction of the bubble sorting

algorithm [109]. In a system with m elements, the time complexity of bubble sorting was $O(m^2)$, which means that in every sampling instant, the functions of comparison are executed at least for m^2 times. The notation ***O*** refers to a function which describes that for m size input, the asymptotic line of the execution time is m^2, which is greater than those for many other sorting algorithms [107]. Time complexity describes the volume of functions or tasks for the processor to complete, where higher time complexity means that a longer time is needed to process the data. Space complexity is a measure of the storage requirements of the processor if it is to complete the application of the algorithm. The evaluations of different sorting algorithms are based on time complexity, space complexity and stability [108]. Table 5-I compares some of the most commonly used sorting algorithms.

Table 5-I Comparison of some commonly used sorting algorithms[106].

Sorting Algorithm	**Time Complexity**			**Space Complexity**	**Stability**
	Average Case	***Best Case***	***Worst Case***		
Bubble Sort	$O(m^2)$	$O(m)$	$O(m^2)$	$O(1)$	$O(m^2)$
Insertion Sort	$O(m^2)$	$O(m)$	$O(m^2)$	$O(1)$	$O(m^2)$
Selection Sort	$O(m^2)$	$O(m^2)$	$O(m^2)$	$O(1)$	$O(m^2)$
Merge Sort	$O(m \log_2 m)$	$O(m \log_2 m)$	$O(m \log_2 m)$	$O(m)$	$O(m \log_2 m)$
Quick Sort	$O(m \log_2 m)$	$O(m \log_2 m)$	$O(m^2)$	$O(m \log_2 m)$	$O(m \log_2 m)$
Heap Sort	$O(m \log_2 m)$	$O(m \log_2 m)$	$O(m \log_2 m)$	$O(1)$	$O(m \log_2 m)$

In this thesis, the evaluation of computational complexity is simplified in order to calculate the time complexity by measuring the functions used for the algorithm. As illustrated in the table above, with regards to time complexity heap sorting is superior to conventional bubble sorting with fewer functions applied during the sorting action. The principle of the heap sorting algorithm is to sort the data based on a heap data structure. The heap tree is normally a binary tree shape which is balanced, space-efficient and fast [110]. This binary tree structure is where

the largest or smallest value is located on the top and is referred to as the root node. Each node can be divided into two children nodes, and the father node is always greater or smaller than the children node. If not, their positions should be swapped.

The heap sorting algorithm has two main steps:

1. The binary heap tree is built up based on the data collected. If the top node has the largest value and children nodes are always smaller than the father node, it is called a max heap, and vice versa for a min-heap. The explanation for building up the max heap is illustrated in Figure 5.1, with a three-element example where the root node (father node) is not the largest. The children node from the second level have larger value, so it swaps positions with the father node.

2. The second step is to remove the largest/smallest elements from the root node one by one and to store them in after-sorting arrays. Next, the root element is swapped with the last element of the tree, then the element is removed and put into the end of the after-sorting array. Then the heap tree again is checked to ensure that it complies with the heap tree rule. If not, the heap tree is re-constructed start with the children nodes. This re-construction process is called heapification which only requires comparison. Finally, the above steps are repeated until the array is filled.

According to Figure 5.1, it takes two comparisons between elements based on the heap tree (6 and 1, 4 and 1) before all the elements can be sorted in the ascending sequence, while for bubble sorting is 3(3-1)/2=3. The CT is smaller because there is no comparison between the same levels. Therefore, it can be concluded that heap sorting has a lower CT than conventional bubble sorting.

The heap sorting algorithm is a slow sorting algorithm and is slower than other sorting algorithms with the same time complexity. However, the characteristics of the heap tree make it highly suitable for MMC voltage balancing since an exact sequence of input elements is not required. Instead, only a few of the SMs are involved in sorting in every sampling period.

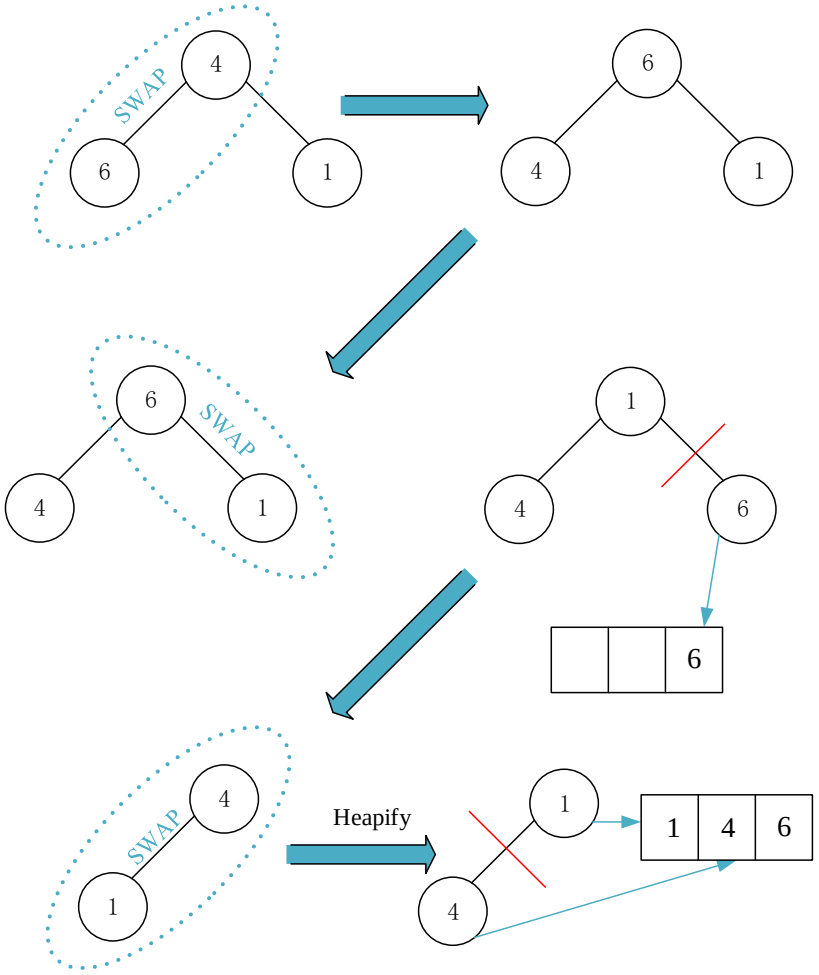


Figure 5.1 Sorting process depending on the heap tree.

5.3 Heap Sorting for the MMC

From the previous analysis, the heap tree has one root node, which can be expanded into two children nodes. Each children node then becomes the father node and is expanded into two nodes until each element has its own father or children node. For an array with N elements, the relationship between the number N and the number of elements of the Max level is $\mathbf{Y}_{max}$. It is assumed that the number of elements that the k level contains is 2^{Y_k-1}. For an MMC arm that contains N SMs, in every sampling period the required number n is fed by modulation methods and varies from 0 to N. The procedure of heap sorting implementation is as follows:

1. The voltage $V_C(i)$ is measured and $0 \leq i \leq N$.

2. If $I_{arm} \geq 0$, the complete max binary heap tree is built, where the root node has the

maximum value; if $I_{arm} < 0$ the min heap tree is built, where the root node has the minimum value.

3. The required inserted number *n* is compared with the number of the lowest levels of heap tree.

   a) If $n \leq 2^{\mathbf{Y}_{max}-\mathbf{1}}$, only the elements of the $\mathbf{Y}_{max}$ level are bubble sorted; i.e. sort a sub-group of *N*. The sorting algorithm chosen here can be either CSA or the heap sorting algorithm.

   b) If $n > 2^{\mathbf{Y}_{max}-\mathbf{1}}$, all of the elements of the $\mathbf{Y}_{max}$ level are switched on and then move upwards to the $\mathbf{Y}_{max} - 1$ level. If $n - 2^{\mathbf{Y}_{max}-\mathbf{1}} > 2^{\mathbf{Y}_{(max-1)}-\mathbf{1}}$, all of the SMs of $\mathbf{Y}_{max} - 1$ are switched on, and this step is repeated moving upwards until the following equation satisfied:

$$n - 2^{\mathbf{Y}_{max}-\mathbf{1}} - 2^{\mathbf{Y}_{(max-1)}-\mathbf{1}} - \cdots - 2^{\mathbf{Y}_{max-t}-\mathbf{1}} \leq 2^{\mathbf{Y}_{(max-1-2-\cdots-t)}-\mathbf{1}} \quad (5.1)$$

4. The lower levels are bubble-sorted with $(n - 2^{\mathbf{Y}_{max}-\mathbf{1}} - 2^{\mathbf{Y}_{(max-1)}-\mathbf{1}} - 2^{\mathbf{Y}_{max-t}-\mathbf{1}})$ SMs, and again this sub-group is sorted and here the difference between the results of bubble sorting and heap sorting is negligible.

Since the computational complexity required by the bubble sorting is very high, an effective way is to limit the comparisons made by the algorithm. Due to the nature of the heap sorting algorithm, it can be found that the lowest level always has the most extreme values of a data array. Therefore, when the SM voltage levels are inserted into the heap tree, the lowest level of the heap tree should contain the SMs which are most urgent to change their states. The SM voltages are not in ascending or descending sequence within the lowest level of the heap tree, and further selection is still based on bubble sorting but the number of SMs involved in the sorting has been halved. This is one way to implement the heap sorting algorithm in the voltage balancing of the MMC. Thus, after building up the heap tree, only one sub-group is involved in sorting. The sorting time decreases significantly, which indicates that computational complexity is also reduced. In order to demonstrate this, an example is depicted in the graph

below.

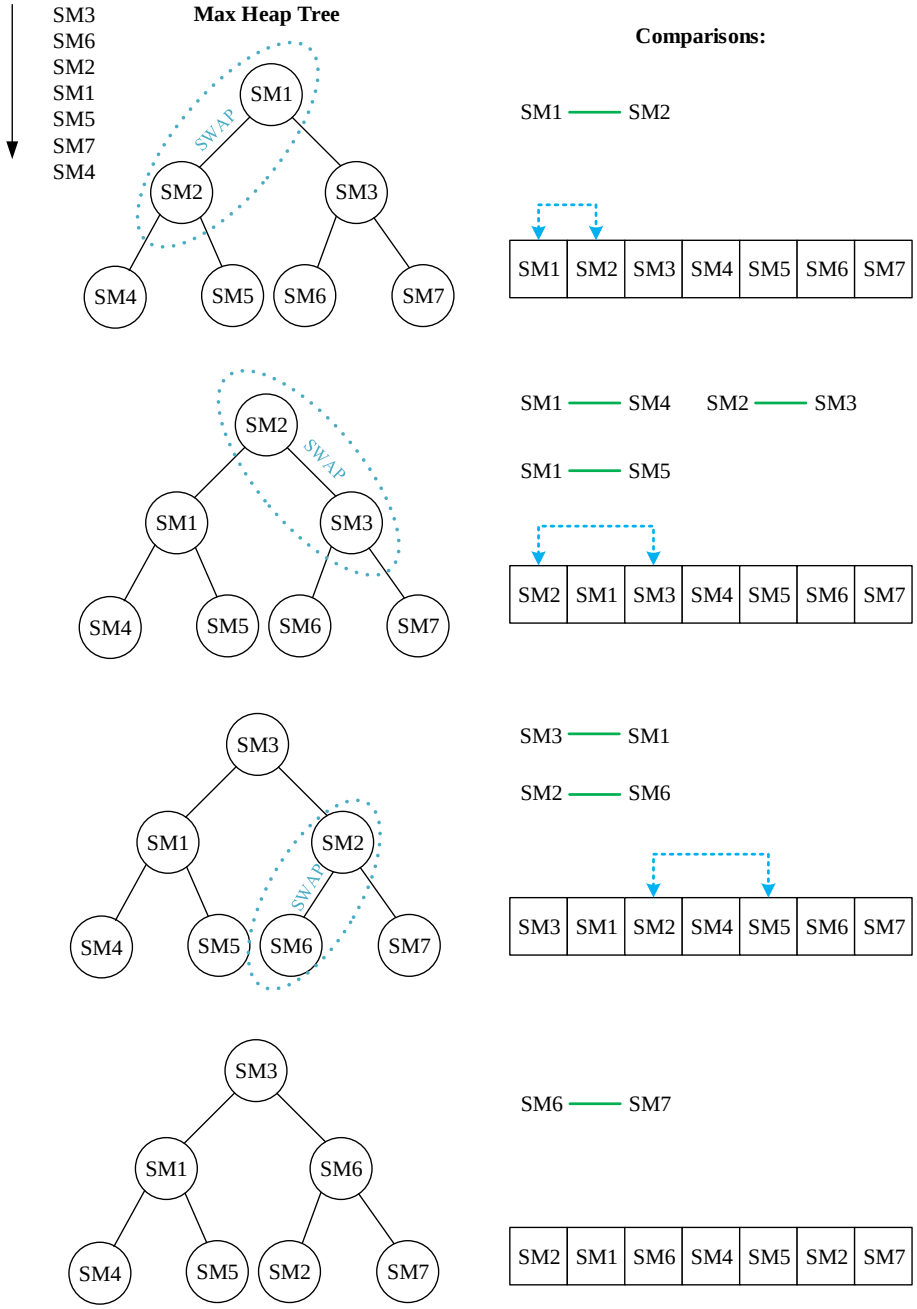


Figure 5.2 Process of building up the max heap tree.

Figure 5.2 provides one example of how the heap sorting algorithm works. For heap sorting of an MMC model that contains 7 SMs per arm, at every sampling period the required number n is fed by modulation methods and it varies from 0 to 7. Firstly, the current is assumed to be positive and the real sequence of voltage level from low to high is [SM4 SM7 SM5 SM1 SM2 SM6 SM3]. Before the actual sorting is applied, it is essential to build up the max heap

tree. Then the data array is initialised from top to bottom as [SM1 SM2 SM3 SM4 SM5 SM6 SM7], where the position in this array represents the position in the max heap tree. Then the top element with its left-hand children node are compared, SM1 is less than SM2, so the positions of SM1 and SM2 are swapped, and the SM1 becomes the children node. Then, the new children nodes are heapified by comparing the new father node with its children nodes again. The above procedure is repeated with the top nodes and its right-hand children node until all the nodes comply with the rules of the heap tree. The left-hand side of Figure 5.2 shows how the heap tree is built step by step, while the right-hand side exhibits all the comparison been conducted by the algorithm as well as the changes in position in the index array. Overall, the total comparisons to build the heap tree equals to the number of SMs which is 7.

Depending on the max heap tree built, the lowest level contains four elements:

- If the required inserted number $n<4$, the normal sorting is applied to all the SMs at the lowest level.
- If the required inserted number $n=4$, all the SMs of the lowest level are switched on and the rest are switched off.
- If the required inserted number $n>4$, the algorithm moves upwards one level, after switching on all the SMs at the lowest level.

Then the algorithm determines whether to sort the second level by comparing the value of n with the elements at both the second and the lowest level. However, the heap tree built here is only one possible situation, and some elements from the lower level are sometimes higher than the higher level of other father nodes, and thus there will exist some degree of error when applying heap sorting directly. From Figure 5.2, the voltage value of SM2 is higher than that of SM1, but the position of SM1 in the heap tree is high than that of SM2 even though all of the SMs are complying the rule of heap tree.

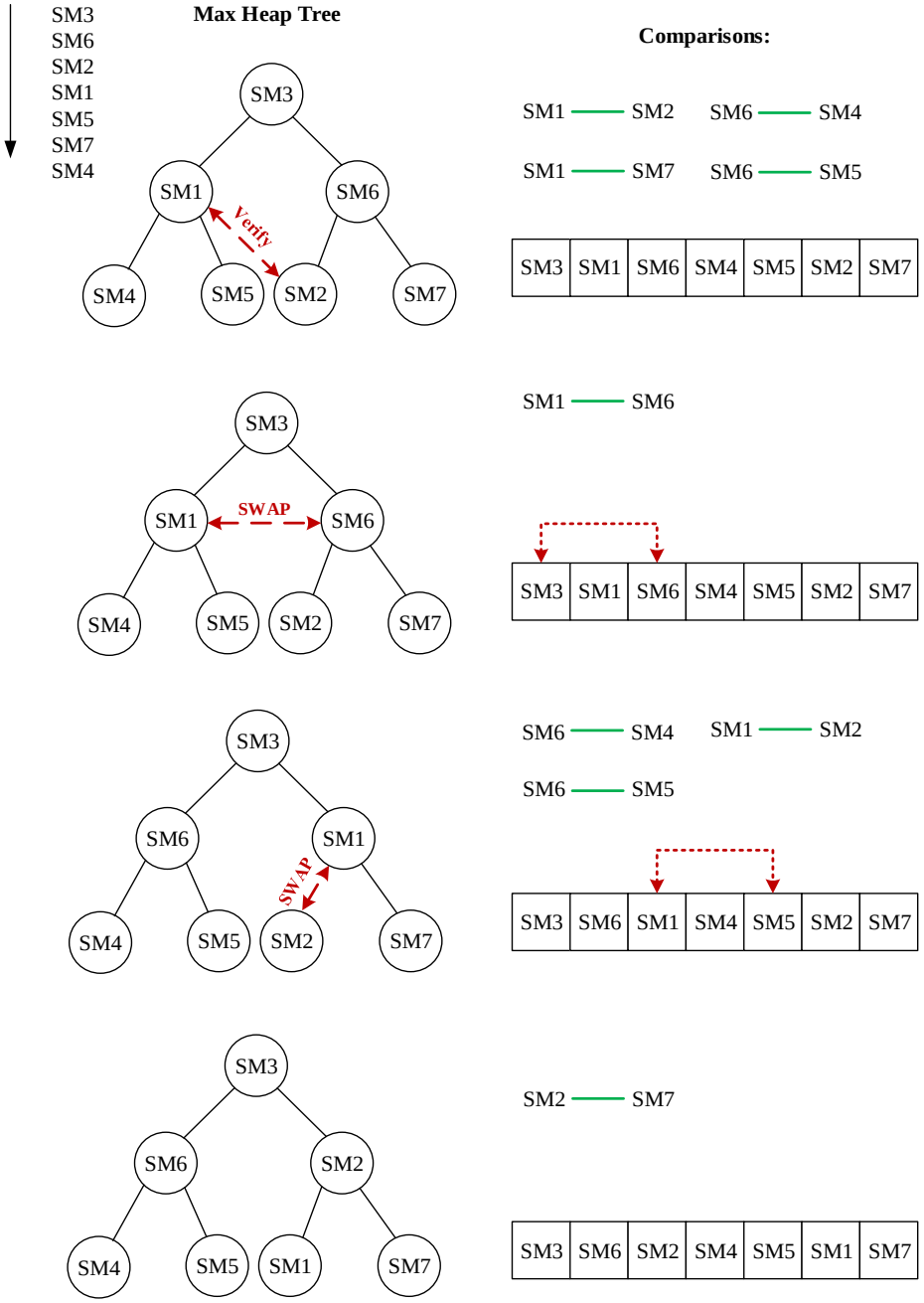


Figure 5.3 Process of building up the absolute heap tree.

The proposed solution is called the absolute heap, which avoids such situations by comparing the father nodes to the adjacent children nodes in the heap tree. This extra process guarantees that elements from the lower level are all lower/higher than elements of the corresponding higher level. Then, the absolute heap tree is built where the elements from different levels are absolutely in accordance with their heap tree level, and within the same level there is no order. Still based on the example from Figure 5.2, the proposed method is illustrated

in Figure 5.3, where the nodes from the second level are compared to with their adjacent children nodes. In this condition, SM1 is less than SM2, so this heap tree is not absolute, which means that further tuning is required before determining which SMs should be switched on. Then the positions of the nodes of the second level are swapped and the heap tree is heapified. Again, the left-hand side of Figure 5.3 shows the hipifications process, while the right-hand side indicates all the comparisons conducted by the algorithm as well as the changes of position in the index array.

Overall, the exact sequence of the data is no longer required, so the computational resources required by the heap sorting is less than that of the original heap sorting. The procedure for this heap sorting can be optimised in the following way:

1. The heap tree is built up.
2. To check the heap tree is absolute or not by comparing one node at the second level with the children nodes of its adjacent node. If it is absolute, proceed to the next step; if not, the positions of the two father nodes are swapped and the heap tree is reconstructed starting from step number one.
3. According to the required switched-on number n. It is determined which level of the heap tree needs to be sorted, then the SMs in lower levels are all switched on and those in higher levels are all switched off.

5.4 Hybrid Heap Sorting Algorithm

Since the absolute heap tree has successfully been designed, the heap sorting helps to significantly reduce the computational complexity. However, it cannot help in reducing the switching frequency, and thus, some further modifications are required to improve performance. For instance, a PFM has been proposed which assembles the SMs into the smallest groups by applying several layers of decomposition [96]. Consequently, each sub-group has only a few SMs, which provides the conditions necessary for the heap sorting algorithm. This is a hybrid control strategy to reduce computational complexity. The whole control strategy is designed for

the application of the sorting algorithm, and as one member of the sorting algorithm family, the heap sorting algorithm is highly compatible with such a strategy.

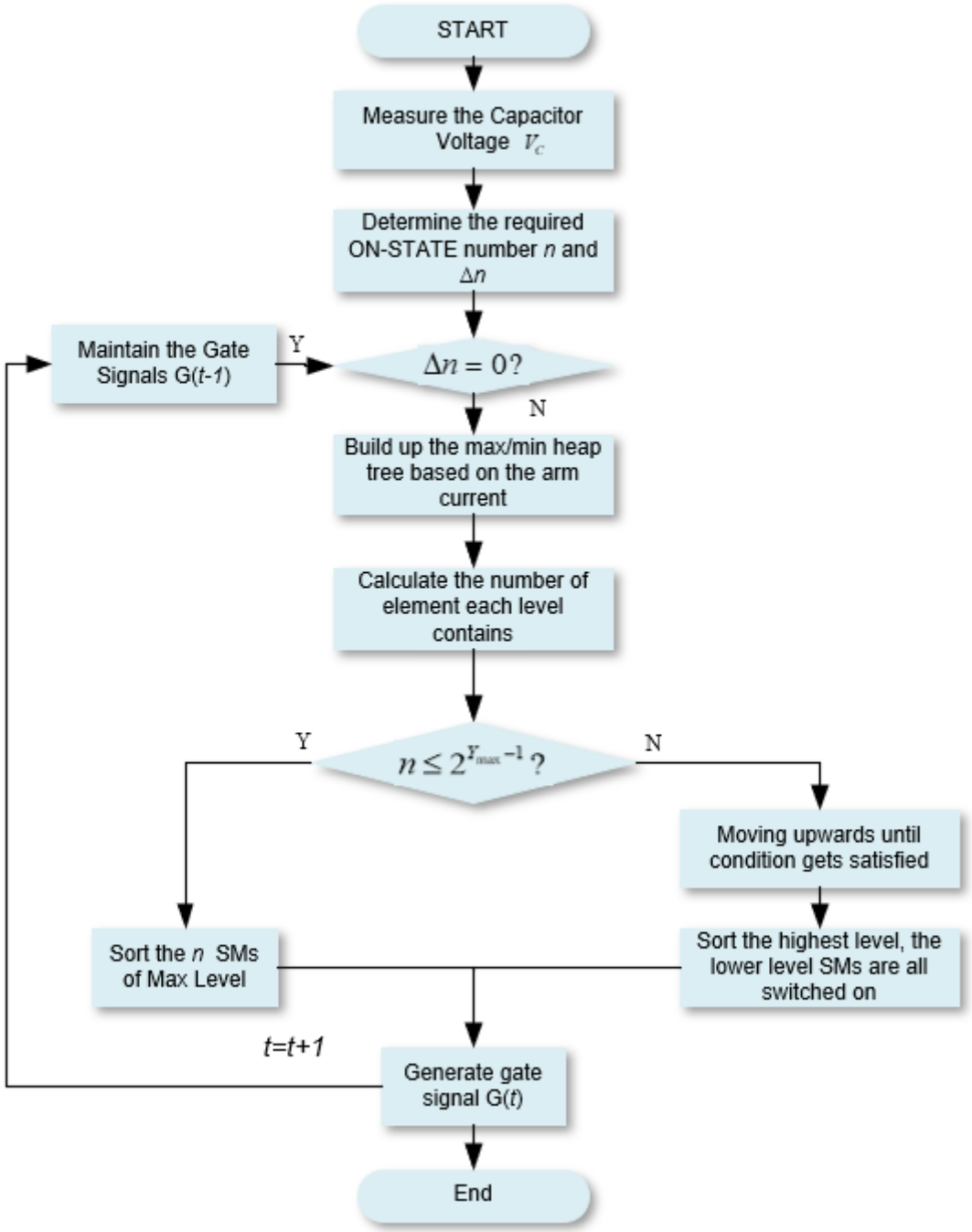


Figure 5.4 Flowchart of HSA.

For the issue of reduction in switching frequency, and the proposed heap sorting algorithm still sorts the SMs every sampling period, meaning that compared to CSA, there is no substantial change. Like the bubble sorting algorithm, the selection process is still executed in every

sampling period even though the CT have already been reduced significantly. In this thesis it is proposed that the heap sorting algorithm should be used in along with the technique described by Tu [36]. The change in the required inserted number is Δn, with the SMs maintaining their states when $\Delta n = 0$. The heap sorting algorithm only applies when $\Delta n \neq 0$, and the SMs are sorted directly. This hybrid strategy can improve control from both sides and is illustrated in Figure 5.4.

In this strategy, hybrid heap sorting algorithm (HSA) either sorts one level of the heap tree or sorts nothing, and when $\Delta n = 0$ no comparison is made. This supports the core concept enabling the SM voltage to fluctuate slightly instead of having to be identical. Thus, the objectives to reduce both switching frequency and computational complexity can be achieved.

5.5 HSA for High Number of SMs

There are several problems associated with heap sorting that hinder its ability to manage the sorting of high quantities of SMs. The speed is relatively slow, and it is not as accurate as of the CSA. Therefore, the combination of strategies of HSA and grouping is essential for success.

Figure 5.5 illustrates one solution for high number of SMs. The SMs are divided into *K* groups, each with the same number of SMs, and *K* is selected based on the desired number of SMs in the sub-groups. For example, if the desired number of one sub-group is 3, *K* equals to the integer part of *N*/3. Then the CSA is applied to the *K* groups to determine the distribution sequence of the inserted number *n*. The rest of the steps are listed as follows:

1. The integer part of *n/K* is calculated, mark as [*n/K*]. This step determines the basic switching rounds. Then, one SM is switched on for every *K* groups for [*n/K*] rounds. Thus, [*n/K*]**K* SMs have been inserted into the circuits.

2. The distribution of the other (n-[*n/K*] **K*) SMs is then determined. If arm current $i_{arm} \geq 0$, from the lowest group to the highest group, one SMs from each group is inserted. However, if $I_{arm} < 0$, from the highest group to the lowest group, one SMs from each group is inserted. The number of groups inserted during this procedure is marked as n_K.

3. The heap sorting algorithm or HSA is subsequently applied for K groups based on n_K, V_C and i_{arm}.

It is worth noting that if the number of SMs cannot be divided evenly, the proposed scheme can still be used. The solution is to ignore the different groups during step 2. Meanwhile, if the value of K is still high after the grouping, the K groups can be further divided, and the distribution of the inserted number of SMs still follow the same procedures. For the real project with hundreds of SMs, three to four rounds of grouping are normally needed.

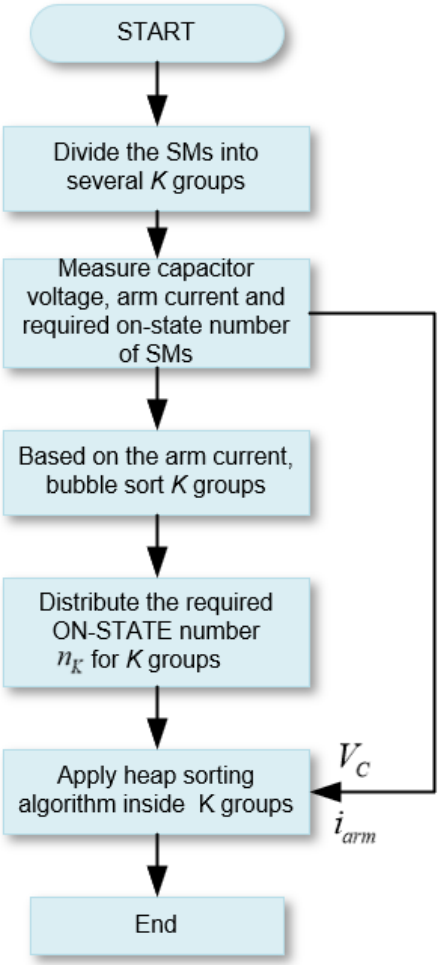


Figure 5.5 Flowchart of heap sorting algorithm with high number of SMs.

In order to give a better illustration of the condition with larger number of SMs, an MMC model with 21 SMs per arm can be taken as an example. In this case, at least a two-level grouping is needed to cope with higher number of SMs. According to Figure 5.6, the 21 SMs

are initially divided into K=7 groups evenly and each group contains 3 SMs. In Level 1 any sorting algorithm can be applied (including heap sorting) to sort the groups and allocate the required inserted number for each sub-group. In Level 2 the heap sorting algorithm is applied to each of the sub-groups and the SMs are switched on according to the allocated inserted number $n_1 - n_6$.

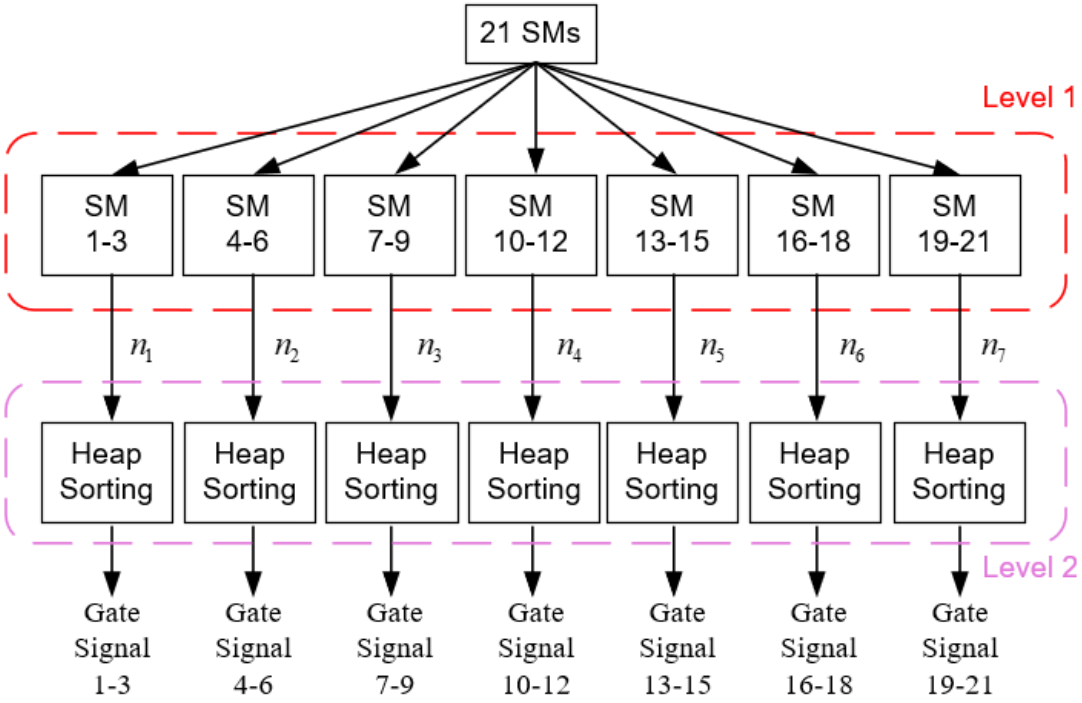


Figure 5.6 Specific 21-SM MMC to illustrate the grouping rules.

In this case, in one sampling period, if the required number n=15, according to the previous analysis, the first step is to calculate the integer part of n/K=2, which means that there are 2 rounds of gate signal distribution, and thus in each group 2 out of 3 SMs are selected based on the sorting within the groups. Then, in the third round, only [n- (n/K)] =1 SM is waiting for group assignment, and so the group with the lowest value is going to change all its SMs to become inserted. Finally, the gate signals are all determined by HSA.

5.6 Analysis and Characteristics of HSA

In contrast to the conventional bubble sorting algorithm, the HSA only needs to compare some of the SMs in one sampling period. The first step is to build up the heap tree, and the worst-case scenario is taken into consideration when dealing with the CT. For example, when $i_{arm} >$

0, which means that the arm current is charging the arm, the max heap tree should be built. However, in this scenario, the existing SMs are listed in the ascending direction, and therefore every element adding to the nodes must swap the position with its previous elements so that the CT is equal to the number of elements *N*.

After building-up the heap tree, only one level needs to be sorted. Again, the worst case is that most of the elements inside the max level need to be sorted, with the most extreme number being $(2^{\mathbf{Y}_{max}-\mathbf{1}}-1)$. Therefore, concluded from equation 5.1, for *N* SMs in one MMC arm the worst-case total comparison which needs to be made is:

$$T_2^{worst} = N + \frac{(2^{\mathbf{Y}_{max}-\mathbf{1}}-1)(2^{\mathbf{Y}_{max}-\mathbf{1}}-2)}{2} \tag{5.2}$$

It is evident that:

$$2^{\mathbf{Y}_{max}-\mathbf{1}} \leq \frac{N}{2} \tag{5.3}$$

So, adding equation 5.4 to equation 5.3, the worst-case total CT is:

$$T_2^{worst} \leq N + \frac{(N-2)(N-4)}{4} \tag{5.4}$$

Or it can be expressed as *N*-*1*+ (*N*-1)/2, where the first part *N* is used in building the heap tree and the second part is used for sorting its max level. Again, with the possibility of heap sorting activation D_p which represents the period when $\Delta n \neq 0$, it is obvious that $D_p \ll 1$.

$$T_2^{worst'} = D_p \cdot T_2^{worst} \tag{5.5}$$

Finally, based on equation 4.2, a clear conclusion can be drawn that the HSA sorting time T_2 is:

$$T_2 \ll T_2^{worst'} \ll T_0 \tag{5.6}$$

where T_0 is the sorting time of the CSA. Equation 5.6 proves the effectiveness in the reduction of computational complexity with the proposed HSA compared to the CSA.

The reduction in switching from the proposed HSA strategy primarily relies on avoiding

unnecessary switching when the number of the inserted SMs does not need changing. However, when the required number does need to be changed, this reduction relies on only several of the SMs involved in switching events. Nevertheless, this unnecessary switching still exists because the bubble sorting is still applied to some of the SMs. Also, this scheme can be improved by combining it with other reduction arrangements. Therefore, further reductions of switching frequency can be achieved. Overall, HSA is a highly efficient and effective technique for the application of MMC, but it must work in conjunction with other techniques.

The CT is reduced significantly because only one level from the heap tree needs to be compared. In the worst-case, the lowest level needs to be sorted, which indicates that nearly half of the SMs do not require comparison, and the worst-case also appears for half of the conditions, and thus the computational complexity is reduced.

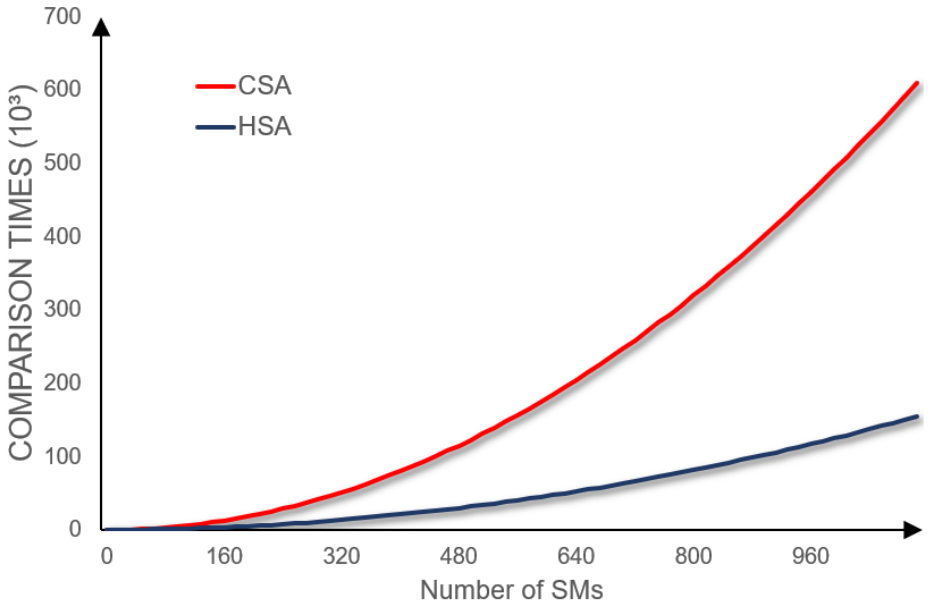


Figure 5.7 Comparison of computational complexity between HSA and CSA.

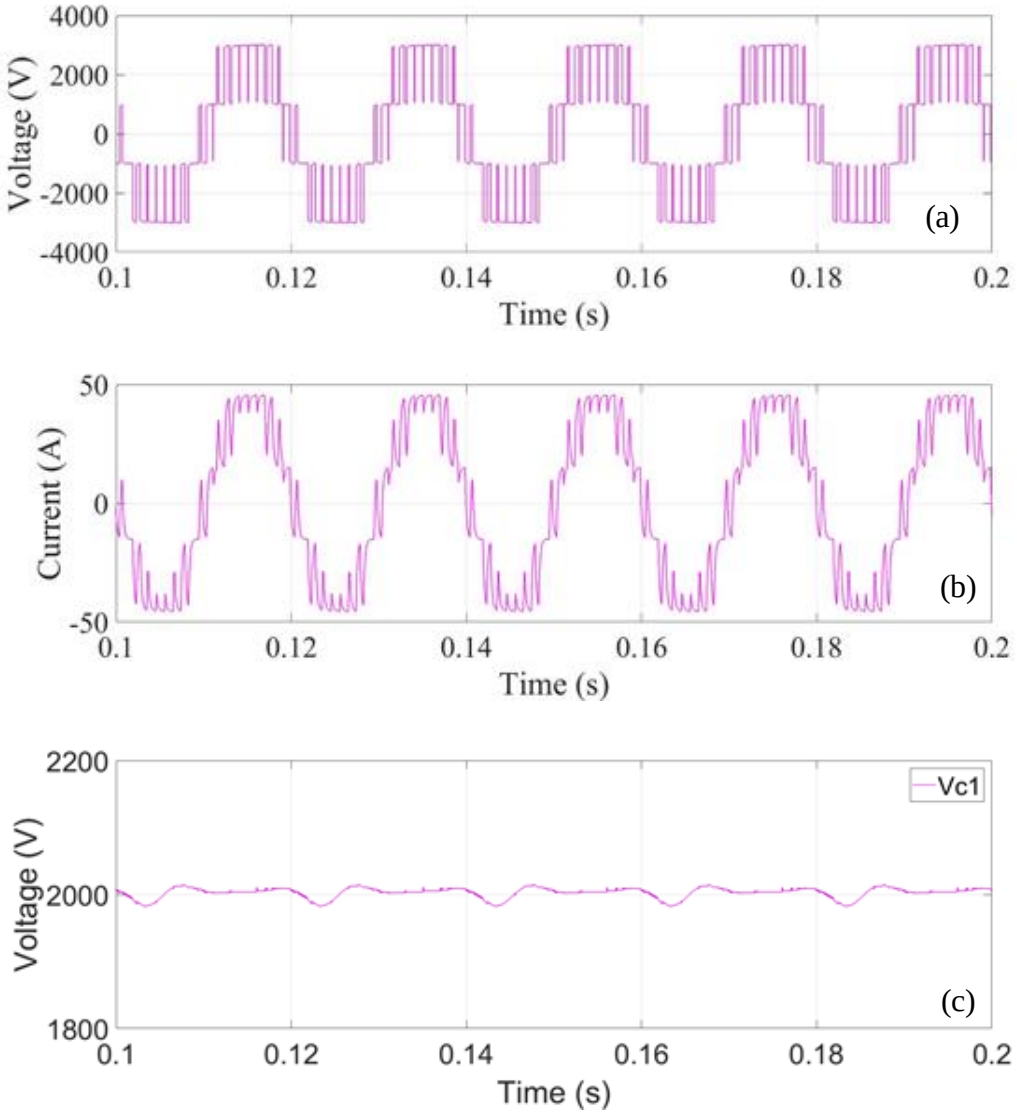
A comparison of HSA and CSA is shown in Figure 5.7, where the CT of the two algorithms with respect to the number of SMs are illustrated. It can be concluded from the figure that the computational complexity of CSA increases exponentially, whist the HSA exhibits a reduction of more than 75% in computational complexity.

5.7 Simulation Results

The simulation studies conducted have the same parameters described in Chapter 4. The main system parameters used in the simulation are listed in Table 4-II. The performance of the heap sorting algorithm and HSA is investigated in this section, and then set against the results for the CSA and ISA presented in Chapter 4, so that the performance of the HSA can be evaluated.

5.7.1 Steady-state performance of heap sorting algorithm

It can be seen from Figure 5.8, the heap sorting algorithm balances the voltage of SMs effectively. With regards to the CSA, the heap sorting algorithm does not have a negative impact on the output voltage and current.



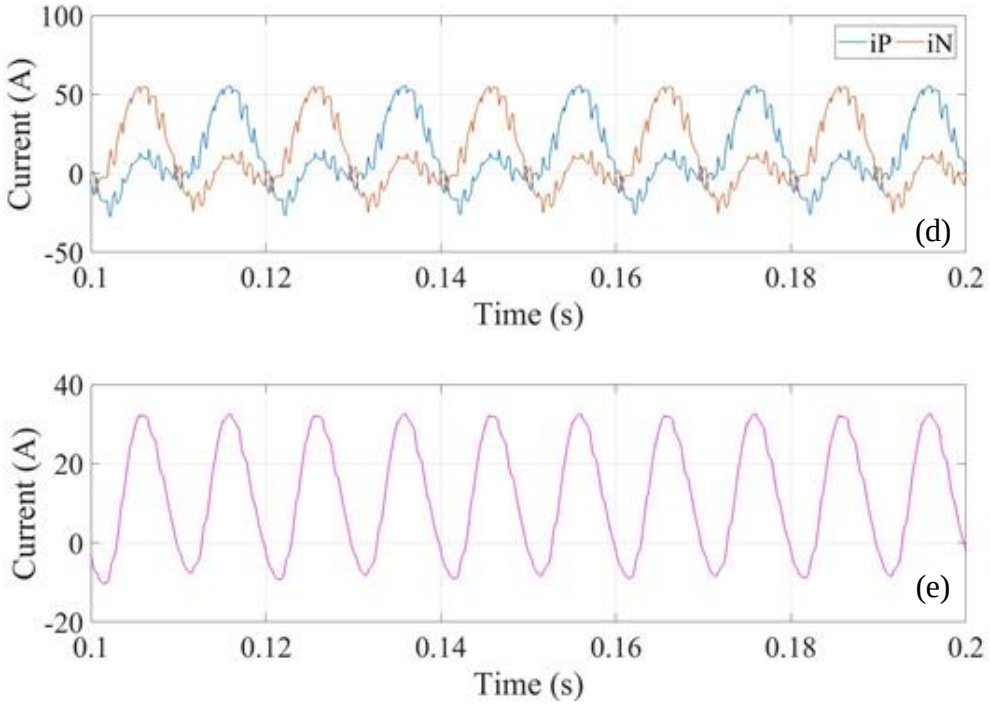
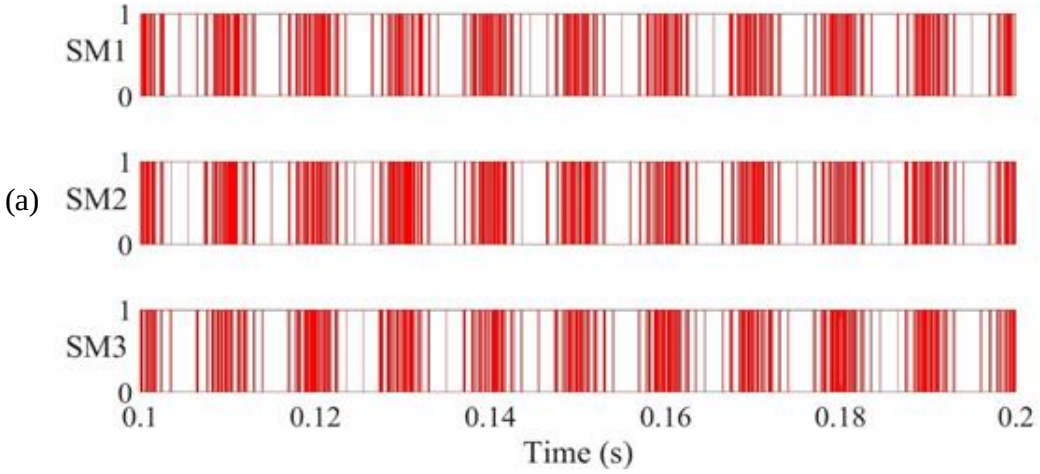


Figure 5.8 Simulation results of heapsorting algorithm. (a) Output load voltage. (b)Output load current. (c)Voltage across C1. (d)Upper arm and lower arm current. (e) Circulating current.

Figure 5.9 to Figure 5.11 shows that there is no substantial difference between CSA and heap sorting algorithm in terms of capacitor voltage, because it still sorts all the SMs every single sampling period. The average switching frequency for entire upper arm is 3320 Hz. The fluctuation of upper arm capacitor voltage is 1%. From Figure 5.11, the voltage variation is slightly increased, but still track the others' values closely.



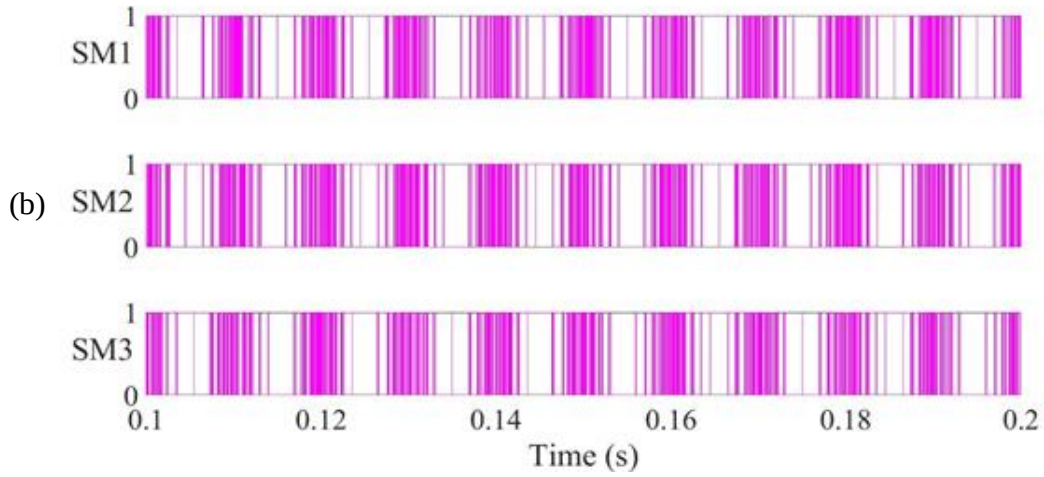


Figure 5.9 Simulation results of gate signal for upper arm SMs with different voltage balancing algorithms. (a) CSA. (b) Heap Sorting algorithm.

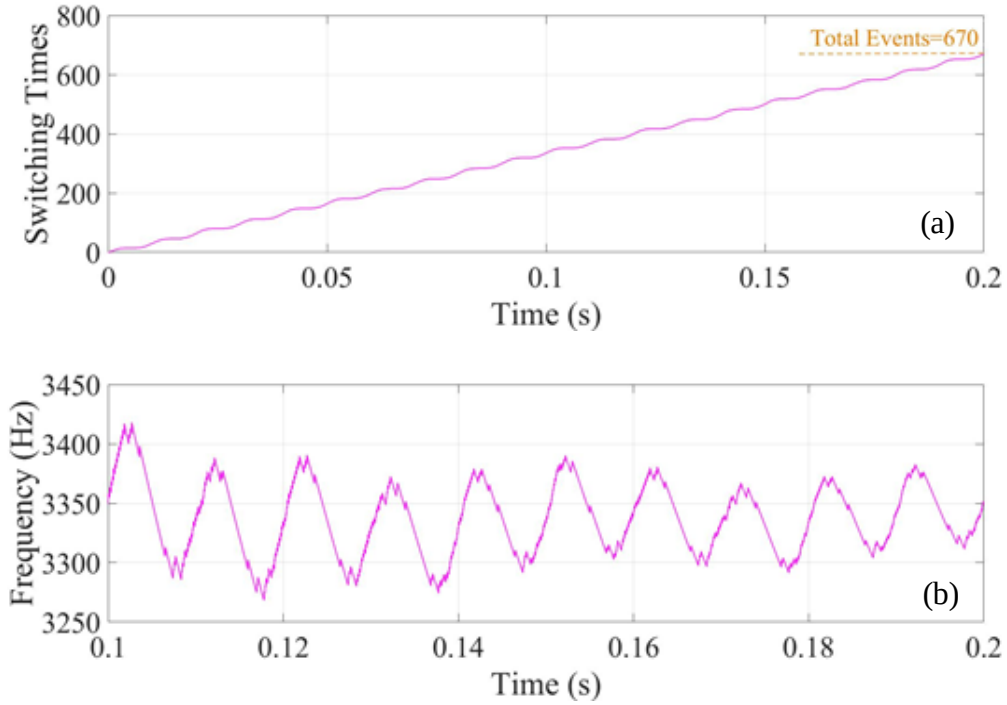


Figure 5.10 Switching condition of SM1 based on heap sorting algorithm. (a)Switching events. (b)Average switching frequency.

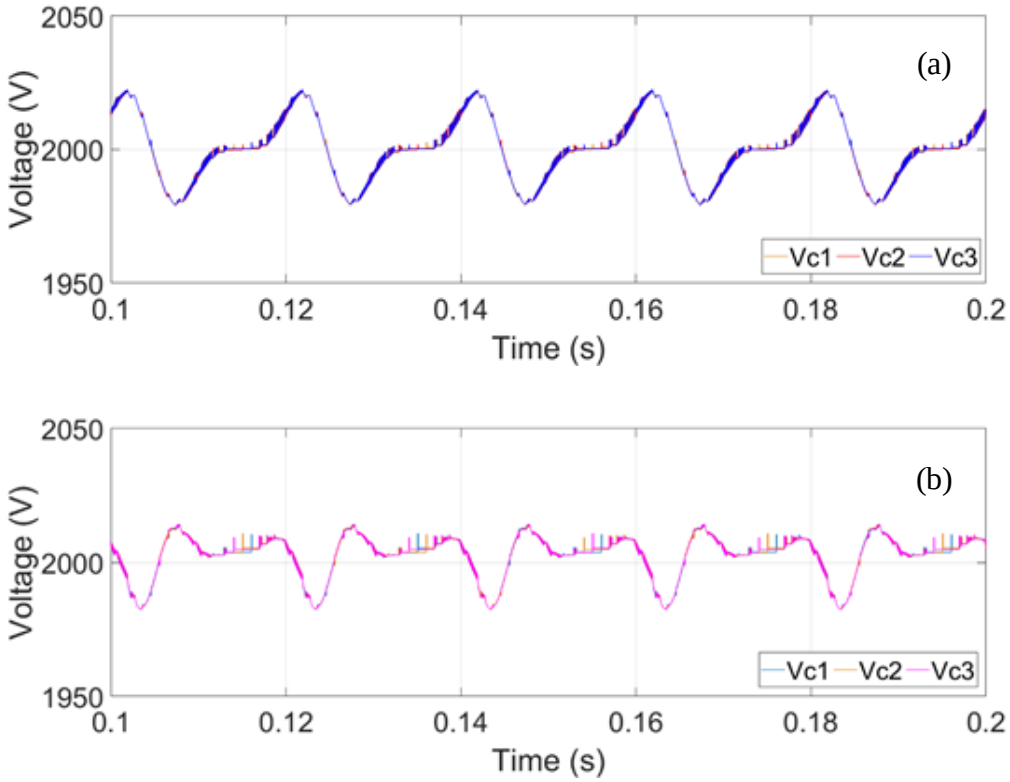
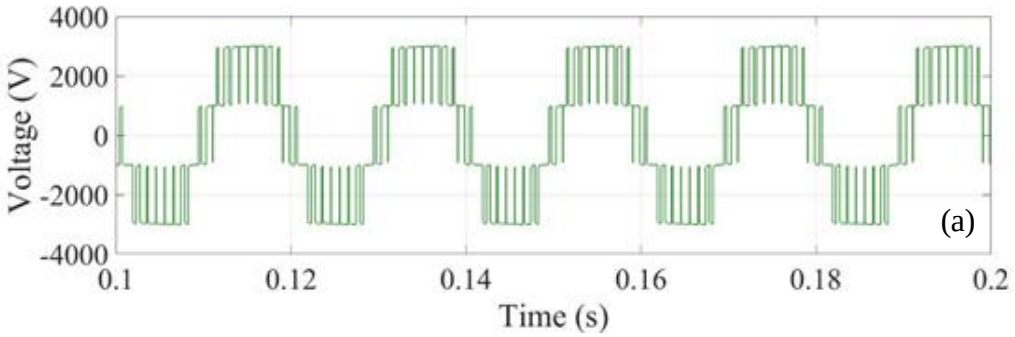


Figure 5.11 Capacitor voltage ripple performance comparison of upper arm. (a) CSA. (b)Heap sorting algorithm.

5.7.2 Steady-state performance of HSA

Even though the heap sorting algorithm does not effectively reduce the frequency, it reduces the computational complexity. The proposed HSA is tested in this section, and it can be observed from Figure 5.12, the HSA has similar performance when compared to CSA, thus the effectiveness of HSA can be verified.



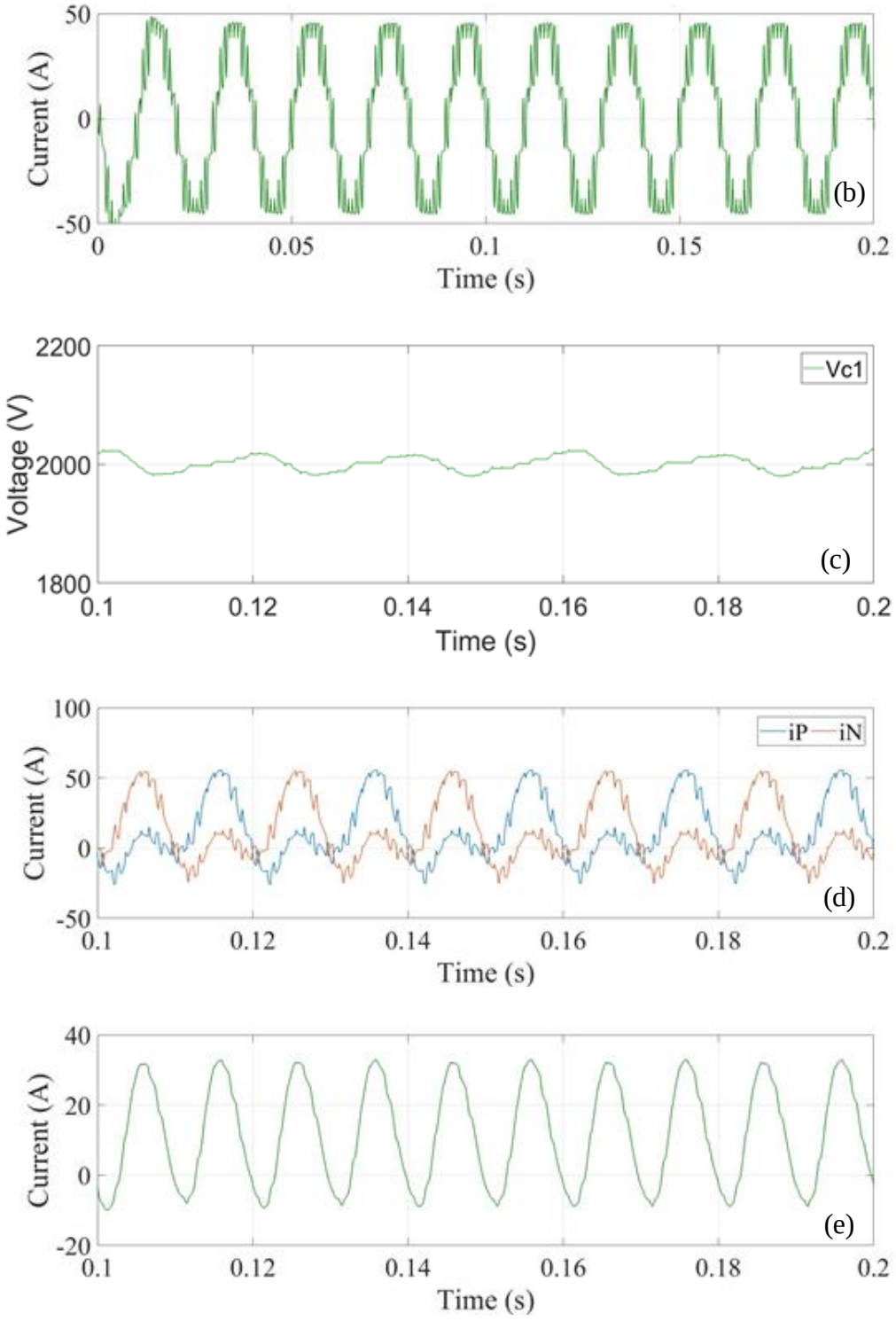


Figure 5.12 Simulation results of conventional sorting algorithm. (a) Output load voltage. (b) Output load current. (c) Voltage across C1. (d) Upper arm and lower arm current. (e) Circulating current.

Figure 5.13 compares the difference between CSA and ISA in terms of the gate signal of upper arm SMs. It is obvious Figure 5.13 (b) from HSA has fewer switching events compared to CSA from Figure 5.13 (a) within the same period. Figure 5.14 demonstrates the average

number of switching transition events and the average switching frequency of upper arm for HSA within 0.1s. Compare to CSA from Figure 4.7, it shows that HSA has better performance in terms of frequency reduction, which reduced the average switching frequency from 3350 Hz to 440 Hz. The outcome shows HSA even has better ability in terms of switching frequency reduction compared to ISA with 510 Hz with 13% reduction. Overall, the effectiveness of switching frequency reduction of HSA has been confirmed by the simulation results.

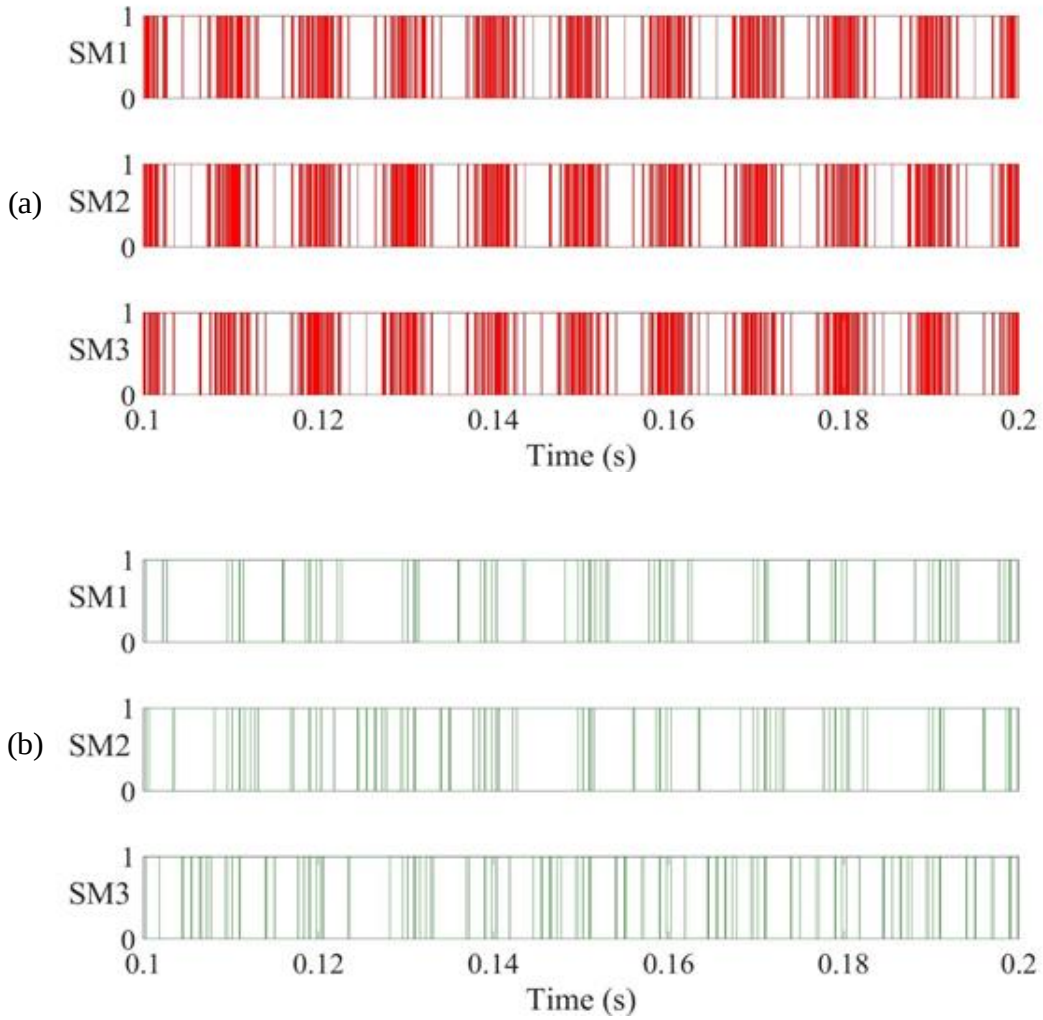


Figure 5.13 Simulation results of gate signal for upper arm SMs with different voltage balancing algorithms. (a) CSA. (b) HSA.

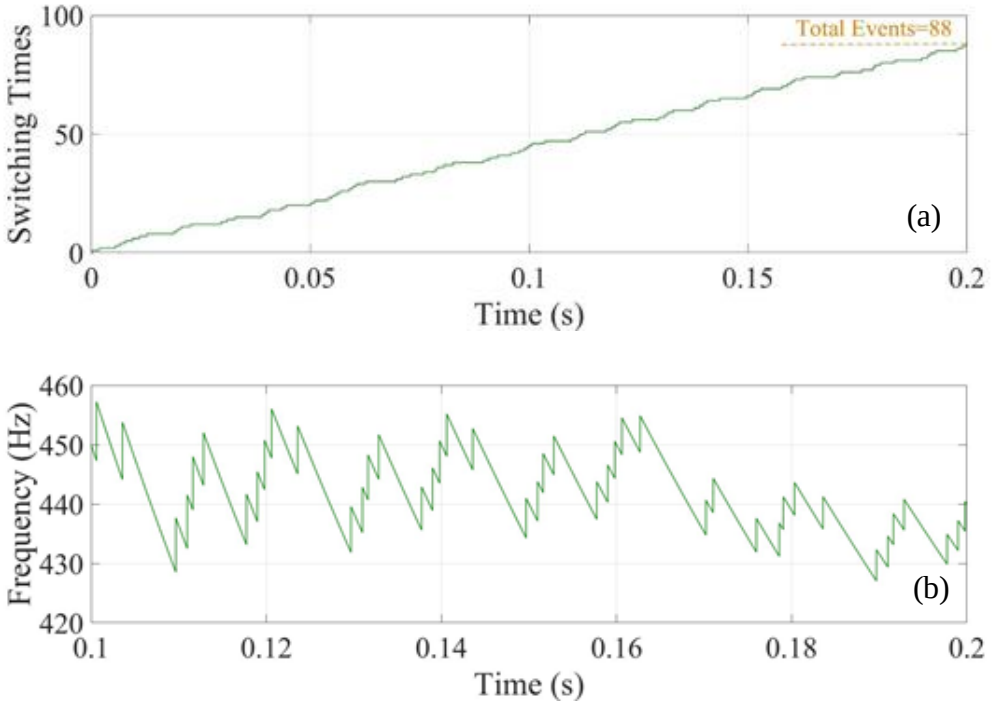


Figure 5.14 Switching condition of SM1 based on HSA. (a)Switching events. (b)Average switching frequency.

Figure 5.15 compares the difference between CSA and ISA in terms of capacitor voltage ripple, the capacitor voltages are no longer requires strictly identical, so that the SMs are highly likely to maintain their switching state, which can be verified by that HSA from Figure 5.15 (b) has more flexibility compared to CSA from the Figure 5.15 (a). The capacitor voltages of HSA have slight variations from each other, but the variation is still within the fluctuation range. In comparison with the ISA in Figure 4.10 (b), the variation is larger, but the switching frequency is slightly smaller. Therefore, it can be concluded that, the less ability to maintain the voltage of SM to become identical, the less switching frequency. The design of improving the sorting algorithm is to have the optimum arrangement with acceptable voltage variation. The capacitor voltages of HSA are clearly having a longer period to maintain their gate signals, due to the contribution of the combined algorithm. However, voltage stress is also increased, which requires further consideration in the future.

Figure 5.16 shows the harmonic distribution with the help of (FFT) of the heap sorting algorithm and HSA during the steady-state. From the figure, the THD of HSA is 1.7% higher than the heap sorting algorithm, and the THD of heap sorting algorithm is same as the CSA in

Chapter 4. Compared to ISA, HSA is also 1.3% higher, this increment is can be ignored considering the overall high THD for a 4-level MMC model.

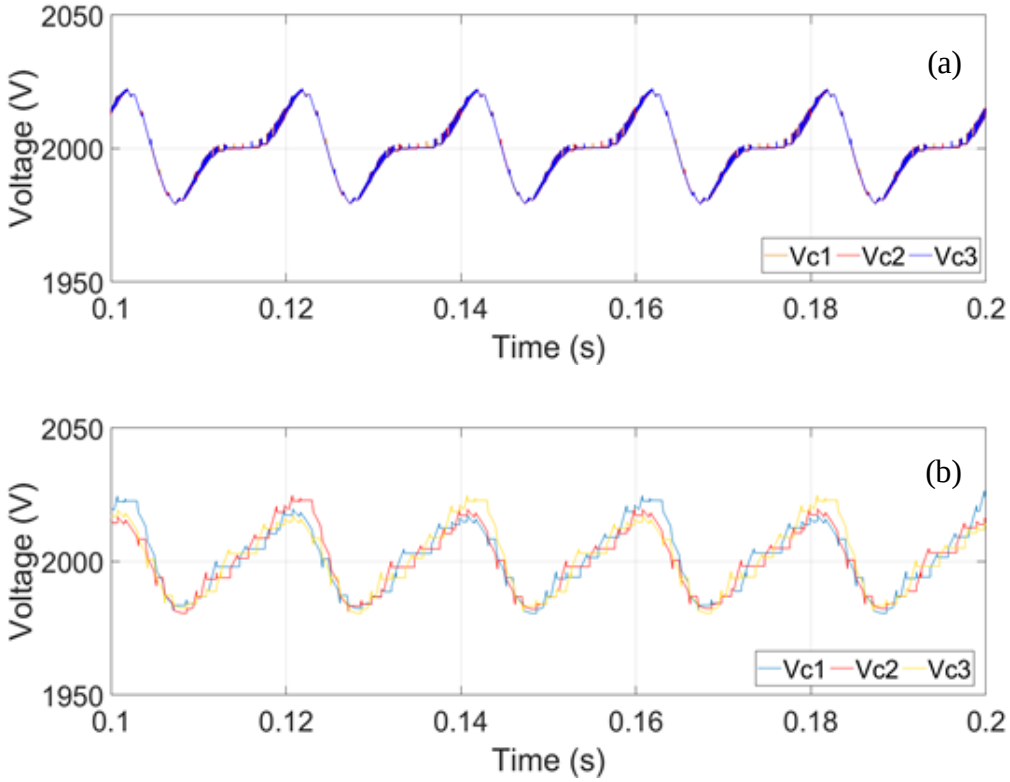
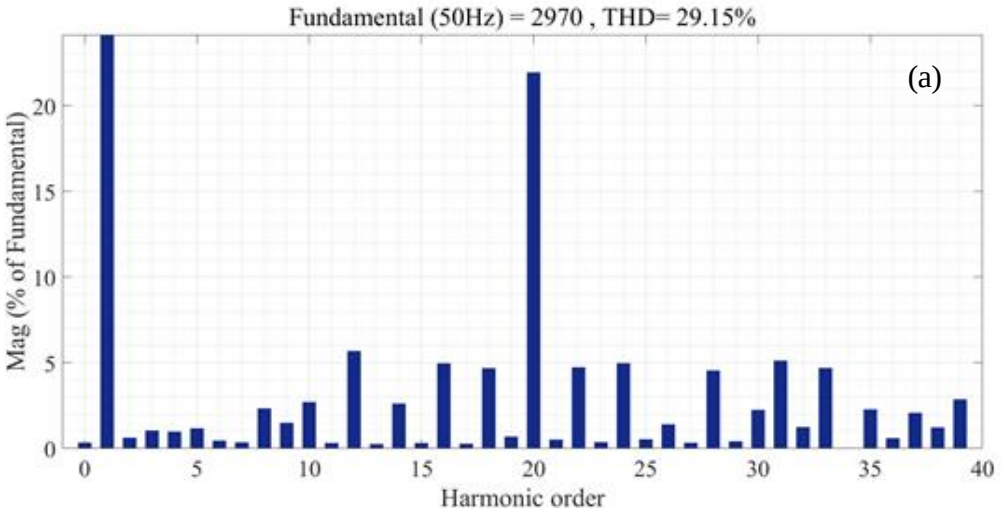


Figure 5.15 Ripple performance comparison of upper arm. (a) CSA. (b)HSA.



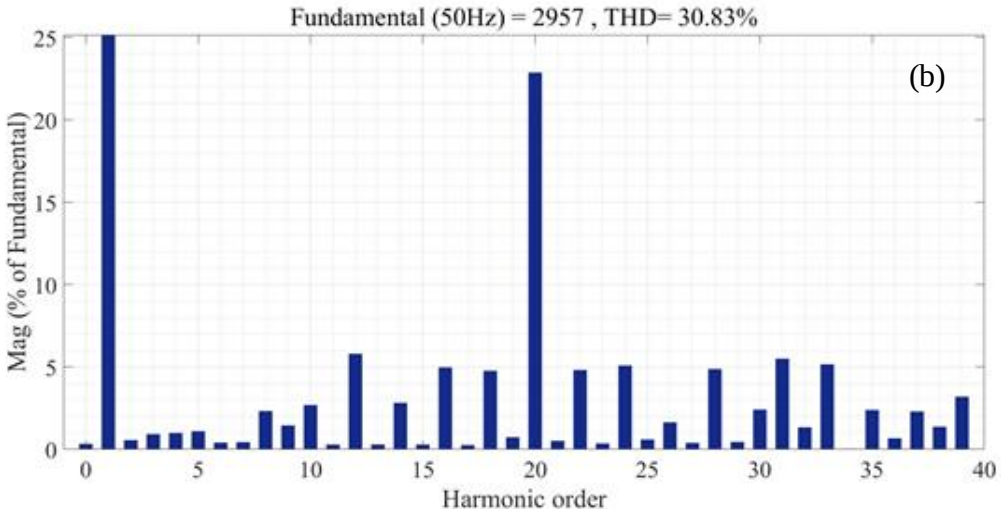
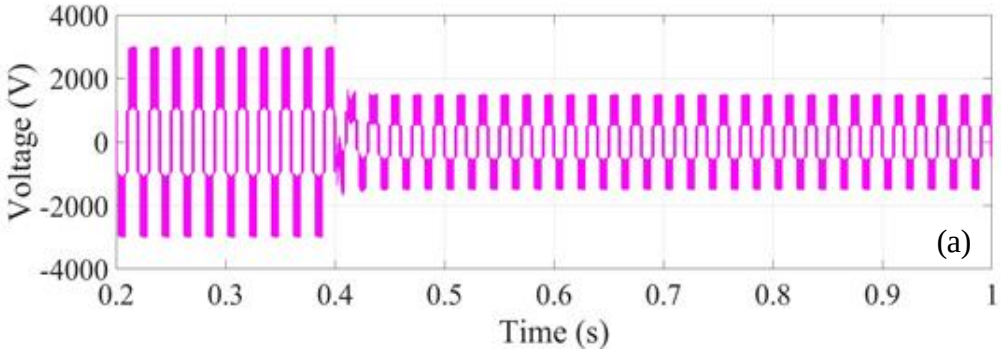


Figure 5.16 Output voltage harmonic performance of (a) heap sorting algorithm and (b) HSA.

5.7.3 Performance during a step change of DC side

The dynamic response of the proposed algorithms is tested, with a step change in the DC side is applied at t=0.4. The DC source is decreased 50% of its original value, drops from 6000V to 3000V. The comparison is made between the heap sorting algorithm and HSA in terms of the output voltage, output current and capacitor voltage.

It can be seen from Figure 5.17 (c) and Figure 5.18 (c), the capacitor voltage of heap sorting and HSA are both able to re-balance at =1000V for less than 0.1s. The capacitor ripples have converged to a new reference voltage rapidly and get re-balanced in 10ms. The results depicted in Figure 5.18 of HSA are close to the results of CSA and ISA algorithms with a step change shown in Figure 4.12 and Figure 4.13, there exist a deviation of ripple during the transient period for HSA, but the overall performance is still acceptable.



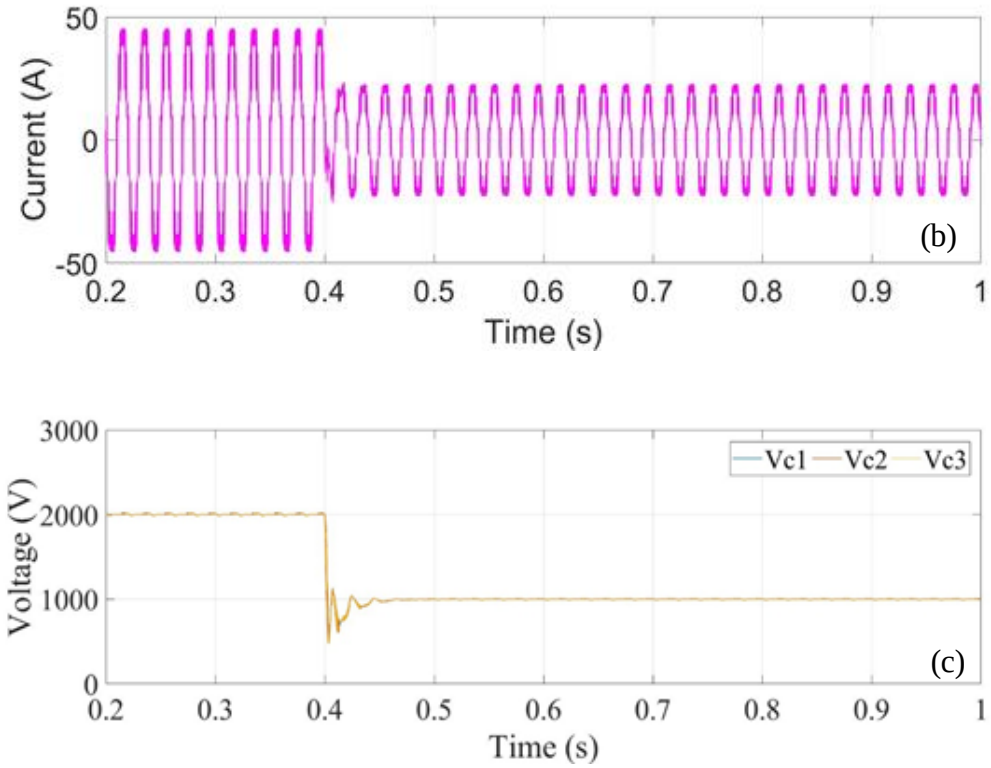
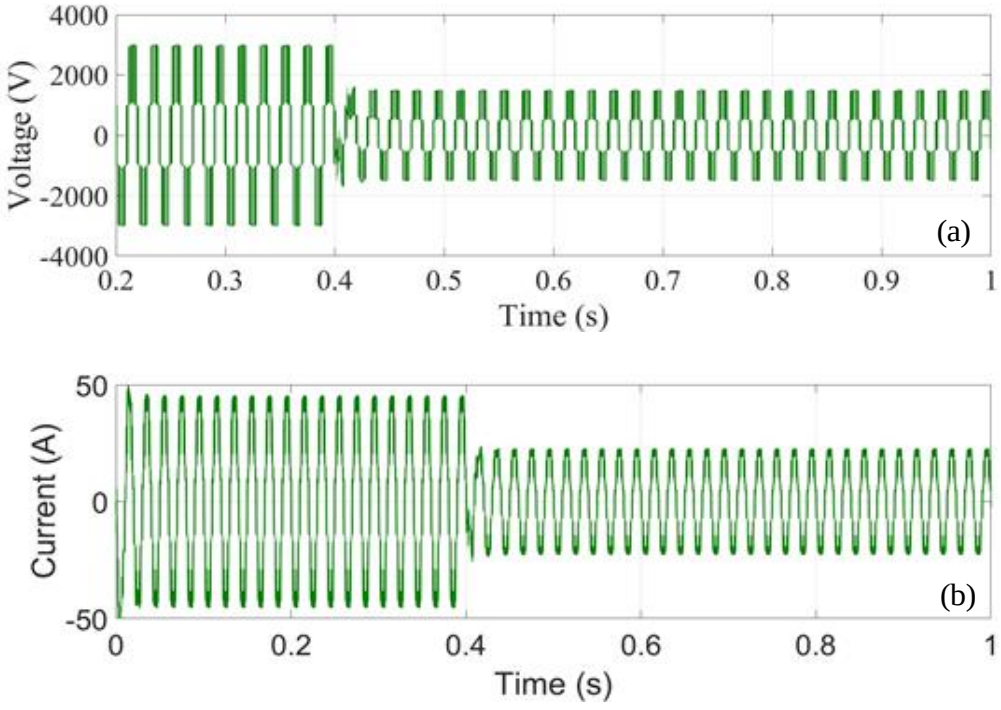


Figure 5.17 Simulation results for DC step change under heap sorting scheme. (a) Output load voltage. (b) Output load Current. (c) Capacitor voltage of upper arm.



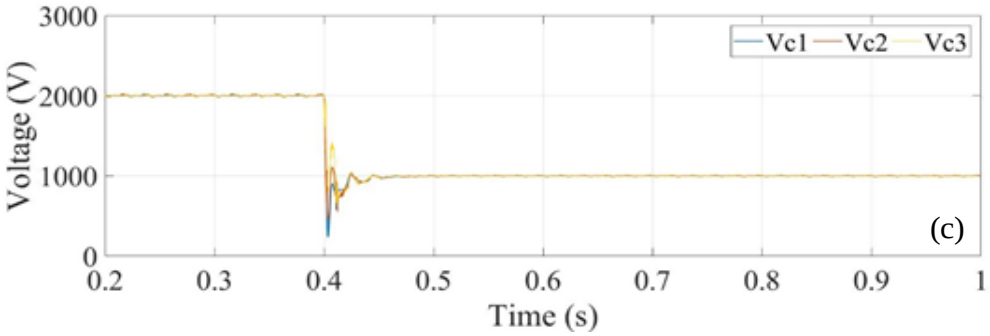


Figure 5.18 Simulation results for DC step change under HSA scheme. (a) Output load voltage. (b) Output load Current. (c) Capacitor voltage of upper arm.

5.7.4 Implementation of Interleaving for heap sorting and HSA

Figure 5.19 shows the response of heap sorting algorithm when applying interleaving modulation technique for the upper arm at t=1s. The expectation of output level is altered from 4-level to 7-level. The output voltage waveform in Figure 5.19 (a) achieved the increasement of output level very quickly. From Figure 5.19 (b), the output current has a good response for interleaving, indicating that the size of the load filter can be reduced. Figure 5.19 (c) and (d) demonstrates the dynamic response of capacitor voltage. The ripples fluctuation of it increased from 1% to 5%, because the circulating current is increased from 50A to 200A. That drawback of the interleaving modulation scheme, to increase the distortion and make the system unstable, limit its application. Compared to the results of CSA in chapter 4, the heap sorting algorithm has no detrimental impact on the system performance with the computational complexity reduction.

Figure 5.20 shows the response of HSA when interleaving modulation scheme is applied for the upper arm at t=1s. Compared to the CSA and heap sorting algorithm, the dynamic response of output is similar according to Figure 5.20 (a)and (b). It can be seen from Figure 5.20 (c) and (d), the voltage ripple and circulating current of HSA is still close to the performance of CSA and ISA that showed in Figure 4.14 and Figure 4.15 respectively. Therefore, it can be conducted that the HSA does not sacrifice the dynamic performance in achieving both switching frequency reduction and computational complexity reduction.

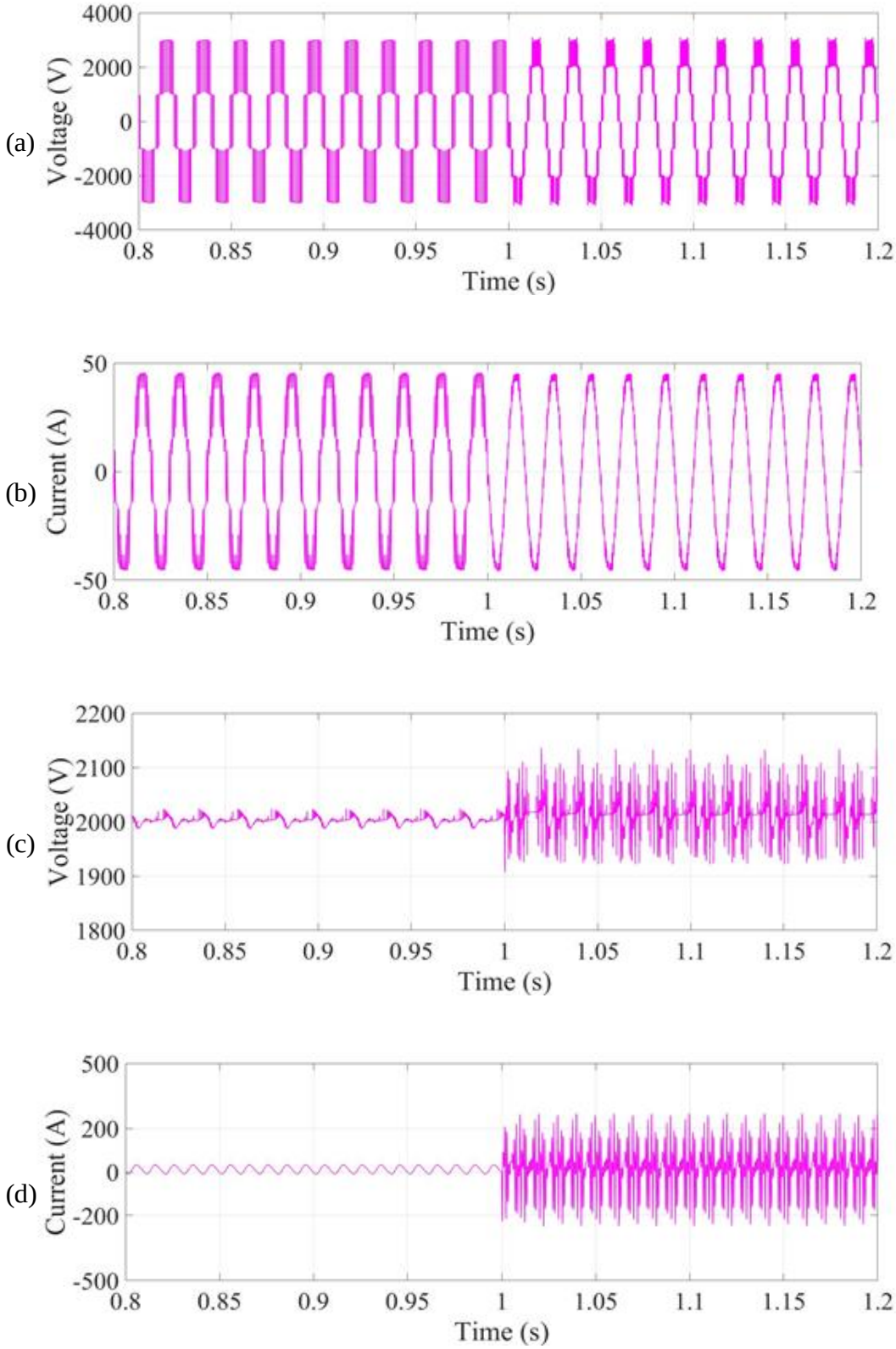


Figure 5.19 Simulation results for applying interleaving modulation scheme 4-level MMC with heap sorting (a) Output load voltage. (b) Output load Current. (c) Capacitor ripple voltage of SM1. (d) Circulating current.

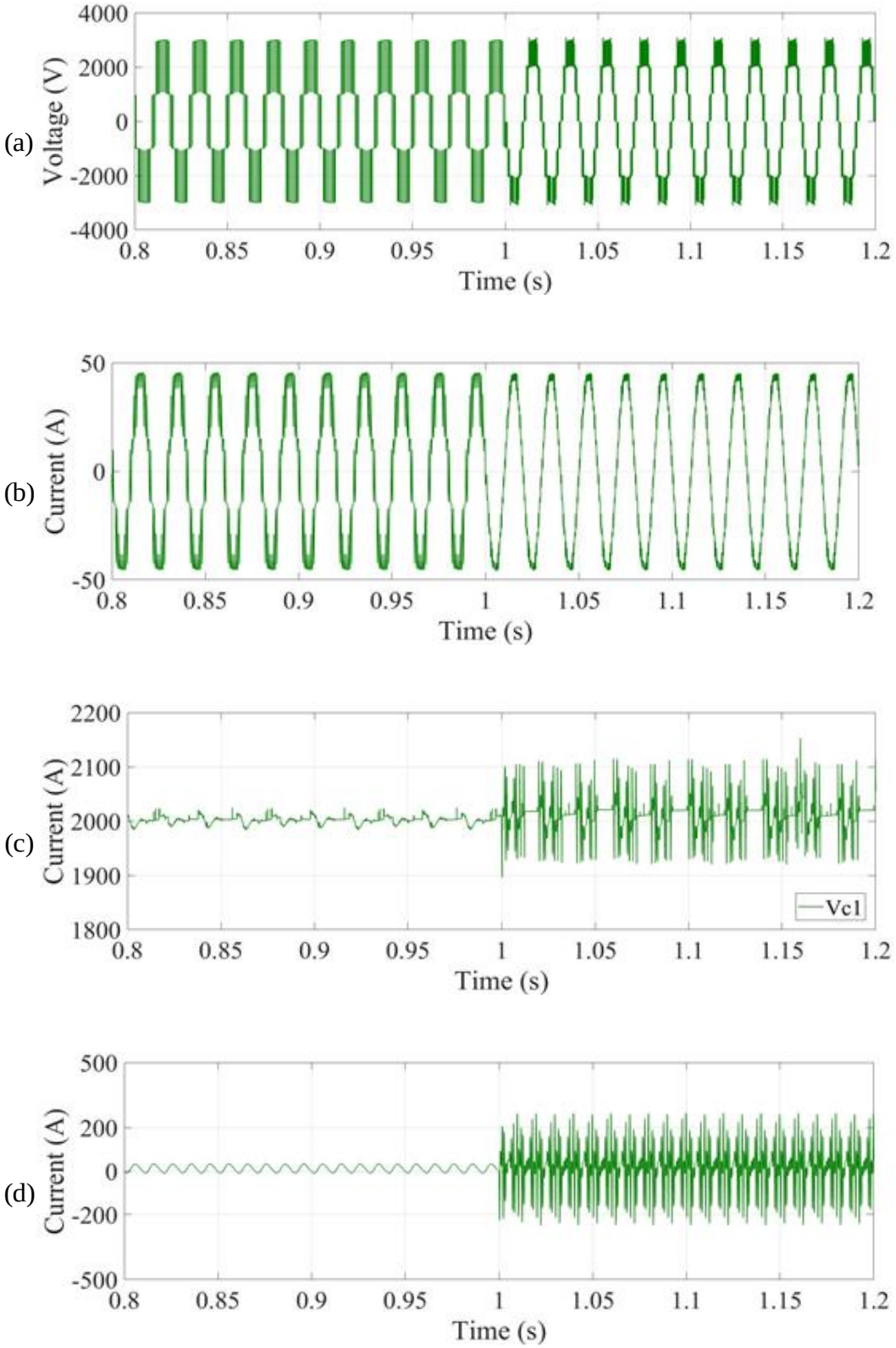


Figure 5.20 Simulation results for applying interleaving modulation scheme 4-level MMC with ISA (a) Output load voltage. (b) Output load Current. (c) Capacitor ripple voltage of SM1. (d) Circulating current.

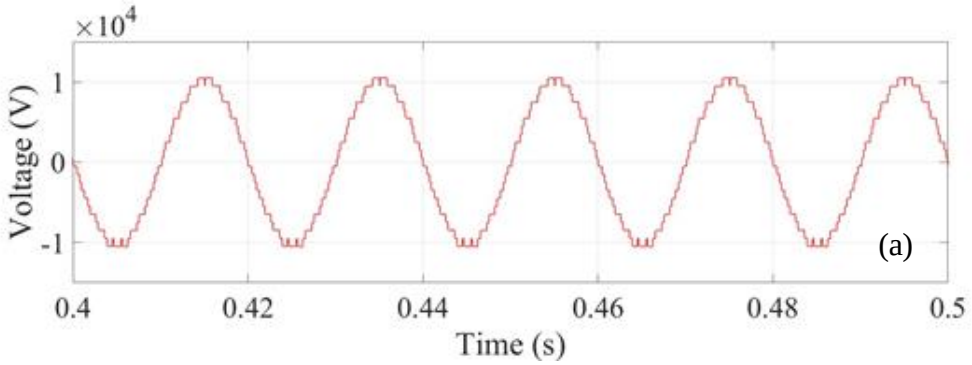
5.7.5 *Performance of HSA with high number of SMs*

In order to verify the effectiveness of the proposed heap sorting algorithm, further investigation is taken by increasing the number of SMs and voltage level of output. The SMs increased from 3 to 21 and the modulation scheme is N+1. The main parameter is still from Table 4-II, the new parameters have been updated and listed in Table 5-II. The sampling frequency is still 20 kHz throughout the whole experiment.

Table 5-II Parameters of MMC with high number of SMs.

Parameter	**Value**
SMs per arm N	21
Output level (N+1)	22
DC source voltage (V_{DC})	2.1 KV
Arm inductance (L)	6.0 mH
Load inductance (L_L)	10.0 mH
Load resistance (R_L)	660 Ω

Figure 5.21 exhibits the performance of CSA for 21-SM MMC with 50Hz fundamental frequency. The voltage of AC output is 10500V with 21 levels, the peak output current is 16A. The peak current is 12A and the ripples oscillation is around 1%.



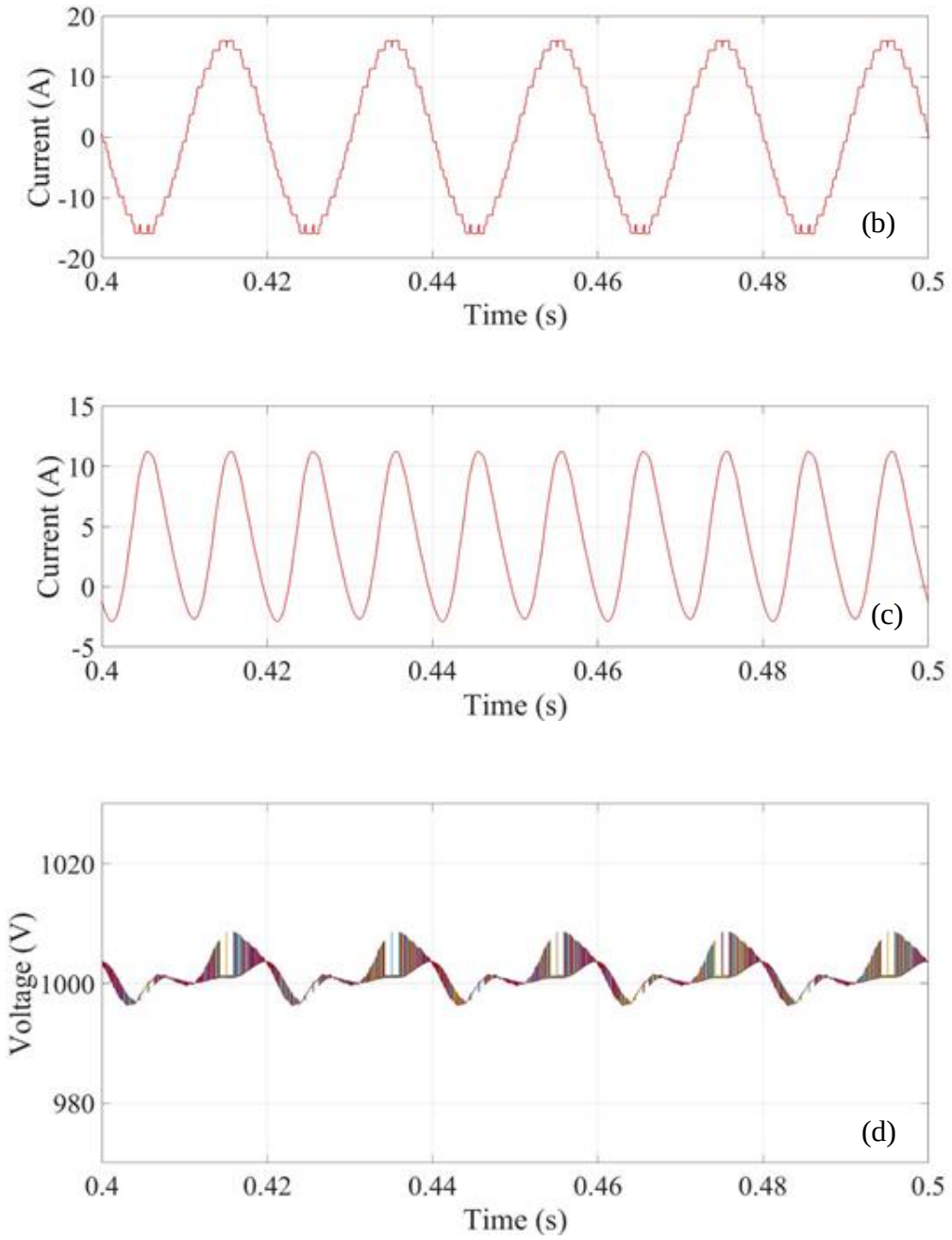


Figure 5.21 The performance of CSA with 21 SMs per arm. (a) Output voltage. (b) Output current. (c) Circulating current. (d) Capacitor voltage ripples of upper arm.

The simulation results of the example shown in Figure 5.6, where 21 SMs are clustered into 7 identical groups. With the help of HSA, the computational complexity is reduced with less switching frequency. The results of the example are shown in Figure 5.22, compared to results of CSA shown in Figure 5.21, all the performance is close except the computational complexity has been extremely decreased.

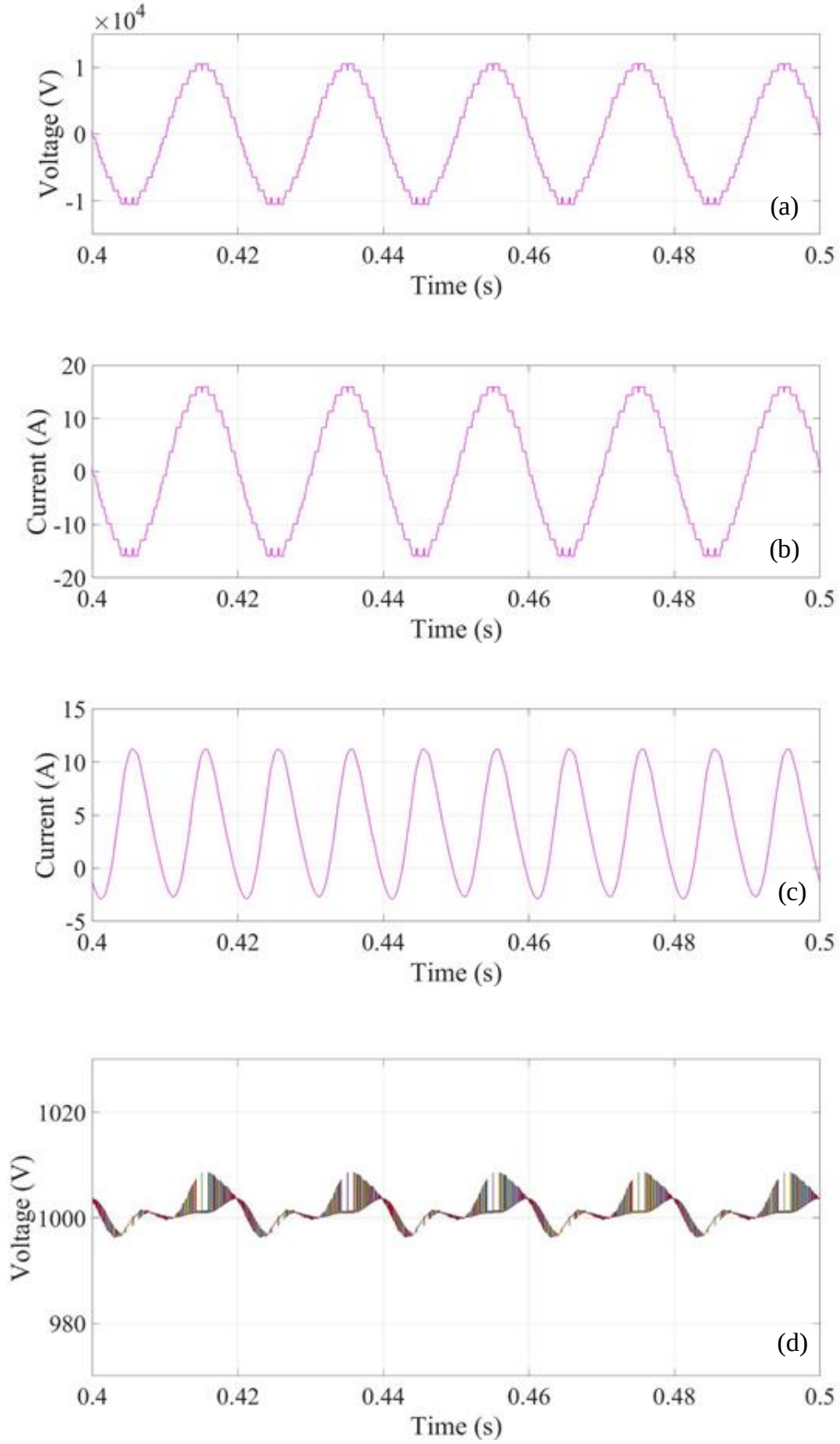


Figure 5.22 The performance of heap sorting with 21 SMs per arm. (a) Output voltage.

(b) Output current. (c) Circulating current. (d) Capacitor voltage ripples of upper arm.

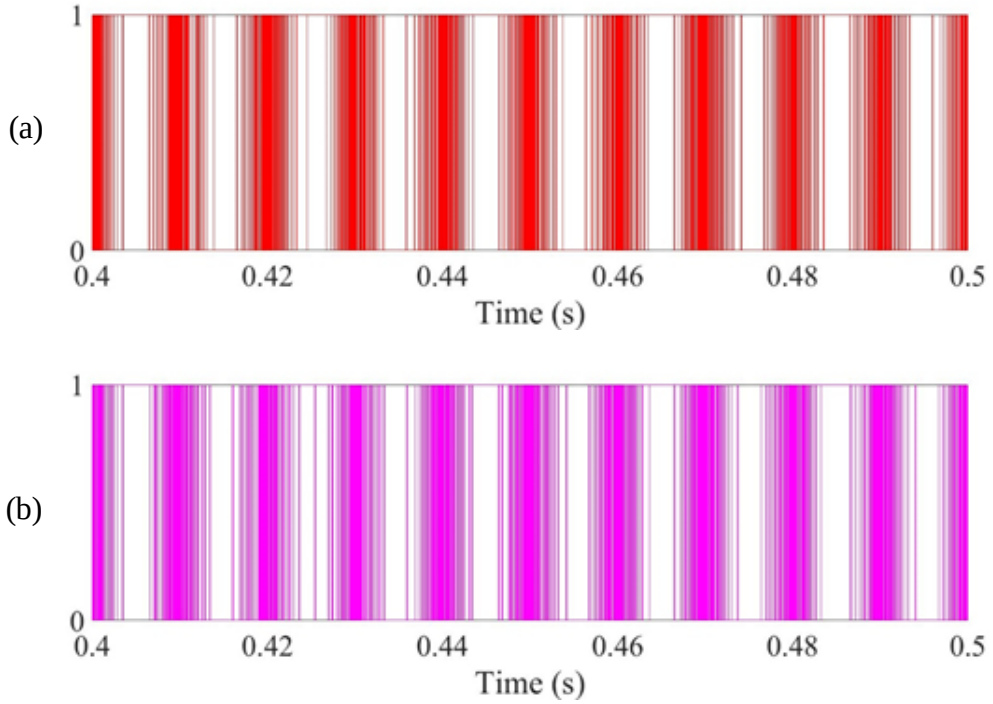
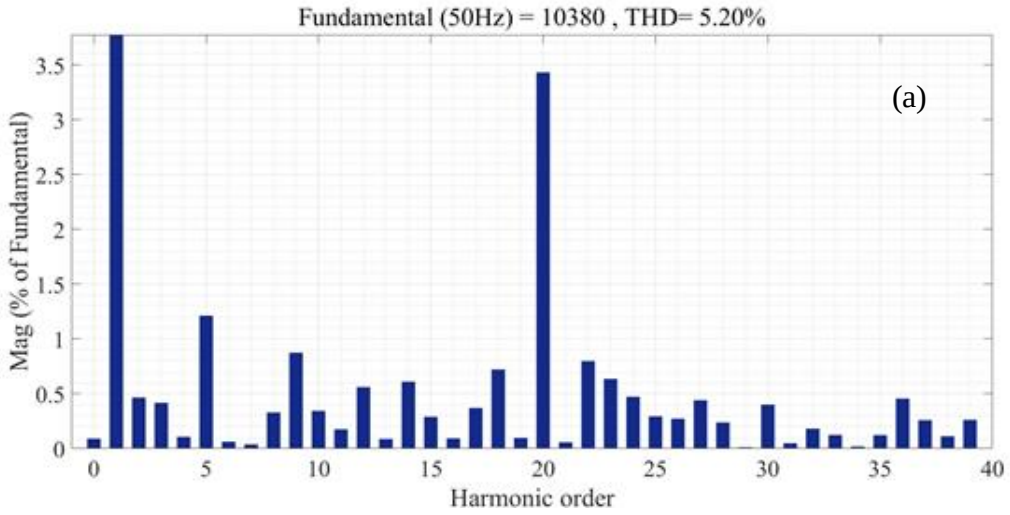


Figure 5.23 Simulation results of gate signal for SM1 with different voltage balancing algorithms for high number SMs. (a) CSA. (b) Heap Sorting algorithm.



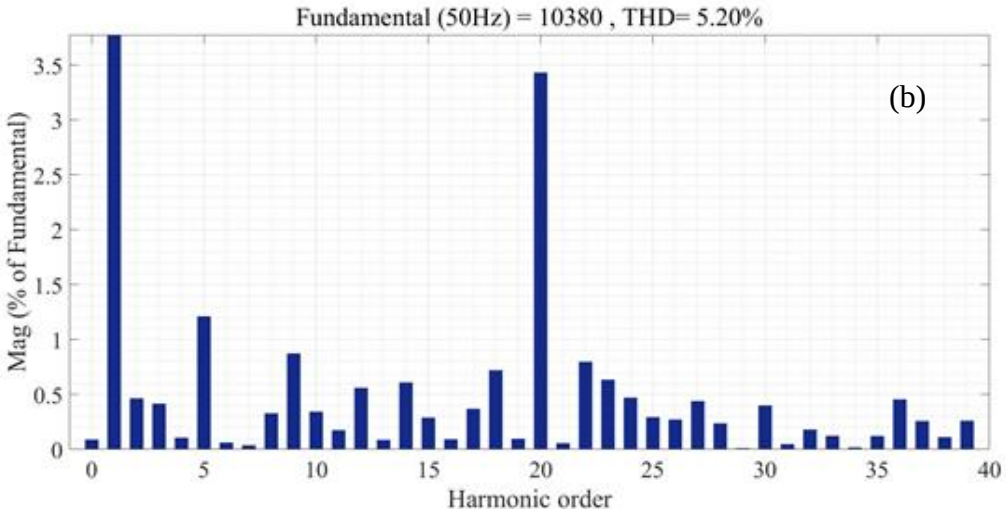


Figure 5.24 Voltage harmonic performance for 22-level MMC model. (a) CSA. (b) Heap Soring Algorithm.

Figure 5.24 shows the harmonic distribution with the help of FFT tools of MATLAB/Simulink. Compared the CSA with HSA during the steady-state for a 22-level MMC model. From the figure, the THD of CSA and HSA are almost the same at 5.20%. Compared to the harmonic performance of the 4-level model, the THD of voltage is reduced more the 20%. Therefore, the further improvement of MMC can be achieved by stacking more SMs for one arm.

5.8 Chapter Summary

In this chapter, another new voltage balancing strategy for MMCs was proposed where the heap sorting algorithm replaces conventional bubble sorting. A comprehensive study was carried out on the principle of this algorithm, and how it can be applied to MMC voltage balancing based on the characteristics of the heap tree. Due to these characteristics, only some of the SMs needs to be involved in the comparison process, and the heap sorting needs to be adjusted before implementing it to MMC. In addition, the effectiveness in computational complexity reduction was also proven mathematically. The advantages and disadvantages of heap sorting are explained in detail in this chapter, and two potential directions for optimisation have been introduced. One of these is to combine it with other methods to reduce switching frequency, in order to create an HSA strategy. The other strategy is to combine heap sorting with PFM, so as to implement the heap sorting for larger numbers of SMs. The effectiveness in switching

frequency reduction was verified through simulations which demonstrated that the proposed HSA strategy performs well in terms of voltage balancing achieving low switching frequency. This conclusion also holds for the model MMC with high number SMs (21).

Chapter 6. Priority-Based Sorting Algorithm

6.1 Introduction

A great number of voltage-balancing methods for MMCs uses the sorting algorithm, since it is one of the most effective algorithms in terms of voltage balancing and limiting capacitor voltage ripple. However, the implementation of the algorithm also brings both undesirable increases in unnecessary switching frequency and computational complexity. In the previous chapters, two solutions have been introduced with respect to the sorting algorithm itself and the switching events arrangement to overcome those disadvantages. Both still require the sorting of all the SMs prior to the determination of the gate signals. Therefore, given the remaining disadvantages, a new optimisation technique is essential, and this is discussed comprehensively in this chapter.

The proposed technique minimises the number of sorting actions as far as possible by grouping the SMs. An SM is first prioritised depending on its location with regards to a pre-set range as well as the gate signals of the previous sampling period. Within that range, the SM voltages can have the flexibility to vary, so that the SMs are highly likely to maintain their switching states. The proposed technique is based on a criterion where the SMs have been divided into six major priority groups in total before implementing the actual sorting actions. The use of these groups doubles the number of groups and halves the number of SMs inside each group compared to traditional tolerance-band methods, which helps in reducing the numbers of SMs involvement during the sorting process. Groups with lower priority are only activated when all of the SMs in the higher priority groups have changed their states. The main advantage of the proposed method is to contribute to narrowing down the comparisons within only one or two groups in every sampling period. Besides this, unlike with traditional grouping methods, the groups themselves are no longer required to be sorted before the SMs inside group are handled. Instead, a fixed sequence of action is implemented. Therefore, the sorting process

is simplified resulting in the avoidance of unnecessary switching events.

Apart from the groups inside the pre-set range, those SMs outside the range can be further divided into several additional groups with identical width based on voltage level. In an MMC with high number of SMs, these hundreds of SMs can be further divided into hundreds of groups. Therefore, according to the required modulation number *N*, again, only a few groups with high priority need to be involved in voltage balancing using the sorting algorithm. The switching frequency and computational complexity are thereby both decreased. Furthermore, as the prioritisation process is based on the pre-set range, analysis and testing need to be carried out to verify its improvement in terms of flexibility.

6.2 Design and Principles of PSA

The CSA is used to sort and judge individual SMs for involvement in switching in every sampling period. This causes unnecessary switching and may result in an extra burden on the hardware. One of the main reasons for the generation of unnecessary switching is when the SM voltage varies slightly, whereupon the algorithm still forces the SMs to change their states. These unnecessary switching events finally accumulate to increase the switching frequency and hence switching losses. One study [65] has attempted to reduce unnecessary switching by introducing the boundaries of capacitor variation voltages. If the variation exceeds the limit, the SM selection process will be triggered; if not, the SMs are maintained at the same voltage. This method enables the SMs within the limits to not be involved in the sorting process, but those outside the limit continue to incur unnecessary switching. Some proposed methods divide the SMs into several groups to reduce the number of switching event by only sorting specific groups, but it is difficult to ensure that the switching events avoided were all actually unnecessary.

The objective of the voltage balancing proposed by Qin [56] was to investigate the possibility of reductions in frequency. The voltage balancing method used does not force individual SMs to have identical voltages every sampling period, but rather ensures that the voltage ripple is restricted to within an acceptable range. Within that range, the SM voltage has the flexibility to vary. Thus, this thesis applied a pre-defined ripple range to help into classifying

the SMs prior to starting the algorithm. This range is insufficient to group-up the SMs because three groups can offer only limited help in reducing the switching frequency. Therefore, gathering information about existing gate signals can increase the efficiency of the classification with the help of a new rule for switching sequence. All of the information required already exists and is available for the sorting algorithm, so no extra hardware or measurement is necessary for the proposed method.

The previous analysis has highlighted the necessity to group all of the SMs prior to the SM selection process. The first step is to establish a reference ripple voltage range, and the SM's capacitor voltage is set at $\frac{V_{DC}}{N}$. In this study, the value of pre-set range is defined as **X** and its relationship to the reference voltage can be expressed as follows:

$$\mathbf{X} = V_{ref} \pm \sigma \tag{6.1}$$

where σ is the range capacitor voltage ripple variation, which is application-specific, and is normally required to be maintained between $\pm 5\%$ to $\pm 10\%$ for HVDC systems [111]. In this paper σ is selected based on the equivalent ripple range of CSA to demonstrate the effectiveness of the PSA in reducing the switching frequency. The core concept for the selection of priority groups is to ensure that groups outside the range have higher priority to change their switching states, while those groups inside the range maintain their existing switching states as far as possible. In other words, the algorithm only selects the most necessary SMs to be involved in the sorting stage to reduce the switching frequency. In addition, the prioritisation also ensures better convergence speed to the desired value for SMs outside the pre-set range.

6.2.1 Prioritisation of SMs

In order to achieve better ripple performance, the priority classification in the proposed for algorithm is presented below. This classification is based on position with respect to the defined ripple range and previous switching states. This grouping process is closely related to the priorities of the actual sorting, and so it is called the 'prioritisation'. The prioritization is way that used only as criterion to divide the SMs into sub-groups and all these sub-groups still need

to be sorted and compared. Conversely, the prioritization in the proposed PSA in this paper assigns each group an order, where groups with high priority always be sorted first. Therefore, the prioritization is not only dividing the groups but also prioritizing them before the sorting stage. Therefore, the proposed PSA has a superior way of prioritization to minimise the involved groups in the sorting process, hence avoiding substantial unnecessary switching events. The prioritisation process is illustrated in Figure 6.1(a) and is explained as follows:

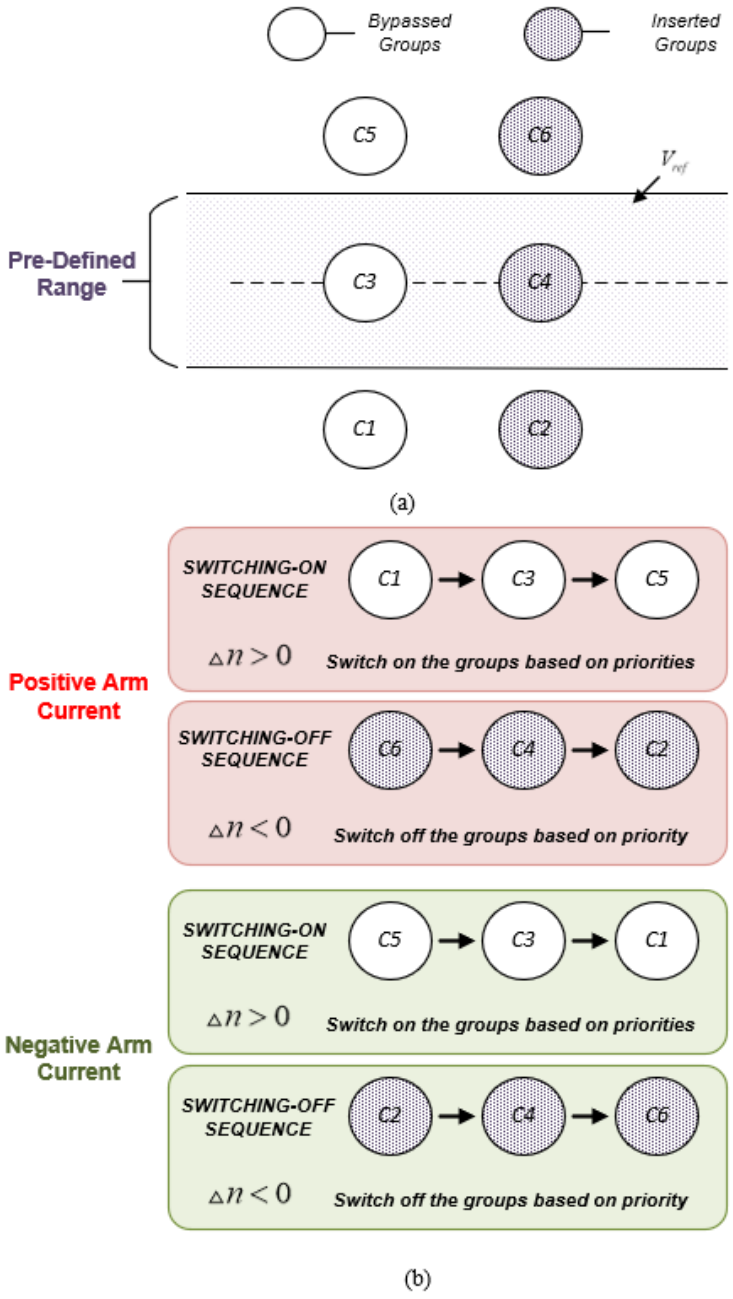


Figure 6.1 Priority-based sorting algorithm. (a) Definition of priorities. (b) Switching sequences of priorities.

- ***C1***: The SM was off in the previous sampling period and is below the pre-defined range.
- ***C2***: The SM was on in the previous sampling period and is below the pre-defined range.
- ***C3***: The SM was off in the previous sampling period and is within the pre-defined range.
- ***C4***: The SM was on in the previous sampling period and is within the pre-defined range.
- ***C5***: The SM was off in the previous sampling period and is above the pre-defined range.
- ***C6***: The SM was on in the previous sampling period and is above the pre-defined range.

According to the details shown in Figure 6.1 (a), the circle represents the SMs in one priority group that either bypassed (white) or inserted (shaded) during the sampling period. After the capacitor voltage measurements and switching states of previous sampling period are sent to the microprocessor, the proposed algorithm assigns priority to the SM. Therefore, the prioritization process requires *N* comparison between two SMs in every sampling period in total. The algorithm then selects the switching sequences of priority groups based on the direction of arm current of previous sampling period. Subsequently, based on the selected switching sequence of the priority groups, switching states of each SM is determined. It is worth noting that, based on the proposed classification method, all SMs are assigned to one of the six groups. Furthermore, a high category number, such as ***C1*** does not refer to a high priority for changing the switching states, but rather the switching sequence is determined by the arm current as will be explained in the following section.

6.2.2 Switching sequences depend on the prioritisation of SMs

In comparison to the required number inserted number of the current and previous sampling period, a change in the required inserted number, Δn, shows the trend of switching events. Due to the nature of modulation techniques, Δn cannot change drastically between two consecutive period, so it is normally fairly small [112]. Therefore, the SM selection process only involves zero or very small number of SMs in every sampling period. For the proposed priority-based sorting algorithm (PSA), the situation of priority selection sequences can be divided into three main conditions, which are also illustrated in Figure 6.1(b):

1. Charging periods:

In the case of positive arm current, which signifies that the current is charging the SMs capacitors.

- If Δn is positive, the PSA searches ***C1*** first. If ***C1*** does not contain any SM, it can be defined as 'empty'. Then ***C3*** is searched followed by ***C5*** until the first non-empty group has been found. Then the SM with the lowest voltage in that group is switched on. The current then charges the selected SM, while the others maintain their previous states.
- If Δn is negative, the PSA searches ***C6*** first, then ***C4*** and ***C2*** until the first non-empty group has been found. Afterwards, SM with the highest voltage in that group is switched on, while the rest of the SMs retain their previous states.

2. Discharging periods:

In contrast, when the arm current is negative, this implies that the arm current is discharging the SM capacitors.

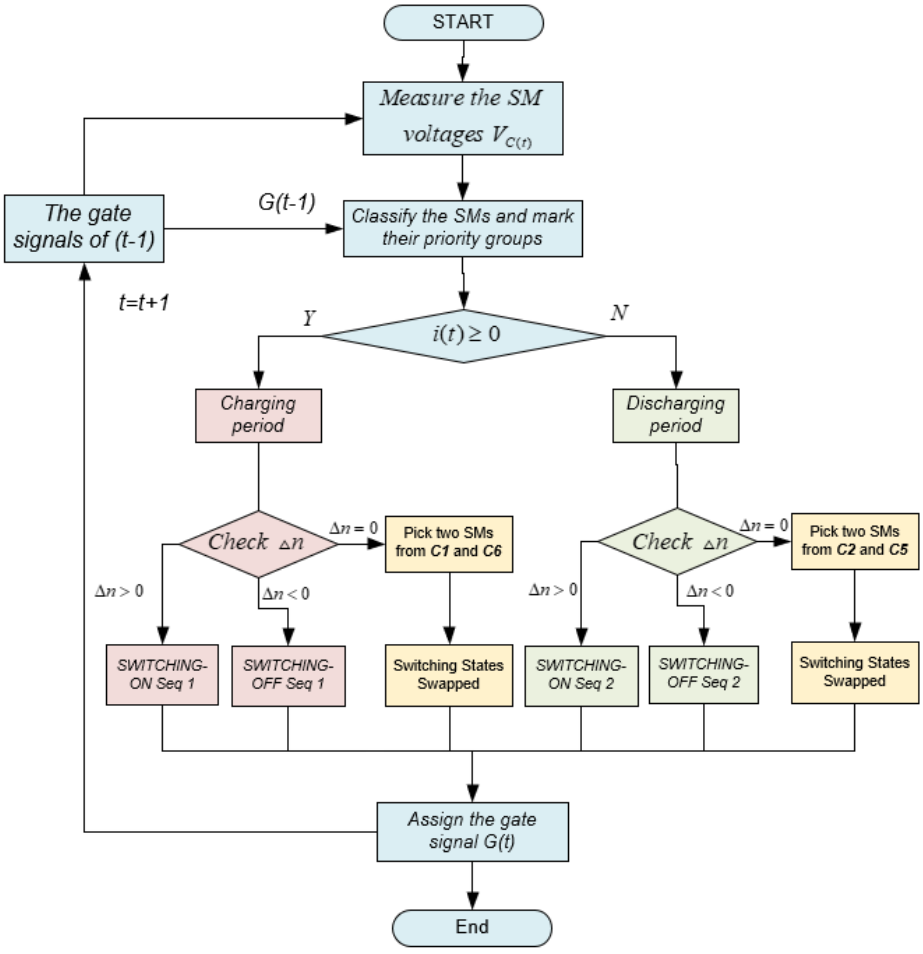
- If Δn is positive, the PSA searches ***C5*** first and then followed by ***C3*** and ***C1*** until the first non-empty group has been found. Unlike the previous condition, this time the SM with the in the group is switched off and the remaining SMs are kept at their previous states.
- If Δn is negative, the PSA searches ***C2*** first, then ***C4*** followed by ***C6***. Once the first non-empty group is identified then the SM with lowest voltage in that group is switched off and the other SMs maintain their previous states.

3. Other conditions:

When $\Delta n = 0$, which means there is no changes in the output voltage level of the converter, but the current still flows through the inserted SMs, causing charging or discharging of the capacitors. However, for PSA, unless the aim is to limit the conduction losses of the switches, otherwise, SMs will not change their states. Alternatively, one SM from the highest priority group and another corresponding one from the lowest priority group are selected, then

their switching states are swapped according to the following scenarios:

- If the current is positive, the PSA only searches ***C1*** and ***C6***, and if they are found to be empty, then no SMs are required to change their states, so all SMs maintain their previous states. Conversely, if they are not empty, the SM with the lowest value from ***C1*** and the SM with the highest value from ***C6*** are selected and their states are swapped.
- If the current is negative, the PSA only searches ***C2*** and ***C5***. As in the previous condition, if they are all empty, all the SMs maintain their previous states. Conversely, if they are not, the SM with the lowest value from ***C2*** and the SM with the highest value from ***C5*** are selected and their states are swapped.



- Figure 6.2 Flowchart of PSA.

Overall, the PSA helps to narrow down the scale of the search during the sorting process.

6.3 Analysis of the PSA.

This study proposes a novel voltage balancing sorting algorithm desired to reduce the high switching frequency caused by the conventional sorting algorithm without sacrificing the output waveform quality of the MMC. Furthermore, computational complexity is reduced when compared with the conventional sorting algorithm. It is worth noting that the main purpose of voltage balancing method is not to force all SMs to have identical voltage values in every sampling period, instead, it maintains the voltage ripple of SMs to within an acceptable range. Within that range, the SM voltages will have the flexibility to vary, which is highly likely to maintain their switching states. The procedure of PSA is summarised in the flowchart in Figure 6.2. The main advantage of the proposed method is to help narrow down the search to only one or two groups in every sampling period. Besides this, unlike in traditional grouping methods, the groups themselves are no longer required to be sorted before dealing with the SMs inside groups. Instead, a fixed sequence arrangement is implemented. Therefore, the sorting process involves fewer sorting actions which leads to the avoidance of unnecessary switching events.

An MMC model with 4-SM per arm during the charging period is taken as an example in Figure 6.3. If the required change number $\Delta n = 1$, only the SM with the highest priority needs to change its state from OFF to ON. The priority sequence here is Charging Sequence 1. The sorting algorithm selects $\Delta n = 1$ SM and the SM in the lowest priority group ***C1*** to switch on. Only one comparison is made in this case. When the group with ***C1*** is empty, the SM inside the second priority group ***C3*** is searched until all the required number Δn of SMs to be changed have been assigned. The results are the same as with the CSA which the lowest SM is identified so as to be switched on. But CSA conducted $4 \times \frac{4-1}{2} = 6$ comparisons while the proposed PSA only conducted one comparison.

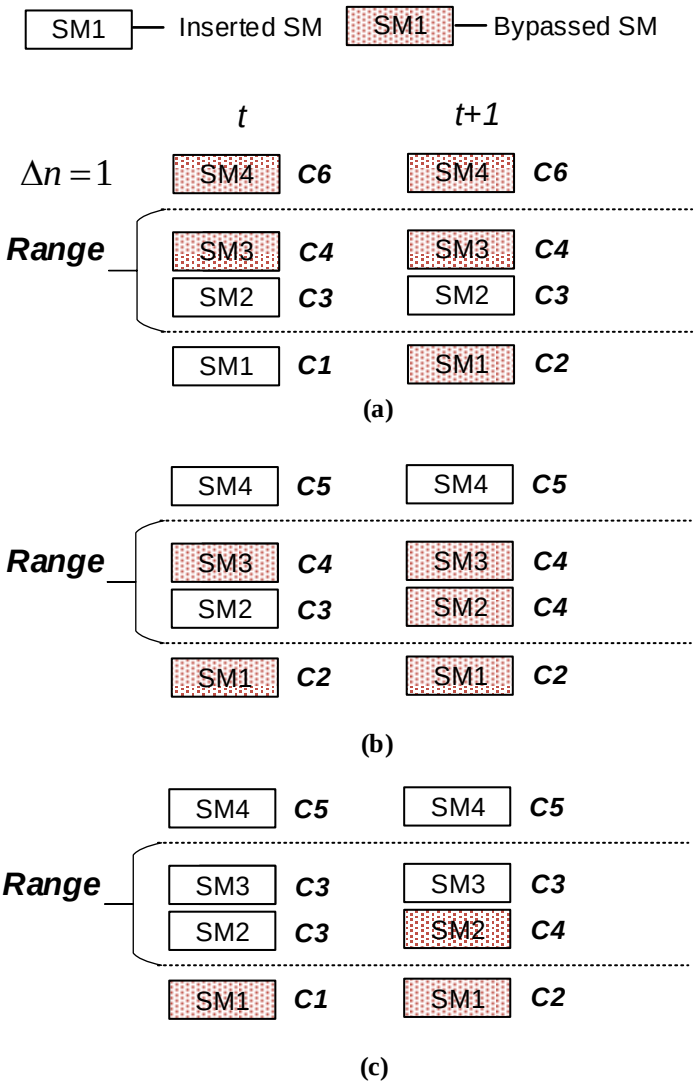


Figure 6.3 Switching events illustration for two classic conditions for proposed sorting optimisation. (a) First priority group has SMs. (b) The second priority group has SMs. (c) The second priority group has multiple SMs.

It is worth noting that, for the proposed PSA with a total of six priority groups, the sorting action is only taken inside one priority group in every sampling period. Therefore, the switching of PSA is simpler compared with the CSA, and the estimated comparison times thus becomes:

$$T_3 = N' \cdot (N' - 1)/2 \tag{6.1}$$

where N' is the SM number that needs to be switched on in total in one sampling period. Compared with N of all the SMs in one arm, N' is normally the SM number inside one group, so:

$$N' \ll N \tag{6.2}$$

Therefore, the relationship of comparison times between CSA and PSA can be determined as:

$$T_3 \ll T_0 \tag{6.3}$$

This proves that the sorting time of the proposed sorting optimisation technique is lower than that of the CSA. Meanwhile, the CTs for the CSA and PSA with increased numbers of SMs are depicted in Figure 6.4. When the number of SMs approaches 1000, which is close to the conditions of real MMC projects, the PSA only sorts one group out of six, and so the CT reduction becomes significant.

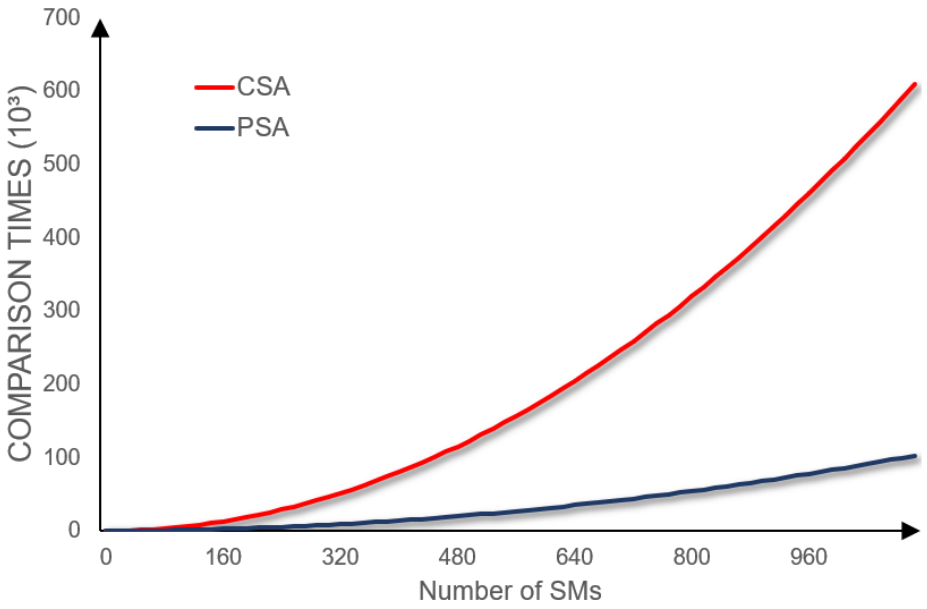


Figure 6.4 Comparison of computational complexity between CSA and PSA.

Therefore, the action of comparison between two adjacent SMs is evidently reduced every sampling period. Compared with the CSA and improved sorting algorithms as discussed in the previous chapters, the key points of the proposed sorting optimisation technique are as follows:

1. More efficient in terms of switching frequency reduction than other previously mentioned methods. The usage of sorting algorithm is further optimised and only the SMs in the highest priority group will change its states.

2. Less time and computational complexity. The time complexity is $O(N'^2)$ and from Equation 6.3, the comparison time is reduced significantly, giving it substantially lower computational complexity than CSA

3. The prioritisation step is based on the pre-set range, where the exact value of the range is variable. Therefore, the designer has the flexibility to determine the behaviour of the proposed technique to ensure its compatibility with different voltage ripple requirements.

6.4 Application of the PSA with High Number of SMs

Since the main concept of the proposed PSA is demonstrated by assembling the SMs into six priority groups, the selection and the change of SMs and their switching states only occur within the selected groups. Therefore, it is not necessary for SMs in other groups to be involved in the sorting process. However, for real projects with hundreds or thousands of SMs connected in series, six groups are clearly insufficient to effectively reduce the unnecessary switching events. Therefore, a further classification is essential.

Fundamentally, the SMs within the pre-set range are less urgent to change their states, voltages above the upper boundary of the pre-set range and below the lower boundary of the range can be further divided into several identical ranges. Each range is according to the accuracy requirement. Hence the ***C1***, ***C2***, ***C5*** and ***C6*** are divided evenly into sub-groups, and named from low to high $U_1, U_2, U_3, U_4 \cdots U_U$ respectively. Then, following the general rules of PSA, the selection of the sub-groups is based on its priorities.

During the PSA scheme, a step is added after establishing the prioritisation, then ***C1***,***C2***,***C5*** and ***C6*** are re-prioritized to $\boldsymbol{C1_U}, \boldsymbol{C2_U}, \boldsymbol{C4_U}$ and $\boldsymbol{C6_U}$ according to which specific sub-group they belong to:

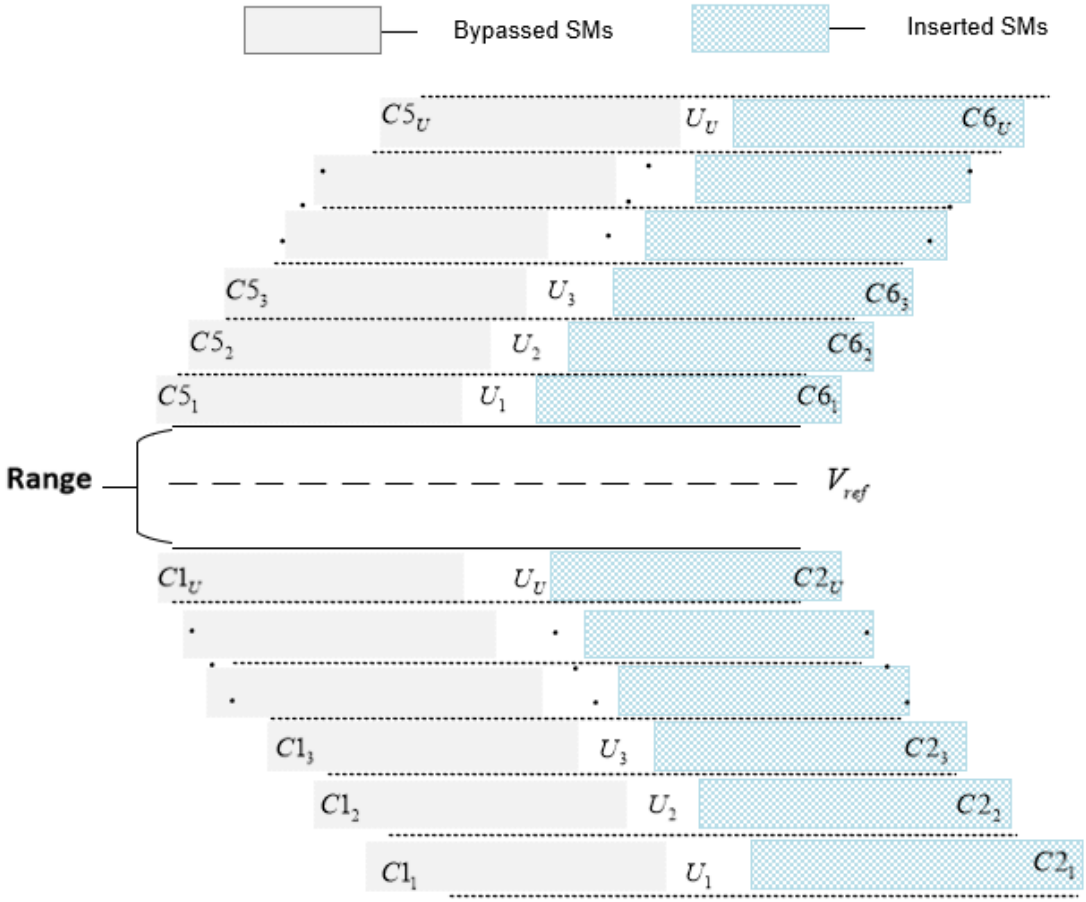


Figure 6.5 Further classification of Priority for MMC with high number of SMs.

1. Classify every SMs into the origin 6 priority groups which is same as PSA with fewer SMs.

2. The SMs in ***C1***, ***C2***, ***C4*** and ***C6*** priority groups are divided into sub-groups $U_1, U_2, U_3, U_4 \cdots U_U$ in order to achieve higher control accuracy.

3. For the condition of Charging Sequence 1, the algorithm begins from $U1_1$, $U1_2$, $U1_3$, $U1_4 \cdots U1_U$, and the numbers of SM in every sub-groups $u1_1, u1_2, u1_3, u1_4 \cdots u1_U$ are recorded.

4. It is assumed that the required number is Δn. If $\Delta n \leq u1_1$, the Δn SMs of $U1_1$ are switched on. If $\Delta n \geq u1_1$, $\Delta n = \Delta n - u1_1$ then for $U1_2$ to $U1_U$ are searched for U SM sub-groups until $\Delta n \leq u1_U$.

5. If $\Delta n \geq \sum(u1_1 + u1_2 + u1_3 + u1_4 + \cdots + u1_U)$, ***C3*** is divided and searched. If Δn is still more than the SMs in ***C3***, step 4 is repeated for ***C5*** until $\Delta n \leq u5_U$. The gate signals are maintained for the rest of the SMs.

6. Steps 3-5 are applied in the same way for the Charging Sequence 2, Discharging Sequence 1 and 2.

It should be highlighted that if there is only one SM in a sub-group, then that SM represents the whole group and its switching states is determined without extra comparison. If there are more SMs in a sub-group, and the ripple requirement is not extremely strict, then the switched-on SMs can be selected randomly; conversely, if the ripple requirement is strict, the algorithm will bubble sort all the SMs within that sub-group. Essentially, the optimisation of PSA decreases the duration of the sorting process as far as possible, thereby minimising unnecessary switching. Meanwhile, the capacitor voltages of SMs vary within the pre-set range. The effectiveness of this technique and whether its use has a slightly negative impact on system performance, which needs to be further investigated.

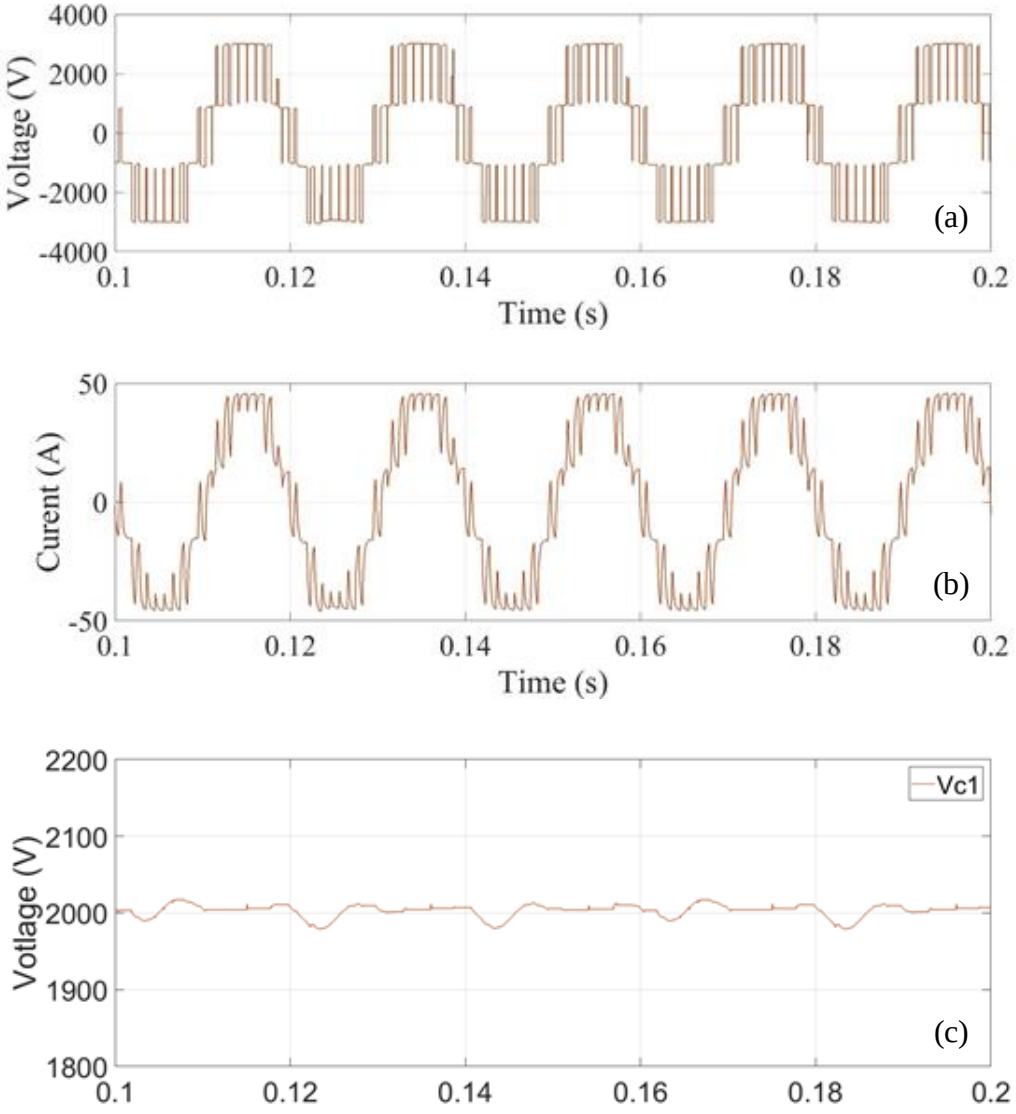
6.5 Simulation Results

To demonstrate the feasibility of proposed PSA, a single-phase (one-leg) MMC model is developed using MATLAB/SIMULATION software package, where intensive simulations studies have been conducted. The model is built using 31 SMs per arm and the main parameters are listed in Table 4-II.

6.5.1 Steady-state operation of PSA

The steady-state results of the 4-level simulation are listed in Figure 6.6, where the pre-defined range **X** is set to 1% for less capacitor ripple. From Figure 6.6 (a) and (b), the waveform of output load voltage and current are resembling the other proposed techniques. Because the variations are not exceeding the limit during the steady-state time. While for the capacitor voltage in Figure 6.6 (c), the waveform is not at its steady-state before t=0.13s which means the convergence speed of PSA is slower than other proposed techniques. It can be seen from Figure

6.6 (d) and (e), the waveform is no longer sinusoidal, and the negative peak value of circulating current is slightly higher than the others. This is because the capacitor voltage is varying within the pre-defined range **X**, so the voltage difference between the arms varies as well, which subsequently increasing the unbalanced voltage between two arms. However, based on the tests of THD, the impact of this peak circulating current to the system is can be disregarded.



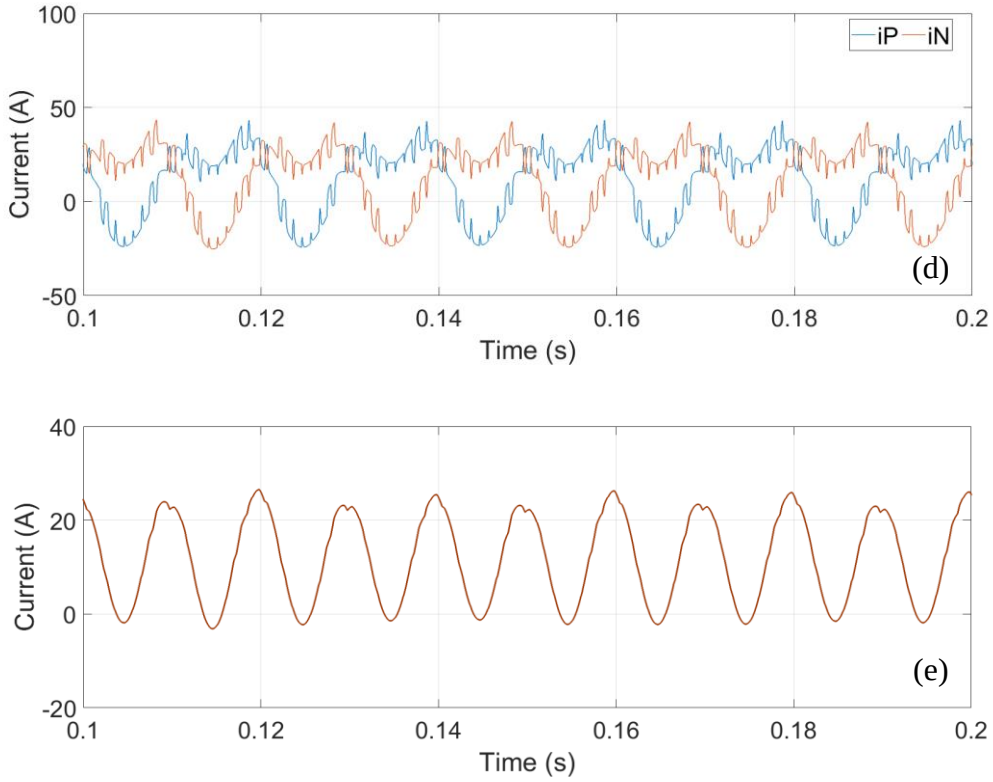


Figure 6.6 Simulation results of PSA. (a) Output load voltage.(b) Output load current.(c) Voltage across C1.(d) Upper arm and lower arm current. (e) Circulating current.

The most attractive feature of PSA is the considerable reduction in switching frequency. This is demonstrated in Figure 6.7 by comparing the switching states of upper arm SMs within the same period to CSA. It is obvious the switching events has been reduced significantly. According to Figure 6.8, where, as an example, the average switching events for the upper arm is 63 and the average switching frequency is 320 Hz, which is an substantially over 90% reduction compared to 3350 Hz of CSA. In comparison with other proposed techniques, it still the best for switching frequency reduction.

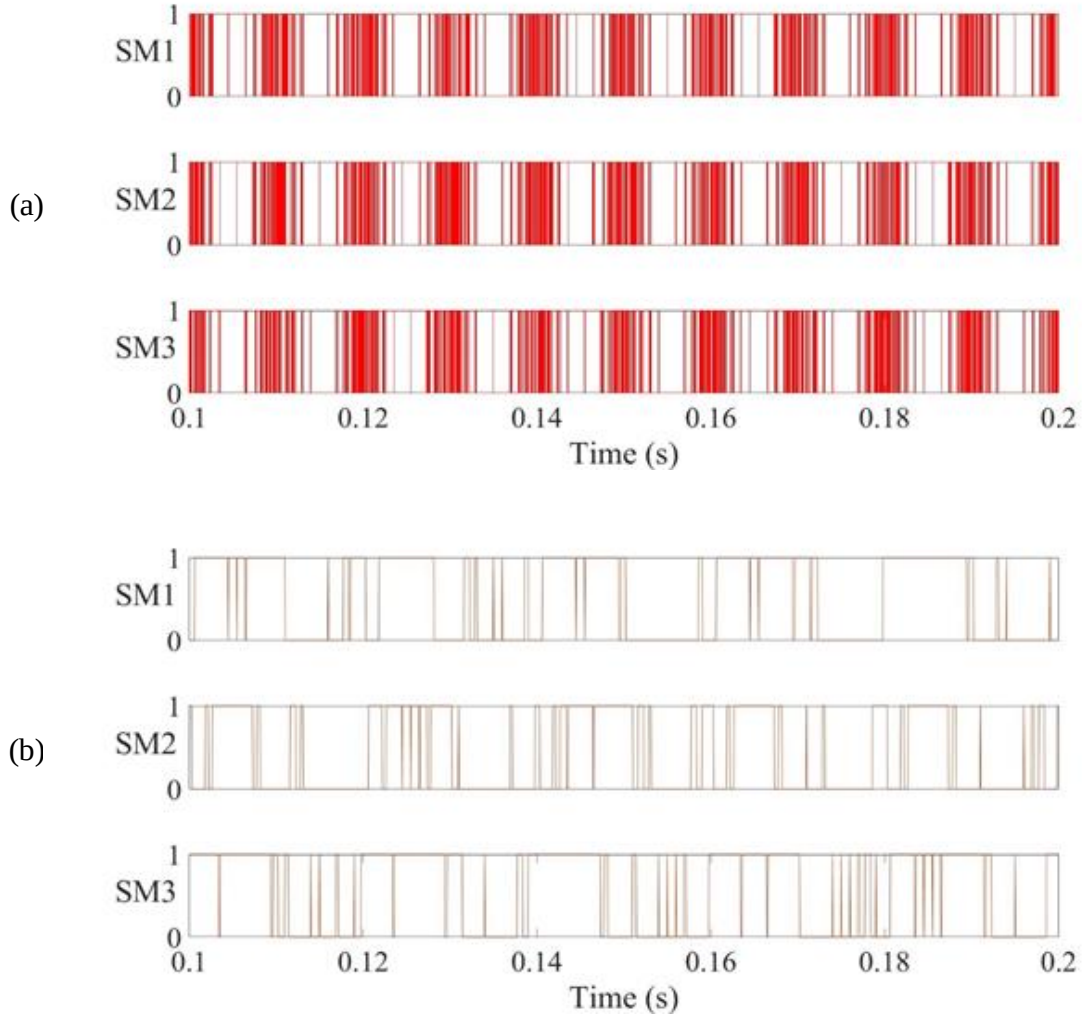
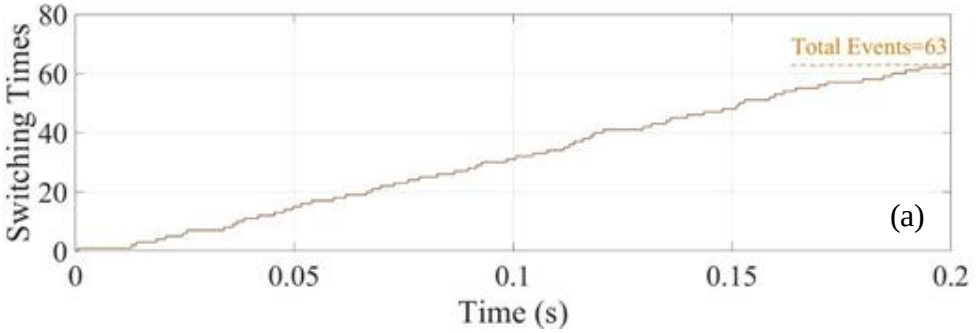


Figure 6.7 Simulation results of gate signal for upper arm SMs with different voltage balancing algorithms. (a) CSA. (b) Heap Sorting algorithm.



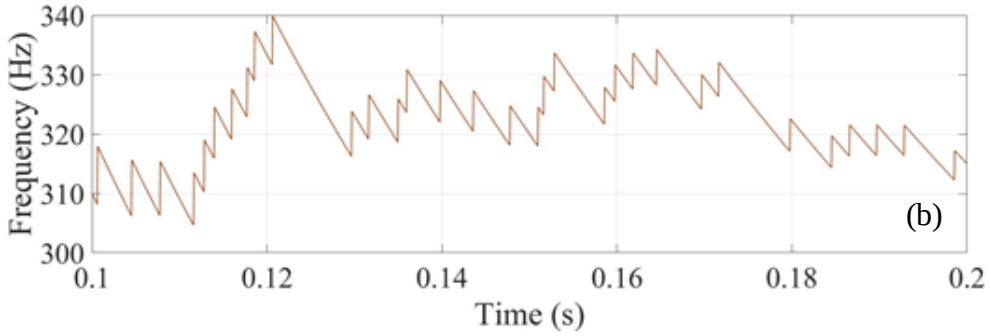


Figure 6.8 Simulation results of gate signal for upper arm SMs with different voltage balancing algorithms. (a) CSA. (b) Heap Sorting algorithm.

Based on the result of CSA, range **X** is set at 1%, so the capacitor ripple fluctuated mainly between 1980V to 2200V. From Figure 6.9 (b), the capacitor voltage of all SMs are maintained varying within the range appropriately. The biggest difference between the CSA and PSA is the capacitor ripple, the capacitor voltage is no longer needed to be identical every sampling period.

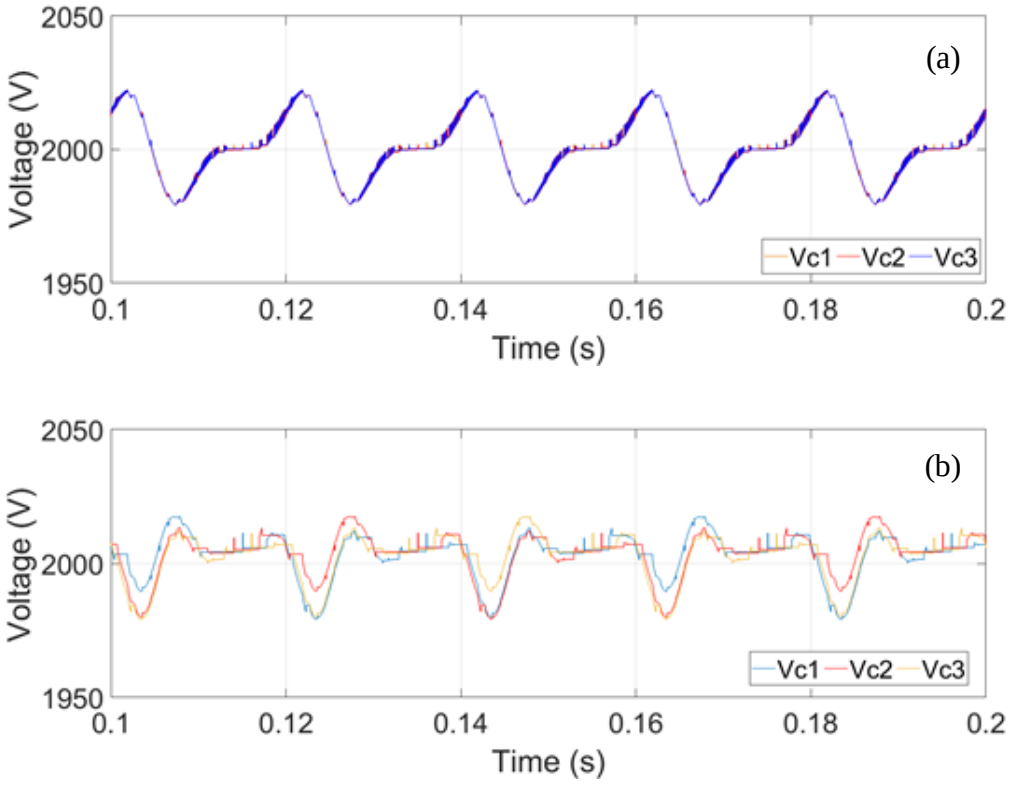


Figure 6.9 Ripple performance comparison of upper arm. (a) CSA. (b)PSA.

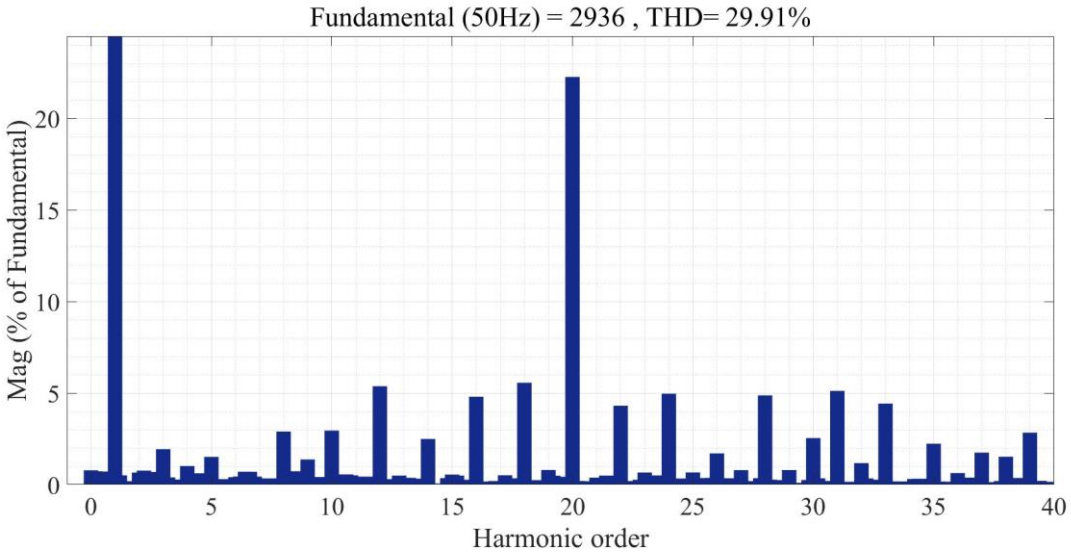


Figure 6.10 Output voltage harmonic performance of PSA.

The harmonic distribution of PSA during the steady-state is shown in Figure 6.10, where the THD of PSA is 1% lower than the HSA in Chapter 5. Compared to ISA in Chapter 4, the THD are very close and both higher than CSA and Heap sorting algorithm. Therefore, the output performance remains the same after reducing the switching frequency and computational complexity.

Table 6-I Comparison between different capacitor voltage balancing schemes under steady-states of the 4-level MMC model. compare the different methods presented in Chapter 4-6 and summarizes their performances under steady-states of the 4-level MMC model.

Table 6-I Comparison between different capacitor voltage balancing schemes under steady-states of the 4-level MMC model.

Voltage Balancing Technique	**Voltage THD (%)**	**Switching Frequency (Hz)**	**Capacitor Voltage Ripple Level**	**Sorting Time**	**Time Complexity**
CSA	29.15	3350	1%	$N(N-1)/2$	$O(N^2)$
ISA	29.56	521	1%	$D_p \cdot N(N-1)/2$	$O(N^2)$
HSA	30.83	435	1%	$\leq D_p \cdot (4N + (N-2)(N-4))/4$	$O(N \log_2 N)$

PSA	29.91	315	Tuneable from 1% to 5%	$N' \cdot (N' - 1)/2$	$O(N'^2)$

From the table, all the proposed scheme reduces the switching frequency effectively, but the PSA demonstrated the best performance. All of them exhibited ripples of less than 1%, which is the ideal scenario. The THD variation are similar with less than 1.5% variation. Sorting time represents the computational complexity, and time complexity has a strong link with algorithm speed. The reduction of computational complexity has been proven mathematically, but in this area, HSA was most effective.

6.5.2 Dynamic response when altering the pre-set range

The dynamic performance has been tested in this section, where the pre-defined range **X** is dropped from 3% to 1%, which in this case, decreases from 60 V deviation to 620 V deviation at the time=1s. From Figure 6.11, the variation of capacitor ripple voltage of SM1, SM2 and SM3 are successfully decreased to 1%, and the transient time is less than 0.02s. The gate signal and average switching frequency shown in Figure 6.12 prove the flexibility of the PSA, the average switching frequency decreases from 335 Hz to 325 Hz. Hence, it can be concluded that with PSA, the patterns of switching events can be controlled.

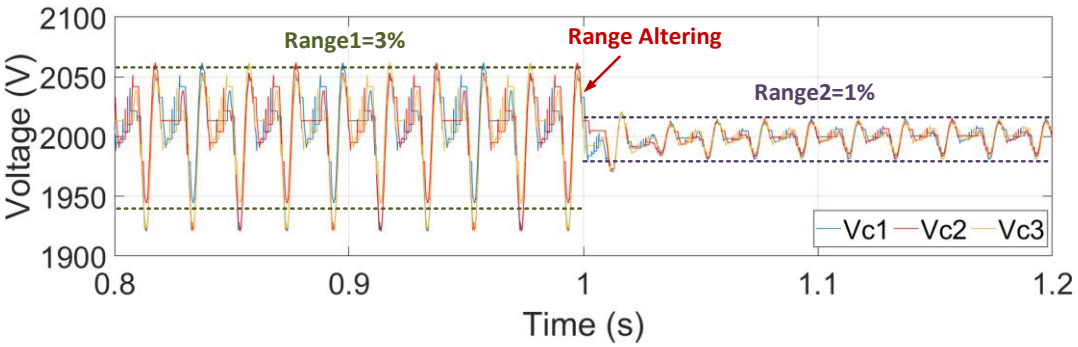
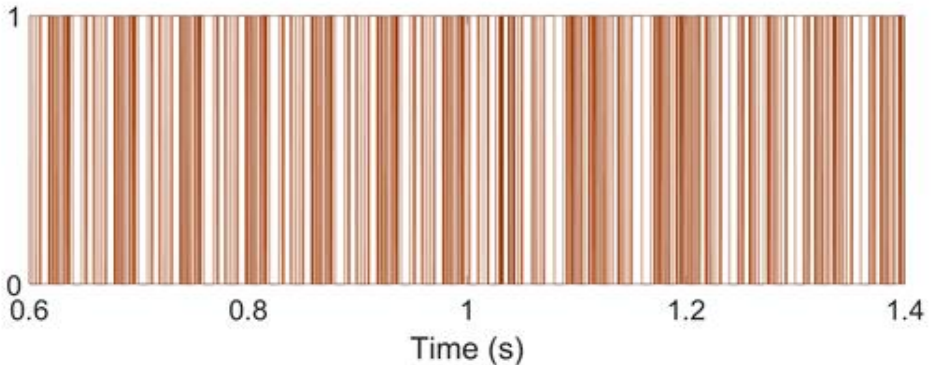


Figure 6.11 Dynamic response of capacitor voltage with PSA, the range change at t=1s.

(a)



(b)

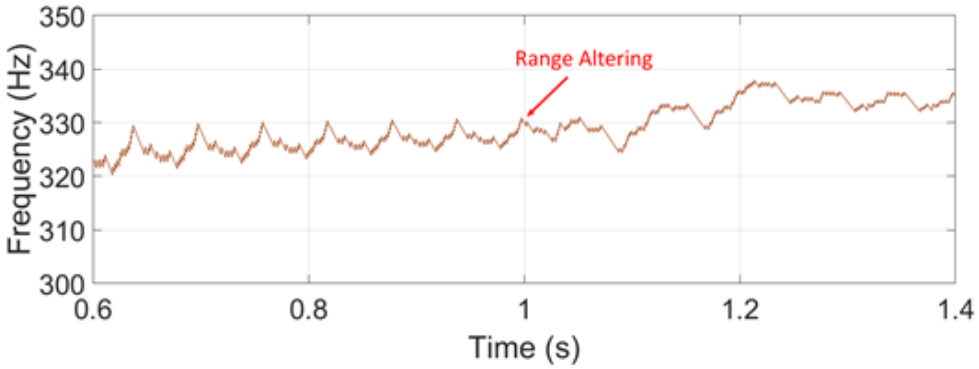


Figure 6.12 The gate signal (a) and the average switching frequency (b) after range change at t=1s.

From the results of altering the range, it is worth noting that the function of **X** is not the same as the tolerance band (TB). The TB triggers immediately when the voltage value of an SM hits or exceeds the limit, whilst **X** is only one condition for the prioritisation. Furthermore, since the PSA has high circulating current within the arms, the tuning of one arm will have an impact on the other one. Therefore, the value **X** only helps to control the ripple fluctuation but how to further limit the ripple accurately need extra investigation.

6.5.3 Performance of PSA during a step change of DC side

In order to verify the dynamic response of the proposed PSA, a step change in the DC side is applied at t=0.4. The DC source loses 50% of its original value, drops from 6000V to 3000V.

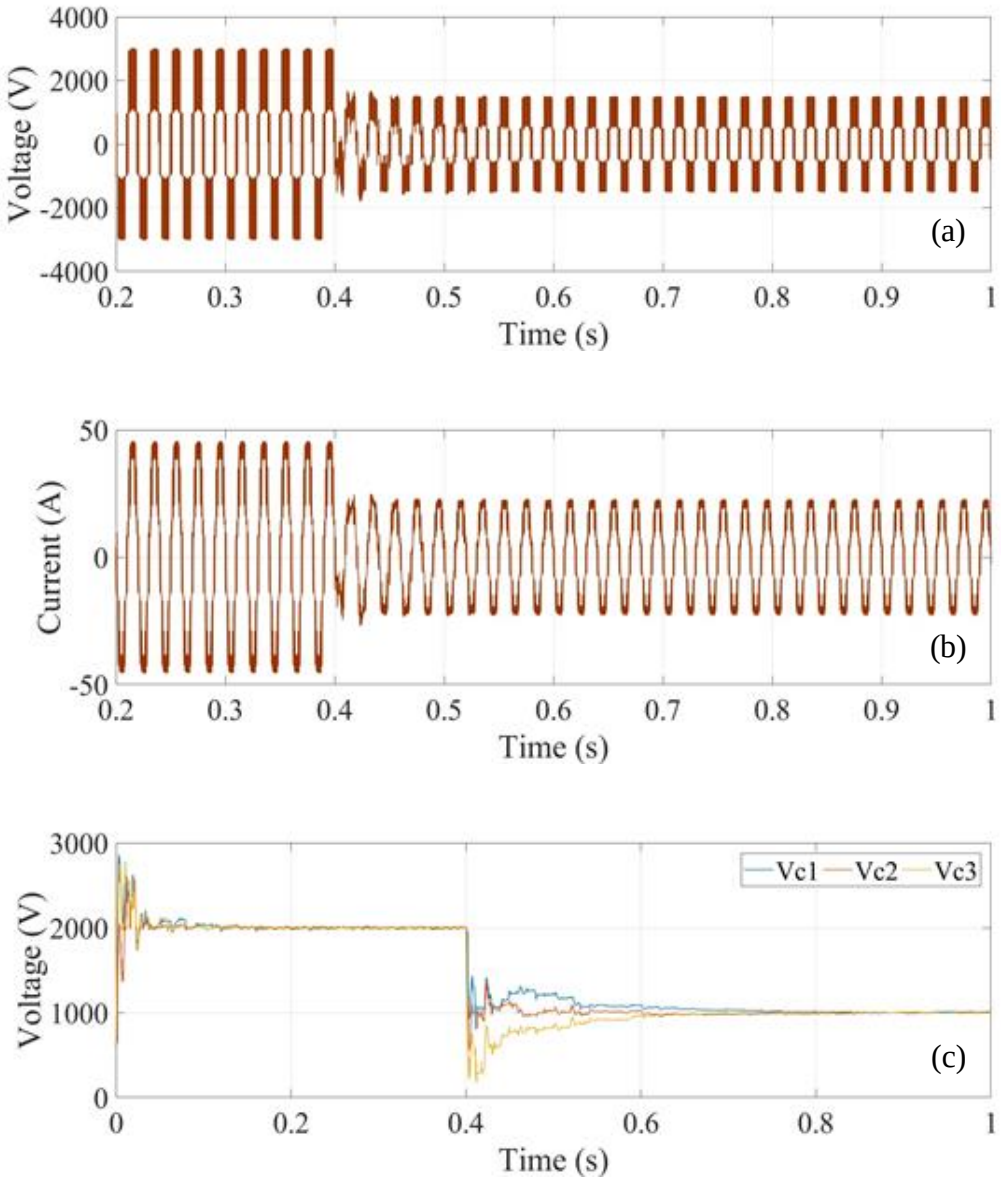


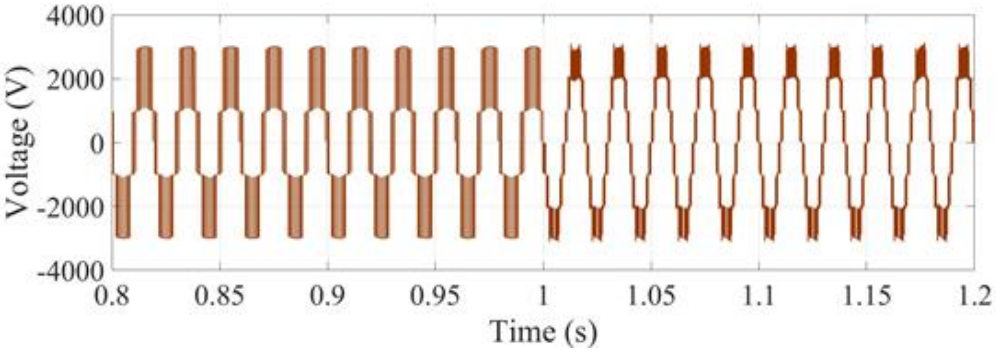
Figure 6.13 Simulation results for DC step change under HSA scheme. (a) Output load voltage. (b) Output load Current. (c) Capacitor voltage of upper arm.

The results of the step change for PSA are depicted in Figure 6.13, which has slightly different from CSA, ISA and HSA have been evaluated in the previous chapters. The transient time raised from less than 0.1s to 0.3s, which can be seen from Figure 6.13 (c). The capacitor voltage of PSA gets re-balanced again at =1000V for more than 0.3s. Therefore, the performance of PSA has slower transient speed, but the overall output performance does not get sacrificed.

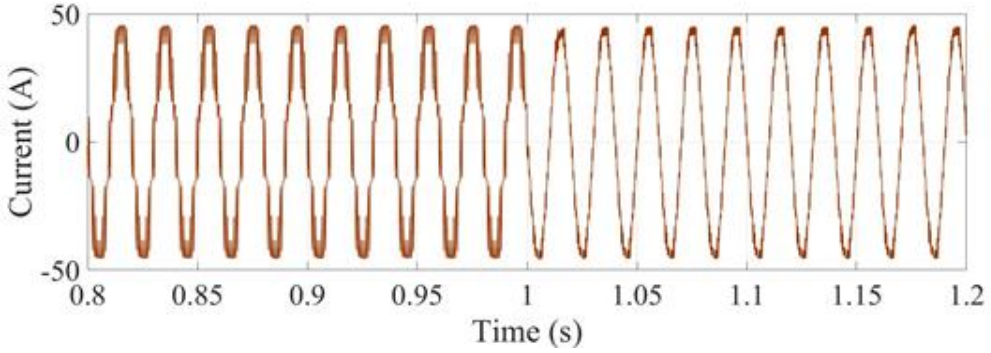
6.5.4 *Implementation of Interleaving for PSA*

Figure 6.14 shows the response of PSA when the interleaving modulation scheme is applied for the upper arm at t=1s. The expectation of output level is altered from 4-level to 7-level. From Figure 6.14 (a), the output level changed very fast and had a positive impact on the output load current on Figure 6.14 (b). Figure 6.14 (c) and (d) reflected the capacitor voltage ripples, the fluctuation range was raised from 1% to 5% because the circulating current was increased from 50A to 200A. This drawback of the interleaving modulation scheme resulted in increasing the distortion of the system. In comparison with the other proposed techniques, the capacitor ripple of PSA is slightly higher but the THD of the output are similar. Overall, the interleaving modulation scheme is implementable for PSA, how to reduce the ripple and circulating current requires more efforts in the future.

(a)



(b)



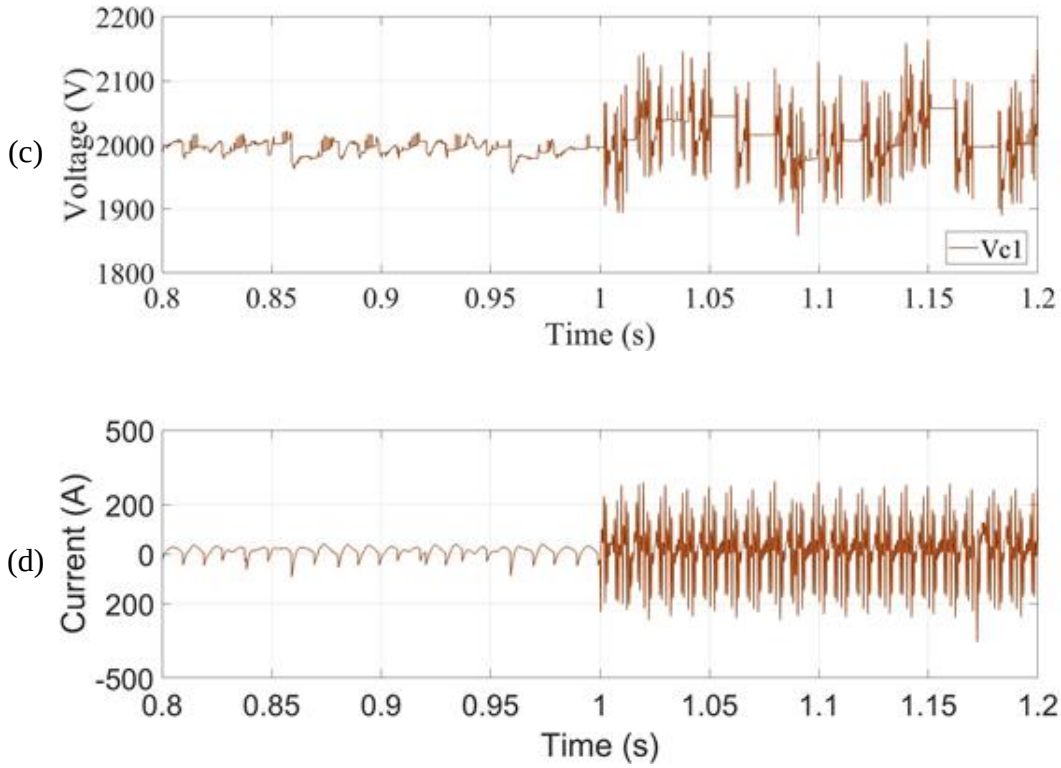


Figure 6.14 Simulation results for applying interleaving modulation scheme 4-level MMC with PSA. (a) Output load voltage. (b) Output load Current. (c) Capacitor ripple voltage of SM1. (d) Circulating current.

6.5.5 Performance of HSA and PSA for high number of SMs

In order to verify the effectiveness of proposed HSA and PSA, further investigation was taken by increasing the number of SMs and voltage level of output. The SMs increased from 3 to 21 and the modulation scheme is N+1. The parameters are listed in Table 5-II from Chapter 5. Figure 6.15 shows the performance of HSA, which implies that generated the 21-level output level properly. In comparison with the CSA and heap sorting, there is no significant difference between them. Therefore, the HSA can operate with high number SMs of MMC. Meanwhile, the capacitor voltage fluctuates with 1% variation to the reference value 21000/21=1000V. The SM voltage curves are no longer identical to each other which helps to reduce the need to CSA.

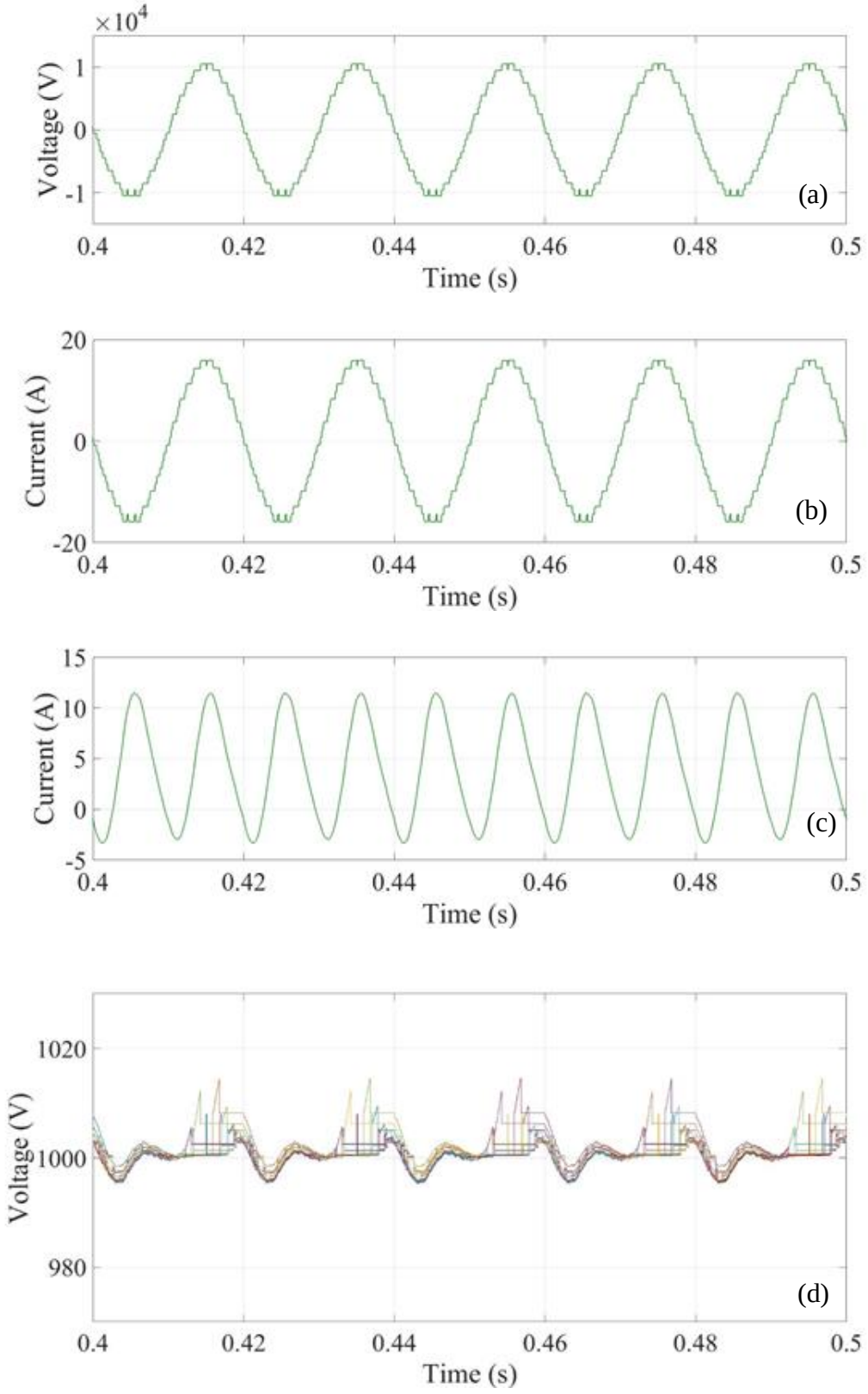
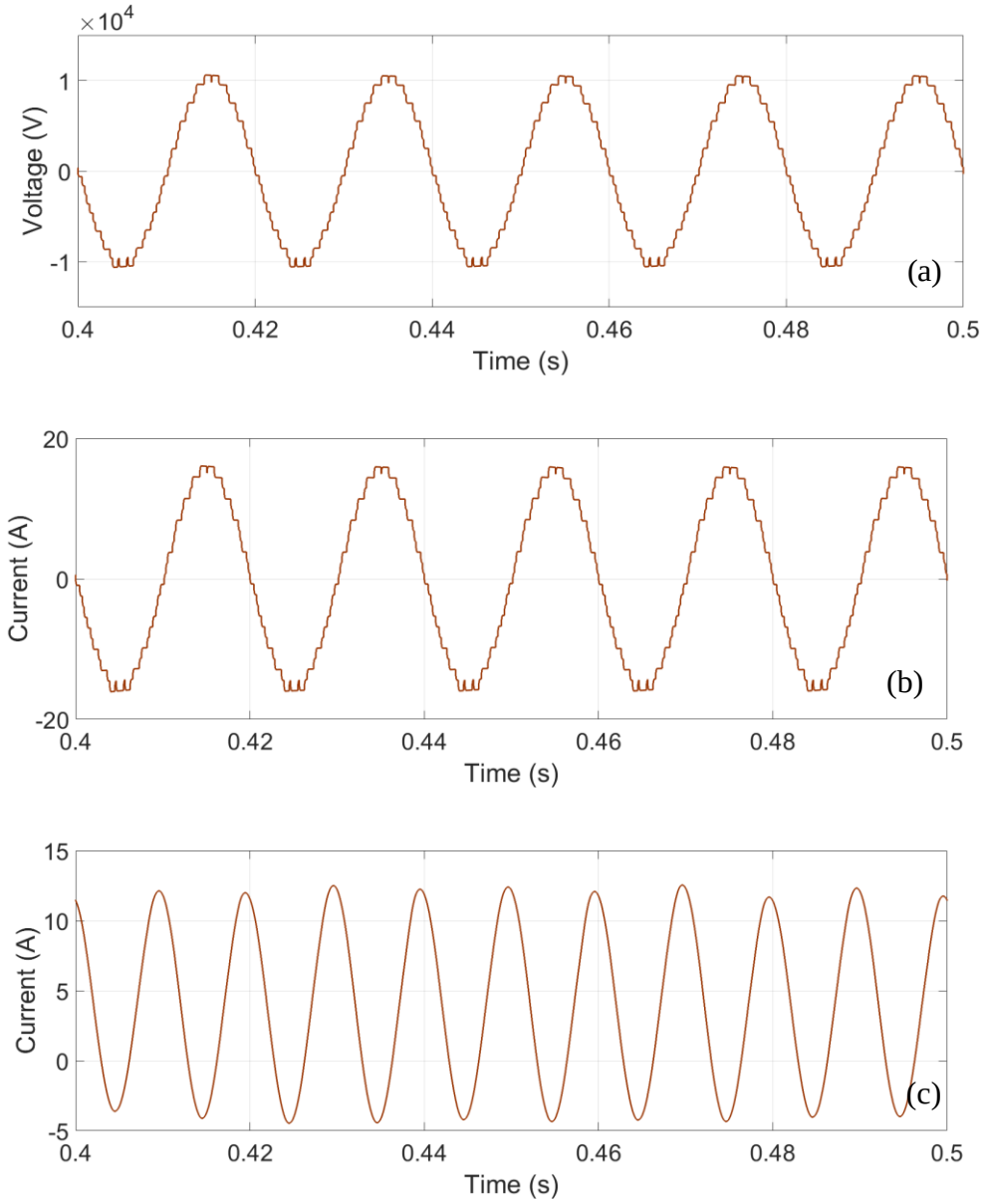


Figure 6.15 The performance of HSA with 21 SMs per arm. (a) Output voltage. (b) Output current. (c) Circulating current. (d) Capacitor voltage ripples of upper arm.

It can be seen from Figure 6.16, the PSA is able to generate a 22-level stair-cased waveform with the 10500V peak output voltage. Figure 6.16 (c) shows the circulating current has increased slightly due to the unbalanced voltage between upper and lower arm. Figure 6.16 (d) illustrate the capacitor ripple voltages of upper arm SMs, the pre-set range **X** is set to 1%. From the graph, most of the capacitor voltages are inside **X** (980V to 1020V), while few them are outside. Those SMs are outside range have higher priority for the next couple of sampling periods. Regarding the CSA and heap sorting, the capacitor ripple is slightly higher with PSA. However, most of the SMs are still inside the acceptable range so the negative impact to the system is ignorable. The SMs inside the range are less likely to change their switching states.



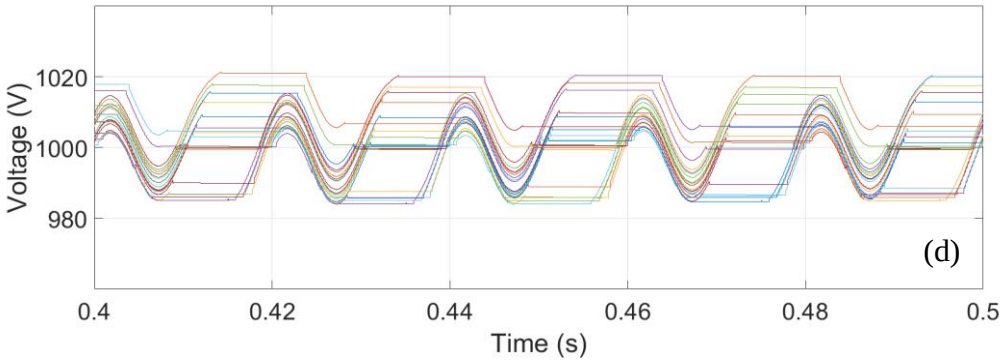


Figure 6.16 The performance of PSA with 21 SMs per arm. (a) Output voltage. (b) Output current. (c) Circulating current. (d) Capacitor voltage ripples of upper arm.

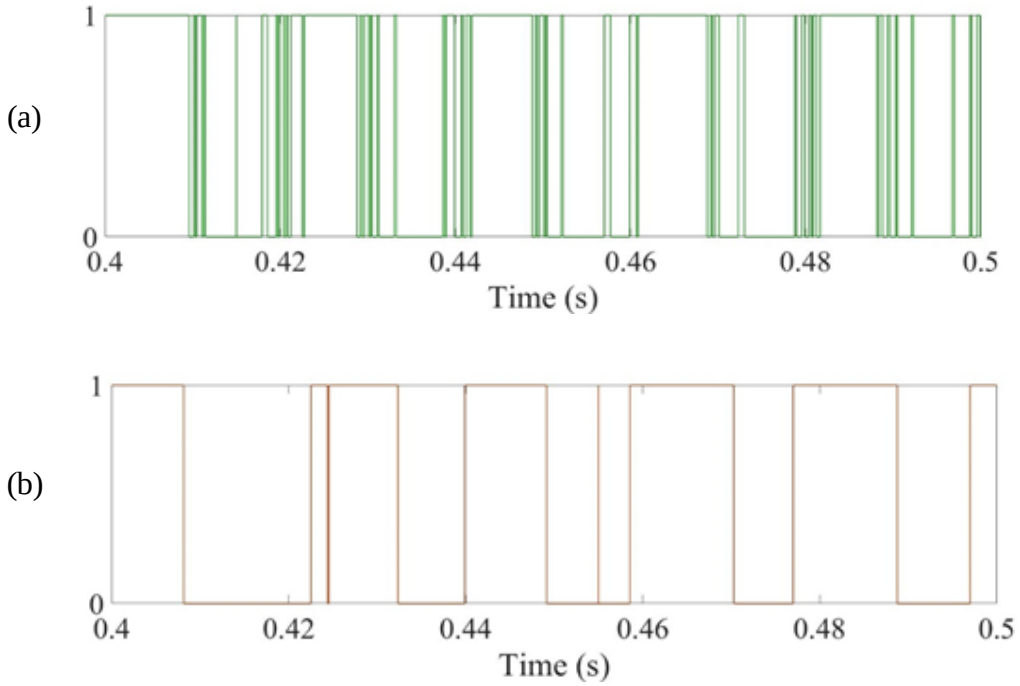


Figure 6.17 Simulation results of gate signal for SM1 with different voltage balancing algorithms for high number SMs. (a) HSA. (b) PSA.

From Figure 6.17, the average switching frequency of HSA and PSA are 440 Hz and 60 Hz, respectively. Compared to the 4-level MMC model, the frequencies of HSA and PSA are at the same level.

Figure 6.18 exhibits the FFT analysis of HSA and PSA, respectively, during the steady-state for 22-level MMC model. From the figure, the THD of PSA and HSA are almost same except the magnitude of fundamental voltage. The THD for both has reduced 20% compared to the performance of 4-level model. In comparison with the harmonic of CSA and heap sorting

algorithm with the same 22-level MMC model, the THD only increased 0.05%, which means the proposed improved sorting algorithm still works for high level SMs.

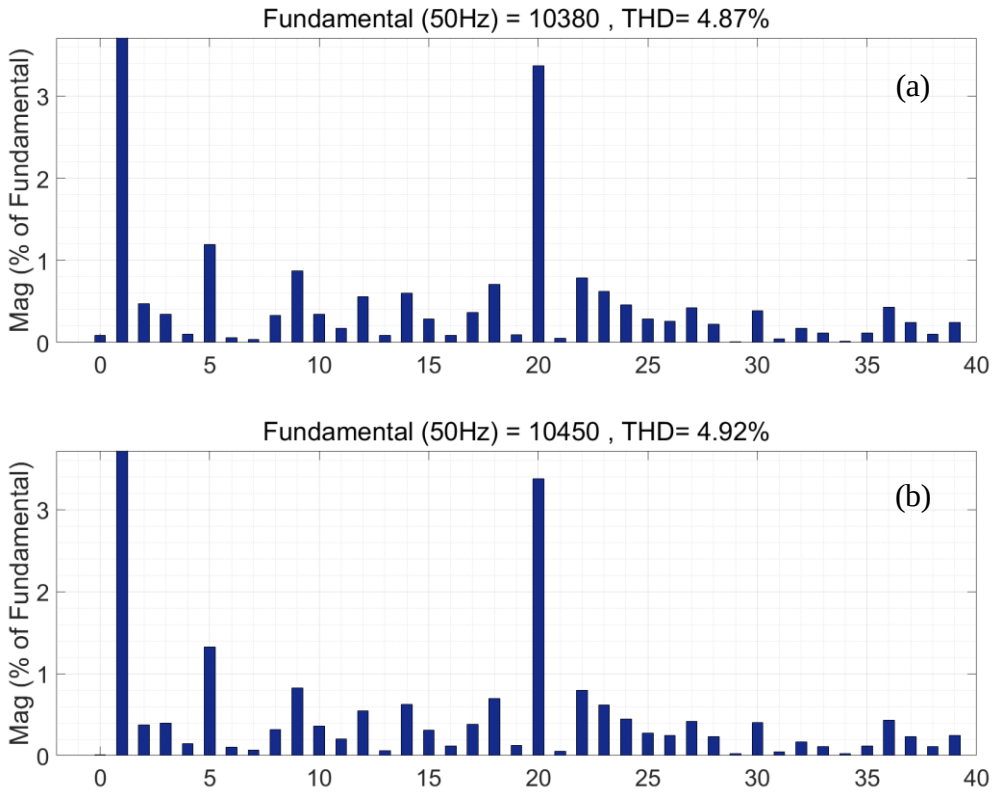


Figure 6.18 Output voltage harmonic performance of HSA and PSA with a 22-level MMC model. (a) HSA. (b) PSA.

6.5.6 *Evaluation of SM losses of all proposed techniques*

The evaluation of the mean loss of IGBT and diodes has been accomplished for one SM for all proposed schemes based on the SimScape package of MATLAB/Simulation. S_1 and $S_2$are the upper and lower IGBTs of the SM, and D_1 and D_2 are their diodes, as shown in Figure 6.19. P_{consS} is the conduction losses of IGBT and P_{swS} is the switching losses. P_{swS} is further divided into turn-on losses P_{onS} and turn-off losses P_{offS} and the relationship between the losses of IGBTs can be expressed as:

$$P_{totalS} = P_{consS} + P_{swS} = P_{consS} + P_{onS} + P_{offS} \tag{6.4}$$

where P_{totalS} is the total losses of the IGBTs. The parameters of the IGBT are obtained from the datasheet of the ABB 5SNG0250P330300 module. The rated voltage is 3000V and the rated current is 250A which is suitable for the simulation with a 12 kW-rated-power system. The

parameters of the testing model are based on Table 4-II. The comparison was carried out at steady-state with the 4-level model built for testing the performance of steady-state in the previous section.

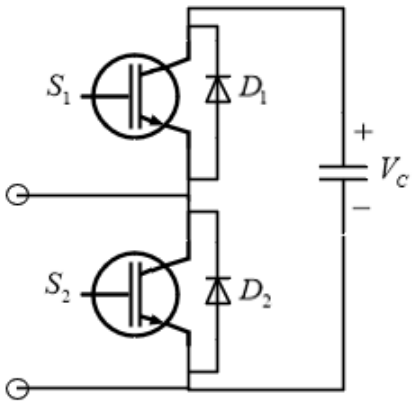


Figure 6.19 SM structure of the IGBT module for the loss evaluation.

The loss evaluation approach used is based on a method introduced elsewhere [39]. To simplify the calculation, the junction temperature is set to 125℃, and the calculated current factor k is set to 1. The block voltage V_{CE} of the IGBT is determined according to the arm current flowing through the IGBT at a certain temperature. The value of V_{CE} can be found in the look-up table from the datasheet. T is denoted as the fundamental period. The system is at steady-state at the point of t_s, and so the conduction losses of the IGBT P_{conS} is given by:

$$P_{conS} = \frac{1}{T}\int_{t_s}^{t_s+T} I_C(\tau)V_{CE}(\tau)d\tau \tag{6.5}$$

As with the calculation of the diode losses, the on-state voltage V_F at a certain temperature is identified from the forward current I_F with the help of the look-up table from which the reverse recovery loss energy is calculated at a certain temperature. The calculation of the conduction losses of the diode, P_{conT}, uses the value of forward voltage and current from the datasheet at the certain temperature:

$$P_{conT} = \frac{1}{T}\int_{t_s}^{t_s+T} I_F(\tau)V_F(I_F(\tau))d\tau \tag{6.6}$$

Meanwhile, assuming that number of the switching pulses within a fundamental time

period is S_P, P_{onS} and P_{offS} are determined after finding the values of turn-on energy E_{onS} and turn-off energy E_{offS} respectively in the look-up table. The switching losses obtained within one fundamental period are shown as:

$$P_{onS} = S_P \cdot \frac{1}{T}\left[\frac{V_{CE,off}}{V_{CE,ref}} E_{ons}(I_C(t))\right] \tag{6.7}$$

$$P_{offS} = S_P \cdot \frac{1}{T}\left[\frac{V_{CE,off}}{V_{CE,ref}} E_{offs}(I_C(t))\right] \tag{6.8}$$

where $V_{CE,off}$ is the blocking voltage occurring in the IGBT and $V_{CE,ref}$ is the reference block voltage in this particular case. Likewise, the reverse recovery energy, E_{rec}, is obtained from the forward current I_F with the help of look-up table at a certain temperature. So, the reverse recovery losses P_{offT} are expressed as:

$$P_{offT} = S_P \cdot \frac{1}{T}\left[\frac{V_{F,off}}{V_{CE,ref}} E_{rec}(I_F(t))\right] \tag{6.9}$$

where $V_{F,off}$ is the blocking voltage occurring in the diode. Therefore, the total losses of the diode are:

$$P_{totalT} = P_{conT} + P_{offT} \tag{6.10}$$

Overall, the total losses of the IGBT can be calculated from Equation 6.5 and 6.10, and the details of the switching and conduction losses of one SM in terms of P_{sw} and P_{con} as tested in this simulation are listed in Table 6-II for all proposed voltage balancing schemes.

When the evaluation of the power losses of all SMs has been conducted, the average total losses of all three SMs for different voltage balancing schemes are calculated. The results for average switching losses, diode losses and total losses of CSA, ISA, HSA and PSA are shown in Figure 6.20. It can be seen from the figure that the conduction losses for the CSA, ISA and HSA are very close, while those for the PSA are increased by 4W. However, the switching losses for the PSA are reduced significantly compared to CSA. The switching losses of two complementary IGBTs are different because, firstly, from the operation, it is known that the lower switch of the SM is always more stressed compared to the upper switch, therefore it is expected that more loss will occur at that switch. Secondly, according to Equation 6.7 and 6.8,

this is a low switching scheme and the currents flowing through them are different, and finally leads to the losses difference between two complementary IGBTs. Compared to the ISA and HSA, the PSA still has the best ability in reducing the switching losses with a 18W reduction. Overall, the PSA is confirmed to have the lowest total power losses, followed by the ISA and HSA.

Table 6-II The details of mean loss of IGBTs and diodes for all proposed schemes and conventional sorting algorithm.

Conduction Losses (W)					
Methods	**S1**	**S2**	**D1**	**D2**	**Total**
CSA	2.011	17.140	2.126	0.514	21.791
ISA	1.773	17.160	2.045	0.828	21.806
HSA	1.833	17.040	2.109	0.736	21.718
PSA	2.730	19.010	2.311	1.989	26.040
Switching Losses (W)					
Methods	**S1**	**S2**	**D1**	**D2**	**Total**
CSA	65.940	146.900	78.380	38.300	329.520
ISA	7.369	47.930	19.310	2.712	77.310
HSA	6.854	47.260	19.740	2.434	76.288
PSA	7.220	36.120	14.150	1.338	58.828

From this section, it can be concluded that all three proposed methods can achieve the reductions in switching frequency, which consequently helps to reduce switching losses during operation. Among them, PSA shows a great reduction in the switching power losses. This distinct characteristic is attractive for real projects with an MMC topology.

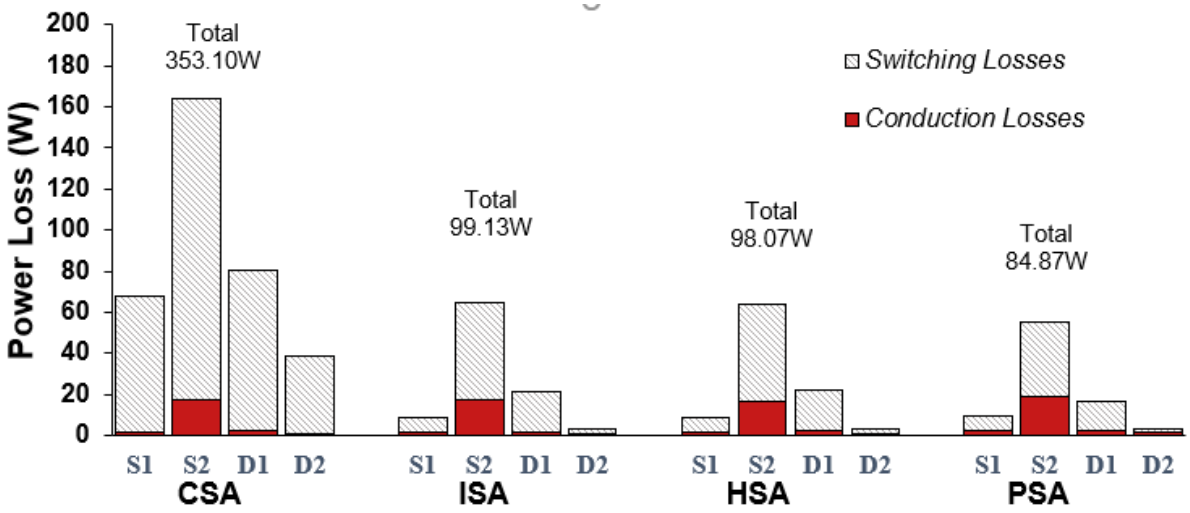


Figure 6.20 Average power loss of IGBTs and diodes (ABB 5SNG0250P330300) of all upper arm SMs for all three proposed scheme and conventional sorting algorithm.

6.6 Chapter Summary

This chapter presented a new priority-based voltage balancing algorithm to improve the well-known sorting algorithm commonly used for MMC. The proposed method helps to narrow down the searching of SMs during every sampling period to a limited number of priority groups to achieve the reduction in switching frequency. The less intensive search also leads to fewer execution resources being used from the processor, which reduces computational complexity. The simulation results have proven the effectiveness of the proposed scheme for both 4-level and 22-level models. In comparison to the other techniques that have been discussed throughout this thesis, this proposed technique has demonstrated a greater reduction in switching frequency. On top of inheriting the advantage of CSA, the PSA can reduce the overall power losses, especially the switching losses of the IGBT module without extra measurement nor hardware. However, precise control of the voltage ripple range is still required further investigation. The proposed algorithms also have been verified on MATLAB/Simulation with different conditions. The proposed algorithms are further validated on a practical prototype in the following chapter.

Chapter 7. Experimental Validation

7.1 Introduction

This chapter presents the results of the validation of the proposed algorithm, through the implementation of real-time control. In order to verify the effectiveness of all proposed techniques, a 4-level MMC scaled-down experimental test-rig was built. This chapter first introduces the generic concept of the whole system platform, and gives detailed information concerning the electrical components selected for the experiment including voltage and current transducers, DC power supply, adjustable RL load, gate driver circuits and the general control board (GCB). Secondly, the method used for real-time control with the help of MATLAB and related packages is illustrated. Thirdly, a comparative study is conducted in order to obtain an in-depth understanding of the difference between the conventional sorting algorithm and proposed sorting algorithms and to verify the superior characteristics of the proposed techniques. Finally, comparisons are made of the results of the simulation and those from the experiment.

7.2 General Diagram

The DC supply of the single 4-level MMC system is fed by two EX354RT TIPPLE 300W power supplies. The output side is connected to an adjustable RL load to test the system's performance under various load conditions. The general block diagram is shown in Figure 7.2 and Figure 7.2 illustrates all of the connections between the different parts of the MMC system. The general control board is the core component which is responsible for data collection and processing, interface communication and control signal generation.

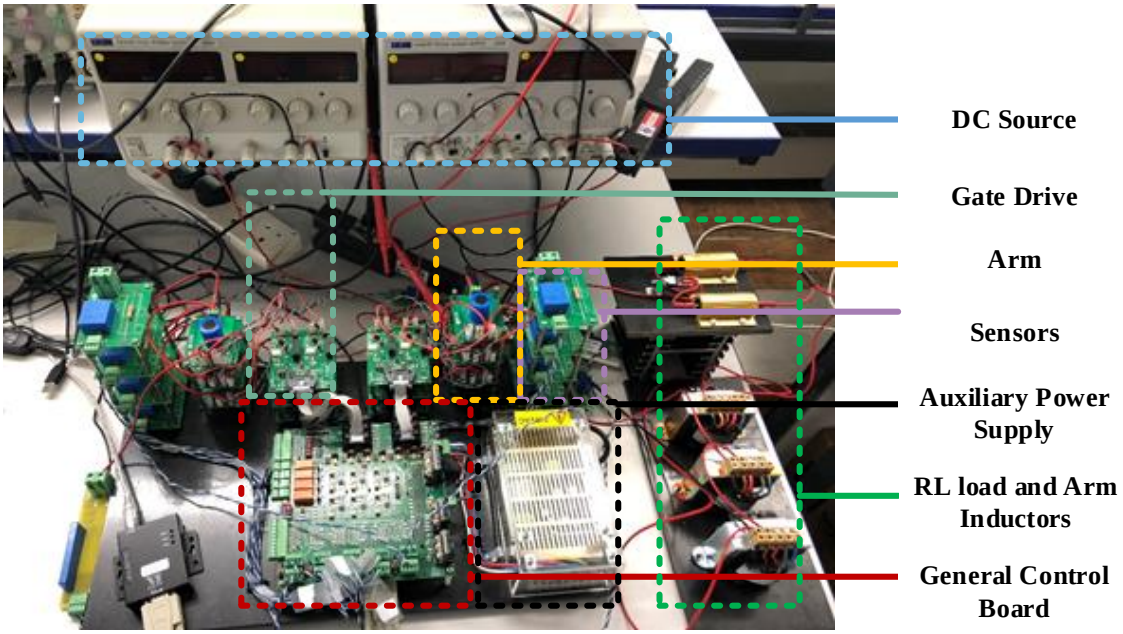


Figure 7.1 Photograph of the test platform.

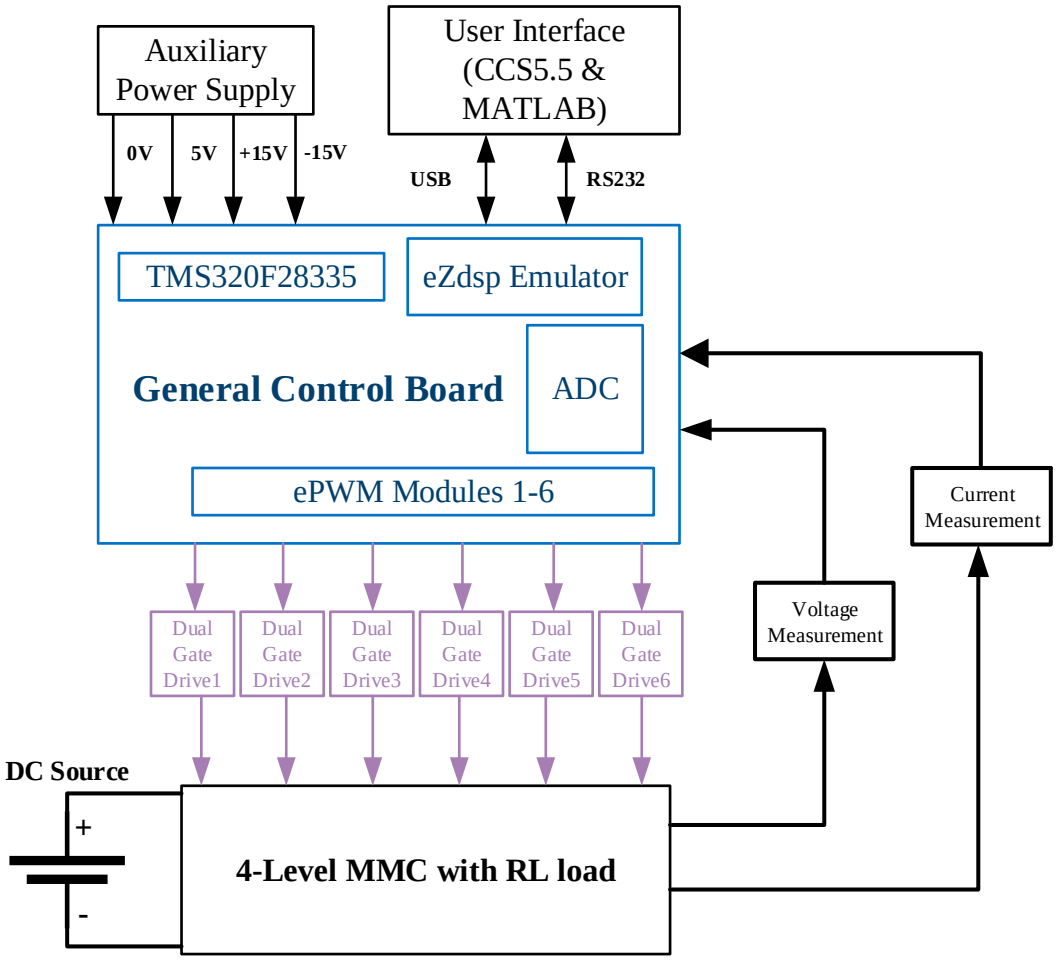


Figure 7.2 General block diagram of the practical experiment.

7.3 Parameter Selection

The design specifications are listed in Table 7-I. For the *N*+1 modulation, the minimum number of SMs required for one arm is 3. The method of the selection of arm inductor and the SM capacitor was introduced in Chapter 3. The RL load is an adjustable load used to test the system's performance from a light mode with 33 Ω load resistance to heavy mode with 68 Ω load resistance.

Table 7-I Parameters of Experiment

Parameters	Value
Number of SMs per arm (N)	3
Modulation index (m_i)	0.9
Carrier frequency (f_c)	2.5 kHz
Processor sampling frequency (f_{sample})	20 kHz
SM capacitor (C)	1000 μF
Arm inductor (L)	1 mH
Load inductor (L_L)	4 mH
Load resistor (R_L)	68 Ω
Output frequency (f)	50 Hz

7.4 Microprocessor Control System

For the experiment, TMS320F28335 DSP for real-time control was selected using a 32-bit floating-point CPU with 34 μs execution time from the Texas Instrument (TI) C2000 series, which has up to 18 PWM. Compared with the previous generation of CPUs from the same supplier (TI), the overall performance is increased by 50%. There are three primary advantages of this processor: it simplifies software development, shortens development cycles, and reduces development costs [113].

The TMS320F28335 DSP is designed to work with Code Composer Studio (CCS v5.5) software. The schematic of the 4-level MMC is built in the MATLAB/Simulation environment, with the help of the Simulink Embedded Target Support Package (TSP) and Real-Time

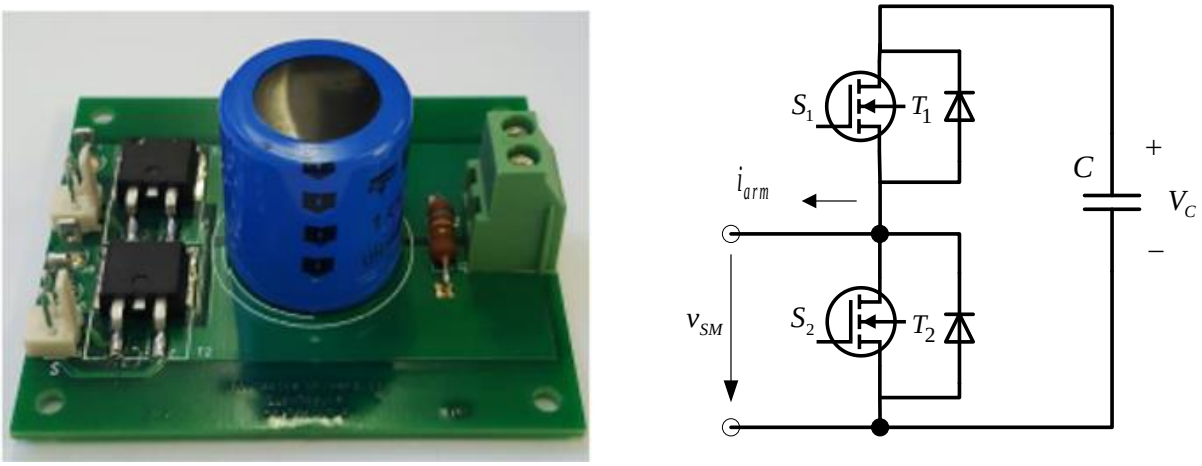
Workshop Embedded Coder (RT-WEC) package. The simulation is converted into downloadable code and subsequently optimised. In order to access the data from the DSP and to achieve real-time processing, an external MATLAB mode is implemented [114]. This external mode establishes communication between Simulink and the generated code on the DSP during the running time. Finally, the converted C code of the system is downloaded to the DSP using CCS v5.5.

7.5 Main Circuit Design

The arm current measured by the CAS-15 current sensors requires a +5V power supply. The SM voltage measurement is monitored by six Hall effect LV25-P voltage sensors, which requires a 15V power supply. Meanwhile, the analogue-to-digital (ADC) channels of TMS320F28335 DSP only have a limited voltage range (0-3V), and therefore it is necessary to set up the voltage divider circuit to the general control board (GCB) in order to supply all the sensors simultaneously. The GCB is designed at Newcastle University and consists of power supply, isolation, filters and voltage divider components as part of the main interface board of the DSP.

7.5.1 Sub-module design

A half-bridge structure is applied for the SM design. Depending on the rated voltage, the two semiconductors selected are IRF530N power MOSFET, which has a rated voltage of 100V, 17 A rated current and 90 mΩ gate resistance. The capacitor is a VISHAY 56 aluminium capacitor that has 1000μF capacitance with ± 20% tolerance and the rated voltage is 63 V. Even though the SM capacitor employed in the real project was the dry type capacitor with much higher capacitance, the choice for this experiment was based on cost-effectiveness. The proposed voltage balancing schemes require less accuracy and have greater voltage tolerance, and the price of aluminium capacitors is 90% lower than that of the dry type. A diagram and photograph of the SM circuit are provided in Figure 7.3.



(a) (b)

Figure 7.3 A half-bridge structure model of SM. (a) Real model. (b) Schematic model.

7.5.2 Gate driver

The half-bridge structure has two complementary power MOSFETs, but the GCB only provides a voltage signal of 0-3V which is insufficient to drive the MOSFETs which require 15V voltage. Given the necessity of isolation and amplification, a dual gate drive designed by Newcastle University which is shown in Figure 7.4 was selected. The drive signals are generated from the sorting and proposed algorithms with 2.5 kHz carrier waveforms. The PWM signals of the upper MOSFET S_1 and the lower MOSFET S_2 are complementary signals with a $3\,\mu s$ deadtime setting. The drive signals are then amplified by the dual gate drive to become the gate signals of the two MOSFETs. Normally the switching signal of the upper MOSFET is defined as to representing the switching state of the corresponding SM. The GCB provides 6 pairs of PWM signals for the 6 dual-gate drive boards and controls the corresponding SMs. Therefore, it is possible to achieve control of the switching all six of the SMs in this single phase 4-level MMC.

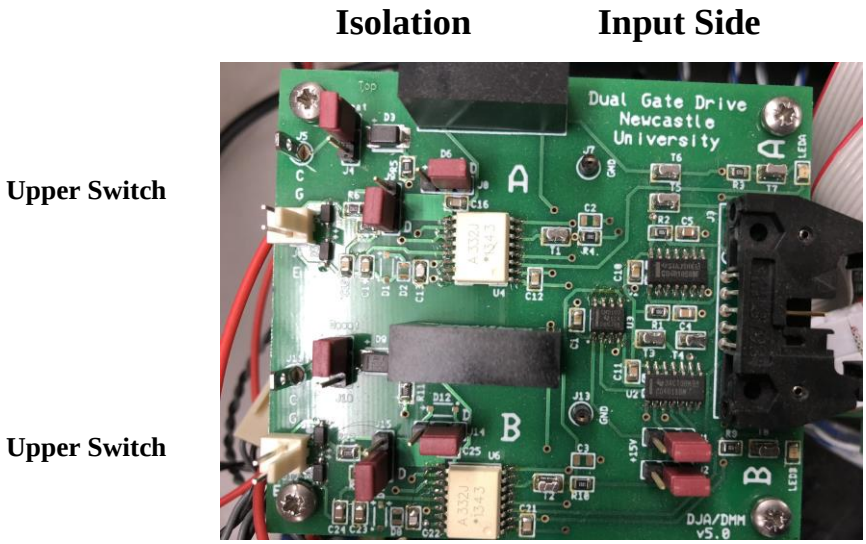
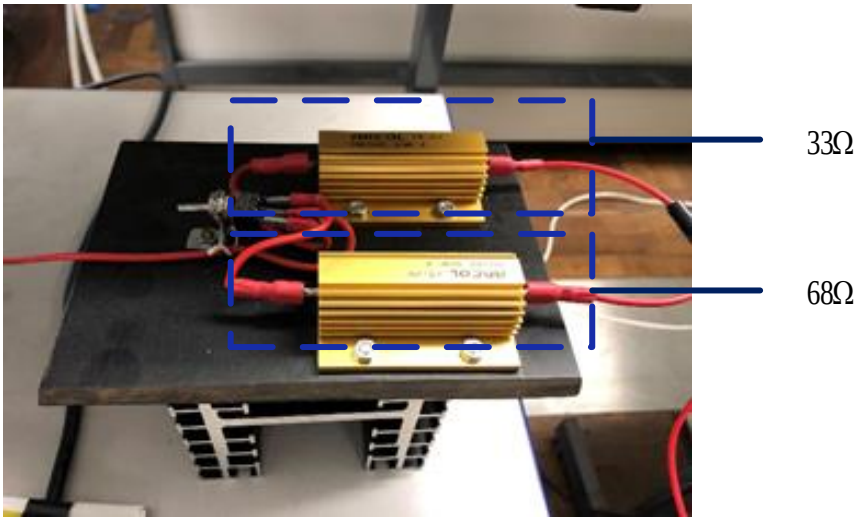


Figure 7.4 Dual gate drive of SM.

7.5.3 RL load and arm inductor

The load resistor R_L of the load has a 'two-way design'. The two resistors R_1 and R_2 are connected in parallel and mounted on a heat sink, where the lower resistor R_1 is 33 Ω and the higher resistor R_2 is 68 Ω. The inductors applied in the circuits are mounted together and include the two arm inductors L and load inductor L_L. Meanwhile, all the inductors are taped inductors and are adjustable from 0 mH to 4 mH. There are three specific reasons for this design: firstly, for the MMC to run at different load conditions; secondly, to verify the function of the arm inductors in terms of circulating current suppression; and thirdly, to enable the testing of dynamic performance when a sudden change in the load occurs in this experiment. Resistors and inductors are shown in Figure 7.5.

(a)



(b)

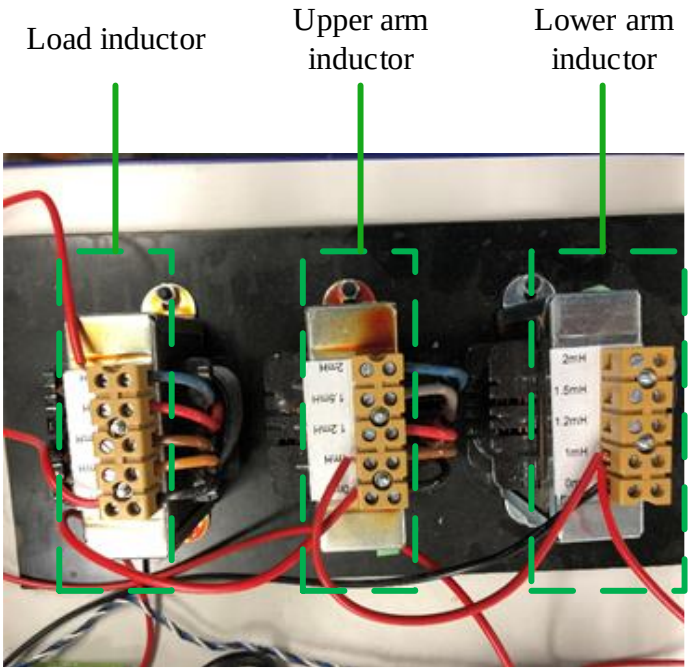


Figure 7.5 R and L configuration. (a) Parallel connection of load resistor. (b) Three adjustable inductors.

7.6 Experimental Results

With the help of a Tektronix MDO3014 Oscilloscope and its matched probes, the results of the experiment can be captured. Also, as the 12-bit ADC was 0-3V input, the accuracy of the ADC is $\frac{3V}{2^{12}} \approx 0.7\text{mV}$, which means that variation less than 0.7mV cannot be detected, and so extra caution should be taken when dealing with the accuracy of the calculation. The modulation signals of all the proposed approaches are tested based on the LSPWM.

7.6.1 Conventional sorting algorithm

The conventional sorting algorithm (CSA) is tested first, where the DC voltage is set at 50V. The results of the output voltage and current are shown in Figure 7.6. The output voltage has clearly 4 levels and the fundamental frequency is 50 Hz. From Figure 7.6, the output voltage is shown on Channel 1 and the output current on Channel 2 for 5 cycles, the peak-to-peak voltage is 50V and the peak-to-peak current is around 800mA.

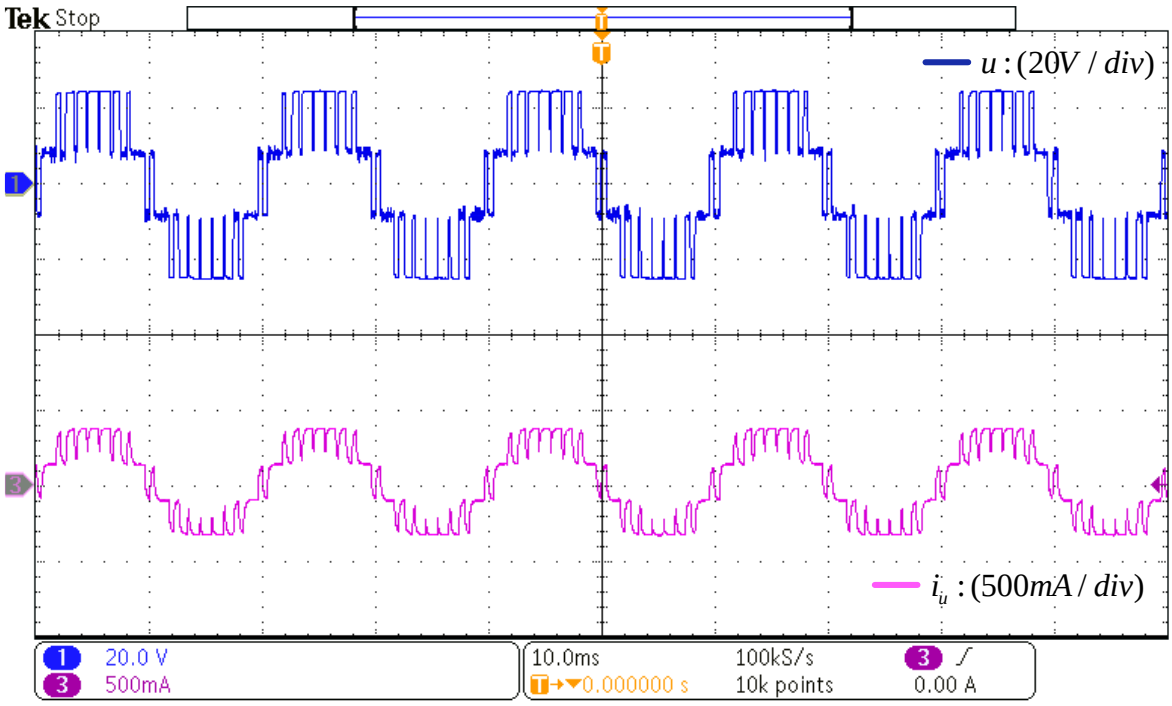


Figure 7.6 Output voltage and current waveform of CSA.

Figure 7.7 shows the capacitor voltage of the upper arm of CSA, which has around 350mV peak-to-peak ripple voltage with respected to the expectation value 16.67V. The SM1, SM2 and SM3 are shown on the channel 2 to 4 respectively. From the zoomed-in graph in Figure 7.7, the ripple voltage of SM1 against the output voltage, arm current and gate signal is clearly depicted, showing the deviation of capacitor ripple is less than 0.4V. Compared to the reference voltage 16.67V, the capacitor voltage ripple is less than 1%

The modulation signal and gate signals of SM1 to SM3 is shown in Figure 7.8. The modulation signal is generated by LSPWM, the gate signals of all three SMs indicate that the switching frequency is high. According to the number of switching pulses over 10 cycles, the average switching frequency in the figure is calculated as 2521 Hz. According to Figure 7.9, the amplitude of the circulating current of CSA is less than 40 mA, and the THD of the output voltage is 36.39%.

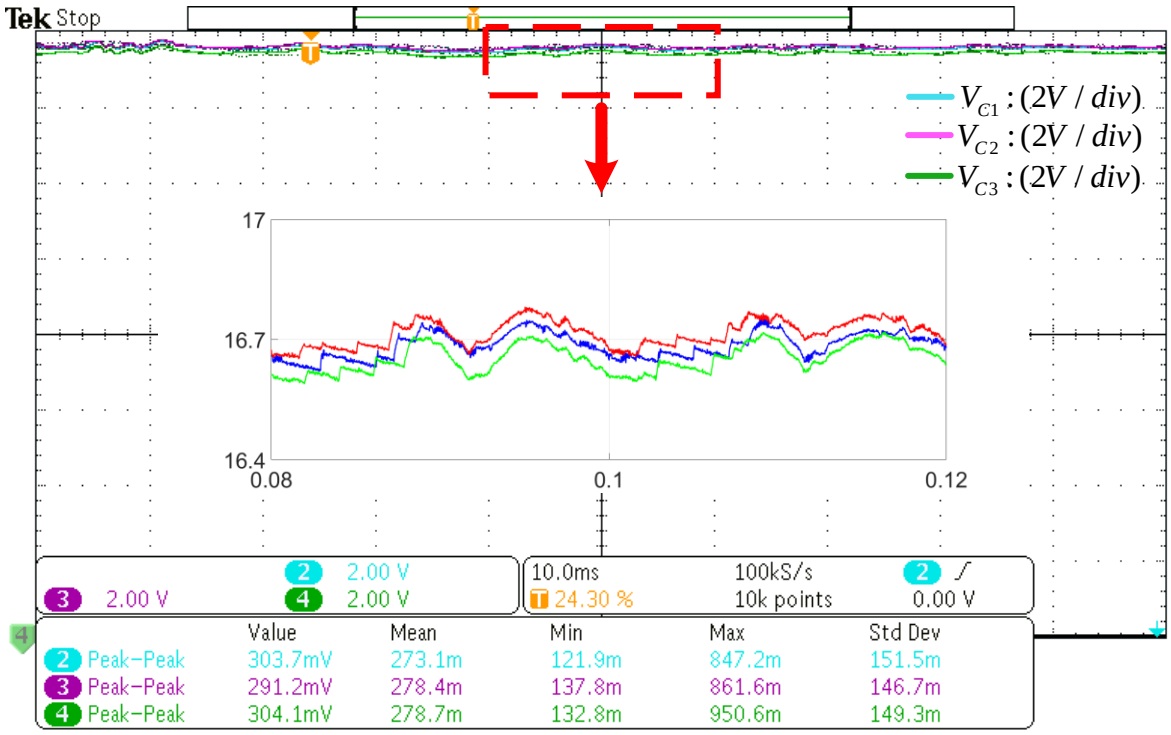


Figure 7.7 SM capacitor voltage ripple for the upper arm SMs of CSA.

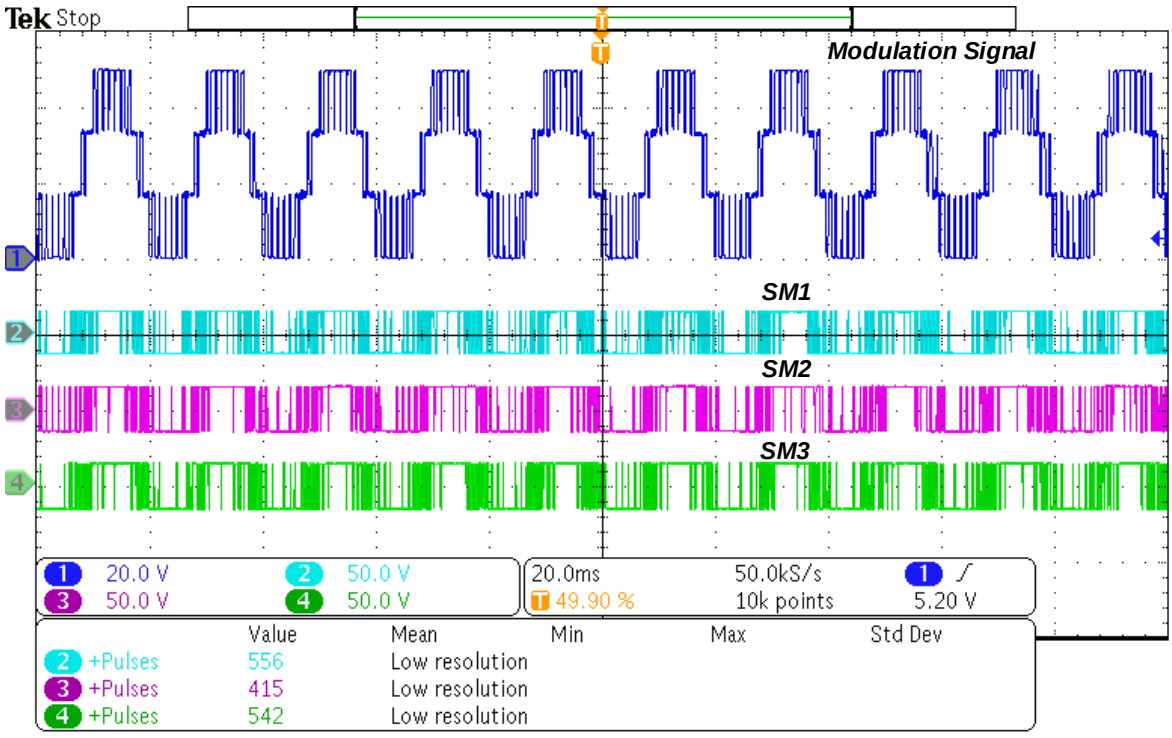
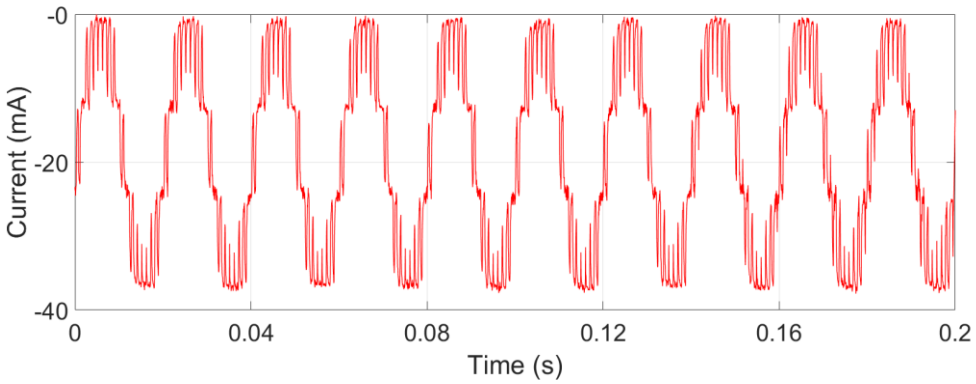


Figure 7.8 Capacitor voltage ripple of upper arm SMs of CSA.

(a)



(b)

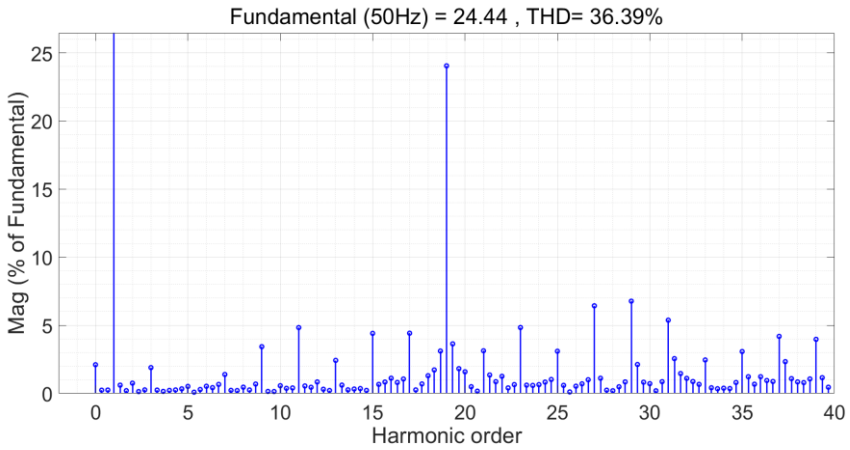


Figure 7.9 Performance of CSA. (a) Circulating current. (b) THD of output voltage.

7.6.2 Index-based sorting algorithm

The coefficient α is set to 1.1 before implementing the ISA to the prototype. The output voltage and current of ISA are presented in Figure 7.10, the output voltage is shown on the Channel 1 and the output current on the Channel 2 for 5 cycles, the peak-to-peak voltage is 50V and the peak-to-peak current is around 800mA, which is similar to CSA.

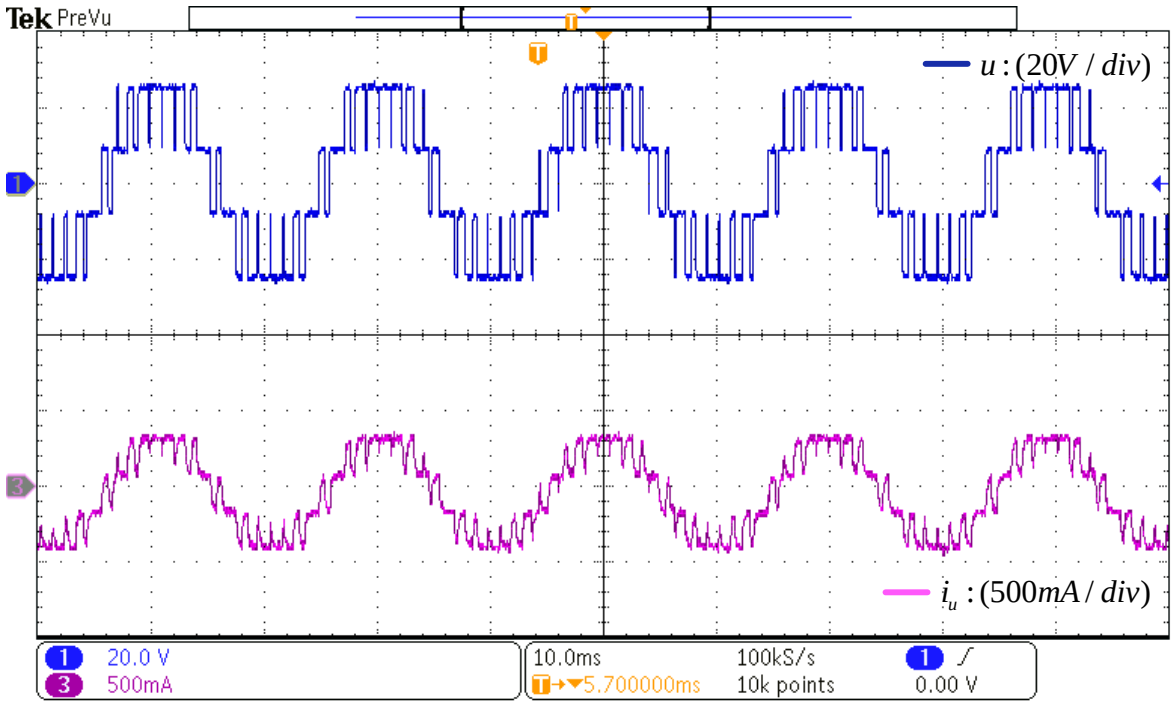


Figure 7.10 Output voltage and current waveform of ISA.

The comparison between SM capacitor voltage of ISA is shown in Figure 7.11, where all the SMs voltage are balanced well. From the zoom-in diagram, the capacitor voltages are balanced at the reference voltage, 16.67V, with less than 318.13mV voltage variation. Moreover, the SM voltage does not track each other's value strictly, so the ripples are 'relaxed' well within the permissible range.

The modulation signal and gate signals of SM1 to SM3 is shown in Figure 7.12. In the diagram, the modulation signal is presented in channel one to demonstrate the required inserted SM number n of the arm, the channel 2-4 shows the gate signal of all three SMs. The average switching frequency can be calculated by the number of the pulses within the 10 cycles, equals to 321.7 Hz. Compared to the CSA, the significant reduction has been achieved. According to Figure 7.13, the amplitude of circulating current of ISA is less than 40 mA which is close to the performance of CSA, and the THD of the output voltage is 37.31%.

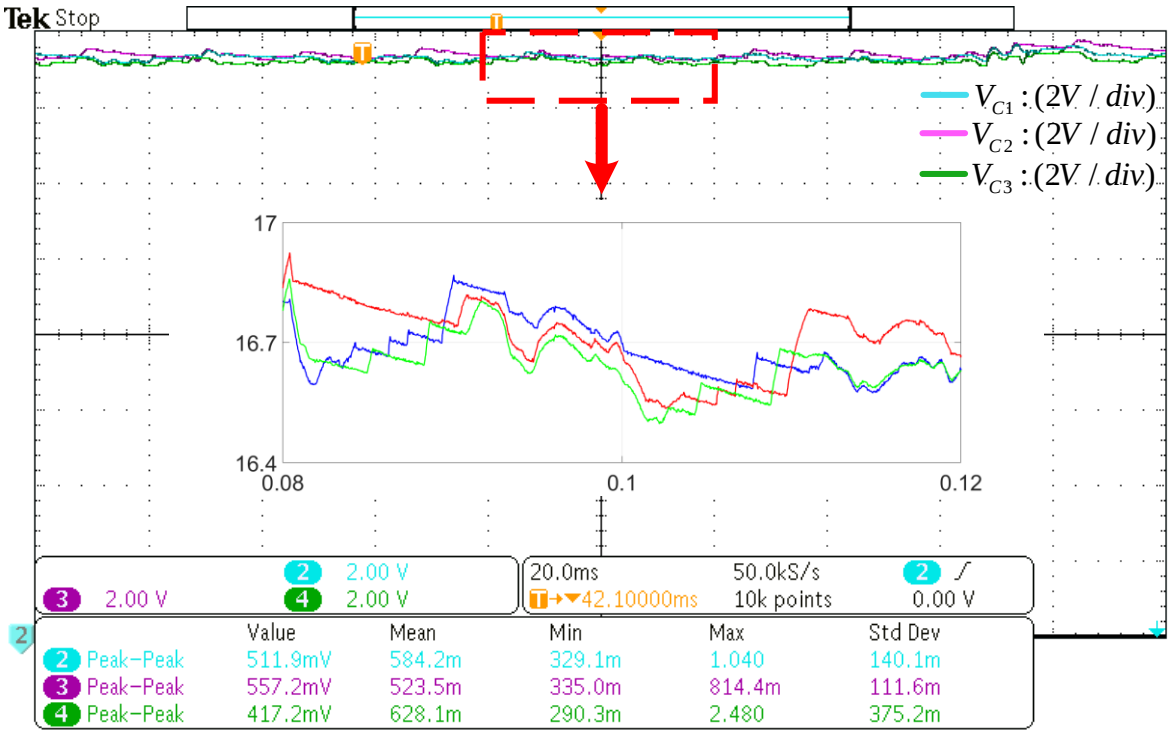


Figure 7.11 SM capacitor voltage ripple for the upper arm SMs of ISA.

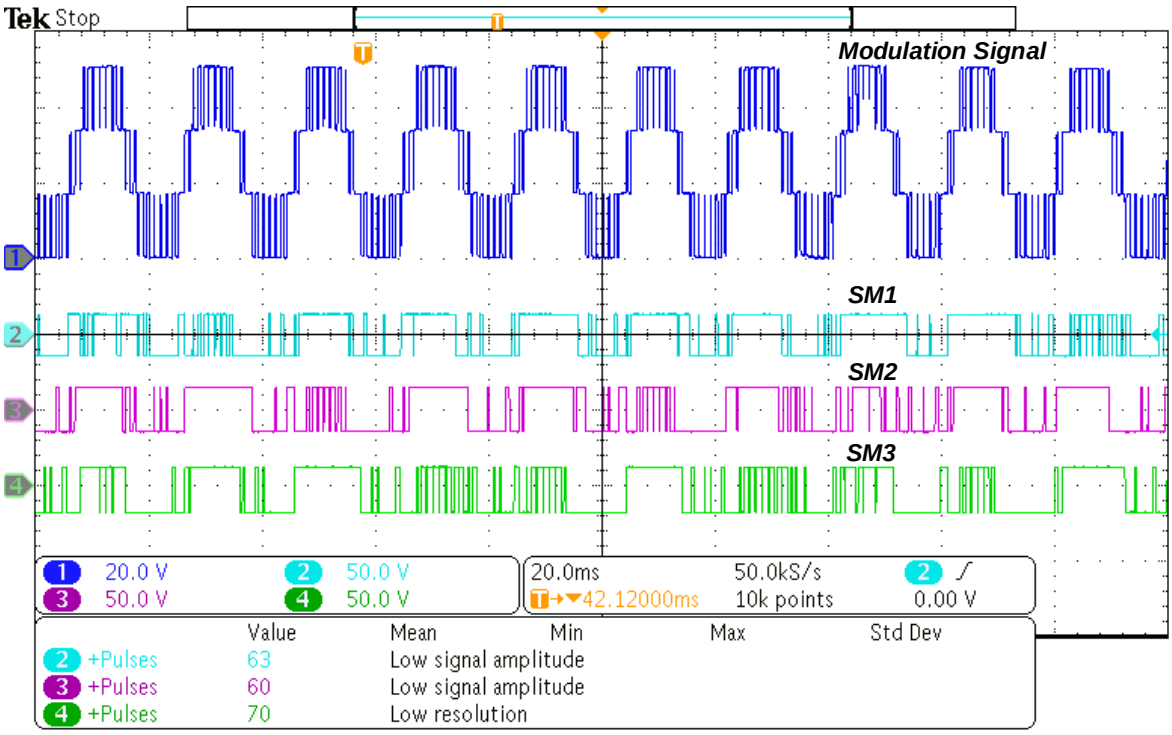
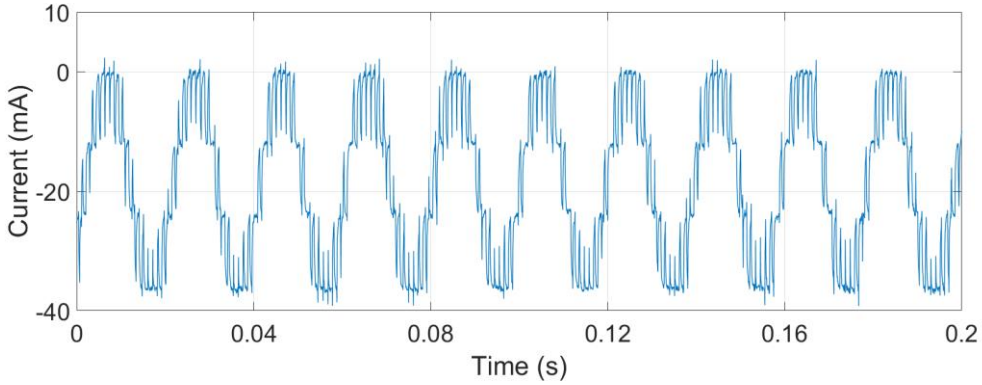


Figure 7.12 Capacitor voltage ripple of upper arm SMs of ISA.

(a)



(b)

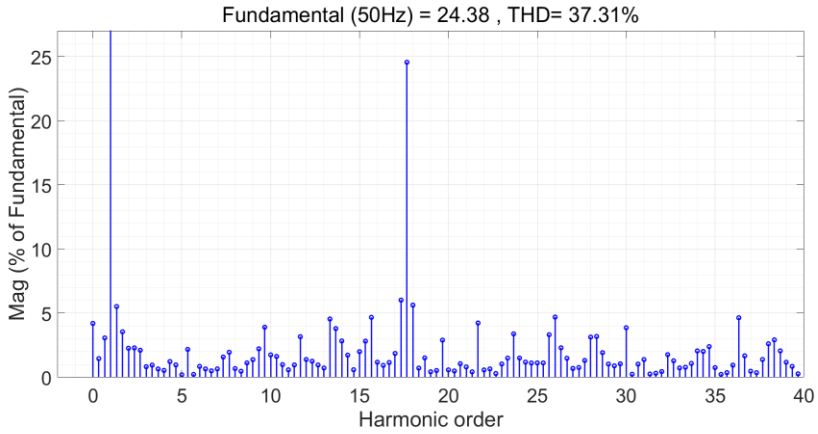


Figure 7.13 Performance of ISA. (a) Circulating current. (b) THD of output voltage.

7.6.3 Hybrid sorting algorithm

The validations of heap sorting are illustrated in Figure 7.14 to Figure 7.16. In Figure 7.14, the output voltage is shown on Channel 1 and the output current on Channel 2 for 5 cycles, the peak-to-peak voltage is 50V and the peak-to-peak current is around 800mA. The capacitor voltage depicted in Figure 7.15 indicates that the capacitor voltage ripple of heap sorting has around 350mV peak-to-peak ripple voltage with respect to the expectation value 16.67V. The SM1, SM2 and SM3 are shown on channel 2 to 4 respectively. The average ripple voltage is 347.4mV which is close to CSA.

The modulation signal and gate signals of SM1 to SM3 is shown in Figure 7.16. In the diagram, the modulation signal is presented in channel 1 and the channel 2-4 shows the gate signal of all three SMs. The average switching frequency equals to 1730 Hz. Compared to the CSA, the minor reduction has been achieved. According to Figure 7.17, the amplitude of the circulating current is less than 40 mA, and the THD of the output voltage is 37.23%.

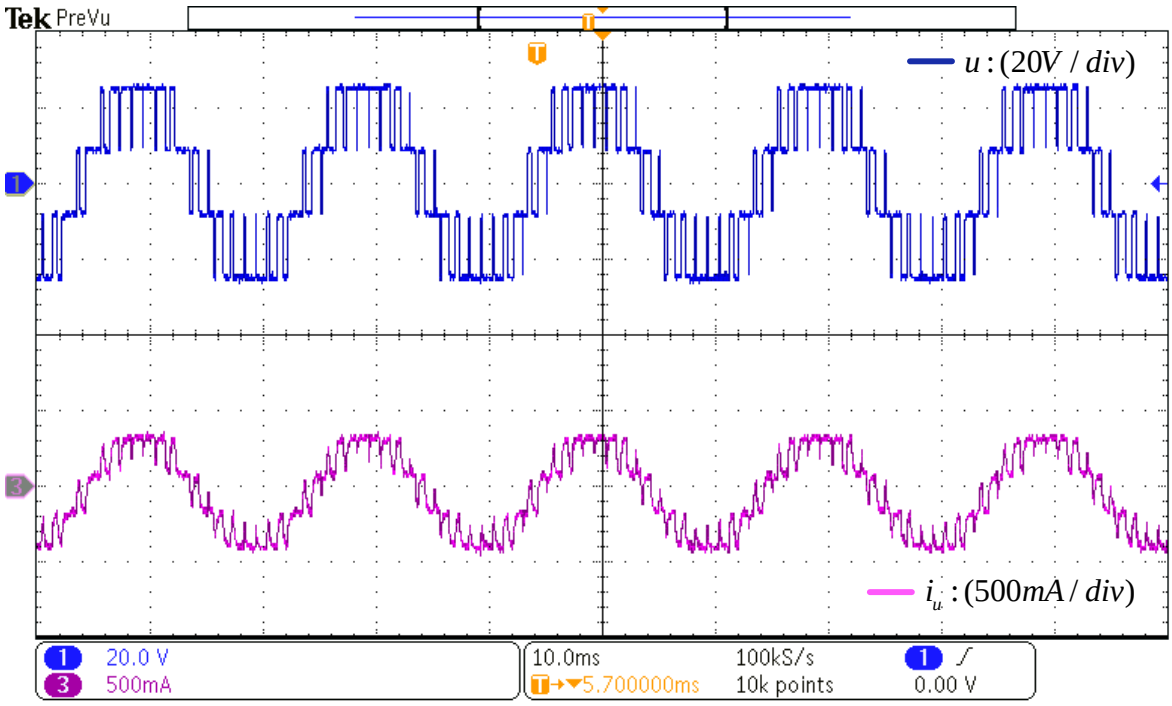


Figure 7.14 Output voltage and current waveform of heap sorting.

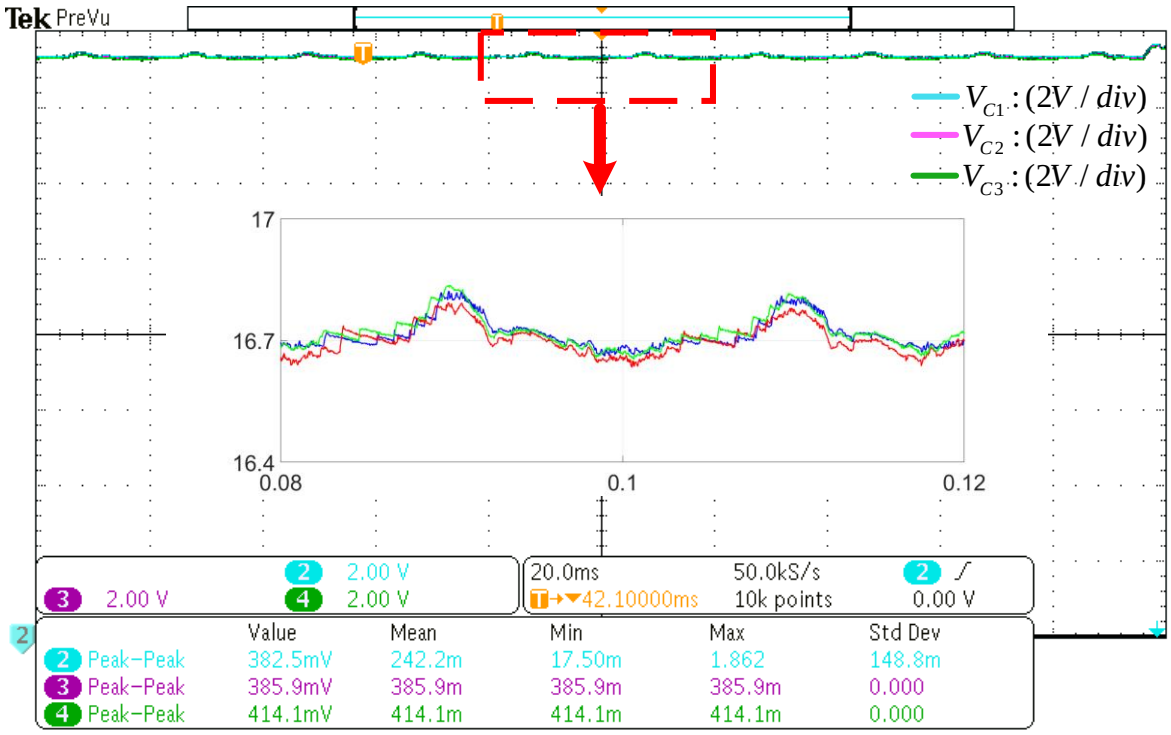


Figure 7.15 SM capacitor voltage ripple for the upper arm SMs of heap sorting.

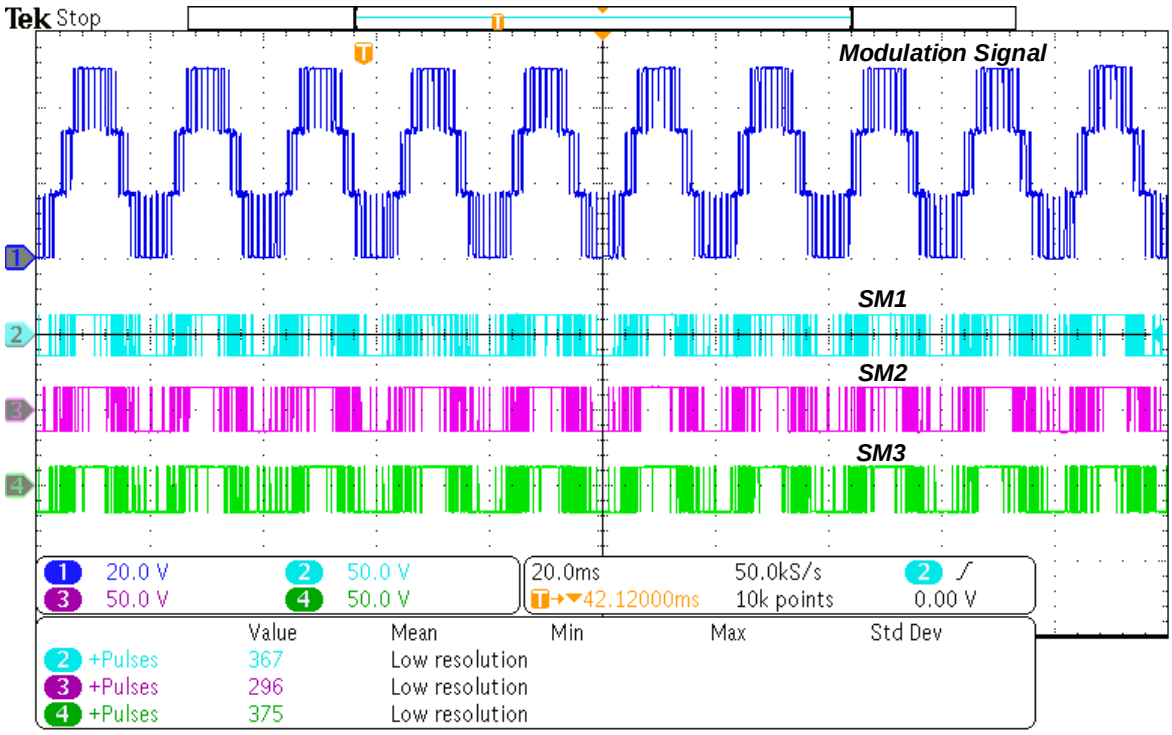
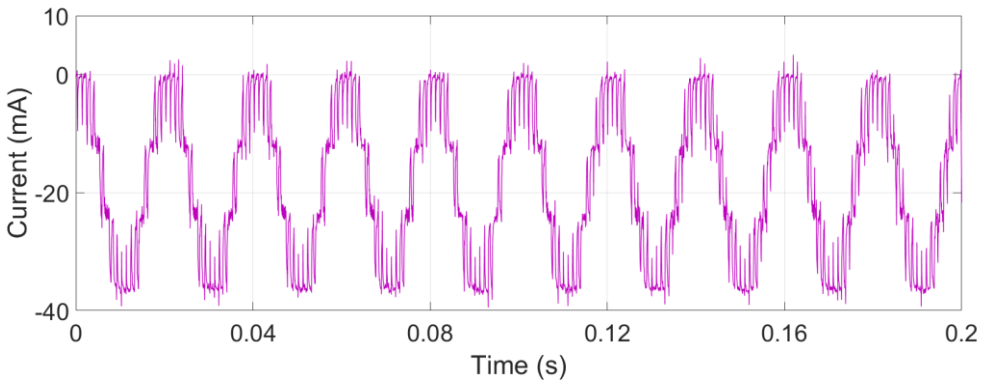


Figure 7.16 Capacitor voltage ripple of upper arm SMs of heap sorting.

(a)



(b)

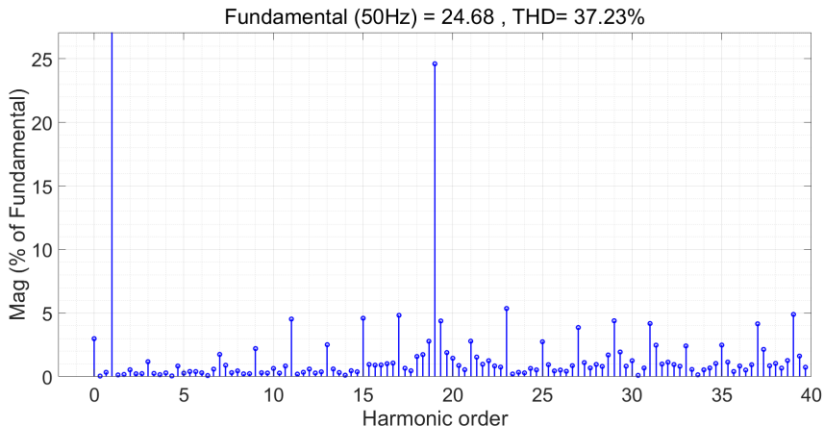


Figure 7.17 Performance of heap sorting. (a) Circulating current. (b) THD of output voltage.

Then, the HSA based on the heap sorting is implemented to the test-rig. Figure 7.18 illustrates the successful stair-cased voltage and current waveform of HSA, where the output voltage is shown on the Channel 1 and the output current on the Channel 2 for 5 cycles, the peak-to-peak voltage is 50V and the peak-to-peak current is around 800mA. The capacitor ripple voltage in Figure 7.18 indicates that the capacitor voltage ripple of HSA has increased to 380.43mV compared to heap sorting, but still within the 3% acceptable range.

The modulation signal and gate signals of SM1 to SM3 are depicted in Figure 7.20. In the diagram, the modulation signal is presented in channel 1 and the channel 2-4 shows the gate signal of all three SMs. Based on the data collected from the oscilloscope, the average switching frequency equals to 312 Hz. Compared to the CSA, the switching frequency reduction is 87.5%, and there is 81.2 reduction when compared to heap sorting. Overall, the effectiveness of both heap sorting and HSA have been verified successfully. The performance of circulating current and THD is shown in Figure 7.21, where the amplitude of circulating current is less than 40 mA and the THD of the output voltage is 37.23%.

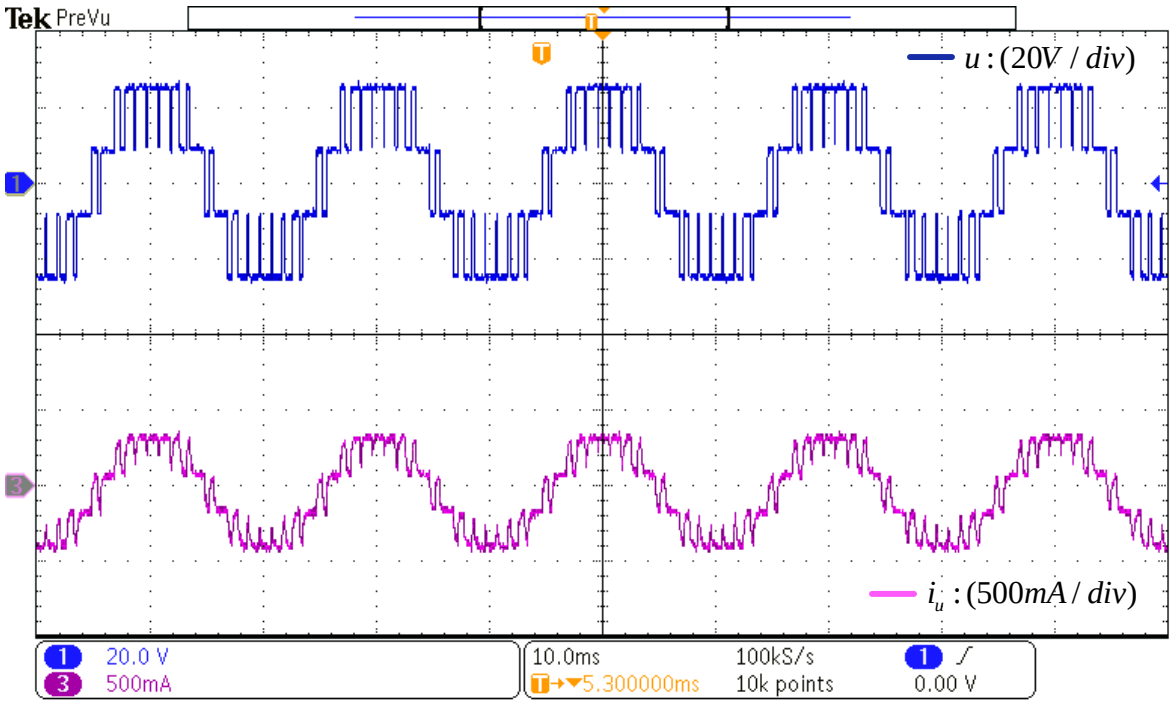


Figure 7.18 Output voltage and current waveform of HSA.

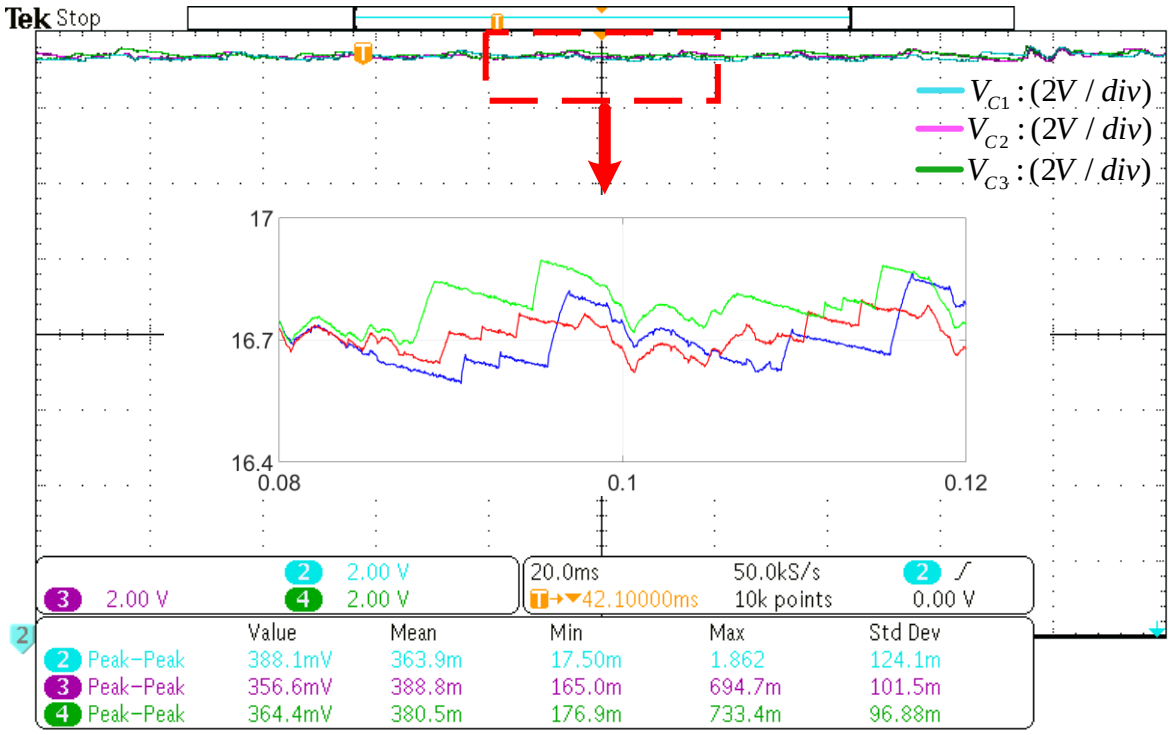


Figure 7.19 SM capacitor voltage ripple for the upper arm SMs of HSA.

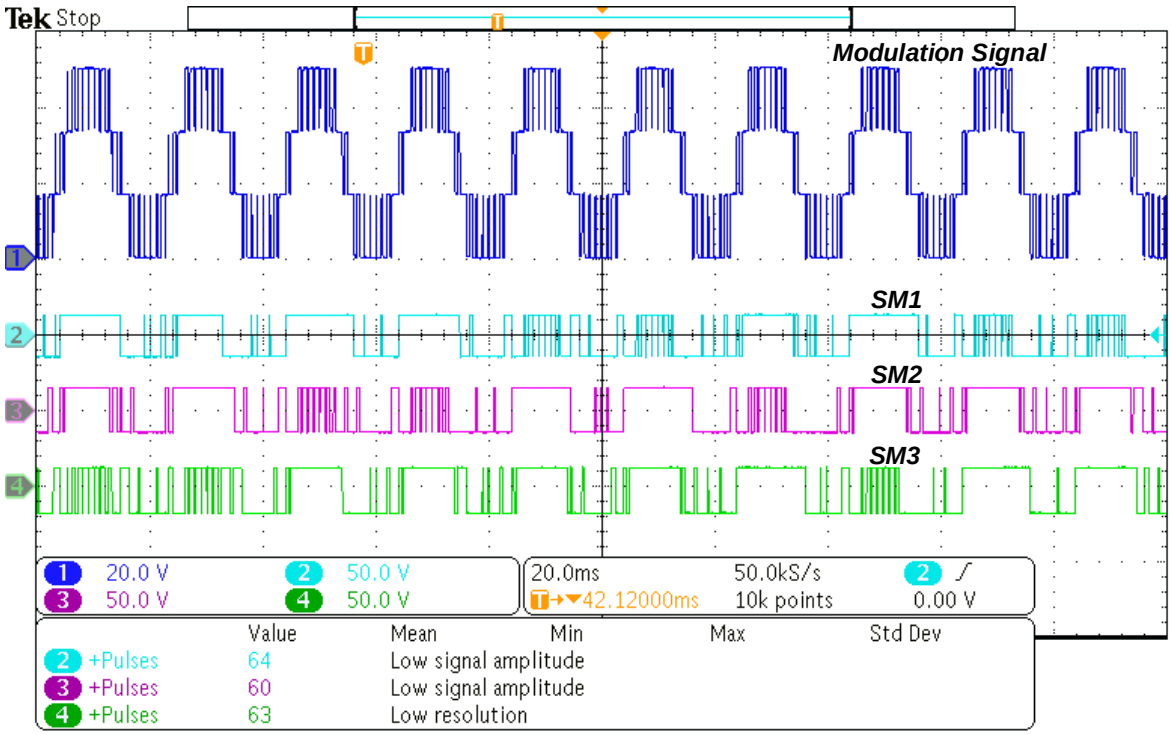
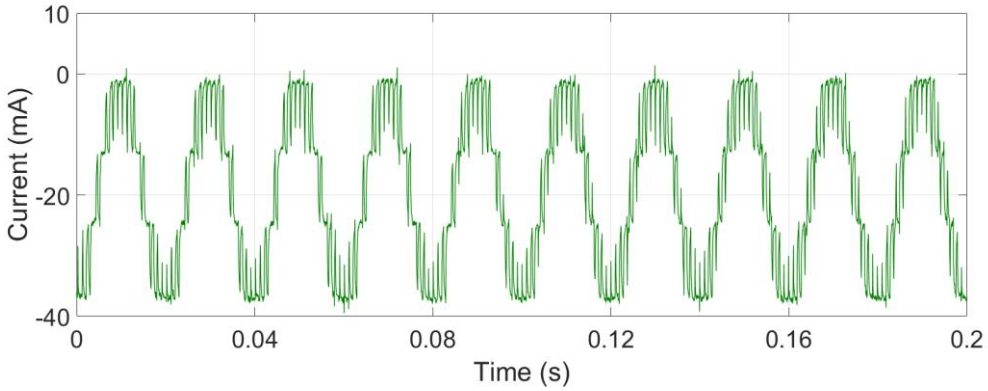


Figure 7.20 Capacitor voltage ripple of upper arm SMs of HSA.

(a)



(b)

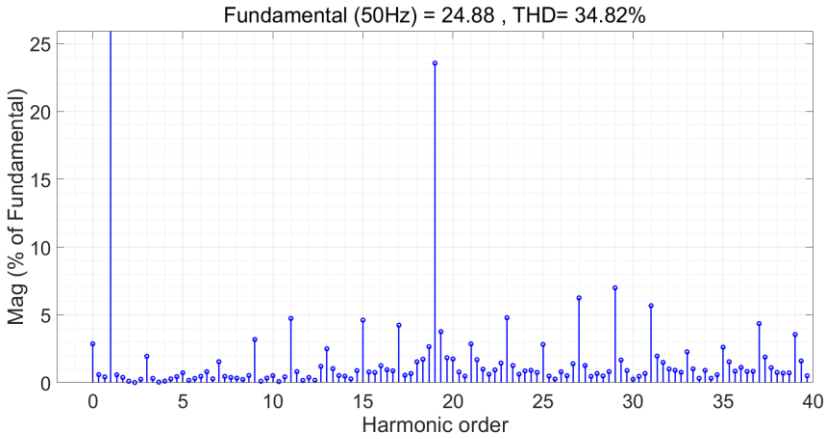


Figure 7.21 Performance of HSA. (a) Circulating current. (b) THD of output voltage.

7.6.4 Priority-based sorting algorithm

The output voltage and current of PSA are shown in Figure 7.22. The output voltage has clearly 4 levels and the fundamental frequency is 50 Hz. From Figure 7.22, the output voltage is shown on Channel 1 and the output current on the Channel 2 for 5 cycles, the peak-to-peak voltage is 50V and the peak-to-peak current is around 800mA. Compared to CSA, the impact of PSA the output quality can be neglected.

Figure 7.8 shows the capacitor voltage of the upper arm of PSA, where the capacitor ripple is increased to 440mV with respect to the expectation value 16.67V. The SM1, SM2 and SM3 are shown on the channel 2 to 4 respectively. From the zoomed in picture in Figure 7.8, the ripple voltage of SM1 against the output voltage, arm current and gate signal is clearly depicted, showing the average peak-to-peak value of capacitor ripple is 542.2mV. Compared to CSA, the voltage value has more flexibility within the ripple range and the ripple range is less than 1.6%, which meets the appropriate operation criteria.

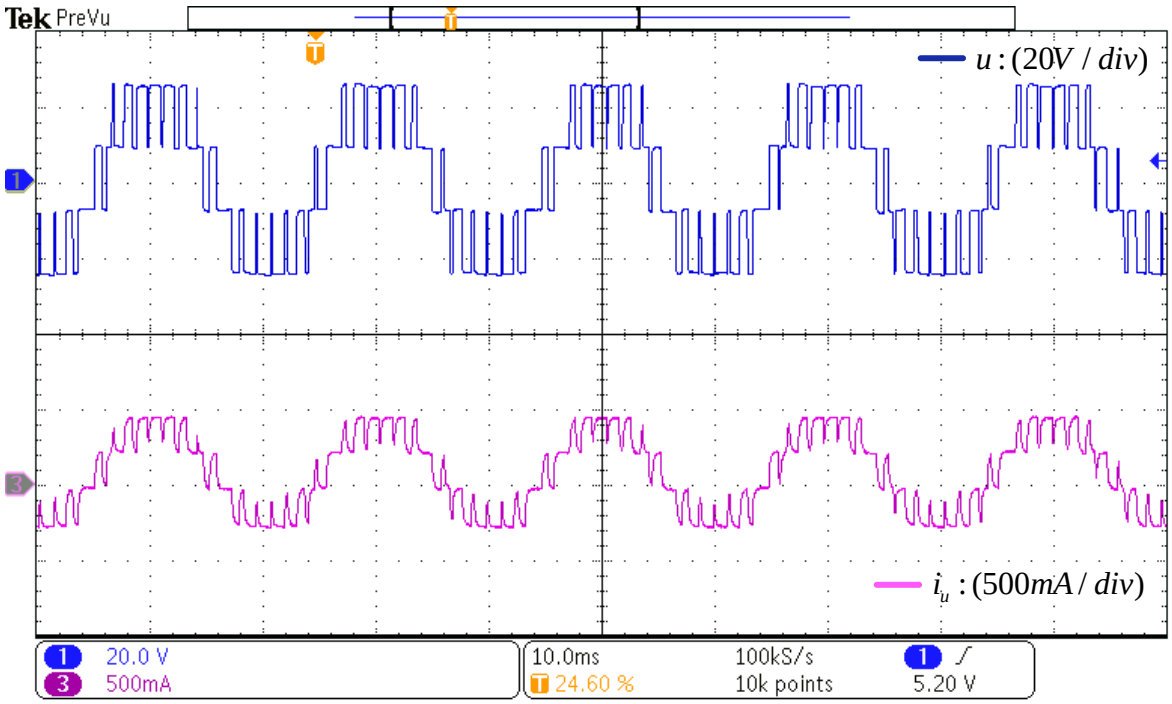


Figure 7.22 Output voltage and current waveform of PSA.

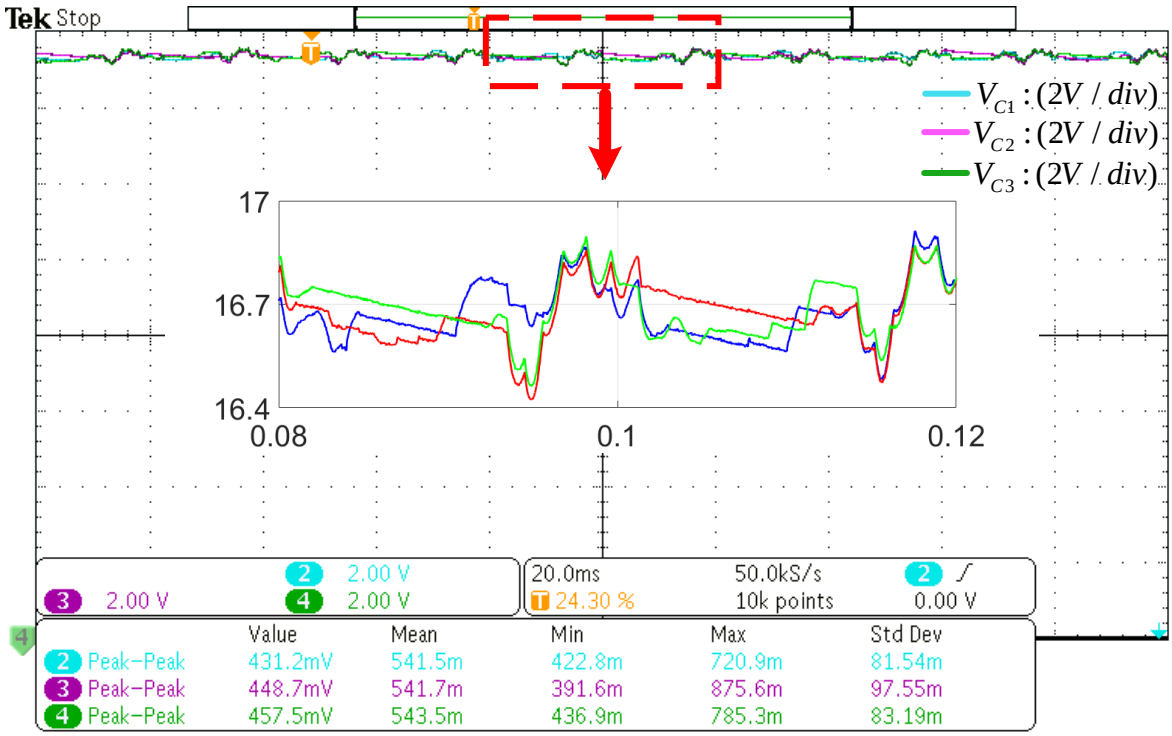


Figure 7.23 SM capacitor voltage ripple for the upper arm SMs of PSA.

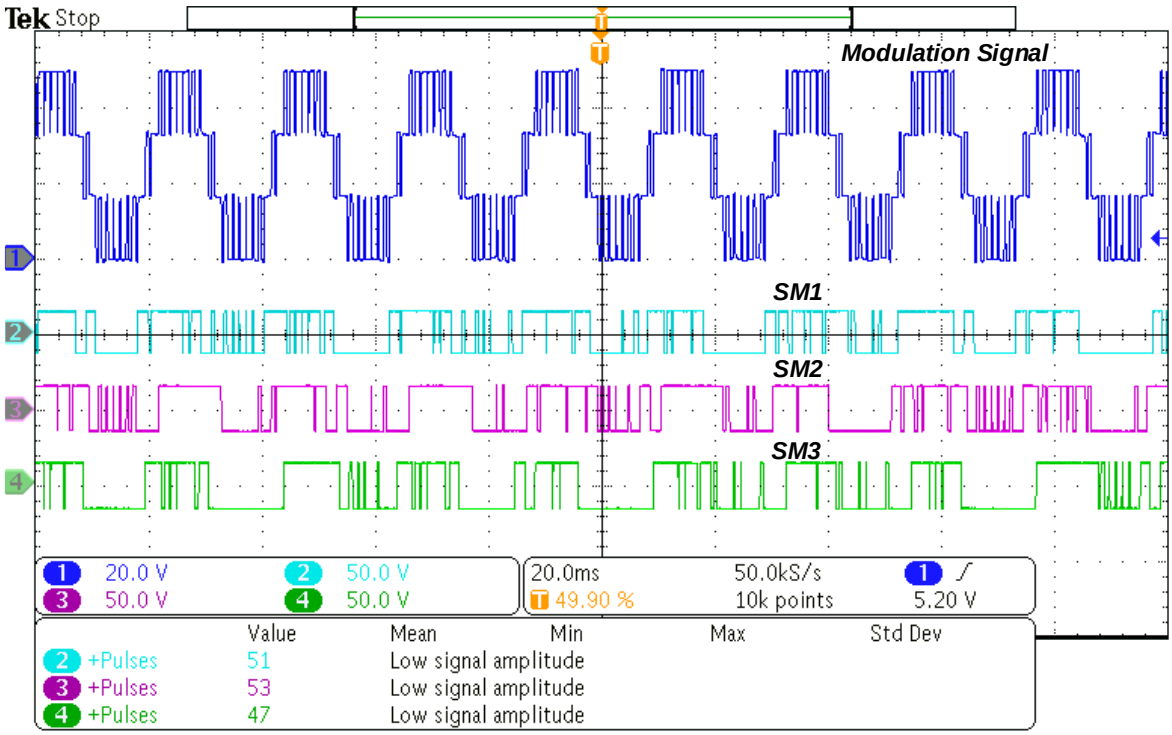
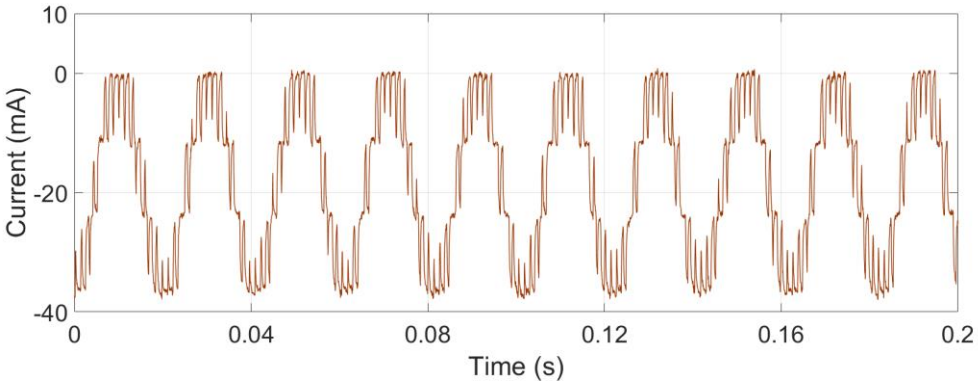


Figure 7.24 Modulation signal and gate signals of upper arm SMs of PSA.

(a)



(b)

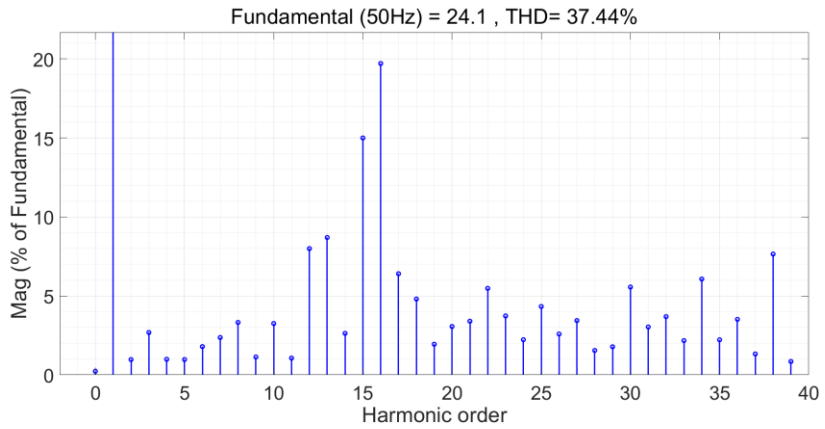


Figure 7.25 Performance of PSA. (a) Circulating current. (b) THD of output voltage.

The modulation signal and gate signals of SM1 to SM3 is shown in Figure 7.8. The modulation signal is generated by LSPWM, the gate signals of all three SMs indicate that the switching frequency has been reduced significantly. According to the number of switching pulses over 10 cycles, the average switching frequency of the SMs is 251 Hz. Compared to CSA, the switching frequency reduction is over 90%. The performance of circulating current and THD of the output voltage is shown in Figure 7.25, where the amplitude of circulating current is less than 40 mA and the THD is 37.44%. Therefore, it can be concluded that all proposed techniques have similar distortion. Overall, the PSA evaluated in the test has better performance in terms of switching frequency reduction because the SMs capacitor voltages inside the pre-defined range **X** are less likely to change their switching states.

7.7 Analysis of Results

The output voltage, capacitor voltage, arm current and gate signals have been reviewed in this chapter. In the previous section, all three of the proposed techniques were successfully verified. In addition, a further experiment was conducted to test the performance of the system with different carrier frequencies, and the results are summarised in Table 7-II. It is evident that the PSA most successfully minimises the switching frequency, with HSA in second place. The ISA is capable of decreasing part of the switching frequency, which is in accordance with the theory discussed from Chapter 4 to Chapter 6.

Also, the THD of the voltage and current were calculated based on the data from the oscilloscope. The rest ripple voltage and THD of all three proposed techniques exhibit no obvious variation, which is in accordance with expectations. The capacitor voltage ripple of the PSA is slightly higher than the others, but all of them are still within the acceptable range, and THD performance has not been sacrificed. Overall, switching frequency has been reduced with no detriment to MMC waveform quality.

Table 7-II Comparison of all proposed approaches.

Voltage Balancing Technique	Average Switching Frequency (Hz)	Capacitor Voltage Ripple (%)	THD of Voltage (%)	THD of Current (%)
CSA	2521.	0.83%	36.39	26.18
ISA	322	0.95%	37.31	25.38
Heap Sorting	1730	1.04%	37.23	25.38
HSA	312	1.14%	34.82	25.38
PSA	251	1.63%	37.44	29.37

7.8 Chapter Summary

This chapter first introduced the configuration and construction of the experimented platform. The functions and parameters of each board and components are explained precisely. The platform of the single-phase 4-level MMC was developed based on a TMS320F28335 floating-point microcontroller. The real-time processing was also described in addition to explaining how it communicates with the implemented hardware. Comparison tests of the conventional sorting algorithm and all three proposed techniques were conducted in terms of switching frequency reduction and output performance. The results verified the function and potential of the proposed techniques.

It is worth noting that the PWM channel of the TMS320F28335 DSP is sufficient for a single-phase MMC with a low number of SMs. The selected DSP is suitable for managing the voltage balancing algorithm and requires minimal execution time. However, this design may not be appropriate for the 3-phase MMC or with high numbers of SMs so that more PWM channels are required. Therefore, extra case should be taken when two or more processors are implemented to deal with the high numbers of SMs, including in the synchronisation and communication between processors. The Field Programmable Gate Arrays (FPGA) is considered to be an attractive solution due to its good I/O pin setting characteristic. In addition, a new generation of DSPs, for example the TMS320F28377 which has 24 PWM channels, is another potential choices [115].

Chapter 8. Condition Monitoring of SM Capacitors Enabled by the Proposed Voltage Balancing Scheme

8.1 Introduction

Considering the fact of the modularity structure of MMC sub-module (MMC), the output level is becoming easily manageable. However, due to the different conditions of each SM capacitors, the SM voltage is not identical or even has a huge difference when the SM is switched on, thus the ripple of the staircase waveform is no longer negligible. Therefore, a health monitoring method or fault-detection scheme is highly required to maintain the operation of the MMC converters which is one big challenge of this area.

This chapter presents an application of the proposed voltage balancing scheme which estimate the capacitance and equivalent series resistance (ESR) of the SM capacitor. The fast-affine projection (FAP) algorithm is cooperatively embedded in the PSA scheme to estimate the capacitor parameters. The proposed sorting optimisation not only reduces the switching events of SMs, but also manages to maintain the capacitor ripple voltage within an acceptable range. Whilst the use of FAP achieves an on-line parametric estimation with superior speed and accuracy. Compared to previous studies, this proposed approach has evident advantages in terms of estimation accuracy and speed without the need for extra hardware.

8.2 Condition Monitoring

Condition monitoring is to measure and estimate the health condition of a component [60]. Most condition monitoring methods are applying the ESR and C as the indicators to reveal the degradation condition of the capacitors. The end-of-life criterion is needed, then compare the estimated value with the degradation curve under specific operation conditions (obtained from test data) to evaluate the condition of the capacitor.

In terms of MMC, the faulty SMs will cause others to withstand increased stresses due to

the series connection of sub-modules in each arm, which may lead to serious problem to the system. In recent years, most papers are focusing on the conditions of semiconductors [57, 75], which predict the voltage or current of next step and compare them with the measured value, then evaluate the conditions of the semiconductors based on the specific criterion. Meanwhile, in [80], the mechanism of redundancy control is introduced after detecting the faulty sub-modules. Despite the capacitor failures are very essential for fault diagnosis, very rare papers have discussed it.

The C and ESR are the main indicators of health condition, by comparing the estimated value with the end-of-life criteria, the degradation level of the capacitor can be revealed. Because when the C and ESR reach a specific value, the degradation rate may become unacceptable fast and the capacitor may not function appropriately[69].

8.3 Associated Challenges

Figure 8.1 illustrates the typical voltage waveform across the SM capacitors. During the OFF-STATEs of SMs, the SMs are bypassed and blocked from the main circuits, and during which time there exist some leakage current which is very difficult to detect. Therefore, for the next ON-STATE period, the estimation algorithm will initialize again without before the results come out. Therefore, it is easier to describe the relationship between voltage and current during ON-STATE.

Also, the ON-STATE period is based on the gate signal is not long enough. For a general adaptive filter, 200 sampling points is normally the minimum required points, due to the limitation of DSP with 100 kHz, the minimum required period is 2ms which results in the disturbance of the capacitor voltage.

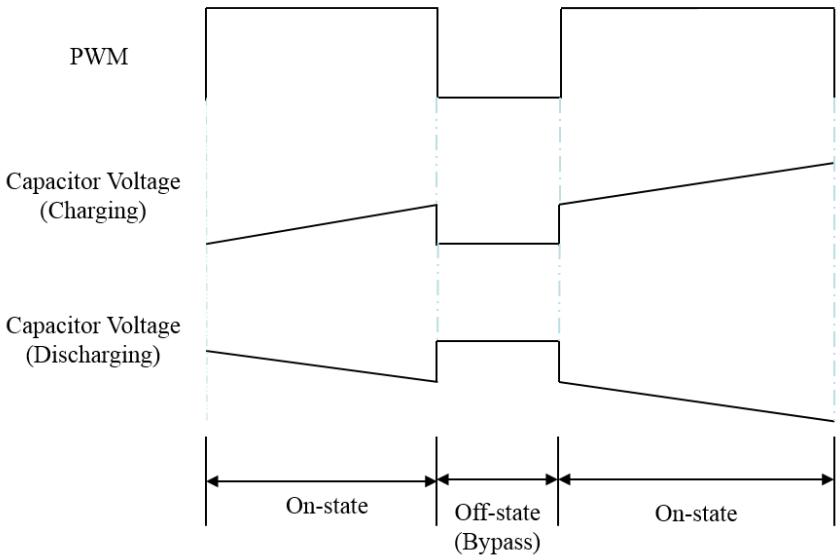


Figure 8.1 Charging/discharging process of one SM.

8.4 Combination of Condition Monitoring and PSA.

For the MMC system with a carrier frequency of 1 kHz to 2.5 kHz. The average ON-STATEs period is less than 2ms. With 20 kHz sampling frequency, normally 40 samples can be collected during one the ON-STATEs period, which is insufficient for further condition monitoring, the condition monitoring method should either have fast convergence speed or less impact on the system operation. Although this can be realized by combining two consecutive ON-STATEs period for parametric estimation, with the effect of leakage current, the accuracy of this method is not reliable. Therefore, this paper proposes an optimised control scheme for condition monitoring. It identifies a longer ON-STATEs period for acquiring and processing data samples, at the same time, having a minimum impact on the system operation. Figure 8.2 shows the proposed PSA scheme combining the estimation approach, this can be described as follows:

1. Define the range of voltage ripple **X**, then prioritize all the n SMs. Count the number m SMs that do not belong to ***C3*** and ***C4***.

2. Identify the available estimation period (AEP) from the lowest SMs Priorities.

3. Trigger the ON-STATE period by comparing the voltage of selected SM with either the upper or lower limit of **X**, depending on the direction of arm current.

4. Collect voltage and current samples during ON-STATE period, implement the estimation algorithm.

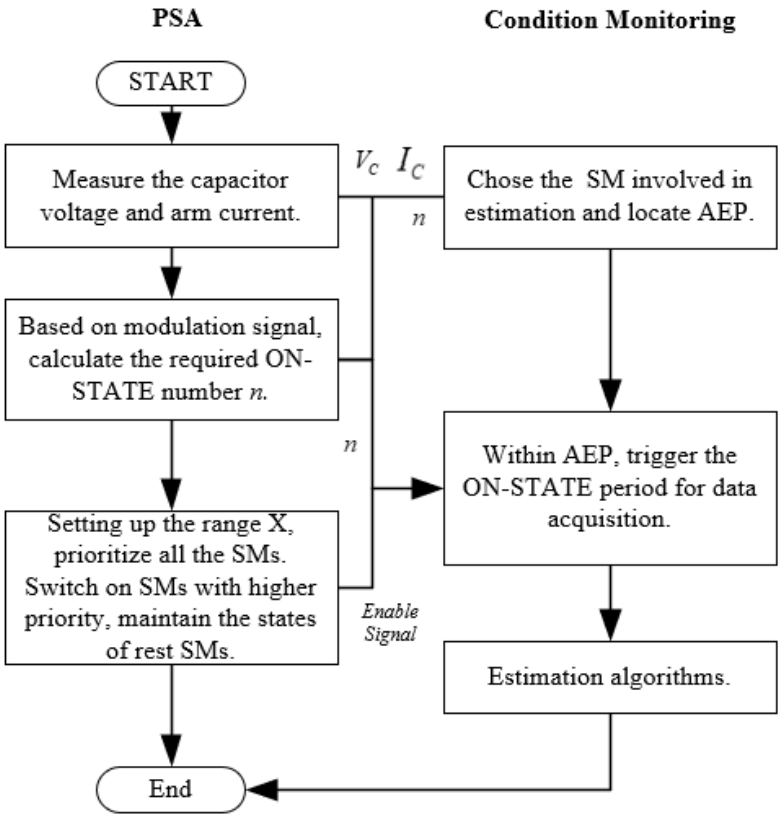


Figure 8.2 Proposed optimised sorting scheme combing the estimation approach.

Instead of accomplishing an identical SM voltage level in the conventional sorting algorithm that brings in unnecessary switching actions, the proposed sorting optimisation operates the capacitor voltage within an acceptable range. The reduced switching frequency is greatly compatible with condition monitoring. Most importantly, the PSA is range-based which helps to secure the ON-STATE period in AEP without sacrificing the output performance. It is worth noting that condition monitoring requires a large set of samples, whereas the ON-STATE period is normally insufficient for most on-line estimation methods. Even with the proposed soring optimisation, an algorithm with fast convergence speed and high accuracy is required to achieve the best performance.

8.5 Condition Monitoring Using Fast Affine Projection

A simplified model of SM capacitor is shown in Figure 8.3 which consists of an inner capacitor and an equivalent series resistor. The voltage across the capacitor V_c is given as:

$$R_{ESR} \cdot S_x \cdot i_{arm} + V_{cap} = V_c \tag{8.1}$$

where V_{cap} is the instantaneous voltage value of the inner capacitor which varies due to the charging and discharging process of the SM capacitor. With considering the switching states of SM in Equation 8.1, the relationship between the inner capacitor voltage and arm current is revealed as:

$$V_{cap} = \int \frac{S_x i_{arm}}{C} \tag{8.2}$$

From Equation 8.1 and 8.2, the capacitor equivalent circuit can be derived into a first-order differential Equation 8.3, and its parameters can be estimated from the current and voltage at certain switching states.

$$\frac{R_{ESR}\, S_x\, di_{arm}}{dt} + \frac{S_x i_{arm}}{C} = \frac{dV_c}{dt} \tag{8.3}$$

Rather than interrupting the system operation using off-line methods [78, 116], this model is suitable for employing adaptive filter algorithms as they provide on-line parameter estimation. The capacitance C and resistance R_{ESR} can be identified by the current and voltage measurements which are readily available in the controller. With a sample time of T_s, the capacitor model Equation 8.3 in Figure 8.3 can be digitalised using zero-order holder:

$$Gz = \frac{R_{ESR} \cdot z + (\frac{T_s}{C} - R_{ESR})}{z-1} \tag{8.4}$$

Corresponding to Equation 8.4, the target sub-module can be structured as a general discrete transfer function:

$$G(z) = \frac{bz+p}{z+a} = \frac{b+pz^{-1}}{1+az^{-1}} \tag{8.5}$$

a, b and p are the transfer function coefficients. Mapping Equation 8.5 to 8.4, yield:

$$a = -1, b = R_{ESR}, p = \frac{T_s}{C} - R_{ESR} \tag{8.6}$$

where b and p are the coefficients to be estimated. The capacitance and ESR can then be obtained from the estimated coefficients.

Among adaptive algorithms, the fast-affine projection (FAP) has superior convergence speed and good estimation accuracy in the applications of parametric estimation. It uses the previous step calculation result in the current iteration to reduce the computational cost, thus providing a better convergence speed [117].

The way of implementing FAP algorithm for parametric estimation can be generally summarized as:

1. Determine the system structure (e.g. system order)
2. Determine the size of the regressor and algorithm step size.
3. Start the estimation process, update the regressor matrices and the weight vector.
4. Repeat the iteration until the error is minimum, achieve an optimal set of transfer function coefficients.
5. Identify system parameters from estimated coefficients.

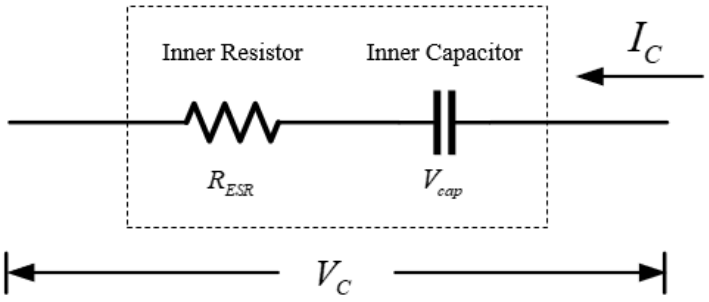


Figure 8.3 One simplified capacitor model.

Compared with Recursive Least Square (RLS) algorithm and Least Mean Square (LMS) algorithm, the FAP has the fastest convergence speed and computational cost is lower than RLS.

Even though LMS has the lowest computational cost, the accuracy and speed make it a non-cost-effective algorithm. The RLS has similar accuracy with FAP but the speed is slower than it which makes FAP very attractive for the fast speed required environment such as online system identification.

8.6 Simulation Results

An MMC model is developed in MATLAB to verify the performance of the proposed scheme. The model is supplied from a 6 kV DC source voltage with 4 SMs each arm, forming a 5-level voltage output. The modulation signals are obtained with the use of phase-shift pulse width modulation (PSPWM). The capacitor voltage and current are measured at a sampling frequency of 20 kHz. The real ESR and capacitance are set to 0.4 Ω and 2000.0μF respectively.

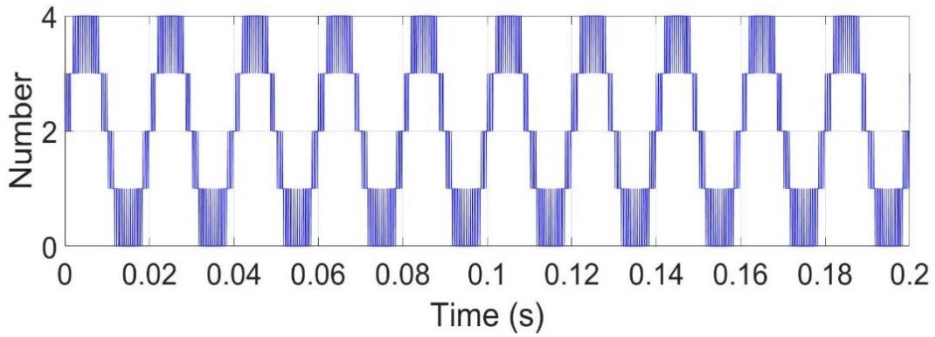


Figure 8.4 The required number of switched-on SMs for one arm based on PSPWM.

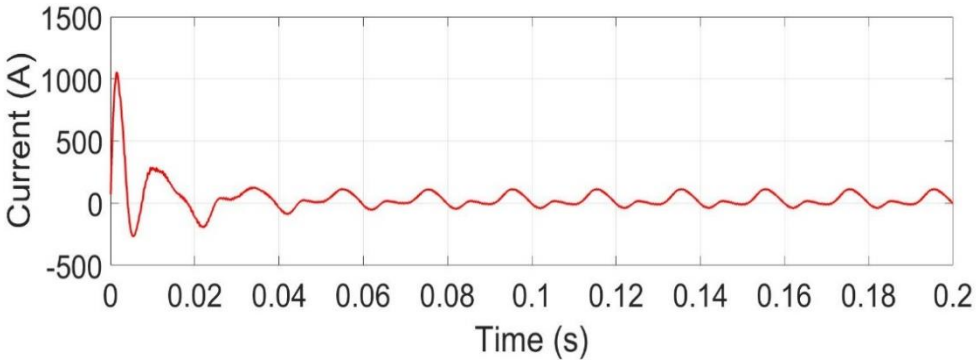


Figure 8.5 Upper arm current.

Figure 8.4 shows the variations of the required number n within 10 cycles. The fundamental frequency is 50 Hz and the AEP appear from 240 degrees to 300 degrees. Figure 8.5 is the arm current of the upper arm, with the impact of dc component within the arm current,

the average current is positive. During the AEP, in this case, the arm current is negative which means discharging the capacitors.

The PSA contains the upper and lower limit of X, where the SM located inside X has less possibility to change its switching states. In this simulation, when the current is positive and the required number is at the lower period between 0.075s to 0.080s, the trigger point is 0.078s when the SM1's voltage reaches the upper limit. Then for the next 25 sampling points, the switching state of SM1 is kept at ON-STATE. From the results in Figure 8.6, the voltage selected estimation SM has small oscillation but kept inside the X so the negative impact to the system is negligible.

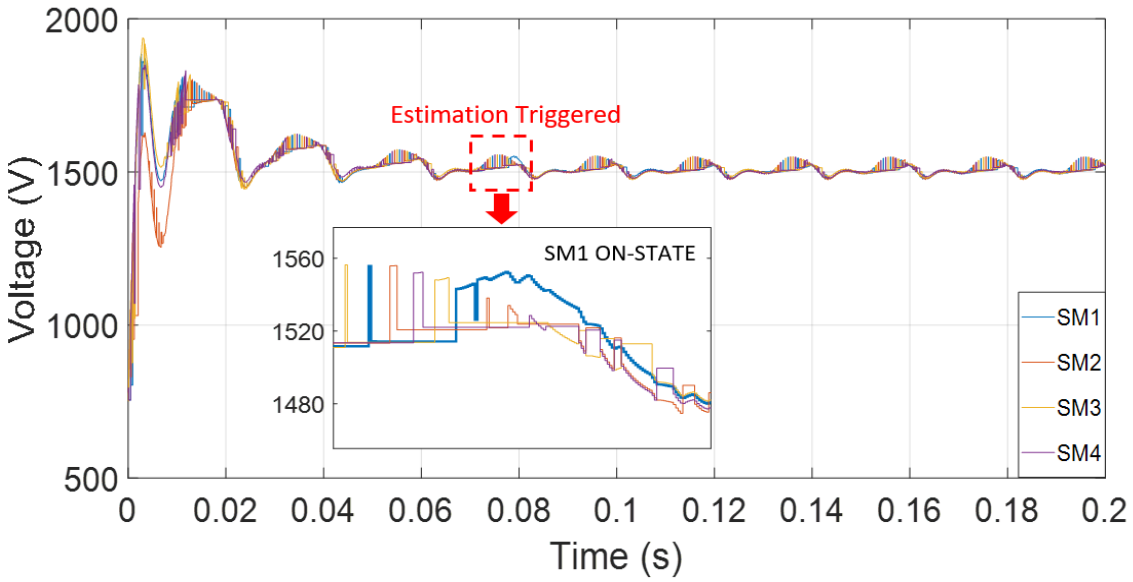


Figure 8.6 Capacitor voltage with implementation of proposed approach.

Figure 8.7 shows the effectiveness of FAP. In this case, the FAP used 20 to 25 point to get the estimated parameter of two coefficient *b* and *p*, the whole estimation time is less than 1.5ms. According to Figure 8.7, the value of coefficient *b* and *p* are 0.4125 and -0.3875 respectively. Then, compare the value of the estimated coefficient with the real value, the coefficient error of *b* is 3.13% and error of *p* 3.33%.

Based on Equation 8.5, the ESR and capacitance of SM capacitor are identified from the estimated coefficients, which are 0.4125 Ω and 2000.0 μF as shown in Figure 8.8. According to the figure, compared to the real value in 0.4 Ω and 2000.0μF, the error of them is 3.3% and

less than 0.01% accordingly.

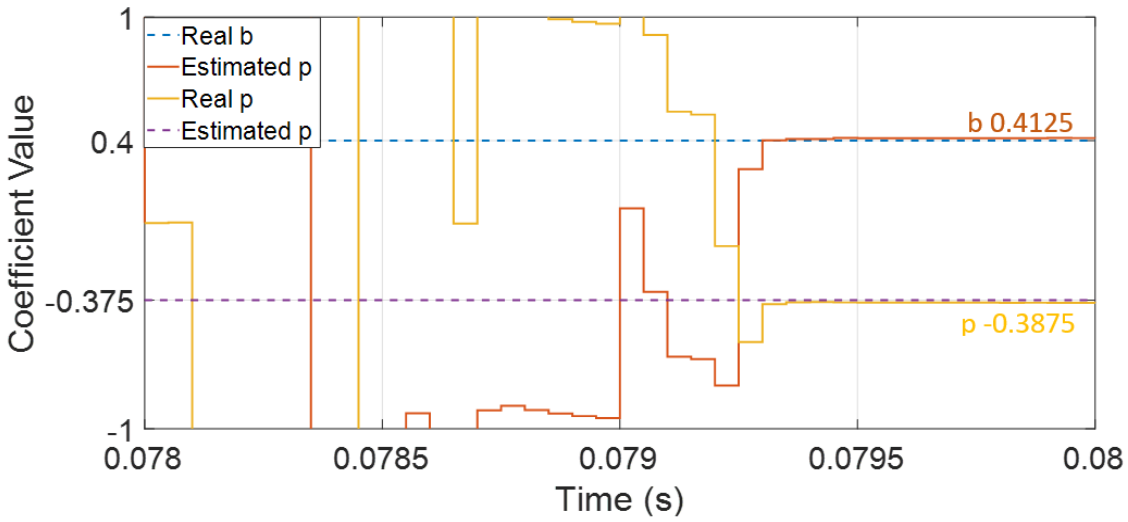


Figure 8.7 Coefficient estimation process.

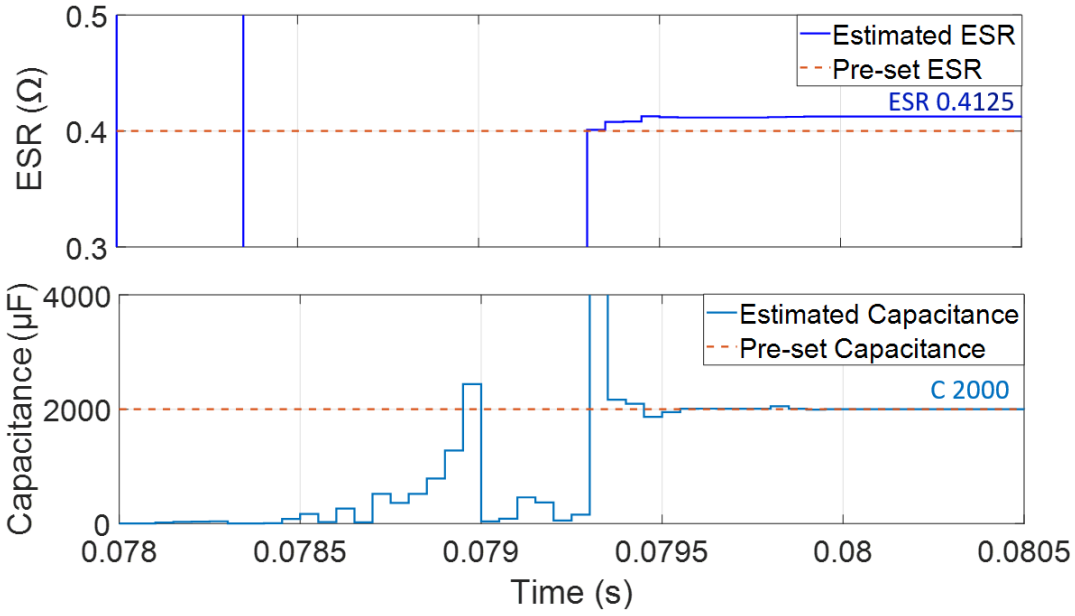


Figure 8.8 Condition monitoring of SM capacitor (ESR and C).

Therefore, the PSA proposed in this thesis is suitable for the FAP implementation. First, it has lower switching frequency than normal sorting algorithm. Second and the most important, the ON-STATE period is enough and predictable. Due to the content of Chapter 6, once the SM has highest priority, for the next couple of sampling point, it will go to the reference range and becomes reluctant to change its switching states.

8.7 Comparison with Other Condition Monitoring Methods

This thesis introduces the FAP algorithm but cannot be applied to the MMC system directly. One way to apply it for capacitance and ESR monitoring is by injecting a noisy signal to the reference waveform and by detecting the disturbance on the MMC output waveform[61]. This method is effective but requires extra signal injection and the disturbance is not controllable which may harmful to the system operation.

Table 8-I summarizes a comprehensive overview of different capacitor monitoring approaches. In comparison with the other approaches, the proposed approach has huge improvement (90%) in accuracy and response time as it requires the least sampling period to achieve the highest accuracy. Meanwhile, it requires no extra hardware or signal injection which can distort the system operation. In addition, the proposed approach can also estimate the ESR of the capacitor which can be another critical indicator to describe the capacitor's health.

Table 8-I Comparisons with the existing estimation methods.

Approaches	Calculation Time	Estimate Error of C	Extra Requirement
Signal injection with RLS[61]	15ms	1.3%	Extra source and filters.
Capacitance estimation with Kalman-filter[118]	400ms	2.0%	No
Calculated ripple-based impedance [119]	100ms	3.5%	Extra Band-pass filter
Proposed improved sorting with FAP	1.5ms	0.01%	No

8.8 Chapter Summary

This chapter presents a non-invasive online condition monitor scheme for SM capacitors in MMC application by utilising FAP with PSA. Compared with the other condition monitoring approaches, the proposed method not only performs evident advantages in terms of estimation

accuracy and speed, but also maintain the system performance with reduced the switching events of SMs. The estimation process is calculated by FAP, which helps to increase the estimation speed. From the simulation results, the convergence speed is less than 1.5ms and the estimation error is less than 3%. Due to its online characteristics, the proposed approach can be cooperatively implemented with redundancy management or be utilised for monitoring the switching devices.

Chapter 9.Conclusion and Future Work

9.1 Conclusion

This thesis presents three voltage capacitor balancing methods to improve the sorting algorithm used for MMCs. The CSA is an effective voltage balancing algorithm which essentially controls the gate signal directly after the modulation stage. The CSA is optimised mainly in terms of two aspects in this thesis, which are to reduce the frequency of unnecessary switching and to decrease the computational complexity of the process. Additionally, all the proposed approaches achieve the objectives without compromising the waveform quality of the output voltage and ripple performance.

The first approach is called the ISA which focuses on minimising the involvement SMs during the sorting process by introducing a tolerance band. This provides three different index options for the gate signals of SMs. Then, the algorithm selects the optimum index based on the prevailing conditions. This approach allows the SMs within the tolerance band to maintain their switching states to so as to decrease the total number of switching events and to help SMs outside the band to converge to the band rapidly. However, there is no significant change in the sorting mechanism from the CSA, so the reduction of computational complexity is very limited.

The second approach concerns the sorting algorithm itself. The heap sorting is closely compatible with MMC voltage balancing control, and has the potential to replace the conventional bubble soring algorithm. The adjusted heap tree structure helps to reduce the computational complexity of the algorithm, and the performance in switching frequency reduction is improved by combining it with other methods. It has been proven to be an efficient and effective algorithm for MMCs.

The third strategy is a comprehensive design based on the group concept from the HSA and range-based control from the ISA. The proposed algorithm applies the tolerance range and gate signals of the last sampling period as the main conditions used to classify the SMs into

several groups, and then determines priority among them according to the direction of the arm current. This algorithm minimises the CT during every sampling period because the sorting and comparison process only takes place inside the highest priority groups. This method can reduce both switching frequency and computational complexity at the minimum cost of increased circulating current. Also, it can alter the tolerance range to change the switching frequency, which makes it a flexible algorithm.

Moreover, the condition monitoring of SM capacitors is introduced, where the proposed PSA helps to enable the FAP to estimate the parameters of the capacitor. This is a fast and accurate scheme where the error of accuracy is less than 3% and estimation time is less than 1.5ms. All of the techniques proposed in this thesis can easily be combined with other methods in order to achieve further improvements. The research has achieved the main objectives as established in Chapter.1.

9.2 Summary of Contributions

The main contributions achieved in this these are as follows:

1. A comprehensive literature review is presented of the latest research into the voltage balancing of MMCs,
2. The conventional bubble sorting algorithm is deeply investigated, and particularly the reasons are evaluated for its production of unnecessary switching events.
3. Three new voltage balancing techniques for MMCs are proposed which significantly reduce the switching frequency and computational complexity compared to CSA.
4. Directions concerning how to further optimise the sorting algorithms by combing them with other strategies are suggested.
5. An online SM capacitance and ESR estimation scheme is introduced which is enabled by the ON-STATE period produced by PSA.

9.3 Future Work

The following points are recommended for future work:

1. The ISA could be combined with further optimised methods to provide more index choices. Then the ISA could be applied to MMCs with high numbers of SMs.

2. The heap sorting algorithm could be implemented for MMC with high number of SMs (Greater than 400). The complexity of heap tree construction and the heapification process cannot be disregarded. How to further reduce the computational cost of heapification and the construction of the absolute heap tree are problematic issues. Resolving them would be the key to successfully applying the heap sorting algorithm to MMCs with many SMs.

3. The improvement of further suppress the circulating current for PSA would be greatly recommended since the variation voltage of PSA has increased unbalanced current inside the arm, so extra controller for the circulating current should be taken into consideration.

4. The test of the robustness of online SM estimation should be improved so that it could be used to monitor the condition of IGBTs. The method could be verified through practical experimentation.

5. The effectiveness of the proposed methods requires further experimental validation on a test rig at a higher voltage level is highly recommended for future research.

Appendix

Derivation FAP algorithm

The cost function of optimal weight vector ω_0 solves

$$\min_{\omega} E|d - \mu\omega|^2 \tag{A.1}$$

where ω is the weight vector E is the expectation, d is the desired regressor and μ is the step size. This equation expresses the cost function of the error signal.

The fast affine projection is derived from the stochastic-gradient algorithm recursion as[120]:

$$\omega_i = \omega_{i-1} + \mu[R_{du} - R_u\omega_{i-1}] \tag{A.2}$$

where ω_i is the $M \times 1$ weight vector with iteration number i, $[R_{du}]$and $[R_u]$ are the regression matrices which represent cross-covariance vector and covariance matrix respectively which contains the information of input and output data, normally different algorithm has different expression to form these matrices. By regularized Newton's recursion, the equation is developed to:

$$\omega_i = \omega_{i-1} + \mu[\epsilon' I + R_u]^{-1}[R_{du} - R_u\omega_{i-1}] \tag{A.3}$$

where ϵ' is a fixed regularisation parameter. In this algorithm, a specific positive integer K is applied $(K \leq M)$ and replace the estimated cross-covariance vector and covariance matrix $[\widehat{R_{du}}]$and $[\widehat{R_u}\}$ with the K most recent observations in the block data matrix form:

$$U_i = \begin{bmatrix} u_i \\ u_{i-1} \\ . \\ . \\ . \\ u_{i-K+1} \end{bmatrix} (K \times M) \tag{A.4}$$

$$d_i = \begin{bmatrix} d_i \\ d_{i-1} \\ \cdot \\ \cdot \\ \cdot \\ d_{i-K+1} \end{bmatrix} (K \times 1) \tag{A.5}$$

The Newton's recursion becomes:

$$\omega_i = \omega_{i-1} + \mu[\epsilon' I + U_i^* U_i]^{-1} U_i^* [d_i - U_i \omega_{i-1}] \tag{A.6}$$

The way to implement the FAP to the parameter estimation can be generally summarized as following steps:

1. Determine system structure based on transfer function/difference equation of the system, select the step size μ.
2. Initialize the system parameters especially deciding the size of the matrices U_i d_i and E.
3. Start algorithm with iteration updated the U_i d_i and E.
4. Based on the weight vector repeat the iteration until the error reach minimum value.
5. Calculate the coefficient.

In FAP, the desired regressor is replaced by the history matrix contains both input and output signals.

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