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# Fully integrated transformer less floating gate driver for 3D power supply on chip

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**Abstract**— Power supply on chip (power SoC) has been caught attentions because it can ultimately miniaturize the power supplies. To realize 3D power SoC which is fabricated using mass production process, we need to meet the various electrical requirements. Series and/or parallel connections is mentioned as good method.

In such a situation, we previously proposed transformer less floating gate driver circuit using Schottky barrier diode (SBD). However, SBD is not suitable for integration. In this paper, we investigate the transformer less floating gate driver using MOS devices.

**Keywords**—3D power SoC, ISOP DC-DC converter, charge pump, integration

## I. INTRODUCTION

3D power SoC, which integrates power device, control and drive circuits, and passive devices, has been caught attention because it can ultimately miniaturize the power supplies [1,2]. In addition, 3D power SoC can realize high efficiency. It can also use mass production processes such as LSI and MEMS processes. Thus, we should develop various applications.

ISOP (Input Series Output Parallel) DC-DC can use lower breakdown power devices. Thus, it has been promising because it can realize high efficiency at high frequency switching [3]. In addition, ISOP topology can use general converter modules. This requires the gate driver with floating power supplies (floating gate driver circuits).

We usually use transformers as power supplies for floating gate driver circuits. However, transformers disturb miniaturization because this needs the winding of large volume. The trench capacitor using Si substrate has been actively studied and realized high density [4,5]. We previously reported the transformer less floating gate driver, which can operate 10 MHz,[6]. This circuit uses the external parts (Schottky barrier diode (SBD)) in bootstrap and charge pump circuit. However, it is hard to integrate SBDs using CMOS process. Approaches of using MOSFETs instead of SBDs have been proposed for charge pump circuit [7-9].

In this paper, we investigate the optimum circuit for the fully integrated transformer less floating gate driver for 3D power SoC.

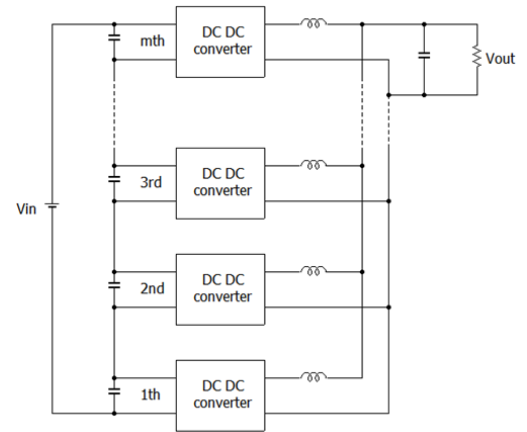


Fig.1 ISOP DC-DC converter

## II. TRANSFORMER LESS FLOATING GATE DRIVER

The previously proposed floating gate driver consists of level shifter, charge pump and buffer [6]. This ISOP converter consists of m stage and input voltage is  $V_{in}$ , so input voltage of a DC-DC converter is input voltage per stage ( $\frac{V_{in}}{m}$ ). When thinking about the ISOP converter of “n” th stage,  $V_{ss,L}$  ( $=\frac{V_{in}}{m}(n-1)$ ) is source voltage of low side switch,  $V_{ss,H}$  ( $=\frac{V_{in}}{m}n$ ) is input voltage of “n” th stage and  $V_{LX}$  is input voltage of inductor. In short, effective input voltage is  $V_{ss,H} - V_{ss,L}$ . When describing about operation principle of this circuit, input pulse is  $0 - V_{dd}$  and voltage drop of SBD is ignored.

First, describing about low side switch. The source voltage of low side switch ( $V_{ss,L}$ ) boosted to  $V_{ss,L} + V_{dd}$  using input pulse ( $V_{p,L} = 0 - V_{dd}$ ) and charge pump circuit, so the power supply voltage of low side driver is  $V_{ss,L} + V_{dd}$ . Input pulse for gate drive circuit ( $V_{p,L} = 0 - V_{dd}$ ) becomes  $V_{ss,L} - “V_{ss,L} + V_{dd}”$  because the pulse is boosted by bootstrap circuit. This circuit consists of a capacitor and a Schottky barrier diode. The current of the low side pulse is amplified by low side driver, so the pulse amplified the current is  $V_{g,L}$ . Finally, the signal of  $V_{ss,L} - “V_{ss,L} + V_{dd}”$  is inputted gate of low side MOSFET

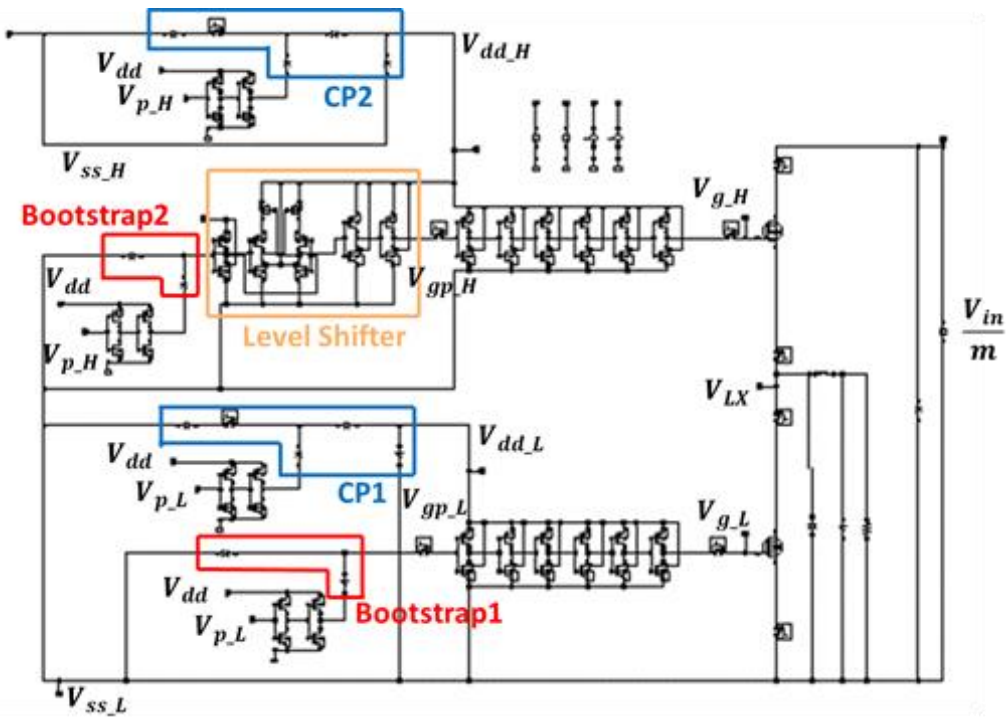


Fig.2 Transformer less floating gate driver

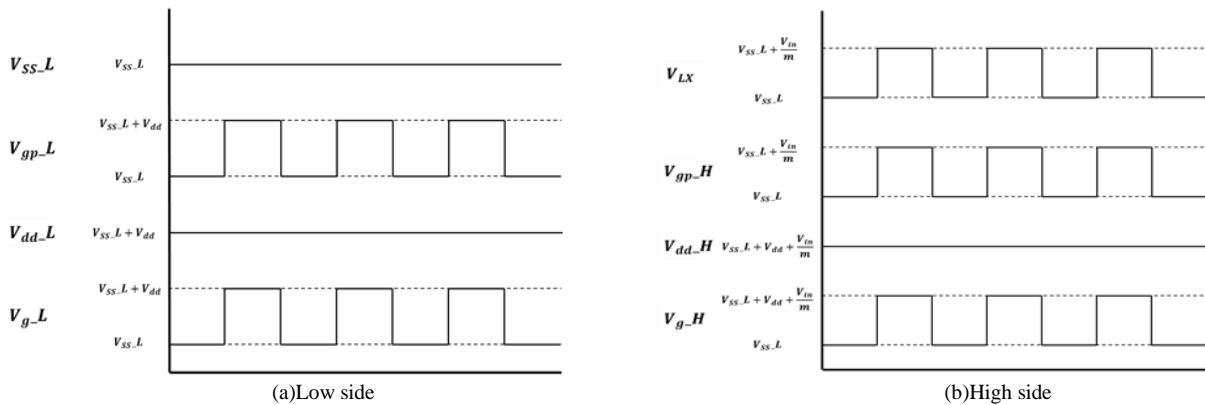


Fig.3 Timing chart

Second, describing about high side switch. The source voltage of high side switch ( $V_{ss,H}$ ) boosted to  $V_{ss,H} + V_{dd}$  using input pulse ( $V_{p,H} = 0 - V_{dd}$ ) and charge pump circuit, so the power supply voltage of high side driver is  $V_{ss,H} + V_{dd}$ . Difference between  $V_{p,L}$  and  $V_{p,H}$  is phase inversion. Input pulse for gate drive circuit ( $V_{p,H}$ ) becomes  $V_{ss,L} - "V_{ss,L} + V_{dd} + \frac{V_{in}}{m}"$  because the pulse of is boosted by bootstrap circuit and level shifter. The current of the high side pulse is amplified by high side driver, so the pulse amplified the current is  $V_{g,H}$ . Finally, the signal of  $V_{ss,L} - "V_{ss,L} + V_{dd} + \frac{V_{in}}{m}"$  is inputted gate of high side MOSFET.

In this study, we assume the 3D stacking structure shown in Fig. 4 taking into the consideration of removal of the heat and minimizing the wiring impedance. GaN power devices, which generate the most heat, should be placed bottom [10]. A driver chip should be put on the GaN power devices to minimize the wiring impedance.

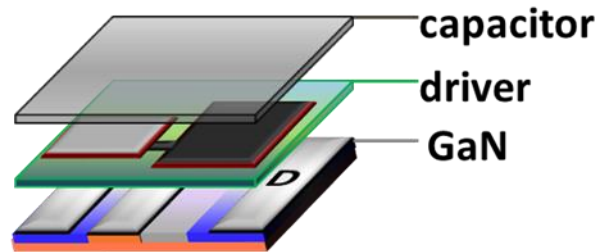


Fig.4 Stacking of GaN, driver and capacitor

### III. CIRCUIT INTEGRATION

One of the most famous charge pumps consist of two capacitors and two switches. Generally, SBD is used as switches. However, SBD is difficult to integrate when we use CMOS process. In this situation, there are two methods to integrate part of charge pump.

First, using MOSFET as diode connected transistor. When connected gate and drain in MOSFET, drain-source voltage ( $V_{DS}$ ) is equal to gate-source voltage ( $V_{GS}$ ). Drain current flows in this circuit by  $V_{DS}$  exceeding threshold voltage of MOSFET ( $V_{TH}$ ). This operation is similar to diode, so we can use MOSFET as diode.

Second, using special charge pump. In this paper, we consider three charge pump circuits.

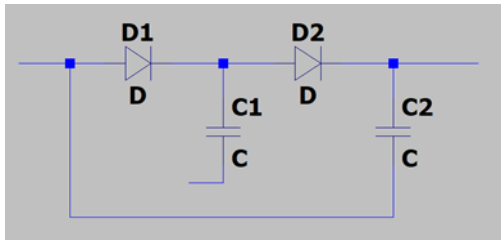


Fig.5 General charge pump

#### A. Dual-Branch charge pump

Dual-Branch charge pump [7] realizes lower ripple and transfer intervals of  $T/2$ . Also advantages of these structures are  $V_{DROP}$  reduction, higher switching frequencies and so on. However, this circuit is not suitable for low voltage operation and cold-start circuits.

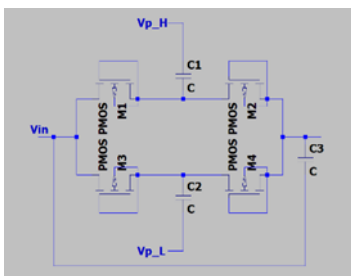


Fig.6 Dual-Branch charge pump [7]

#### B. Cross-coupled charge pump

Cross-coupled charge pump has dual compensated structures which is similar to dual-branch structures [8]. This charge pump realizes high efficiency (89%), fast pump speed (0.1ms), high capacitive drivability, charge transferability. However, like dual-branch, this is not suitable for low voltage operation (minimum start-up voltage is 320mV).

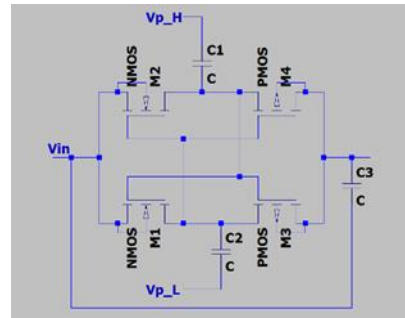


Fig.7 Cross-coupled [8]

#### C. Adiabatic charge pump

Adiabatic charge pump uses adiabatic switching to lower power consumption [9]. This circuit can recycle energy by rerouting charge transfer path back to the load. This operation is realized high efficiency because of reducing power consumption.

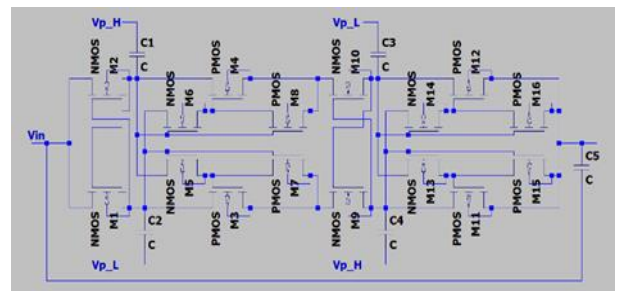


Fig.8 Adiabatic charge pump [9]

#### IV. SIMULATION RESULTS

We simulated the transformer less floating gate driver by using circuit simulation[11]. All circuit parameters are listed in Table 1.

In Fig.2, bootstrap1 and bootstrap2 are adopted diode connected transistor. Figure.9 shows the voltage by bootstrap using diode and Fig.10 shows it using MOSFET. These figures show that bootstrap circuit operates without any trouble. As the reason not to use special bootstrap circuit, it is hard to adjust the timing.

Also Table 2 shows the simulation results of these circuits. From Figures.9-13 show the gate-source voltage of simulations of five circuit configurations.

According to figures about gate-source voltage, transformer less floating gate driver could operate even if using the diode. However Table 2 shows the some differences between these circuits.

The amplitude of output gate drive voltage of Cross-coupled charge pump is highest (3.5V). From the point of view of the current consumption, Adiabatic is the lowest (0.1961A). Also Adiabatic charge pump shows the highest efficiency (95.74%) when the circuit used in buck converter.

Table 1 Circuit parameters

Input voltage $\frac{V_{in}}{m}$	5[V]
Input pulse $V_p$	0-4[V]
Power supply voltage $V_{dd}$	4[V]
Source voltage of low side switch $V_{ss\_L}$	10[V]
Switching frequency	10[MHz]
Duty ratio	46[%]
Level shift capacity	10[nF]

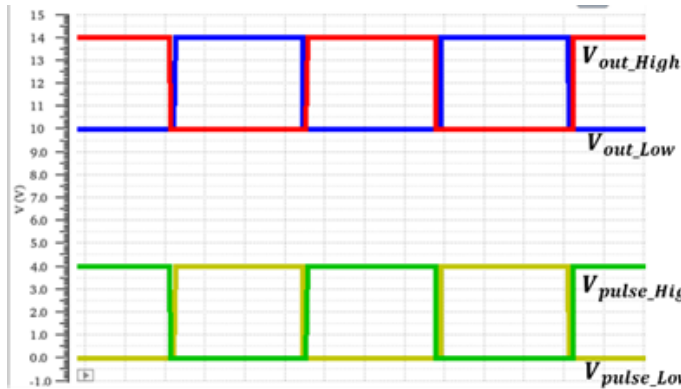


Fig.9 Pulse wave form using SBD based bootstrap

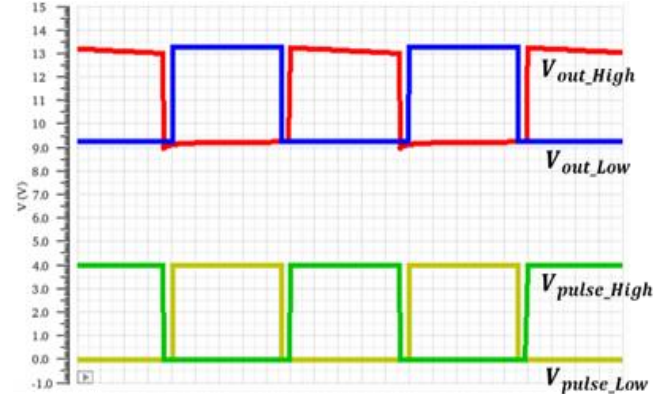


Fig.10 Pulse wave form using diode connection MOSFET based bootstrap

Table 2 Simulation results

	gate-source voltage[V]	current consumption[A]	quantity of MOSFET	efficiency[%]
Dual-Branch	2.55	0.70841866	4(all p-MOSFETs)	25.98087031
Cross-coupled	3.5	0.263435449	4(2 n-MOSFETs and 2 p-MOSFETs)	69.75143273
Adiabatic	2.88	0.196130286	16(8 n-MOSFETs and 8 p-MOSFETs)	95.74248008
diode	3.45	0.330211714	2 diodes	65.22058148
diode connected transistor	2.48	0.25904329	2 p-MOSFETs	73.5506409

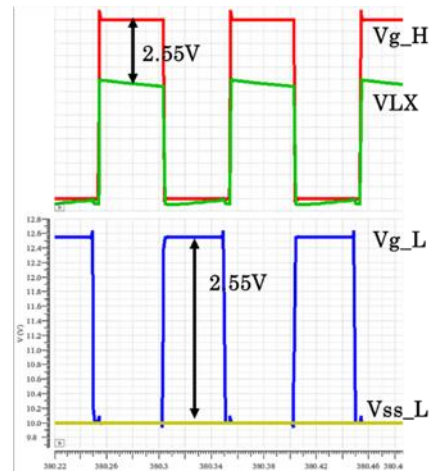


Fig.13 Gate-source voltage wave form of Dual-Branch

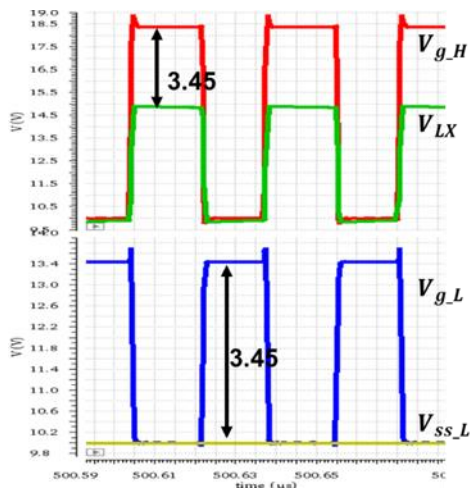


Fig.11 Gate-source voltage wave form of general charge pump

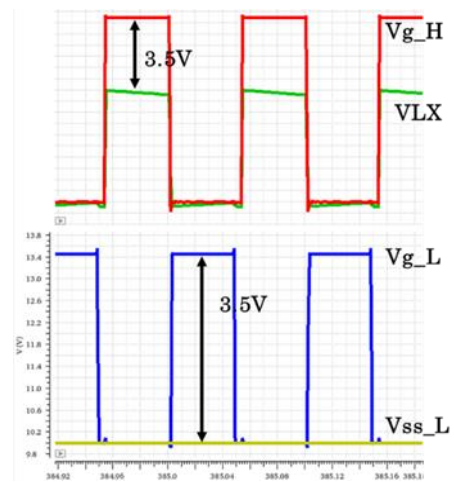


Fig.14 Gate-source voltage wave form of Cross-coupled

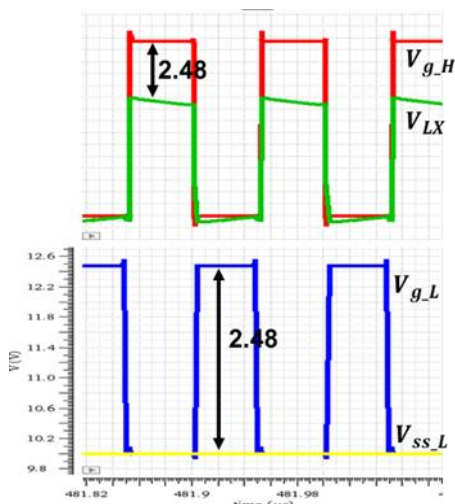


Fig.12 Gate-source voltage wave form of diode connected transistor

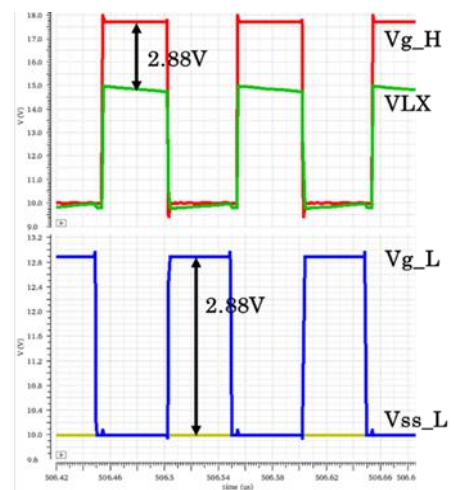


Fig.15 Gate-source voltage wave form of Adiabatic



## V. CONCLUSION

We investigate the suitable circuit configuration for fully integrated transformer less gate driver circuit. The simulation results show that Adiabatic is the best.

## ACKNOWLEDGEMENTS

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## REFERENCES

- [1] K. Hiura, Y. Ikeda, Y. Hino, and S. Matsumoto, "Impact of the 3D Stacking Power Supply on Chip for High Frequency DC-DC Converter", *Japanese Journal of Applied Physics*, 56, 04CR13, 2017.
- [2] K. Ono, K. Hiura and S. Matsumoto, "Design consideration of 3D stacked power supply on chip", 2018 IEEE ECTC, Session 27.7, 2018.
- [3] Y. Hayashi Y. Matsugaki, T. Ninomiya, S. Kose, and H. Tanoue, "Transformer less multicellular dc-dc converter for highly efficient next generation dc distribution system", *EPE'2017*, DOI:10.23919/EPE17ECCEurope.2017.8099166,
- [4] R. Pulugurtha, "Integration of pre-fabricated ultra-high density (1000 nF/cm<sup>2</sup>) capacitor films (50-70 microns) onto wafers and panels", 2016 Power Supply on Chip Workshop, Session 5.1, 2016.
- [5] F. Nodet, "Low profile integrated Silicon Capacitors Tailored for power supply on chip", 2018 Power Supply on Chip Workshop, Session 3.3, 2018.
- [6] M. Nakayama, S. Abe, and S. Matsumoto, "Transformer-less floating gate driver for 3D power SoC2", 2019 International 3D System Integration Conference, B4P-C 4055, 2019.
- [7] L.F. New, Z.A.B.A. Aziz and M.F. Leong, "A low ripple CMOS charge pump for low-voltage application", *Proceedings of 4th International Conference on Intelligent and Advanced Systems*, pp: 784-789, 2012.
- [8] Z. Luo, M-D. Ker, W-H. Cheng, and T-Y. Yen, "Regulated charge pump with new clocking scheme for smoothing the change current I low voltage CMOS process", *IEEE Trans. Circuits and systems-1*, vol.64, No.3, pp.528- 536, 2017.
- [9] C. Lauterbach, W. Weber, and D. Romer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps", *IEEE Journal of Solid-State Circuit*, Vol.35, No.5, pp.719-723, 2000.
- [10] A. Furue and S. Matsumoto, "Numerical investigation for 3D power supply on chip by coupling of thermal-fluid, circuit, and electromagnetic simulations", to be presented at 2021 International 3D System Integration Conference.
- [11] [https://www.cadence.com/content/dam/cadence-www/global/ja\\_JP/documents/tools/custom-ic-analog-rf-design/virtuoso-mmsim\\_ds\\_jp.pdf](https://www.cadence.com/content/dam/cadence-www/global/ja_JP/documents/tools/custom-ic-analog-rf-design/virtuoso-mmsim_ds_jp.pdf)