

Numerical study on the suppression of 4H-SiC PiN diodes forward bias degradation due to substrate basal plane dislocations

| | |
|------------------------------|---|
| 著者 | Torimi Satoshi, Obiyama Yoshiki, Tsukuda Masanori, Omura Ichiro |
| journal or publication title | Solid-State Electronics |
| volume | 166 |
| page range | 107770-1-107770-7 |
| year | 2020-02-05 |
| URL | http://hdl.handle.net/10228/00008713 |

doi: <https://doi.org/10.1016/j.sse.2020.107770>

Numerical Study on the suppression of 4H-SiC PiN diodes forward bias degradation due to substrate basal plane dislocations

Satoshi Torimi^{1,2}, Yoshiki Obiyama¹, Masanori Tsukuda¹ and Ichiro Omura¹

¹ Kyushu Institute of Technology

2-4 Hibikino, Wakamatsu-ku, Kitakyushu-shi, Fukuoka, 808-0196, Japan

Phone: +81-93-695-6037 E-mail: torimi.satoshi492@mail.kyutech.jp, omura@ele.kyutech.ac.jp

² Toyo Tanso, Co., Ltd

2181-2 Nakahime, Ohnohara-cho, Kanonji-shi, Kagawa, 769-1612, Japan

Phone: +81-875-54-2628

Abstract

We propose a calculation model of current density that causes forward bias degradation from substrate basal plane dislocations (BPDs) in 4H-SiC PiN diodes. The hole concentration above which substrate BPDs expand to single Shockley stacking faults (1SSFs) at the buffer/substrate interface was experimentally evaluated from forward-current stress tests of 4H-PiN diodes by comparison with our model results, resulting in $8.0 \times 10^{15} \text{ cm}^{-3}$. We confirmed the dependence of the current density on the dopant concentration and the hole lifetime in the buffer layer numerically. The model was extended to the case where BPD converted to threading edge dislocations (TEDs) in the substrate, and the relational expression between the depth of the BPD-TED conversion position in the substrate and the current density at which BPD expanded to 1SSF was obtained. The model suggested that it will be an effective technique for suppressing forward bias degradation by shorter lifetime and deeper BPD-TED conversion position in the substrate.

Keywords: 4H-SiC, PiN diode, forward bias degradation, carrier lifetime, BPD-TED conversion position

1. Introduction

SiC power devices are capable of a higher breakdown voltage and lower on-resistance than Si power devices because of their excellent properties, and this can reduce power conversion loss [1]. Forward bias degradation is an important reliability issue for SiC devices operating in bipolar mode. These devices include PiN diodes such as body diodes in metal oxide semiconductor field-effect transistors. Forward bias degradation is caused by basal plane dislocations (BPDs) in the SiC epitaxial wafer. The BPDs expand to single Shockley stacking faults (1SSFs) under forward bias operation in SiC bipolar devices. This results in an increase in on-voltage [2]. On the other hand, it has been reported that TEDREC (Temperature Degradation Reduction of Electrical Characteristics) phenomena improves on-state voltage degradation due to forward bias degradation at high temperature operation above 150 °C [3]. However, high temperature annealing at 550 °C is required to shrink the expanded 1SSFs [4], and it has been reported that some of 1SSFs lower the blocking voltage in the reverse bias mode [5]. It is important not to expand 1SSFs from BPDs for the substantial improvement of forward bias degradation.

BPDs in the SiC substrate can generally be converted to harmless threading edge dislocations (TEDs) at the epi/substrate interface via epitaxial growth technology, which can almost eliminate (> 95 %) BPDs in the epitaxial film [1,6]. However, it has been reported that 1SSF expansion occurs when excess carriers reach BPDs in the substrate under high current conditions [7].

Increasing the current density is unavoidable in miniaturization to exploit the performance of SiC power devices. It is therefore important to design device structures that suppress forward bias degradation.

Recent studies considered the mechanism by which BPDs in the substrate expand to 1SSFs. Tawara et al. extracted the critical hole concentration at which a BPD in the substrate expands to a 1SSF [8]. Hayashi et al. experimentally estimated the critical current density of 1SSF expansion corresponding to the depth of the BPD position in the substrate [9]. Several device structures to prevent injected holes from reaching BPDs in the substrate have been reported. Their designs have involved increasing the thickness of the buffer layer and increasing the dopant (N) impurity concentration [10], and shortening the lifetime in the buffer layer by co-doping of impurities such as B [11], Ti and V [12]. Various structural improvements have been proposed to suppress forward bias degradation. However, the improvement in current density that causes forward bias degradation owing to those structural parameters has not been sufficiently estimated numerically.

Here, we propose a calculation model for the critical current density (J_{crit}) that predicts forward bias degradation originating from 1SSFs expanded from BPDs in the substrate. We discuss the device structures and substrate characteristics for suppressing forward bias degradation.

The calculation model for the total current density (J) considered the temperature dependence in the PiN diode using the hole concentration at the bottom of the buffer

layer. J was then used to evaluate the critical current density that causes 1SSF expansion from BPDs converted to TEDs at the buffer/substrate interface. The critical hole concentration (p_{crit}) which made BPDs expand to 1SSFs was estimated using the model. The temperature and current density derived from high-temperature forward-current stress tests with PiN diodes were experimentally obtained. The improvement in J_{crit} by introducing the lifetime control parameter into the buffer layer was numerically investigated. J_{crit} was evaluated when the lifetime in the substrate was shortened and when the BPD-TED conversion position within the substrate was changed.

2. Experimental and calculation model

2.1 Calculation model for current density in the PiN diode

Fig. 1 shows a schematic of the cross-sectional structure of a typical SiC PiN diode. The distributions of hole concentration (p) and electron concentration (n) are set as shown in Fig. 2. The position coordinate system x in the drift, the buffer, and the substrate region sets the position of the interface on the anode electrode side to zero. We assume the one-dimensional forward current flow under the uniform doping concentration with position at each region, and we also assume the charge neutrality holds at steady state except the each junction,

$$p - n + N_D^+ = 0 \quad , \quad (1)$$

where N_D^+ is the ionized donor concentration. At each junction, the mass action law as shown equations (2) holds since the quasi-Fermi level on both sides is equal at the junction under the forward bias,

$$\begin{aligned} pn &= n_i \exp\left(\frac{E_i - E_{Fp}}{k_B T}\right) \times n_i \exp\left(\frac{E_{Fn} - E_i}{k_B T}\right) \\ &= n_i^2 \exp\left(\frac{E_{Fn} - E_{Fp}}{k_B T}\right) \quad , \end{aligned} \quad (2)$$

where n_i is the intrinsic carrier concentration, E_i is the Fermi level, E_{Fp} is the quasi-Fermi level for holes, E_{Fn} is the quasi-Fermi level for electrons, k_B is the Boltzmann constant and T is the absolute temperature. The electron current density J_n and the hole current density J_p at each region under the electric field intensity E are calculated by the following equations,

$$J_p = q\mu_p pE - qD_p \frac{dp}{dx} \quad , \quad (3)$$

$$J_n = q\mu_n nE + qD_n \frac{dn}{dx} \quad , \quad (4)$$

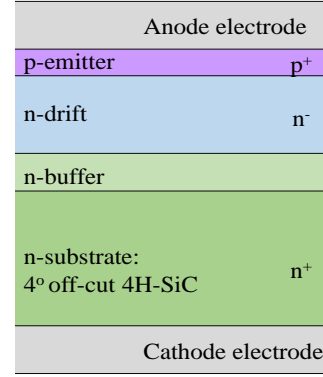


Fig. 1. Schematic of the cross-sectional structure of the SiC PiN diode.

where q , μ_p , μ_n , D_p and D_n are the elementary

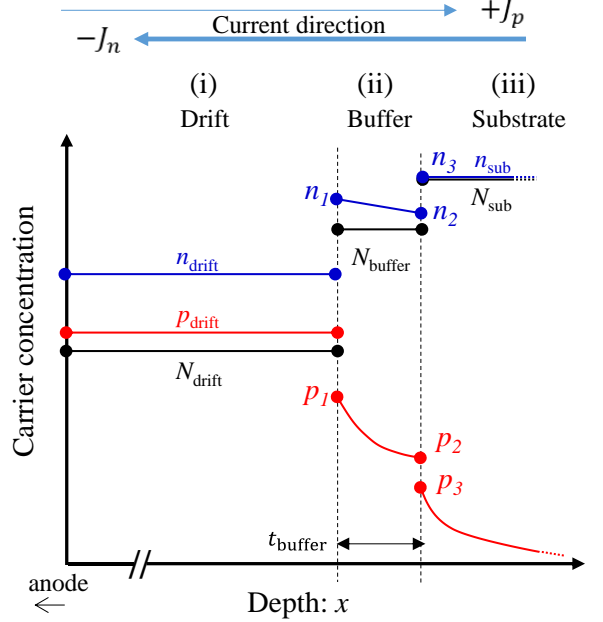


Fig. 2. Model of the carrier concentration distribution in the drift layer, buffer layer and substrate.

charge, the electron mobility, the hole mobility, the diffusion coefficient for electrons and for holes, respectively.

The detailed conditions of the hole concentration distribution at each region is explained as follows:

(i) Drift layer

In the drift region, the carrier distribution is assumed to be a flat profile. The distribution of the hole and electron concentrations can be expressed as constants p_{drift} and n_{drift} , respectively.

$$p(x) = p_{\text{drift}} \quad , \quad (5)$$

$$n(x) = n_{\text{drift}} \quad , \quad (6)$$

J is the sum of the electron current density $J_{n(\text{drift})}$ and the hole current density $J_{p(\text{drift})}$ in the drift layer. Each current density can be written by only the drift current component because of flat carrier profile ($dp/dx = dn/dx = 0$) using equations (3) and (4). J is expressed by the following equations using $J_{p(\text{drift})}$:

$$J_{p(\text{drift})} = q\mu_{p(\text{drift})}p_{\text{drift}}E \quad , \quad (7)$$

$$J_{n(\text{drift})} = q\mu_{n(\text{drift})}n_{\text{drift}}E \quad , \quad (8)$$

$$J = \left(1 + \frac{\mu_{n(\text{drift})}n_{\text{drift}}}{\mu_{p(\text{drift})}p_{\text{drift}}}\right)J_{p(\text{drift})} \quad , \quad (9)$$

where $\mu_{n(\text{drift})}$ and $\mu_{p(\text{drift})}$ are the mobility of electrons and holes in the drift layer, respectively.

(ii) Buffer layer

In the buffer region, the carrier distribution is assumed to obey the minority carrier diffusion equation [13] represented as:

$$D_{\text{buffer}} \frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_{\text{buffer}}} + \frac{\partial p(x,t)}{\partial t} + G \quad , \quad (10)$$

where D_{buffer} is the diffusion coefficient of holes, τ_{buffer} is the hole lifetime, and G is the generation rate due to light in the buffer layer. In this model $G = 0$ is set assuming in the dark condition. D_{buffer} can be calculated using the Einstein relationship as shown in equations (11),

$$D_{\text{buffer}} = \frac{k_B T}{q} \mu_{p(\text{buffer})} \quad , \quad (11)$$

where $\mu_{p(\text{buffer})}$ is the mobility of holes in the buffer layer. The function of the hole concentration at the steady-state can be expressed as shown in equations (12) corresponding to the solutions of equation (10),

$$p(x) = \frac{p_2 \sinh\left(\frac{x}{L_{\text{buffer}}}\right) + p_1 \sinh\left(\frac{t_{\text{buffer}} - x}{L_{\text{buffer}}}\right)}{\sinh\left(\frac{t_{\text{buffer}}}{L_{\text{buffer}}}\right)} \quad , \quad (12)$$

where t_{buffer} is the thickness of the buffer layer and L_{buffer} is the diffusion length in the buffer layer. L_{buffer} is calculated as shown equations (13),

$$L_{\text{buffer}} = \sqrt{D_{\text{buffer}}\tau_{\text{buffer}}} \quad . \quad (13)$$

τ_{buffer} is calculated using the exponential interpolation equation (14). The concentration dependence of the

minority carrier lifetime is considered using the value at room temperature and 523 K in ref. [10].

$$\tau_{\text{buffer}}(T[\text{K}]) = \left(\frac{T}{300}\right)^\alpha \tau_{\text{buffer}}(T=300\text{K}) \quad [\text{s}] \quad (14)$$

where $\tau_{\text{buffer}}(T=300\text{K})$ [s] is the hole lifetime at 300 K. In the dopant concentration range of 1.0×10^{16} to 1.0×10^{19} cm^{-3} , α is estimated to be 1.7 to 2.2 using the lifetime values calculated from the literature [10] at room temperature and 523 K.

Holes injected from the drift region diffuse into the buffer region and generate a diffusion current. The hole current density at the top of buffer region ($J_{p_buffer(x=0)}$) and at the bottom of buffer region ($J_{p_buffer(x=t_{\text{buffer}})}$) is given by:

$$\begin{aligned} J_{p_buffer(x=0)} &= -qD_{\text{buffer}} \left. \frac{dp}{dx} \right|_{x=0} \\ &= -qD_{\text{buffer}} \frac{p_2 - p_1 \cosh\left(\frac{t_{\text{buffer}}}{L_{\text{buffer}}}\right)}{L_{\text{buffer}} \sinh\left(\frac{t_{\text{buffer}}}{L_{\text{buffer}}}\right)} \quad , \quad (15) \end{aligned}$$

$$\begin{aligned} J_{p_buffer(x=t_{\text{buffer}})} &= -qD_{\text{buffer}} \left. \frac{dp}{dx} \right|_{x=t_{\text{buffer}}} \\ &= -qD_{\text{buffer}} \frac{p_2 \cosh\left(\frac{t_{\text{buffer}}}{L_{\text{buffer}}}\right) - p_1}{L_{\text{buffer}} \sinh\left(\frac{t_{\text{buffer}}}{L_{\text{buffer}}}\right)} \quad . \quad (16) \end{aligned}$$

Here, assuming that $E=0$ and the hole current density at each junction is equal from the continuity of the current, the following equation holds at the drift/buffer interface,

$$J_{p(\text{drift})} = J_{p_buffer(x=0)} \quad . \quad (17)$$

In addition, according to the mass action law considering the bandgap narrowing (BGN) effect described in Sect. 2.2, the following equation holds for the drift/buffer interface.

$$p_{\text{drift}}n_{\text{drift}} = p_1 n_1 \exp\left(\frac{\Delta E_{g(\text{buffer/drift})}}{k_B T}\right) \quad . \quad (18)$$

where $\Delta E_{g(\text{buffer/drift})}$ is the difference in band gap energy between the buffer and the drift region.

(iii) Substrate

In the substrate region, assuming that the substrate is sufficiently thicker than the hole diffusion length in the substrate L_{sub} , and assuming that the concentration of free electrons is sufficiently higher than the injected hole

concentration, then the hole concentration distribution is set to decay exponentially according to,

$$p(x) = p_3 \exp\left(-\frac{x}{L_{\text{sub}}}\right) \quad , \quad (19)$$

L_{sub} is calculated from equation (20) using the diffusion coefficient of holes in the substrate D_{sub} and the hole lifetime in the substrate τ_{sub} .

$$L_{\text{sub}} = \sqrt{D_{\text{sub}}\tau_{\text{sub}}} \quad . \quad (20)$$

Since typical τ_{sub} is reported to be less than 10 ns [14], we assumed $\tau_{\text{sub}}=1$ ns at room temperature and $\tau_{\text{sub}}=8$ ns at 498 K, and estimated the temperature change of τ_{sub} using equation (14). In this case, calculated α is 4.1. D_{sub} can be calculated using the mobility of holes $\mu_{p(\text{sub})}$ from the Einstein relationship as shown in equations (21),

$$D_{\text{sub}} = \frac{k_B T}{q} \mu_{p(\text{sub})} \quad . \quad (21)$$

The hole current density at the top of the substrate ($J_{p(\text{sub})}$) is expressed by the following equation same as in the buffer region,

$$J_{p(\text{sub})} = -qD_{\text{sub}} \left. \frac{dp}{dx} \right|_{x=0} = qD_{\text{sub}} \frac{p_3}{L_{\text{sub}}} \quad . \quad (22)$$

From the assumption of current continuity, the following equation holds for the buffer/substrate interface,

$$J_{p\text{-buffer}(x=t_{\text{buffer}})} = J_{p(\text{sub})} \quad . \quad (23)$$

The mass action law gives following equation for the buffer/substrate interface same as the drift/buffer interface.

$$p_2 n_2 = p_3 n_3 \exp\left(\frac{\Delta E_{g(\text{sub}/\text{buffer})}}{k_B T}\right) \quad . \quad (24)$$

where $\Delta E_{g(\text{sub}/\text{buffer})}$ is the difference in band gap energy between the substrate and the buffer region.

The total current density J in the PiN diode can be calculated from the continuity of hole current density and the mass action law at each interface. We assumed to expand ISSFs from BPDs when the hole concentration at the BPD position (p_{BPD}) is equal or more than p_{crit} . In this study we focused on BPDs converted to TEDs at the buffer/substrate interface, we calculated J_{crit} by giving the value of p_{crit} to p_2 in this model. In addition, we extended the model to the case where the BPD-TED conversion position was in the substrate, we also calculated J_{crit} by changing the BPD-TED conversion depth d . J_{crit} was calculated under the condition of Table.1 in the temperature range from 298 K to 498 K as a temperature dependence.

2.2 Physical models considering temperature dependence

We introduce physical models of the impurity ionization, the BGN effect and the mobility for 4H-SiC considering temperature dependence. For accurate ionized dopant concentration (N is typically used as the dopant for n-type) in the epitaxial layer and the substrate, the impurity ionization model for n-type is calculated using equation (25) [15],

$$N_D^+ = \frac{\gamma}{2} \left(\sqrt{1 + \frac{4N_D}{\gamma}} - 1 \right) \quad , \quad (25)$$

where N_D is the donor concentration before ionization. γ is expressed as shown in equation (26),

$$\gamma = \frac{N_C}{g_D} \exp\left(-\frac{E_C - E_D}{k_B T}\right) \quad , \quad (26)$$

Table 1 Condition of using parameter for J_{crit} calculation in the model.

| BPD –TED conversion position | Parameter | Range | Calculation result of J_{crit} |
|------------------------------|---|---|---|
| Buffer/substrate interface | Buffer doping concentration (N_{buffer}) | $1 \times 10^{16} - 1 \times 10^{19} \text{ cm}^{-3}$ | Fig. 6 |
| | τ_{buffer} | 0.1 – 1000 ns | Fig. 7 |
| | $t_{\text{buffer}}/L_{\text{buffer}}$ | 0.1 – 1 | Fig. 8 |
| | τ_{sub} | 0.1 – 1000 ns | Fig. 9 |
| In the substrate | d | 0 – 1 μm | Fig. 11 |

where N_C is the effective density of states in the conduction band, and g_D is the degeneracy factor (a g_D value of 2 is used for the donor). The ionization energy of $E_C - E_D$ for nitrogen is adopted as 0.061 eV for the hexagonal lattice sites. N_C is calculated from equation (27),

$$N_C = 2 \left(\frac{2\pi m_{de}^* k_B T}{h^2} \right)^{3/2}, \quad (27)$$

where h is the Planck constant and m_{de}^* is the density-of-states effective mass. m_{de}^* is used as 0.7 times the free electron mass m_0 . Since our model deals only with the hole concentration as minority carrier after injected into the drift layer, the activation of acceptor concentration is not discussed.

It is important to consider the BGN effect for carrier transport across each region in the PiN diode. This is because n_i changes due to the band edge displacement corresponding to the doping concentration of the epitaxial layer and the substrate. The band edge displacement ΔE_g is reported as shown in equation (28) using N_D^+ [cm^{-3}] [16],

$$\Delta E_g = 1.2 \times 10^{-2} \left(\frac{N_D^+}{10^{18}} \right)^{\frac{1}{2}} + 1.5 \times 10^{-2} \left(\frac{N_D^+}{10^{18}} \right)^{\frac{1}{3}} + 1.9 \times 10^{-2} \left(\frac{N_D^+}{10^{18}} \right)^{\frac{1}{4}} \quad [\times 10^{-3} \text{ eV}]. \quad (28)$$

n_i , considering the BGN effect, is expressed by equation (29),

$$n_i = \sqrt{N_C N_V} \exp \left(-\frac{E_g - \Delta E_g}{2k_B T} \right), \quad (29)$$

where N_V is the effective density of states in the valence band and E_g is the bandgap energy. $\Delta E_{g(\text{buffer/drift})}$ in equation (18) and $\Delta E_{g(\text{sub/buffer})}$ in equation (24) can be calculated using equation (28) and (29). $\Delta E_{g(\text{buffer/drift})}$ and $\Delta E_{g(\text{sub/buffer})}$ are expressed by equation (30) and (31),

$$\Delta E_{g(\text{buffer/drift})} = \Delta E_{g(\text{buffer})} - \Delta E_{g(\text{drift})}, \quad (30)$$

$$\Delta E_{g(\text{sub/buffer})} = \Delta E_{g(\text{sub})} - \Delta E_{g(\text{buffer})}, \quad (31)$$

where $\Delta E_{g(\text{drift})}$, $\Delta E_{g(\text{buffer})}$ and $\Delta E_{g(\text{sub})}$ are the band edge displacement in the drift, buffer and substrate region, respectively.

To calculate the mobility considering the temperature dependence and carrier concentration, the Caughey-Thomas mobility model [17] is used. The mobility is calculated from equations (32) and (33) using

T [K], N_D^+ [cm^{-3}] and the ionized acceptor concentration N_A^- [cm^{-3}],

$$\mu_n = \frac{1141 \left(\frac{T}{300} \right)^{-2.8}}{1 + \left(\frac{N_D^+ + N_A^-}{1.94 \times 10^{17}} \right)^{0.61}} \quad [\text{cm}^2/\text{Vs}], \quad (32)$$

$$\mu_p = \frac{124 \left(\frac{T}{300} \right)^{-2.8}}{1 + \left(\frac{N_D^+ + N_A^-}{1.76 \times 10^{19}} \right)^{0.34}} \quad [\text{cm}^2/\text{Vs}]. \quad (33)$$

$N_A^- = 0$ is used in the n-type epitaxial layer and substrate.

2.3 Forward-current stress tests of PiN diodes for p_{crit} estimation

1.5 mm-square PiN diodes were fabricated using a commercial 3-inch n-type 4H-SiC (0001) Si-face wafer with 4° off-cut towards the $[11\bar{2}0]$ direction ($5 \times 10^{18} \text{ cm}^{-3}$ of N-doping concentration). H_2 etching of 10 nm was carried out prior to the epitaxial growth. Epitaxial growth was performed using a buffer layer thickness of 0.5 μm and n-type carrier concentration of $1 \times 10^{18} \text{ cm}^{-3}$, and a drift layer thickness of 10 μm and concentration of $1 \times 10^{16} \text{ cm}^{-3}$. The p^+ anodes with a concentration of about $3 \times 10^{20} \text{ cm}^{-3}$ were formed by Al ion-implantation on the n-type epitaxial film with high temperature ($> 1600 \text{ }^\circ\text{C}$) activation annealing. Finally, the anode electrodes (Al) and cathode electrodes (Au) were formed on the implanted p^+ anode region and the back side of the wafer by the sputter deposition, respectively.

The position of BPDs propagated into epitaxial layer, not converted to TEDs were identified in advance by observing with photoluminescence (PL) imaging with 313 nm-wavelength excitation and a 650 nm long-pass filter for luminescence detection after epitaxial growth.

Forward-current stress tests of the PiN diodes were performed at a current density in the range of 50 A/cm^2 to 500 A/cm^2 in increments of 50 A/cm^2 using a typical direct current power supply under heating conditions at 300 K, 373 K and 423 K.

The expansion of ISSFs from the BPDs was observed by synchrotron X-ray topography with a 0.10–0.15 nm wavelength beam and PL imaging with a 425 nm bandpass filter after removing the electrodes from the stress-tested PiN diodes. ISSFs expansion positions originating from the BPDs were identified by comparing the obtained images with PL images recorded after epitaxial growth.

3. Results and discussion

We compared the results of the PiN diodes in this

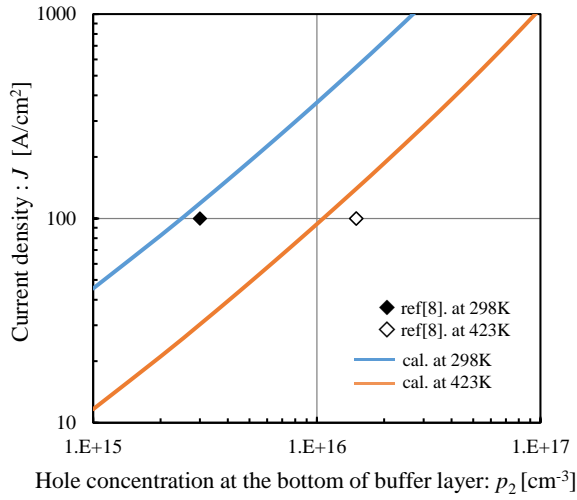


Fig. 3. Calculated J corresponding to hole concentration at the bottom of the buffer layer p_2 . Open and closed diamond symbols are values estimated from ref. [8]

study with literature results that calculated the hole concentration at the buffer/substrate interface, to assess the validity of our calculation model. Fig. 3 shows the calculated J corresponding to p_2 at different temperatures. The calculations were performed using the PiN diode structure parameters described in ref. [8]. Open and closed diamond symbols are plots of values estimated from ref. [8]. Although the value of our calculation is slightly larger than the literature as shown in Table 2, they are almost in good agreement. The difference in their value seems to be attributed to differences in the physical constants and models used in the calculations.

Fig. 4 shows the observation example of 1SSFs expanding from BPDs with 500 A/cm^2 for 60 min at 300 K. The triangular 1SSFs expanded from BPDs propagated into the epitaxial layer after the stress tests, as shown in Figs. 4a and b. BPDs in the substrate could not be detected by PL imaging. However, the bar-shaped 1SSF expanding from the BPD was obviously recognized in PL and X-ray topographic images after stress tests, as shown in Figs. 4 (b) and (c). In this way, we extracted the current density and temperature conditions of 1SSFs expansion from only the BPDs converted to TEDs at the buffer/substrate interface or in the substrate.

Fig. 5 shows the calculated J as a function of temperature at different p_2 and the experimentally

Table 2 Comparison of J values calculated from our model and literature values [8].

| Temperature [K] | hole concentration : p_2 [cm^{-3}] | Current density : J [A/cm^2] | |
|-----------------|---|---|-------------|
| | | Ref. | calculation |
| 298 | 3.0×10^{15} | 100 | 118.5 |
| 423 | 1.5×10^{16} | 100 | 139.6 |

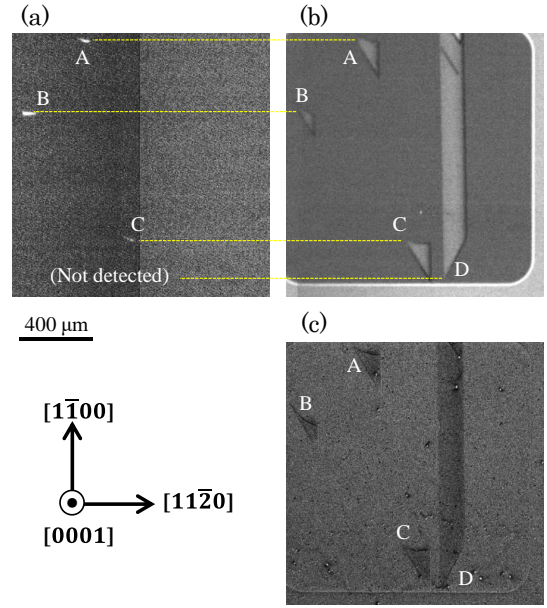


Fig. 4. Observation of 1SSFs expansion from the BPDs with 500 A/cm^2 for 60 min at 298 K. All images are same area. (a) PL image after epitaxial growth. A, B and C indicate BPDs in the epilayer. (b) PL image after stress test. (c) X-ray topographic image at $g = 2\bar{2}010$ after stress test. D indicates the origin of bar-shaped 1SSF expansion from the BPDs in the substrate.

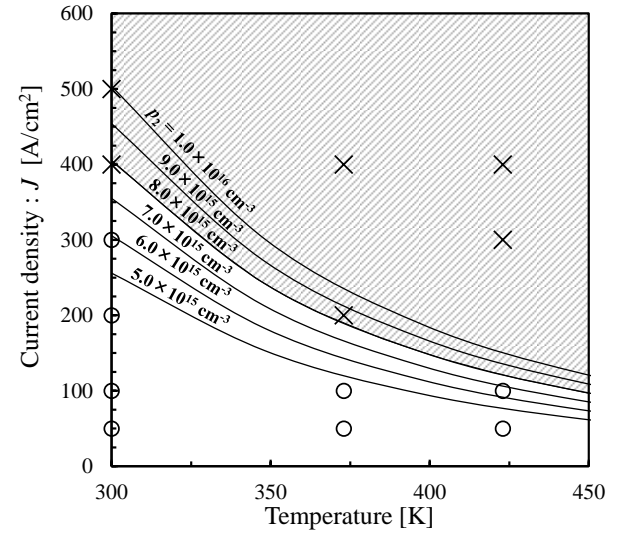


Fig. 5. J as a function of temperature at different value of p_2 . Conditions when the substrate BPDs expanded to 1SSFs in the forward-current stress test of the PiN diode are plotted as X symbols. The circled plots indicate the conditions under which the substrate BPDs did not expand.

extracted conditions of temperature and current density represented as the X symbols. The circled plots indicate the conditions under which the substrate BPDs did not expand. In the calculation of J , the device-structure parameters are based on the tested PiN diode in the Sect.

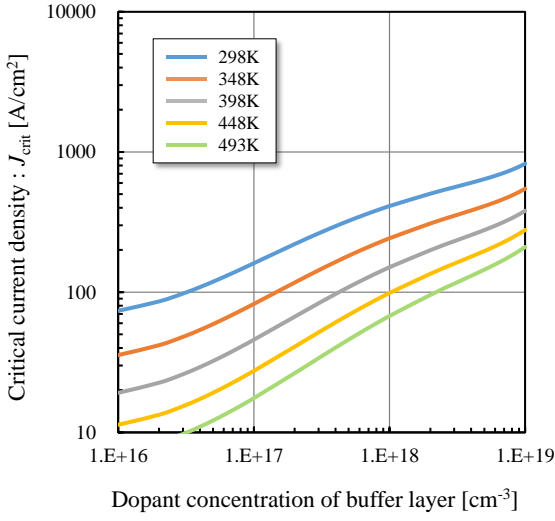


Fig. 6. J_{crit} as a function of dopant concentration of the buffer layer at different temperatures.

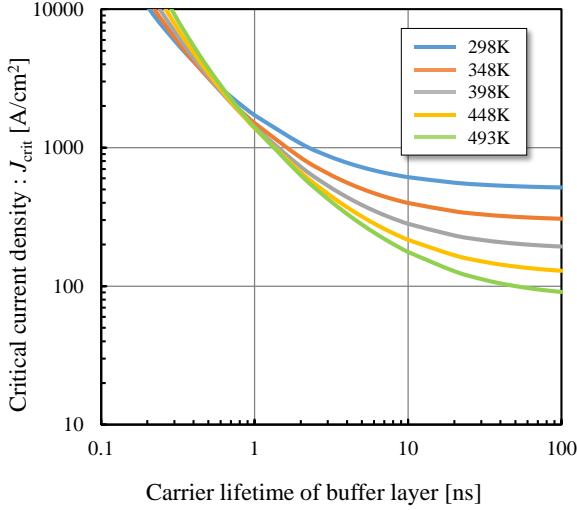


Fig. 7. J_{crit} as a function of τ_{buffer} at different temperatures.

2.3. We estimated p_{BPD} under the condition that BPDs were expanded to 1SSFs by changing p_2 . Here, p_2 was fixed with respect to changes in temperature. The resultant distribution of temperature and current density are positioned near and above the line of $p_2 = 8.0 \times 10^{15} \text{ cm}^{-3}$, therefore we estimate that the substrate BPD expands under the conditions of the hatched area in Fig. 5. Assuming that BPDs expand to 1SSFs when $p_{\text{BPD}} \geq p_{\text{crit}}$, we adopted the value of $8.0 \times 10^{15} \text{ cm}^{-3}$ as the p_{crit} for calculating J_{crit} in our model.

First, we calculated the dependence of J_{crit} when changing the parameters of various device structures, assuming carrier recombination was enhanced in the buffer layer. Fig. 6 shows J_{crit} as a function of the dopant concentration of the buffer layer at different temperatures. J_{crit} strongly depended on the buffer concentration, and greatly increased at high buffer concentrations. J_{crit}

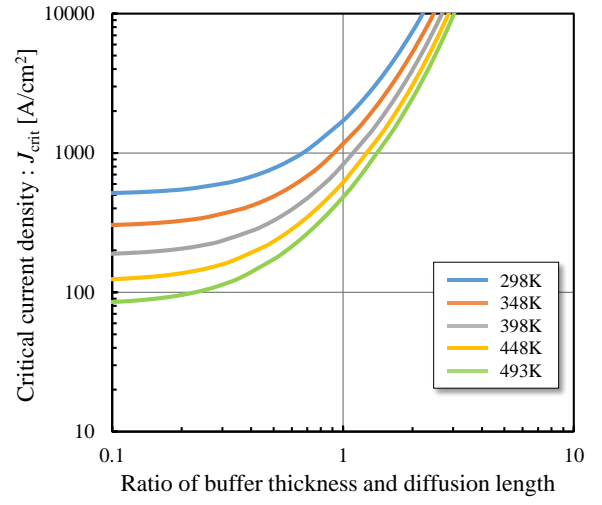


Fig. 8. J_{crit} as a function of $t_{\text{buffer}}/L_{\text{buffer}}$ at different temperatures.

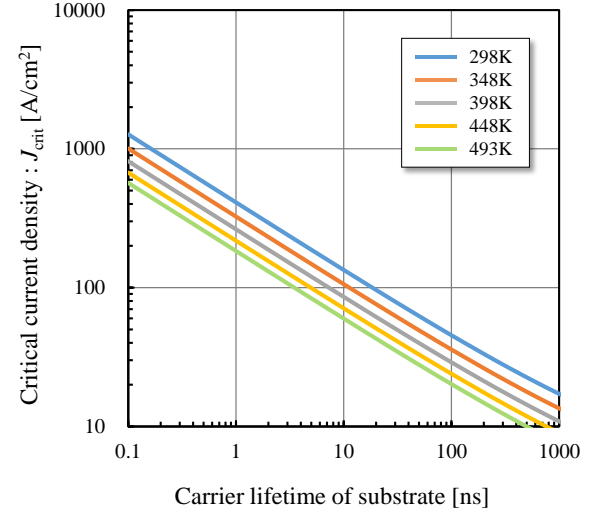


Fig. 9. J_{crit} as a function of τ_{sub} at different temperatures.

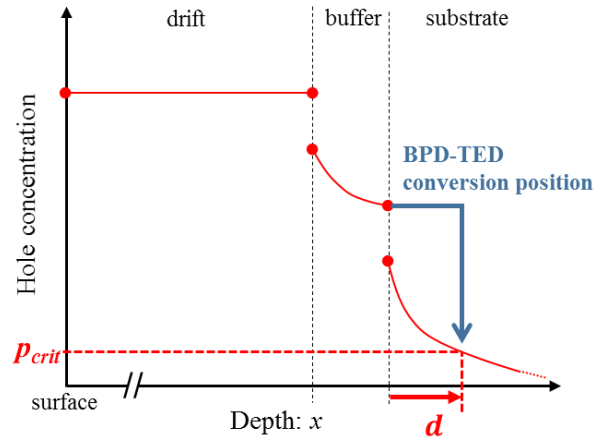


Fig. 10. Hole concentration profile for BPD-TED conversion located inside the substrate and displacement of p_{crit} .

decreased dramatically with increasing temperature.

Fig. 7 shows the calculation result of J_{crit} when τ_{buffer} was changed from 0.1 ns to 100 ns. J_{crit} increased to over 1000 A/cm² because L_{buffer} decreased as τ_{buffer} decreased, especially under conditions of 1 ns at $t_{\text{buffer}} = 0.5 \mu\text{m}$. The effect of J_{crit} on the diffusion length varied depending on the size of the buffer layer. Fig. 8 shows the dependence of J_{crit} on the ratio of t_{buffer} to L_{buffer} . The diffusion length was required to be sufficiently shorter than the buffer layer ($t_{\text{buffer}}/L_{\text{buffer}} > 1$) for improving the J_{crit} .

Next, the calculation model numerically determined that J_{crit} was improved by reducing the lifetime in the substrate τ_{sub} . Fig. 9 shows J_{crit} as a function of τ_{sub} at different temperatures. This suggested that a short $\tau_{p(\text{sub})}$ reduced the hole current density component of the total current density in the PiN diode, resulting in increasing J_{crit} , especially when $\tau_{\text{sub}} < 10$ ns. Although J_{crit} can be expected to improve by shortening the lifetime in both the buffer layer and the substrate in this model, increase of power loss is anticipated due to increased recombination of electrons and holes. The design of t_{buffer} is limited by τ_{buffer} based on the results of Fig. 8. In contrast, the substrate thickness can be thinned to reduce the substrate resistance [18] and the power loss. Since the control of τ_{sub} and the design of the thickness cannot be applied in this model, the effect on the device by shortening τ_{sub} requires further discussion.

We estimated J_{crit} considering the position of BPD-TED conversion in the substrate. The depth d underneath the buffer/substrate interface (as shown in Fig. 10) was set in the calculation model. The hole concentration p_3 at the top of the substrate when p_{crit} reaches depth d is expressed by equation (34) using equation (19),

$$p_3 = p_{\text{crit}} \exp\left(\frac{d}{L_{\text{sub}}}\right), \quad (34)$$

J_{crit} was similarly calculated by p_3 using the model. Fig. 11 shows the dependence of J_{crit} with BPD-TED conversion depth d at different temperatures. J_{crit} increased exponentially with increasing d . The approximate expression is represented as $J_{\text{crit}} = A \exp(Bd)$. The values of the coefficients A and B were obtained from the calculation model of the fabricated PiN diode structure as shown in Table 3. High-temperature annealing in Ar [19] and thermochemical etching in Si vapor (Si-vapor etching: Si-VE) [20] have been reported for converting BPDs to TEDs in the SiC substrate. For Si-VE, values for BPD-TED conversion at depths of 80 nm and 140 nm or more are reported. J_{crit} estimated from the calculation model was 709 A/cm² and 804

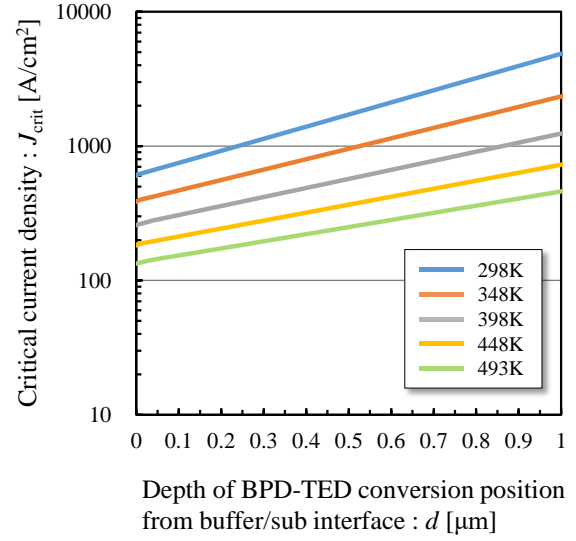


Fig. 11. J_{crit} as a function of BPD-TED conversion depth d at different temperatures.

Table 3 Values of coefficients A and B for the approximate expression $J_{\text{crit}} = A \exp(Bd)$ at each temperature (unit of d is μm).

| T [K] | 298 | 348 | 398 | 448 | 489 |
|---------|------|------|------|------|------|
| A | 599 | 385 | 258 | 182 | 134 |
| B | 2.10 | 1.81 | 1.57 | 1.39 | 1.24 |

A/cm² at 80 nm and 140 nm, respectively at 298 K. J_{crit} for the BPD converted at the buffer/substrate interface was 411 A/cm².

Increasing J_{crit} due to shorter L_{sub} and deeper BPD-TED conversion position d corresponds to an effect which makes it more difficult for the injected hole to reach the BPD during forward bias operation. This effect also corresponds to increasing allowed p_3 by getting larger d and smaller L_{sub} in the exponential term of equation (34). The model suggests that it will be an effective technique for suppressing forward bias degradation by controlling the characteristics of the substrate. In addition, further J_{crit} improvement is expected by optimizing the buffer concentration and lifetime based on the results of Fig. 8.

In this model, J_{crit} gives a threshold of current density for ISSF expansion and does not strictly represent a threshold for on-voltage degradation. Therefore, it seems that the on-voltage degradation actually reduces at 423 K or higher [3]. However, we believe that the results of our model will be useful for concerns about the degradation of the blocking voltage [5] in the reverse bias mode due to the expanded ISSFs.

4. Conclusions

We proposed a calculation model for the 4H-SiC PiN diode which considers temperature dependence. This model can estimate the critical current density J_{crit} for forward bias degradation originating from BPDs in the SiC substrate. We discussed the device structures and substrate characteristics for suppressing forward bias degradation.

The results from the calculation model are in good agreement with reported current densities at 298 K and 423 K. We estimated the critical hole concentration p_{crit} at which the BPDs in the substrate expanded to ISSFs, from forward-current stress tests of PiN diodes and PL and X-ray topography imaging. The p_{crit} at the bottom of the buffer layer evaluated from experiment by comparison with our model results was $8.0 \times 10^{15} \text{ cm}^{-3}$.

We confirmed the effect of introducing carrier recombination into the buffer layer in the calculation model. J_{crit} greatly increased in the high concentration region of the buffer layer and decreased dramatically with increasing temperature. J_{crit} increased rapidly under the condition of $t_{\text{buffer}}/L_{\text{buffer}} > 1$.

We numerically showed the improvement in J_{crit} by shortening the substrate lifetime and deepening the BPD position in the substrate. The approximate expression for J_{crit} was estimated in the case of BPD-TED conversion in the substrate. J_{crit} was 411 A/cm^2 when BPD-TED conversion located at the buffer/substrate interface, while J_{crit} was 709 A/cm^2 and 804 A/cm^2 at 80 nm and 140 nm depth of BPD-TED conversion position in the substrate, respectively at 298 K.

Shorter lifetime and deeper BPD-TED conversion position in the substrate provide an effect that makes it difficult for the injected hole to reach the BPD during forward bias operation. We believe the calculation model provides useful guidance on the SiC bipolar device structure, material design and device usage to suppress forward bias degradation caused by BPDs in the substrate.

Acknowledgements

We thank Dr. J. Senzaki of the National Institute of Advanced Industrial Science and Technology (AIST) for fabrication of the PiN diodes and discussion of electrical characteristics. We thank Lasertec Corporation for PL imaging observations. Experiments using synchrotron radiation were performed at the beamline BL09 of the SAGA Light Source with the approval of the Kyushu Synchrotron Light Research Center (Proposal No. 1809084R and 1907060R /BL09).

References

- [1] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices", Jpn. J. Appl. Phys. 54, 040103 (2015).
- [2] H. Lendenmann et al., "Degradation in SiC Bipolar Devices: Sources and Consequences of Electrically Active Dislocations in SiC", Mater. Sci. Forum, 433-436, 901-906 (2003).
- [3] K. Nakayama et al., "Behavior of Stacking Faults in TEDREC Phenomena for 4.5 kV SiCGT", Mater. Sci. Forum 600-603, 1175-1178 (2009).
- [4] T. Miyanagi et al., "Annealing effects on single Shockley faults in 4H-SiC", Appl. Phys. Lett. 89, 062104 (2006).
- [5] T. Ishigaki et al., "Analysis of Degradation Phenomena in Bipolar Degradation Screening Process for SiC-MOSFETs", Proc. of ISPSD, 259-262 (2019).
- [6] S. Ha et al., "Dislocation conversion in 4H silicon carbide epitaxy", J. Cryst. Growth 244 (3-4) 257-266 (2002).
- [7] K. Konishi et al., "Stacking fault expansion from basal plane dislocations converted into threading edge dislocations in 4H-SiC epilayers under high current stress", J. Appl. Phys. 114, 014504 (2013).
- [8] T. Tawara et al., "Injected carrier concentration dependence of the expansion of single Shockley-type stacking faults in 4H-SiC PiN diodes", J. Appl. Phys. 123, 025707 (2018).
- [9] S. Hayashi et al., "Relationship between depth of basal-plane dislocations and expanded stacking faults by application of forward current to 4H-SiC p-i-n diodes", Appl. Phys. Express 12 051007 (2019).
- [10] T. Tawara et al., "Short minority carrier lifetimes in highly nitrogen-doped 4H-SiC epilayers for suppression of the stacking fault formation in PiN diodes", J. Appl. Phys. 120, 115101 (2016).
- [11] T. Miyazawa et al., "Carrier Lifetime Control of 4H-SiC Epitaxial Layers by Boron Doping", Mater. Sci. Forum 51-54, 897 (2017).
- [12] T. Miyazawa et al., "V and Ti Doping in 4H-SiC Epitaxy for Reduction of Carrier Lifetimes", Mater. Sci. Forum 67-70, 897 (2017).
- [13] T. Kimoto and J. A. Cooper, "Fundamentals of Silicon Carbide Technology", Chapter 7 p.287, John Wiley & Sons, Singapore, (2014).
- [14] J. R. Jenny et al., "Effects of annealing on carrier lifetime in 4H-SiC", J. Appl. Phys. 100, 113710 (2006).
- [15] T. Kimoto and J. A. Cooper, "Fundamentals of Silicon Carbide Technology", Appendix A p.512, John Wiley & Sons, Singapore, (2014).
- [16] U. Lindefelt, "Doping-induced band edge displacements and band gap narrowing in 3C-, 4H-, 6H-SiC, and Si", J. Appl. Phys. 84, 5, 2628-2637 (1998).
- [17] T. Kimoto and J. A. Cooper, "Fundamentals of Silicon Carbide Technology", Chapter 9 p.392, John Wiley & Sons, Singapore, (2014).

- [18] R. Rupp et al., "Performance of a 650V SiC Diode with Reduced Chip Thickness", Mater. Sci. Forum 921-924, 717-720 (2012).
- [19] N. A. Mahadik et. al., "Mitigation of BPD by Pre-Epigrowth High Temperature Substrate Annealing", Mater. Sci. Forum 233-236, 858 (2016).
- [20] Y.Sudoh et al., "BPD-TED Conversion in the SiC substrate after High-Temperature Si-VE", Ext. Abst. of ICSCRM, Th-1B-04 (2019).