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A Novel Control Method For Grid Side Inverters Under Generalized Unbalanced Operating Conditions

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A NOVEL CONTROL METHOD FOR GRID SIDE INVERTERS UNDER GENERALIZED UNBALANCED OPERATING CONDITIONS

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It took me a while to finish this thesis. Had I known at the start of my master's program that I would only be completing it ten years later, I probably would have opted-out for an easier route. Nevertheless, I'm not regretting this long journey, since it helped me to learn many great things on the way.

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A NOVEL CONTROL METHOD FOR GRID SIDE INVERTERS UNDER GENERALIZED UNBALANCED OPERATING CONDITIONS

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ABSTRACT

This thesis provides a summary on renewable energy sources integration into the grid, using an inverter, along with a comprehensive literature research on variety of available control methods. A new generalized method for grid side inverter control under unbalanced operating conditions is also proposed. The presented control method provides complete harmonic elimination in line currents and DC link voltage with adjustable power factor. The method is general, and can be used for all levels of imbalance in grid voltages and line impedances. The control algorithm proposed in this work has been implemented by using MATLAB Simulink and dSPACE RT1104 control system. Simulation and experimental results presented in this thesis are in excellent agreement.

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NOMENCLATURE

SRF: Synchronous Reference Frame

d-q: Direct and Quadrature Axes

IGBT: Insulated-Gate Bipolar Transistor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

THD: Total Harmonic Distortion

EMI: Electro-Magnetic Interference

DC: Direct Current

AC: Alternating Current

PF: Power Factor

VUF: Voltage Unbalance Factor

APF: Active Power Filter

RES: Renewable Energy Sources

DER: Distributed Energy Resources

ESS: Energy Storage System

PEC: Power Electronics Converters

DG: Distributed Generation

GSI: Grid Side Inverter

VSI: Voltage Source Inverter

CSI: Current Source Inverter

PCC: Point of Common Coupling

PV: Photovoltaic

PMG: Permanent Magnet Generator

PLL: Phase Locked Loop

DSP: Digital Signal Processing

PI: Proportional-Integral

PR: Proportional-Resonant

VOC: Voltage Oriented Control

POC: Power Oriented Control

DPC: Direct Power Control

DTC: Direct Torque Control

VDTC: Virtual Direct Torque Control

MPC: Model Predictive Control

CC: Current Control

SMC: Sliding Mode Control

PWM: Pulse Width Modulation

SVM: Space Vector Modulation

FACTS: Flexible AC Transmission Systems

STATCOM: Static Synchronous Compensator

MPPT: Maximum Power Point Tracking

LVRT: Low Voltage Ride Through

FRT: Fault Ride Through

IPT: Instantaneous Power Theory (PQ Theory)

CHAPTER I

INTRODUCTION

1.1 Renewable Energy Sources

In the past few decades, the demand and interest in Renewable Energy Sources (RES) has been continually on the rise. A growing energy demand, along with concerns for depleting fossil fuels and air pollution, are some of the factors that have significantly accelerated the growth of the renewable energy sector [47]. According to EIA [1], renewable energy resources accounted for more than 17% of total U.S. electricity generation in 2019 (Fig. 1), and the energy consumption from RES in the same year, has exceeded the consumption of coal for the first time since 1885 [2]. The same upward trend in renewable energy is observed in the whole world (Fig. 2).

Resources such as wind, solar energy (photovoltaic), hydropower, geothermal, biomass, fuel cells, and others, are increasingly integrated into power systems as part of the Distributed Generation (DG), also known as Distributed Energy Resources (DER). As a consequence, much work has been done lately on design and control of Grid Side Inverters (GSI), also known as Voltage Source Inverters (VSI), to successfully integrate RES into the power grid.

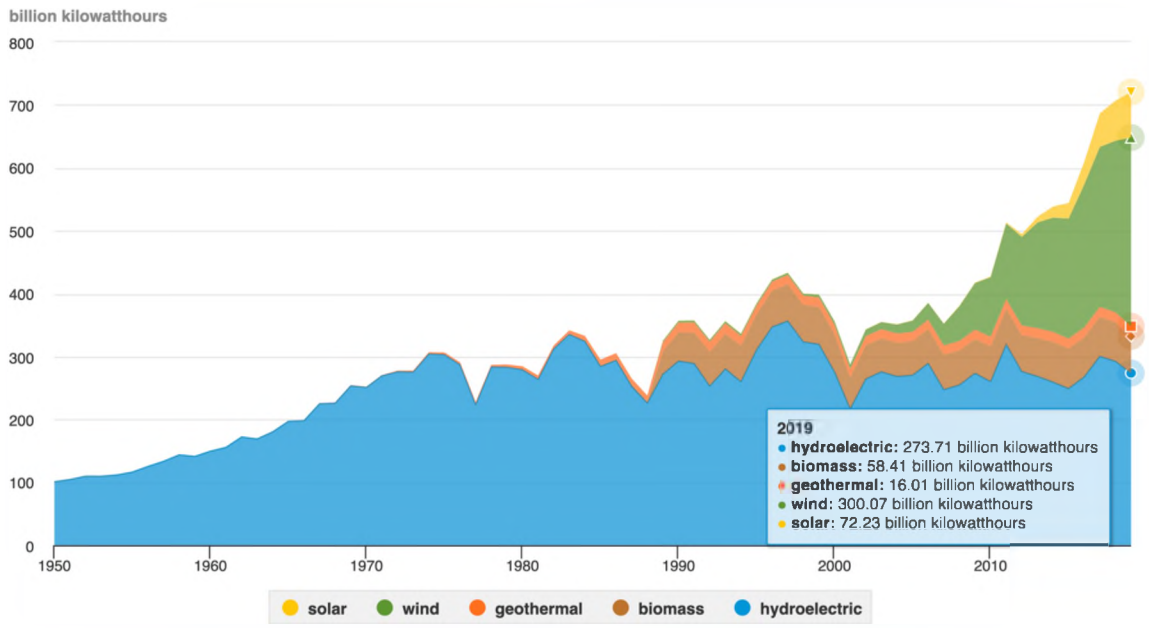

Figure 1: U.S. Electricity Generation from RES, 1950-2019, taken from [1].

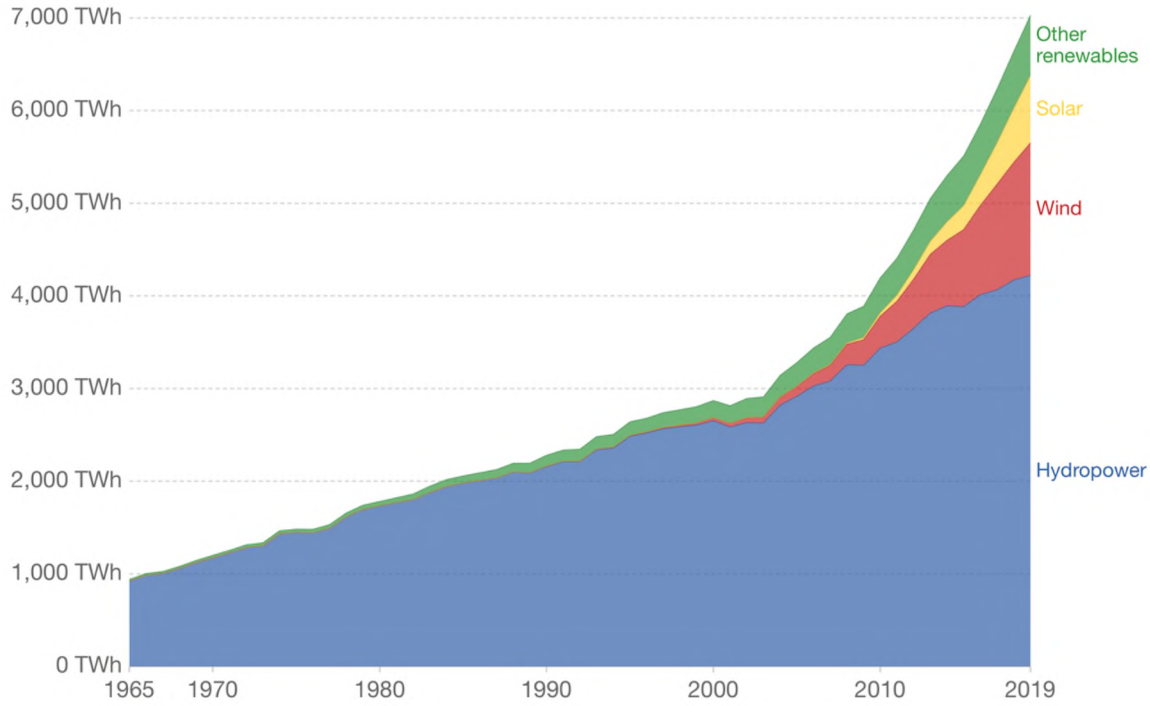

Figure 2: Renewable Energy Generation in the World, 1965 to 2019, taken from [3].

A continuous decrease in the price of silicon has made GSI a standard choice for connecting RES to the utility. There are many inverter topologies utilized today, implementing different multi-level and multi-phase converters. Some of the more common include capacitor midpoint, three H-bridge, neutral point clamped, and various four-leg configurations, however the most commonly adapted is a two-level, three-phase (three-leg) converter that uses six switches to change energy into a fixed grid-frequency power [4]. Power harvested from RES is obtained in various forms. PVs and fuel cells produce DC, while wind or hydropower typically provide variable AC. Power electronic converters (PEC) become useful at this point, since they can easily convert one form of energy into another, either with a rectifier (AC to DC) or an inverter (DC to AC). The two converters are commonly used in back-to-back configuration, separated (decoupled) by a DC-link capacitor, which allows for independent control of the two converters.

To maximize power output, variable-speed wind applications are oftentimes preferred over the constant-speed ones, hence the power is converted with rectifier-inverter configuration in two stages [52]. Variable-frequency AC power from a wind turbine cannot be fed directly into the power line, thus it is rectified into a fixed DC during the first stage. The second stage uses VSI to convert DC to three-phase, grid-frequency AC power (Fig 3). In photovoltaic (PV) applications, harvested DC energy can either be stored by an energy storage system (ESS) for later use, or stepped-up with a boost converter (DC to DC) in the first stage, and inverted to AC with VSI in the second [27]. Unless the harvested DC voltage is greater than the peak line-to-line voltage at the output of the inverter, DC to DC boost conversion is required in the first stage to be able to send power to the grid, otherwise only the second stage is necessary [4, 31, 32].

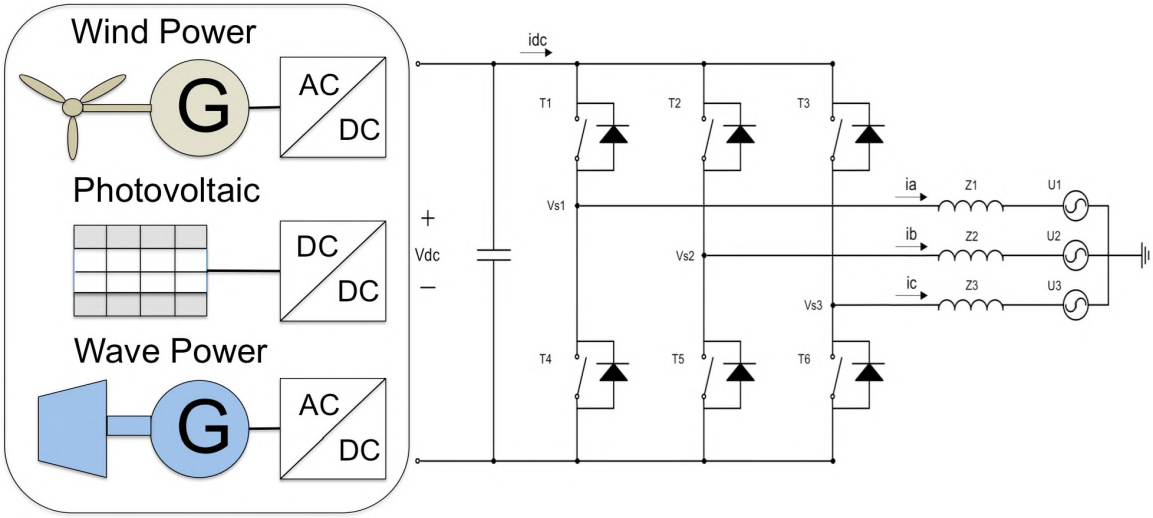

Figure 3: Renewable Energy Sources and the Grid Side Inverter.

1.2 Grid Requirements

Several considerations have to be made when working with RES. A lot depends on a particular application, the amount of power RES can generate, and whether it will operate in islanded (standalone) mode, or it will be part of the network or a microgrid, operating in grid-connected mode (grid-feeding or grid-supporting) [26]. Grid integration involves compliance with the established national and international grid codes (i.e. IEEE Std.1547, 519-2014, 929-2000, IEC 61727, etc.), which are becoming more and more restrictive as more RES are being connected to power systems [24, 40, 45].

One of the major requirements has to do with the power quality, measured in total harmonic distortion (THD), where injected grid currents have to be less than 5% THD. Other codes require DER to have low voltage ride through (LVRT), also known as fault ride through (FRT), capability for a specified amount of time if the grid faults are momentary and not severe (usually less than 10% voltage drop) [22, 28]. These requirements also differ from country to country [32, 40]. In cases when the fault is more

severe/longer lasting, anti-islanding is required and the DER has to disconnect. But more recent grid codes revisions prefer the inverters to remain connected during grid faults and to provide power even if the main grid power is absent, in the case of islanding [32, 42]. In addition to high power quality and LVRT capability, RES converters are expected to provide ancillary services of conventional generation – to inject reactive current to support grid voltage under grid faults, but these new grid codes are still in the process of development due to uncertainties how these reactive currents should be calculated [8]. In summary, grid codes oftentimes require DER to possess reactive power injection, inertia, oscillation damping during transients, steady-state stability, and offer voltage support during faults, including FRT capability [22].

1.3 Grid Unbalance and Faults

Operation and control of GSI is relatively straight-forward in normal-operating grid, but challenges emerge when the grid voltage is asymmetrically unbalanced. Unbalances typically occur in weak ac systems and can be caused by the presence of nonlinear/unbalanced loads, single-phase loads, or by faults (disturbances) occurring anywhere on the transmission line (remote grid faults) [38]. In islanded operation, most of the unbalance is caused by unbalanced loads or DG, while in grid-connected mode, they can also come from utility failure [27]. In addition to existing sources of unbalance, the increasing number of DER themselves also contribute to grid instability, because of their integration to the grid by nonlinear power electronics converters, and also due to the absence of real synchronous machines (often the case in microgrids [4]), that produce

inherent rotor inertia and damping characteristic to sustain constant grid frequency [21, 22].

Voltage unbalance and faults can be classified into different categories. Voltage unbalance can be symmetric, where all three phases drop equally in magnitude, and asymmetric, where one or more phases differs in magnitude. This asymmetry is typically represented in percentage with Voltage Unbalance Factor (VUF). Voltage sags can be classified into seven distinct types, ranging from A to G based on ABC classification, where phases deviate in magnitude and angle from their balanced values [18, 22]. Distribution line faults are similarly divided into four types, listed in the order of severity:

- Single Line to Ground fault (SLG)
- Line to Line fault (LL)
- Double Line to Ground fault (LLG)
- Three-Phase fault (3P)

In summary, the nature of grid unbalance can include changes in voltage magnitude (sags or swells), frequency drifts, phase shifts, presence of unwanted harmonics, periodic interruptions, and longer lasting single or multiple-line faults.

Under balanced conditions (also in symmetric voltage drop cases) only positive sequence components in voltages and currents flow, however during asymmetric unbalance, zero sequence components (if the neutral wire is present) and negative sequence components appear. If the inverter is connected and operating under such conditions, various low-order harmonics (even on the DC side and odd on the AC side) start to flow, causing voltage fluctuations (ripple) at the DC link capacitor, and current harmonics at inverter's output [52]. The primary danger comes from oscillations at twice the grid

frequency (100 or 120 Hz). As a result, these oscillations decrease capacitor lifetime, and various current spikes cause overheating and equipment damage if not regulated. At other times these oscillations will lead to instability [38]. Also, sudden voltage drop at the mains causes the current to quickly increase at inverter's output, which might trigger overcurrent safety mechanisms, causing the inverter to disconnect [40]. All these circumstances lead researchers to develop various control methods, so inverters are able to handle and to properly respond to grid unbalance.

1.4 Unbalance Correction

Harmonics caused by faults and nonlinear loads can be compensated with passive filters, active power filters (APFs), or hybrid compensators, that combine the advantages of the two [26]. Passive filters are simple to implement and they can effectively trap current harmonics near the source of disturbance, but are oftentimes tuned to a fixed loading condition. APFs, on the other hand, are more robust and are designed to adapt to various nonlinear conditions, which makes them a good choice in grid unbalance situations.

APFs can be connected in series with the power line, acting as voltage sources, and inject negative sequence voltage to correct grid unbalance. They can also be connected in parallel (shunt), a more common way of connection, and inject negative sequence current. They can also be placed as series-parallel compensators, that combine voltage/current injection, or as static synchronous compensators (STATCOMs), to inject positive and negative sequence reactive powers [38]. Voltage unbalance on the transmission line is traditionally corrected by the utility with static VAR compensators (also STATCOMs and FACTS). Their main job is to compensate reactive power to support grid voltage by

keeping the power factor (PF) close to unity. But in micro/smart grids, and in islanded operation, this function could be fulfilled by GSI, hence the extra cost associated with traditional compensators is often eliminated. During symmetrical voltage sags (low voltage faults), inverter systems provide reactive power to the grid per grid codes [28, 31]. Moreover, inverters, now as APFs, can be controlled to do much more than just provide reactive power, but that will depend on the specific application, the mode of operation, the rating of the converter, and other factors.

1.5 Power Flow

Power flow from RES to the utility can also be characterized by either grid-driven or RES-driven feeding. In a grid-driven feeding, RES is satisfying the requirements of the grid by controlling the power to maintain utility voltage and frequency during unbalance (grid-forming mode), or producing a predefined amount of power to the grid that does not depend on grid imbalance but is still specified and adjusted by the utility management unit (grid-supporting mode). In RES-driven feeding, the RES itself is setting those requirements, and inverter systems, such as wind or PV, are typically operated at MPPT to maximize their power delivery [13].

For total control of the output power flow, the DC voltage at the input capacitor of GSI needs be greater than the peak value of the line-to-line voltage at the inverter's output (except for H-bridge) [4]. The capacity of the RES and the type of load at the PCC also affect the flow. Resistive loads take active power from the inverter, or from the grid if RES can't meet the full demand. Similarly, loads operated at PF other than unity, will be fed active/reactive power either from RES or the grid at desired proportion. In the event when

the load is not operating, the inverter can be supplying the power to the utility, hence feeding the grid.

When the grid is asymmetrically unbalanced, power flow control becomes more challenging, since the converters themselves now have to be protected from lower order harmonics on DC-link and AC sides, by canceling them with appropriate opposite-phase signal injection, usually with negative sequence currents [25], while still providing power to the load at desired PF. In addition to converter protection, control strategies provide voltage compensation to the unbalanced grid, by controlling positive and negative sequences of active and reactive powers [38]. If grid current is a controlled signal, current harmonics in unbalanced grid are eliminated by calculating appropriate reference currents, sometimes using PQ theory, and then forcing the inverter output currents to track these calculated references [43, 44]. The key for controlling the power flow is typically in controlling VSI output currents and maintaining them sinusoidal during all conditions – balanced and unbalanced grid voltage or grid/load impedance.

In summary, power flow between GSI and the grid can be bi-directional, and depends on the mode of operation of the inverter. VSI can transfer active power harvested from RES, and supply/absorb reactive power as demanded by the local loads, while eliminating harmonics caused by unbalanced loads or unbalanced grid at DC-link and at the point of common coupling (PCC), and maintaining sinusoidal grid currents [47]. Factors such as the capacity of the RES, the rating of the components, the severity of the unbalance, and the robustness of the control method will also determine if all the functions described above can be successfully performed.

1.6 Control Strategies

As already mentioned, VSI's connection to the grid depends on its mode of operation (grid-feeding, grid-supporting, or standalone), hence an appropriate control strategy is employed in each case. In standalone (islanded) operation, droop and virtual impedance control are used to control multiple inverters, connected in parallel, sharing the load [27]. In grid-connected operation however, inverters are typically treated as voltage controlled current sources, connected in parallel with the grid, where the output power or the output voltage and frequency is regulated [26]. Methods, such as Voltage Oriental Control (VOC), Direct Power Control (DPC), Virtual Direct Torque Control (VDTC), and Current Control (CC) are often implemented, using one or several control loops. The slower outer loop typically controls either the DC side voltage, the AC side voltage, or the output power at the PCC, while the faster inner loop controls the inverter current that normally follows current references generated by the outer loop [8]. DPC and VDTC can be implemented with only one loop, where active and reactive power are directly controlled, while VOC usually contains two loops, – the outer active/reactive power loop and the inner current loop.

The above control strategies are implemented with various linear and non-linear controllers [6]. Linear controllers, such as PID, are widely used due to their easy implementation, and generally benefit from constant switching frequency, but experience difficulties with steady-state error, nonlinear signals, periodic disturbances, and have a tradeoff between system stability and good dynamic response during transients [35]. Non-linear controllers, such as hysteresis (HC), are also widely used. Their benefits include easy implementation, good stability, no steady-state error, fast response, maximum current

limiting, and robustness to load parameter variations [35]. Nevertheless, HC has drawbacks from high and variable switching frequency. Proportional-Resonant (PR) controller, often an alternative for PI, solves the issue of the steady-state error and harmonic disturbance, but does not respond well to frequency variations. Since conventional controllers each have their own limitations, other strategies such as sliding mode, resonant, predictive, or repetitive control are also used [24]. While sliding mode is growing in interest, due to its robustness and fast response, it is limited by its dependence on the plant knowledge. Predictive controllers are also complex and require knowledge of load parameters, and repetitive controllers suffer from slow response and weak stability [4, 35, 42].

Many of the control strategies above (especially PI) are based on instantaneous power theory (IPT), also known as PQ theory, where active (P) and reactive (Q) powers are decoupled, using sequence components, and are controlled separately. PQ-based control is essentially expressed in a form of power-characteristic-oriented control, focusing on the oscillations in the output power, or voltage-support-oriented control, controlling the amount of active/reactive power, to compensate voltage unbalance at PCC [8, 22]. In this theory, P and Q are the instantaneous fundamental components of active and reactive power respectively, but additional pulsating terms appear if unbalance is present [20, 25]. Constant terms (a desired quantity) appear as a result of voltage and current interaction from the same sequence, while the oscillating terms (undesired quantity) appear when their interaction is from positive and negative sequences [8]. Various strategies are undertaken to eliminate the pulsating components (usually the negative sequence component), but despite the efforts, the oscillations exist either in the output active and/or reactive power, or the output current is not sinusoidal [32]. IPT can be implemented in both stationary $\alpha\beta$,

and rotating *dq* reference frames. A natural link between real/reactive power and reference currents in *dq* frame allows control of power by controlling the angle of the current [23]. When the current is aligned with the grid voltage vector (d-axis), active power is controlled, and if the current is aligned with the q-axis, reactive power is controlled [10, 22].

1.7 Reference Frames

With many inverter control strategies available, all of them are executed in a particular reference frame. The choice is usually between a stationary *abc*, stationary $\alpha\beta$, or synchronous rotating *dq* frame. Some utilize more than one, which requires transformation from one to another. The relationship between these three can be seen in Figure 4.

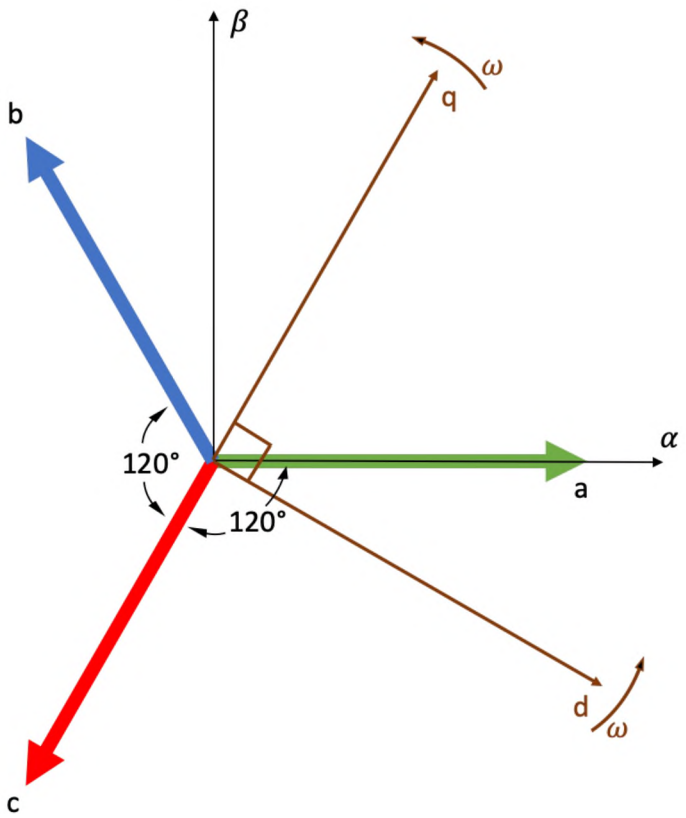

Figure 4: Stationary *abc*, $\alpha\beta$, and rotating *dq* reference frames.

A stationary $\alpha\beta$ reference frame uses Clarke's transformation matrix to represent each vector of *abc* frame, with its horizontal and vertical components, α and β, using two orthogonal axes, separated by 90 degrees. The advantage of this frame is that it does not require coordinate transformation to a rotating frame that causes extra delay, and that positive, negative, and zero sequence components can be controlled simultaneously in a stationary frame [40]. If the inverter has no neutral wire, zero-sequence component is zero [28]. Still, a negative sequence component is apparent during unbalance and thus must be controlled. Negative sequence component causes oscillations, primarily at twice the grid frequency, in the output current (also output active and reactive powers) [23]. This double frequency can be eliminated with a notch filter, but at the expense of extra delay, affecting the stability of the control system [28]. Consequently, methods in this reference frame oftentimes employ proportional-resonant (PR) controllers, that theoretically have an infinite gain at the resonant frequency, and when tuned to double-grid frequency, they are effective in removing the steady-state error. But computational burden increases as the number of PR controllers increases, tuned for each additional harmonic, hence various strategies are undertaken to reduce the number of resonant terms [24]. Also, PR doesn't respond well to initial conditions, or when the grid frequency isn't constant, or when disturbances are nonperiodic [22]. One also has to be careful when designing control, especially when the switching frequency is getting close to the resonant frequency, and the two might interfere. Nevertheless, compared to rotational frames, the control variables in this frame are still AC quantities, hence the control complexity is simpler, easier to implement, with computational savings [37]. While the delay in the stationary frame is

mostly digital, its accumulation must be accounted for in the stages of detection, filtering, computation, and when sending the driving waveforms [40].

Another popular control frame is a synchronous (rotating) *dq* reference frame (SRF), that uses Park's matrix to transform from stationary frames. The primary purpose of this conversion is to separate the fundamental component from the rest of the harmonic content by rotating the cartesian plane orthogonal axis (*dq*) with the same angular frequency (ω) as the grid voltage fundamental wave [40] (see Fig. 4). The d-component is synchronized with the grid voltage, rotating counterclockwise, with phase-locked loop (PLL), which is the most common way to synchronize DG with the utility [24]. As a result, positive sequence components of the controlled variables become constant (DC), and a simple linear Proportional-Integral (PI) controller is used to get rid of the steady-state error. PI control works well in balanced conditions, however during unbalance, negative sequence components are oscillating at double-grid frequency (2ω, 100 or 120 Hz), and need to be eliminated either with a low-pass filter, a notch filter, or another resonant controller. Sometimes a dual SRF is utilized (Fig. 5), where one frame is rotating counterclockwise (along with the grid), controlling positive sequence components, and the other rotating clockwise, controlling negative sequence components, hence two separate PI controllers are used, regulating both sequence components as DC quantities [19, 23, 28, 40]. If the neutral wire is present, zero sequence components also need to be regulated, sometimes in the stationary frame. Nevertheless, even with a dual SRF, negative sequence components in positive rotating frame, and positive sequence components in negative rotating frame appear as double oscillations, and additional filtering needs to be employed [19]. Consequently, during unbalance, linear PI controllers become limited due to their

inability to get rid of the steady-state error in non-DC signals. Some of their disadvantages include the cross-coupling between positive and negative sequences [22], slow response, especially when the number of control loops is increased, their inability to reject higher frequency harmonics [36], low bandwidth limitations [25], and problems with grid frequency drift [43]. When considering synchronization, PLL is not able to accurately estimate the grid voltage angle during unbalance because of the 2nd harmonic oscillation [22]. Filtering these harmonics adds to extra computation and delay, and in case of severe faults, the grid phase voltage changes, and PLL delay leads to more delay and overcurrent, thus phase-compensators need to be used [40]. Because PI-based controllers can't handle periodic disturbances well, methods such as resonant, repetitive, predictive or sliding control are used instead [24]. Even though rotating frame brings the advantage of simple PI control under balanced conditions, its main disadvantages under significant unbalance are the controller's design complexity and high computational burden [37].

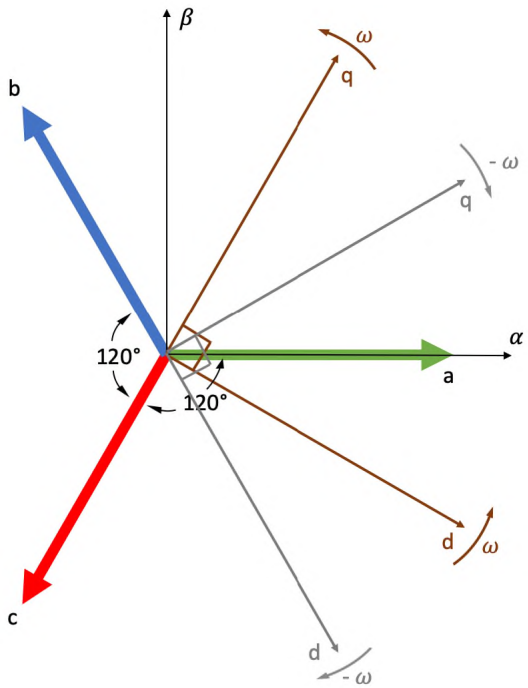

Figure 5: Dual rotating *dq* reference frame.

Finally, a classic stationary (natural) *abc* reference frame (used in this thesis) is also commonly implemented, where three-phase voltages and currents are represented as three phasors, 120 degrees apart (Fig. 4). Voltage is oftentimes synchronized with the grid with PLL, that works as a rising-edge zero-crossing detector. Various control methods, including dead beat (DB), sliding mode (SMC), H-infinity, repetitive, HC, and others are executed in this stationary frame. These methods are typically easy to implement. They respond well to nonlinearities and grid frequency variation, and provide good stability and fast response. Most of the control methods employed in this frame are nonlinear, and although relatively easy to work with, have their limitations as well, such as finite sampling frequency in digital control, and switching losses in analog control [43]. Other reference frames are also used, but the three presented in this section are the most common.

1.8 Switching Topologies

Once the choice for a desired reference frame is made, control methods use several modulation techniques to turn VSI switches on and off in a particular sequence, to make the controlled signal follow its reference. These switching topologies can be classified into carrier-based (e.g. space vector modulation (SVM), sinusoidal pulse-width-modulation (SPWM)) and carrier-less (e.g. model predictive control (MPC), hysteresis control (HC)) [4]. Many of them use some form of pulse-width-modulation (PWM), which controls the duty-ratio (time-on/time-off) of the switch that controls the output signal. SPWM uses a triangular carrier frequency signal to generate a PWM pattern, while SVM divides vector space into six 60-degree segments and places the controlling vector into an appropriate segment using switching tables [6, 7]. Carrier-based topologies are usually favored due to

constant switching frequency, although these methods are more difficult to implement in real-time [4]. In carrier-less modulation strategies, such as hysteresis control (HC), the switch's state changes whenever a boundary of the signal tolerance band is reached, hence the switching frequency is often variable, which requires EMI filtering [18]. In HC, although still variable, the switching can be controlled by tightening and relaxing the upper and the lower bands around the reference signal: whenever the bands are tightened, the oscillations around the reference signal are more restricted, but at the cost of increasing switching, and vice versa. Therefore, there is always a tradeoff between performance accuracy and the switching frequency [35]. On the positive side, the dynamic response in carrier-less controllers is typically vary fast.

1.9 Filtering

VSI is interconnected to the grid with some passive damping filters that compensate the switching frequency. It's important to note, these typically serve as low-pass filters, designed to attenuate high-frequency noise caused by inverter switching, in addition to active damping strategies developed for low-order harmonics caused by grid unbalance. A common practice is to use either a first-order L-filter, or a third-order LCL-filter, depending on the controller design. LCL-filters are currently growing in interest since they attenuate switching harmonics quite well, allow the use of lower switching frequency, and reduce EMI [36]. Even though LCL provides good attenuation, it introduces a resonant frequency to the plant that needs to be suppressed with various damping strategies. If not regulated, this can lead to instability [23]. At the same time, stability design becomes challenging due to poor damping of complex poles located near to the right-hand-side of the complex plane.

Additionally, the uncertain nature of the grid and its parameter variations add more complications. Other challenges appear when the sampling and resonant frequencies get too close [36]. The resonant frequency is typically selected to be at least ten times the grid frequency and less than half of the switching frequency. In contrast to third-order LCL-filters, first-order L-filters require no resonance damping, and are quite effective [41]. Unfortunately, L-filters require large inductors or high switching frequency to attenuate it well, and generally consume more power compared to LCL. Other 2^{nd} order filters are also used, such as LC [18, 29, 42] or CL [28], but LC-filters are essentially LCL, because the grid has its own inductance, hence this fact also needs to be considered while designing the filter [42].

1.10 Organization of this Thesis

This thesis utilizes two-level, three-leg inverter with six switches under various unbalance conditions, ranging from unbalanced load to most severe line faults, including Double Line to Ground (LLG) fault. The method uses relatively straightforward current control, where line currents are tracking current references, specifically calculated for each fault condition. The method effectively eliminates current harmonics and demonstrates bi-directional power flow with complete PF adjustability. Hysteresis control is executed in *abc* reference frame, hence no reference frame transformation, sequential component extraction, and extra online calculation is required. Each phase of the inverter is connected to the grid with a single inductor (L-filter), sufficient to eliminate high frequency noise and satisfy grid requirements.

This thesis is organized as follows. CHAPTER II reviews up-to-date published literature on inverter control. CHAPTER III describes a proposed analytical method for input-output harmonic elimination of a grid side inverter under generalized unbalanced operating conditions, and presents the proposed control method. CHAPTER IV details the implementation of the proposed method in MATLAB Simulink, using dSPACE DS1104 digital controller board. Simulation results for eight different cases, ranging from balanced grid voltages to extremely unbalanced grid voltages and line impedances, are presented in CHAPTER V. The laboratory prototype along with the digital control algorithm implemented in dSPACE is presented in CHAPTER VI. Results obtained experimentally are in excellent agreement with those in the simulation. Conclusion and future work are presented in CHAPTER VII.

CHAPTER II

LITERATURE REVIEW

In the last few decades, a lot of attention has been dedicated to renewable energy resources, and as a result, a significant amount of publication on RES integration to the grid and inverter control has been submitted. This chapter will review the published literature by separating it into three sections, based on the reference frame used by the control method. Studies in [13-28] present control in dq rotating reference frame. The second group [29-40] implements control in a stationary $\alpha\beta$ frame. Control methods in a third section [41-47] utilize traditional abc reference frame. Some authors presented their methods using more than one reference frame, thus their work was generally placed into a section to which their control method contributed the most. Other non-cartesian frames are also used but those are not very common [48]. A summary on the presented literature is given at the end of this chapter, while the proposed method of this thesis, and the studies on which it is based on are also introduced.

2.1 DQ Reference Frame

This section reviews studies in [13-28] that primarily present their control method in *dq* reference frame. This frame in general, proves to be a good solution for linear controllers, such as PI, and works well under balanced or slightly unbalanced grid conditions. While this rotating frame has its benefits, it is usually associated with computational burden caused by frame transformations, PLL delay, and controller's inability to eliminate steady-state error under more severe unbalanced conditions.

Authors in [13] summarize several control strategies, which involve sequence component decomposition, and describe how PI control is typically used in PV/Hybrid inverter systems in grid-forming, grid-supporting, and grid-parallel feeding modes, under balanced and unbalanced loads. It is shown that in grid-forming mode, inverter voltage and current is controlled to meet the demands of the changing load, whereas in grid-supporting mode, inverter power (active, reactive or both) is controlled to meet the demand of grid power requirements.

Hysteresis control of the inverter, connected in back-to-back configuration to a rectifier, driven by a PMG wind turbine is presented in [14]. Negative sequence current is injected into the grid under unbalanced voltage, with unacceptable THD. This negative current is suppressed after sequence component decomposition using improved PLL method. Only one slightly unbalanced case was presented.

Reference [15] presents SPWM control, while controlling positive and negative sequence components independently. The authors include a more severe unbalanced case (SLG fault) in this study, however the method balances the AC-line currents at the expense

of DC-link 120-Hz ripple. If the DC-link ripple is eliminated, the line currents become unbalanced.

Authors in [16] present PWM control of active and reactive power separately, which is pushed into the grid under a Type "B" fault in one phase (20.5% voltage unbalance). Zero sequence component does not exist, since there is no neutral line, but the 100-Hz pulses are filtered out by a notch and a low-pass filters that introduce delay. Both, positive and negative sequences are controlled with dual current controller (DCC), and while the output current is relatively sinusoidal, the active power pulsations are minimized at the expense of reactive power oscillations.

Since multiple feedback loops oftentimes cause delay in DSP, a new observer-based disturbance-estimation control algorithm was proposed in [17] as a remedy, designed for systems with limited current-controller bandwidth with reduced PWM switching frequency. Type C voltage unbalance event was used for testing with switching frequency of 5 kHz. With the proposed compensator, 120-Hz ripple on the DC link was suppressed, but again at the expense of the increased unbalance on the output currents. Closed-loop observer was developed in z-domain, with total computational time of 15 μs.

Extended Direct Power Control (DPC) with Space Vector Modulation (SVM) using constant switching frequency was proposed in [18]. Three separate controls for active, reactive, and DC voltage are executed in *dq* frame. Two additional compensation modules were used. Voltage dips compensator, eliminates the 100 Hz component on the DC-link with a notch and a low-pass filter in series. The method converts between $\alpha\beta$ and *dq* frames several times. Higher harmonics current compensator eliminates the output current harmonics and meets the grid code standards, but only one case at unity PF was shown.

Traditionally, negative and positive sequence components are regulated in one SRF, typically positive (counterclockwise). Authors in [19] proposed a dual current control scheme, where negative sequence current is regulated by PI in negative SRF and positive sequence current is regulated by another PI in positive SRF, since both appear as DC quantities. Since low-pass filter causes instability and limits control bandwidth, a notch filter was used instead in each SRF, to filter out the 120 Hz component, present from the positive sequence current in negative SRF, and from the negative sequence current in positive SRF. Compared to traditional PI, the quality of the DC link voltage and output currents were improved, and although real power (P) can be adjusted, reactive power (Q), though without a dc component, still oscillates and can't be controlled, hence PF can't be fully adjustable either. No cases with severe unbalance were tested in this study.

Authors in [20] proposed a robust feedback linearizing control with sliding mode compensation. A PV system was integrated to a grid via inverter and was tested during balanced and unbalanced grid conditions. DC-DC converter was designed to control the dc-link voltage, and active and reactive power of the inverter is controlled by controlling the d and q components of the output current. It was shown by PQ theory, that under grid faults, instantaneous active and reactive powers contain 2^{nd} order oscillating terms, which are eliminated, and only average values of P and Q are controlled. The proposed method is compared with conventional PI control, and proven to be superior during uncertainties, and although P and Q responded well to reference commands, grid currents were distorted.

A PV system with inverter is also presented in [21], utilizing active disturbance rejection control (ADRC) strategy based on the virtual synchronous generator (VSG). With the increase of DG based on RES, the stability of the grid has been of a concern due to the

absence of synchronous machines, which provide inherent rotor inertia and damping characteristic to support the stability of grid frequency. Thus, a new concept of VSG has been proposed, where a short-term energy storage along with suitable control will emulate a real synchronous machine. Dual closed-loop PI feedback decoupling control has been implemented. ADRC improves PID control due to its ability to handle disturbances better. Similar to [20], the oscillating components of controlled variables (power and current) were suppressed, while VUF represented a 20% drop in one phase. Based on the simulation results, power fluctuations in both active and reactive power are only reduced but not eliminated. No traces of output current have been shown either.

An improved inverter control under unbalanced voltages while comparing its main advantages to the classical control techniques has been presented in [22]. The proposed method uses delay signal cancellation block in PLL loop (used for synchronization) to differentiate between positive and negative sequence voltage, and in current loop to mitigate negative sequence current. The improved PLL has an additional resonant loop while the currents are controlled with PI controllers. The proposed strategy was experimentally verified under various asymmetrical voltage conditions at the PCC, including grid voltage phase shifts, one phase voltage swell of 10%, and severe type E fault (two-phase voltage sag of 40%). While the proposed method was able to show superiority compared to classical control under various conditions, the attention was concentrated on the output currents, which for the most part were sinusoidal (the negative sequence component was mitigated), but at the same time the issue of oscillating active and reactive powers was still apparent.

Similar to [19], authors in [23] proposed a strategy for controlling active and reactive power oscillations with double sequence frame current regulators, where two frames are rotating in opposite directions, hence both positive and negative sequence components become DC quantities. The proposed strategy can eliminate either real or reactive power oscillations, or balance the output currents under unbalanced grid. Experimental results test the proposed strategy under varying resistive-inductive impedance, while the power is injected to the grid by the inverter at different PF. While the given method is able to separately control the average value of active and reactive power injection, double frequency oscillations in one or the other are still present, and the grid currents can only be balanced at the expense of these oscillations.

Reference [24] uses an internal model-based current controller, with a linear matrix inequality approach to optimize the feedback gains, and a state estimator to reduce the number of current sensors. Authors incorporate a moving average filter (MAF) concept to address inaccuracy issues of PLL during grid unbalance, and a phase lead compensator is used to improve the response time. Experimental results include 80% voltage sag in Phase C, and the proposed method is compared against other PI-based strategies. While the proposed method shows its effectiveness in both dynamic and steady-state response, and the output current quality satisfies the harmonic limits according to IEEE 1547 standards, the method is complicated in design, and borders with marginal stability when considering grid impedance variations.

In contrast to a conventional PI controller, a Proportional (P) controller is proposed in [25], with first order low-pass filter disturbance observer to control positive and negative grid current sequence components independently, under asymmetric grid unbalance. One

of the advantages of the proposed controller is that it is insensible to grid parameter variations. Double frequency power oscillations are eliminated by injecting the appropriate negative sequence currents. Four different simulations showed how the negative sequence current and double frequency power oscillations were controlled and finally compared the proposed strategy to the conventional PI-controller. The new method showed better dynamic performance, and successfully eliminated oscillations in active power, however the reactive power was not controlled and still contained oscillations. Also, voltage unbalance was only 30% in Phase A, with only simulation results presented.

Reference [26] aims to compensate harmonic current when GCI is connected to the unbalanced grid without the use of compensation devices (active or passive filters). The proposed control method uses PI control that contains two units: active/reactive power control unit, and harmonic current compensation unit. Simulation results include three DG units connected at PCC: a PV, a microturbine, and a fuel cell, all connected to the grid via inverter along with two other nonlinear loads. The authors compare three strategies: one without any compensation devices, another with APF and distributed PFs, and finally one without any compensation devices (APFs and PFs) but only with the proposed control strategy implemented on the PV. Simulation results show that harmonic currents, caused by nonlinear/unbalanced loads, are successfully eliminated with the new strategy, while active/reactive power injected into the grid is successfully controlled. Even though the proposed method shows superiority over traditional active and passive filter compensators, no grid faults were studied, but only unbalanced/nonlinear load was simulated.

A novel unified voltage correction strategy on ESS (DC Energy Storage System), connected to the microgrid at PCC via inverter along with other unbalanced loads and a

single-phase PV DG is presented in [27]. A PCC switch is closed, connecting the microgrid to the utility grid based on the allowed amount of voltage unbalance per grid code, and opens if the limit is exceeded. The proposed strategy is tested in both grid-connected and in islanded modes. In both cases, the proposed control on the ESS inverter successfully eliminates negative-sequence currents and balances MG's unbalanced voltages, however only slight level of unbalance was tested (VUF of 7%).

Finally, [28] presents an improved CSI topology with added buck chopper at the DC-link, and a PIR controller (rather than notch filter) on a PV system, to suppress 2nd order DC-link currents and negative sequence components of grid currents under symmetrical/asymmetrical grid unbalance. The proposed method rightly shows how conventional CSI control cannot handle serious voltage sags that cause instability, and how the proposed method overcomes these issues, however the unbalanced case shows only 20% voltage sag in two phases for the asymmetrical case. Moreover, no power traces or power factor adjustability were shown.

2.2 Alpha-Beta ($\alpha\beta$) Reference Frame

Authors in [29-40] presented their control mostly in the stationary $\alpha\beta$ frame. Compared to the rotating dq, this frame does not carry the extra delay associated with the transformation, and the control is relatively easy to implement. PR controllers are commonly used in this frame since PI controllers struggle to get rid of the steady-state error. While PR controllers are tuned to various resonant frequencies with the intent to eliminate them, they sometimes struggle with stability, which adds complications to the design and to the output quality.

Reference [29] presents model predictive control on a four-leg inverter, but focuses primarily on protecting DER during severe grid faults, thus the strategy is not concerned with the output power quality.

A single-stage PV system, operating at MPPT, using predictive current control during unbalance voltage sags and swells is presented in [30]. The proposed strategy controls active and reactive power delivered to the grid, however reactive power is oscillating, and the output currents are not sinusoidal as well.

A simple control on a two-stage PV inverter, operating at MPPT, based on PQ theory, is presented in [31]. Two different nonlinear load cases are considered in the study, with first requiring less power than provided by the solar panel, hence no extra grid power is necessary, and second requiring more power, hence drawing the remaining demand from the grid. The proposed method demonstrates how active and reactive power is delivered to the unbalanced load while maintaining grid balance, however, only balanced grid cases are considered in this study.

Reference [32] uses two PR controllers on a two-stage PV inverter as well, but proposes to operate below MPPT under severe faults in order to limit the injected currents and not allow them to exceed their maximum rating. The proposed strategy successfully provides sinusoidal output currents (within 5% THD requirement), and eliminates double grid frequency from active power, while keeping the injected current from exceeding its limits under severe faults. Nevertheless, the reactive power is still oscillating.

A new control scheme with multifrequency PR controller is proposed in [33] to improve steady state dynamic response under several unbalanced conditions, including varying load impedance, LVRT, and SLG fault. The method showed to have better FRT

compared to traditional dual PI control in terms of steady-state and transient operation. DC-link double frequency is eliminated, but control is more complicated, using several domains. While improvements with varying impedance were shown, the output current quality wasn't good during SLG fault.

Direct Power Control (DPC) on back-to-back rectifier-inverter system, is presented in [34], where instantaneous active and reactive powers are controlled by bang-bang controller, following the appropriate switching state tables. The output currents seem to be well regulated, but only a small case with unbalance ratio of 7.32% was shown, and it wasn't demonstrated that both active and reactive power could be controlled separately.

Authors in [35] presented a new vector-based hysteresis current control (HCC) for the inverter. Even though HCC control is simple, and has fast transient response, its drawback is the high switching frequency. Thus, a multilevel comparator, integrated with a switching table, designed to keep the current error in an assigned tolerance, is proposed to limit the switching. Conventional three-phase HCC, along with three other HCC methods are compared. Simulation shows that a proposed method significantly reduces the switching frequency, while being able to track highly non-sinusoidal command signal, but no real unbalance examples with adjustable power control were demonstrated.

A control scheme on GCI with a robust multiloop current controller, dual-sequence hybrid voltage controller, and active power controller, interfaced to the grid with LCL filter, is proposed in [36]. Presented control provides wide-band damping against grid unbalance, and responds well to its fast and dynamic disturbances. Experimental results compare this method with proportional harmonic resonant controller. They include two loads at the PCC: a dynamic load (an induction motor) and a variable static load. Under

heavy unbalanced loading that caused 8.9% voltage unbalance, the double power-frequency oscillations of the negative sequence component of the grid voltage are regulated to zero and positive sequence component is constant. No testing under extreme unbalance was conducted in this study.

Authors in [37] proposed a new stationary frame strategy to control power oscillation and current harmonics without a need of PLL when inverter is connected to the unbalanced grid. It is shown theoretically (with PQ-theory) and verified with simulation, that the inverter current is not sinusoidal (contains double frequency) when the reference inverter output active/reactive powers are constant. Hence, the double frequency harmonics in the current are eliminated with a notch filter, but power fluctuations appear as a result, which also oscillate at twice the fundamental frequency. PR controller was used to regulate inverter low-order current harmonics. This study demonstrates a tradeoff in oscillations between the output current and the output powers, under slightly unbalanced conditions.

Two strategies to compensate unbalanced grid voltage under various unbalanced loads are discussed in [38]. One strategy minimizes active power oscillation, and the other controls negative sequence current to be in-phase with grid's negative sequence current. Experimental results are conducted with inductive and weak grid, under various DG's active and reactive output powers. While presented strategy showed how output current and active/reactive power can be controlled under various conditions, power oscillations never go away despite the minimization strategy.

Reference [39] investigates a strategy, where a 4-wire inverter supports the local grid voltage during unbalance, caused by nonlinear load, while regulating active power injection. The first loop controls active power injection by controlling the output current

fundamental positive sequence component. The other loop corrects the local voltage at PCC by controlling its negative and zero sequence components and the harmonics. The system is modeled together with the LCL filter, while harmonic resonant filters (PR) are tuned to compensate for each harmonic. It is shown how current control, harmonic compensation, and voltage unbalance correction, each contribute to the output current THD and VUF reduction. While the design of the controller is complicated, only unbalanced load case is considered in this strategy and no general grid unbalance is discussed.

Finally, authors in [40] present a single-stage PV inverter connected to the grid with LCL filter, and propose PR control in $\alpha\beta$ frame, while comparing it to three other control strategies: PI control in *dq* ref. frame, PI control in dual *dq* ref. frame, and active damping compensation control. Authors address important questions of elimination of double frequency oscillation in active and reactive power and in negative sequence output current during grid voltage dip. To address PLL insufficiencies under unbalanced grid, a sliding Goertzel filter is used to eliminate oscillations caused by negative sequence components. Grid voltage feedforward control algorithm is designed to address transient current spike caused by sudden grid voltage drop. Simulation and experimental results showed that the proposed PR method successfully eliminates power and negative sequence current oscillations during grid faults, however the most extreme case depicts only a 30% drop in one phase.

2.3 ABC Reference Frame

Authors in [41-47] presented their control methods in *abc* reference frame. This frame is relatively simple in implementation, and requires no transformation and no

sequential component extraction that leads to a lot of online calculations. Control in this frame, such as sliding mode, deadbeat, or hysteresis oftentimes provides fast response and good stability. While there are many benefits in this frame, it is oftentimes associated with bandwidth limitations and high switching losses.

A sliding-mode control (SMC) strategy for grid connected inverter with LCL filter in *abc* frame is proposed in [41]. Sliding surface functions of only two phases are controlled, which eliminates the need for extra sensor for a third phase. Capacitor voltage references are generated by PR controllers, which remove the steady-state error of the line current. The performance of the proposed control method was also tested in the rotating *dq* frame and the results are compared under various unbalanced conditions. It was concluded that SMC in natural frame had better THD, and was simpler since it doesn't require transformations, however the unbalanced case represented only a 10% drop in one phase, hence the method wasn't tested under severe unbalanced conditions.

Reference [42] presented a current controller in *abc* frame based on H-infinity and repetitive control, on an inverter with LC filter connected with grid interface inductor L (essentially LCL filter). The main objective of this control is to inject low THD current into the grid in the presence of unbalanced, nonlinear loads with grid-voltage distortions. The proposed method was compared with traditional PR, PI, and predictive DB (deadbeat) control. Experimental results show that the proposed method outperforms traditional methods in terms of output current quality, however the method suffers from slow dynamics. Moreover, the study only considers unbalanced/nonlinear loads, and no significant grid voltage unbalance is tested.

Authors in [43] proposed to control both active and reactive powers from RES with a nonlinear Lyapunov function-based controller in parallel with a spatial repetitive controller (SRC) to estimate and effectively deal with steady-state and transient grid periodic disturbances. Because the method is in *abc* frame, no PLL is needed, hence no transformations, no extra online computation and extra delay is added. VSI is interfaced to the grid with line inductors. A nonlinear capacitive load is connected at the PCC, and the output line currents are regulated. Proposed control is compared with traditional multiple PI + cascaded PR controller, and shows superiority in many aspects, especially in its separate active and reactive power control, and its ability to provide sinusoidal grid currents under grid unbalance, while still compensating for the nonlinear current delivered to a nonlinear load. Current references are calculated based on PQ theory. Nevertheless, the unbalanced grid voltage represented only a 20% negative sequence contamination, hence the method was not shown to be working for all levels of unbalance. Also, there were some undesirable transients observed in line currents when grid frequency was changed. The validity of this method is also presented with a 4-switch inverter topology in [44].

A new *abc* frame complex coefficient filter and controller to control inverter current under unbalance is presented in [45]. With the proposed strategy, the fundamental negative sequence component of grid voltage is eliminated, and the higher harmonics are also attenuated. The method is simple and does not need frame transformations. Experimental results show that under 30% VUF and 5% THD of grid voltage, output currents don't contain the unwanted harmonics, and pass the 5% IEEE 929-2000 standard. However, the study does not demonstrate the method's ability to control active or reactive power, and no severe grid unbalance was used in the study.

A new deadbeat (DB) controller in parallel with a hybrid multi-resonant (RC) controller on a four-legged inverter is proposed in [46]. Such control offers fast dynamic response, good stability and a low computational burden. RC helps with decreasing of the steady-state error that DB controller can't handle. The additional forth leg has some advantages but most experimental results deal only with unbalanced loads. As previous studies, the proposed control method wasn't tested under severe unbalanced grid conditions, and did not demonstrate independent power control.

Finally, a hysteresis controller in *abc* frame, also on a four-legged inverter, is proposed in [47]. The inverter was operated in various modes with highly nonlinear load at PCC. In the first operating mode, the inverter was controlled as a shunt APF, where all active power to the load was provided by the grid, but the inverter provided load reactive power demand while compensating current unbalance and load current harmonics. In another mode, the inverter provided active power while maintaining the output power filtering. If the active power of the inverter exceeded the demand of the load, the excess power was injected to the grid at unity power factor with quality sinusoidal grid currents. Such control is valuable, yet again, only unbalanced load conditions were investigated, without considering unbalanced grid.

2.4 Literature Summary

While the papers above present various strategies for inverter control under grid or load unbalance, with attempts to eliminate harmonics and to control power flow, using different reference frames, some general statements can be made regarding the shortcomings in the reviewed literature:

a. Only balanced grid is assumed.
b. Voltage unbalance is small. Methods work under slight unbalance but run into quality/stability issues or bandwidth limitations when the unbalance is severe.
c. Harmonics are minimized but not completely eliminated.
d. One variable is controlled at the expense of undesired oscillations in another.
e. Only certain quantities can be controlled (active or reactive power, or output currents, but usually not all). Thus, the method is not general, and PF can't be adjusted to any desired value.
f. Either active or reactive power or both oscillate at double grid frequency, and if neither oscillate, the injected currents are not sinusoidal.
g. Sequential component extraction, complicated controller design, and multiple control loops require lots of online calculations and cause extra delay.
h. Control techniques are difficult to implement in real-time.

In contrast to these shortcomings, the proposed method in this thesis overcomes many of them, and provides fast response and good stability, while operating under various severe unbalanced conditions, in both, grid voltages and line impedances. The method effectively eliminates current harmonics, provides bi-directional and oscillation-free power flow, with fully adjustable power factor (PF). It can easily be implemented in real time, in natural *abc* frame, and no extra transformations, sequential component extractions, that require a lot of online calculations, is necessary.

2.5 Intro to the Proposed Method

The control method used in this thesis was first introduced by Stankovic and Lipo in [49], and later was experimentally verified on a rectifier, using DSPACE controller and Lab-Volt test bench by Ke Chen in [50] and [51]. Upadhyay continued the work of Chen and modified the method using constant switching frequency in [56], however ran into the issue of limited bandwidth of DSPACE controller. Krishnan used a faster C2000 Delfino controller to show the validity of this method in [57]. The proposed method has been experimentally verified to work well on a rectifier. Simulation work on the inverter, driven by a wind turbine has also been presented in [53] and [54].

This thesis builds primarily on references [49-52] and [55] and provides experimental verification of the inverter control. It is based on hysteresis control that compares the actual current with its calculated reference value. The states of the six switches are changed based on the error between the two signals. The width of the hysteresis band determines the maximum deviation the actual currents can have from their references. In this thesis, both simulation and experimental work on the inverter has been presented.

While this method has many advantages compared to the ones reviewed earlier in this chapter, it is certainly not without limitations, and these are listed as follows:

a. Variable switching frequency is used. This causes EMI and adds difficulties to filter design.
b. Power loss due to high frequency switching.
c. A constant DC source is assumed at the DC link, hence the effect of the unbalanced grid on the DC-link capacitor is not studied.

d. Unbalanced conditions are pre-determined ahead of time, hence initial conditions of the unbalance are not studied.

The issue of variable frequency was addressed by references [56] and [57] on the rectifier side, so the future work after this thesis might follow a similar path on the inverter. The power loss was observed to be improved with IGBT unit, however at the time of working on this thesis, only MOSFET unit was available. Finally, even though a constant DC power supply was used at inverter's input, simulation studies in [53] and [54] have demonstrated that the control method is effective at keeping the DC link capacitor voltage relatively constant with very minimal ripple.

CHAPTER III

PROPOSED CONTROL METHOD

Harmonic elimination with adjustable power factor is achieved by generating unbalanced reference commands for grid currents under unbalanced grid voltages and line impedances. Fig. 6 and Fig. 7 show the grid side inverter and its per phase equivalent circuits respectively under unbalanced operating conditions.

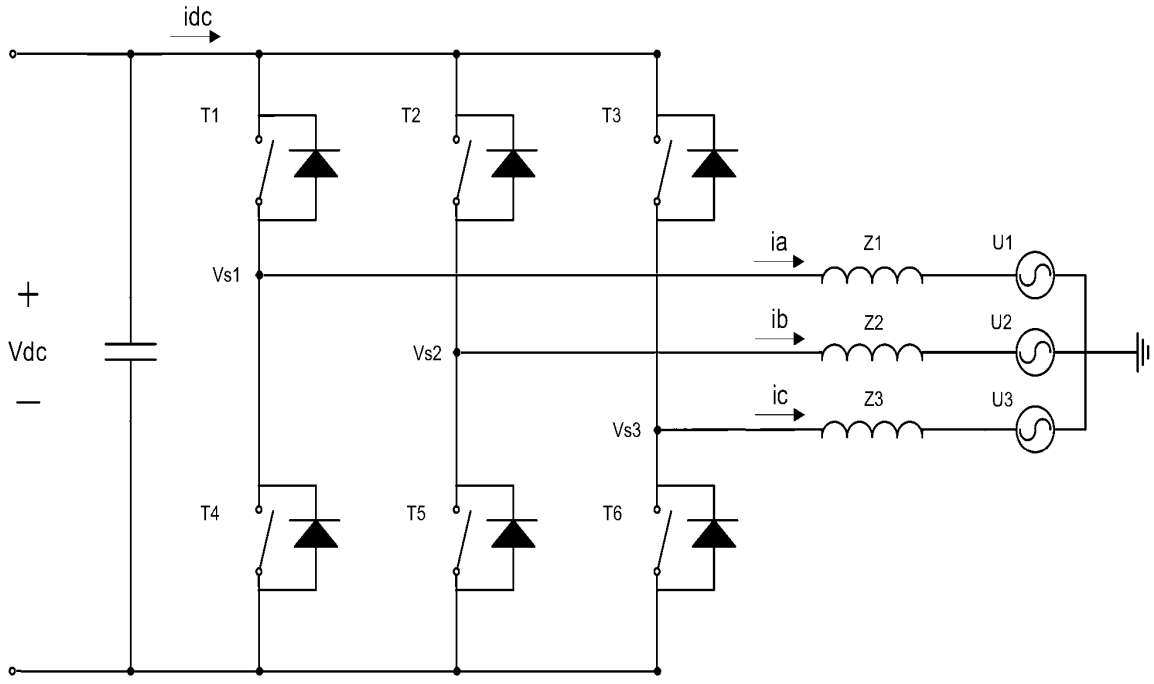

Figure 6: Grid Side Inverter.

3.1 Theoretical Analysis

Under unbalanced operating conditions, both grid voltages as well as line impedances have to be considered unbalanced. From Fig. 7(a), (b), and (c), three phasor equations for three phases are obtained and given by,

$$U_1 = -z_1 I_1 + V_{s1} \tag{1}$$

$$U_2 = -z_2 I_2 + V_{s2} \tag{2}$$

$$U_3 = -z_3 I_3 + V_{s3} \tag{3}$$

where U_1, U_2, and U_3 are grid side voltages, z_1, z_2, and z_3 are line side impedance, and I_1, I_2, and I_3 are grid side currents. V_{dc} is the DC link voltage, V_{s1}, V_{s2}, and V_{s3} are synthesized voltages at the output of the inverter, and SW_1, SW_2, and SW_3 are the switching functions. All quantities are represented as phasors. V_{s1}, V_{s2}, and V_{s3} can also be expressed as:

$$V_{s1} = SW_1 \frac{V_{dc}}{2\sqrt{2}} \tag{4}$$

$$V_{s2} = SW_2 \frac{V_{dc}}{2\sqrt{2}} \tag{5}$$

$$V_{s3} = SW_3 \frac{V_{dc}}{2\sqrt{2}} \tag{6}$$

By substituting equations (4), (5), and (6) into (1), (2), and (3), the following equations are obtained and expressed as:

$$U_1 = -z_1 I_1 + SW_1 \frac{V_{dc}}{2\sqrt{2}} \tag{7}$$

$$U_2 = -z_2 I_2 + SW_2 \frac{V_{dc}}{2\sqrt{2}} \tag{8}$$

$$U_3 = -z_3 I_3 + SW_3 \frac{V_{dc}}{2\sqrt{2}} \tag{9}$$

By multiplying equations (7), (8), and (9) by I_1, I_2, and I_3 respectively and adding them up, the following equation is obtained and given by,

$$U_1 I_1 + U_2 I_2 + U_3 I_3 =$$

$$= -z_1 I_1^2 - z_2 I_2^2 - z_3 I_3^2 + \frac{V_{dc}}{2\sqrt{2}}(SW_1 I_1 + SW_2 I_2 + SW_3 I_3) \quad (10)$$

The steady state solution for the harmonic elimination under unbalanced operating conditions is given by,

$$SW_1 I_1 + SW_2 I_2 + SW_3 I_3 = 0 \quad (11)$$

$$U_1 I_1 + U_2 I_2 + U_3 I_3 = -z_1 I_1^2 - z_2 I_2^2 - z_3 I_3^2 \quad (12)$$

The complex conjugate power is given by,

$$S^* = -U_1^* I_1 - U_2^* I_2 - U_3^* I_3 \quad (13)$$

According to Kirchhoff's current law (KCL),

$$I_1 = -I_2 - I_3 \quad (14)$$

By substituting equations (14) into (13) and (12) we arrive at,

$$S^* = -U_1^*(-I_2 - I_3) - U_2^* I_2 - U_3^* I_3 \quad (15)$$

where $S = P + jQ$ represents complex power

$$I_2(U_2 - U_1) + I_3(U_3 - U_1) = -(z_1 + z_2) I_2^2 - (z_1 + z_3) I_3^2 - 2 z_1 I_2 I_3 \quad (16)$$

Equation (15) can be rearranged as:

$$I_2 = \frac{S^* + I_3(U_3^* - U_1^*)}{U_1^* - U_2^*} \quad (17)$$

By substituting (17) into (16), the solution for harmonic elimination with adjustable power factor is obtained and given by,

$$\frac{S^* + I_3(U_3^* - U_1^*)}{U_1^* - U_2^*}(U_2 - U_1) + I_3(U_3 - U_1) =$$

$$= -(z_1 + z_2)\frac{S^{*2} + 2S^* I_3(U_3^* - U_1^*) + I_3^2(U_3^* - U_1^*)^2}{(U_1^* - U_2^*)^2} +$$

$$-(z_1 + z_3) I_3^2 - 2 z_1 \frac{S^* + I_3(U_3^* - U_1^*)}{U_1^* - U_2^*} I_3 \quad (18)$$

Equation (18) can be rearranged as:

$$\left(-(z_1+z_3)-\frac{2z_1(U_3^*-U_1^*)}{(U_1^*-U_2^*)}-(z_1+z_2)\frac{(U_3^*-U_1^*)^2}{(U_1^*-U_2^*)^2}\right)I_3^2+$$

$$\left(-(U_3-U_1)-\frac{(U_3^*-U_1^*)(U_2-U_1)}{(U_1^*-U_2^*)}-2(z_1+z_2)\frac{(U_3^*-U_1^*)\,S^*}{(U_1^*-U_2^*)^2}-2z_1\frac{S^*}{(U_1^*-U_2^*)}\right)I_3$$

$$+$$

$$\left(-\frac{S^*(U_2-U_1)}{(U_1^*-U_2^*)}-\frac{(z_1+z_2)S^{*2}}{(U_1^*-U_2^*)^2}\right)=0 \qquad (19)$$

Current I_3 is obtained from the above quadratic equation.

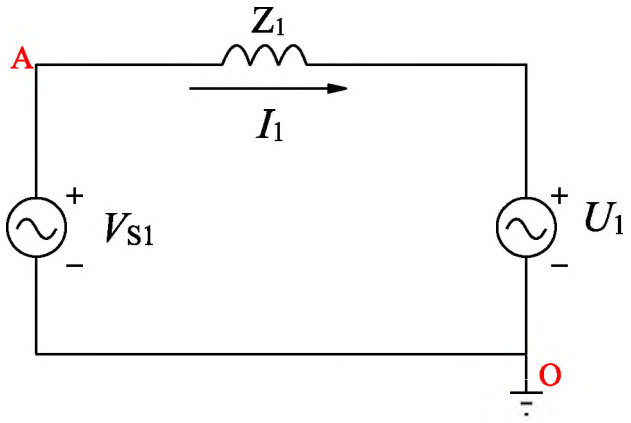

Figure 7(a): Per-phase equivalent circuit for Phase 1.

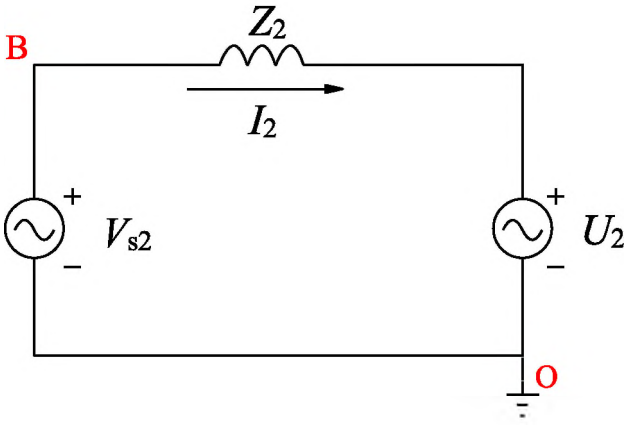

Figure 7(b): Per-phase equivalent circuit for Phase 2.

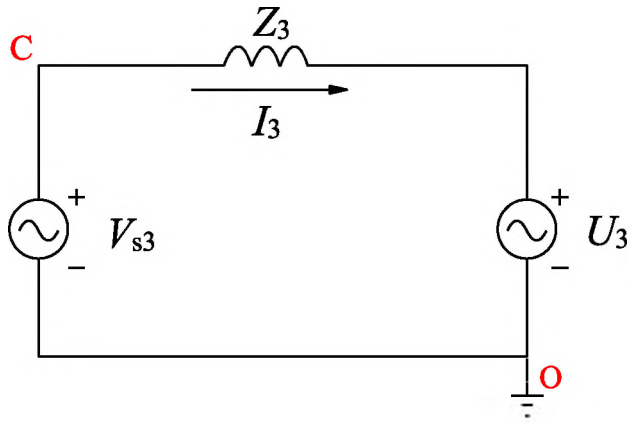

Figure 7(c): Per-phase equivalent circuit for Phase 3.

Equations (14), (17) and (19) represent the open loop steady state solution for harmonic elimination under generalized unbalanced operating conditions. Active and reactive power is adjusted by setting the value for $\boldsymbol{S}$ in equations (17) and (19). An analytical solution represented by equation (19) always exists unless all the coefficients of the quadratic equation are equal to zero. By setting the value for complex power in equations (17) and (19) the power factor under unbalanced operating conditions can be varied according to equation (20),

$$PF = \frac{P}{\sqrt{P^2+Q^2}} \tag{20}$$

where P and Q are active and reactive power. For the unity power factor operation, the reactive power should be set to zero in equations (17) and (19).

When impedances are balanced, and only the grid voltage is unbalanced, a maximum level of unbalance, for which the proposed solution still exists is given by the following constraint:

$$U_1 \neq 0, \qquad U_2 = U_3 = 0$$

$$z_1 = z_2 = z_3 \neq 0$$

Similarly, when the grid is unbalanced in both voltage and impedance, a maximum level of unbalance, for which the solution exists is also given by the constraint below:

$$U_1 \neq 0,$$

$$U_2 = U_3 = 0$$

$$z_1 = 0$$

$$z_2 \neq z_3 \neq 0$$

3.2 Control Method

Based on the analysis in the open loop presented above, a control method is proposed and shown in Figure 8. The line voltages U_1, U_2, and U_3, as well as line impedances z_1, z_2, and z_3 have to be measured. Based on this information and the set value for active and reactive power, P and Q, reference currents are calculated according to equations (14), (17) and (19), which become reference signals for the hysteresis controller.

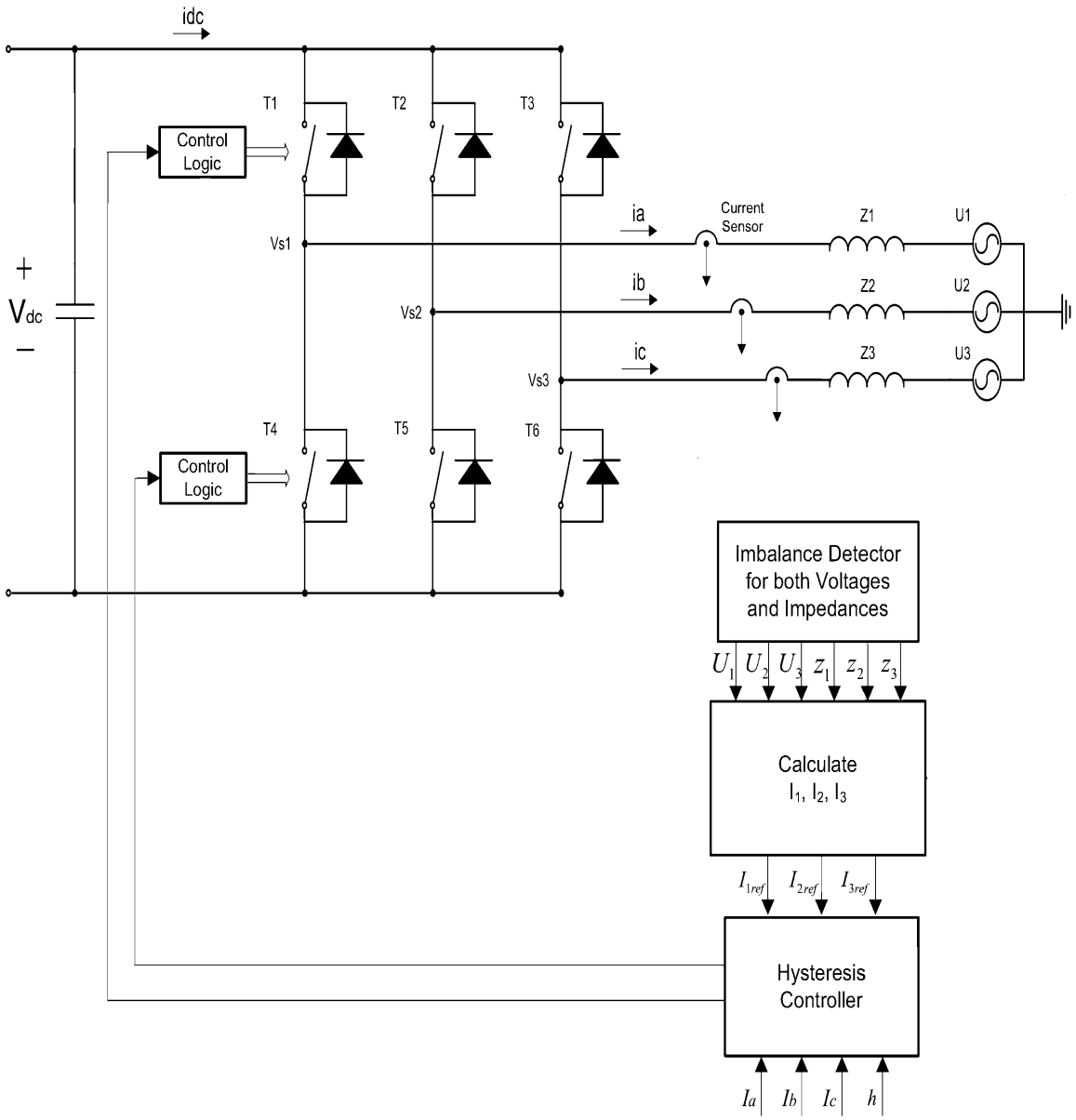

Figure 8: Proposed control of a GSI under unbalanced operating conditions.

In this control method, the DC link voltage is set to a constant value. Three actual output line currents are measured by current sensors, and are compared to the calculated current references by the hysteresis controller. The output of the controller is controlling the state of the inverter's switches, in such a way that the actual currents are tracking the references.

CHAPTER IV

IMPLEMENTATION

This section describes the implementation of the control method presented in the previous section. The majority of the implementation on the inverter is very similar to that of a rectifier, described in [50]. The proposed method has been implemented on a laboratory prototype with Lab-Volt test bench and dSPACE digital control board.

dSPACE DS1104 digital controller, along with MATLAB Simulink were used to build the control loop. The choice for DS1104 was made primarily because it is a cost-effective system for controller development. Also, being a single-board system (Fig. 9), with real-time hardware and comprehensive I/O interface, that can easily be installed in any PC with available 5V PCI slot, makes this controller a good choice.

Another advantage of the DS1104 Controller Board is its ability to run applications in real time. Real Time Interface (RTI) allows graphical I/O interface in Simulink. All I/O's can be configured graphically by inserting them into a Simulink block diagram. Real-Time Workshop Toolbox in Simulink converts the Simulink's block diagram into a real-time DSP code and downloads it to dSPACE controller's memory. The real-time model is compiled, downloaded, and started automatically. This reduces the implementation time to

a minimum, and the functions designed in Simulink are executed in real time on dSPACE controller board.

CP1104 Connector Panel, shown in Fig. 10, provides an interface between the host computer and the driving circuit using serial connectors, 16-bit A/D and D/A converters. Only A/D and D/A converters were needed to be used in this application.

Figures 11 and 12 provide a hardware and software configuration diagrams of dSPACE setup implemented with the control method respectively. Table I lists all the hardware equipment used. The blocks of software configuration diagram shown in Fig. 12 is discussed in detail in the following section.

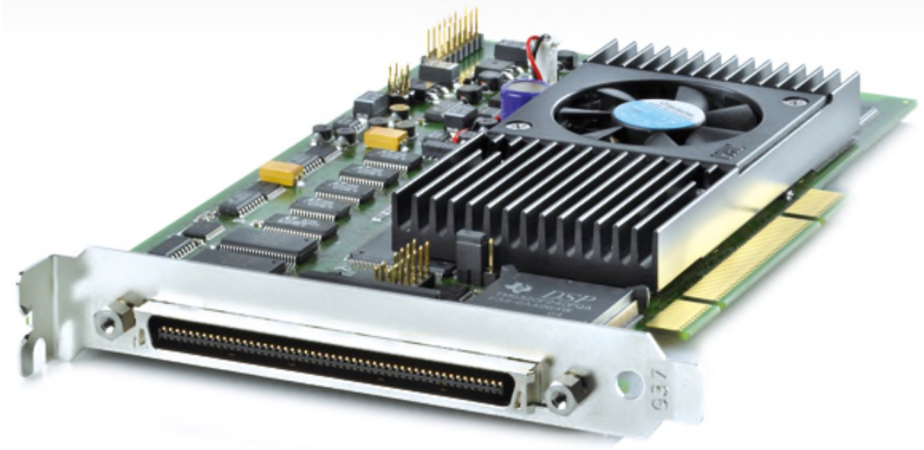

Figure 9: dSPACE DS1104 Controller Board, (dSPACE courtesy).

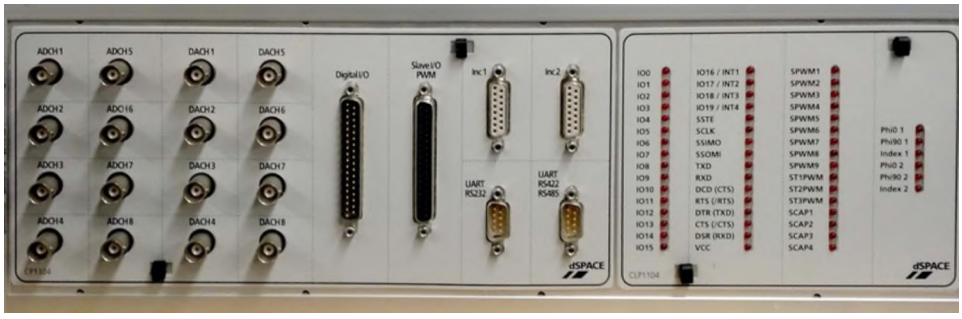

Figure 10: dSPACE CP1104 Connector Panel, taken from [57].

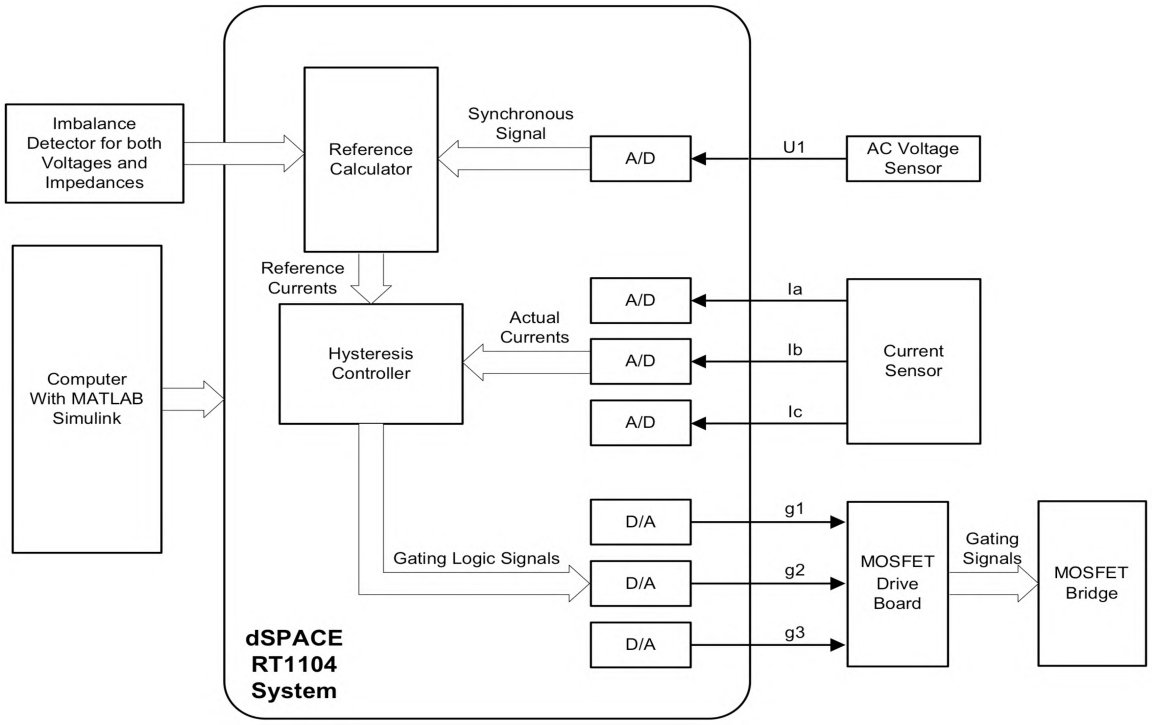

Figure 11: Diagram of Hardware Configuration, adapted from [50].

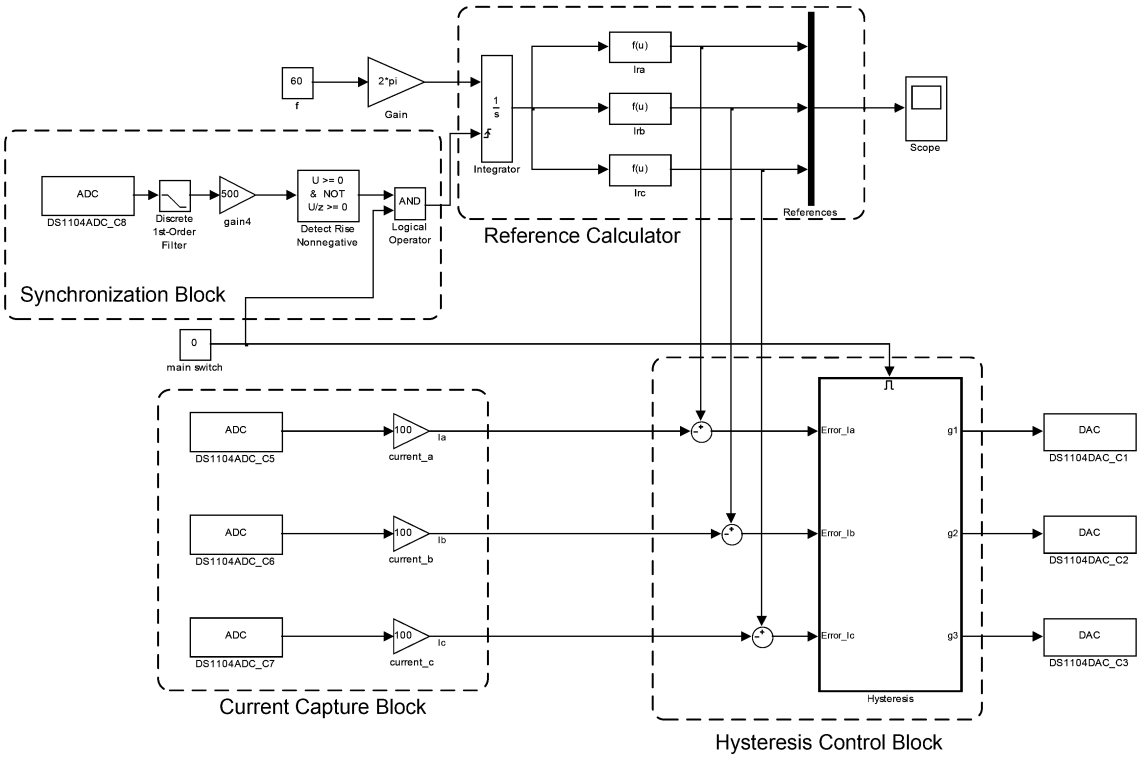

Figure 12: Diagram of Software Configuration, taken from [50].

TABLE I: LIST OF HARDWARE EQUIPMENT

Description	Manufacturer	Model
Voltage Sensor	Tektronix	P5200
Current Sensors (3)	Fluke	80i-110s
10 mH Inductors (3)	Hammond Reactor	195J20
AC Power Supply	Lab-Volt	8821-20
DC Power Supply	Instek	SPS606
MOSFET Drive Chip (3)	International Rectifier	IR21091S
Controller Board	dSPACE	DS1104
Connector Panel	dSPACE	CP1104
MOSFET Inverter	Lab-Volt	8837-00
Oscilloscope	Tektronix	TDS2014

The DC side of the inverter bridge is connected to a 60 VDC power supply in parallel with the DC-link capacitor. The bridge consists of six MOSFET switches with six antiparallel diodes, controlled by six different gating signals. Each phase of the AC side of the inverter is connected to a 10mH inductor (one for each phase), and to a three-phase AC voltage source.

4.1 Synchronization

One voltage sensor is used as a zero-crossing detector, which synchronizes the control signal with the AC voltage. The signal is reset every cycle to avoid possible phase shift caused by small frequency deviation. Small filter capacitor is connected in parallel with the detector to eliminate high frequency noise to avoid unwanted resets.

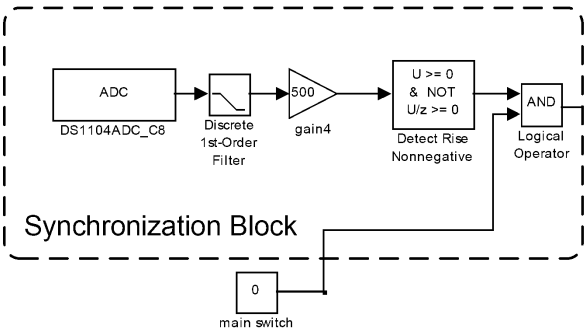

Figure 13: Synchronization Block.

Voltage sensor measures Phase A voltage of the AC power supply and connects to one of the A/D channels on the connector panel. The scale factor of 1/50 is used on the sensor so that the limit of ±10V on A/D channel is not exceeded. DS1104ADC_C8 block in Simulink acquires this signal as a digital value and sends it through a low-pass filter to eliminate unwanted noise (Fig 13). After multiplying it by a large gain (i.e. 500), the following block looks for a rising edge in the signal. When this condition is met, and the main switch that enables the Hysteresis Controller is ON, the logical AND gate is outputting a "1", which resets the reference currents.

4.2 Current Acquisition

Three current sensors are used to measure the actual currents on the AC side of the inverter. A scale factor of 1/100 is used on each sensor before they are connected to three A/D channels on the connector panel. Blocks DS1104ADC_C5, C6 and C7 in Simulink are used to acquire the digital signal of the current in each phase (Fig. 14). Currents are multiplied by a gain of 100 to compensate for the scaling factor used on the current sensors before the conversion, and are compared with the reference currents generated by a Reference Calculator Block discussed next.

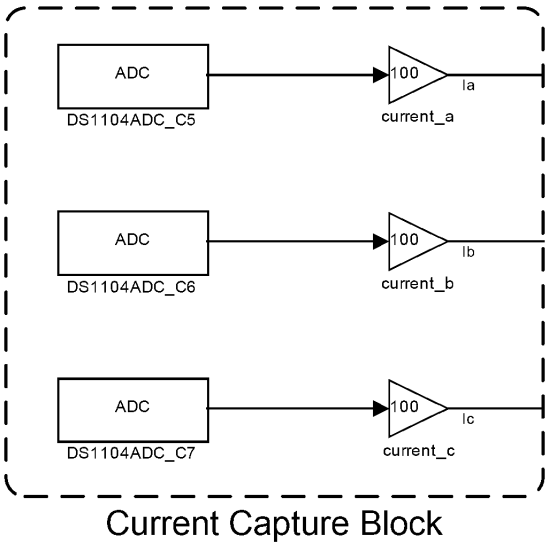

Figure 14: Current Capture Block.

4.3 Reference Calculation

To obtain the values of the reference currents, line voltages as well as line impedance are measured or predetermined and entered in the MATLAB's m-file. Based on this information and the set value for active and reactive power, P and Q, the magnitudes and phase angles of the reference currents are calculated according to equations (14), (17), and (19). It takes about 14 μs to obtain these values. The obtained magnitude and phase angle of current in each phase is sent to three f(u) function blocks in the Reference Calculator. Three-phase reference currents are calculated according to the following equations:

$$I_a = A_a \, sin \, (\omega t + \theta_1)$$

$$I_b = A_b \, sin \, (\omega t + \theta_2)$$

$$I_c = A_c \, sin \, (\omega t + \theta_3)$$

where $\omega = 2\pi f$. Since AC voltage source depicts the grid,

$$f = 60 \, Hz$$

Fig. 15 shows how three reference currents are generated by a Reference Calculator block in Simulink.

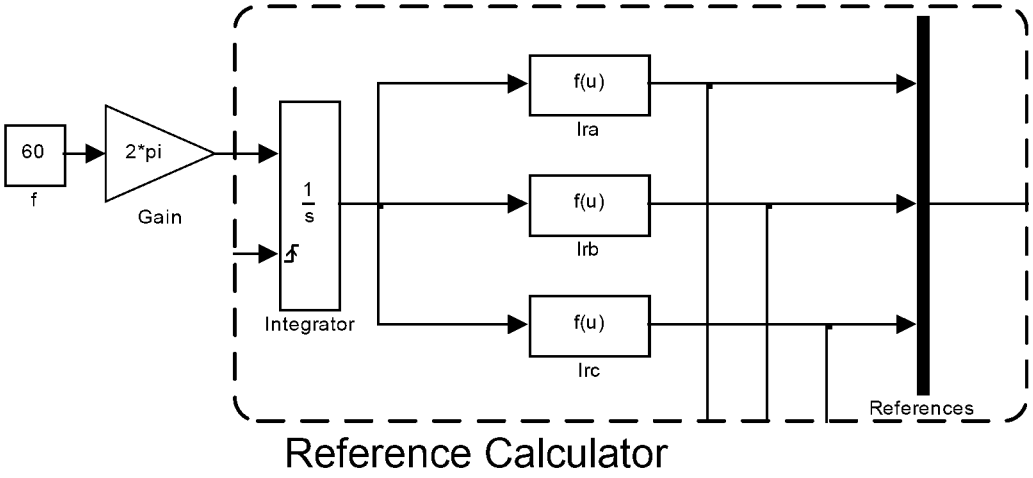

Figure 15: Reference Calculator Block.

4.4 Hysteresis Controller

A hysteresis controller block, shown in Fig. 16 is used to compare the actual currents with the reference currents. Once the main switch is enabled, the hysteresis controller starts working and the error between the actual and the reference current is interpreted as a "high" or a "low" signal. Fig. 17 shows how three independent hysteresis controllers work, where if the reference current is greater than the actual current the controller outputs a "1", and if the reference current is less than the actual current the controller outputs a "0". The same is true for all three controllers, which work independently for each phase. Signals from g1, g2, and g3 are sent to DS1104DAC_C1, C2 and C3 blocks respectively, after which they are converted to analog signals (0 or 5 V), and are sent to the MOSFET Drive Board from the three analog channels on the connector panel.

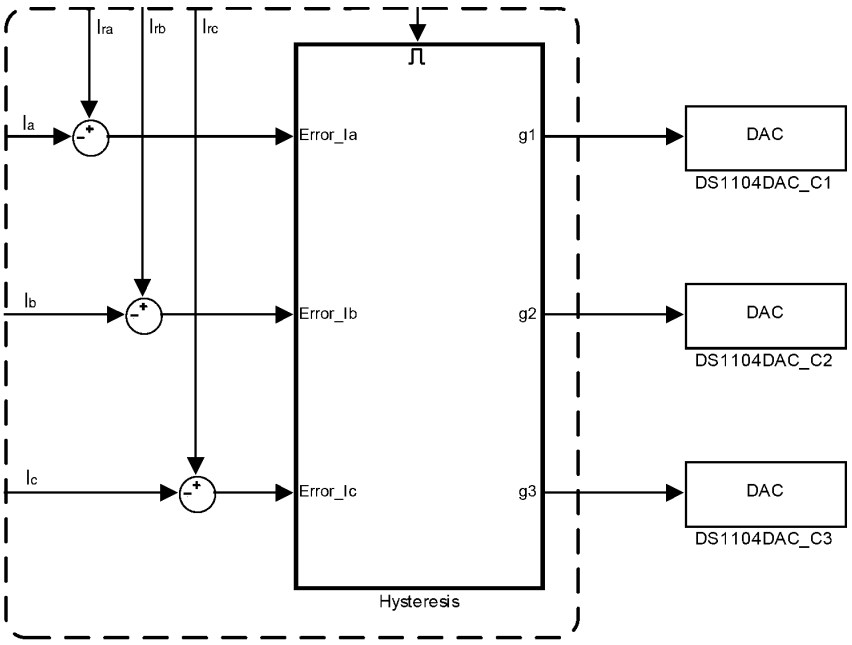

Figure 16: Hysteresis Block.

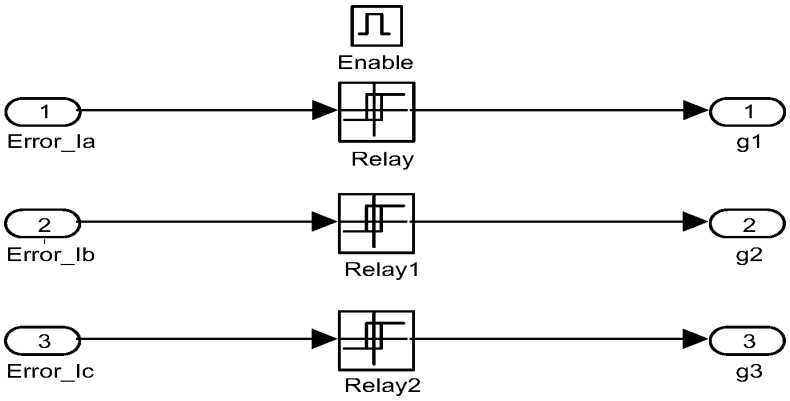

Figure 17: Hysteresis Controller.

4.5 Drive Board

MOSFET drive board is designed with three IR21091S drive chips, shown in Fig. 18, where each driver controls two switches in one leg of the converter. The chip provides two logic signals (0 and 5V) at the output in such a way that whenever one signal is 0V, the other is 5V and vice versa.

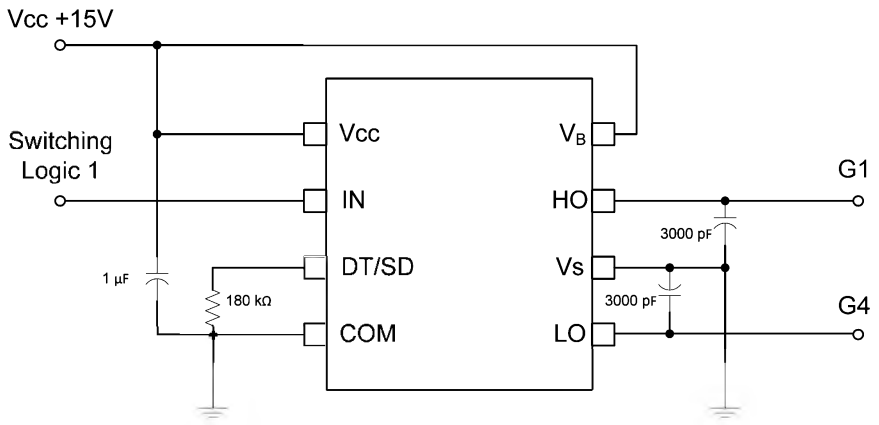

Figure 18: Control chip to drive one leg of the MOSFET Inverter, taken from [50].

MOSFET driver chip has a programmable dead time at the transient of switching, that prevents the two switches in one leg from conducting at the same time. The definition of dead time switching is shown in Fig. 19, and can be simply viewed as a safety time delay after a change in input signal, before the control system processes it and starts responding. The required minimum dead time for MOSFET inverter switching is 1200 µs. A resistor of 180 kΩ is selected to satisfy this requirement.

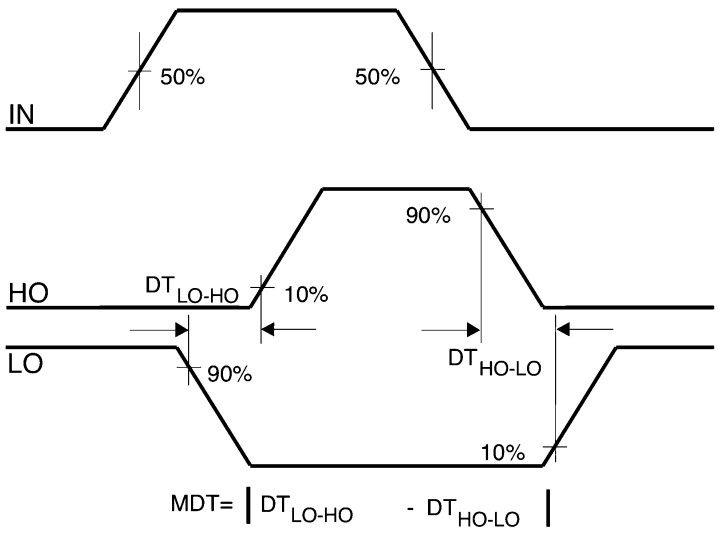

Figure 19: Dead time waveform definitions.

The outputs of the drive chips are connected to switching control of the MOSFET Inverter shown in Fig. 20. Each HO and LO output of drive chips 1, 2, and 3 control MOSFETs 1 and 4, 2 and 5, 3 and 6 respectively. The work implemented on MOSFET can also be repeated with better efficiency on IGBT Inverter shown in Fig. 21.

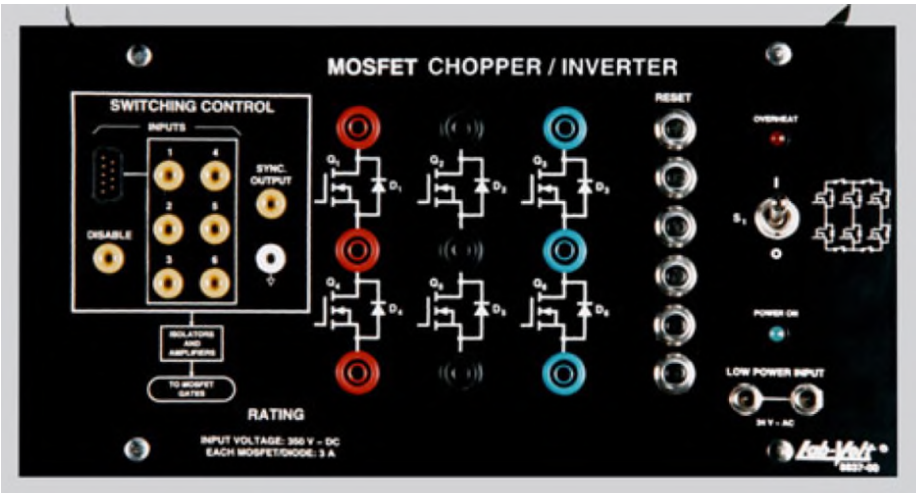

Figure 20: Lab-Volt MOSFET Inverter (Lab-Volt courtesy).

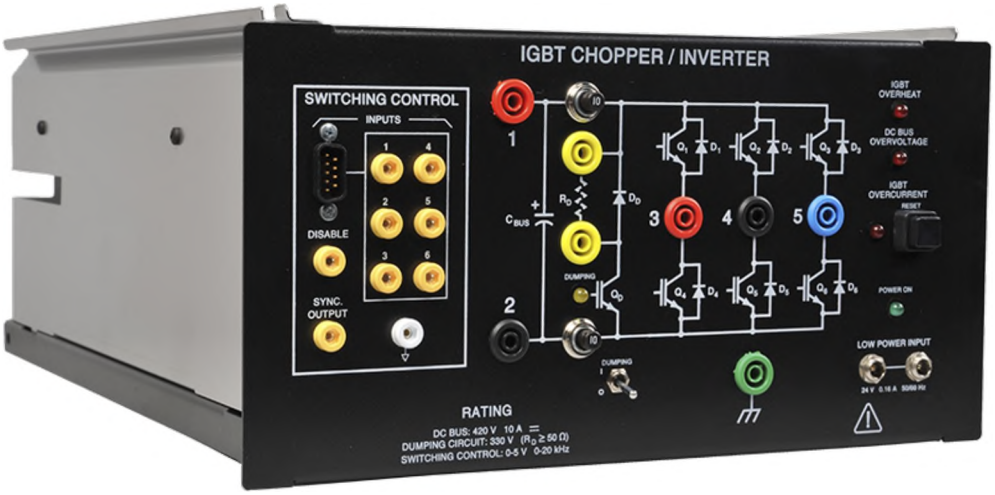

Figure 21: Lab-Volt IGBT Inverter (Lab-Volt courtesy).

CHAPTER V

SIMULATION RESULTS

The circuit of a Grid Side Inverter, shown in Fig. 22, has been built for the simulation part of this work, using MATLAB Simulink. Input DC voltage was set to 60V. Impedances Z1, Z2, and Z3 were each set to 10 mH, depicting the line inductors. Eight cases, shown in Table II have been chosen to represent balanced to extremely unbalanced conditions. Cases 1-7 show how the presented control method handles various levels of grid unbalance, including SLG and LLG faults. Case 8 demonstrates how the proposed circuit behaves when connected to unbalanced load, in addition to SLG fault. In each case, the power factor (PF) is set to different values to show active and reactive power transfer, to and from the grid, while the actual currents are closely following the reference currents. All obtained results are shown in Figs. 23-46. Figures 23-38 show the output currents with respect to grid line voltage, while Figs. 39-46 demonstrate active and reactive power exchange between the grid and the inverter. Table III details the parameters used in this simulation. Finally, the MATLAB code (m-file), used in this section can be found in Appendix A.

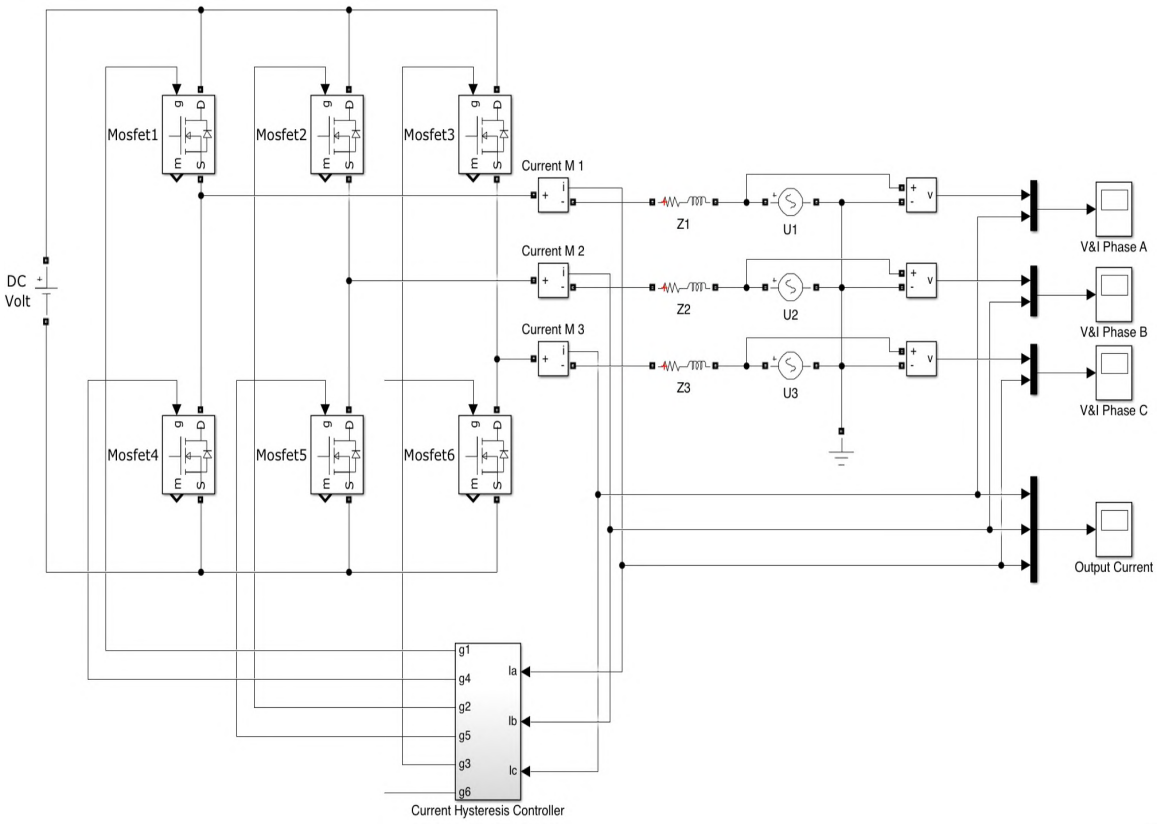

Figure 22: Simulation Diagram of a Grid Side Inverter.

In CASE 1, grid side inverter operates with the unity power factor under balanced grid voltages and line impedances, and delivers 50W to the grid. The negative sign was chosen as a convention to be used when the power is delivered to the grid.

In CASE 2, grid side inverter continues to operate with the unity power factor under unbalanced grid voltages with a single line-ground fault (SLG) in Line 3. The line impedances are balanced, and the inverter delivers 50W to the grid.

In CASE 3, grid side inverter operates under unbalanced grid voltages, with a single line-ground fault (SLG) and balanced line impedances. The PF is set to 0.707 lagging, and 30W of active power and 30Vars of reactive power is delivered to the grid.

In CASE 4, grid side inverter continues to operate under unbalanced grid voltages, with a single line-ground fault (SLG) and balanced line impedances, but now the PF is set to 0.707 leading. 30W of active power is still delivered to the grid, while 30Vars of reactive power is now absorbed from the grid.

CASE 5, brings a more severe level of unbalance, where grid side inverter operates with unity power factor under unbalanced grid voltages, with a double line-ground fault (LLG) and balanced line impedances, while delivering 25W to the grid.

In CASE 6, grid side inverter continues to operate under unbalanced grid voltages, with the double line-ground fault (LLG) and balanced line impedances, while delivering 15W of active power and 15Vars of reactive power to the grid.

In CASE 7, grid side inverter operates under unbalanced grid voltages, with a double line-ground fault (LLG) and balanced line impedances. It supplies 15W to the grid and absorbs 15Vars from the grid.

In addition to the unbalance in grid voltages, CASE 8 adds the effect of the unbalanced load. Grid side inverter operates with unity power factor under unbalanced grid voltages, with a single line-ground fault (SLG) and unbalanced line impedance (L2=0), while delivering 50W to the grid.

The simulation of all of these cases demonstrates the control method's capability to operate successfully under various unbalanced voltage and impedance conditions. The same eight cases, listed in Table II, are also experimentally verified in the next section. The choice of the values, including the power setting, the input DC voltage and the output AC voltage were primarily based on the ratings of the used equipment.

TABLE II: CASES USED IN SIMULATION AND EXPERIMENT

Case	Grid Voltages (Volts)	Line Impedances (mH)	Power Setting (W, VAR) (P ± jQ)
1	U1 = 10∠0 U2 = 10∠-120 U3 = 10∠120	L1 = L2 = L3 = 10	- 50
2	U1 = 10∠0 U2 = 10∠-120 U3 = 0	L1 = L2 = L3 = 10	- 50
3	U1 = 10∠0 U2 = 10∠-120 U3 = 0	L1 = L2 = L3 = 10	- 30 - j30
4	U1 = 10∠0 U2 = 10∠-120 U3 = 0	L1 = L2 = L3 = 10	- 30 + j30
5	U1 = 10∠0 U2 = 0 U3 = 0	L1 = L2 = L3 = 10	- 25
6	U1 = 10∠0 U2 = 0 U3 = 0	L1 = L2 = L3 = 10	- 15 - j15
7	U1 = 10∠0 U2 = 0 U3 = 0	L1 = L2 = L3 = 10	- 15 + j15
8	U1 = 10∠0 U2 = 10∠-120 U3 = 0	L1 = L3 = 10 L2 = 0	- 50

TABLE III: SIMULATION PARAMETERS

Parameter	Value
Fundamental frequency, f	60 Hz
Hysteresis Band	20 mA
Diode on Inductance	0 H
MOSFET on Resistance	0.1 Ω
Diode Resistance	0.01 Ω
Diode Forward Voltage	0 V
Snubber Resistance	1e5 Ω
Snubber Capacitance	Inf. (F)

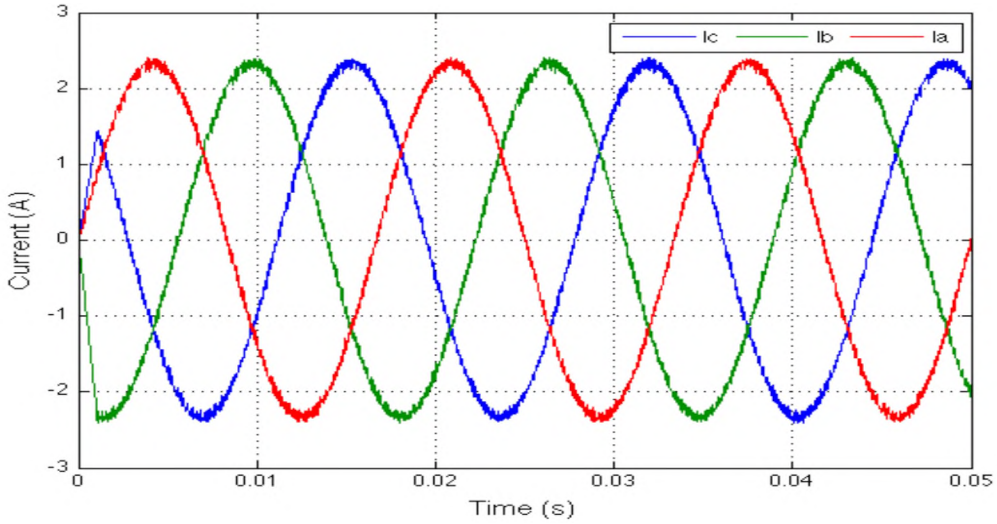

Figure 23: Grid Currents for Case 1 (Simulation Results).

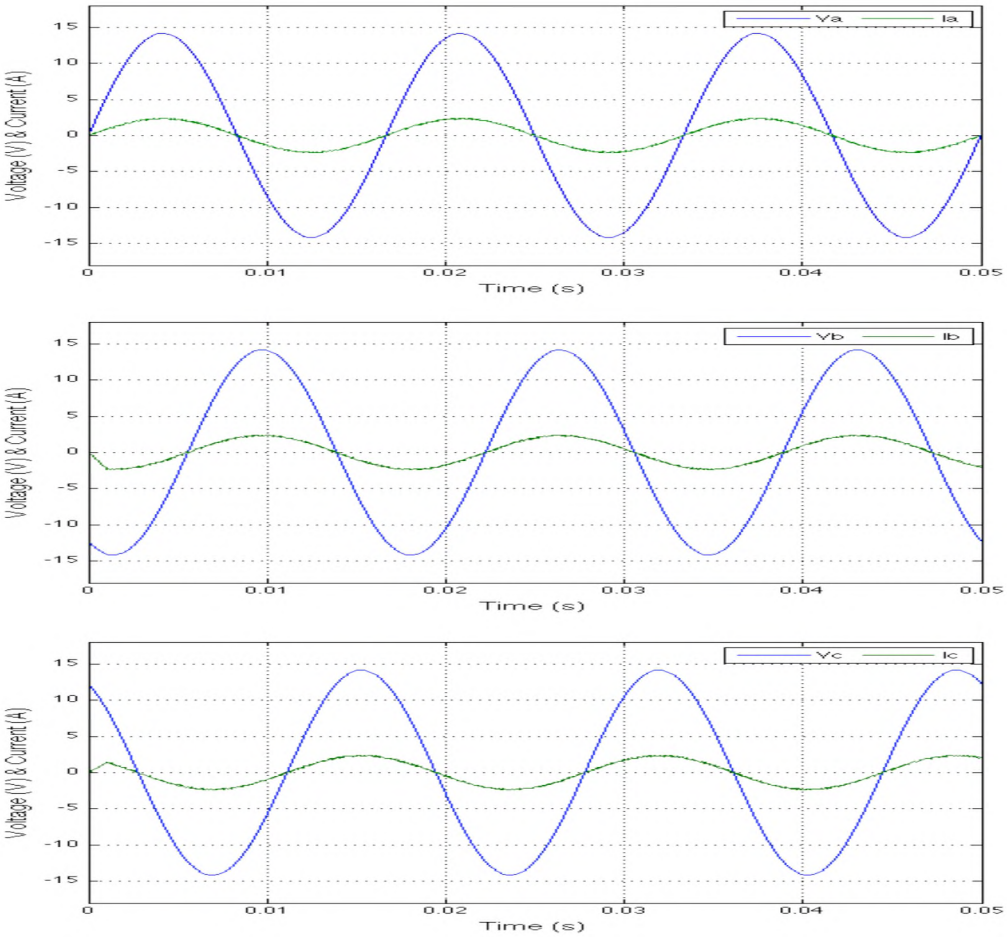

Figure 24: Voltage and Current in Phases A, B, and C, Case 1 (Simulation Results).

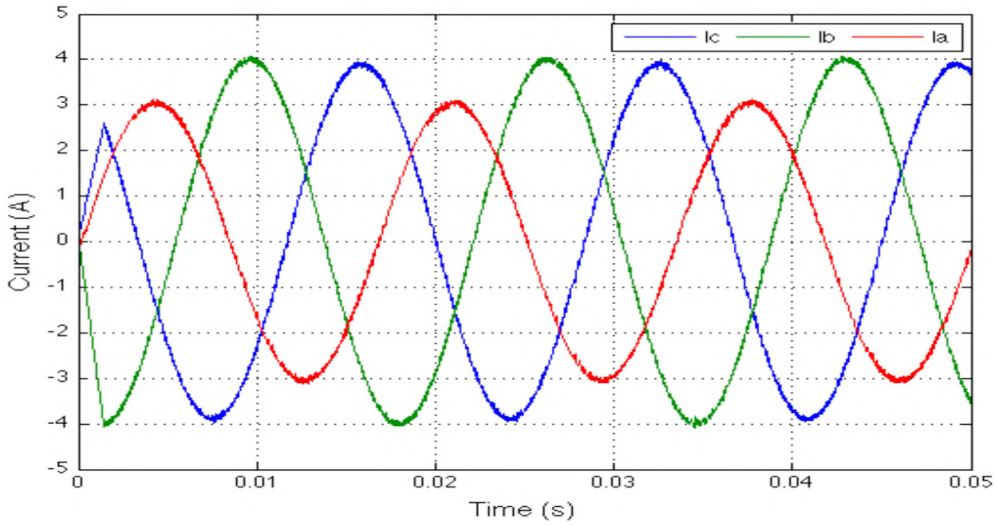

Figure 25: Grid Currents for Case 2 (Simulation Results).

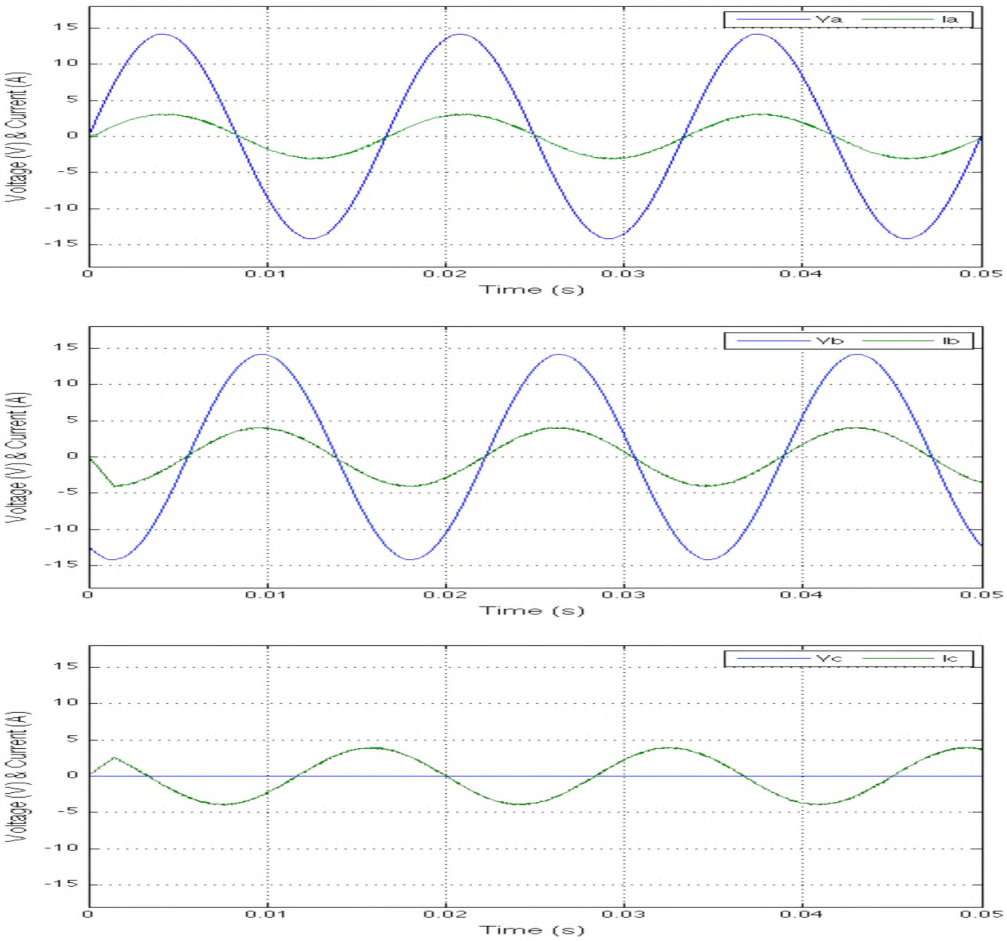

Figure 26: Voltage and Current in Phases A, B, and C, Case 2 (Simulation Results).

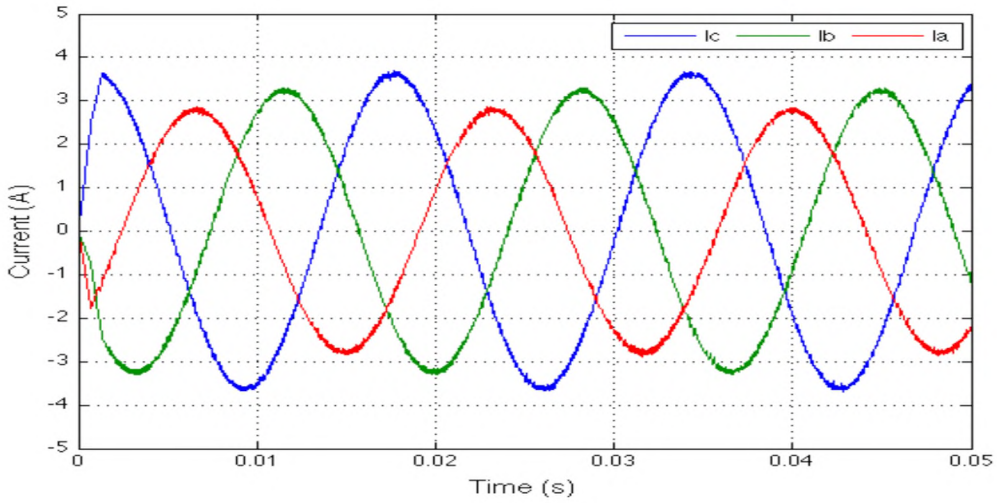

Figure 27: Grid Currents for Case 3 (Simulation Results).

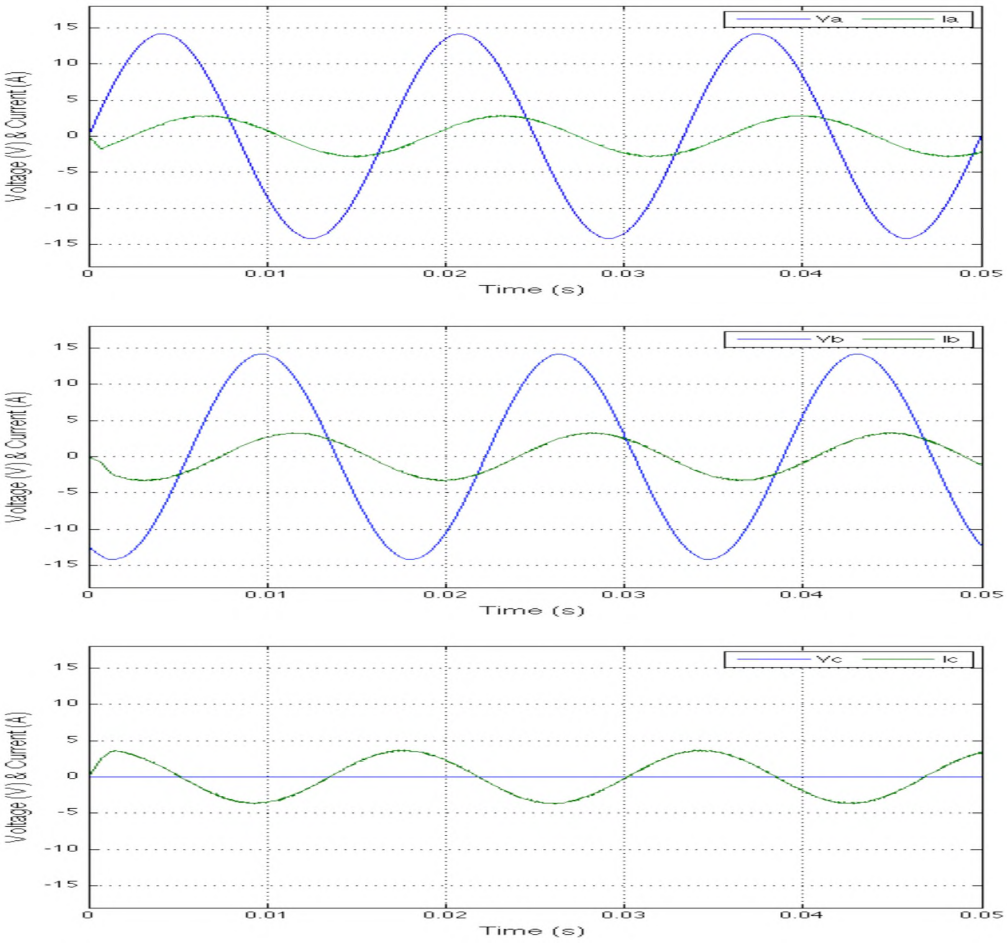

Figure 28: Voltage and Current in Phases A, B, and C, Case 3 (Simulation Results).

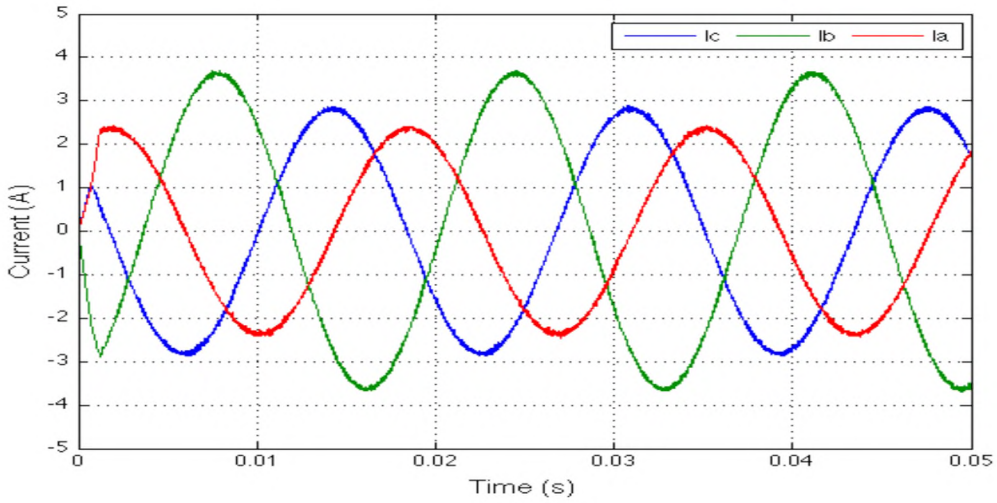

Figure 29: Grid Currents for Case 4 (Simulation Results).

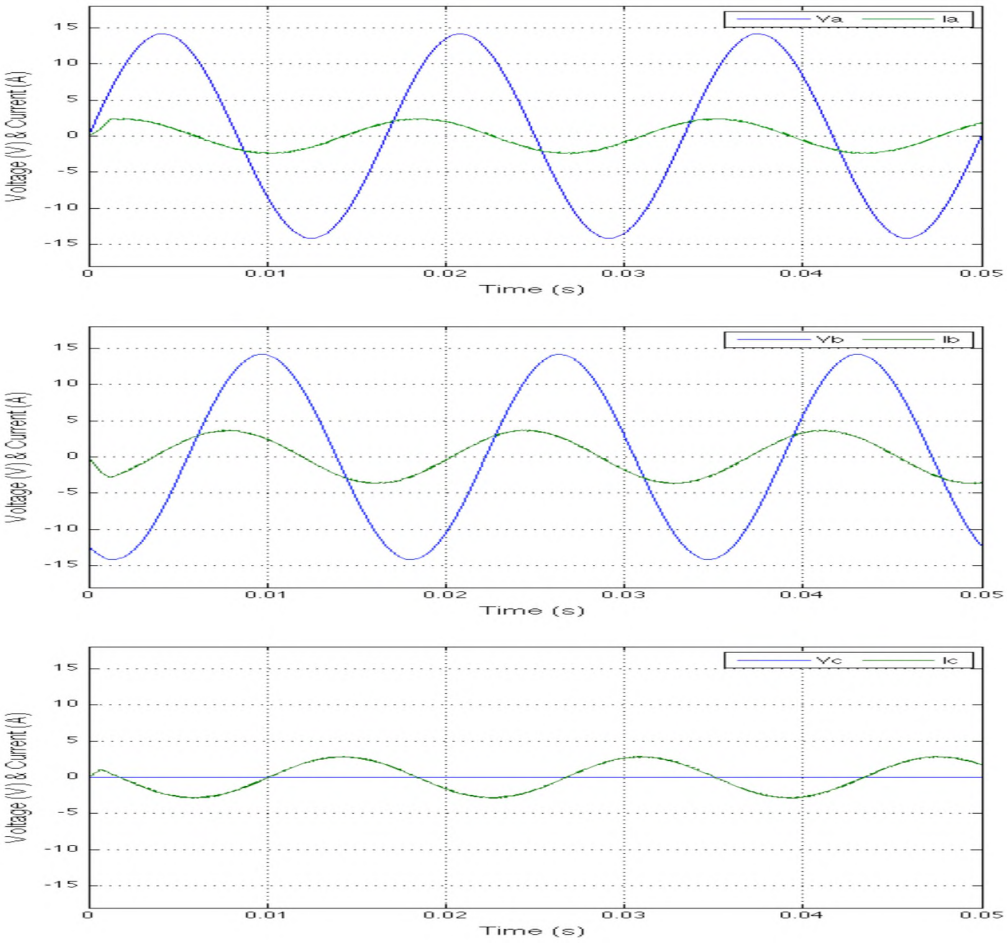

Figure 30: Voltage and Current in Phases A, B, and C, Case 4 (Simulation Results).

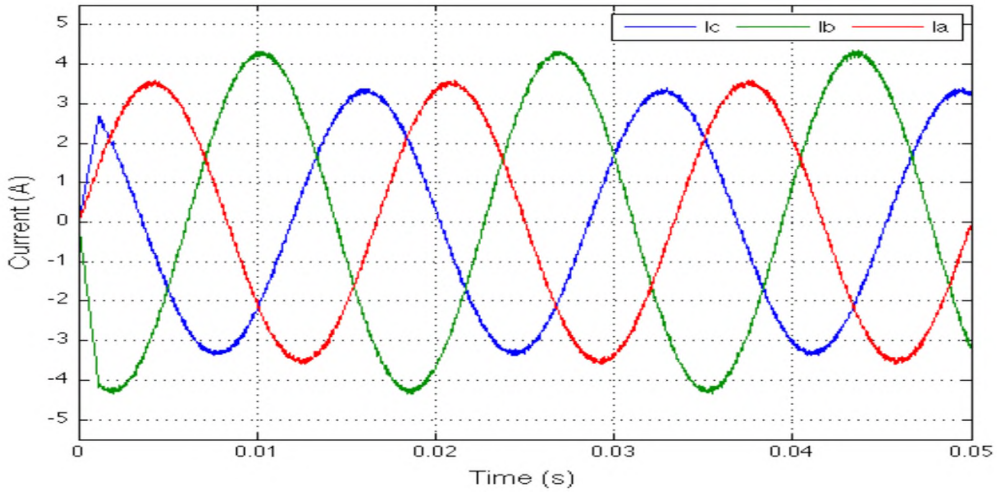

Figure 31: Grid Currents for Case 5 (Simulation Results).

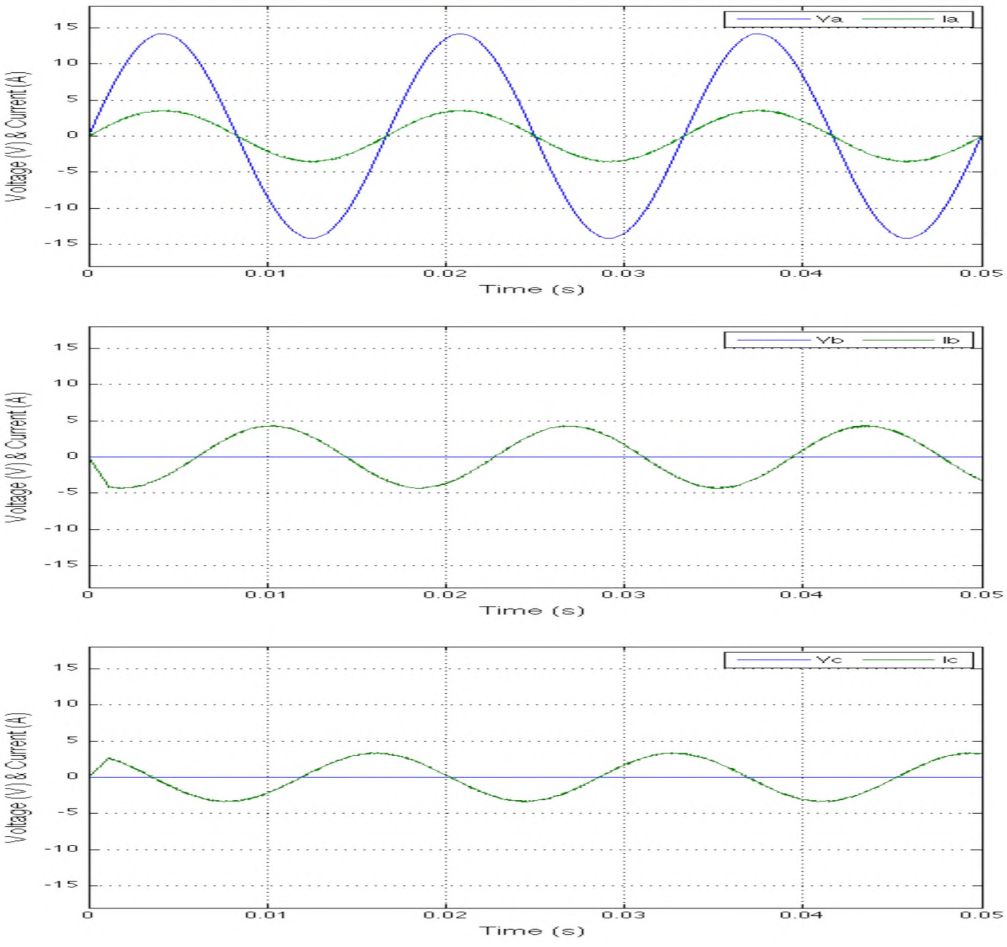

Figure 32: Voltage and Current in Phases A, B, and C, Case 5 (Simulation Results).

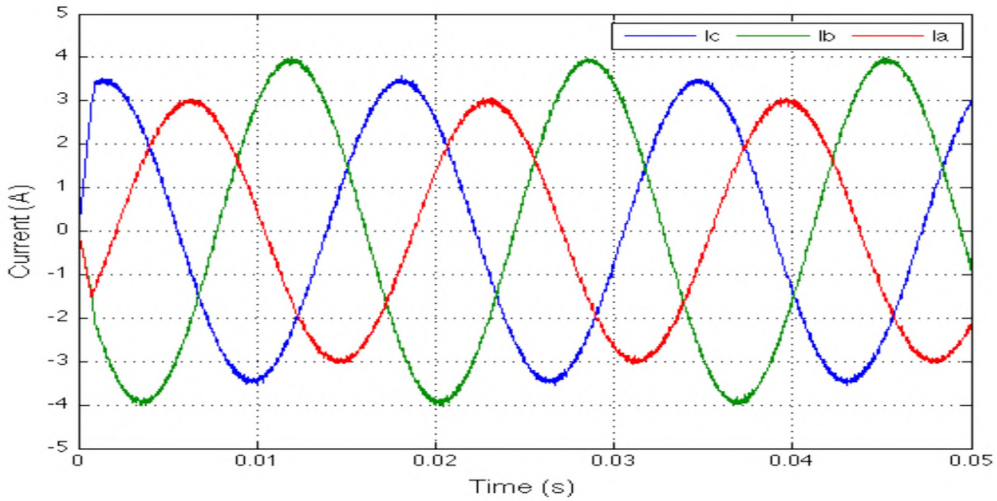

Figure 33: Grid Currents for Case 6 (Simulation Results).

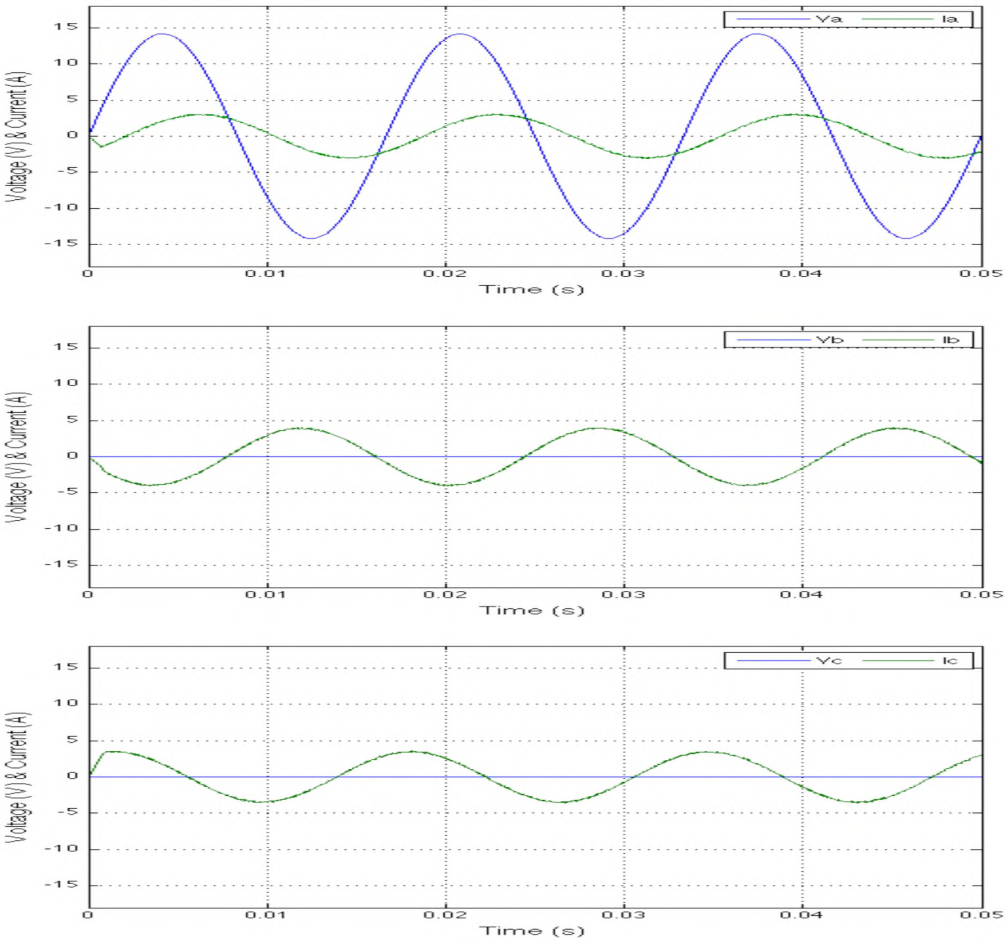

Figure 34: Voltage and Current in Phases A, B, and C, Case 6 (Simulation Results).

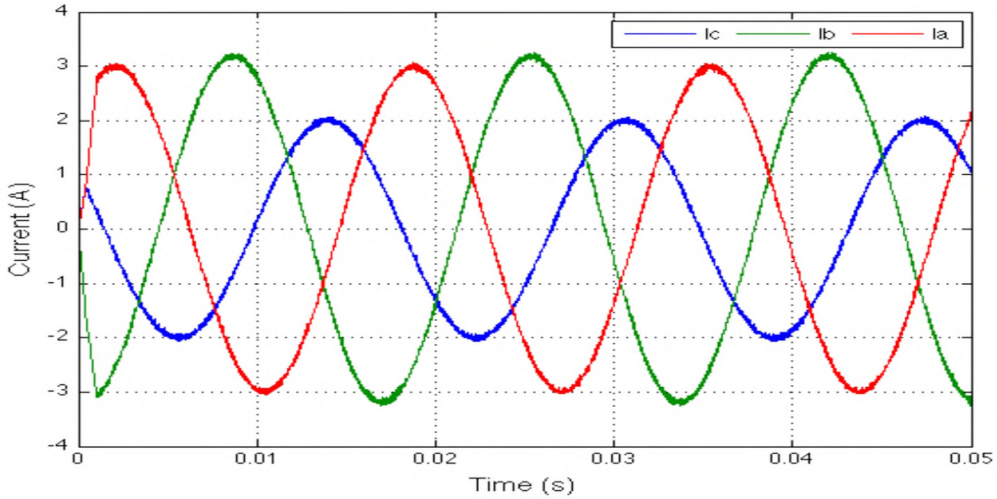

Figure 35: Grid Currents for Case 7 (Simulation Results).

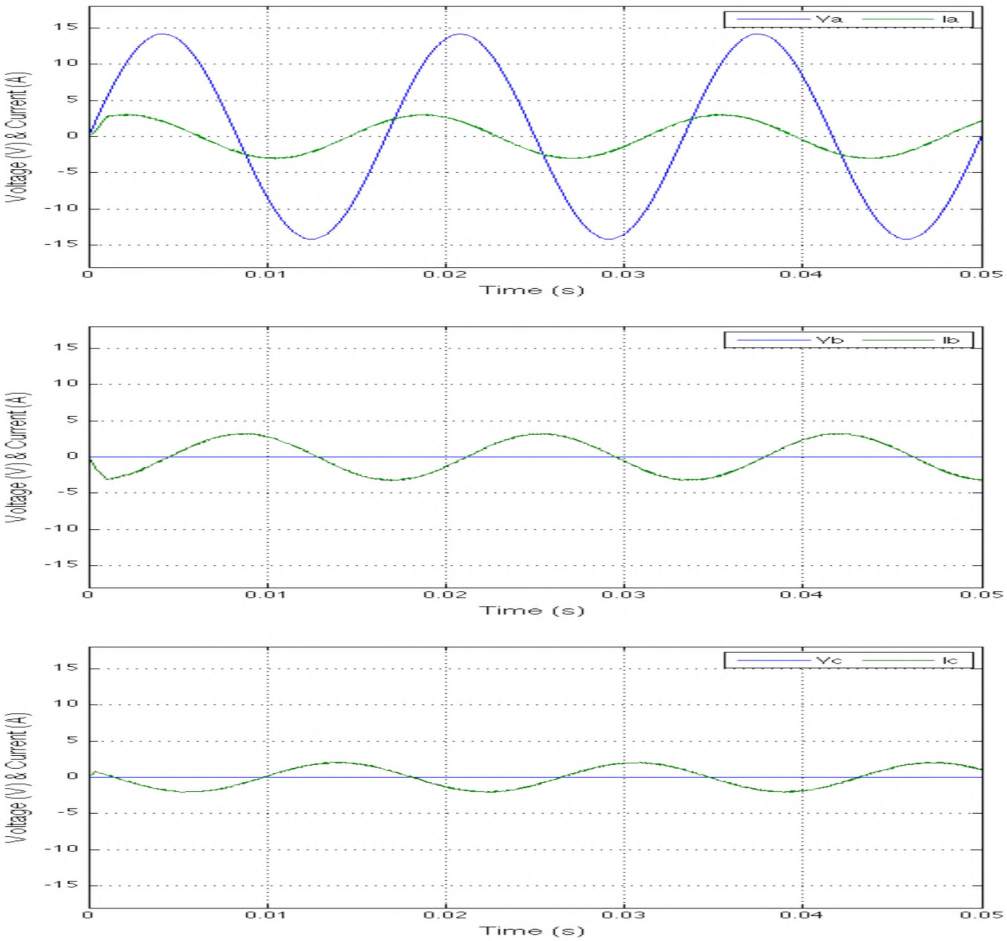

Figure 36: Voltage and Current in Phases A, B, and C, Case 7 (Simulation Results).

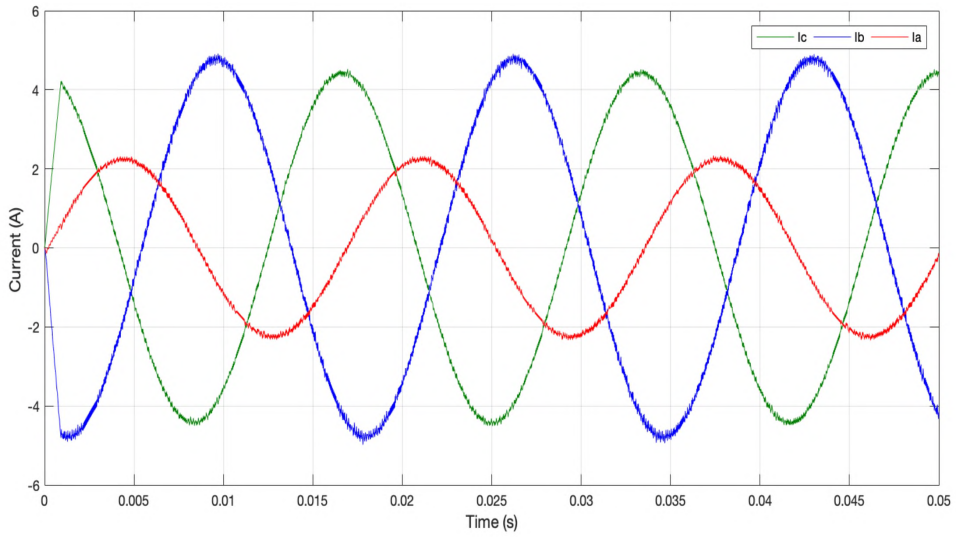

Figure 37: Grid Currents for Case 8 (Simulation Results).

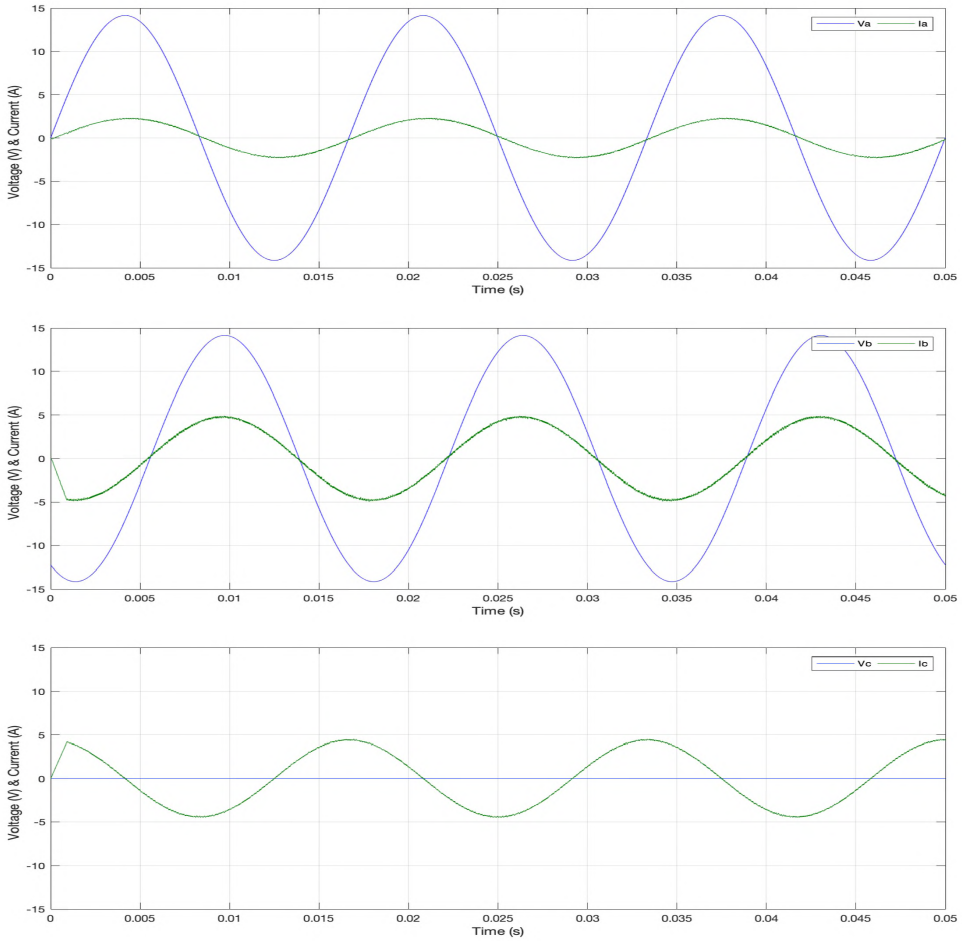

Figure 38: Voltage and Current in Phases A, B, and C, Case 8 (Simulation Results).

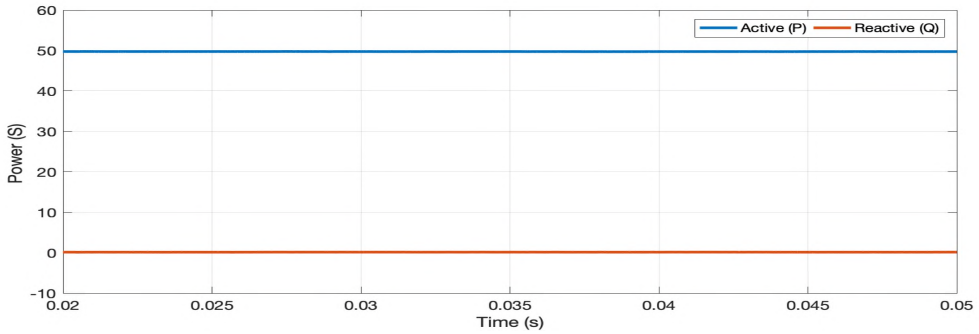

Figure 39: Balanced, 50W delivered to the grid (Case 1).

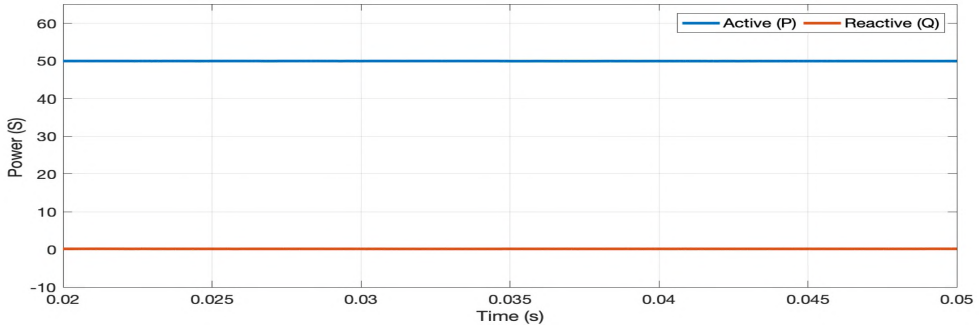

Figure 40: SLG fault, 50W delivered to the grid (Case 2).

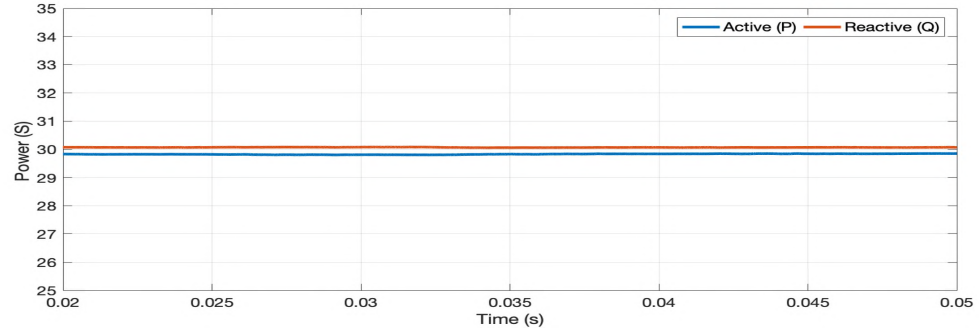

Figure 41: SLG fault, 30W and 30VAR delivered to the grid (Case 3).

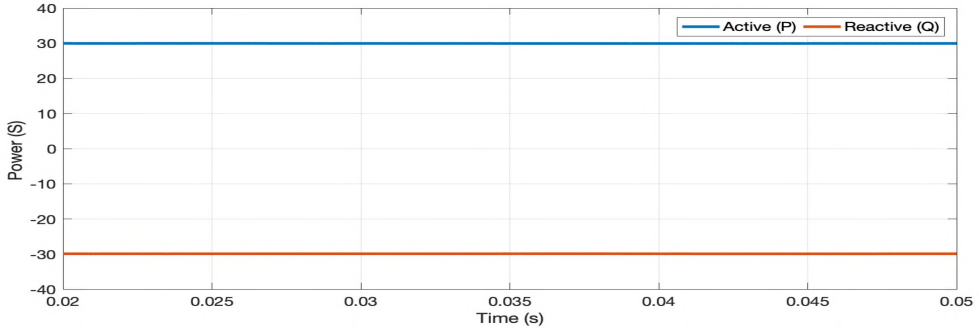

Figure 42: SLG fault, 30W delivered to the grid, 30Var absorbed by the grid (Case 4)

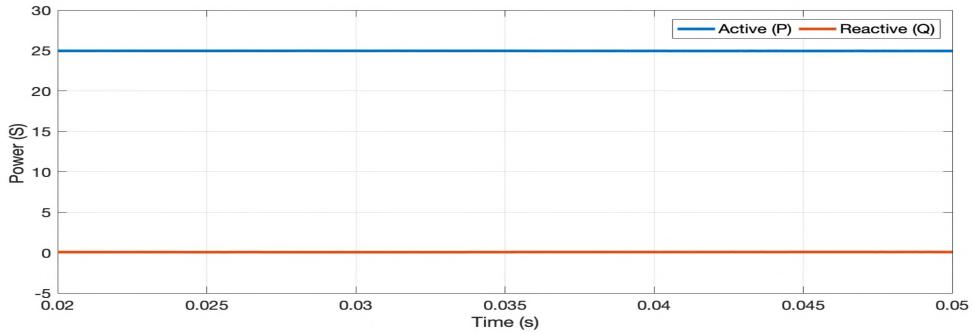

Figure 43: LLG fault, 25W delivered to the grid (Case 5).

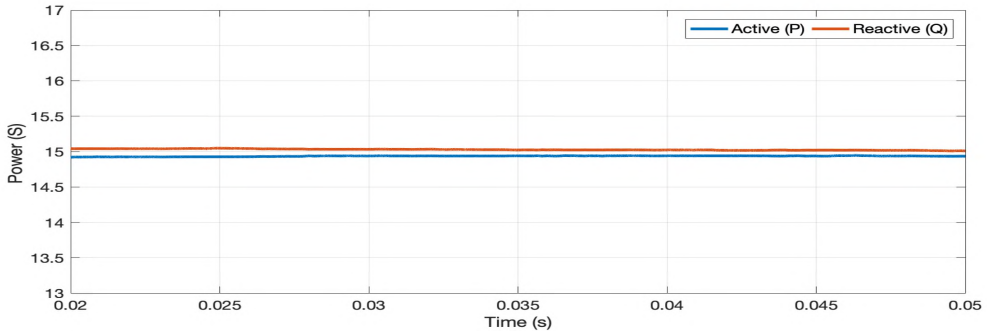

Figure 44: LLG fault, 15W and 15VAR delivered to the grid (Case 6).

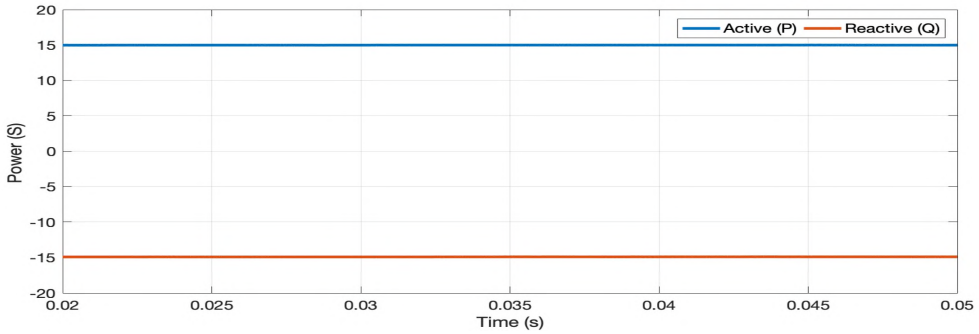

Figure 45: LLG fault, 15W delivered to the grid, 15Var absorbed by the grid (Case 7)

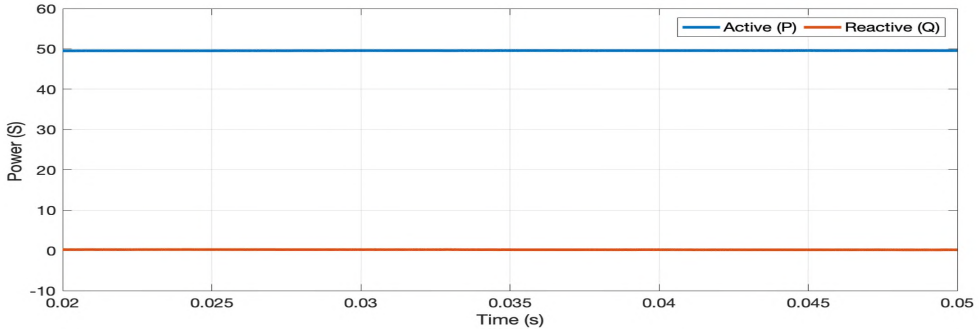

Figure 46: SLG fault, Unbalanced load, 50W delivered to the grid (Case 8).

CHAPTER VI

EXPERIMENTAL RESULTS

The laboratory prototype shown in Fig. 47 has been built and tested in the power lab. Three-phase MOSFET inverter, manufactured by Lab-Volt has been used for all experimental work. The control algorithm has been implemented by MATLAB Simulink and DSPACE RT1104 control system. The hardware configuration, discussed earlier, is shown again in Fig. 48. As shown in the diagram, grid voltage and impedance unbalance must be known, after which the values for active and reactive power, P and Q are set. Based on the values of P and Q, the powerful functions of MATLAB and Simulink (reference calculator), calculate reference currents according to equations (14), (17), and (19). The actual currents are measured, and are forced to track the reference values by digital hysteresis controller, as shown in Fig. 49. A detailed Simulink model used in the whole experiment is depicted in this figure. The output of the hysteresis controller generates switching signals for the MOSFETs. MOSFET drive board is designed with three IR21091S drive chips, shown in Fig. 50, where each driver controls two switches in one leg of the converter. The chip provides two logic signals (0 and 5V) at the output, such that whenever one is 0V, the other is 5V and vice versa, but never "high" for both.

The total time to obtain the solution to equations (14), (17), and the quadratic equation in (19) is about 14 μs. The sampling time (T_s) is set to 20μs, and the hysteresis band is set to 20mA, hence the switching frequency (f_s) is variable and does not exceed its maximum value of 25 kHz, which satisfies the Nyquist sampling theorem and prevents aliasing [51].

In this section, all eight cases presented earlier in the simulation in TABLE II, have been experimentally verified. The input DC side is powered by a 60V power supply. Each line is of the inverter is connected to the AC side through a 10 mH inductor. The currents in these lines are measured by current sensing probes, and are compared against the reference currents. The hysteresis controller makes sure the references are followed, and in each case, appropriate power (active and reactive) is transferred from the DC side to the AC side, and vice versa. As in the simulation, line currents in each case are shown to be closely following the references when this control method is used, under balanced conditions and under extreme unbalanced conditions, including SLG and LLG faults, and load unbalance. In each case the power factor (PF) is set to various values to demonstrate bi-directional power flow between the grid and the inverter. Experimental results for eight unbalanced cases are shown in Figs. 51-65. MATLAB code (m-file), used in this section can be found in Appendix B. As expected, the experimental section usually contains more losses than the simulation, and in this case, the MOSFET unit contributed to that loss. The converter's efficiency could have been improved if the IGBT inverter had been used instead. Unfortunately, the IGBT module was only available during the initial stages of this experiment, since it failed due to unexpected overcurrenting, and needed to be sent for repairs.

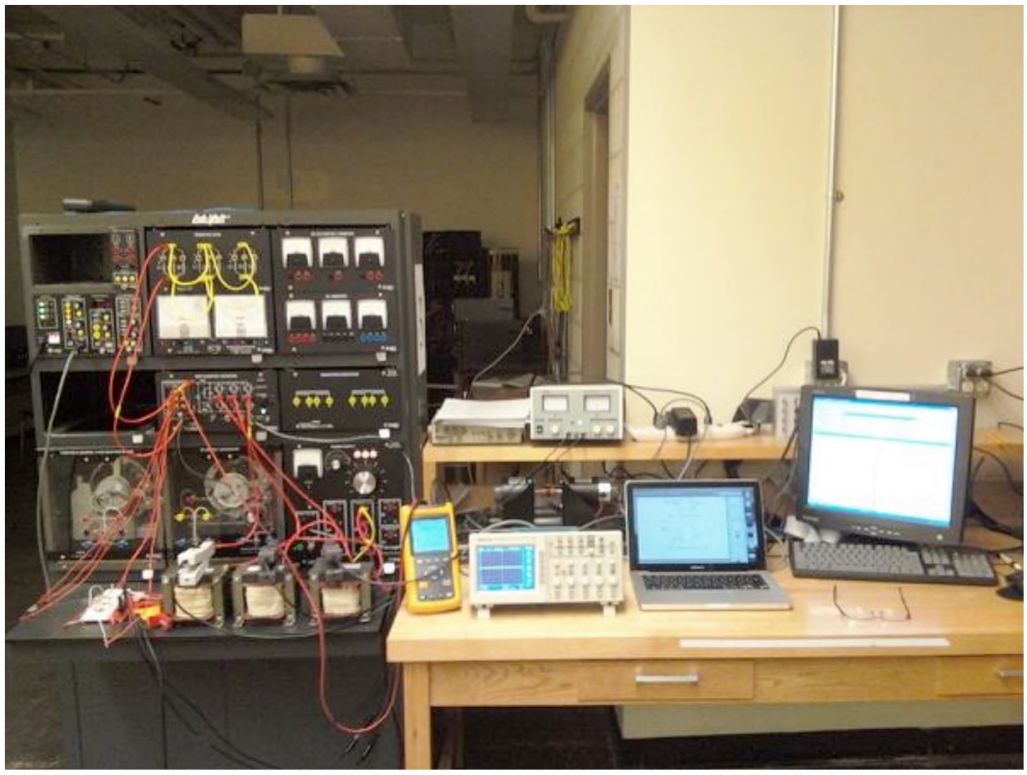

Figure 47: Laboratory Prototype.

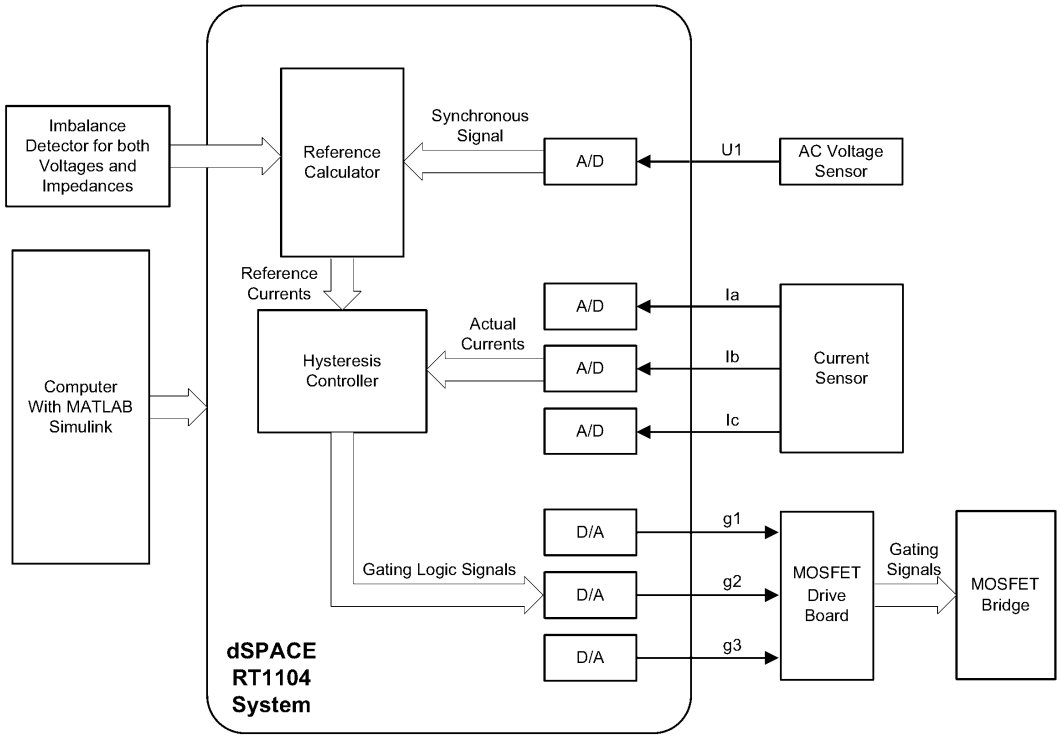

Figure 48: Hardware Configuration, adapted from [50].

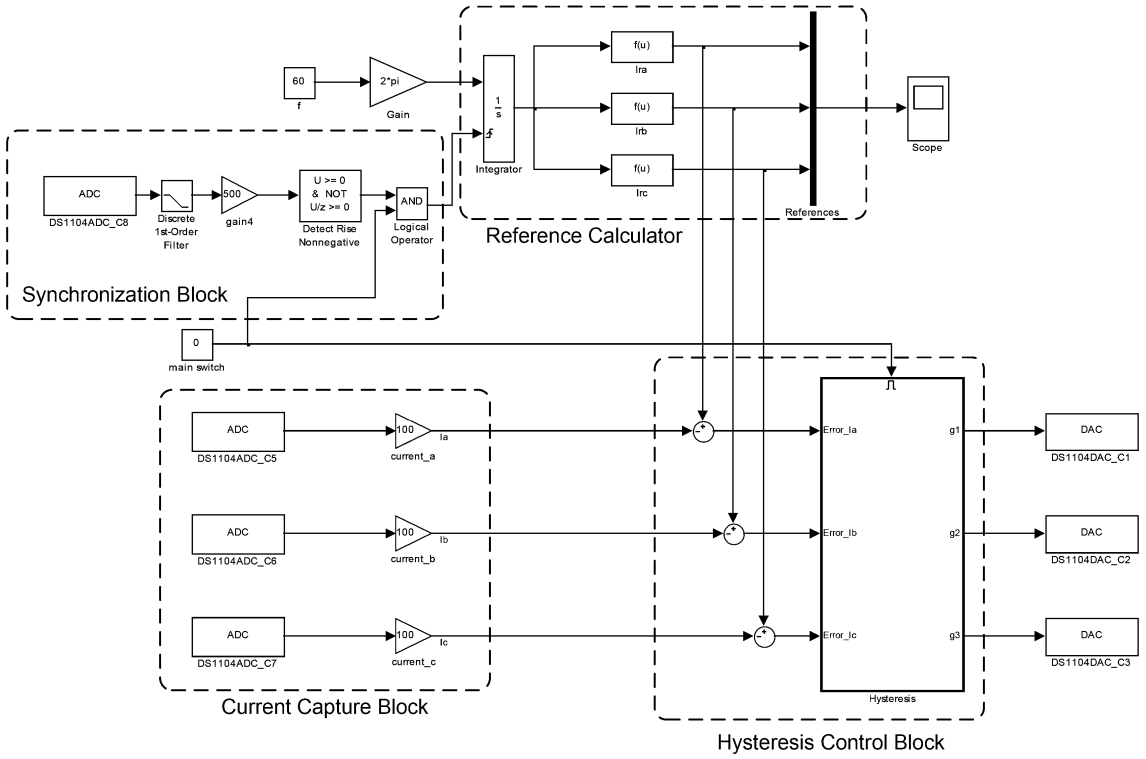

Figure 49: Simulink model used in the experiment, taken from [50].

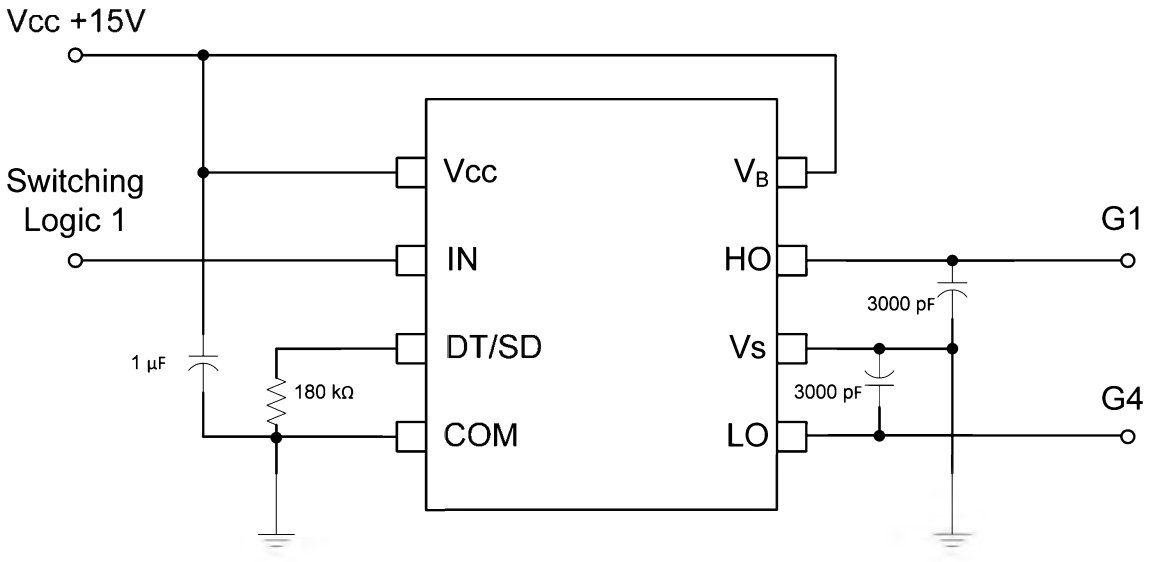

Figure 50: Control chip to drive one leg of the MOSFET Inverter, taken from [50].

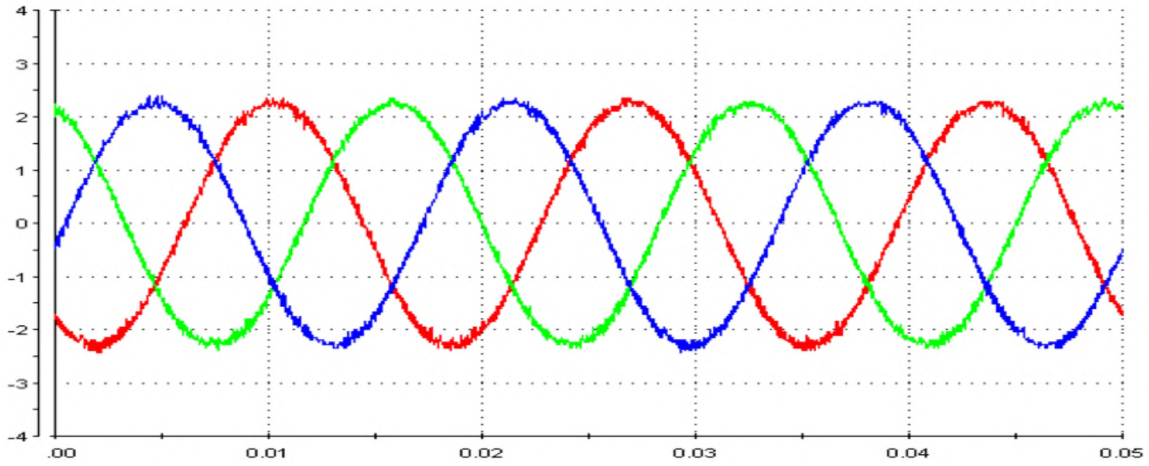

Figure 51: Grid Currents for Case 1 (Experimental Results).

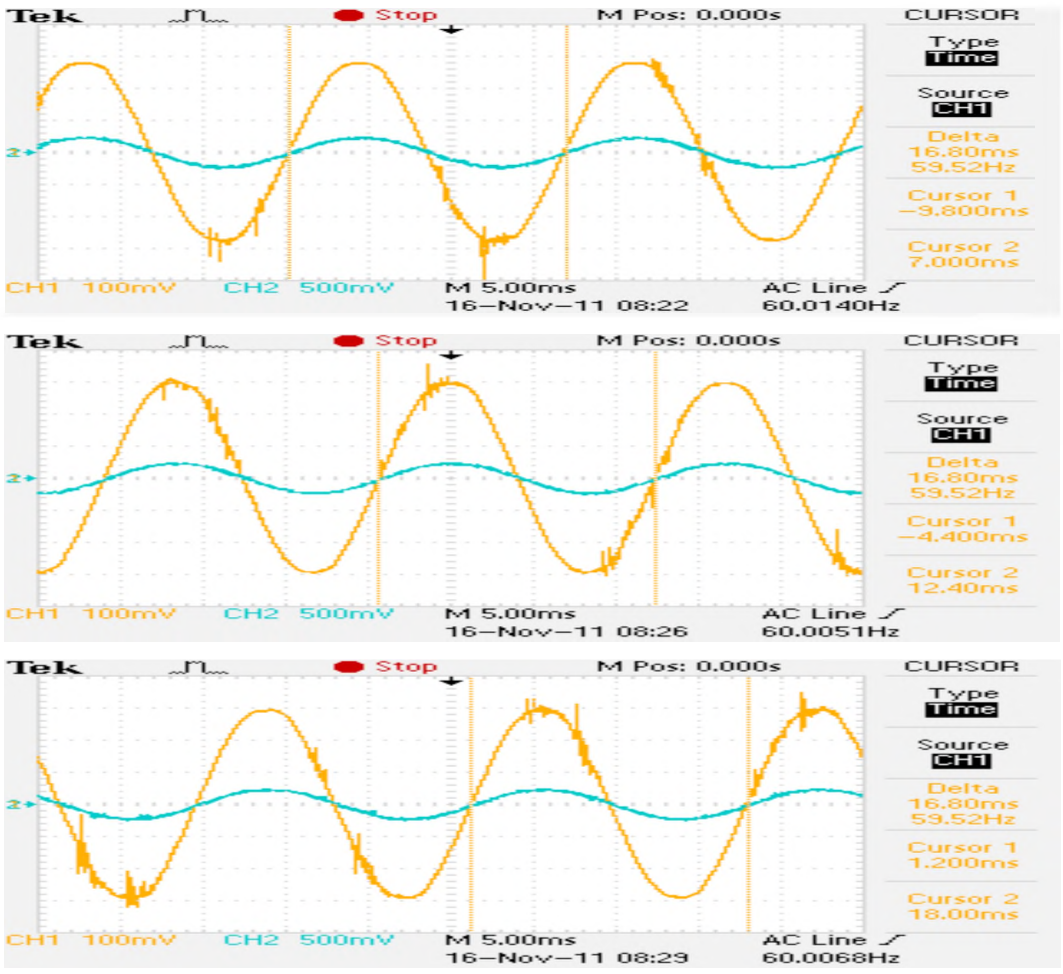

Figure 52: Voltage and Current in Phases A, B, and C, Case 1 (Experimental Results). Voltage probe: 20 mV/V. Current probe: 100 mV/A.

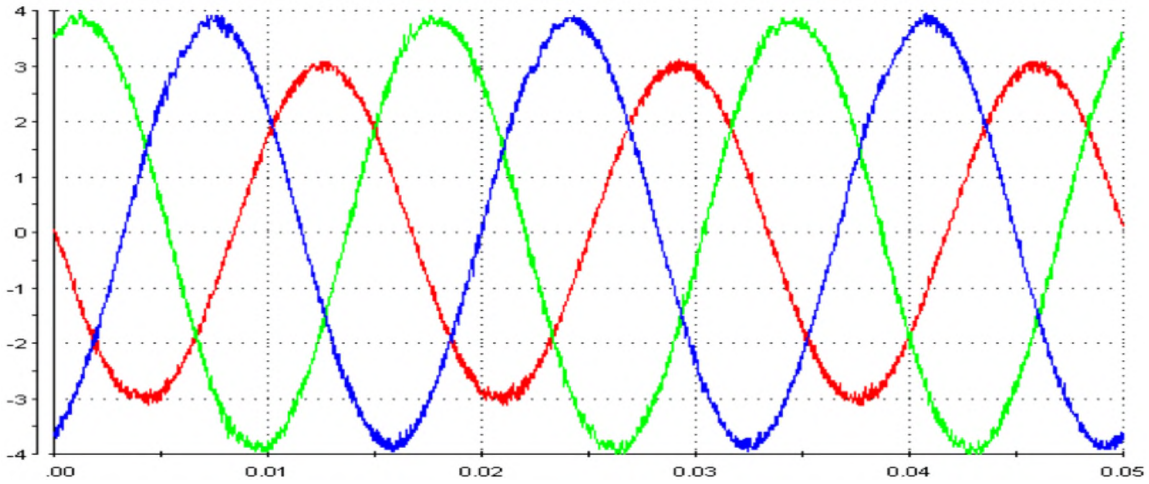

Figure 53: Grid Currents for Case 2 (Experimental Results).

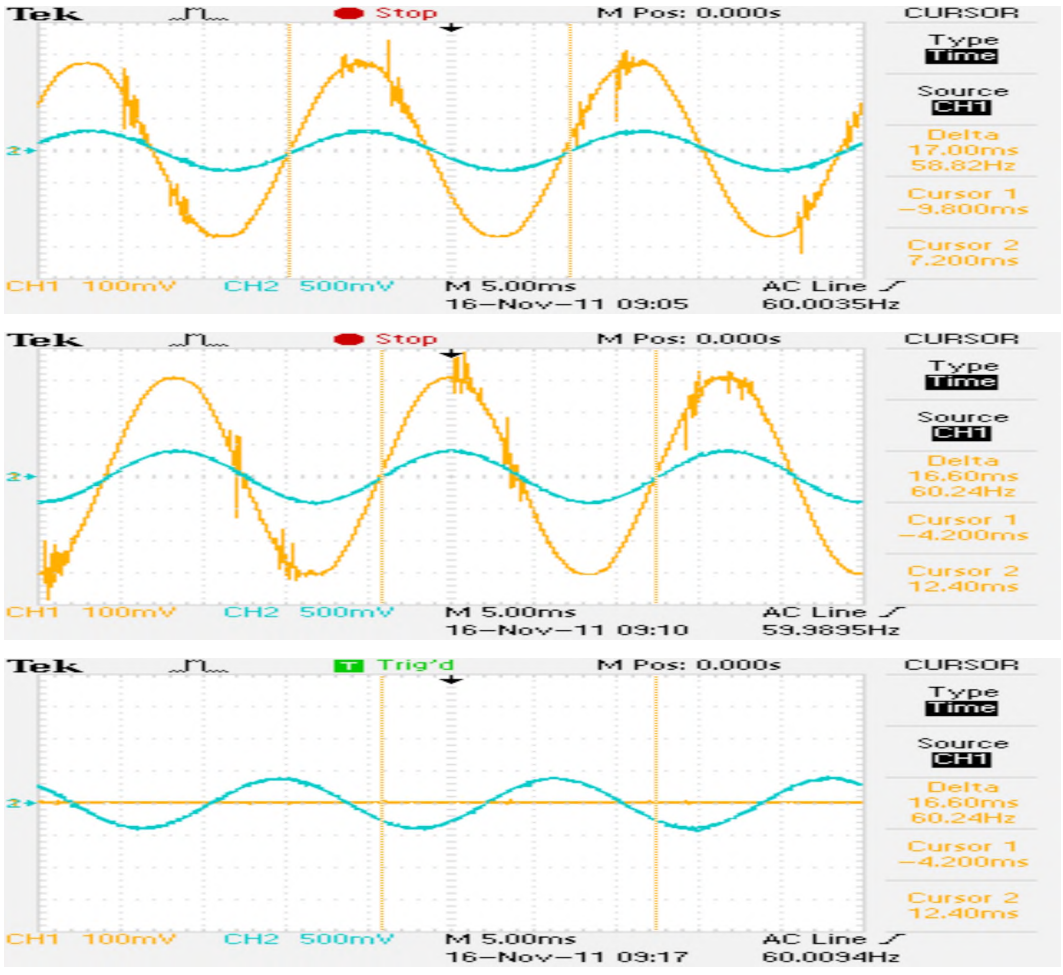

Figure 54: Voltage and Current in Phases A, B, and C, Case 2 (Experimental Results). Voltage probe: 20 mV/V. Current probe: 100 mV/A.

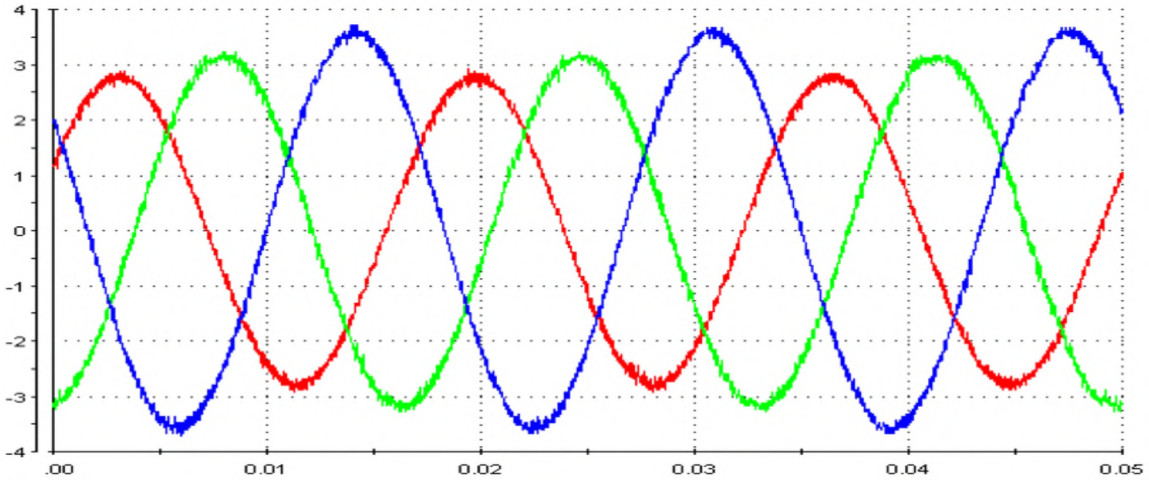

Figure 55: Grid Currents for Case 3 (Experimental Results).

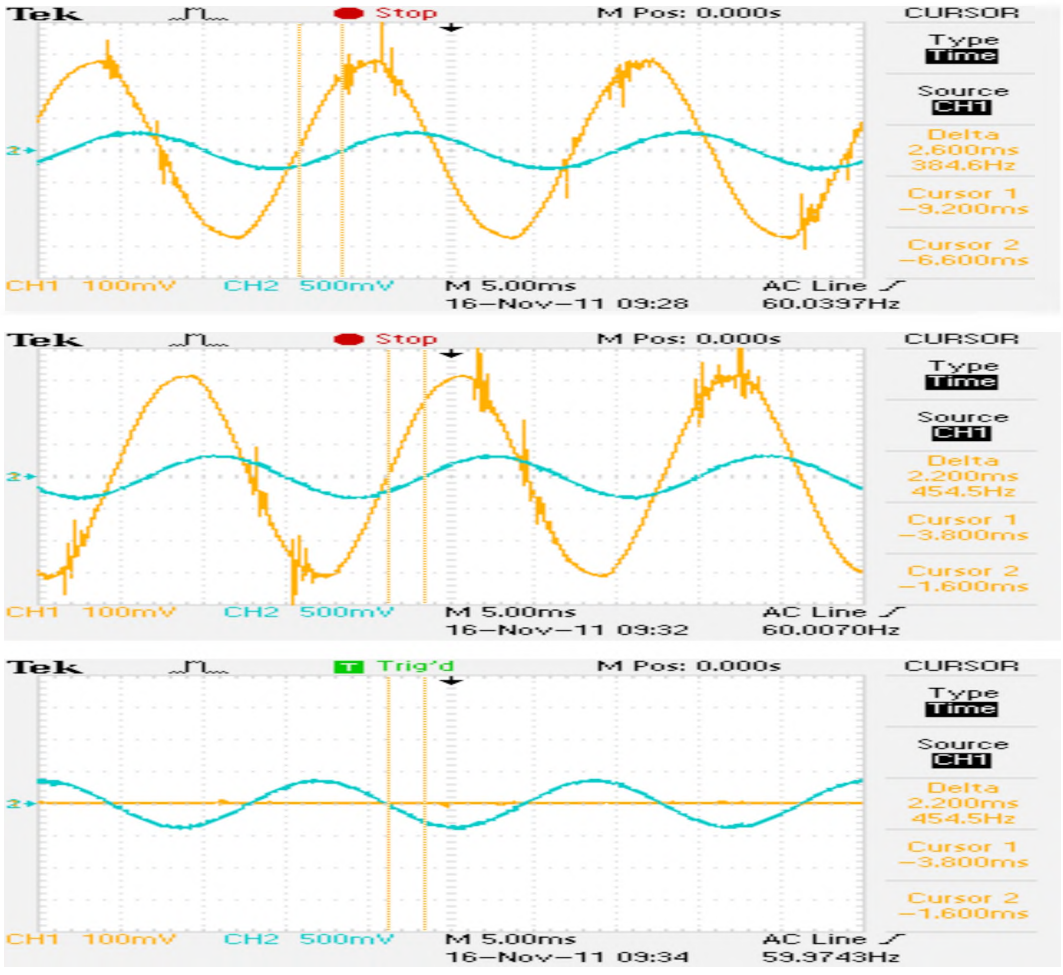

Figure 56: Voltage and Current in Phases A, B, and C, Case 3 (Experimental Results). Voltage probe: 20 mV/V. Current probe: 100 mV/A.

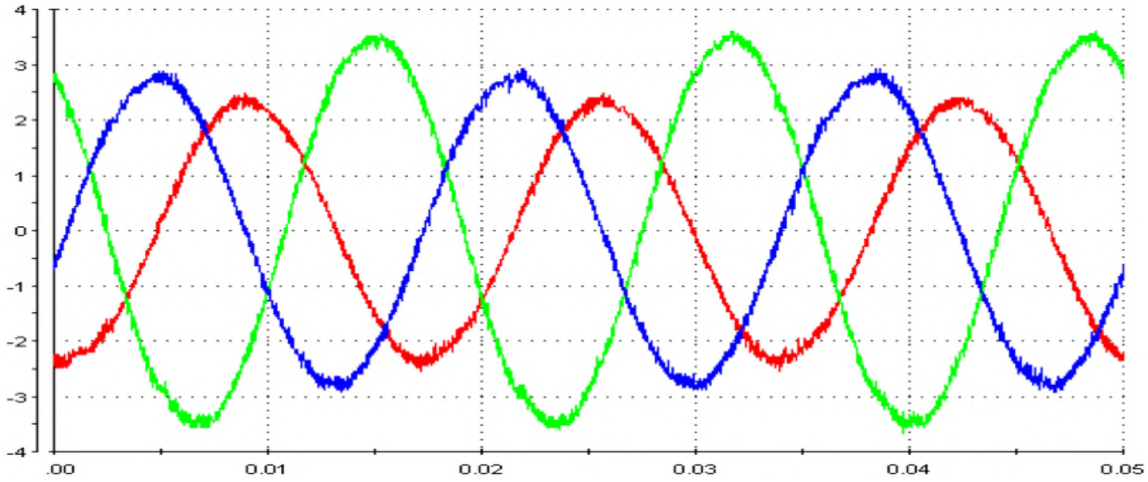

Figure 57: Grid Currents for Case 4 (Experimental Results).

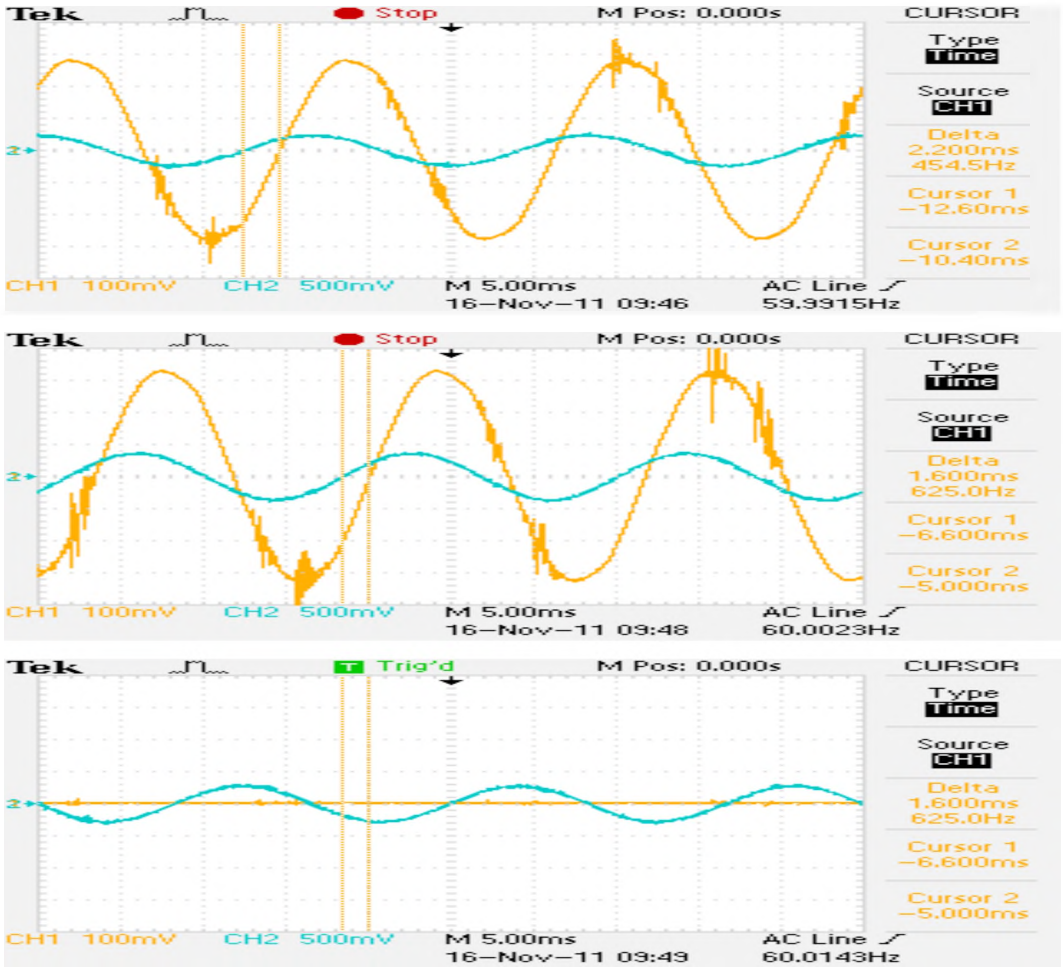

Figure 58: Voltage and Current in Phases A, B, and C, Case 4 (Experimental Results). Voltage probe: 20 mV/V. Current probe: 100 mV/A.

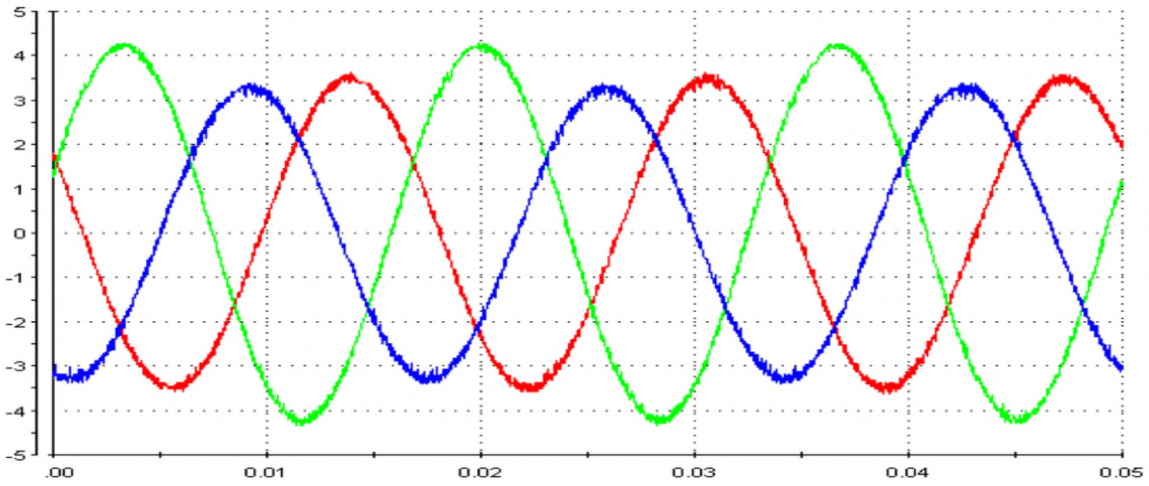

Figure 59: Grid Currents for Case 5 (Experimental Results).

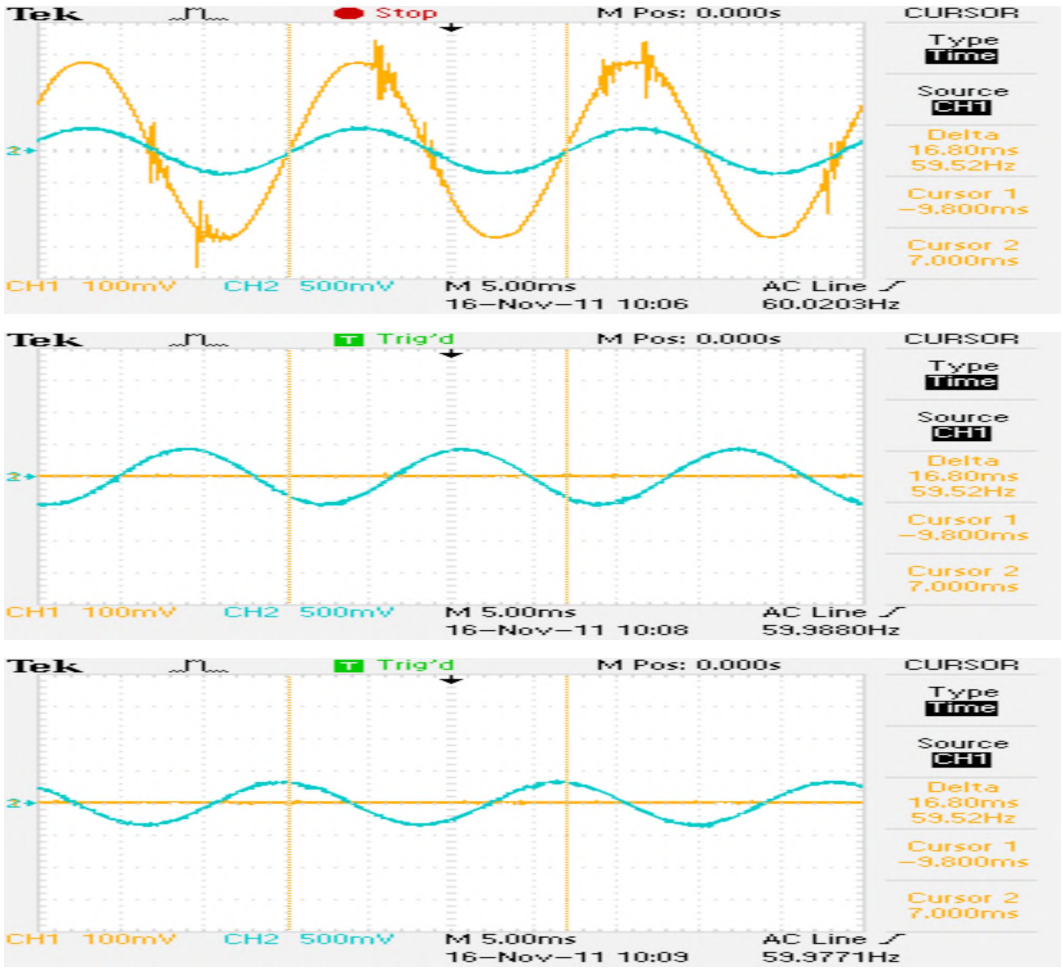

Figure 60: Voltage and Current in Phases A, B, and C, Case 5 (Experimental Results). Voltage probe: 20 mV/V. Current probe: 100 mV/A.

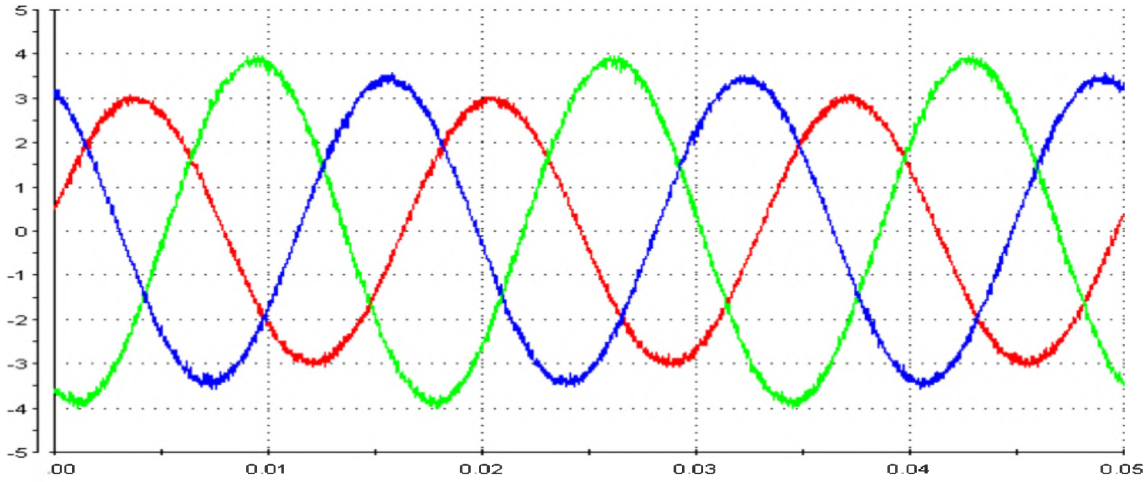

Figure 61: Grid Currents for Case 6 (Experimental Results).

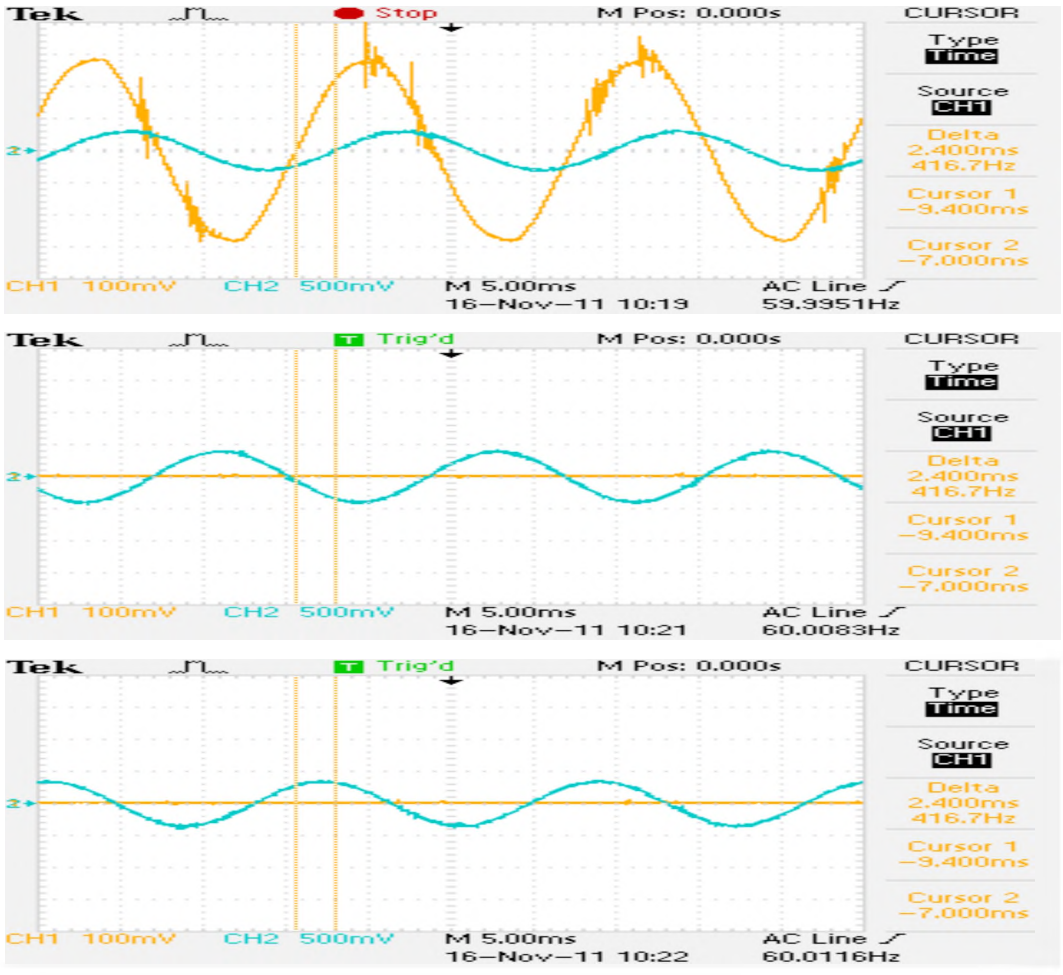

Figure 62: Voltage and Current in Phases A, B, and C, Case 6 (Experimental Results). Voltage probe: 20 mV/V. Current probe: 100 mV/A.

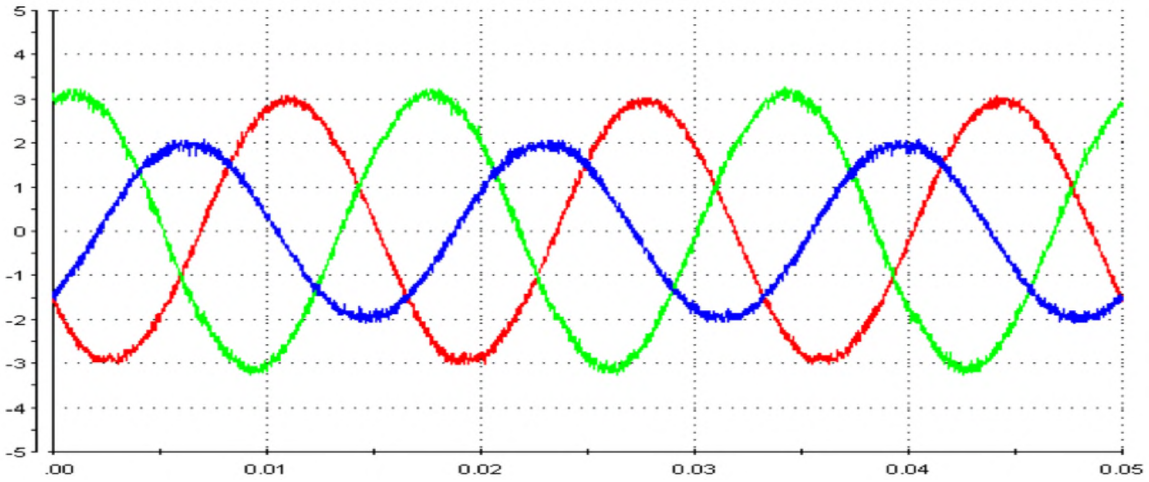

Figure 63: Grid Currents for Case 7 (Experimental Results).

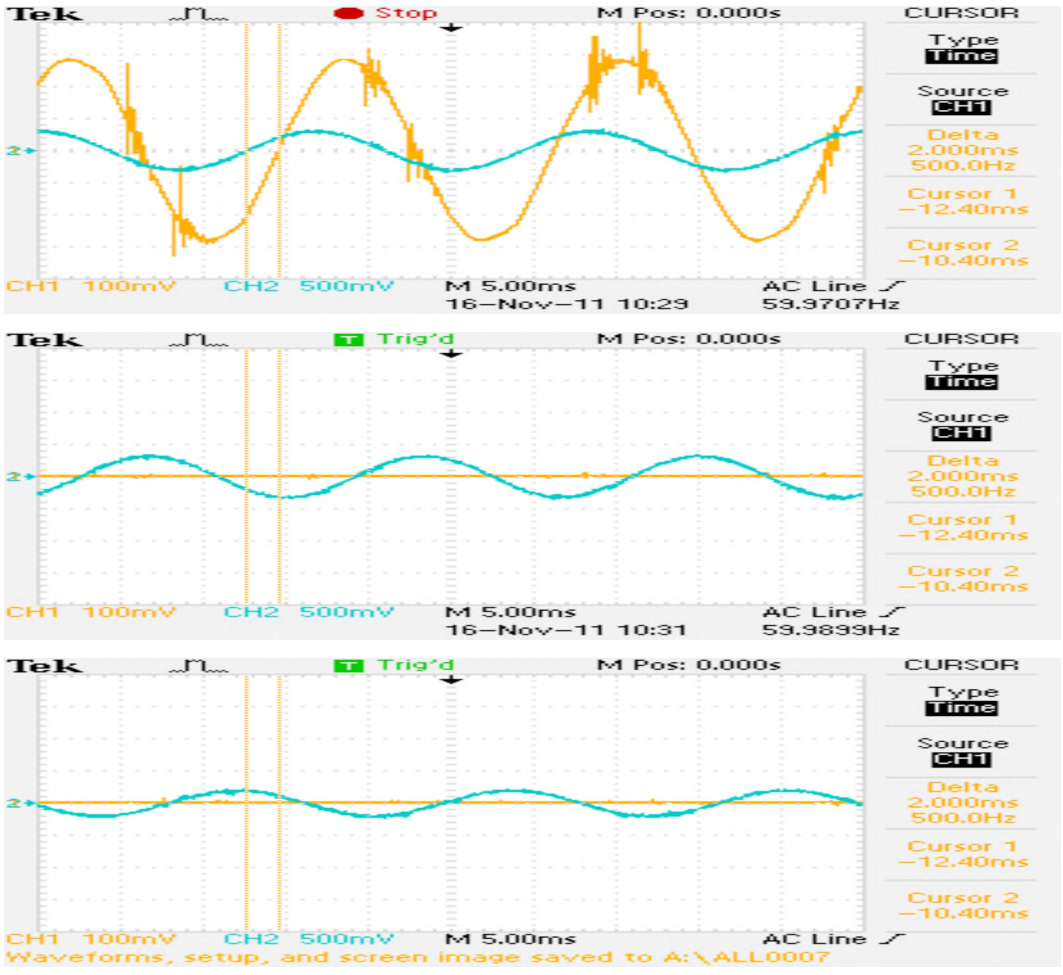

Figure 64: Voltage and Current in Phases A, B, and C, Case 7 (Experimental Results). Voltage probe: 20 mV/V. Current probe: 100 mV/A.

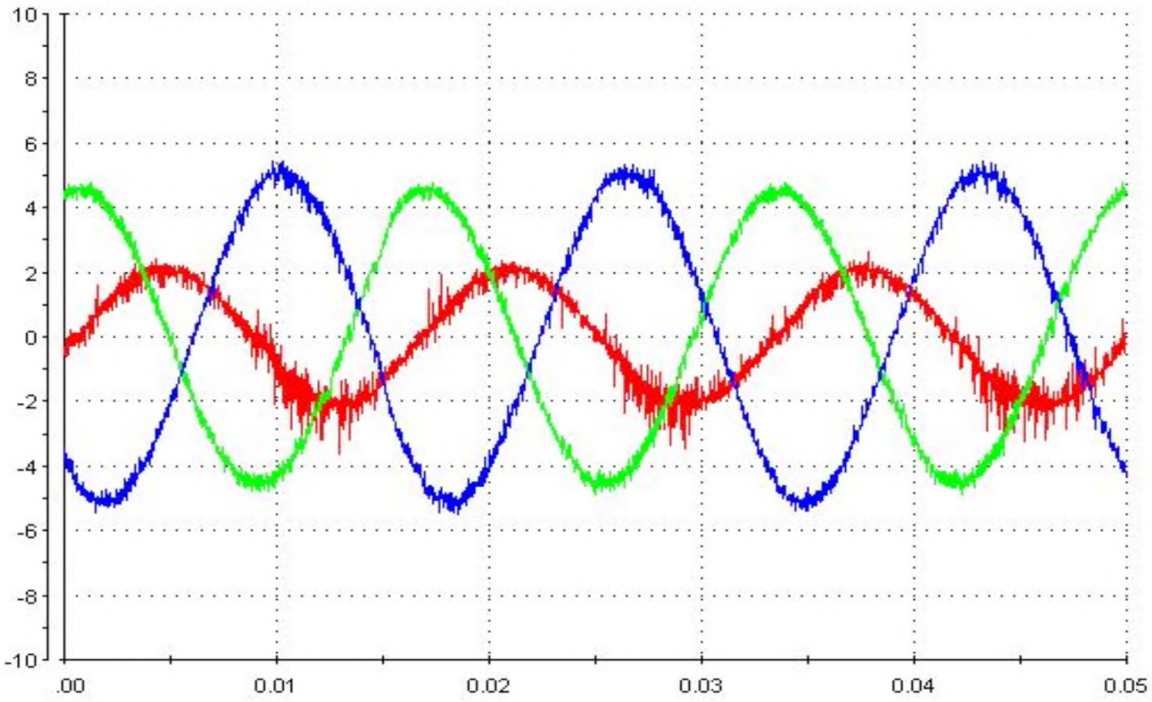

Figure 65: Grid Currents Under Unbalanced Grid Voltage and Unbalanced Line Impedance, Case 8 (Experimental Results).

CHAPTER VII

CONCLUSION AND FUTURE WORK

This thesis, addressed the increasing demand in renewable energy resources (RES), and explored various control methods used by the researchers today to successfully integrate them into the grid. Even though many ways have been shown, the unbalanced nature of the grid and the strict requirements cause the researchers to continually look for new improved methods. A new grid side inverter control method, tested under significant grid unbalance was proposed in this thesis. The method was shown to be general, capable to be used for all levels of unbalance in line voltages and impedances, providing complete harmonic elimination in line currents, with fully adjustable power factor, allowing bi-directional power flow. The analytical method has been presented. Based on the analytical solution, the control method was verified on a SIMULINK model for eight different cases of unbalance. The proposed control method has been also implemented in dSPACE and experimentally verified on the laboratory prototype. Experimental results obtained using a laboratory prototype are in excellent agreement with the simulation results. The proposed control technique demonstrated to produce high quality line currents under extreme unbalanced operating conditions.

As any new method, this control strategy is not without its limitations. The primary shortcoming is in the variable switching frequency which contributes to the losses, creates high frequency noise, and creates challenges for filter design. Good efforts to use constant switching frequency based on this control method were produced in [56] and [57] on a rectifier. A similar approach can be applied to the inverter. Additional power losses could have been minimized if the IGBT unit, instead of the MOSFET inverter was used in the experiment. Further work could include testing of the proposed method on the rectifier and the inverter, connected in back-to-back configuration. Also, since the unbalanced conditions are pre-determined ahead of time, and the controller responds to steady-state conditions of the unbalanced grid or load, more future work can be done to analyze the method's response during the initial conditions of the unbalance, while the real-time calculations are made to meet and respond to the given challenge.

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APPENDICES

A. MATLAB CODE (SIMULATION)

```
clc
clear
Ts=0.00002;
f=60;

%%%%%%%%%%%%%%%%%%%%%%%%%%%% Define the power %%%%%%%%%%%%%%%%%%%%%%%%%%%%

S=-50-0*j;      %Case 1 & 2
%S=-30-30*j;    %Case 3
%S=-30+30*j;    %Case 4
%S=-25-0*j;     %Case 5
%S=-15-15*j;    %Case 6
%S=-15+15*j;    %Case 7
%S=-50-0*j;     %Case 8

%%%%%%%%%%%%%%%%%%%%%%%% Define Inductance Values %%%%%%%%%%%%%%%%%%%%%%%%

R=0.0001;
L1=0.01;
L2=0.01;
%L2=0;
L3=0.01;

%%%%%%%%%%%%%%%%%%%%%%%%%% Define the relay point %%%%%%%%%%%%%%%%%%%%%%%%%

RE=0.02;

%%%%%%%%%%%%%%%%%%%%%%%% Define the unbalanced voltage %%%%%%%%%%%%%%%%%%%%

U1=10*(cos(0)+j*sin(0));
U2=10*(cos(-2*pi/3)+j*sin(-2*pi/3));
U3=10*(cos(2*pi/3)+j*sin(2*pi/3));
%U3=0;
%U2=0;
%U2=A2+A3;

%%%%%%%%%%%%%%%%%%%% Define the three phase input voltage %%%%%%%%%%%%%%%%%

V=zeros(1,3);
V(1)=U1;
V(2)=U2;
V(3)=U3;
VM=abs(V)*sqrt(2);
VA=angle(V)*180/pi;

%%%%%%%%%%%%%%%%%%%%%% Define the unbalanced impedance %%%%%%%%%%%%%%%%%%%%

Z1=2*pi*f*L1*j+R;
Z2=2*pi*f*L2*j;
Z3=2*pi*f*L3*j-R;
```

```
%%%%%%%%%%%%%%%%%%%%%% Giving the initial condition %%%%%%%%%%%%%%%%%%%%%%

I=zeros(1,3);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Calculation %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Up1=conj(U1);
Up2=conj(U2);
Up3=conj(U3);
Sp=conj(S);

a=-(Z1+Z3)-2*Z1*(Up3-Up1)/(Up1-Up2)-(Z1+Z2)*(Up3-Up1)^2/(Up1-Up2)^2;
b=-(U3-U1)-(Up3-Up1)*(U2-U1)/(Up1-Up2)-2*(Z1+Z2)*(Up3-Up1)*Sp/(Up1-
Up2)^2-2*Z1*Sp/(Up1-Up2);
c=-Sp*(U2-U1)/(Up1-Up2)-(Z1+Z2)*Sp^2/(Up1-Up2)^2;

delta=b^2-4*a*c;

%%%%%%%%%%%%%%%%%%%%%%%% Checking phase sequence %%%%%%%%%%%%%%%%%%%%%%%%

I(3)=(-b-sqrt(b^2-4*a*c))/(2*a);
I(2)=(Sp+I(3)*(Up3-Up1))/(Up1-Up2);
I(1)=-I(2)-I(3);

if angle(I(3))<angle(I(1))|| angle(I(2))>angle(I(1))

I(3)=(-b+sqrt(b^2-4*a*c))/(2*a);
I(2)=(Sp+I(3)*(Up3-Up1))/(Up1-Up2);
I(1)=-I(2)-I(3);

end

%%%%%%%%%%%%%%%%%%%% Solve for the reference current %%%%%%%%%%%%%%%%%%%%

IM=abs(I)*sqrt(2);
IA=angle(I);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Checking %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%P=S;
Vdc=60;
%SW1=U1*2*sqrt(2)/sqrt(R*P);
%SW2=U2*2*sqrt(2)/sqrt(R*P);
%SW3=U3*2*sqrt(2)/sqrt(R*P);
SW1=((U1+Z1*I(1))*2*sqrt(2))/Vdc;
SW2=((U2+Z2*I(2))*2*sqrt(2))/Vdc;
SW3=((U3+Z3*I(3))*2*sqrt(2))/Vdc;

SW1M=abs(SW1)
SW2M=abs(SW2)
SW3M=abs(SW3)
```

B. MATLAB CODE (EXPERIMENTAL)

```
clc
clear
Ts=0.00002;
f=60;

%%%%%%%%%%%%%%%%%%%%%%%%%%%% Define the power %%%%%%%%%%%%%%%%%%%%%%%%%%%%

S=50;
R=0.0001;
L=0.01;

%%%%%%%%%%%%%%%%%%%%%% Define the unbalanced voltage %%%%%%%%%%%%%%%%%%%%%%

U1=10*(cos(0)+j*sin(0));
U2=10*(cos(-2*pi/3)+j*sin(-2*pi/3));
U3=10*(cos(2*pi/3)+j*sin(2*pi/3));

%%%%%%%%%%%%%%%%%% Define the three phase input voltage %%%%%%%%%%%%%%%%%%

V=zeros(1,3);  % V(1)=0, V(2)=0, V(3)=0 initially

V(1)=U1;
V(2)=U2;
V(3)=U3;

VM=abs(V)*sqrt(2);
VA=angle(V)*180/pi;

%%%%%%%%%%%%%%%%%%%% Define the unbalanced impedance %%%%%%%%%%%%%%%%%%%%%%

Z1=2*pi*f*L*j+R;
Z2=2*pi*f*L*j;
Z3=2*pi*f*L*j-R;

%%%%%%%%%%%%%%%%%%%%%%% Giving the initial condition %%%%%%%%%%%%%%%%%%%%%%

I=zeros(1,3);

%%%%%%%%%%%%%%%%%%%%%%%%%%%% Calculation %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Up1=conj(U1);
Up2=conj(U2);
Up3=conj(U3);
Sp=conj(S);

a=-(Z1+Z3)-2*Z1*(Up3-Up1)/(Up1-Up2)-(Z1+Z2)*(Up3-Up1)^2/(Up1-Up2)^2;

b=-(U3-U1)-(Up3-Up1)*(U2-U1)/(Up1-Up2)-2*(Z1+Z2)*(Up3-Up1)*Sp/(Up1-
Up2)^2-2*Z1*Sp/(Up1-Up2);

c=-Sp*(U2-U1)/(Up1-Up2)-(Z1+Z2)*Sp^2/(Up1-Up2)^2;
```

```
%%%%%%%%%%%%%%%%%%%%%%%% Checking phase sequence %%%%%%%%%%%%%%%%%%%%%%%%

I(3)=(-b-sqrt(b^2-4*a*c))/(2*a);
I(2)=(Sp+I(3)*(Up3-Up1))/(Up1-Up2);
I(1)=-I(2)-I(3);

if angle(I(3))<angle(I(1))|| angle(I(2))>angle(I(1))

I(3)=(-b+sqrt(b^2-4*a*c))/(2*a);
I(2)=(Sp+I(3)*(Up3-Up1))/(Up1-Up2);
I(1)=-I(2)-I(3);

end

%%%%%%%%%%%%%%%%%%%%%% Solve for the reference current %%%%%%%%%%%%%%%%%%%%

IM=abs(I)*sqrt(2);
IA=angle(I);
```