A new embedded control system for SUSI

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ABSTRACT

The Sydney University Stellar Interferometer uses embedded processors to control each siderostat station as well as other major components of the instrument. The maintenance of the original controllers has become a significant issue and we set out to design a new system that would be inexpensive, suitable for the relatively harsh operating environment and simple to maintain. We have demonstrated that the new system works satisfactorily and we are currently replacing the existing controllers with new ones.

Keywords: control system, embedded processor, stellar interferometry

1. INTRODUCTION

The Sydney University Stellar Interferometer is located at the Paul Wild Observatory, near Narrabri in northern New South Wales. It consists of a North-South array of input stations (siderostats) and the available baselines range from 5 m to 640 m.[1] The original control system[2] used embedded or distributed processing, but the technology is now obsolete and maintenance and repair has become a major problem. We set out to develop a replacement system that meets the following criteria: low cost, simple to maintain, robust and able to operate over a wide temperature range. A new controller for one major SUSI subsystem (the longitudinal dispersion corrector or LDC) has been installed and we are currently installing controllers for the siderostat stations.

2. THE ORIGINAL CONTROL SYSTEM

Each major subsystem in SUSI has its own embedded processor. The subsystems include the siderostat stations, the optical path length compensator, and the longitudinal dispersion corrector. Each controller consists of two parts: a single-board computer based on the Motorola 6800 processor and a finite state machine (FSM). The computer was an "AV68K" made by Avenue Electronics in Burwood East, VIC. The FSM comprises several large printed circuit boards with discrete TTL logic circuitry, digital-to-analog converters (DACs), etc. Six TTL registers are mapped onto the memory space of the 6800 to allow the transfer of data between the computer and the FSM. The FSM in turn is directly wired to the switches, motor amplifiers, and shaft encoders on the equipment.

The siderostat stations are located up to 300 m from the central laboratory. At the time SUSI was constructed fiber optics were not available and consequently the stations are connected to the center using serial (RS232/432) links. This means that communication between the stations and the center has limited bandwidth. Consequently the graphical user interfaces (UI) for the embedded systems were designed as separate applications that run on a Linux machine in the main control room. A simple data transfer protocol was designed to link the UIs with the embedded processor.

It should be emphasized that the only data exchanged between the stations and the center are "engineering" data such as motor rates, shaft encoder readings, etc, and this does not require a wide bandwidth. The "science" data in SUSI is handled completely separately. It is worth noting that the simple design of the UI system along with the low data rates made it feasible to implement a remote observing mode. This was first demonstrated with the CHARA Array[3] and a similar mode has been adopted for SUSI. The UI also interfaces to the rest of SUSI with a TCP/IP messaging system based on the CHARA messaging system. This enables control and communication by a queue scheduler or graphical UIs based in Sydney or elsewhere in the world.

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Figure 1. One of the single-board computers used as embedded processors in SUSI.

The AV68K computer (Fig. 1) had a clock speed of 20 MHz and the FSM used a 5 MHz clock derived from the 20 MHz signal. In addition there was a clock signal with an 80 ms period. The siderostat control program was implemented as an interrupt server triggered by the 80 ms pulse. This same signal is used by the FSM to latch and buffer all the data from the siderostats. It then checks for any user input on the serial line, processes the data as required, output new settings to the FSM and sent any requested information back to the UI via the serial link.

The siderostats are driven by precision stepper motors operating in a microstepping mode. This means that they operate with digitally synthesized sine and cosine waveforms. The advantage of stepper motors is that their maximum torque occurs at low speeds; in the case of the siderostats the maximum shaft speed is 1 revolution per second. The siderostat positions are monitored by two encoders for each axis. A 0–359 absolute encoder attached to each siderostat shaft gives the shaft position to within one degree. The gearing between the motors and the siderostat shafts is 360:1, so one rotation of the motor also corresponds to one degree. A 1024 line incremental encoder is attached to the motor shaft to interpolate the absolute encoder readings. The FSM has two 10-bit registers to keep track of the incremental encoder changes for the azimuth and elevation axes. These registers as well as the absolute encoder readings, were read by the control program every 80 ms.

In the original system the motor signals were generated by the FSM. The AV68K controlled the rate using binary rate multipliers. The output of the multipliers was used to step through look-up tables and DACs were used to convert the output to analog signals. When the FSM was powered on, or in the event of a computer malfunction, the FSM could generate undefined rates. Override switches were installed to prevent this from happening but it was still possible to have uncontrolled motion of the siderostats.

Essentially the same controller was also used for the longitudinal dispersion corrector (LDC). This system consists of a set of moveable glass blocks and wedges that are used to compensate for the dispersion introduced by the optical delay line, which is in air rather than vacuum. The wedges were driven analogously to the siderostat axes, and the limit switches for the wedges and blocks were connected directly to the AV68K memory registers. Ideally these switches should have been latched but this would have meant designing a new FSM. It was found in practice that the 80 ms interrupt period meant that the state of the switches were occasionally misread; the system could only be restored by manually positioning the wedges and blocks and then restarting the system.

Fig. 2 shows the electronics bay for one of the original siderostat stations. In addition to the single-board computer and the FSM it also contains power supplies and power amplifiers for the station motors. The power

Figure 2. Part of the electronics station at a siderostat. The upper module is the FSM consisting of four hand-wired circuit boards and a power supply. The module beneath it is the single-board computer and its power supply.

supplies and amplifiers have proved to be extremely robust and we have no immediate plans to replace them. To minimize the effects on the local "seeing" the electronics are located in cabinets away from the actual siderostat optics. The temperature inside the cabinets can range from below 0°C to over 40°C; in the summer the operation of the electronics can become unstable.

3. DESIGN CONSIDERATIONS FOR THE NEW SYSTEM

The goal was to build a robust, affordable system from off-the-shelf components. The exact choice of hardware, however, was dictated by several design criteria that we discuss below.

3.1 Time-critical operations

There are three parts of the control system which are time-critical: the system that generates the analog signals for the stepper motors, the counters that keep track of the incremental encoders and the main processing thread.

3.1.1 The motor signals

Any latency in outputting the analog sine and cosine waveforms to the motor amplifiers will result in irregularities in the motor drive and consequently affect tracking. It was decided to implement the control program using three threads: a main control thread and two threads that are dedicated to sending rate signals to the azimuth and elevation axes. Obviously the details of the timing for the threads would depend on the final decision regarding the processor and associated interface electronics and we return to this in section 3.4. A related issue is the accuracy of the DAC used to convert the digital signals to analog waveforms. If the digitization is too coarse it will degrade the tracking performance.

3.1.2 The incremental encoders

It is essential that all the incremental encoders pulses are recorded. In the original controller this was done by the FSM which has its own registers for keeping track of the encoder outputs. There are two possible solutions. The first is to use computer which is fast enough not to miss any encoder pulses. It would almost certainly need a real-time operating system in order to reliably register all the encoder signals. This did not appear to be a particularly economical solution.

The alternative was to use an external counter to keep track of the encoder signals. The LabJack U3[4] offers this capability. This is a general purpose digital input output (DIO) unit that interfaces to a host computer via a USB port. The individual channels are highly configurable. In particular two channels can be configured as a 32-bit "quadrature counter" that is ideally suited for most incremental encoders, which typically have quadrature outputs. The output of the LabJack quad counter is a signed number that represents the number of steps since the last reset of the counter. The increased capacity of the counter compared to the 10-bit range of the original system greatly simplifies the algorithm for determining the shaft positions.

The LabJack U3 has a built-in DAC, but its resolution was not sufficient for our purposes. However the "LJTickDAC" is an accessory that can be added to the LJ U3. It converts two DIO channels to a 14-bit precision DAC with a range of $\pm 10\,\mathrm{V}$ (with no power supply other than the USB port).

3.1.3 The main processing thread

In the original system the AV68K controller was implemented as an 80 ms interrupt process. As noted in 2 this was not fast enough to reliably register all the switch data. While not as critical as the other two timing issues it was clear that the average cycle time for the main processing thread would need to be significantly less than 80 ms.

3.2 Communication

One of the weaknesses of the original system was the serial communication link between the embedded controllers and their associated UIs, which ran on a computer in the main SUSI control room. The protocol was not sufficiently robust, and communication failures occurred frequently. It was decided to merge the UI and the actual control program at the ARK-1370 and use standard TCP/IP to link the stations to the center. The current SUSI UI libraries are still based on the original ones and consequently do not require high bandwidths.

3.3 Environmental considerations

As mentioned in section 2 the stations are subject to a wide range of temperatures and it became clear that any implementation would need to use components that are rated for industrial applications. In addition the environment can be very dusty sometimes and extremely humid at other times. The system is also required to operate remotely and robotically for years without regular maintenance.

The LabJack U3 has an operating temperature range of $-40°$ C to $85°$ C. As well it has an inbuilt sensor that can be used to monitor the temperature. We identified the ARK-1370 computer[5] as being suitable. This is designed for industrial process control, kiosk operation, etc., and uses flash memory rather than a hard disk drive. It has an operating range of $-40°$ C to $60°$ C.

3.4 Final hardware and software specification

The final specification for each station was one ARK-1370, two LabJack U3s and two LJTickDACs. The only custom electronics that are required are differential line drivers/receivers used with the incremental encoders. The driver/receiver boards have only two TTL circuits each, and they have been socketized to facilitate field repair if necessary.

To make the new embedded control system consistent with the rest of SUSI it was decided to install Linux on the ARK-1370s. As a consequence it was possible to migrate the UI to the ARK-1370 and integrate it with the hardware controller. The UI runs as the main thread of the program; two other threads are used to send rates to the motors via the LJTickDAC.

The ARK-1370 is the slowest in that particular family of computers and we decided to trial it as the new LDC controller to see if it was fast enough for our application.

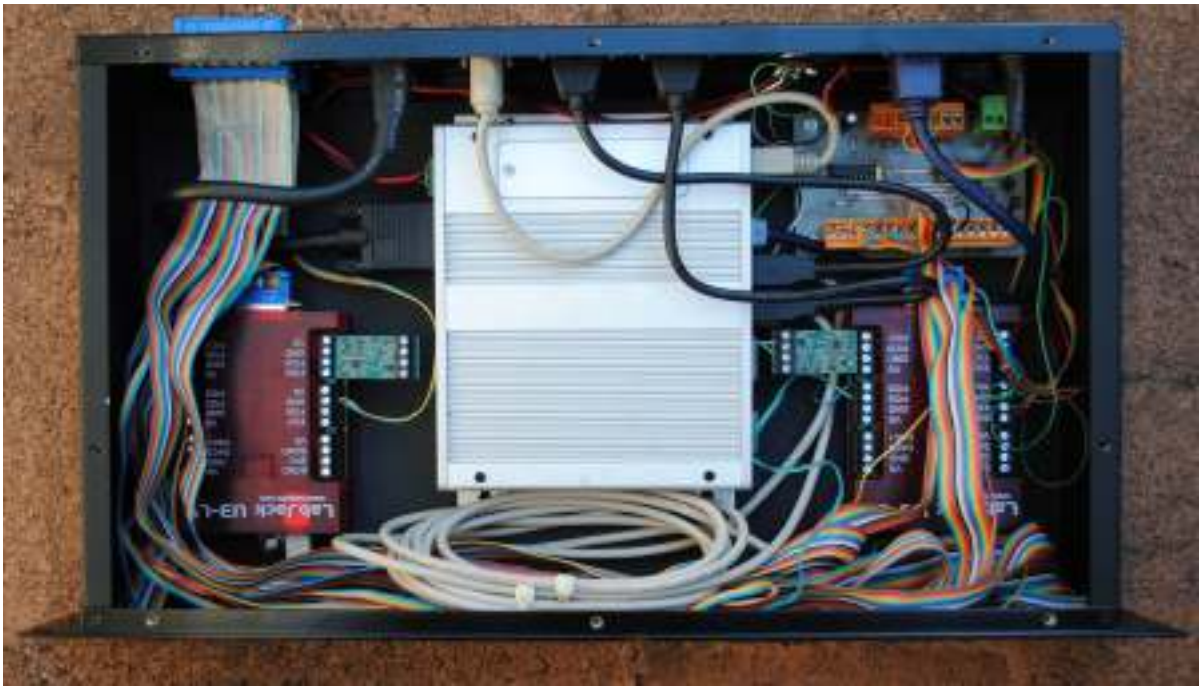

Figure 3. The new controller for the siderostats and longitudinal dispersion corrector (LDC). The unit shown is the LDC controller, which currently only uses one LJTickDAQ. The ARK-1370 and the two LabJacks fit into a 2 unit high 19 inch rack chassis. The small printed circuit board at the upper right is the differential line receiver for the incremental shaft encoder.

4. INTEGRATION, TESTING AND PERFORMANCE

Fig. 3 shows the final version of the controller built for the longitudinal dispersion corrector (LDC) in SUSI. All the components fit into a standard 19 inch chassis (two units high). The ribbon cables seen in the figure connect to rear panel sockets; cables from the external equipment plug into these sockets. The remaining cables are the USB cables connecting the LabJacks to the ARK-1370 computer and extension cables that connect the spare USB, VGA, Ethernet and keyboard/mouse inputs on the computer to the back panel.

When sending rates to the motors the average time required to update the two LJTickDAC channels has been found to be ~ 15 ms. When tracking the motors are driven with "microsteps" and the output signals in volts are

$$A(t) = 10\sin(2\pi f[t - t_0]) \quad (1)$$

$$B(t) = 10\cos(2\pi f[t - t_0]) \quad (2)$$

where f is the demand frequency and t_0 is the time when the current tracking operation commenced. The motors have 200 steps per revolution and the gearing between the motor shaft and the siderostat shaft is 360:1. If the required shaft speed in arcsec/s is $\omega''/72$ Hz.

Slewing is accomplished by driving the motors as conventional stepper motors. Assuming a stepping period of 15 ms per step this gives a slew speed of $0.33^\circ \cdot s^{-1}$. This is somewhat slower than the slew speed of the old system but is entirely adequate.

The risk of uncontrolled motion of the siderostats has been virtually eliminated with the new system. Because the motor drive signals are generated in software and in the event of a computer crash the signals will no longer be updated and the motors will stop.

The time to execute one cycle of the main processing thread has been found to be ~ 25 ms. Most of this time is associated with reading and writing data to the LabJacks. In the case of the LDC this has virtually

eliminated the risk of missing a limit switch signal. As a consequence we decided to use this system to replace all the AV68K processors at SUSI. The LDC processor was installed in early 2010 and the siderostat embedded processors are currently being replaced.

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