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Implementing Inverse Design Tools for Plasmonic Digital Logic Devices

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ABSTRACT

Despite the benefits that optics and photonics have brought to improving communications, there remains a lack of commercialized optical computing devices and systems, which reduces the benefits of using light as an information-carrying medium. We are developing architectures and designs of photonic logic gates for creating larger-scale functional photonic logic circuits. In contrast to other approaches, we are focusing on the development of logic devices which can be cascaded in arbitrary ways to allow for more complex photonic integrated circuit design. Additionally, optical computing often uses on-off keying, which fails to take advantage of denser encoding schemes often used to optically transmit data. We propose that devices that operate on phase-shift keying will not only be more efficient, but easier to cascade. To achieve the goal of cascadable devices operating on phase-shift keying, we have designed a plasmonic waveguide logic device using inverse design tools. These tools have allowed us to create a device with an arbitrary topology that has increased performance and reduced footprint compared to a conventional device with the same operation. In addition, inverse design simplifies the process of designing devices that operate with phase-shift keying, which can become complicated with conventional design methods. In order to implement inverse design tools for plasmonic devices and phase-shift keying, we used fully 3D FDTD simulations. We compare the inverse-designed devices to more conventional devices in order to characterize their performance.
Keywords: plasmonics, photonic logic, inverse design, photonic integrated circuits, plasmonic devices

1. INTRODUCTION

Conventional communication links typically rely on light to transmit information, but use electronic signals to process it[1–3]. By replacing the electronic processing with photonic circuits, we can allow for faster, lower power data transfer[4–6]. In other words, we can achieve increased information processing speed and higher-density information encoding as well. Typically, light intensity acts as an input and output for logic gates, but by using other encoding mechanisms, such as phase-shift keying (PSK), we can increase the density of our encoding.

Additionally, there are numerous photonic device architectures and geometries that are studied for use in photonic logic devices[7–10]. However, these architectures and geometries are often not compatible with one another, which is a barrier to designing large and complex photonic integrated circuits.

Our goal is to use surface plasmon polariton (SPP) waveguides to build faster and more compact logic gates. SPPs are electromagnetic surface waves that travel along a metal-dielectric interface. They have many benefits, including tight optical confinement which leads to small device footprints[11]. Using SPPs, which can be coupled beyond the diffraction-limit, we can construct photonic logic gates at the nanoscale.

To design and optimize a plasmonic logic gate, we use Lumerical FDTD, a photonic simulation software. Within Lumerical, we design our devices using a dielectric-loaded SPP (DLSPP) architecture. They consist of a metal layer on top of a substrate with a dielectric strip to define the waveguide. We are using binary

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phase-shift keying (BPSK) to encode the input and output of our device. Lumerical also provides us with multiple forms of optimization. For this work, we focus on using the inverse design optimization tools provided with Lumerical[12]. We compare the efficiency of both inverse and conventional designs and verify that inverse design creates a more compact, efficient design.

2. METHODS

2.1 Circuit Architecture

The plasmonic device uses silica stripes on gold film (Figure 1). Silica waveguides are used to help mitigate traditionally heavy loss exhibited by plasmonic circuits. This DLSPP architecture also provides a benefit when using inverse design tools, as we can optimize the dielectric material on top of the metal layer, reducing the complexity of the optimization task. The simulations are run with an operating wavelength of 1,550 nm, which is a typical wavelength used in optical communications.

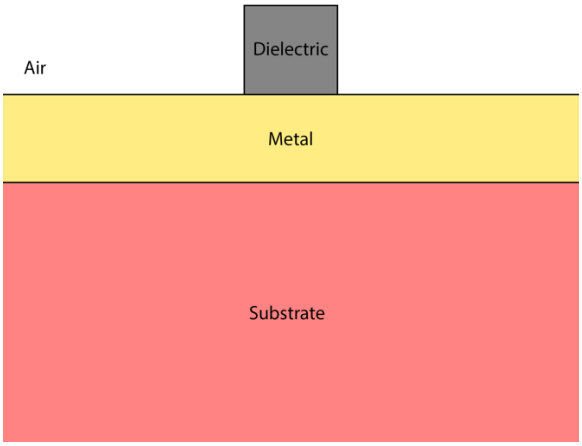

Figure 1. Schematic cross-section of dielectric-loaded surface plasmon polariton waveguides. The metal material is gold and the dielectric material is SiO_2.

2.2 Designing an XOR gate

To initiate the procedure of designing photonic logic components, we chose to design an XOR gate, which lends itself particularly well to certain inverse design constraints and our use of binary phase-shift keying. Consider the conventional XOR gate, which has two inputs and 1 output. The output of the XOR gate is 1 if the two inputs are different from each other. When they are the same, the output is 0. Using BPSK, we assign 0° of phase to the logic 0 and 180° of phase to the logic 1 (Table 1). Therefore, the output of the logic gate should be 180° if the inputs are out of phase, and 0° if the inputs are in phase. For our photonic logic gate, the goal was to use two waveguides as inputs and a single output, but due to constraints with the inverse design tools, we initially design the device with two outputs and on-off keying at these outputs.

2.3 Optimization

To optimize our photonic logic gate and explore the effectiveness of inverse design tools for this purpose, we compared simple conventionally-designed devices to a device designed with an inverse design optimization.

The inverse design tools allow us to define inputs and a figure of merit (output), and uses an adjoint-method based optimization to optimize the topology of a pre-defined region based on those constraints[13]. Traditional design, which is often guided by intuition, often involves parameter sweeps and is time-consuming if one wants to explore a large portion of the parameter-design space. Because inverse design uses gradient based algorithms to compute a set figure of merit in an iterative loop, fewer simulations are needed to explore the design space and the result is more compact designs with better performance using less time than conventional design methods.

Table 1. XOR logic gate operation with phase-shift keying.

Input A	Input B	Output
Logic 0: 0° phase	Logic 0: 0° phase	Logic 0: 0° phase
Logic 0: 0° phase	Logic 1: 180° phase	Logic 1: 180° phase
Size of each file	Logic 0: 0° phase	Logic 1: 180° phase
Logic 1: 180° phase	Logic 1: 180° phase	Logic 0: 0° phase

3. RESULTS

The results of conventionally-designed multi-mode interferometers (MMIs) designed with the goal of using them for an XOR gate are shown in Figure 2. The plots show the power of the optical fields in the device. For both simulations, the relative phase difference of the inputs is 180°, and the device is 10 μm wide. The position of the input waveguides is shifted between the two simulations. These designs demonstrate how varying a single parameter (spacing between input waveguides) leads to drastically different results. The goal of designing an XOR gate is made much more difficult when relying solely on conventional design.

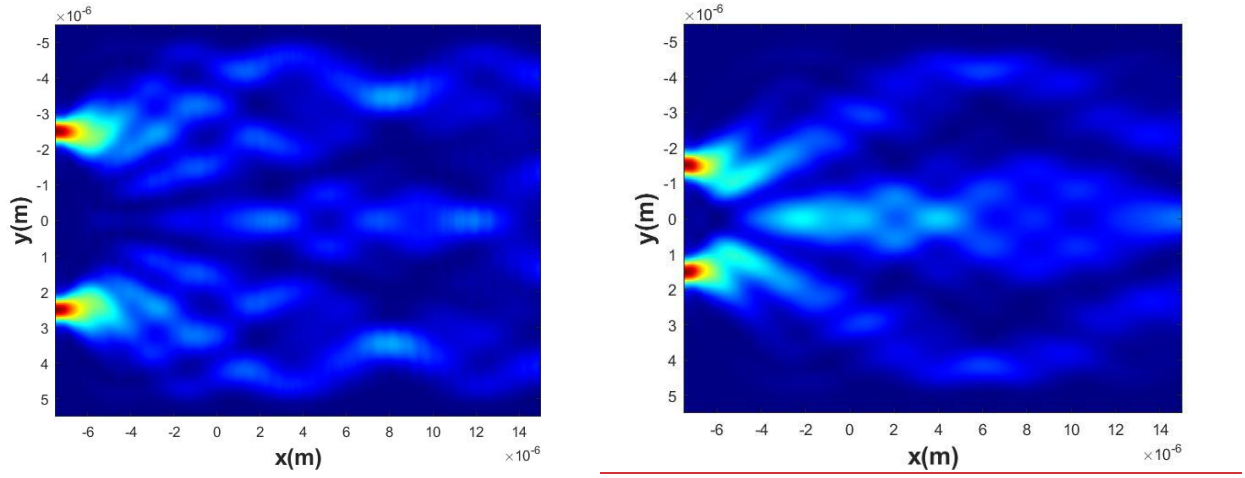

Figure 2. FDTD simulation results of conventionally designed MMIs with sources 180° out of phase.

In contrast, using inverse design tools, we can accomplish complex design over multiple parameters more efficiently. For this design, we used two inputs and two outputs. We specified the relative phase of the inputs (in phase or 180° out of phase) and a single output waveguide for each condition. Figure 3 shows simulation results from inverse-designing the XOR gate. These simulations also show the power of the optical fields in the device. The simulation results show that the light will be sent to different outputs based on the relative

phase of the inputs. And in fact, the behavior shown in the simulations can be considered an XOR operation, with BPSK encoding at the inputs and on-off keying encoding at the outputs.

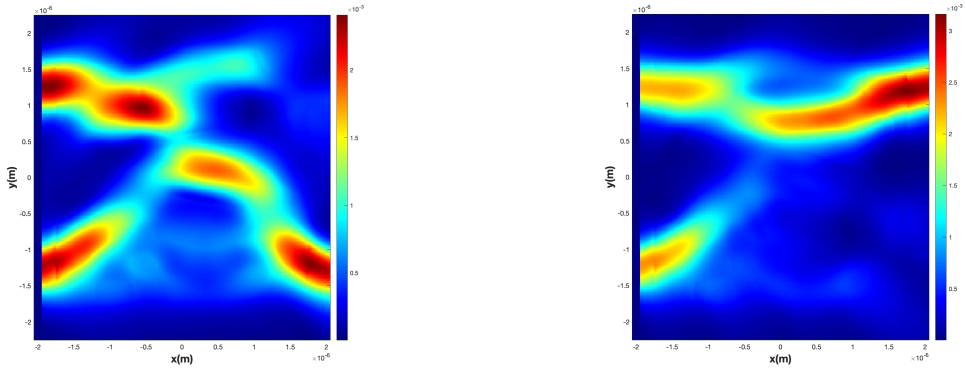

Figure 3. FDTD simulation results of inverse-designed XOR gate. On the left, the inputs are in phase and the signal is active at the bottom output. On the right, the inputs are 180° out of phase and the signal is active at the top output.

4. CONCLUSION AND FUTURE WORK

We have demonstrated the feasibility of using plasmonic devices to construct logic gates, allowing for smaller, more efficient digital photonic components. In particular, we designed a plasmonic waveguide device using a DLSPP architecture that exhibits XOR-gate behavior using PSK-encoded inputs. Furthermore, we verified the advantages of inverse design for this process. These findings will allow us to optimize designs for other devices that behave as photonic logic gates. In the future, we will consider other digital logic gates, and consider how to re-encode the output to PSK, with the end goal of creating larger, more complex photonic integrated circuits.

5. ACKNOWLEDGEMENTS

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