Amplifier MMICs for Electrosurgical Devices and Microwave Therapeutic Systems

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Abstract

Advancement in semiconductor technologies and fabrication processes has enabled the development of advanced microwave circuits having the capability to generate high enough levels of microwave power at an affordable cost. These circuits that were once used in the communications sector have found applications in electrosurgical devices and microwave therapeutic systems during the past decades, due to the non-ionising nature of microwave energy and its interaction with the human body that can be defined in terms of electrical properties. Electrosurgical devices and therapeutic systems are being widely used for the treatment of various medical conditions like tumours, cancer, ablation, coagulation, atrial-fibrillation, wound sterilisation, enhanced liposuction, keratoconus, endoscopic, laparoscopic and open surgeries; with RF cutting, coagulation and ablation being the most popular biomedical modalities. However, many challenges need to be overcome, a few of which include focused power delivery and tissue dissection with small depth of effect, smart and integrated high efficiency power sources, localised generation of microwave power close to the treatment site to reduce transmission losses and distributed tissue heating, and large size of microwave power generators that are difficult to employ beyond specialised medical facilities, especially in portable electrosurgical devices. Research work presented in this thesis targets above mentioned limitations of microwave power sources by exploiting recent advances in high efficiency power amplifier and oscillator circuits; especially class AB, class J, class F, class F^{-1} power amplifiers and class E switching mode oscillators, that can be developed using discrete or Monolithic Microwave Integrated Circuit (MMIC) fabrication technologies.

High efficiency discrete power amplifiers operating at 5.8 GHz ISM (Industrial Scientific and Medical) band frequencies developed during the scope of this PhD research include: class AB amplifier that provides 13 W continuous wave (CW) output power with 62.1 % power added efficiency (PAE), class F amplifier that provides 15.2 W CW power with 55.2 % PAE, and multistage amplifier with class AB and class F amplifiers in gain and power stages, respectively that provides 21.9 W CW output power with 65.4 % DC to RF efficiency. The amplifiers were tested and validated to effectively cause coagulation on liver bench test model with controlled depth of effect. An application envisioned for discrete amplifiers is portable field haemostasis.

High efficiency class E oscillator and class AB amplifier were developed using WINPP10-15 GaAs MMIC process from WIN Semiconductors foundry. Class AB amplifier provides 17.43 dBm output power with 49 % PAE at 30 GHz, while class E oscillator provides 24 dBm output power with 40 % DC to RF efficiency at 14.5 GHz. These results are based on large signal simulations with EM simulated circuit elements. Initial small signal on-wafer measurements of class AB MMIC die showed similar trends; however, comparison between simulated and measured results indicated inaccuracies in MMIC process design kit models. On-wafer measurements of class E oscillator were performed at reduced bias conditions due to limited power handling capability of the bias tees at the measurement facility. Clean oscillations with 16.4 dBm output power and 27.9 % DC to RF efficiency at 10.7 GHz were obtained. Further tests will be performed after packaging the MMIC dies followed by mounting on a custom designed PCB evaluation board. Class E oscillator and class AB amplifier MMICs are envisaged for application within an endoscopic channel for localised power generation close to the treatment site, and an on-chip diagnostic and neutralisation system, for medulloblastoma and glioblastoma highly malignant grade IV cancerous cells, respectively.

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Dedication

To,

My mummy jaan, Professor Zohra Zaka;

and

My little champ, Haider.

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Manchester,
December 2019.

Publications

1. A. M. A. Pirkani, C. I. Duff, R. Sloan, C. P. Hancock, and S. Preston, 'High Efficiency Amplifier for use in portable Haemostatic Applications - Part A', *ARMMS RF Microw. Soc. Dig.*, p. 5, Nov. 2017.
2. A. M. A. Pirkani, S. Preston, C. I. Duff, R. Sloan, and C. P. Hancock, 'High Efficiency 5.8 GHz Class F and Class J Amplifiers with Portable Haemostatic Applications', in *2019 49th European Microwave Conference (EuMC)*, 2019, pp. 157–160.
3. A. M. A. Pirkani, C. I. Duff, R. Sloan, and C. P. Hancock, 'High Efficiency Class E MMIC Oscillator for X-band Medical Applications - Part A', *ARMMS RF Microw. Soc. Dig.*, Nov. 2019.
4. A. M. A. Pirkani, S. Preston, C. I. Duff, R. Sloan, and C. P. Hancock, "GaN HEMT Power Amplifier and Applicator Structure for Microwave based Medical Applications" in *Postgraduate Research Poster Conference, 2016*, School of EEE, The University of Manchester, UK.

Submitted Publications

1. A. M. A. Pirkani, S. Preston, C. I. Duff, R. Sloan, and C. P. Hancock, 'High Efficiency 5.8 GHz Class AB, Class F and Class J Amplifiers with Portable Haemostatic Applications', in *International Journal of Microwave and Wireless Technologies*, 2020.

Participation in Student Competitions and Awards

1. Participated in student design competition with class F high efficiency amplifier at International Microwave Symposium 2017 at Hawaii, USA.
2. Received Young Engineer Award from ARMMS RF & Microwave Society to attend society meeting in November 2017 and November 2019.
3. Received PhD Student Sponsorship from IEEE MTT-S society to attend International Microwave Symposium 2017 at Hawaii, USA.
4. Received Student Award from European Microwave Association (EuMA) to attend European Microwave Weeks at London and Paris in 2016 and 2019, respectively.
5. Received runner up prize for best paper at RF and Microwave Society ARMMS November 2017 conference.
6. Received runner up prize for the best poster at Postgraduate Summer Research Conference (PGSRC) held at the University of Manchester in 2016.

List of Abbreviations and Symbols

RF	Radio Frequency
EM	Electro Magnetic
AC	Alternating Current
ESU	Electrosurgical Unit
GaAs	Gallium Arsenide
InP	Indium Phosphide
SiC	Silicon Carbide
GaN	Gallium Nitride
Si	Silicon
Al	Aluminium
PAE	Power Added Efficiency
$[S]$-parameters	Scattering parameters
MESFET	Metal Semiconductor Field Effect Transistor
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
MMIC	Monolithic Microwave Integrated Circuit
MIC	Microwave Integrated Circuit
AlGaN	Aluminium Gallium Nitride
InGaAs	Indium Gallium Arsenide
AlGaAs	Aluminium Gallium Arsenide
InAlAs	Indium Aluminium Arsenide
FET	Field Effect Transistor
2DEG	Two Dimensional Electron Gas
2DHG	Two Dimensional Hole Gas
BJT	Bipolar Junction Transistor
IV	Current Voltage
PUF	Power Utilisation Factor
MODFET	Modulation Doped Field Effect Transistors
DC	Direct Current
pHEMT	Pseudomorphic High Electron Mobility Transistor
CW	Continuous Wave
ADS	Advanced Design System
PCB	Printed Circuit Board

DRC	Design Rule Check
MoM	Method of Moments
MWO	Microwave Office
Q-factor	Quality factor
SAR	Specific Absorption Rate
HR	Heating Rate
RFA	Radio Frequency Ablation
VCO	Voltage Controlled Oscillator
CNS	Central Nervous System
iMRI	Intra-operative Magnetic Resonance Imaging
MS	Microstrip
CPW	Coplanar Waveguide
TFR	Thin Film Resistor
COV	Capacitor on Via
CS	Common Source
CG	Common Gate
MIM	Metal Insulator Metal
Y-parameters	Admittance Parameters
GSG	Ground Source Ground
GSGSG	Ground Source Ground Source
f	signal frequency
ω	signal angular frequency
V_{DS}	drain to source DC bias voltage
V_{GS}	gate to source DC bias voltage
V_{ds}	drain to source DC plus signal voltage
V_{gs}	gate to source DC plus signal voltage
I_{ds}	drain to source DC plus signal current
I_{gs}	gate to source DC plus signal current
R_{ds}	transistor's output resistance
R_i	transistor's input resistance, or charging resistance
C_{ds}	transistor's output capacitance (drain to source capacitance)
C_{gs}	transistor's input capacitance (gate to source capacitance)
C_{ds}	gate to drain capacitance
R_{on}	transistor's on resistance

Chapter 1

Introduction

1.1 Background

RF and microwave devices have effectively found applications in the field of medicine and opened new dimensions for research and development. The concept of Electrosurgery involves the use of RF or microwave alternating current sources to generate high enough energy to cause an intercellular rise in temperature to achieve vaporisation of tissue, desiccation, resection and coagulation. Biological effects of alternating current on human tissues were studied by Arsené D' Arsonval in 1893, which laid foundations for employing the concepts of blood coagulation and resection together to reduce bleeding during surgical procedures. Arsonval defined the process as fulguration, where capacitors were used to develop a high voltage discharge in the form of sparks to burn intended tissue site; however, his student Rivère modified the spark and applied it directly to the tissue site to perform coagulation without creating a spark [1]. Electrosurgical devices and therapeutic systems have been in use for several decades now, with the first device presented by Bovie in the 1920s. The electrosurgical unit developed by Bovie was used by Cushing, a neurosurgeon, to remove a mass from a patient's head by using RF energy to cause coagulation and cutting [2].

De Forest's invention of the "Audion" in 1907 (US patent 879,532) was a triode-containing vacuum tube to amplify electrical signals for radio broadcasting. Audion facilitated the development of high frequency AC signals for coagulation and tissue vaporisation. These inventions laid the foundation for Bovie's ESU which was developed into commercial unit operating at 1 MHz in the 1950s to perform neurosurgical treatments; and continued to be used as a model for all subsequently produced ESUs until the invention of solid-state generators and isolators in the 1970s [3]. Research about the interaction between RF and microwave energy and biological tissues in the 1970s was focused on thermal effects that occurred as a result of the transformation of energy entering the tissues into increased kinetic energy [4]; which was defined as key factor for the production of general heating in the tissue. The electromagnetic field spectrum has however demonstrated biological significance in terms of thermal heating between 1 MHz and 100 GHz because these fields can be readily transmitted, absorbed and reflected at the biological tissues and their boundaries [5].

There have been some controversies regarding health issues and potential adverse effects of RF and microwave field exposure. However, many beneficial effects of using high power RF energy for tissue heating have been used in the treatment of tumours. Medical applications of RF and microwave energy in the past were restricted to applications based on heating and medical diagnostic. The treatment of hyperthermia that involves RF heating had been in practice for over half a century while diagnostic applications of RF and microwaves involve dielectric constant measurements to assess the condition and properties of target tissue. However, more recent studies and development of medical applications involve RF ablation, coagulation, tissue resection, wound sterilisation, atrial fibrillation, enhanced liposuction, keratoconus and endoscopic, laparoscopic and open surgeries.

1.2 Motivation

The current paradigm for research and development in electrosurgical devices and therapeutic systems has been discussed in [3], [6]–[8], which can help to identify areas where some contribution can be made:

1. Reduction in patient trauma, blood loss and recovery time through minimally invasive and non-invasive surgical solutions. This is becoming a popular practice in the UK and rest of the world where majority of the patients are aimed to be discharged on the same day as their surgical procedure.
2. Enabling focused microwave power delivery and tissue dissection with small depth-of-effect and minimal collateral damage to the healthy tissues at an affordable cost.
3. Need for smart integrated devices and energy sources that can delivery efficient tissue-cutting and coagulation or ablation performance.
4. Need to perform key-hole, laparoscopic or endoscopic surgery with minimal risk to the patient.
5. Removing lesion en-bloc without causing damage to the specimen to give histologists the best chance to identify cancerous cells. Current biopsy procedures and tests can take up to 42 days [9], however, on-chip cancerous cell characterisation and treatment systems are under development which can significantly reduce diagnostic and treatment time.
6. Allow for a physically less strenuous procedure for the medical practitioner.

The motivation for research presented in this thesis is utilisation of non-ionising RF and microwave energy for the diagnosis and treatment of human subjects for various medical

conditions like tumours, cancer, ablation/coagulation, atrial fibrillation, wound-sterilisation, enhanced liposuction, keratoconus, and endoscopic, laparoscopic and open surgeries [8], [10]. Development in RF and microwave devices over the past few decades have enabled to generate high enough levels of high frequency microwave power at an affordable cost, which can be used in electrosurgical devices and therapeutic systems that operate in the frequencies ranging from a few MHz to tens of GHz. Some practical implementations of these systems include [6], [11]:

1. Antenna and applicator structures that may be introduced in interstitial, local-external, or regional arrangements to deliver microwave energy into the tissue to perform key-hole, laparoscopic and endoscopic surgeries.
2. Integrated systems to deliver low frequency RF energy for tissue cutting and high frequency microwave energy for tissue coagulation and ablation.
3. Specialised microwave cannula to reduce blood loss during enhanced liposuction procedure via blood vessel coagulation.
4. Loaded waveguide for the treatment of menorrhagia to minimise excessive uterine bleeding.
5. Small wideband microstrip based antennas having tapered tip for ease of insertion into the body for in-body ablation of liver, kidney, breast and bone tumours.

Michaelson (1987) in [12] and Thuéry (1992) in [13] have presented comprehensive review of the biological effects and interaction of microwaves with the human body.

1.3 Research Problem

Currently, microwave power generators producing tens of Watts of microwave power feed energy to the treatment site via a lossy coaxial cable, which is thin enough to travel down the instrument channel of an endoscope that may be 2.8 mm or 3.2 mm in diameter [14]. Important issues with the system are energy loss during transmission of microwave power to the intended tissue site, and the resultant distributed tissue heating. However, these issues can be overcome by the development of high efficiency microwave power sources that can travel close to the treatment site via an endoscopic channel. Also, microwave power generators are commonly large and cumbersome which limit the development of portable electrosurgical devices; for instance, performing coagulation to stop excessive bleeding in emergency stricken areas. However, small and efficient microwave power sources followed by multistage amplifiers can be integrated within an antenna or applicator structure to generate tens of watts of microwave power for portable electrosurgical applications.

Recent advances in high efficiency class AB, class F, class F^{-1} and class J power amplifiers, class E switching mode oscillators and active transistors using GaAs and GaN technologies can be utilised to develop discrete and MMIC power sources and amplifiers for various medical applications in C-band, X-band Ku-band and Ka-band microwave frequencies. Some of the application areas that will be covered in this thesis include: 1) C-band portable haemostatic device for coagulation of traumatic bleeding sites in emergency situations where access to specialised medical facilities is limited, 2) K-band on-chip device for diagnosis and neutralisation of glioblastoma and medulloblastoma brain cancers, and 3) X-band microwave power source for integration within the tip of an endoscopic channel for the treatment of benign and cancerous lesions, male sterilisation and menorrhagia.

1.4 Thesis Organisation

This chapter presented background into electrosurgical devices and therapeutic systems, and their underlying limitations that aided in developing research problem for the scope of work presented in this thesis. Literature review and research work presented in this thesis has been organized into six chapters (2-7) which are summarised below; while Chapter 8 presents conclusions and recommendations for future work.

1.4.1 Chapter 2

Chapter 2 will present literature review of semiconductor heterostructures and corresponding transistor devices with targeted discussion on characteristics and performance analysis of GaAs and GaN semiconductor materials; and HEMTs formed by their respective GaAs/AlGaAs and GaN/AlGaN heterostructures. Material properties and physical characteristics help to identify performance and limitations posed by these devices towards the development of high efficiency discrete and MMIC power amplifiers.

1.4.2 Chapter 3

Chapter 3 will discuss review of various high efficiency power amplifiers that include class B, class AB, class J, class E, class F and class F^{-1} amplifiers and class E switching mode oscillator with discussion on non-linear effects, design considerations and large signal characterisation. Comparison in terms of performance and efficacy for various application areas specifically intended medical applications will also be discussed.

1.4.3 Chapter 4

Chapter 4 will present discussion on the development of high efficiency discrete power amplifiers that include class AB, class F, and multistage class AB and class F amplifiers.

Various design aspects including characterisation of commercially available GaN HEMT CGH55015 and CGH55030, load-pull analysis, EM simulations and layout have been discussed. Large signal results and analysis have also been presented which discuss the relationship between gain, output power and PAE as a function of the input power. The application area envisaged for these amplifiers is portable haemostasis device for blood coagulation in the battlefield and emergency stricken areas.

1.4.4 Chapter 5

Chapter 5 will discuss theoretical background and basic concepts related to electrosurgery while extending review on various effects that are observed due to the interaction of RF and microwave energy with the human body. Initial tests of high efficiency discrete power amplifiers developed in Chapter 4 will be presented to demonstrate their suitability for implementation within a portable haemostatic system operating at 5.8 GHz, to achieve sufficient power density to coagulate bleeding sites in emergency stricken areas where conventional treatment procedures are ineffective.

1.4.5 Chapter 6

Chapter 6 will discuss the development of high efficiency class AB MMIC amplifier processed using WIN PP10-15 GaAs process with support from Semtech Limited. The chapter will present overview of MMIC technology and PP10-15 GaAs process while extending the discussion to design, small and large signal simulations, layout processing and initial on-wafer $[S]$-parameter measurements. The amplifier operates at 30 GHz and has been envisaged for application within an on-chip diagnostic and neutralisation system for glioblastoma and medulloblastoma cancerous stem cell.

1.4.6 Chapter 7

Chapter 7 will present discussion on high efficiency class E MMIC oscillator developed using WINPP10-15 GaAs process with support from Semtech Limited. The oscillator MMIC measuring 2450×1330 μm has been targeted to provide over 20 dBm localised microwave power for endoscopic surgical procedures operating at X band microwave frequencies. Initial on-wafer measurements will also be presented.

Chapter 2

Semiconductor and Transistor Device Technology in Review

2.1 Introduction

Solid state vacuum tubes were the initial devices utilised for power amplification units in communication systems. With advancement in RF electronics, semiconductor devices were developed to replace vacuum tubes due to their promising performance in terms of electrical and material properties, high frequency operation and reduced device size. In their initial days, semiconductor devices had a dominance of group IV semiconductors like silicon and germanium. However, this trend was soon replaced by alloy semiconductors like GaAs, InP, SiC and GaN. The landscape paved way for the development and mass scale fabrication of transistor devices for high power and frequency operation, something that is far superior to vacuum tubes and pure Si based devices. Semiconductor compounds allowing complex multiple layer device fabrication were the breakthrough to enable superior device performance in terms of power and high frequency operation. DC and RF performance of semiconductor devices is critically dependent on electronic, thermal and mechanical properties of semiconductors and their heterostructures presented in Table 2. 1 which has been reproduced from [15].

Table 2. 1: Semiconductor material parameters [15]

Semiconductor (Typical Materials)		Silicon	Gallium Arsenide	Indium Phosphide	Silicon Carbide	Gallium Nitride
Characteristic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.25	3.49
Electron Mobility at 300 K	cm^2/Vs	1500	8500	5400	700	1000-2000
Saturated Electron Velocity	$x\ 10^7$ cm/s	1	1.3	1	2	2.5
Critical Breakdown Field	MV/cm	0.3	0.4	0.5	3	3.3
Thermal Conductivity	W/cm K	1.5	0.5	0.7	4.5	>1.5
Relative Dielectric Constant	ε_r	11.8	12.8	12.5	10	9

Critical material properties of semiconductors corresponding to Table 2. 1 include [16]:

Wide bandgap energy prevents the device from undergoing electronic breakdown by withstanding high enough internal electric fields.

Relative dielectric constant indicates capacitive loading of semiconductor devices, thus, affecting its terminal impedance. Lower values of relative dielectric constant are important to reduce capacitive loading of the device. This allows larger area of the device to be fabricated to permit high RF currents and RF power.

Thermal Conductivity is important for heat extraction from the device. Higher value of thermal conductivity ensures that the device loses heat efficiently. Diamond and SiC have higher values of thermal conductivity; thus, they can be used as excellent substrates for transistor devices made from semiconductors or heterostructures releasing higher heat energy like GaN.

Critical Breakdown Field defines the strength of electrical fields that could be supported within the device without breakdown. Higher values are desirable for achieving high power performance of the device. GaN shows critical breakdown field strength of 3.3×10^6 V/cm that is far superior than competing semiconductor device technologies like GaAs and InP, having values of 0.4×10^6 V/cm and 0.5×10^6 V/cm, respectively [15]. High electric field strength mean higher operating drain voltage could be supported to generate higher RF power.

The relationship between electron velocity and electric field intensity is important to achieve high frequency and high current operation of the device. The DC and RF currents that pass through the semiconductor device mainly depend upon electron velocity and electric field intensity. Higher values of charge carrier mobility and saturation velocity are desired. Comparison between electron velocity and electric field intensity for various materials has been shown in Fig. 2. 1, which has been reproduced from [16].

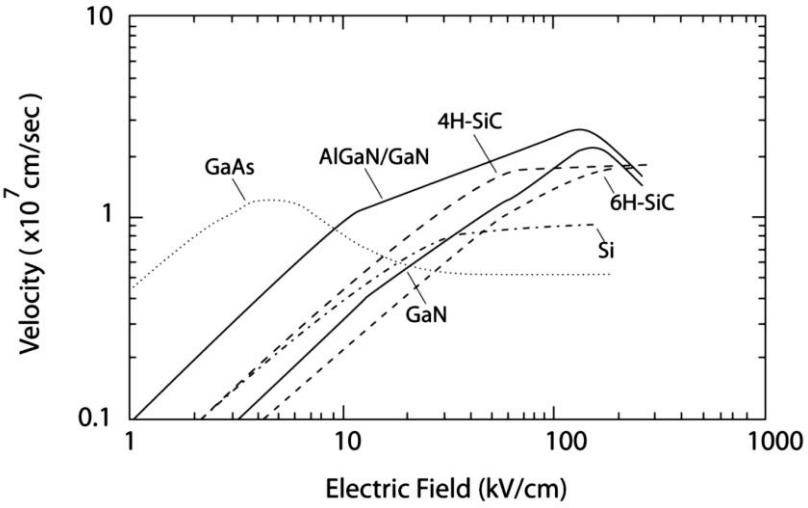


Fig. 2. 1: Comparison between electron velocity and electric field intensity for semiconductor materials and heterostructures [16]

High power and frequency operation of wide bandgap semiconductor devices require them to have the capability to support high currents and electric fields (or voltage). The performance is often restricted by lower bias voltage, smaller value of electron mobility (velocity) and current, and thermal conductivity of the device. Comparing the curves and material properties shown in Fig. 2. 1 and Table 2. 1, it can be inferred that due to higher electron mobility, GaAs transistor devices depict low noise and high frequency performance compared to other semiconductor devices. However, they cannot provide very high-power performance because of their lower bandgap energy and critical breakdown field intensity. GaN devices on the other hand depict high-power performance due to their capability to support higher electric fields; however, their noise performance is poor compared to GaAs devices. Semiconductor devices that operate at higher frequencies have been report by Schwierz (2003) in [17], and include:

GaAs RF Devices

GaAs MESFETs are low cost devices that can operate with low noise and high power up to 20 GHz. GaAs HBTs provide high linearity and high output power density and are a popular choice for cellular communications. GaAs HEMTs can provide low noise and reasonable power performance at higher frequencies and can be realised as MMICs.

InP RF Devices

InP based HEMTs are very high frequency devices and have least noise figure of all competitive devices, while InP based HBTs have the highest operating frequencies amongst competitive HBT semiconductor technologies. Being an expensive semiconductor technology, InP devices remain limited to high performance applications.

GaN RF Devices

These devices are relatively new and have the highest output power performance allowing high operating temperature and breakdown voltage. GaN and AlGaN/GaN RF devices find their applications for high power and high frequency applications.

This chapter on literature review of semiconductor heterostructures and their respective transistor devices has been divided into two sections. Section 2.2 presents review, characteristics and underlying performance of heterostructures formed by GaAs and GaN compound/alloy semiconductor materials. While Section 2.3 presents discussion on the characteristics and performance of high electron mobility (HEMT) transistor devices formed by well known GaAs/AlGaAs and GaN/AlGaN heterostructures.

2.2 Heterostructures

2.2.1 Introduction

Heterostructure is a structure grown by having at-least two or more layers of different semiconductor materials with distinct bandgap energies. This leads to the formation of an interface between two semiconductor layers called the heterojunction. Heterostructures have greatly improved the capabilities of semiconductor devices in high frequency and high-power operation and has led to the development of some high performing devices. HEMTs are heterostructure based vertical FET devices that are fabricated with several layers of compound semiconductor materials to improve carrier mobility, which can be further enhanced by including additional transition layers having distinct bandgap energies between semiconductor materials [17], [18]. Basic outline of the most common heterostructure formed with GaAs and AlGaAs has been shown in Fig. 2. 2. A similar heterostructure is also formed with GaN and AlGaN which will be presented later in this chapter with discussion on some specific performance characteristics.

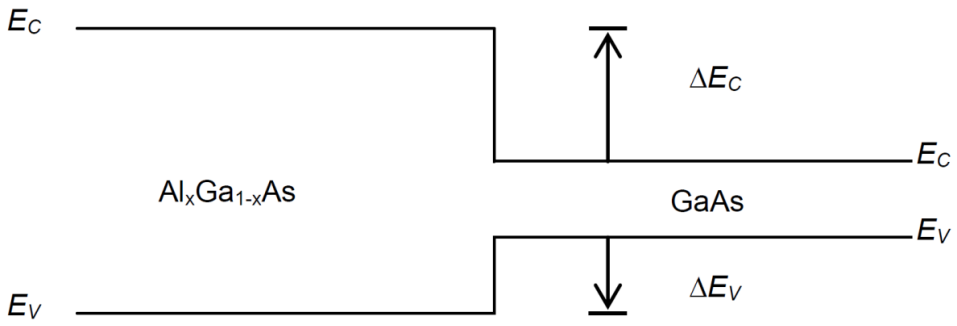


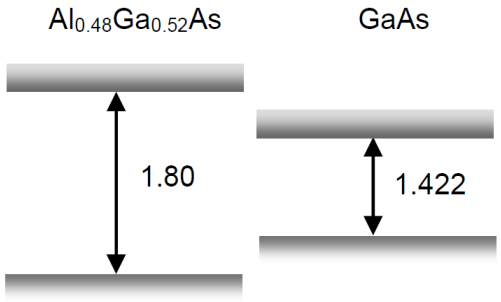
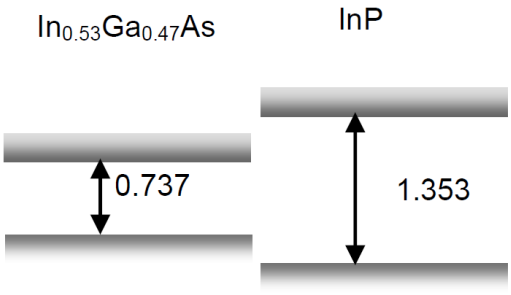
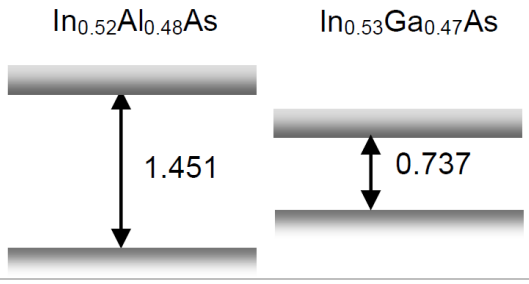
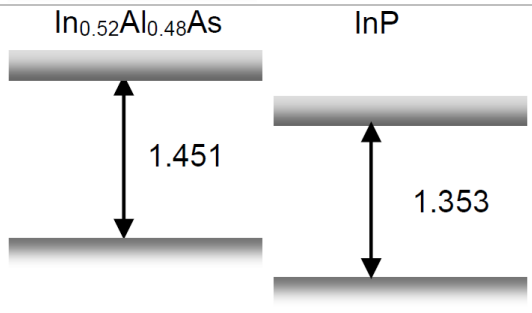
Fig. 2. 2: Heterostructure of GaAs and AlGaAs with energy levels of conduction and valence bands

Energy levels of conduction and valence band for the respective semiconductor materials have been represented as E_C and E_V, respectively in Fig. 2. 2. There are two distinct energy gaps between materials forming the heterostructure; thus, the conduction and valence bands of the two materials are discontinuous across the heterojunction. The difference in energy levels between the two conduction and valence bands of the semiconductor materials are called conduction and valence band offsets and are represented as ΔE_C and ΔE_V, respectively. Energy gap difference is defined as the sum of conduction band and valence band offsets and given by Eq. 2.1 [19].

$$\Delta E_G = \Delta E_C + \Delta E_V \tag{2.1}$$

Bandgap difference and bandgap offset are important to define the performance of heterojunction devices like HEMTs and HBTs. Table 2. 2 enlists some common heterostructures, their bandgap difference and band offsets [17], [19].

Table 2. 2: Band diagrams for various heterostructures [19]

Heterostructure	Band Diagram	ΔE_C	ΔE_V
AlGaAs/GaAs		0.219	0.159
InGaAs/InP		0.271	1.353
InAlAs/InGaAs		0.52	0.737
InAlAs/InP		0.253	0.155

In the heterojunction formed between GaAs and AlGaAs, energy bandgap of GaAs at 300K is 1.42 eV as indicated through Table 2. 1, while the bandgap in AlGaAs depends on the concentration of Al within the semiconductor compound. Thus, the energy gap may be given as Eq. 2.2 [19].

$$E_G = 1.424 + 1.247x \qquad 0 < x < 0.45 \tag{2.2}$$

Another important characteristic of this heterostructure discussed by Brennan (2002) in [19] is the close lattice matching between GaAs and AlGaAs, where the two semiconductor materials have similar lattice constants. In heterostructures that are not lattice matched, the mismatch should be accommodated through strain or by forming misfit dislocations. Another factor that affects the heterojunction is the doping type and the concentration of semiconductor materials within the heterojunction. Heterojunctions can be either formed by growing two intrinsic semiconductor materials or by using semiconductor materials, either or both of which may be doped (n-type or p-type) [19]. Thus, various junctions may be formed in the heterojunction.

2.2.2 Charge Carrier Enhancement- Modulation Doping

Modulation doping is an alternative technique to the conventional charge carrier enhancement techniques in which the number of free charge carriers and conductivity in a semiconductor material layer is significantly increased without the introduction of an impurity. The process of modulation doping overcomes some undesirable effects observed in semiconductor devices like increased ionized impurity scattering and the inherent reduction in carrier mobility due to impurities. This happens because of the spatial separation between dopants and free charge carriers [19]. Thus, modulation doping increases the number of free charge concentration without compromising the charge mobility. Consider a modulation doped semiconductor heterostructure (shown in Fig. 2. 3) formed between two materials, i.e. 1) a wide bandgap material like AlGaAs that is doped n-type, and 2) a relatively narrow bandgap material like GaAs, that has been unintentionally doped. Brennan (2002) in [19] discusses that the most common materials to demonstrate modulation doping are GaAs and AlGaAs. When in equilibrium, Fermi level of the charges must align across the heterostructure. Fig. 2. 4 shows Fermi levels of the heterostructure when the two semiconductor materials are apart from each other.

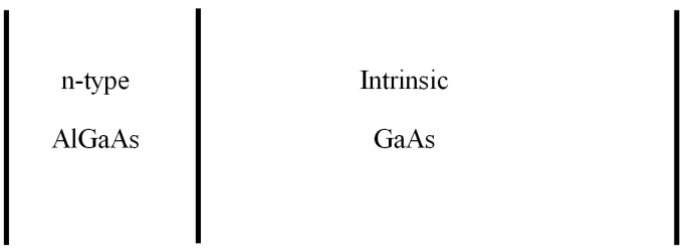


Fig. 2. 3: Layer structure for GaAs and AlGaAs modulation doped heterostructure

It can be inferred that the Fermi level of AlGaAs (n-type doped) is much closer to conduction band level compared to the Fermi level of GaAs with its respective conduction band. However, when the two semiconductor materials come in contact, the Fermi levels

of both the semiconductor materials should balance and align with each other. Thus, electrons will transfer from AlGaAs (having larger concentration of charge carriers) to GaAs [19]. This transfer of electrons from AlGaAs to GaAs will significantly increase electron concentration in GaAs without introducing any ionized donor impurity. The transfer of electrons between the two layers and the resulting energy levels has been shown in Fig. 2. 5 which has been reproduced from [19].

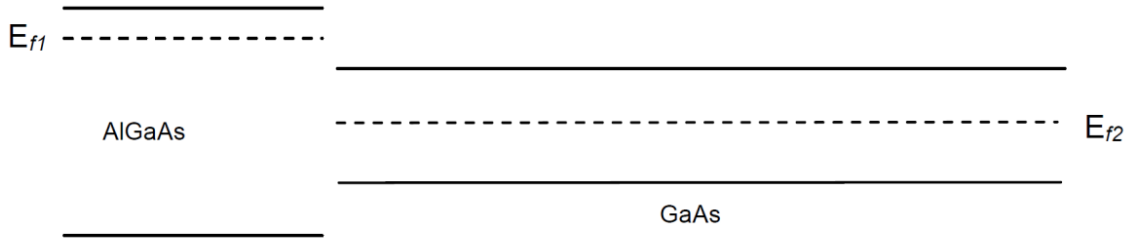


Fig. 2. 4: Energy band diagram of AlGaAs and GaAs heterostructure and Fermi level when the semiconductor materials are apart in equilibrium

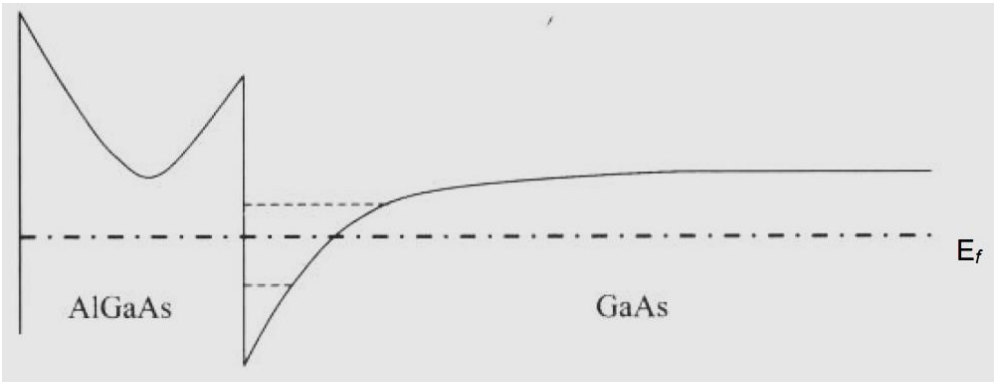


Fig. 2. 5: Aligned Fermi levels of AlGaAs and GaAs [19]

In Fig. 2. 5 [19], the two horizontal dashed lines at the heterojunction within the GaAs layer indicate energy sub-bands due to spatial quantization effects. Sizeable increase in electron concentration in GaAs leaves a net positive charge in AlGaAs to balance the net negative charge due to electron transfer in GaAs semiconductor layer. Ionized donor atoms in AlGaAs influence electron transfer in the GaAs layer, Coulomb's interaction between the charges is mitigated because of spatial separation between the two semiconductor layers. Thus, ionized impurity scattering of the transferred electrons is reduced and electron mobility is increased [19]. When the spatial separation of electrons (or electron gas) and their ionized donors is large, the ionized scattering rate is weak. To further reduce ionized impurity scattering, spatial separation between electrons from their ionized donor is increased by having a spacer layer of an un-doped AlGaAs between the doped AlGaAs and intrinsic GaAs layer, which further improves electron mobility.

2.2.3 Two-Dimensional Electron Gas in GaAs Heterostructures

Fig. 2. 6 presents an expanded view of the discontinuity due to bending in the conduction band of intrinsic GaAs at the heterojunction. Steep slope in the conduction band of GaAs occurs because of electron transfer from n-AlGaAs layer to the i-GaAs layer. Brennan (1999 and 2002) in [19], [20] discusses that electron transfer from n-AlGaAs semiconductor layer leaves a net positive charge on the n-AlGaAs layer (ionized donors) and creates a net negative charge on the i-GaAs layer. Gaussian surface that encloses total charge within the system (having a net zero charge) can be considered to draw the conduction band diagram. As an electron start its journey from n-AlGaAs towards i-GaAs, it sees a negative charge on the other side of the heterojunction that raises its energy near the heterojunction. This can be observed with the upward bend in conduction band at the heterojunction.

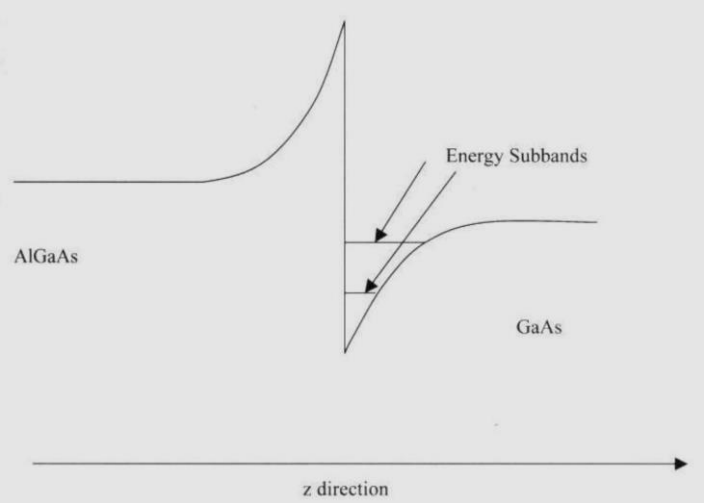


Fig. 2. 6: Representation of the conduction band discontinuity at the n-AlGaAs and i-GaAs heterojunction showing an upward bend in the conduction band at the heterojunction [19]

Net charge towards left of the heterojunction (n-AlGaAs) is positive, thus, a negative test charge (electron) in the i-GaAs semiconductor layer will be attracted towards the heterojunction. Energy of an electron will be lower closer to the heterojunction, which causes the conduction band in GaAs layer to bend or have a “downhill roll”. This leads to a discontinuity and the creation of a potential difference in the i-GaAs layer [17], [20]. Electrons within this region are confined by a well of potential difference, called the ‘potential well’ discussed in [19], [20]. The dimensions of this potential well are typically very small ≈ 10 nm or less [20]. As a result of this potential well and conduction band bending, spatial quantization effects occur at the location of potential well producing discrete energy bands called the sub-bands [19]. Quantization effects or quantized energy

is observed perpendicular to the heterojunction (along z-direction shown in Fig. 2. 6). However, these effects are non-existent in the x-y plane due to no restriction on electron movement by the band bending. Thus, they constitute an unrestricted movement in the two-dimensional x-y plane (parallel to the heterojunction) called the Two-Dimensional Electron Gas (or 2DEG) [19].

Another case of GaAs heterostructures, which is one of the most widely used heterostructure for HEMT transistors, includes a slightly doped p-GaAs semiconductor layer and a heavily doped n-AlGaAs. This heterostructure comprises of barrier and channel layers. Barrier layer exists in heavily doped n-AlGaAs having a higher conduction band while the channel layer exists in lightly doped p-GaAs having a lower conduction band. Difference between n-AlGaAs/p-GaAs and n-AlGaAs/i-GaAs heterostructures is that the diffusion of both holes and electrons take place in the former with Two-Dimensional Hole Gas (2DHG) at n-AlGaAs/p-GaAs heterojunction. However, Trew (2005) and Brennan (2002) in [16], [20] both agree that 2DHG are less practical compared to 2DEG. shows band diagram of the n-AlGaAs/p-GaAs heterostructure.

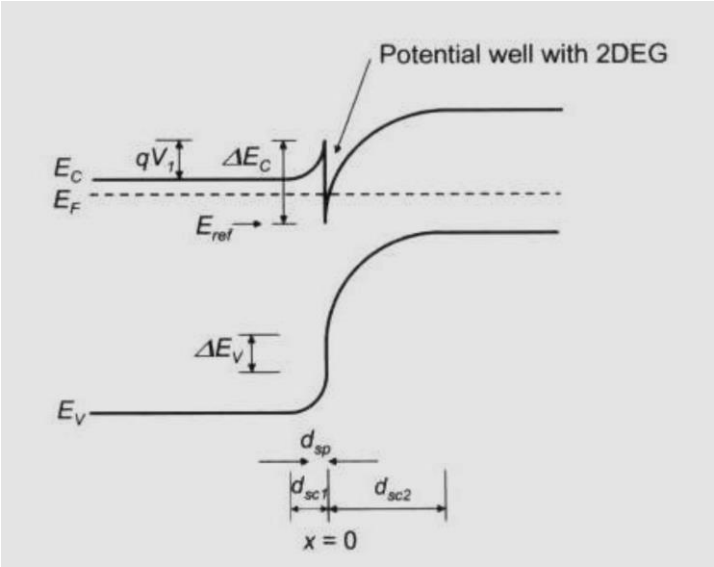


Fig. 2. 7: Band diagram for n-AlGaAs/p-GaAs heterostructure [19]

Fig. 2. 7 shows space charge region where an electric field exists due to donor ions on n-AlGaAs side and accumulated electrons on p-GaAs side. It also slightly depends upon acceptor ions on the p-GaAs; however, the effect is insignificant. Trew (2005) in [16] suggests that an i-AlGaAs spacer layer with a very small thickness of a few nanometres may be introduced in this type of heterostructure to improve electron mobility by separating the barrier and channel layers.

2.2.4 GaN Heterostructures

GaN heterostructures present the possibility of achieving very high concentration of 2DEG compared to their competitor GaAs heterostructures without any layer doping. This is achieved by epitaxial growth of AlGaN layer on top of GaN buffer layer; thus, removing issues with intentional doping of GaN or its' alloy layers. Jarndal (2006) in [21] discusses that there are two types of polarization effects in AlGaN/GaN compound structure: spontaneous and piezoelectric polarizations. Spontaneous polarization occurs because of built-in polarization field in the unstrained crystal lattice. While, piezoelectric polarization occurs because of distortions in the crystal lattice. High concentration of 2DEG in heterostructures is achieved primarily because of high polarization contribution of every layer within the heterostructure. Polar layer with a different crystal lattice once grown on top of the buffer layer introduces piezoelectric polarization along with a polarization vector, this effect generates a high sheet charge that largely depends on lattice mismatch between the two layers [21]. Fig. 2. 8 illustrates sheet charge resulting due to strain at the two faces of AlGaN layer in the AlGaN/GaN heterostructure.

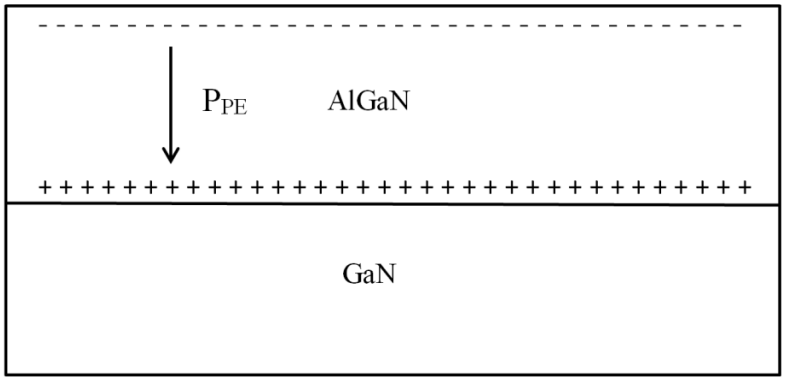


Fig. 2. 8: Charge sheet and electric field due to piezoelectric polarisation in AlGaN layer

Charge sheet due to piezoelectric polarization has been shown in Fig. 2. 8. Electrons tend to recompense the effect of positive charge as a result of which an additional 2DEG component is generated adjacent to the heterojunction in the GaN layer. Jarndal (2006) and Brennan (2002) in [21] and [19], respectively suggest that the sheet density of this additional 2DEG component may be considerably large and needs to be accounted for in overall 2DEG in the AlGaN/GaN heterojunction. Fig. 2. 9 shows combined effect of spontaneous and piezoelectric polarization effects in the AlGaN/GaN heterostructure.

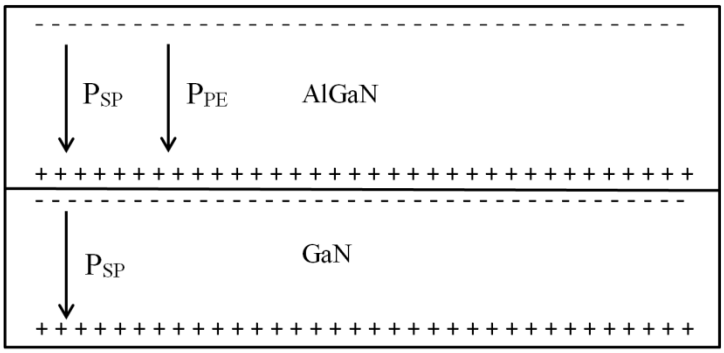


Fig. 2. 9: Combined spontaneous and piezoelectric polarization effects in AlGaN/GaN heterostructure

Brennan (2002) in [19] discusses the difference between conduction band diagrams of the AlGaN/GaN heterostructure once polarization effects are considered, the illustration has been reproduced from [19] in Fig. 2. 10.

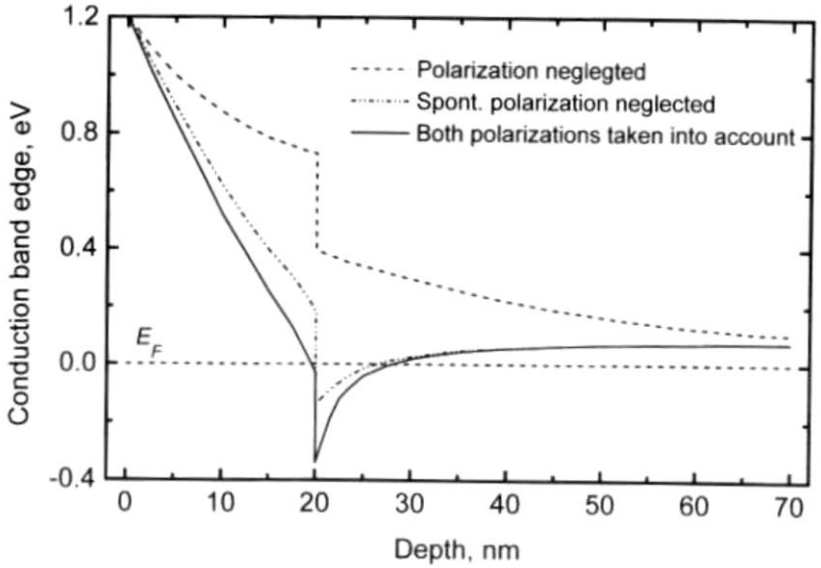


Fig. 2. 10: Conduction band diagram of AlGaN/GaN heterostructure with polarization effects [19]

At the heterojunction shown in Fig. 2. 10, conduction band is 0.3 eV below the Fermi level while considering polarization effects. This gives rise to a high 2DEG electron sheet density. However, the 2DEG wouldn't exist once polarization effects are not considered because conduction band is 0.4 eV above the Fermi level in that case. Thus, Jarndal (2006), Brennan (2002) and Schwierz (2003) in [19], [21], [22] suggest that significant 2DEG electron sheet density can exist in AlGaN/GaN heterostructures even without doping the AlGaN layer.

2.2.5 Surface Charge States in GaN Heterostructures

Trew (2002) in [23] suggests that crystal energy in semiconductor materials increase with an increase in layer thickness. Thus, crystal energy of AlGaN increases with an increase in thickness during the growth process. After certain thickness of the layer has been achieved, internal electric field intensity becomes significant to ionize the donor layer. This results in electrons being shifted towards the AlGaN/GaN heterojunction with a subsequent decrease in the electric field. A 2DEG will be generated at the heterojunction under equilibrium condition. It has been discussed in [22], [23] that critical breakdown field formed in GaN/AlGaN heterostructures are significant, i.e. $E_C > 10^6$ V/m compared to GaAs and Si that are around $E_C > 10^5$ V/m. Besides this, AlGaN/GaN heterostructures have high values of 2DEG electron charge density around 10^{13}cm^{-2}. These high breakdown fields and 2DEG electron charge density enable GaN devices to operate with larger electric fields at higher operating bias voltage and high DC and RF currents to produce high output power. It has been discussed that spontaneous and piezoelectric polarization effects cause charge sheets of opposite polarity to be created at the top and bottom faces of the AlGaN layer in the heterostructure. However, this effect cannot alone describe generation of 2DEG within the heterojunction. Thus, a positive charge sheet as shown in Fig. 2. 11 at the AlGaN surface causes the 2DEG to exist within the GaN channel. Ibbetson in [24] suggests that the origin of this positive charge sheet is the ionized donor states at the surface.

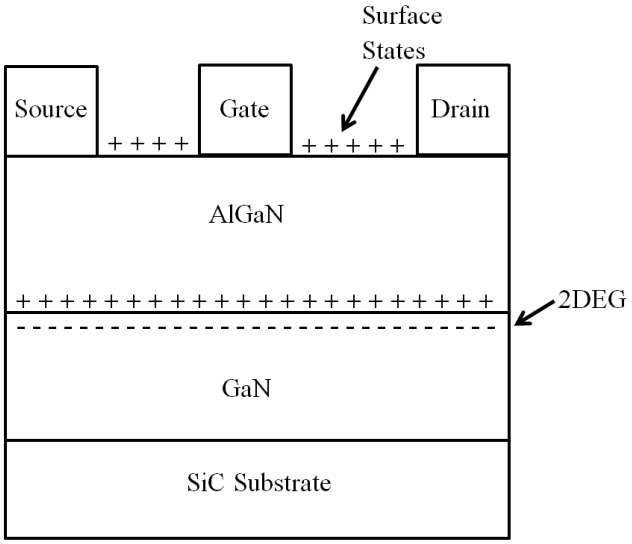


Fig. 2. 11: AlGaN/GaN heterostructure having polarization induced charges and 2DEG

'Surface charge states' is also considered an origin of positive charges at the top of AlGaN layer that compensate for the negative charges induced by polarization at the bottom edge

[24]. With an increase in the thickness of AlGaN layer; Fermi level existing at the surface reduces, approaching the donor level. Once Fermi level equals the surface state, the surface charges starts to empty. Thus, a 2DEG is formed at the heterojunction of AlGaN/GaN and the field in barrier layer (AlGaN) is reduced. With a further increase in the AlGaN thickness, the 2DEG will achieve saturation, thus, approaching the amount of induced charges due to polarization [23], [24]. Hence, energy of surface states increases with an increase in the thickness of AlGaN layer. Electrons will transfer from space states to the empty conduction band state at the heterojunction when energy of surface states equals the Fermi level, for a particular thickness of AlGaN layer. This transfer of electrons creates a 2DEG leaving behind positively charged surface sheet charges.

2.2.6 Wide Bandgap III-V Heterostructures for RF Power Devices

Bandgap energies of semiconductor materials and alloys play an important role in determining their suitability for power devices. In the earlier days, vacuum tube transistors were major devices for current to power conversion, but they were soon replaced by Silicon based solid state transistors. Silicon based devices presented some fundamental limitations that include blocking voltage capability, operating temperature and switching frequency. These limitations and physical restraints reduced efficiency of their power convertors [25]. However, group III-V alloys showed promising material and electrical properties against the limitations in Si devices. This efficacy paved way for the implementation of group III-V semiconductors within RF electronics and being widely accepted by the industry. One of the important material properties that group III-V semiconductors provide is high bandgap energy to enable high efficiency power devices. The promising candidate semiconductor materials with considerably higher bandgap energies than Si are: Silicon Carbide (SiC) and Gallium Nitride (GaN). Table 2. 1 presents fundamental material properties of semiconductor materials. Thermal conductivity is an important material property as discussed earlier. SiC, Diamond (C) (~6 W/cm K) and GaN show better thermal conductivity values than Si. Diamond is still not a mature technology and its efficacy under consideration compared to SiC and GaN, thus, GaN and SiC show promising performance from amongst group III-V semiconductor materials. Amongst SiC and GaN, the former has larger thermal conductivity, but on the other hand, GaN provides better bandgap energy, critical breakdown field and the theoretical maximum junction temperature. Thus, GaN is a better choice from group III-V semiconductor material for advanced power devices [25], [26].

Significant developments have been made in process technology and bulk substrate material for SiC for high power applications. Owing to its larger dielectric critical field for the same drift layer thickness, SiC based power rectifiers have shown over 10 times better blocking voltage capabilities compared to Si based devices [25]. Besides this, SiC devices can operate at much higher current densities compared to Si devices without complex cooling systems due to the high thermal conductivity values. These devices are well suited for aerospace and space mission applications. SiC based power switches have also shown remarkable performance due to their conductivity modulation [25].

2.3 High Electron Mobility Transistors

2.3.1 Field Effect Transistor

Field effect transistors are three terminal semiconductor devices used for amplification and switching of electronic signals. Voltage or current variation at one of the device terminals is utilised to control current at the other two terminals, thus, providing amplification of the input signal. Field effect transistors are single charge carrier devices that operate with the majority charge carriers which may be electrons or holes. Fig. 2. 12 shows the basic model of a FET, which was first described by Leistiko (1964) in [27].

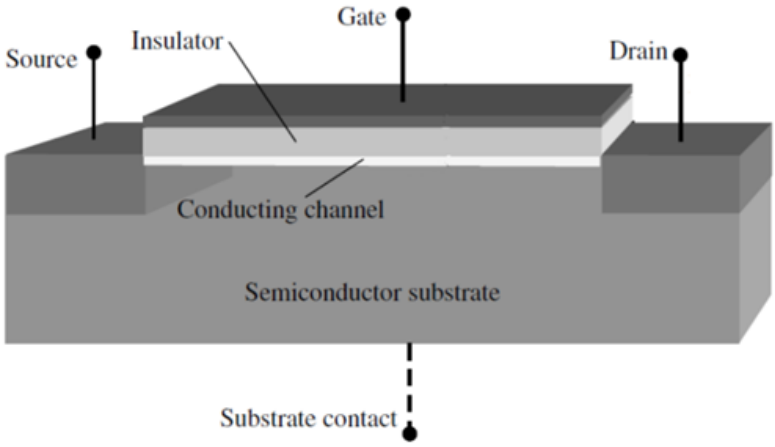


Fig. 2. 12: Basic cross-sectional model of a field effect transistor [27]

As indicated by the basic model of an FET shown in Fig. 2. 12, a conduction channel is formed between Source and Drain terminal of the FET. Material properties discussed in preceding sections of this chapter play an important role in defining conductivity of the channel, electrical fields, critical breakdown field, electron or hole mobility, operating temperature and the frequency. Width of the channel is controlled by voltage applied at the gate terminal (V_G). The channel may be made fully open ($V_G = 0$ V) or fully closed ($V_G =$ large negative value or pinch off), these are also called ON and OFF states of the

transistor. Compared to BJTs that operate with dual carrier charges, FETs provide high gain and low noise performance at high microwave and millimetre wave frequencies.

The three states (On, Off and Intermediate) of the transistor operation with varying gate voltage have been shown in Fig. 2. 13, where an FET wafer has been developed with heavily doped GaAs and lightly doped GaAs layers grown on an intrinsic GaAs substrate. The architecture shown here may not be utilised to express RF behaviour due to the oxide layer. Ohmic contacts (gold) define the three device terminals, i.e. drain, source and gate. Conduction channel is established in lightly doped GaAs layer between drain and source terminals of the device when a forward bias positive voltage is applied at the drain terminal. This permits free electrons to travel across the channel that is generally formed in the n-type layer to permit good availability of free electrons for conduction of the current. Width of conduction channel is controlled by applying different voltages at the gate terminal. The channel may be fully open as shown in Fig. 2. 13(a), when voltage at the gate terminal, $V_G = 0$ V (ON or saturation state). All free electrons in the n-type semiconductor layer travel through the channel from drain to source. This state is called saturation state of the transistor when all free electrons are conducting through the channel. The channel may be slightly closed and conduction reduced when a slight negative voltage (relative to drain voltage) is applied at the gate terminal, i.e. $V_G = -0.5$ V as shown in Fig. 2. 13(b). This reduction in channel width occurs because slight negative voltage applied at the gate terminal repels electrons that are travelling through the channel, thus, creating a depletion region. Within the depletion region, free electrons to conduct drain current do not exist. A large depletion region is created (and the channel closes), with an increase in high negative voltage applied at the gate.

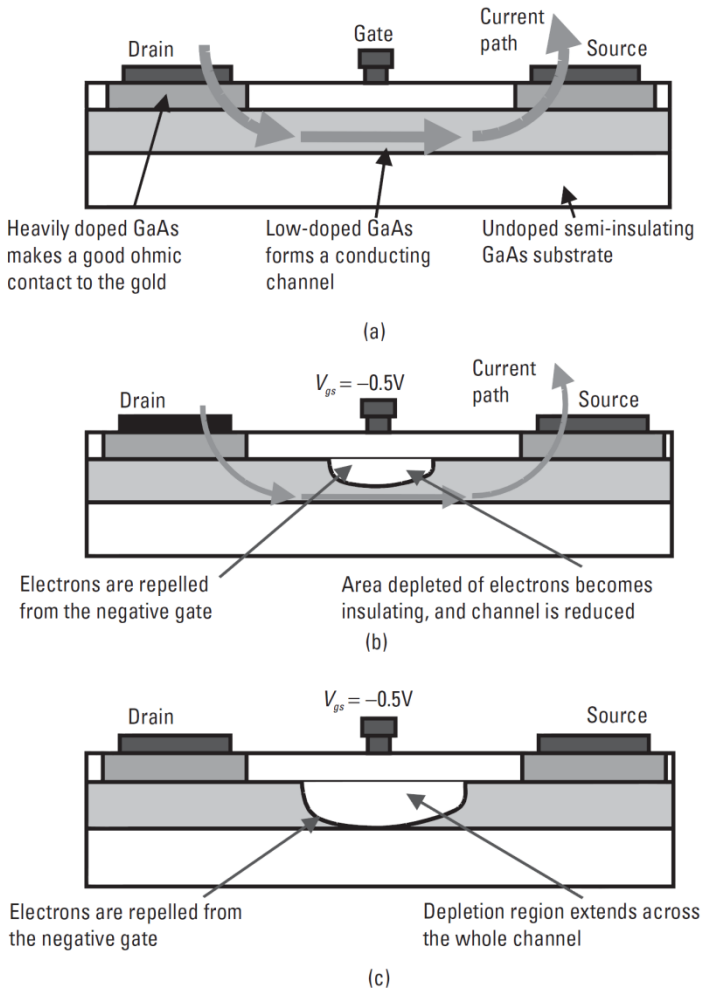


Fig. 2. 13: Cross sectional view of a general field effect transistor showing variation in channel width due to the applied gate voltage [28]

The channel may be completely closed (OFF or pinched off state) when a large negative voltage, i.e. $V_G = -1$ V is applied at the gate terminal; this has been shown in Fig. 2. 13(c). The application of large negative voltage at the gate repels electrons further away in the channel until the channel has been completely closed and there are no free electrons to carry the channel current. Current-voltage (IV) characteristics of a transistor can be defined according to the behaviour depicted by drain current to changes in the drain or gate voltages explained above. Fig. 2. 14 shows IV characteristics of the transistor shown in Fig. 2. 13, both these figures have been reproduced from [28].

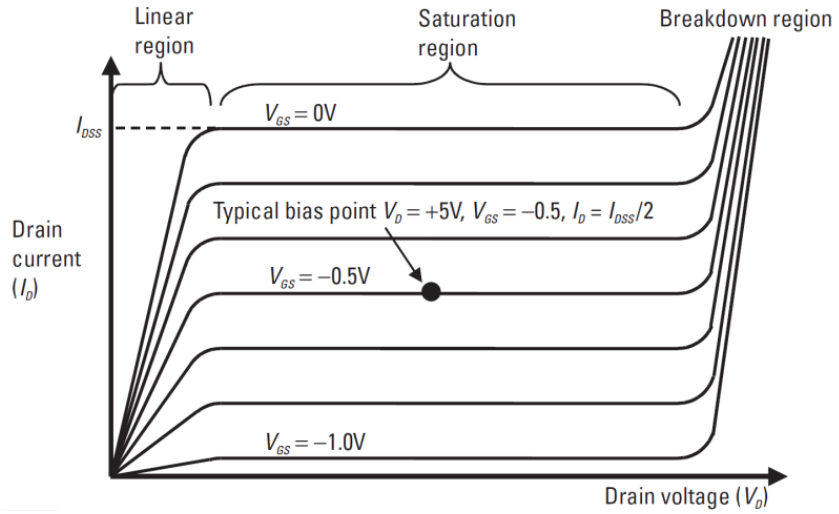


Fig. 2. 14: Current versus voltage curves for an FET with varying drain and gate voltages [28]

Drain current passing through the channel rises linearly with drain voltage; this starts from the knee region and extends until the boundary of saturation region where all free electrons are conducting. When a slight positive voltage is applied at the drain terminal, free electrons in the n-type lightly doped semiconductor layer form a channel and start conducting from drain to the source. The number of free electrons participating in conduction is proportional to the applied drain voltage, and this continues until all free electrons in the channel are conducting. At this stage, any further increase in drain voltage will not bring about any increase in the drain current. The transistor is said to have reached saturation.

At further higher drain voltages, semiconductor material and the transistor may breakdown with the drain current increasing rapidly. Breakdown of a transistor also depends upon material properties of the semiconductor that include critical breakdown field or the maximum electric field intensity that can exist within the transistor. Thus, transistors made from semiconductor materials having higher values of critical breakdown field like GaN have the capability to operate at higher drain voltages. Besides this, the channel should also be prevented from overheating by ensuring efficient heat dissipation. Devices with good thermal conductivity of the semiconductor material ensure proper dissipation of heat from the transistor. Gate voltage applied to an FET defines the number of free electrons available in the channel to conduct current from drain to the source terminal. However, conduction of available free electrons is determined by the applied drain voltage. With an increase in the drain voltage, larger number of free electrons will participate in conduction and this would increase until all free electrons are conducting.

2.3.2 HEMT Structure and Characteristics

High electron mobility transistors (HEMTs) are the type of FETs that have a vertical structure and utilise high electron mobility within the heterojunction of heterostructure semiconductors for conduction of channel current. Their operation is quite similar to that of FETs except that the channel is developed in the heterojunction instead of the n-type lightly doped semiconductor layer in FETs. 2DEG in the heterojunction conducts free electrons and causes drain current to flow. Various design engineering methods, may be used to reduce quantization effects, increase electron mobility in the channel and improve channel noise. HEMTs are also sometimes called Modulation Doped Field Effect Transistors (MODFETs). Fig. 2. 15 (reproduced from [29]) shows cross sectional structure of a typical AlGaAs/GaAs HEMT device, which will be used to understand the structure and characteristics of HEMTs. GaN HEMT devices and their underlying issues will be discussed later in this section.

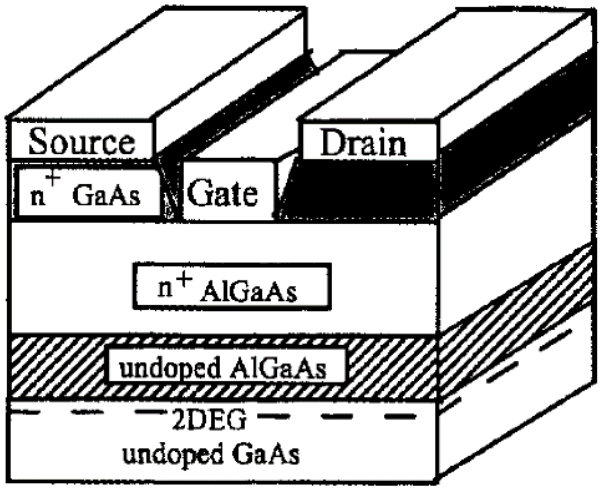


Fig. 2. 15: Cross sectional view of AlGaAs/GaAs high electron mobility transistor [29]

Robertson (2001) in [29] has discussed the structure and characteristics of HEMT devices that was invented by Horst Störmer at Bell Labs. Low resistance ohmic contacts to the device are formed by using doped GaAs caps and the gate is placed in a recess trench between source and drain terminals, to allow improved vertical scaling of the device and reduced access resistance to the gate. n-AlGaAs layer provides electrons to form current channel between source and drain terminals. Electron mobility through the channel is facilitated by the spacer layer of undoped AlGaAs that also spatially separates free electrons from their donor ions. Concentration of aluminium in doped and undoped AlGaAs controls the concentration of electrons accumulation layer in the channel and can be varied according to the intended application. Random alloy scattering tends to decrease channel mobility with an increase in aluminium concentration. Thus, best trade-off

between aluminium concentration and electron mobility is best achieved with 30% aluminium. However, high mobility can still be achieved because AlGaAs has higher bandgap energy than GaAs and so the electrons in the n-AlGaAs layer naturally accumulate at the heterojunction [29].

Channel current between source and drain terminals, passing through the 2DEG, can be calculated by electrons' sheet concentration below the gate terminal. In this case, the gate terminal may be considered to act as a capacitor with the two plates being 2DEG and gate metal contact. Dielectric of this capacitor should be depleted n-AlGaAs and i-AlGaAs spacer layers. Changing gate bias conditions do not necessarily affect the gate capacitance because separation is fixed by the thickness of two dielectric layers. Current modulation takes place when charge is removed or added to the 2DEG as a result of variations in applied gate voltage. This follows the basic capacitance relationship $Q = CV$ where, Q is the total charge within the 2DEG, C is the gate capacitance and V is the gate voltage [29]. Fig. 2. 16 shows conduction band diagram of the corresponding AlGaAs/GaAs HEMT, which has been reproduced from [29].

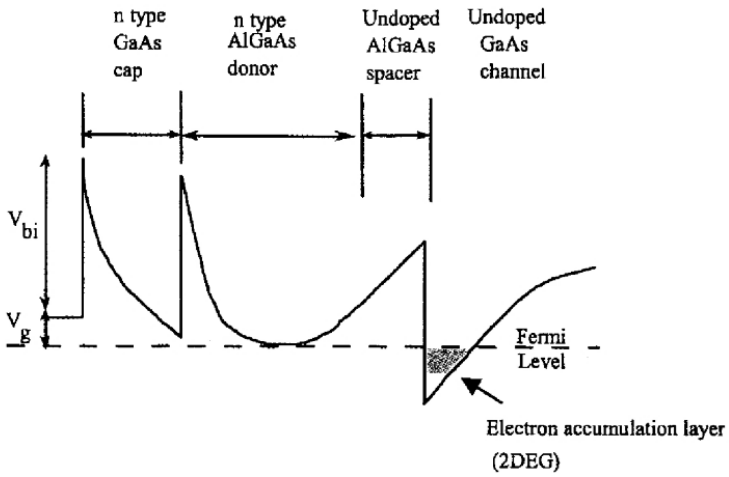


Fig. 2. 16: Conduction band diagram of AlGaAs/GaAs HEMT [29]

Threshold voltage of the device is defined when the channel is pinched-off, i.e. channel current between source to drain is completely stopped, by reverse biasing the gate terminal. However, when the HEMT is sufficiently forward biased, current across the channel flows from drain to source through two paths, i.e. the 2DEG, and the un-depleted part of the n-AlGaAs through the parallel conduction layer. Robertson (2001) in [29] discusses that this is not a feasible operation as the performance of the HEMT device is degraded due to carrier transport through the n-AlGaAs donor layer which has a lower electron mobility than GaAs.

2.3.3 DC Characteristics of HEMTs

DC *IV* characteristics of HEMTs are similar to the characteristics shown in Fig. 2. 14 in linear and saturation regions. However, due to higher electron mobility in HEMT devices, knee voltage for device saturation region occurs at a lower value compared to FETs. Besides this, extrinsic transconductance is improved and device access resistance is reduced. Drain current of HEMTs follows the relationship given in Eq. 2.3 within the linear region [29].

$$I_D = qn_{2D}\mu W\frac{V_D}{s} \tag{2.3}$$

Where, n_{2D} represents two dimensional electron sheet concentration under the gate, μ represents 2DEG mobility, W defines device gate width, s defines separation between source and drain contacts, and V_D is the applied drain voltage [29]. Robertson (2001) has discussed *IV* characteristics for HEMT devices in [29] which have been reproduced in Fig. 2. 17.

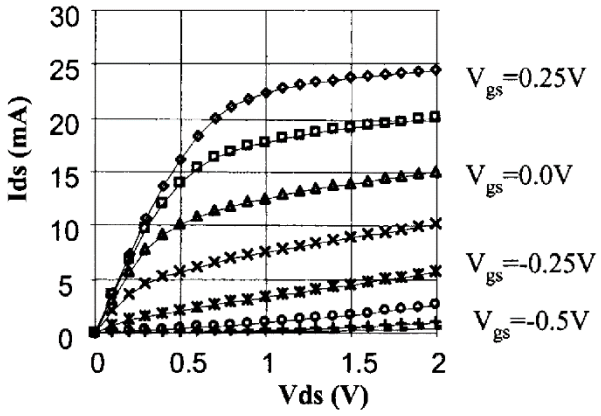


Fig. 2. 17: I/V Characteristics of a HEMT Device

Drain current in saturation region can be written as Eq. 2.4, where, v_{eff} is the effective channel velocity [29].

$$I_D = qn_{2D}v_{eff}W \tag{2.4}$$

Total charge under gate terminal may be written as Eq. 2.5, where, L is gate length of the device, $\varepsilon_0\varepsilon_r$ is effective permittivity of n-AlGaAs donor and spacer layers, h is the thickness of both n-AlGaAs donor and spacer layers, and V_G is applied gate voltage [29].

$$WLqn_{2D} = \frac{WL\varepsilon_0\varepsilon_r}{h}V_G \tag{2.5}$$

Transconductance of HEMT devices has been shown in Eq. 2.6, which depends on the thickness of AlGaAs donor and spacer layers (gate channel separation) and effective carrier velocity through the channel [29].

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\varepsilon_0 \varepsilon_r v_{eff}}{h} W \tag{2.6}$$

Transconductance represented in Eq. 2.6, assumes current saturation condition. Here, the semiconductor layer is uniformly doped and saturation occurs everywhere beneath the gate. This model is also reasonably applicable to short gate length devices [19].

2.3.4 Small Signal Equivalent Circuit Model of HEMTs

Small signal equivalent circuit models are utilised to describe RF behaviour of a transistor and are representative of various resistive, capacitive, inductive and transconductance effects taking place within the transistor. These also help to identify parasitic effects in transistors. The RF behaviour depicted by HEMTs is very similar to FETs, except that the device transconductance is different. Fig. 2. 18 shows lumped component equivalent circuit model of HEMT devices, which has been discussed in [14], [29], [16].

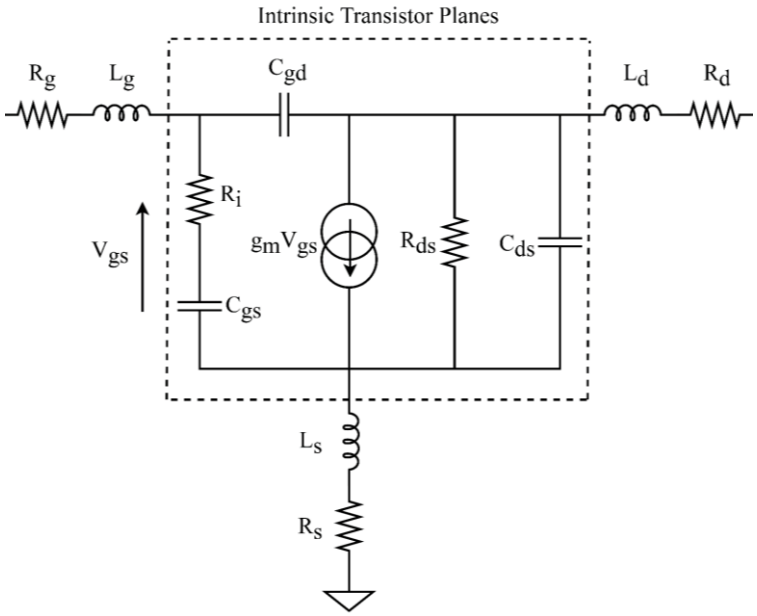


Fig. 2. 18: Lumped component equivalent circuit model of an FET

Gate to source capacitance C_{gs} represents charge beneath the gate in depletion region towards the source. Gate-drain capacitance C_{gd} represents charge in the depletion region towards the drain, generation and modulation of which is controlled by the gate to drain voltage. Overall gate capacitance is the sum of C_{gs} and C_{gd}, which has been given in Eq.

2.7 [29], where, L_g is gate length of the device, and a is thickness of the depletion region below the gate. These variables are utilised in Eq 2.7 to Eq. 2.9.

$$C_g = \frac{\varepsilon_0 \varepsilon_r W L_g}{a} \tag{2.7}$$

Input resistance R_i of the device, also known as the channel resistance, represents impedance of the semiconductor beneath the gate. R_{ds} represents finite output impedance of the device. The value of output impedance at microwave frequencies is lower than the value at DC. Robertson (2001) in [29] explains that this is caused by dispersion which mainly occurs because of charge exchange within deep levels at the junction between device buffer and channel. Drain to source capacitance C_{ds} is represented parallel to the output impedance R_{ds} because of capacitive coupling between drain and source's doped region that are separated via the depletion region. This is also called output capacitance of the device. Current generator within the device indicates small signal or linear gain of the device, and is product of transconductance (g_m) and V_{gs} (voltage applied at the gate terminal or alternatively voltage drop across gate capacitance (C_g).

Extrinsic components of the model include source and drain series parasitic resistances R_s and R_d. Robertson (2001) in [29] discusses that these parasitic impedances arise because of contact resistance due to ohmic contact to the device channel and semiconductor's bulk resistance in the two interface access regions, i.e. drain-gate and source-gate. Gate resistance R_g has been expressed in Eq. 2.8 [29].

$$R_g = \frac{\rho W L_g}{3m^2 y L_g} \tag{2.8}$$

Where, ρ is resistivity of the gate material, m is number of gate fingers, and y is the gate height. Distributed nature of RF gate resistance is indicated by a factor of 3 in the denominator of Eq. 2.8. Current gain of the device is the ratio between drain and gate currents and has been given in Eq. 2.9 [29].

$$\frac{i_d}{i_g} \approx \frac{g_m}{j\omega(C_{gs} + C_{gd})} \tag{2.9}$$

Based on the preceding discussion, cut off frequency of the FET (f_T), which is the frequency at which the short circuit current gain of the transistor is unity (with drain shorted to source, i.e. $V_{out} = 0$ V). Eq. 2.10 [29] represents cut-off frequency.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.10}$$

Cut-off frequency can also be given in terms of effective carrier velocity v_{eff} through the channel (Eq. 2.11) and lumped component elements shown in the equivalent circuit model of Fig. 2. 18 as Eq. 2.12 [29].

$$f_T = \frac{v_{eff}}{2\pi L_g} \tag{2.11}$$

$$f_T = \frac{g_m}{2\pi\left[\left(C_{gs} + C_{gd}\right)\left(1 + \frac{R_s + R_d}{R_{ds}}\right) + g_m C_{gd}(R_s + R_d)\right]} \tag{2.12}$$

The relationships given in Eq. 2.10 – 2.12 are important and lay foundations in the design of active devices including amplifiers and oscillators. To achieve large cut-off frequency (f_T), it is necessary to minimise gate parasitics that include C_{gs} and C_{gd}, and parasitic resistances within the transistor that include R_s and R_d. Robertson (2001) and Virdee (2004) in [29] and [30], respectively have discussed that this may be achieved by having an effectively high carrier velocity in the channel, shorter gate length processes, and technologies that are well engineered to provide low parasitic resistances.

Small signal lumped component model (shown in Fig. 2. 18) can also be utilised to express maximum available gain and maximum frequency of oscillation (f_{max}) of the device, which are the maximum power gain that can be achieved from an FET (or HEMT) when the gate (input) and drain (output) terminals are conjugately matched, and the frequency at which maximum available gain falls to unity, respectively. Maximum available gain (at frequency f) and f_{max}, derived by Robertson (2001) in [29] have been given in Eq. 2.13 and 2.14, respectively.

$$\text{MAG} = \frac{\left(\frac{f_T}{f}\right)^2}{4\left(\frac{R_g + R_i + R_s}{R_{ds}}\right) + 4\pi f_T C_{gd}\left(2R_g + R_i + R_s\right)} \tag{2.13}$$

$$f_{max} = \frac{f_T}{2\left[\left(\frac{R_g + R_i + R_s}{R_{ds}}\right) + \left(2\pi f_T R_g C_{gd}\right)\right]^{\frac{1}{2}}} \tag{2.14}$$

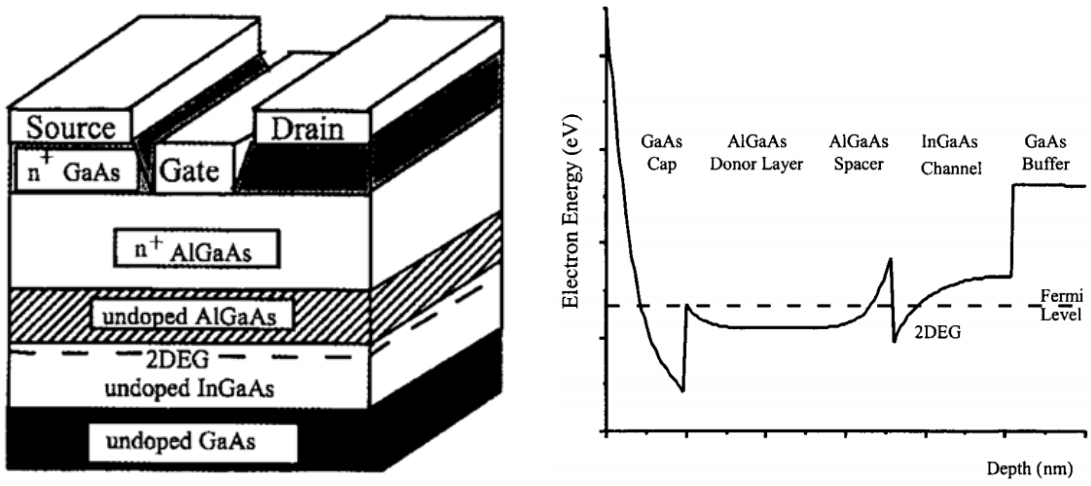
The maximum frequency of oscillation (f_{max}) can be optimised for high frequency operation by considering its direct dependence on f_T, and requires reduction of gate resistance (R_g), which has been expressed in Eq. 2.8. Robertson (2001) in [29] explains that R_g may be reduced by increasing the number of fingers; however, it causes parasitic

capacitive effects between parallel gate fingers which results in reduction of f_T and f_{max}. However, other techniques like T-gate where a short gate-length device with a large cross-sectional area may be utilised to effectively reduce gate resistance. Chung (2010) in [31] explains that f_{max} up to 400 GHz in AlGaN/GaN HEMT devices may be achieved by using recessed source/drain Ohmic contacts and by having a short source-drain distance.

This section presented detailed discussion about small signal equivalent circuit model of FETs (and HEMTs). However, in the design of power amplifiers and oscillators, large signal (or non-linear) effect of parasitic elements are also required to be considered which will be discussed in Chapter 3 of this thesis, alongside the review of power amplifiers and oscillators.

2.3.5 Pseudomorphic High Electron Mobility Transistor

Pseudomorphic HEMTs (pHEMTs) are advanced vertical structure HEMT devices that have an additional thin pseudomorphic layer of a semiconductor material that is strained to the lattice constant of the surrounding semiconductor material; commonly used to increase operating frequency and electron mobility. Typically, an additional thin layer of InGaAs called the pseudomorphic layer is introduced with the surrounding AlGaAs layer in GaAs HEMT devices. Marsh (2006) and Robertson (2001) in [28] and [29], respectively suggest that higher electron mobility and charge density on the sheet can be achieved this way, due to better charge carrier transport properties of InGaAs and larger bandgap discontinuity with the surrounding AlGaAs layer. Cross sectional structure of AlGaAs/InGaAs/GaAs pHEMT and its conduction band diagram has been shown in Fig. 2. 19 (a) and Fig. 2. 19 (b), which have been reproduced from [29].



(a) (b)

Fig. 2. 19: (a) cross-sectional area and (b) conduction band diagram of AlGaAs/InGaAs/GaAs pseudomorphic HEMT [29]

InGaAs layer has indium concentration in the range of 20-30% [28], making lattice constant of the channel greater than i-GaAs substrate layer, buffer and cap layers, n-AlGaAs donor layer, and i-AlGaAs spacer layer. This way a strained channel is formed. Strain of the channel can be accommodated within the crystal without any defects if the channel layer is kept extremely thin. Thus, the channel takes lattice constant of rest of the structure and is called pseudomorphic [28], [29]. Under these concentrations of iridium, channel mobility is increased along-with slight increase in effective charge velocity, thus, improving high frequency performance of the device.

Conduction band diagram in Fig. 2. 19 (b) reveals two conduction band discontinuities, i.e. 1) At the interface between n-GaAs Cap layer and n-AlGaAs donor layer, and 2) At the interface between AlGaAs spacer and InGaAs pseudomorphic layer. However, the discontinuity is larger at the later heterojunction because of the smaller bandgap of InGaAs compared to GaAs. Thus, the channel sheet concentration in GaAs pHEMT is larger compared to the GaAs HEMT providing it larger drive current capabilities. Step in the conduction band at the InGaAs/GaAs buffer layers indicate that the device channel electrons are confined at the backside, thus, providing improved charge control and pinch-off sharpness, and reducing output conductance of the device. The higher drive current capability is an important consideration and paves the path to the development of high-power class AB amplifier and class E oscillator that have been presented in Chapter 6 and Chapter 7 of this thesis, respectively.

2.3.6 AlGaN/GaN HEMT Structure

A simplified structure of AlGaN/GaN HEMT has been shown in Fig. 2. 20, while a more practical structure presented in [22] has been shown in Fig. 2. 21. The layer structure consists of a substrate material that may be SiC, Si or Sapphire, followed by the 'nucleation layer'. GaN buffer/channel layer and AlGaN barrier layers are at top of the nucleation layer. Cap, Ohmic drain and source contacts and Schottky gate are located at the top [22]. Source and drain contacts are generally alloyed contacts with titanium (Ti), aluminium (Al), nickel (Ni) or gold (Au). The cap layer in the structure shown in Fig. 2. 21 may be an undoped GaN or AlGaN while the barrier layer is AlGaN. The barrier layer is generally 30 nm thick with aluminium (Al) concentration (x) varying in the range $0.15 < x < 0.3$. The barrier layer may be undoped or doped. However, with undoped barrier layers, the 2DEG is formed primarily due to the polarization effects which has been discussed earlier in this chapter. Polarity of the AlGaN and GaN layers are enabled

through the nucleation layer that also helps in monocrystalline growth of these layers above the highly mismatched SiC or sapphire substrates [22].

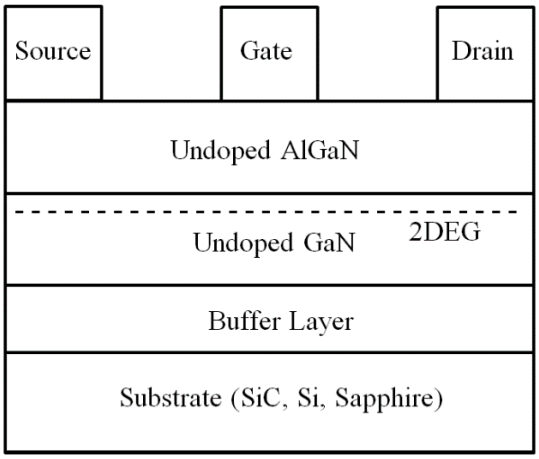


Fig. 2. 20: cross sectional structure of a basic GaN HEMT

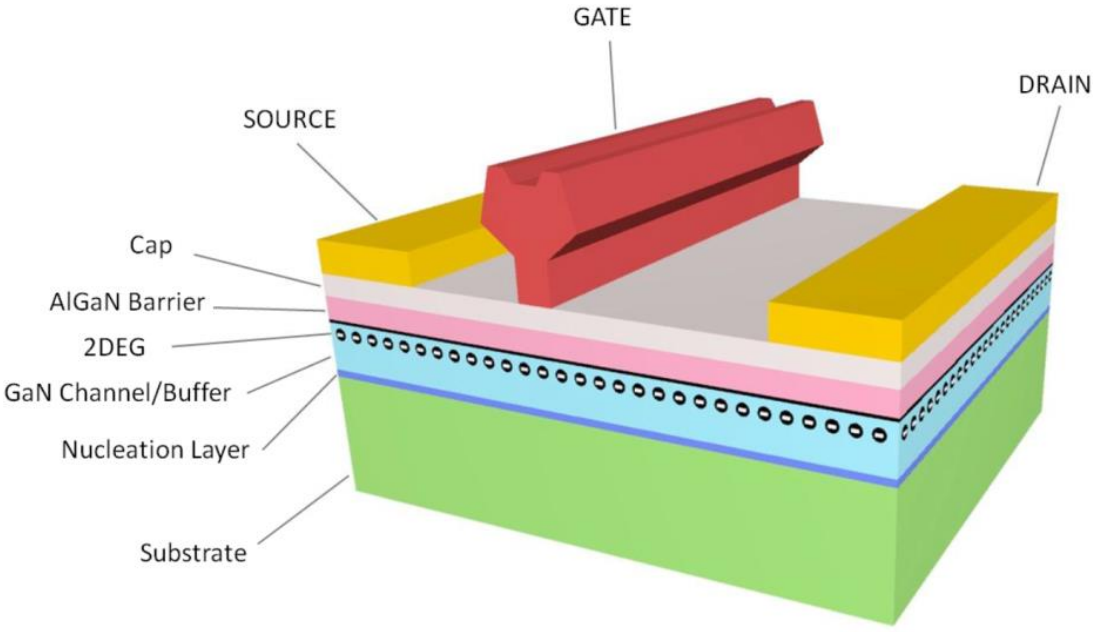


Fig. 2. 21: A practical GaN HEMT structure presented by Marsh (2006) in [22]

GaN HEMT devices having high critical breakdown field can provide high drain voltage operation enabling the device channel to operate at very high temperatures. This requires the substrate to efficiently conduct and dissipate heat from the device, to prevent the channel from over- heating. Dissipation of heat depends upon the heat flow equation given in Eq. 2.15 [29].

$$c\frac{\partial T}{\partial c} = \vec{\nabla} \cdot \left(k\vec{\nabla}T\right) + H \tag{2.15}$$

Where, c is the heat capacity, k is the thermal conductivity, H is the rate of Joule heat generation given by $H = \vec{j} \cdot \vec{E}$ [29]. Thermal behaviour of various substrate materials has been given in Table 2. 3, which are based on two different sources in [32], [33].

Table 2. 3: Thermal parameters of various substrate material [32], [33]

Substrate	Thermal Conductivity ($W.cm^{-1}.K^{-1}$)	Heat Capacity ($J.g^{-1}.K^{-1}$)	Density ($g.cm^{-3}$)
Al_2O_3	0.35-0.42	0.77	3.98
Si	1.5	–	–
4H-SiC (sapphire)	3.3-3.6	0.66	3.21
GaN	1.6-1.7	0.49	6.1

SiC is a very popular substrate material for GaN HEMT devices having a lattice mismatch of 4% with GaN. SiC substrate is preferred for high frequency operation of the device with the density of dislocation under 3×10^8 cm^{-2}. The nucleation layer of AlN is generally added to the vertical architecture of HEMT devices to ensure smooth transition from the crystalline structure of SiC to GaN [34]. Sapphire has a lattice mismatch between 14-23% with GaN, depending on relative orientation between the two materials. As observed from Table 2. 3, the thermal conductivity of sapphire in comparison to other substrate materials is poor. However, sapphire is a comparatively cheaper substrate material and readily available in large dimension wafers [34]. Si has a lattice mismatch around 17% with GaN crystal. Performance of GaN device grown on a silicon substrate is degraded because of crystalline defects that may occur during device growth [32], [34]. Wolfspeed in [35] recently presented a GaN on SiC mmWave Foundry process for high frequency applications requiring high efficiency and wider bandwidth operation. The process provides a SiC substrate thickness of 75 µm in a GaN on SiC MMIC process.

2.3.7 DC Characteristics of GaN HEMTs

DC behaviour of GaN HEMTs is similar to the behaviour of FETs discussed earlier in this chapter. However, the characteristics presented in this section consider various non-linear, parasitic and trapping effects observed in GaN HEMT devices. Fig. 2. 22 shows DC IV characteristics of GaN HEMT device presented by Fornetti (2010) in [36]. These characteristics have been shown for GaN HEMT device limited with different maximum values of drain voltage (V_D) [36].

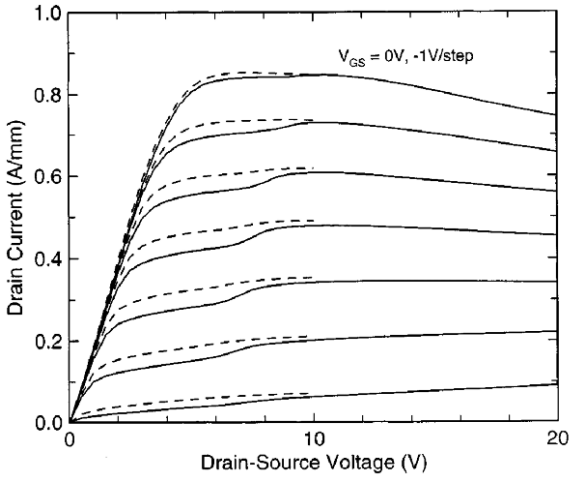


Fig. 2. 22: Drain I-V Characteristics of GaN HEMT [22]

Two cases have been shown in Fig. 2. 22. The first case limits maximum drain voltage to 10 V (dashed line), while the second case limits maximum drain voltage to 20 V (solid line). Reduction in drain current for the latter case has been observed due to current dispersion (or collapse) for a higher value of drain voltage. This effect is attributed to current dispersion because of hot electrons and trapping in the buffer layer [36].

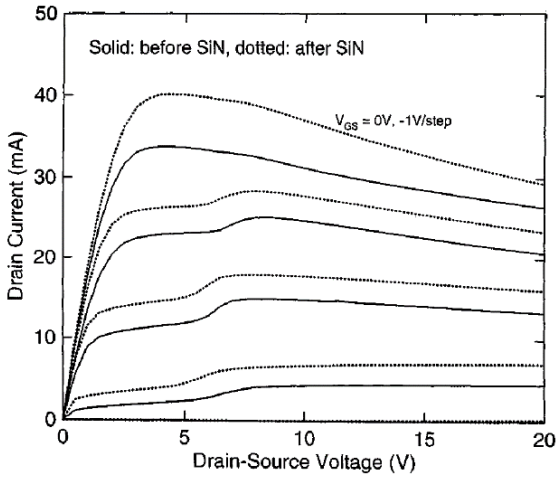


Fig. 2. 23: Drain I-V Characteristics of GaN HEMT with SiC Passivation Layer [22]

Introduction of SiC passivation layer is an important technique to mitigate surface state degradations in the device operation of GaN HEMTs. DC characteristics of the GaN HEMT device with SiC passivation layer have been shown in Fig. 2. 23. Binari (2002) in [37] discusses that with SiC passivation layer, the electron sheet density improves resulting in an increase in the drain current. This is an important design aspect to consider in high power amplifiers, which facilitates large drain current and help to achieve high gain and power. A typical AlGaN/GaN HEMT transistor with SiC passivation layer discussed by Mishra (2002) in [38] has been shown in Fig. 2. 24.

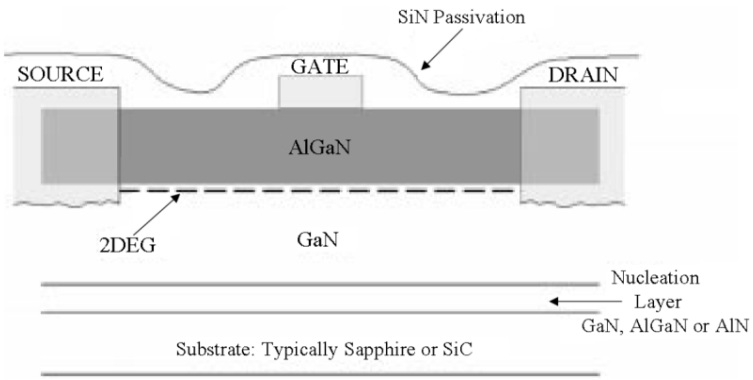


Fig. 2. 24: AlGaN/GaN HEMT with SiC Surface Passivation [24]

2.3.8 RF Limitations of GaN HEMT Devices

RF limitations of GaN HEMT devices are mainly experienced during high power operation when the transistor operates in the non-linear or saturated region. High efficiency power amplifiers and the oscillator discussed in this thesis operate in saturation region with low-voltage/high-current or high-voltage/low-current conditions; which makes RF limitations of the transistor an important design consideration. Trew (2004) in [39] has discussed *IV* characteristics of an AlGaN/GaN HEMT with non-linearities occurring both due to high voltage and high fields. This has been shown in Fig. 2. 25.

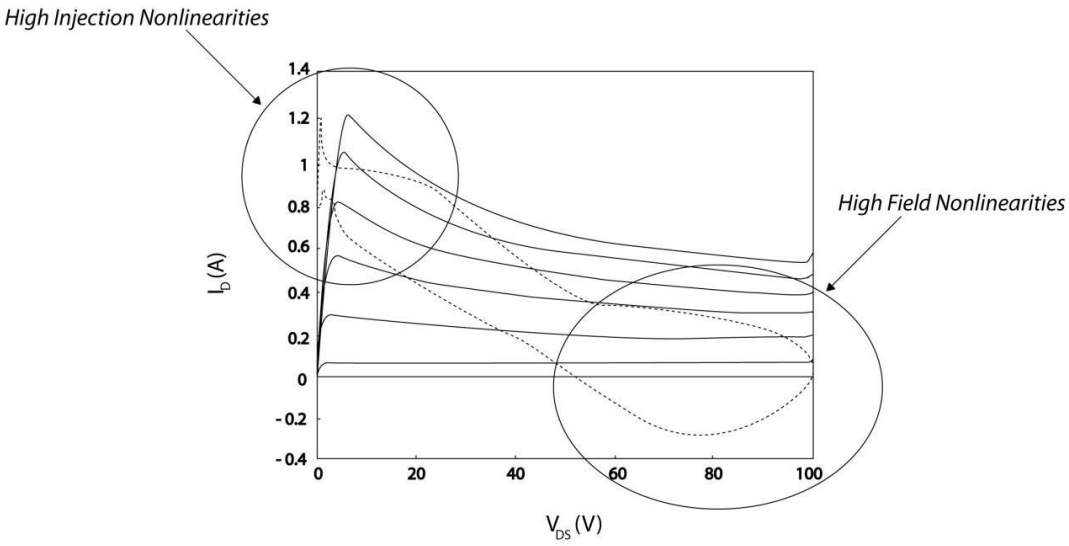


Fig. 2. 25: DC and RF current-voltage characteristics for an AlGaN/GaN HFET class A amplifier under optimum power added efficiency at 10 GHz ($V_{DS} = 40$ V) [25]

Fig. 2. 25 illustrates two different non-linearities, i.e. 1) high injection non-linearities due to high charge injection under low voltage or high current operating conditions, and 2) high field non-linearities due to high gate leakage and surface trap charges under high voltage or low current operating conditions. Similar non-linear behaviour is also experienced in conventional GaAs based HEMT devices. However, these effects are more

significant in GaN devices due to their high values of current densities and electric fields [39]. Non-linearities of GaN devices occurring due to physical phenomenon are associated with the free movement of electrons within the device due to an applied electric field [36].

GaN devices can be operated with very high voltage due to their wide bandgap energy. As a result, high electric field and current densities are induced within the device resulting into large amount of heat generation. Balaz (2010) in [34] has discussed that transport properties of electrons within the lattice structure are affected due to an increase in the lattice temperature; and substrates with large amount of thermal conductivity are required for high power GaN devices due to their effective heat dissipation.

High efficiency operation of the device requires either the voltage or current waveform to be zero, which makes the current-voltage product zero. Thus, 100% device efficiency may be achieved. However, current voltage product or power consumption cannot be effectively zero because of the finite resistance and parasitic capacitances of the device. For GaN HEMT devices, the power loss during on-state of the device is low along-with the parasitic capacitances. Joshin (2014) in [29] discusses that low power loss during on-state enables GaN HEMT transistors to operate with lower power consumption compared to other Si and GaAs based devices.

2.4 Conclusion

This chapter presented an overview of semiconductor technologies that includes Si and advanced GaAs and GaN materials. Some properties of heterostructures and the corresponding HEMT devices that may be fabricated from them to achieve high frequency, power and efficiency operation were also discussed. These provide basic concepts about the structure of transistor which are used in the design of high efficiency discrete and MMIC power amplifiers (presented in Chapters 4 and 6) and high efficiency MMIC oscillator (discussed in Chapter 7). Small signal equivalent circuit model and various parasitic elements like output capacitance and output impedance were discussed which play an important role in high efficiency power amplifiers. Definitions of current gain, cut-off frequency, maximum available gain and maximum frequency of operation in terms of small signal equivalent circuit model were stressed.

Chapter 3

High Efficiency Power Amplifiers and Oscillators in Review

3.1 Introduction

Active devices like transistors and vacuum (or electron) tubes are used for signal detection, generation, amplification, mixing, multiplication and switching operation in RF and Microwave systems. The operation of a transistor for amplifiers and oscillators is governed by various factors including: high resistance current source or switch that remains 'on' for a specific interval, or hybrid of the two where the transistor acts both as a current source and a switch during separate parts of the 'on' interval; bias conditions and input signal level that may drive the transistor into saturation or non-linear region of a transistor's IV-curve; and termination networks that may be designed for fundamental frequency component or to trap higher order harmonic components. *Fig. 3. 1* illustrates IV transfer characteristics of an FET [41], [42].

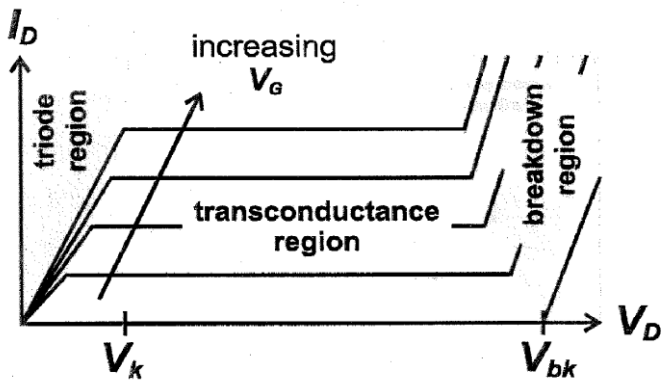


Fig. 3. 1: IV Characteristics of an FET [41]

Three regions to consider in the transfer characteristics shown in *Fig. 3. 1* are triode, transconductance and the breakdown region. Within the triode region (also called linear region), the device conducts large current linearly with an increase in the drain voltage. In this region, the drain current is very sensitive to any changes in drain voltage and the transistor may be considered as a controlled resistor. However, when the transistor is sufficiently forward biased above the knee voltage (V_k) with a high value of $+V_D$, the IV characteristics of the transconductance (also called saturation) region are observed. Saturated current (I_{sat} or I_S) is observed that is independent of changes in the drain voltage and the transistor may be described as a controlled current source. Any further increase in drain voltage beyond the breakdown voltage (V_{bk} or V_{BR}) causes the current to become very high due to breakdown of the channel. This results in destructive failure

or breakdown of the transistor. Based on transistor's region of operation, conduction angle of the input signal through the channel, bias conditions, and the termination networks; amplifiers may be broadly classified as: transconductance amplifiers, saturated transconductance amplifiers, saturated amplifiers with harmonic trapping networks, and switching amplifiers which will be explained later in this chapter.

An oscillator uses an active nonlinear device alongside a passive feedback network or resonator to convert DC into steady state sinusoidal RF or microwave signal. At higher RF and microwave frequencies cavity or dielectric resonators are used to produce oscillations at fundamental frequencies up to 100 GHz [42]. Generally, the behaviour of an oscillator is that of an amplifier operating in the transconductance region with a feedback path. This may be provided through the operation of an amplifier in the unstable region or through a transmission line or lumped component feedback path between the drain and gate of an FET, to provide the necessary conditions for oscillations until a steady state is achieved. Oscillators are broadly classified as feedback oscillators and negative resistance oscillators [42] which will be explained in the later part of this chapter.

Thus, design and analysis of power amplifiers and oscillators require the consideration of non-linear or saturation region of the IV-curves of a transistor's operation, large signal boundaries, and the behaviour of higher order frequency harmonics. These also dependent on material properties of the semiconductor discussed in Chapter 2, for instance GaN HEMTs can be driven with a larger input power level compared to GaAs HEMTs due to their higher breakdown voltage; making the former more lucrative for power hungry applications.

This chapter presents overview of power amplifiers and oscillators, which has been divided in four parts: study of non-linear effects, design considerations and large signal characterisation of power amplifiers; various classes of amplifiers; high efficiency power amplifiers; and microwave oscillators.

3.2 Non-Linear Behaviour of Power Amplifiers and Design Considerations

3.2.1 Weakly Non-linear Effects

Consider the block diagram of an amplifier shown in Fig. 3. 2 where the amplifier block includes an active transistor and passive matching circuitry. The output of this amplifier consists of an infinite number of non-linear products or harmonics that have been represented by Cripps (2006) in Eq. 3.1 [41].

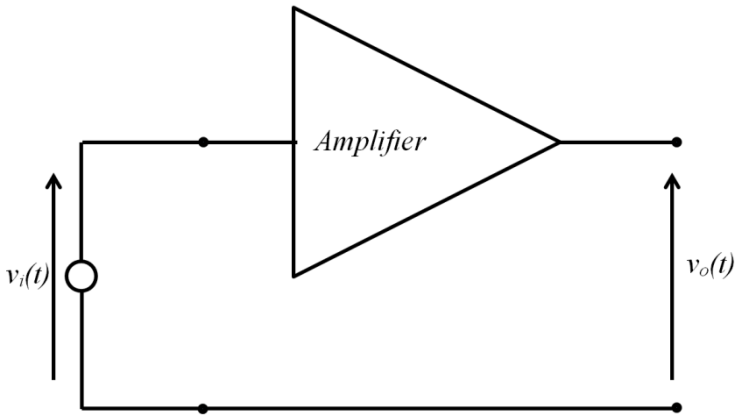


Fig. 3. 2: Amplifier representation with block including input and output matching networks [41]

$$v_o = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + a_4 v_i^4 + \cdots \quad (3.1)$$

Weakly non-linear effects represented by third degree power series have been illustrated through dotted line in Fig. 3. 3. The power series expressed in Eq. 3.1 may also be expressed by including phase effects as Volterra series. However, it represents non-linear behaviour of the device in the vicinity of its DC bias or operating point. The coefficients, $a_1, a_2, a_3, \ldots$ are very sensitive to the input and output drive levels and to the operating bias point of the device. This formulation is useful to evaluate "weakly non-linear" behaviour of the device that includes lower level intermodulation distortion (< -30 dBc). However, strong non-linear behaviour of the device due to its operation in the cut-off or saturation region for high power or high efficiency amplifiers cannot be described by Eq. 3.1. Especially, when the amplifier is driven beyond 1 dB compression point [41].

3.2.2 Strongly Non-linear Effects

Strongly non-linear effects are especially important in power amplifiers, which occur due to limiting behaviour of the transistor. These occur when the input signal waveform distorts due to its swing outside the linear region of transistor operation. Consider the ideal transfer characteristics of a FET illustrated in Fig. 3. 3 by Cripps (2006) in [41].

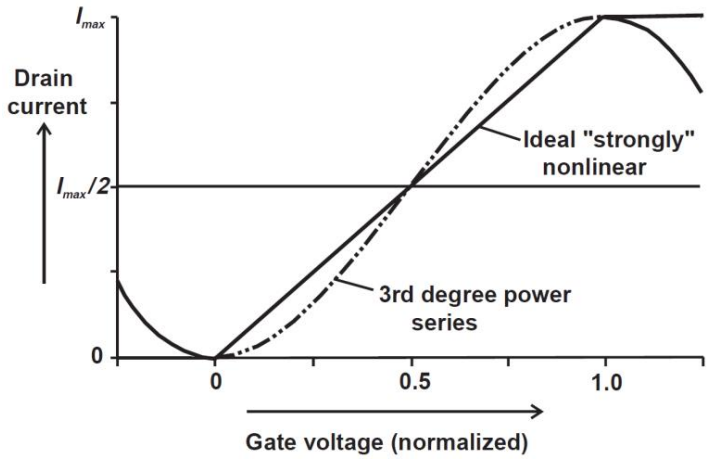


Fig. 3. 3: Transfer characteristics of an ideal FET with strongly and weakly non-linear effects [41]

In Fig. 3. 3, dotted line represents weakly non-linear effects while solid line represents strongly non-linear effects. This behaviour is highly idealized; however, a more realistic behaviour has been shown by the dotted line where weakly non-linear behaviour has been modelled [41]. High enough negative gate voltage applied to the transistor completely closes the drain channel, this condition (expressed in Chapter 2) is called the cut-off or pinch-off of the device. Besides this, drain channel is fully open when the applied gate voltage $V_{GS} = 0$ and the device operates in saturation. Channel current can be modelled by using a third order power series represented in in Eq. 3.2. However, strongly non-linear effects cannot be justified through it, as outside the linear region hard shifts to saturation or linear region are highly idealised [41]. Thus, higher order terms need to be added to Eq. 3.2 to explain strongly non-linear effects. A combined weak and strongly non-linear model of the drain current presented by Cripps (2008) in [41] corresponding to Eq. 3.2 has been illustrated in Fig. 3. 4.

$$I_d = +3 \cdot V_G^2 - 2 \cdot V_G^3 \tag{3.2}$$

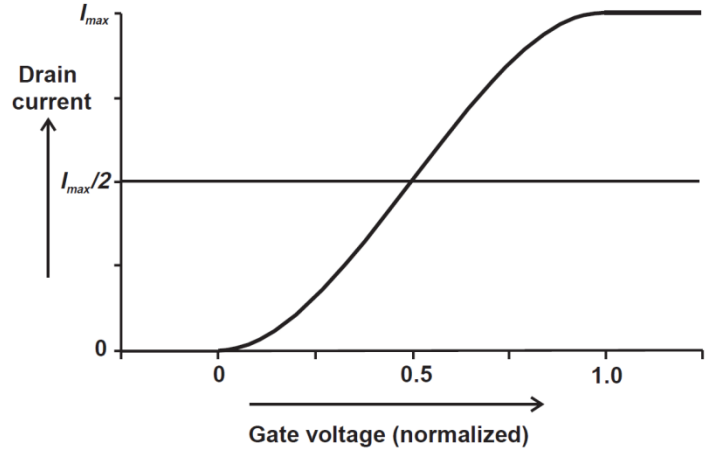


Fig. 3. 4: Combined weak and strong non-linear model of an FET [41]

It has been discussed in [41] that small signal linear gain and third degree non-linearities are a function of operating DC bias point of the transistor. In CAD applications utilised to design amplifiers, complete model of a transistor should include: physical architecture of the transistor involving physical behaviour and fabrication specific physics; equivalent small signal and large signal circuit behaviour represented in terms of circuit elements; and electrical behavioural model of the transistor described in terms of measured DC characteristics at various bias conditions [41]. In terms of output spectrum, the non-linear behaviour of an amplifier has been illustrated in Fig. 3. 5.

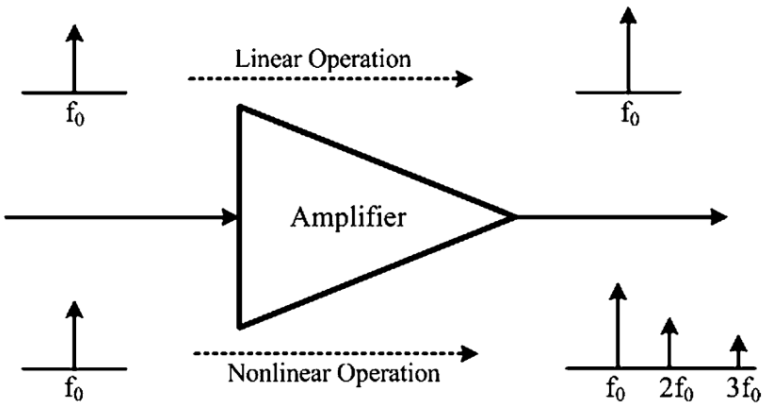


Fig. 3. 5: Harmonic spectrum representation of linear and non-linear behaviour of an amplifier [43]

3.2.3 Gain Compression and 1 dB Compression Point

Considering the amplifier shown in Fig. 3. 2 operates in the non-linear region as a current source, the output containing various products called harmonic products (or harmonics) may be represented using the power series shown in Eq. 3.3 [41], where c_n are the respective nth order coefficients.

$$i_{out}(t) = c_o + \frac{c_2 \cdot V_1^2}{2} + \left(c_1 \cdot V_1 + \frac{3 \cdot c_3 \cdot V_1^3}{4}\right) cos(\omega_1 t) + \frac{c_2 \cdot V_1^2}{2} cos(2\omega_1 t) + \frac{c_3 \cdot V_1^3}{4} cos(3\omega_1 t) \quad (3.3)$$

In Eq. 3.3, first two terms on the right-hand side of the equation represent DC component of the output current, third term represents the fundamental component or harmonic, fourth term represents the second harmonic, while the fifth term represents the third harmonic [43]. A quantitative measure of the onset of an amplifier's saturation is provided by 1 dB compression point that is defined as input power for which the output power is 1 dB less than that of an idealized amplifier [43], [44]. The gain corresponding to 1 dB compression point is expressed as: $G_{1dB} = G_o - 1$ dB, where G_o is small signal linear gain of the transistor, and $G_{1\text{dB}}$ is the gain at 1 dB compression point. Fig. 3. 6

illustrates the concept of 1 dB compression point and reduction of gain from linear behaviour. Fundamental component is defined by the term $c_1 v_1$when the amplifier behaves linearly. However, non-linear behaviour of the amplifier requires an additional third order term $\frac{3 \cdot c_3 \cdot V_1^3}{4}$ for the definition of fundamental component, to indicate the dependence on transistor's physical properties and the phase between $c_1$and c_3. Deeper the transistor is driven into compression, larger would be the signal power transferred from fundamental component to higher order harmonics. This defines the concept of gain compression [43].

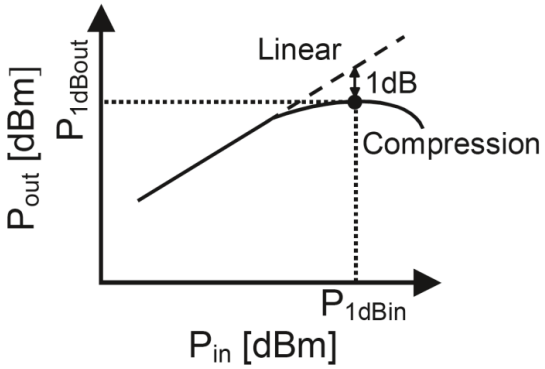


Fig. 3. 6: Illustration of 1 dB compression point and gain compression [43]

Gain compression plays an important role in the design of high efficiency power amplifiers. A very large input power level would drive an amplifier into deep saturation levels where non-linearities would be high and the gain would be highly compressed. For these amplifiers, gain compression up to 3 dB (or even 6 dB) is analysed during the design stage resulting in higher order harmonic having higher power levels. This results in efficiency enhancement through higher order harmonic components trapping. Fig. 3. 7 shows a typical output spectrum of class E MMIC amplifier to emphasize the effect of gain compression on harmonic components. The effect of gain compression at 1 dB, 3 dB and 6 dB levels on spectral components at the fundamental, second, third and fourth harmonic frequencies has been elaborated. Suitable output termination network can be utilised to trap higher order harmonic components for efficiency and output power enhancement at higher gain compression levels.

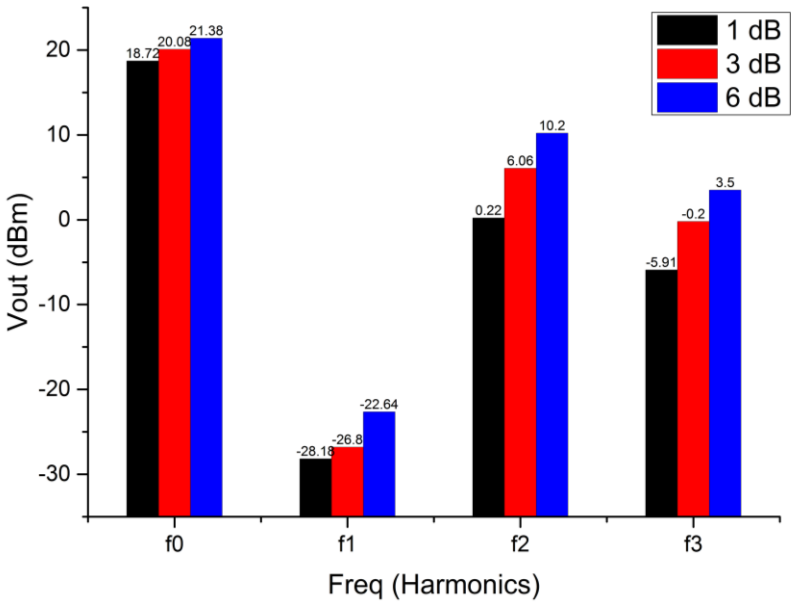


Fig. 3. 7: Output spectrum of EM simulated class E MMIC amplifier (f_0=14.5 GHz)

3.2.4 Intermodulation Distortion

Third order intercept point is defined as the intersection between power curves of the fundamental frequency and third order intermodulation frequency components. Consider a time-varying signal: $v_{in}(t) = V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t)$ is input to a non-linear device. Output of the device will consist of various products defined in Eq. 3.4 [43].

$$
\begin{aligned}
i_{out}(t) = {} & c_o + c_1[V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t)] \\
& + c_2 \left[\frac{V_1^2}{2}(1 + \cos(2\omega_1 t)) + \frac{V_2^2}{2}(1 + \cos(2\omega_2 t)) \right. \\
& \left. + V_1 V_2 (\cos(\omega_1 + \omega_2)\, t + \cos(\omega_1 - \omega_2)\, t) \right] \\
& + c_3 \left[\left(\frac{3}{4} V_1^3 + \frac{3}{2} V_1 V_2^2 \right) \cos(\omega_1 t) \right. \\
& + \left(\frac{3}{4} V_2^3 + \frac{3}{2} V_2 V_1^2 \right) \cos(\omega_2 t) \\
& + \frac{3 V_1^2 V_2}{4} (\cos(2\omega_1 + \omega_2)\, t) \\
& + \frac{3 V_1^2 V_2}{4} (\cos(2\omega_1 - \omega_2)\, t) \\
& + \frac{3 V_2^2 V_1}{4} (\cos(2\omega_2 + \omega_1)\, t) \\
& + \frac{3 V_2^2 V_1}{4} (\cos(2\omega_2 - \omega_1)\, t) + \left(\frac{3}{4} V_1^3 \right) \cos(3\omega_1 t) \\
& \left. + \left(\frac{3}{4} V_2^3 \right) \cos(3\omega_2 t) \right] + \cdots
\end{aligned}
\tag{3.4}
$$

Eq. 3.4 shows intermodulation products that may be represented by: $(n \cdot \omega_1 \pm m.\, \omega_2)$ are generated besides the fundamental component and its harmonics. These intermodulation

products cause distortion in the output of non-linear amplifiers, known as *intermodulation distortion*. Fig. 3. 8 illustrates the output spectrum of the output signal expressed in Eq. 3.4 up to a limited order [43].

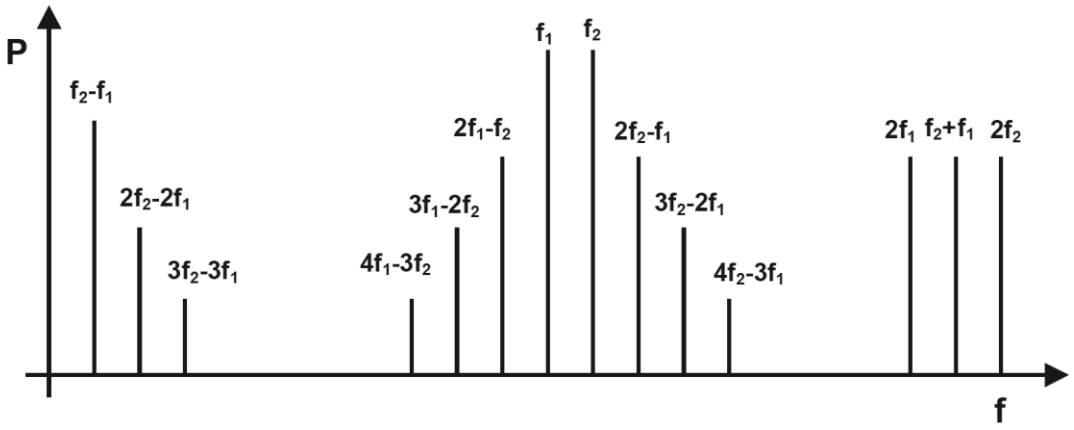


Fig. 3. 8: Output spectrum of a non-linear device showing fundamental component, higher order harmonics and intermodulation products [43]

The third order intermodulation (IM3) or third order intercept point (IP3) are important figures of merit for the linearity of microwave circuits and networks [43]. These are defined by the frequencies: $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ and due to proximity of IM3 with the fundamental frequency, it is difficult to filter them out.

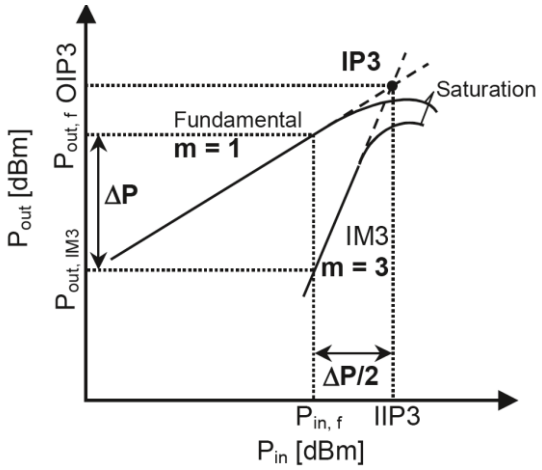


Fig. 3. 9: Extrapolation of the TOI [43]

At lower levels of input power, the signal doesn't swing in the saturation or non-linear region, thus the slope between input and fundamental component is unity and the IM3 is very low. However, for larger input power levels, the effect of IM3 becomes significant due to the term V^3. Considering Fig. 3. 9, IP3 at the input (IIP3) may be expressed through Eq. 3.5 [43].

$$IIP3 = P_{in,fundamental} + \frac{\Delta P}{2} \tag{3.5}$$

Where, $\Delta P = P_{out,fundamental} - P_{out,IM3}$.

3.2.5 Large Signal Characterisation of Power Amplifiers

A transistor will behave linearly when the input signal power is below 1 dB compression point within the linear region and will start to observe non-linearities as it approaches compression. Under these conditions, small signal performance of the device (or *[S]*-parameters) will be inadequate to predict performance of the amplifier and will require consideration of other factors like: transistor bias conditions, transconductance, non-linearities, input signal drive level, load and source termination networks, operating frequency and the device's temperature.

Large signal device modelling helps to characterise the performance of a transistor by measuring output power and gain as a function of operating frequency, bias conditions, and the source and load termination impedances. This is performed by determining large signal source or load reflection coefficients and the associated impedances to achieve a specified output power or gain from the amplifier. Large signal modelling is important in the design of power amplifiers, as it helps to identify gain compression or expansion, harmonic distortion or intermodulation distortion at large input signal levels. The corresponding optimum load and source impedances are measured or simulated using hardware or software-based techniques, respectively to achieve the desired performance in terms of power or power added efficiency of the amplifier.

Drain Efficiency and Power Added Efficiency

Drain efficiency and power added efficiency are important figures of merit for power amplifiers where an input signal swings through the drain channel of the transistor and appears across the drain terminal. Fig. 3. 10 illustrates power flow across various terminal/ports within an amplifier circuit. P_{in} or input power is transferred from the source to the input matching networks. If the transistor is conjugately matched to the input matching network, maximum power will be transferred to the transistor's gate terminal which in-turn flows through the channel. A part of this power will be reflected or dissipated as heat (P_{diss}) due to mismatches, leading to a non-zero value of the reflection coefficient. DC power is also provided to the active device through its DC bias (P_{DC}) which causes the transistor to operate in a particular transconductance region to amplify P_{in}. Due to non-linear nature of the amplifier, harmonic products will be generated. This has been indicated through two output power representations, i.e. P_{out} and $(P_{out})_{\mathrm{H}}$, which are output power at fundamental frequency component and harmonic frequencies,

respectively. At each stage within the amplifier, power is also lost as heat due to the lossy nature of these stages.

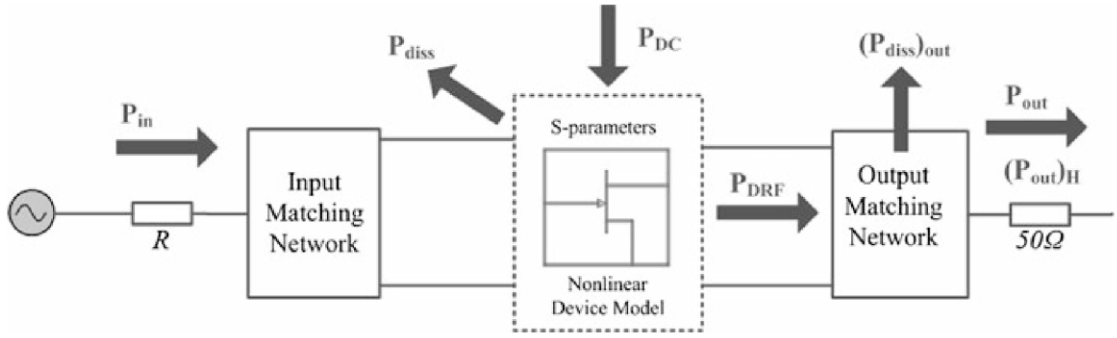


Fig. 3. 10: Power flow representation within an amplifier network [43]

Drain efficiency is defined as the ratio between output power of the amplifier and DC bias power provided to the transistor. The relationship for drain efficiency has been expressed in Eq. 3.6 [45].

$$\text{Drain efficiency} = \eta_D = \frac{P_{out}}{P_{DC}} \tag{3.6}$$

Drain efficiency is an important figure of merit for amplifiers that provide larger gain without considering the effect of input power. Total efficiency of an amplifier however considers all the powers input to the amplifier that includes power of the input drive signal. The relationship for total efficiency has been expressed in Eq. 3.7 [45].

$$\text{Total efficiency} = \eta_T = \frac{P_{out}}{P_{DC} + P_{in}} \tag{3.7}$$

Power added efficiency is an important efficiency metric for high efficiency power amplifiers as they are driven in the saturation region and require an evaluation of the total power added by the amplifier circuit. The relationship for PAE has been expressed in Eq. 3.8 [45].

$$\text{Power added efficiency} = PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta_D\left(1 - \frac{1}{G}\right) \tag{3.8}$$

The expression for PAE defines an important relationship between PAE, gain and drain efficiency. Drain efficiency increases linearly with input power until the amplifier has reached saturation, however, GaN devices depict gain expansion in the linear region. At this point, PAE of the amplifier becomes maximum. Within the saturation region, PAE decreases because there is no further addition of power by the amplifier with an increase in the input power. At some point P_{out} and P_{in} might become equal, making their difference zero. Thus, the PAE of an amplifier may attain zero or negative values [42].

3.2.6 Load Pull Analysis

An important aspect of large signal modelling is the determination of optimum source and load impedances to achieve specified high power or high efficiency performance by developing a relationship between maximum linear power and 1 dB or 2 dB compression points. Cripps (2006) is considered as the pioneer in load pull systems and states that the concept of load pull defines a functional relationship between output power and output match [41]. The determination of source and load impedances is performed by means of source and load pull techniques, in which various complex source and load conditions are provided to the transistor (ideally at the terminal reference planes) to determine optimal loading conditions. Various parameters may be determined either my means of CAD based software utilities or hardware-based load pull systems. These include drain or power added efficiency, output power, power gain, etc. of the transistor.

During literature review, a report on evaluation of GaN HEMT transistors on the Triquint 0.25 µm GaN on SiC 3MI process with 100 mm wafer size performed at the University of Manchester (UoM) in collaboration with Filtronic Broadband Limited, was reviewed by the author of this thesis. In this study, load pull measurements were undertaken at the UoM to ascertain the maximum power output from the GaN devices over the required frequency bands of 6-8 GHz, 13-15 GHz and 23 GHz. Large signal measurements were carried out using Maury Microwave slide screw tuners (type no. 8045P) connected to the input and output on-wafer probes. A high power GSG Picoprobe was employed on the drain terminal of the device and a Mini-circuits high power amplifier (ZVE-3W-183+) was used to drive the gate terminal. The input and output screw tuners were adjusted for maximum power output at various drive levels and the tuner positions were noted. Then, the tuners were reset, and their impedances were measured using 8510XF and 8510C VNAs. The load-pull measurement setup has been shown in Fig. 3. 11.

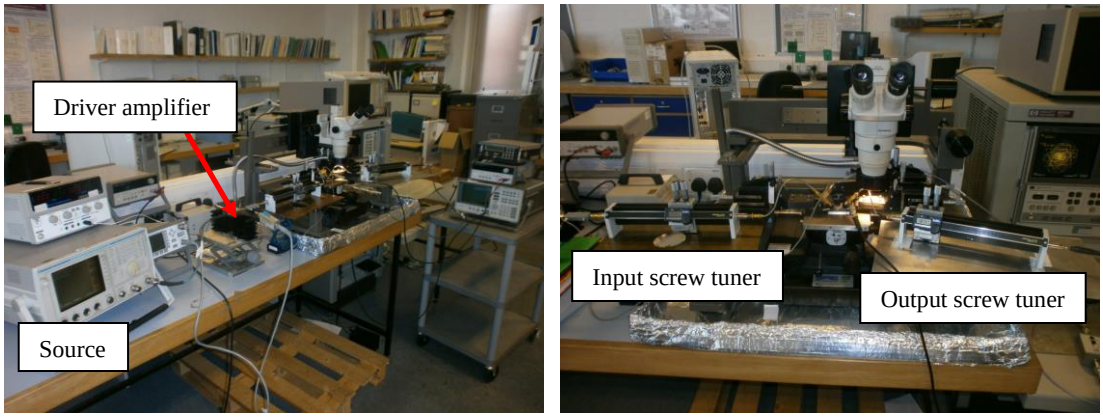


Fig. 3. 11: Load pull measurement setup

A drawback experienced during these load pull measurements was the restriction of VSWR matching range (and restricted impedances on the Smith chart) of the tuners, due to the necessary length of the transmission line between screw tuner and gate and drain of the transistors (including the probes). Thus, matching circuits were employed for mounting close to the DUT to bring the required match to 10 Ω, with the view that the input and output tuners would be able to accommodate with the necessary cables and probes. The impedances were measured and corrected for device terminal's reference planes. The results from this study for 12x125 µm GaN HEMT transistor were utilised by the author of this thesis to write a review paper (annexed as A) on an integrated applicator structure achieving enough power distribution density to cause coagulation in the human tissue. De-embedded s-parameter and large signal measurements have been shown in Fig. 3. 12, while the corrected impedances (at device terminals) to give maximum output power at 6 GHz have been shown in Fig. 3. 13.

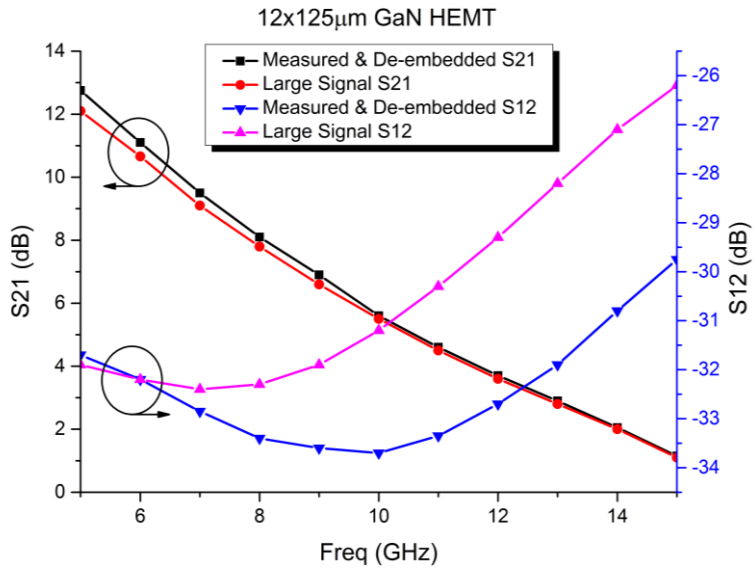


Fig. 3. 12: Measured S_{21} and S_{12} for 12x125 µm GaN HEMT device

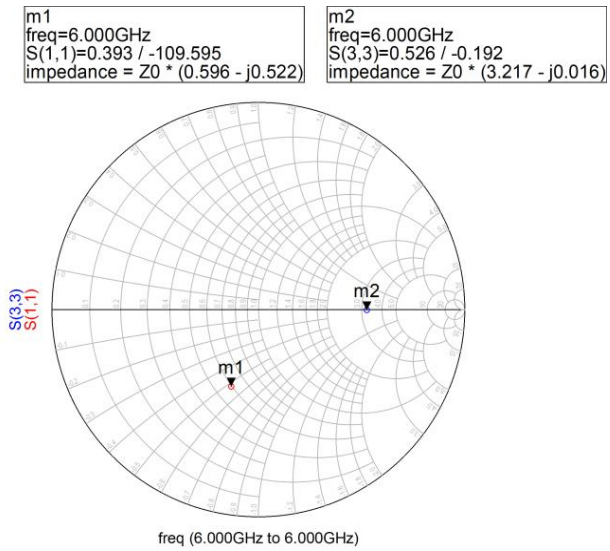


Fig. 3. 13: Input (m1) and output (m2) impedance for 12x125 µm GaN HEMT at 6 GHz

The input and output impedances (shown in Fig. 3. 13 by markers m1 and m2) for 12x125 µm GaN HEMT from 6 to 14 GHz are $Z_{in} = 29.8 - j26.1\ \Omega$ and $Z_{out} = 160.85 - j0.8\ \Omega$, respectively. These results were obtained in the linear and compressed input power levels and utilised to design the respective input and output matching networks for maximum output power performance of the device using Keysight's ADS. The input matching network includes: a shunt stub in series with a very small length of a transmission line, while, the output matching network is a series quarter wavelength transmission line. These networks provide a match to 50 Ω and were designed by the author of this thesis on RT Duroid 5870 laminates. Fig. 3. 14 shows maximum power output of the 12x125 µm device for the given input power at the stated frequencies of 6, 7 and 8 GHz with the measured matching networks.

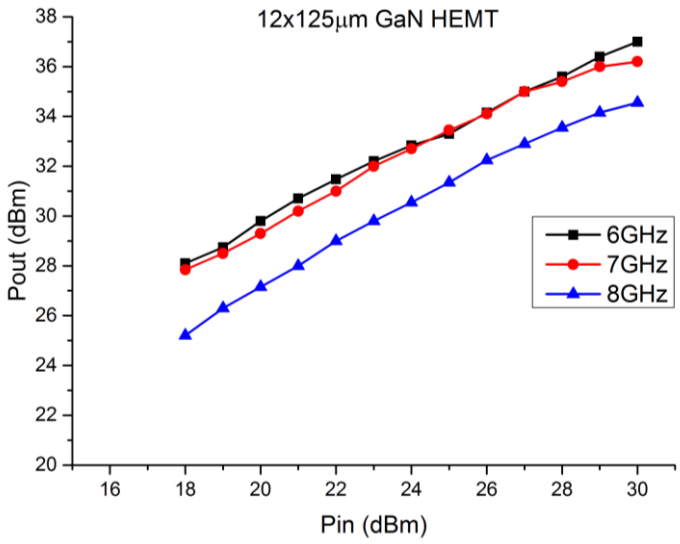


Fig. 3. 14: Pout versus Pin for 12x125 m GaN HEMT device

The PA designed with impedances shown in Fig. 3. 13 provided 37% PAE at 1 dB gain compression for $P_{in} = 30$ dBm and the study helped to realise the significance of load pull measurements in the design of power amplifiers to achieve specified power and PAE. However, large signal models for both discrete transistors and those available through MMIC process design kits have been much improved and can be utilised in software packages like Keysight's ADS to very accurately perform load pull analysis. Fig. 3. 15 shows the output of software-based load pull simulation performed using WIN PP10-10 pdk in Keysight's ADS for a 4x100 µm GaAs HEMT device at 5.8 GHz, to determine optimum load impedance for high PAE performance. The utility takes into consideration bias conditions, input power drive level, and the specified gain compression level.

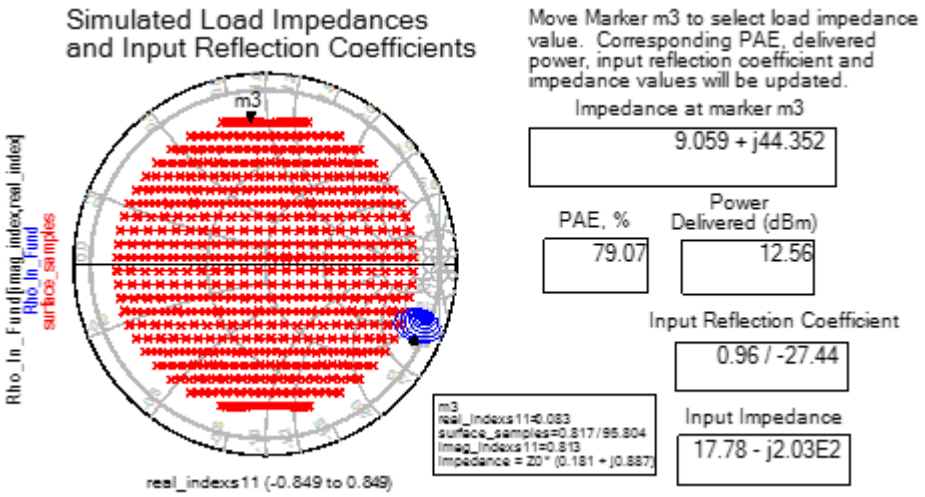


Fig. 3. 15: Output of load pull simulation in Keysight's ADS to determine optimum load impedance for high PAE performance

3.3 Classification of Amplifiers

This section presents brief overview of different classes of amplifiers based on the transistor's region of operation in the transfer characteristics, bias conditions, conduction angle and the input power level from the perspective of output power and efficiency. However, detailed review of amplifiers and oscillator that have been discussed in Chapter 4, 6 and 7 will be presented in the following sections, respectively.

3.3.1 Transconductance Amplifiers

Transconductance amplifiers are the simplest types of amplifiers that act as a voltage controlled current source. These are generally designed using the topology shown in Fig. 3. 16. The FET is provided an input drive signal through the gate terminal and the drain acts as a current source that feeds current to the termination network (or filter) through the transistor's drain terminal [42].

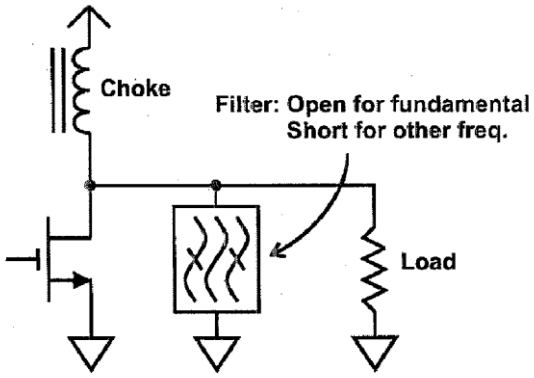


Fig. 3. 16: Basic circuit topology of transconductance amplifiers [42]

Load termination network is designed to provide high or open circuit impedance at the fundamental frequency and short circuit impedance at harmonic frequencies. This effectively makes voltage at the output terminal of the transistor sinusoidal in nature, irrespective of current waveform driven through the transistor. This concept is very important to achieve variable performance from the transistor by varying the current waveform and always finding a sinusoidal voltage waveform at the output. Some classes of transconductance amplifiers are explained next, these include Class A, Class AB, Class B and Class C amplifiers. Fig. 3. 17 illustrates the relationship between RF power, conduction angle, and efficiency for different classes of transconductance amplifiers. The fundamental RF output power remains similar for class A, AB and C amplifiers and reduces considerably for class C amplifiers. However, the efficiency improves nearly in a linear manner as we move from class A towards class C amplifiers.

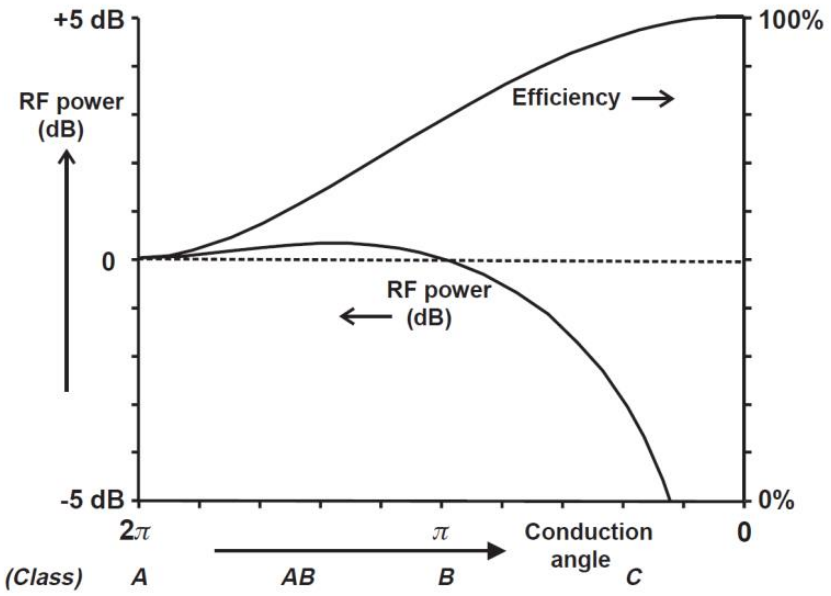


Fig. 3. 17: RF Power and amplifier efficiency as a function of conduction angle for transconductance amplifiers [68]

Class A Amplifiers

Class A amplifiers are the most widely used linear amplifiers in which the transistor conducts current at all times. Transistor is such biased so as to keep voltage waveform within the transconductance region, without swinging into breakdown or triode region. IV-waveforms, and load line for class A amplifiers have been shown in Fig. 3. 18 [42].

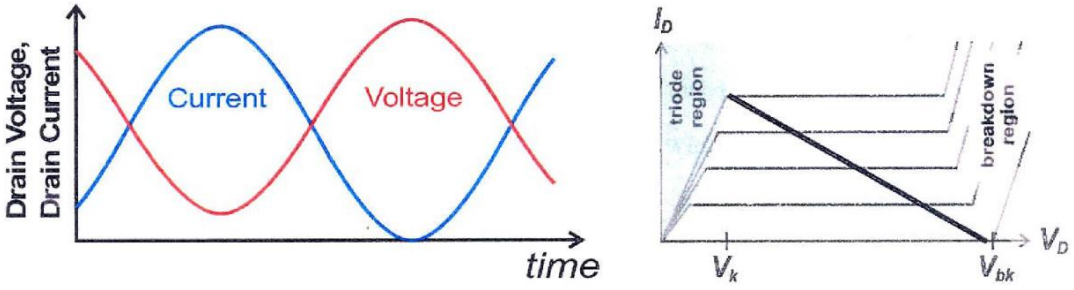


Fig. 3. 18: IV waveforms and loadline for class A amplifiers [41], [42]

Since transistor is always ON and conducting, thus, the conduction angle is 360^o. IV-waveforms of class A amplifiers and the relationship for drain efficiency can be mathematically represented by Eq. 3.9, 3.10 and 3.11, respectively [42].

$$V_D = \left(\frac{V_{bk} + V_k}{2}\right) - \left(\frac{V_{bk} - V_k}{2}\right) sin(\omega t) \tag{3.9}$$

$$I_D = I_{DD} \cdot (1 + sin(\omega t)) \tag{3.10}$$

$$\eta_D = \frac{P_{out}}{P_{DC}} = \frac{1}{2} \cdot \left[\frac{1 - {V_k}/{V_{bk}}}{1 + {V_k}/{V_{bk}}}\right] \tag{3.11}$$

Class A amplifiers may have a maximum theoretical efficiency of 50% depending on their conduction angle of: 360^o. However, the efficiency of transconductance amplifiers may be improved by reducing the conduction angle.

Class AB, Class B and Class C Amplifiers

Class AB, class B and class C are reduced conduction angle (α expressed below) transconductance amplifiers that are biased closer to the knee region to provide improved efficiency. Bias conditions effectively change the respective current waveforms which results in the clipping of the waveform.

$$180^o < \alpha < 360^o \quad (Class\ AB)$$

$$\alpha = 180^o \quad (Class\ B)$$

$$\alpha < 180^o \quad (Class\ C)$$

Fig. 3. 19 shows the effect of reduced conduction angle on gate voltage, drain current and drain voltage for a typical transconductance amplifier.

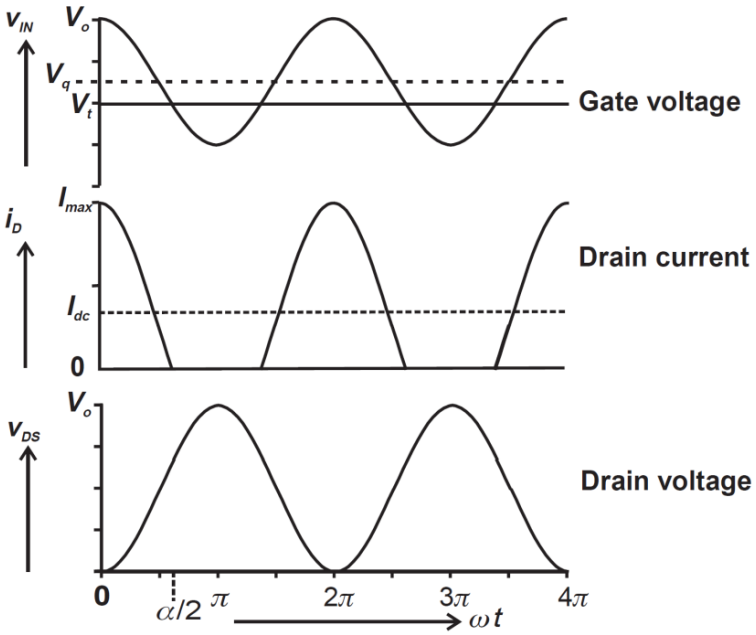


Fig. 3. 19: Waveforms for a typical reduced conduction angle transconductance amplifier [41]

Current in class B amplifiers only flows during half a cycle, thus a waveform similar to that shown in Fig. 3. 20 is achieved. For class AB amplifiers, current flows during a slightly longer duration compared to class B amplifiers as shown in Fig. 3. 21. However, for class C amplifiers the conduction of current is during the least duration as shown in Fig. 3. 22. The voltage waveform remains sinusoidal for all three cases.

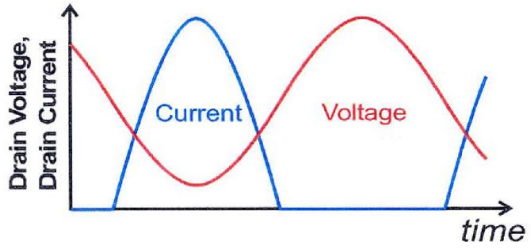


Fig. 3. 20: *IV* waveforms for class B amplifiers [42]

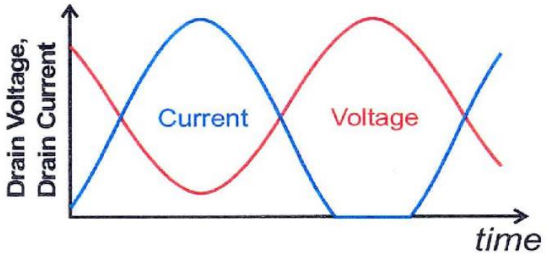


Fig. 3. 21: *IV* waveforms for class AB amplifiers [42]

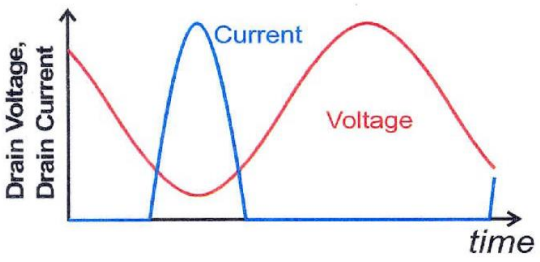


Fig. 3. 22: *IV* waveforms for class C amplifiers [42]

During periods of no conduction, the transistor acts as an open circuit making the current equal to zero. However, the voltage waveform has positive (and maximum) values during these periods. Thus, the product of voltage and current achieves a low value resulting in an enhanced efficiency due to low DC power consumption. By analysing the load lines for these type of reduced conduction angle transconductance amplifiers, it can be inferred that the device spends more time closer to the knee region, consuming less power. Least DC power is consumed by Class C amplifiers as the channel is closed for most of the duration. Though these amplifiers provide an improved efficiency but at the cost of reduced gain because the drain is biased at a lower voltage V_{DS} closer to the knee voltage. Expressions for amplifier efficiency and output power applicable to class AB, class B and class C amplifiers have been given in Eq. 3.12 and 3.13, respectively [42].

$$\eta_D = \frac{P_{out}}{P_{DC}} = \frac{1}{2} \cdot \left[\frac{1 - {V_k}/{V_{bk}}}{1 + {V_k}/{V_{bk}}}\right] \cdot \left[\frac{\alpha - \sin\alpha}{2sin\left(\frac{\alpha}{2}\right) - \Theta\cos\left(\frac{\alpha}{2}\right)}\right] \tag{3.12}$$

$$P_{out} = \frac{1}{8\pi} \cdot \left[1 - {V_k}/{V_{bk}}\right] \cdot \left[\frac{\Theta - \sin\alpha}{1 - \cos\left(\frac{\alpha}{2}\right)}\right] \tag{3.13}$$

Effect of DC Bias on Transconductance Amplifier Performance

As discussed earlier that bias voltages applied at drain and gate terminals play an important role in defining the conduction angle. The relationship between bias conditions and performance of amplifiers in terms of gain, noise performance, linearity and efficiency has been illustrated in Fig. 3. 23. Point I represent low noise amplifier bias conditions, the amplifiers depict decent noise performance due to low drain current I_{dss} and reduced DC power consumption. However, the issue with such a biasing is the limited power handling capability as the device is biased close to the knee or pinch off region. Point II represents amplifiers that may be designed to provide high values of small signal gain because the channel is widely open. However, transistors consume high DC power and show poor noise performance when biased at these conditions. Amplifiers can be

made to operate with high linearity at point III and most class A amplifiers are biased at these conditions. Point IV represents high efficiency operation. Though the amplifiers have reduced gain and poor linearity under these conditions, but they provide very high efficiency performance with low DC power consumption. Class AB amplifiers are generally biased at point IV [29].

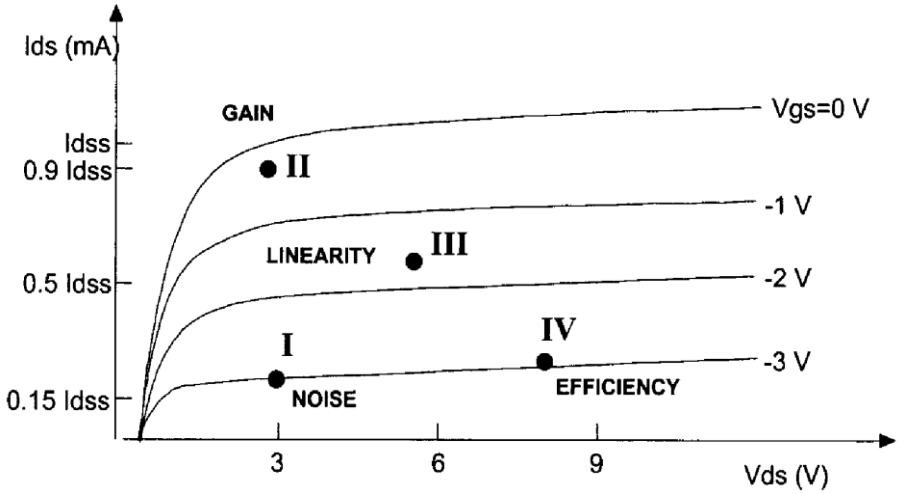


Fig. 3. 23: Relationship between bias conditions and amplifier linearity, gain, efficiency and noise performance [29]

Saturated Transconductance Amplifiers

Saturated transconductance amplifiers are biased close to the knee region. When driven with high enough input power level, voltage waveforms swings into the knee region, which is called hard driven or over driven condition. Since the load termination networks tend to maintain sinusoidal nature of the voltage waveform, the current waveform will start to distort while voltage waveform is in the knee region due to current reductions. This generally results in the clipping of the current waveform (distortion) with some useful effects like: increase in output power and slight overall increase in efficiency [42]. These amplifiers are not very popular because of the very limited advantages they present over transconductance amplifiers and because of saturated amplifiers discussed in the succeeding sections. A typical voltage and current waveform for class B overdriven amplifier has been shown in Fig. 3. 24.

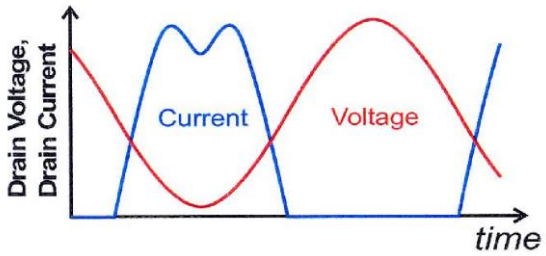


Fig. 3. 24: *IV* waveforms of a typical overdriven Class B amplifier [42]

3.4 High Efficiency Saturated Power Amplifiers

This section presents review on high efficiency power amplifiers with consideration of various fundamental concepts like waveform engineering, harmonic tuning networks, high efficiency operation, harmonic load/source pull, stabilisation of amplifiers, biasing considerations, effect of oscillations and non-linearities, gain enhancement techniques and limitations.

3.4.1 Class F Amplifiers

Class F amplifiers are saturated amplifiers that provide very high efficiency and output power by means of harmonic tuning networks that terminate the active transistor device and perform waveform engineering. Fundamental limitation of transconductance amplifiers is that the voltage waveform is required to be kept purely sinusoidal, while the current waveform is shaped differently (conducting for less than a cycle) by changing the bias conditions. However, if both the waveforms are engineered such that the product of voltage and current remains very low (or effectively zero) during most of the transistor's operation, then much higher values of efficiency may be attained.

3.4.2 Waveform Engineering

An important aspect for the design of class F amplifiers is 'waveform engineering' that mainly involves shaping the voltage waveform as a square wave by utilising harmonic tuning networks. This transformation from pure sinusoid to square waves can be explained through the differences between the two in terms of their Fourier analysis or the spectrum. A pure sinusoidal wave has only got fundamental harmonic component in its spectrum; while, a square wave is combination of fundamental and higher order odd harmonic products. Fig. 3. 25 shows time domain and Fourier domain representations of a square wave. A square wave is a collection of fundamental component and higher order odd harmonic components with its flatness depending upon the number of higher order harmonics added. However, the significance of higher order harmonics beyond the 5th harmonic is minimal because of their contribution towards the waveform.

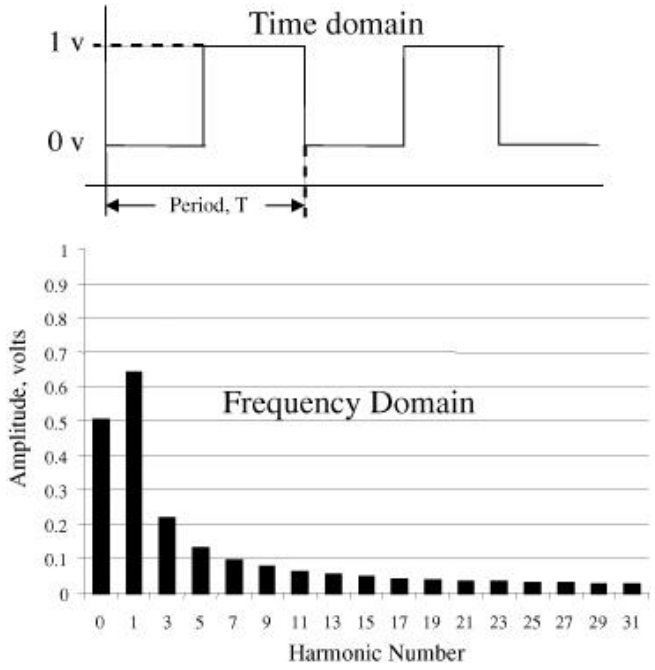


Fig. 3. 25: Time domain and frequency domain representation of a square wave [47]

Analysis of a sinusoidal wave presented by Cripps (2006) in [41] has been shown in Fig. 3. 26. Up to the third harmonic products have been added to the sinusoidal wave to change its shape. Variation in terms of the amplitude of the third harmonic component has been shown.

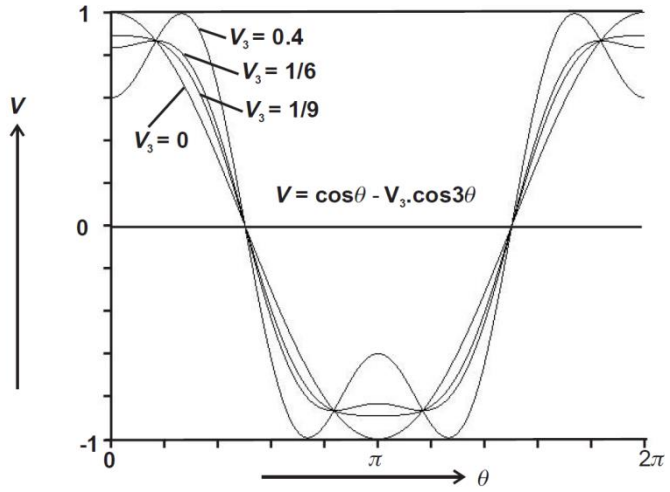


Fig. 3. 26: Effect of adding third harmonic to a sinusoidal waveform [41]

The waveforms shown in Fig. 3. 26 can be mathematically expressed as Eq. 3.14 [41].

$$v(\theta) = V_1 \cdot \cos(\theta) - V_3 \cdot \cos(3\theta) \tag{3.14}$$

Third harmonic components once added to the fundamental component in phase, reduce peak to peak swing of the resultant waveform. If they are added in the correct ratio or amplitude compared to the fundamental, a maximally flat waveform can be engineered with the amplitude of the fundamental component being greater than the peak to peak

swing. A single maximally flat peak with a magnitude of $V_{pk} = (V_1 - V_3)$ is achieved in the waveform if the ratio $\frac{V_3}{V_1} < \frac{1}{9}$ is maintained. Any values beyond this ratio will result in distortion of the waveform accompanied by double or multiple peaks and an increase in the peak to peak swing. Double peaks will continue to reduce until: $\frac{V_3}{V_1} = \frac{1}{6}$, at which the minimum peak value, $V_{pk} = \frac{\sqrt{3}}{2} V_1$. Thus, peak voltage should be kept lower less than V_1 by a factor of 'k', where k may have a minimum value: $k = \frac{\sqrt{3}}{2}$. If V_3 in controlled within the range defined in Eq. 3.15 (a), conditions for peak voltage can be maintained. The relationship between peak voltage, third harmonic component and efficiency have been illustrated by Cripps (2006) in [41], the graph has been reproduced in Fig. 3. 27.

$$v(\theta) = V_1 \cdot \cos(\theta) - V_3 \cdot \cos(3\theta)$$

$$0 < V_3 < \frac{V_1}{2.5} \qquad (3.15\ a)$$

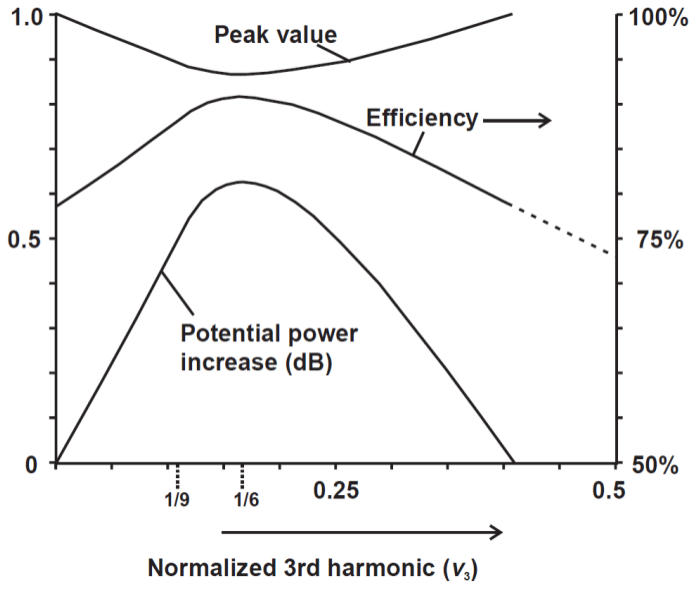


Fig. 3. 27: Relationship between peak voltage, efficiency and the amplitude of third harmonic components [41]

Waveform engineering in class F amplifiers significantly helps to increase efficiency of the amplifier. Besides this, an increase in output power is also achieved due to an increase in the amplitude of fundamental component. Due to the addition of third harmonic component to the waveform, an increase in the fundamental takes place according to Eq. 3.15 (b) defined by Cripps (2006) in [41].

$$V_1 = \frac{V_{max}}{k} \qquad (3.15\ b)$$

Where, V_{max} is the maximum amplitude for peak to peak swing limited by the conditions defined in succeeding discussion. For the optimum case where, $\frac{V_3}{V_1} = \frac{1}{6}$, the value of $k = \frac{\sqrt{3}}{2}$, an increase in the fundamental power by $\frac{2}{\sqrt{3}}$ or 0.6 dB will be observed. Cripps (2006) indicates that waveform engineering discussed in above discussion will result in an increase in the efficiency to 90.7 %. On the other side, maximally flat waveform will have $k = \frac{8}{9}$ or an increase in the fundamental power by 0.5 dB with 88.4 % efficiency [41]. Current and voltage waveforms for the maximally flat case of class F amplifier have been shown in Fig. 3. 28.

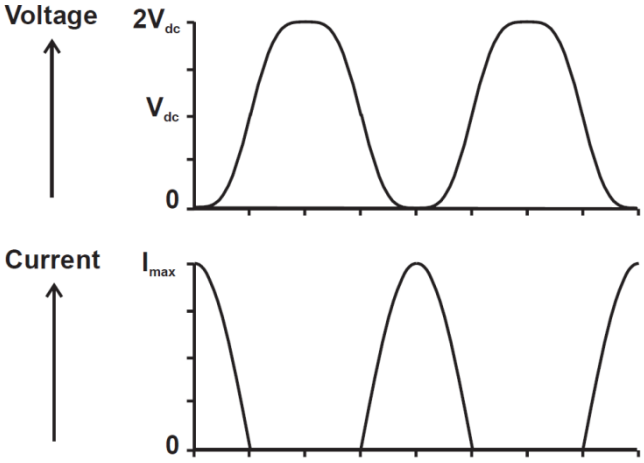


Fig. 3. 28: Maximally flat waveforms for class F amplifier [41]

Addition of odd harmonics beyond the third harmonic could improve the waveform and provide higher efficiency and output power. However, as we move towards higher order harmonics, their contribution towards the square waveform reduces with an associated significant increase in complexity of the circuit. Eq. 3.16 shows generalized form of a normalized composite waveform made by adding fundamental component with odd harmonic components. Negative sign with harmonic components indicate the requirement for an inverted voltage waveform assuming that the current wave is a half rectified waveform [41].

$$v(\theta) = 1 - v_1\, sin(\theta) - v_3 sin(3\theta) - v_3 sin(5\theta) + \cdots \quad (3.16)$$

The effect of adding higher order components to the composite waveform is illustrated in Fig. 3. 29. Considering up to fifth harmonic components, optimum value for $V_1$is given by: $V_1 = \frac{1+\sqrt{2}}{2}$. This increases the efficiency to ~94.8 % by a factor of $\frac{1+\sqrt{2}}{2}$ [41].

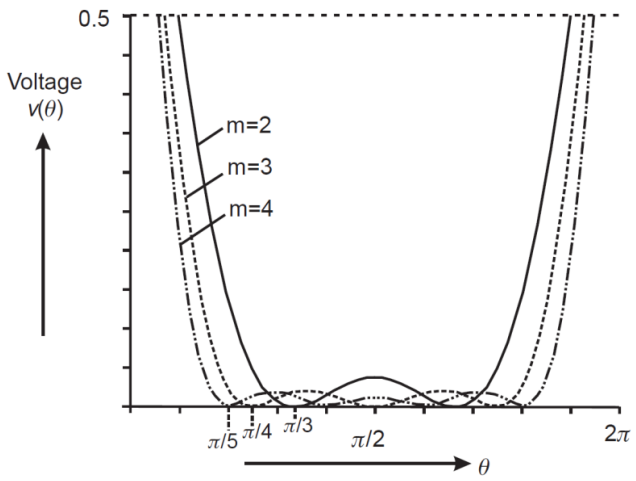


Fig. 3. 29: Composite voltage waveform with 3rd, 5th and 7th order harmonics [41]

Furthermore, consideration of fundamental and odd harmonics up to the seventh harmonic component will result in an increase in the efficiency to about 96.7 %. Thus, in the limit where the number of higher order odd harmonics tend to infinity, a perfectly shaped square voltage waveform similar to that shown in Fig. 3. 25 will be obtained and the amplifier will have an efficiency of 100 %. For this particular case of a square voltage waveform, the fundamental voltage component V_1 will have a value of: $V_1 = \frac{4}{\pi} \cdot V_{DC}$, indicating an increase of $\frac{4}{\pi}$ or 1 dB compared to a class B amplifier under similar bias conditions [41].

3.4.3 Generation of Third Order Current Harmonics

When the transistor is biased at the threshold between the knee and transconductance regions, peaks of the current waveform may be clipped because of the swing into the knee region. Clipping of the peak results in substantial generation of third order odd harmonics of the current. Fig. 3. 30 shows comparison between current waveforms with and without considering knee effects for a class F amplifier biased near the threshold region [41], [46].

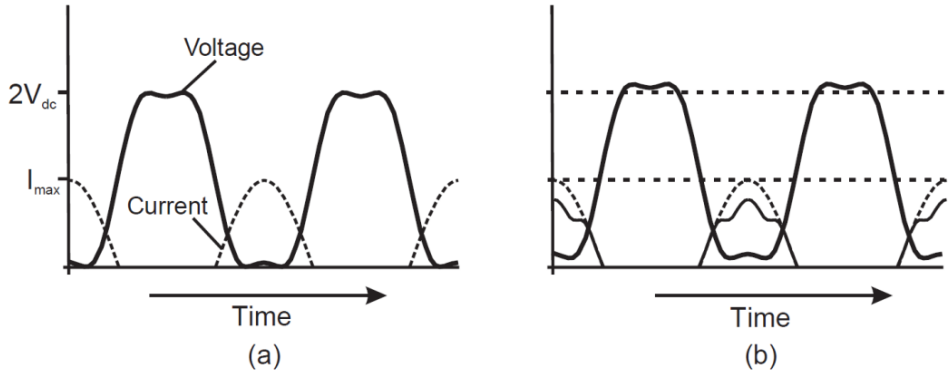


Fig. 3. 30: *IV* waveforms of a typical Class F Amplifier, (a) without the effects of knee region, (b) with the clipping effect of knee region on the current waveform [41]

Thus, odd harmonics of both current and voltage will be generated by: 1) biasing the transistor near the threshold between knee and transconductance regions and considering that the knee effects clip peak of the current waveform; and 2) by terminating the transistor into impedances tuned for odd harmonic components (open circuit), respectively.

3.4.4 Significance of Open Circuit Termination for Odd Harmonics

Ideally, fundamental harmonic components are required to be terminated in a resistive load. However, ideal termination for odd harmonics must be defined. Cripps (2006) presents a methodology to determine values of termination impedances for fundamental and third harmonic components for the required voltage and current waveforms. Considering the voltage and current waveforms for class F amplifier with knee effects, it can be observed that: 1) voltage wave has a maximum value when the current is zero, 2) voltage wave has a very low value during conduction cycle of the current wave. The output voltage waveform given in Eq. 3.16 can be re-written as Eq. 3.17 [41].

$$V_0 = V_{DC} - V_1 \cdot \sin(\theta) - V_3 \cdot \sin(3\theta) \tag{3.17}$$

Similarly, drain current can be written by considering the knee effects as Eq. 3.18 [41].

$$\begin{aligned} i_{dc} = v_{in} \cdot I_{max} & \\ \cdot \left[\frac{1}{\pi} + \frac{1}{2}\sin(\theta) - \frac{2}{3\pi}\cos(\theta) - \frac{2}{15\pi}\cos(4\theta)\right. & \\ \left. - \frac{2}{35\pi}\cos(6\theta)\right] \cdot [V_{DC} - V_1 \cdot \sin(\theta) - V_3 \cdot \sin(3\theta)] & \end{aligned} \tag{3.18}$$

Third harmonic current and voltage components can be related with each other through Eq. 3.19 where the coefficients have been normalized to the DC bias V_{DC} [41].

$$\begin{aligned} I_3 = v_{in} \cdot I_{max} \left[-\frac{v_3}{\pi}\sin(3\theta) + \frac{v_1}{3\pi}\sin(3\theta) - \frac{v_1}{15\pi}\sin(3\theta)\right. & \\ \left. - \frac{v_3}{70\pi}\sin(3\theta)\right] & \end{aligned} \tag{3.19}$$

At maximum drive level, normalised input voltage $v_{in} = 1$ and maximum current under this condition also normalises to: $I_{max} = 1$. Eq. 3.20 is the expression derived by Cripps (2006) to show the dependence of third harmonic component on the impedance (R_3) that is presented by the termination network to it [41].

$$\frac{v_3}{v_1} \approx \frac{4}{15\left[1 + \frac{\pi}{R_3}\right]} \tag{3.20}$$

Very weak dependence of the third harmonic component on the impedance R_3 can be inferred from Eq. 3.20. Thus, open circuit termination for third order harmonics provides optimum efficiency to the amplifier [41].

3.4.5 Wideband Continuous Class F Mode of Operation

Continuous class F mode allows wideband operation with similar high efficiency and output power characteristics by providing reactive fundamental and even harmonic terminations. Open circuit condition for odd harmonics remains unchanged and fundamental impedance loci can be supported with a variable reactive component. High efficiency performance of continuous class F mode can be maintained by keeping the voltage level above zero by varying reactive parts of fundamental and second harmonic (changing its phase). Thus, larger design space for the realization of passive networks, providing greater relative bandwidth than conventional design is achieved [47]. An operator defined in Eq. 3.24 is multiplied either with voltage or current waveform to change the waveform [48]. Fig. 3. 31 shows the extended set of voltage waveforms.

$$h(t) = (1 - \alpha\, cos(\beta\omega t)) \qquad -1 \leq \alpha \leq 1 \tag{3.24}$$

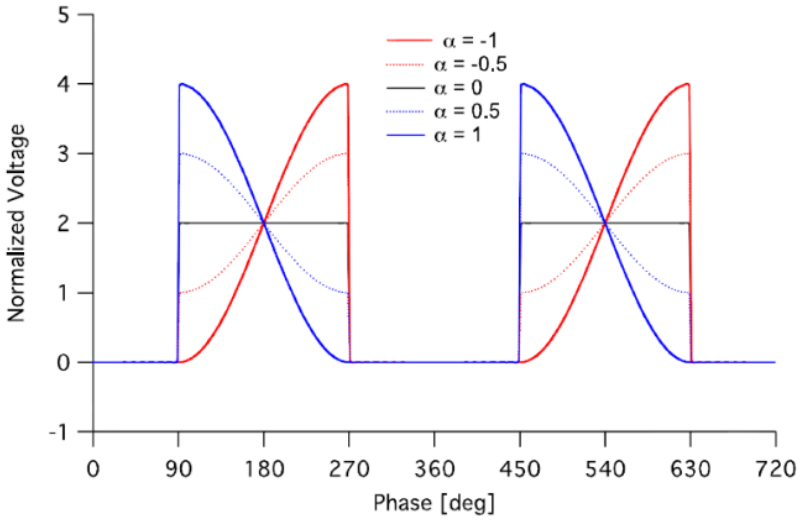


Fig. 3. 31: Normalised Voltage Waveforms Set for Continuous Class F Mode of Operation [52]

The transformation of voltage or current waveform results in the creation of a new set of waveforms having the same DC level and fundamental component. However, continuous mode of operation may be supported by transistors having high breakdown fields due to an increase in the maximum voltage swing. As opposed to Eq. 3.21-3.23, the impedance space for continuous class F mode has been defined in Eq. 3.25-3.27 [48].

$$Z_1 = \frac{2V_{DC}}{I_{max}}\left(\frac{4}{\pi} + j\alpha\right) = R_{opt}\frac{4}{\pi}\left(1 + j\frac{\pi}{4}\alpha\right) \tag{3.25}$$

$$Z_{2r} = \frac{2V_{DC}}{I_{max}}(-j2\alpha r) = R_{opt}\frac{4}{\pi}\left(-j\frac{\pi}{2}\alpha r\right) \tag{3.26}$$

$$Z_{2r=1} = \infty \tag{3.27}$$

Comparison between design spaces of continuous class F amplifier and traditional class F amplifier has been shown in Fig. 3. 32. Circles show impedance termination points for traditional class F amplifiers, while heavy lines show extended design space for reactive second harmonic and fundamental components for continuous class F amplifiers. γ is the variable that extends the design space for harmonic termination impedances [47], [49].

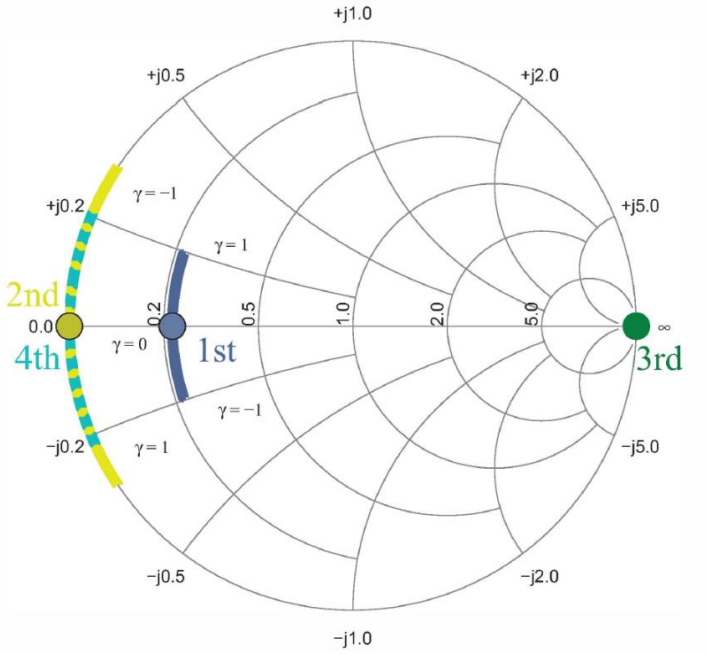


Fig. 3. 32: Comparison between the harmonic network design spaces for traditional and continuous mode class F amplifiers [54]

3.4.8 Inverse Class F Amplifier

Inverse class F amplifiers are similar to class F amplifiers in the sense that both of them require open and short circuit terminations for higher order harmonic components to make the current and voltage product zero at all harmonic frequencies except the fundamental. However, in inverse class F amplifiers, even harmonics are provided open circuit terminations while odd harmonics are provided short circuit terminations. Also, the current and voltage waveforms are square and half-rectified sinusoidal, respectively. Optimum load termination impedances to be presented to fundamental and higher order terminations are given by Eq. 3.28-3.30 [50].

$$Z_{net}(\omega_o) = R = \frac{\pi^2}{8}\frac{I_D}{V_{DC}} \tag{3.28}$$

$$Z_{net}(2n\omega_o) = \infty \tag{3.29}$$

$$Z_{net}((2n+1)\omega_o) = 0 \tag{3.30}$$

Fig. 3. 33 show the comparison between voltage and current waveforms for class F and inverse class F amplifiers.

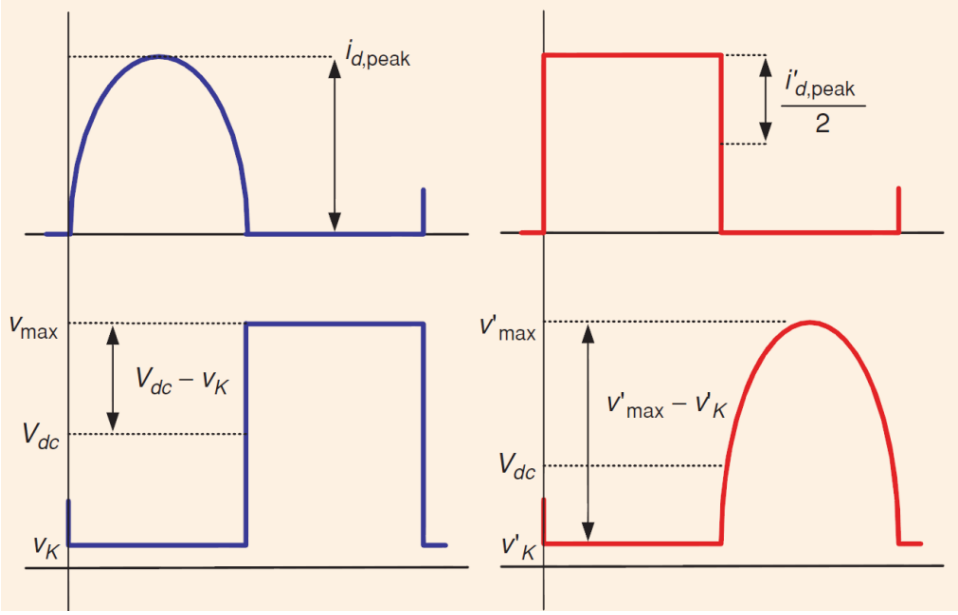


Fig. 3. 33: Comparison between the voltage and current waveforms of class F and inverse class F amplifiers (left to right respectively) [68]

Load termination networks of inverse class F amplifiers take the generalised form shown in Fig. 3. 34.

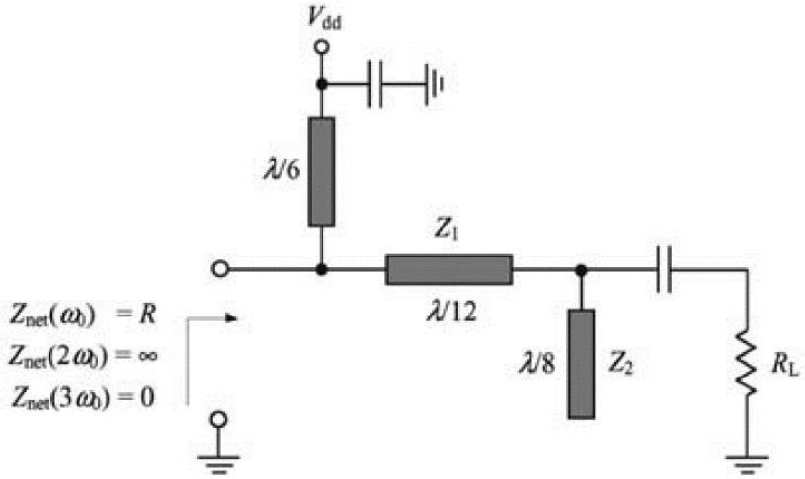


Fig. 3. 34: Ideal harmonic tuning network for inverse class F amplifiers [48]

In Fig. 3. 34, shunt λ/6 impedance provides very low (effectively short circuit) impedance to the third harmonic and combines with the series combination of λ/12 transmission line and λ/8 open circuit stub to provide impedance peak (effectively open circuit) for the second harmonic. An alternative approach for the harmonic network has been given in

Fig. 3. 35 where an additional λ/8 transmission line may been added to present a more practical approach [51].

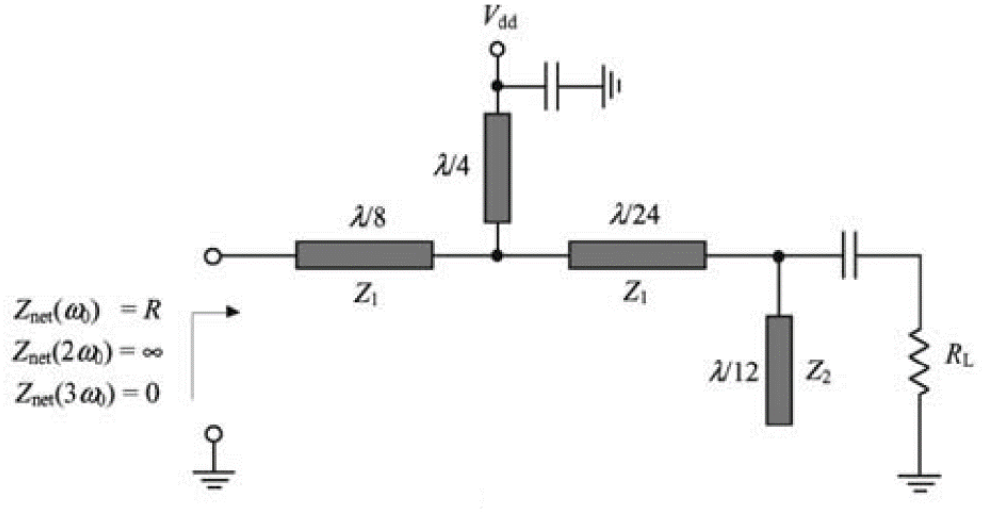


Fig. 3. 35: Alternative harmonic tuning network for inverse class F amplifiers [48]

In the harmonic tuning network shown in Fig. 3. 35, λ/4 shunt transmission line along-with λ/8 series transmission line provides open circuit condition to the second harmonic. While λ/12 open circuited shunt stub along-with the series combination of λ/8 and λ/24 transmission lines provide short circuit termination to the third harmonic [46].

3.4.6 Comparison between Class F and Inverse Class F Amplifiers

Inverse class F amplifiers have shown better performance than conventional class F amplifiers in terms of higher PAE and drain efficiency performance. [52] and [53] show detailed comparison between the two classes of amplifiers and justify that it mainly occurs because of the transistor's on resistance. R_{on}, the transistors on-resistance, represents very small value of resistance experienced by the drain current when the transistor is on. Thus, product of peak current and on-resistance of transistor ($R_{on} \cdot i_{d.peak}$) defines the knee voltage. Efficiencies of class F and inverse class F amplifiers can be defined (Eq. 3.31) in terms of peak drain current, on-resistance and DC bias voltage provided to the transistor [52], [53].

$$\eta = 100\frac{(V_{dc} - R_{on} \cdot i_{d.peak})}{V_{dc}} \quad (\%) \tag{3.31}$$

The difference in efficiencies of the two amplifiers mainly occurs due to different peak drain current and the knee voltage. Comparison between the efficiencies of class F and inverse class F amplifiers has been shown in Fig. 3. 36. Inverse class F amplifiers show better performance because of higher ratio between V_{peak} and V_{knee} as the values of R_{on} increase to maintain the same fundamental output power [52]. Inoue, et al. (2000) in [54]

suggest that inverse class F amplifiers provide better gain compression and higher load resistance compared to class F amplifiers.

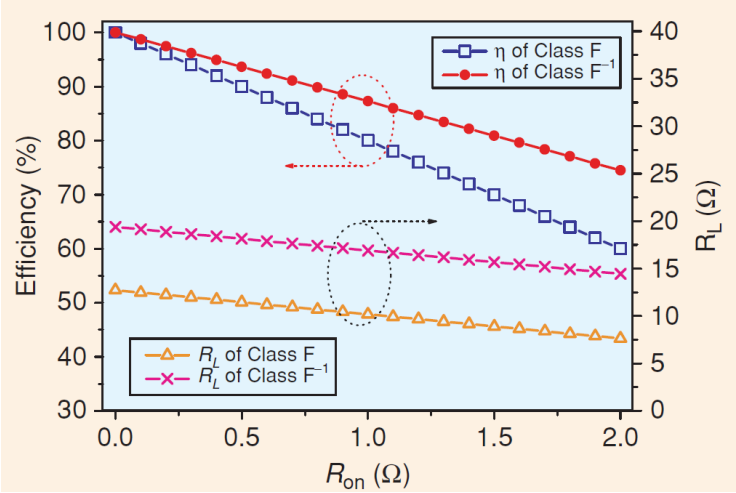


Fig. 3. 36: Comparison between efficiencies of class F and inverse class F amplifiers with increasing values of R_{on}, and typical load resistance R_L [68]

Transistor consume less DC power with an increase in the values of R_{on} for inverse class F compared to class F amplifier configuration, as shown in Fig. 3. 37.

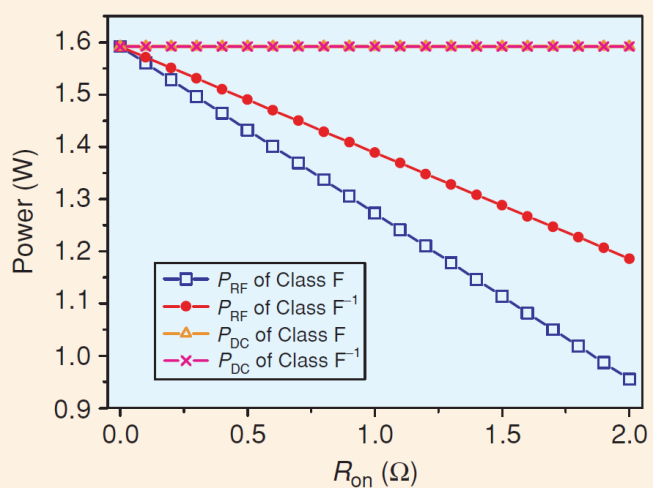


Fig. 3. 37: DC power consumption of class F and inverse class F amplifiers for different values of R_{on} [68]

3.4.7 Distributed High Efficiency Power Amplifiers

Distributed amplifiers are broadband amplifiers with gain distributed over various transistor stages located between artificial transmission lines. Gain-bandwidth product is a limiting factor for broadband amplifiers due to the gate and drain capacitances. However, distributed amplifiers have been highly effective in linear amplification as these capacitances are absorbed in input and output artificial transmission lines. Conventional distributed amplifiers have identical transistor stages terminated onto an optimum output drain line towards the drain side. But this method is not suited for power

amplifiers as optimum load and source impedances for each transistor stage needs to be defined according to large signal simulations and load pull measurements. Besides this, only a small fraction of power output from the drain terminal is combined at the output transmission line [55], [56], and [57]. Non-distributed amplifiers use transistors with different gate-width that are terminated on an optimum drain line determined through non-linear and load pull simulations. These have been presented in [55], [58] and [59]. Basic structure of distributed power amplifier has been shown in Fig. 3. 38 [60].

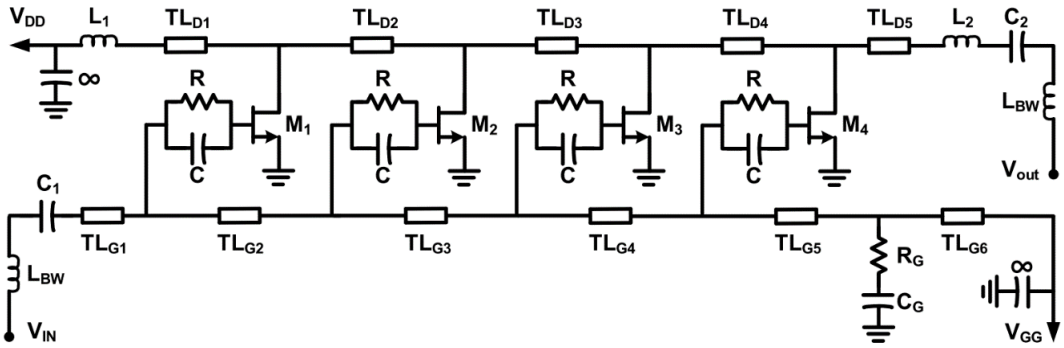


Fig. 3. 38: Basic structure of distributed power amplifier [64]

Distributed configuration of transistors can help in improving bandwidth of the amplifiers, however, chip size become large for power amplifiers with high dc power consumption. Techniques like drain line tapering can be used to improve efficiency, where an up-tapered drain line is used from the first towards the last transistor stage. In addition to up-tapering, length of transmission lines is adjusted to add currents coming out of the transistors in phase. This aid towards terminating all transistor stages with optimum load impedances enabling them to deliver maximum output power [60], [61].

The concept of tapered drain line amplifiers has been implemented on 0.25 µm GaN on SiC Triquint process. The amplifier provides 15 W peak output saturated power with PAE ranging between 20 % to 38 % over an operating bandwidth of 1.5 to 17 GHz. Photograph of the MMIC has been shown in Fig. 3. 39 [61].

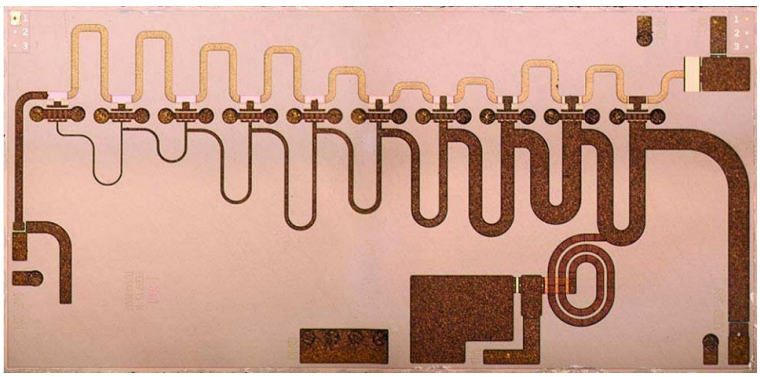


Fig. 3. 39: Distributed power amplifier MMIC with up-tapered drain transmission Line [65]

Distributed configuration has been applied to high efficiency modes like class F and inverse class F. However, harmonic tuning networks are generally narrowband. Architecture for a distributed class F amplifier has been shown in Fig. 3. 40. The amplifier has been designed using two Fujitsu FLK012WF FETs which provide 22 dBm output power with 71 % drain efficiency [62].

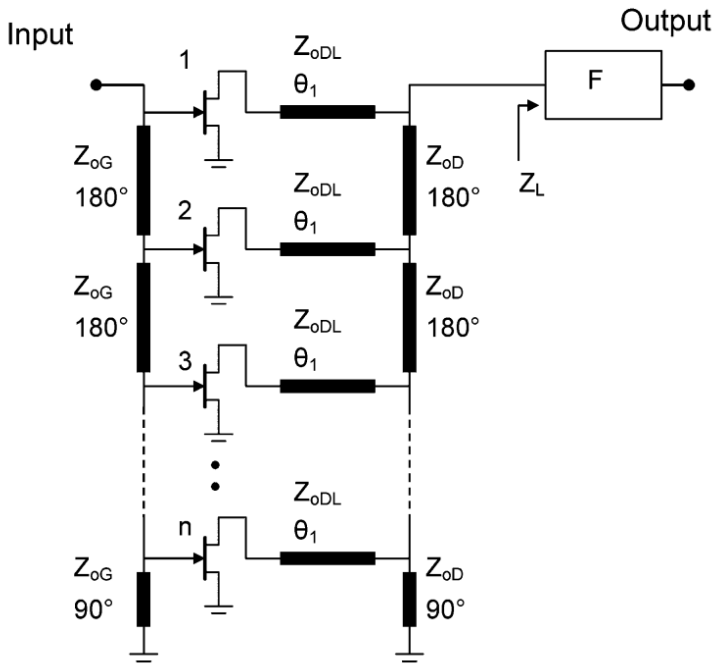


Fig. 3. 40: Distributed class F power amplifier [66]

3.5 High Efficiency Transconductance Power Amplifiers

3.5.1 Introduction

Efficiency requirements for power amplifiers are ever increasing due to power conservation and reduced heat dissipation challenges imposed by various application areas including: mobile phones where the battery has to be conserved, base stations where heating problems are experienced due to low efficiency power amplifiers, and medical

application areas where lossy cables deliver microwave energy to the intended treatment site (for microwave ablation) from large and cumbersome power sources resulting in high heat dissipation (loses) and unintended tissue heating.

3.5.2 Class AB Power Amplifiers

Class AB amplifiers were briefly introduced earlier in this chapter and it was discussed that the current conduction angle lies somewhere between class A and class B amplifiers; and the quiescent bias point somewhere in the middle of class A bias and the knee voltage. This has been shown in Fig. 3. 41.

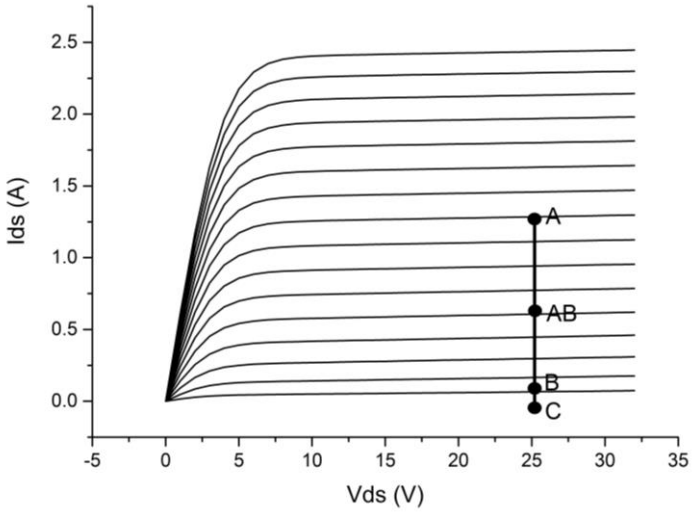


Fig. 3. 41: Quiescent bias conditions of typical class A, class AB, class B and class C amplifiers

Classical class AB amplifier assumes the fundamental load impedance is complex, while harmonic components are terminated into short circuit conditions. The current waveform is made to swing between 0 and I_S by adjusting the input power level. Zero current level corresponds to the swing of input voltage going below cut-off point. Truncated current sine wave consists of high harmonic component, while voltage waveform consists of no harmonic contents. These current and voltage waveforms are maintained through appropriate bias conditions shown in Fig. 3. 41 and termination of higher order harmonics into short circuit conditions. Cripps (2002) presents basic circuit topology shown in Fig. 3. 42 for classical class AB amplifiers where a parallel shunt resonator tuned at the fundamental frequency, comprising of a high value capacitor, provides short circuit conditions to harmonic components while terminating the fundamental frequency component into a resistive load. As a result of this, output voltage at the resistive load would be a sine wave which depends upon the input power level (maximum would cause peak current of I_{max} or I_s) and the resistive load [63].

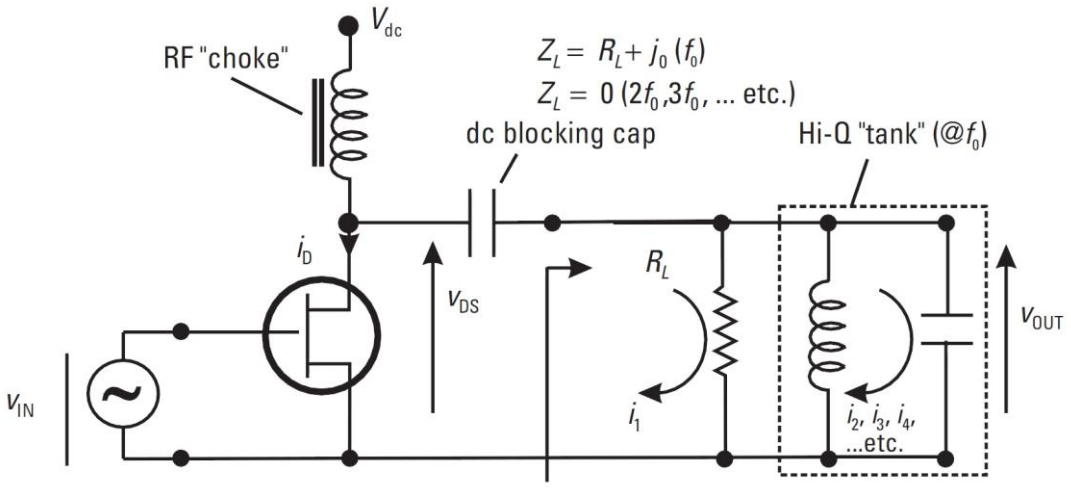


Fig. 3. 42: Circuit topology for classical class AB amplifier [68]

An important relationship discussed by Cripps (2002) in [63] is between quiescent bias point, input drive level and power gain that may be achieved through class AB amplifiers. Classical class AB amplifiers require the input drive level to maintain I_s (or I_{max}), and closer the amplifier is biased to class B conditions (quiescent $I_d = 0$), higher would be the required input drive level to maintain I_{max}. For instance, if the quiescent bias point is moved from class A ($I_{max}/2$) to class B conditions, input power is required to be doubled to maintain the same I_{max} and efficiency, which equates to 6 dB increase of input power and corresponding decrease in power gain. However, the amplifier can be operated at under driven conditions with only 3 dB more input power level than class A conditions; along-with an increase of load resistance at the fundamental frequency by a factor of: $\sqrt{2}$. This way, 1 dB decrease in power gain with the same theoretical efficiency of class B amplifiers, i.e. 78 % is achieved. This case can be extended to class AB amplifiers by operating them with a lower input power level, however, conduction angle increases so the efficiency does not return to the same values of fully-driven conditions [63].

3.5.3 Capacitive Harmonic Termination and Deep class AB/Class J Mode

The design of class B and class AB amplifiers require provision of short circuit termination to harmonic components which comes at the cost of reduced output power levels, linearity and increased complexity of the circuit. However, similar efficiencies can be achieved through capacitive harmonic termination conditions under the same quiescent bias that are practical and provide improved output power levels and linearity [41]. Consider the circuit topology shown in Fig. 3. 43.

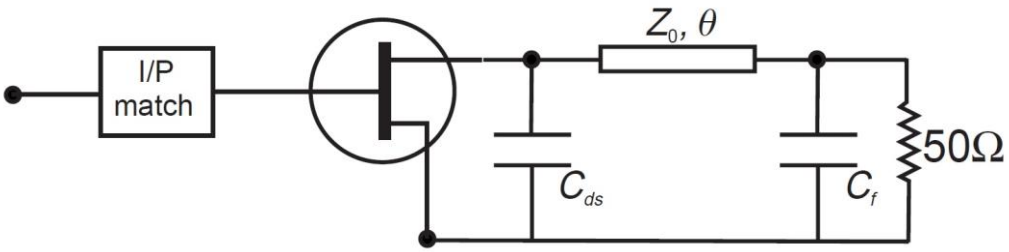


Fig. 3. 43: Circuit topology for class AB amplifier with capacitive harmonic termination network [41]

Shunt capacitance C_{ds} shown in Fig. 3. 43 is output capacitance of the transistor. Large value of this capacitance along-with other elements of the low pass matching network (including the transmission line (Z_0, θ) and shunt capacitance C_f provide short circuit conditions for classical class AB amplifier [41].

However, it should be noted that close to ideal conditions of class AB amplifier require the value of output capacitance C_{ds} to be large and various non-linear models, including WIN MMIC GaAs PP10-15 pdk utilised to design class AB amplifier and class E oscillator presented in this thesis, are overestimated, and thus inaccurately predict behaviour of harmonic components. The ratio between reactance of output capacitance and loadline resistance: X_{Cds}/R_L should be essentially greater than 1 to achieve close to ideal characteristics of class AB amplifier that include: sinusoidal voltage waveform, efficiency and output power [41]. However, in practical design implementations this can be included as quarter wavelength transmission lines in the drain bias network.

If the ratio X_{Cds}/R_L is greater than unity, large reactive component in the fundamental matching network can provide the required conditions for classical class AB amplifier operation. However, this results in altered current and voltage waveforms compared to classical class AB amplifier. Cripps (2006) in [41] presents analysis of the circuit topology shown in Fig. 3. 44. The transistor biased at class B conditions, acts as halfwave sine current source and the fundamental load impedance is assumed to provide short circuit conditions to harmonic components.

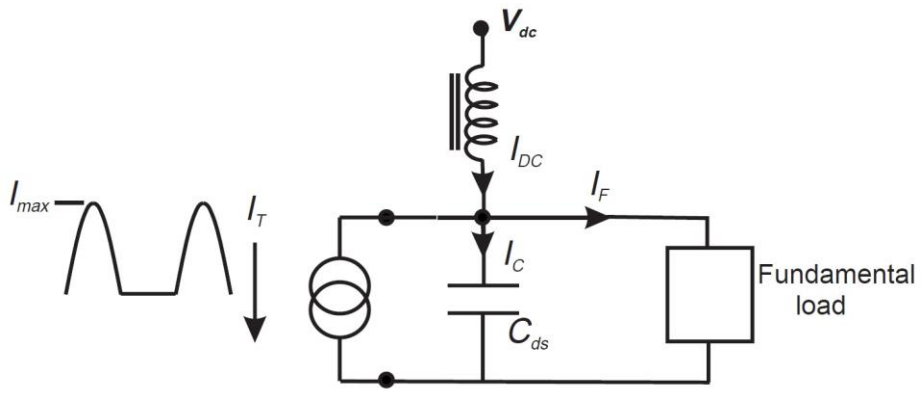


Fig. 3. 44: Circuit topology showing transistor as an ideal current generator biased at class B conditions to provide halfwave current waveform [41]

Eq. 3.32, Eq. 3.33 and Eq. 3.34 represent: transistor current I_T of the current source, fundamental current I_F passing through the fundamental matching network, and current I_C passing through the shunt capacitor of Fig. 3. 44, respectively [41].

$$I_T = \begin{cases} I_{max}\sin\theta, & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi \end{cases} \tag{3.32}$$

$$I_F = I_1 \sin(\theta + \phi) \tag{3.33}$$

$$I_C = I_{DC} - I_T - I_F \tag{3.34}$$

In Eq. 3.33, I_F and ϕ are the variables that define circuit elements of matching networks while I_c in Eq. 3.34 is the current passing through the shunt capacitor. I_{DC} is defined in terms of I_{max} in Eq. 3.35 while the output voltage V_o can be given as Eq. 3.36 [41].

$$I_{DC} = \frac{I_{max}}{\pi} \tag{3.35}$$

$$V_o(\theta) = \begin{cases} \dfrac{1}{\omega C}\left[\displaystyle\int_0^{\theta}\left(I_{max}\sin\theta - \frac{I_{max}}{\pi} - I_1\sin(\theta+\phi)\right)d\theta\right] + V_{off}, & 0 < \theta < \pi \\ \dfrac{1}{\omega C}\left[\displaystyle\int_0^{\pi}\left(I_{max}\sin\theta - \frac{I_{max}}{\pi} - I_1\sin(\theta+\phi)\right)d\theta + \int_{\pi}^{0}\left(-\frac{I_{max}}{\pi} - I_1\sin(\theta+\phi)\right)d\theta\right] + V_{off}, & \pi < \theta < 2\pi \end{cases} \tag{3.36}$$

Eq. 3.36 can be expanded as Eq. 3.37 [41].

$$\omega C V_o(\theta) = \begin{cases} I_{max}\left[1 - \dfrac{\theta}{\pi} - \cos\theta\right] + I_1[\cos(\theta+\phi) - \cos\phi] + V_{off}, & 0 < \theta < \pi \\ I_{max}\left[2 - \dfrac{\theta}{\pi}\right] + I_1[\cos(\theta+\phi) - \cos\phi], & \pi < \theta < 2\pi \end{cases} \tag{3.37}$$

In Eq. 3.37, V_{off} is DC offset value that will be assigned to keep: $V_0(\theta) \geq 0$ and to ensure knee conditions of classical class B amplifier are met [41]. Analysis of waveforms is performed by selecting independent variables I_1 and ϕ, followed by calculation of the function V_o for the whole cycle expressed in Eq. 3.36; to find the minimum value. Minimum value of the function V_o helps to define offset voltage V_{off} and scales the former along-with suitable choice of reactance scaling factor $\left(\frac{1}{\omega C}\right)$ to provide a mean value of 1, i.e. ($V_o = 1$) [41].

3.5.4 Comparison between Class B and Class J Amplifiers

Fig. 3. 45 shows three different voltage waveform cases defined by the selection of independent variables I_1 and ϕ, i.e. $I_1 = 2, 0.7, 0.6$. The first case $I_1 = 2$ is a close match to class B operation with the presence of minimal harmonic components in sine voltage waveform. However, for the other two cases i.e. $I_1 = 0.7$ and $I_1 = 0.6$, voltage waveforms indicate presence of higher harmonic components and deviation from sinusoidal waveform. The latter two cases have higher fundamental voltage components but also larger phase shifts from corresponding current waveforms. Higher fundamental voltage component arises due to the presence of reactive voltage components which are generated by the flow of harmonics into the capacitor. Fundamental load impedances (normalised to corresponding loadline resistance) can be determined through in-phase and quadrature components of V_o that are calculated through Fourier integrals shown in Eq. 3.37. Normalised capacitive reactance that scales V_o to $V_o = 1$ is also a function of the selected values of I_1 and ϕ [41].

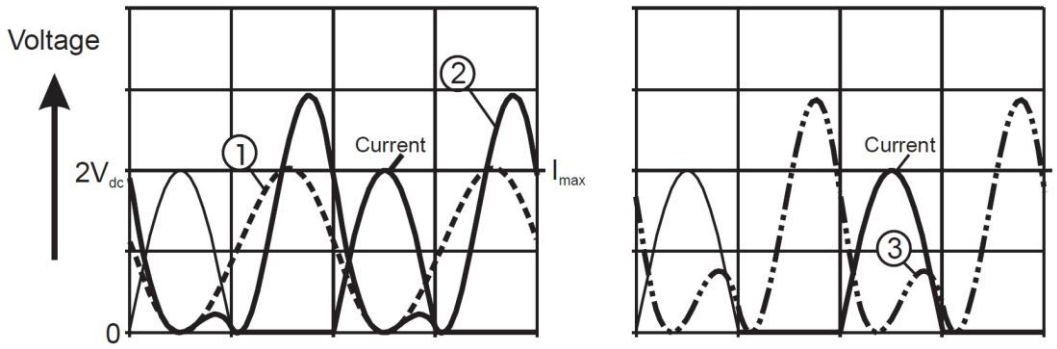
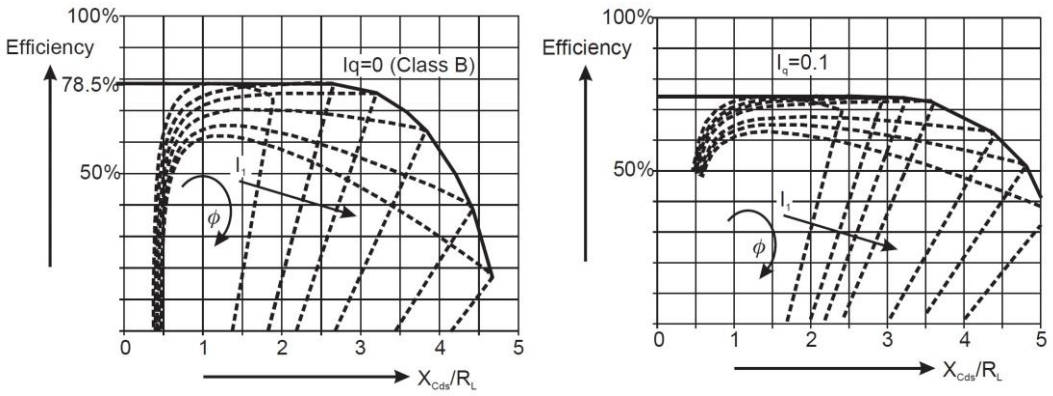


Fig. 3. 45: Current and voltage waveforms for: (a) $I_1 = 2$ and 0.7, (b) $I_0 = 0.6$ [1]

Analysis of the three cases by Cripps (2006) in [41] shows that the first two cases, i.e. $I_0 = 2$ and 0.7 provide same efficiencies as class B amplifier (78.5 %) with much difference in their waveforms. It has also been discussed that the ratio between reactance

of output capacitance and loadline resistance: $\frac{X_{cds}}{R_L} = 0.27$ for the first case is well below 1 and close to classical class B performance. However, reactance of fundamental component provides same efficiency as class B mode. The discussion highlights significance of output capacitance (C_{ds}) as an important performance index, however, values of $\frac{X_{cds}}{R_L} > 2.5$ result into a sharp drop in efficiency and output power. The second case ($V_o = 0.7$) indicates the limiting condition where: $\frac{X_{cds}}{R_L} = 2.65$. However, it shows same efficiency as class B amplifier at the cost of higher peak voltage. Limiting condition of $\frac{X_{cds}}{R_L}$ can be improved by moving slightly above quiescent class B bias ($I_\mathrm{q} = 0$) towards deep class AB bias ($I_\mathrm{q} = 0.1$). Comparison between ranges for $\frac{X_{cds}}{R_L}$ has been shown in Fig. 3. 46, where (a) and (b) show useable ranges under class B and class AB bias conditions, respectively [41].



(a) (b)

Fig. 3. 46: Comparison between the usable ranges of $\frac{X_{cds}}{R_L}$ and respective efficiencies for: (a) class B, and (b) deep class AB bias conditions [1]

Deep class AB operation is categorised by Cripps (2006) as class J mode in [41].

3.5.5 Effect of Non-Linear Output Capacitance

In deep class AB (or class J) configuration, harmonic components generated by output capacitance (C_{out} or C_{ds}) are added to the fundamental component which contribute towards enhancing efficiency and output power of the amplifier. However, linear behaviour of the capacitor was discussed. This section presents review of non-linear output capacitance (discussed in [41], [63], [64] and [65]) towards efficiency enhancement of transconductance amplifiers which essentially reduces phase difference between voltage and current waveforms (shown in Fig. 3. 45).

Consider the equivalent circuit model of an ideal FET shown in Fig. 3. 47 [65]. Where, C_{out} is output capacitance that includes drain to source capacitance (C_{ds}), and gate to drain capacitance (C_{gd}). These capacitances are modulated by their respective voltages, i.e. V_{ds} and V_{gd}. However, contribution of C_{gd} on output capacitance is negligible compared to C_{ds}, thus, it has not been considered in the analysis [41]. The relationship between linear and non-linear output capacitance (C_{ds}) and respective drain to source modulating voltage V_{DS} has been shown in Fig. 3. 48 [65].

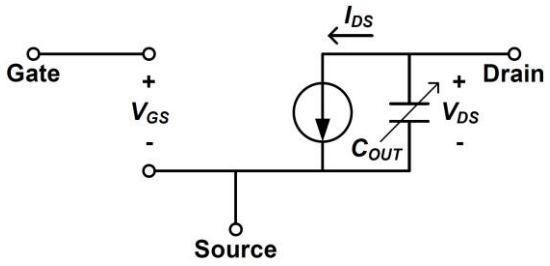


Fig. 3. 47: Equivalent circuit model of an idealized FET with output capacitance (C_{out}) that includes: C_{gd} and C_{ds} [71]

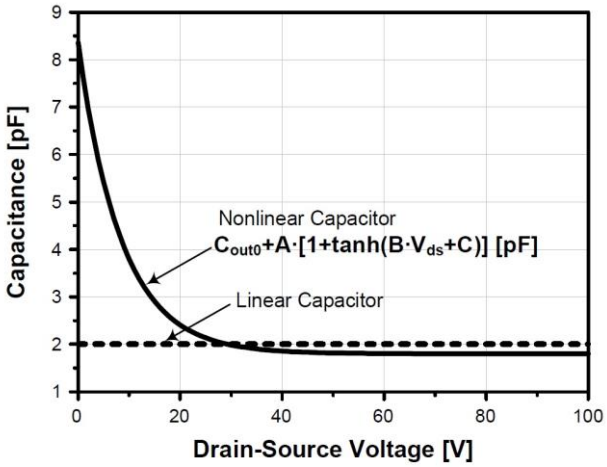
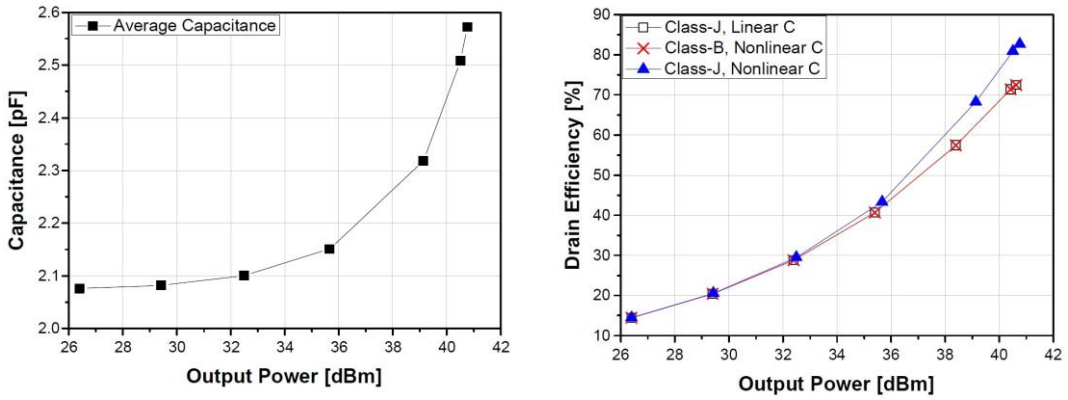


Fig. 3. 48: Relationship between linear and non-linear output capacitance C_{ds} and the respective drain to source modulating voltage [71]

It can be observed from Fig. 3. 48 that variation of non-linear capacitor is considerably large at low values of V_{ds} and there is much difference between linear and non-linear capacitances. It has been suggested in [64] and [30] that the input non-linear capacitance C_{gs} has minimal effect on the performance of transconductance power amplifiers, though it contributes towards harmonic component generation. However, appropriate input harmonic termination networks can be utilised to maintain sinusoidal nature of the input drive signal going into the gate for transconductance power amplifiers like class B, class AB and class J. Fig. 3. 49 (a) presents average capacitance versus output power for class J amplifier designed by considering non-linear output capacitance. Fig. 3. 49 (b) shows

drain efficiency versus output power for class J amplifier designed by considering both linear and non-linear output capacitances, and class B amplifier designed by considering non-linear output capacitance [65].



(a) (b)

Fig. 3. 49: (a) average capacitance of class J amplifier versus output power for non-linear output capacitance, (b) drain efficiency versus output power for class J amplifier with linear output capacitance, and class B and class J amplifiers with non-linear output capacitance [32]

Fig. 3. 49 shows important results for the analysis of non-linear output capacitance in class J amplifiers. When output capacitance in class J amplifiers is considered linear, performance similar to classical class B amplifiers can be achieved. However, when output capacitance is considered non-linear, an improvement in efficiency compared to classical class B or class J amplifiers is observed which is mainly due to the reduction in phase difference between voltage and current waveforms. It has also been suggested in [65] that if a purely resistive fundamental load impedance is presented, phase difference could be effectually reduced to zero. This would also reduce heat dissipation and improve efficiency during the regions where non-zero current and voltage waveforms overlap each other. This way, authors of [65] were able to achieve 77.7 % PAE at 2.14 GHz with 11.5 W output power, through class J saturated amplifier with non-linear output capacitance in the absence of a harmonic loading network. The amplifier was designed using commercially available Cree CGH40010 GaN transistor.

3.5.6 State of the Art in Class AB Amplifiers

Class AB amplifiers have been designed to provide tens of watts of microwave power with very high efficiencies, some state-of-the-art class AB amplifiers that have been recently developed are presented in this section.

Gadallah et al. (2015)

Gadallah et al. (2015) in [66] presents a high efficiency multistage class AB X-band CMOS power amplifier with 7.21 dBm output power, 38.5 % PAE (5 GHz) and 12 dB gain from 3-7 GHz. This amplifier utilised CG configuration transistor in the gain stage while CS configuration transistor in the power stage. Post layout simulation results have been presented.

Alqadami et al. (2017)

Alqadami et al. (2017) in [67] presents a 5 W high efficiency class AB power amplifier using GaN HEMT discrete transistor device at 3.4 GHz to 3.7 GHz frequency band with 51.9 % PAE and 37 dBm output power suitable for LTE base station applications.

Malik et al. (2017)

Malik et al. (2017) in [68] presents a 14 W high efficiency class AB balanced power amplifier using commercially available GaN HEMT discrete transistor for wireless cellular communications with 111 % fractional bandwidth, 11.4 dB - 13.5 dB gain and 43 % - 54.7 % PAE.

Chen et al. (2018)

Chen et al. (2018) in [69] presents a 56 W high efficiency class AB power amplifier using commercially available GaN HEMT discrete transistor with 200 MHz bandwidth and up to 70 % PAE at 2.4 GHz using trapezoidal taper matching network.

3.5.7 State of the Art in Class J Amplifiers

Design of classical class J amplifiers utilises the phase overlap between current and voltage waveforms, and is performed independently through bias conditions, input drive level and active multi harmonic load pull. Harmonic load impedances at fundamental and second harmonic are obtained using Eq. 3.38 and Eq. 3.39 (presented in [70]) which are then optimised for the desired output power and efficiency performance. Harmonic components beyond the second harmonic are considered to be short circuited through a large output capacitance of the transistor Class J high efficiency power amplifiers are also less sensitive to termination networks at higher order harmonics and wideband performance can be achieved with real impedance terminations networks. Brief description of some class J amplifiers is enlisted below:

Wright et al. (2009)

Wright et al. (2009) presents a mechanism of achieving high efficiency over wide bandwidth by performing active load pull and waveform measurements in [71] and [70].

A high efficiency linear power amplifier operating over a wider bandwidth from 1.4 GHz to 2.6 GHz has been demonstrated by performing active harmonic load pull for up to the third harmonic component and restricting the design space for the fundamental load impedance to prevent non-zero crossing voltage waveform (or the clipping that causes nonlinearities, AM-AM distortion and gain compression) during any point in the RF cycle. Output power of 39 dBm was achieved throughout the band with at-least 50 % PAE through a commercially available 10 W GaN HEMT transistor [70].

Moon et al. (2010)

Moon et al. (2010) in [65] presents design and analysis of class J saturated amplifier with non-linear output capacitance by providing a purely resistive fundamental load impedance to effectually reduce phase difference between the current and voltage waveforms to zero, consequently achieving high efficiency. 77.7 % PAE was demonstrated at 2.14 GHz with 11.5 W output power using commercially available Cree CGH40010 GaN HEMT transistor.

Kim et al. (2011)

Kim et al. (2011) in [72] have utilised the inherent phase difference of $\pi/4$ between current and voltage waveforms of class J amplifiers to present class J and inverse class F amplifiers to increase the drain efficiency by manipulating both voltage and current waveforms. The concept has been demonstrated through a commercially available 60 W GaN HEMT transistor from Cree. The second harmonic current component of class J mode is modified by: the elimination of in-phase component and manipulation of the quadrature component. While the voltage waveform is manipulated by introducing a phase shift of $\pi/4$ and $\pi/2$ in the fundamental and second harmonic components, respectively. The third and higher harmonics are short circuited through large output capacitance. Thus, the phase difference is reduced from $\pi/4$ (in class J) to 0 (in inverse class F) to achieve 91.07 % theoretical efficiency in inverse class F amplifiers. Fabricated class J amplifiers delivers 46.8 dBm saturated output power with 66.7 % and 56.6 % drain efficiency and PAE, respectively. While fabricated inverse class F amplifier delivers 47 dBm output power with 68.2 % and 59.6 % drain efficiency and PAE, respectively.

Alizadeh et al. (2017)

Alizadeh et al. (2017) in [60] presents proof of concept for 1.5-10 GHz distributed class J amplifiers developed using 0.25 µm AlGaAs-InGaAs pHEMT technology. The amplifier achieves an average of 20 dBm output power with 10 dB large signal gain and 33-44 % PAE. The maximum PAE occurs at 6.5 GHz.

Couturier et al. (2018)

Couturier et al. (2018) in [73] presents high efficiency multistage class J amplifier developed using 250 nm gate length GaN on SiC MMIC technology from UMS (GH25-10). The amplifier has been biased under class AB conditions with appropriate fundamental and second harmonic load terminations determined through software based load pull analysis. 20 W CW output power is achieved in 7.8 to 8.8 GHz frequency band with 19 dB power gain and at-least 50 % PAE.

Poluri et al. (2019)

Poluri et al. (2019) in [74] presents high efficiency class B/J amplifier with waveforms in the continuum between class B/J and inverse class F mode amplifiers by partially removing the in-phase second harmonic component of class J mode amplifier. The authors achieve 79.7 % drain efficiency with 42.2 dBm output power at 2.6 GHz through the amplifier fabricated using commercially available GaN HEMT CGH40010F transistor. The amplifier also shows at least 58 % and 65 % drain efficiency and PAE, over a bandwidth of 600 MHz from 2.2 GHz to 2.8 GHz.

Sharma et al. (2019)

Sharma et al. (2019) in [75] presents a new class of waveform engineered high efficiency amplifier by providing open circuit conditions (open-open or O^2) to both second and third harmonic components. This is opposed to class B amplifiers where both are short circuited, class J where the second harmonic component is short circuited or reactive in a continuum between short circuit and open circuit conditions, and class F where the second and third harmonic components are short and open circuited, respectively. Besides this, waveform engineering is O^2 is performed on both input and output harmonic components.

3.6 Switching Mode Power Amplifiers

3.6.1 Introduction

Switching amplifier were briefly introduced earlier in this chapter and discussed to provide up to 100% theoretical efficiencies by having the transistor ‘switch’ between high impedance ‘off state’ and low impedance ‘on state’ during the RF cycle. This way the overlap region between voltage and current waveforms is minimised and power dissipation takes place only at the switching intervals. However, modelling of the transistor as a simple switching element at high frequencies [41] and power dissipation at switching intervals remains an important concern which is mainly caused due to short circuiting of the parasitic capacitance when the switch closes. Relatively small amount of energy is also lost due to parasitic series inductance when the switch opens, non-zero on

resistance (R_{on}) and non-infinite off resistance. This section discusses design equations, waveforms engineering techniques, high frequency class E amplifier operation, efficiency enhancement techniques, and review of the state of art in class E amplifiers. Cripps (2006) presents schematics for an ideal switching amplifier in [41] which has been reproduced in Fig. 3. 50. The switch is assumed to act as ideal short circuit (on-state) or ideal open circuit (off-state), with the switching controlled through input power drive level and bias conditions. Instantaneous switching is assumed to occur between 'on' and 'off' states.

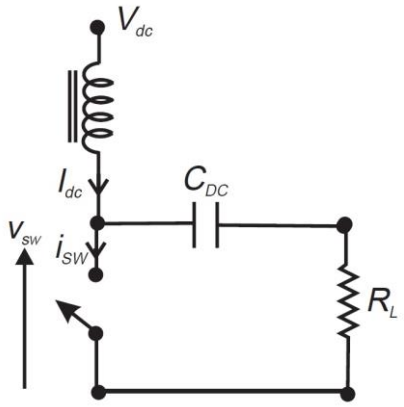
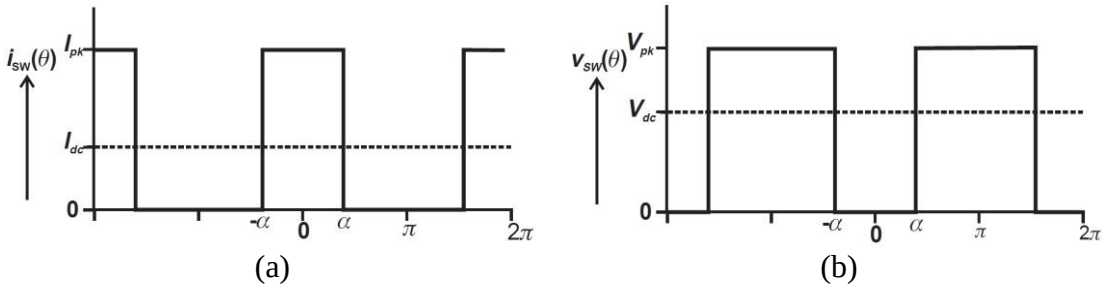


Fig. 3. 50: Ideal topology for an RF switching mode amplifier [41]

Circuit schematics shown in Fig. 3. 50 includes choked supply and load resistance that is connected through RF blocking capacitor. Current and voltage waveforms with switching duty cycle of 50 % have been reproduced from Cripps (2006) in Fig. 3.51. Conduction angle for this case is 2α, in accordance with the switch closure period. Maximum current for the switch is controlled through supply voltage V_{DC} and load resistor R_L. Peak voltage V_{pk} is a function of conduction angle α and supply voltage V_{DC}. DC supply voltage V_{DC} is assumed to remain constant to variations in the conduction angle. These assumptions result in an asymmetrical voltage waveform where V_{pk} is proportional to twice the supply voltage when the conduction angle α is varied above or below $\frac{\pi}{2}$ [41].



(a) (b)

Fig. 3.51: (a) current, and (b) voltage waveforms for the ideal RF switch [1]

RF power P_{rf} in terms of DC supply voltage and current (V_{dc} and I_{dc}), and conduction angle α is given in Eq. 3.38, while output efficiency has been given in Eq. 3.39 [41].

$$P_{rf} = V_{dc} \cdot I_{dc} \cdot \frac{2 \cdot sin^2\alpha}{\alpha(\pi - \alpha)} \tag{3.38}$$

$$\eta = \frac{2 \cdot sin^2\alpha}{\alpha(\pi - \alpha)} \tag{3.39}$$

For a symmetrical square waveform (Fig. 3.51), the maximum efficiency about 81 % or $\frac{8}{\pi^2}$ occurs at $\alpha = \frac{\pi}{2}$, while maximum proportion of fundamental power in relation to the linear power occurs at a conduction angle of about $116°$ or $\alpha = 0.63\pi$. Thus, symmetrical square waveform corresponding to an ideal switch does not provide theoretical efficiency of 100 % as the power is distributed to higher order harmonics [41].

3.6.2 Tuned Switching Amplifier

Undesirable power at higher order harmonics can be eliminated by providing short circuit conditions across the load to higher order harmonics, this provides a theoretical efficiency of 100 %. Fig. 3. 52 shows schematics for an ideal tuned switching amplifier with a "Tank" circuit across the load resistor R_L [41].

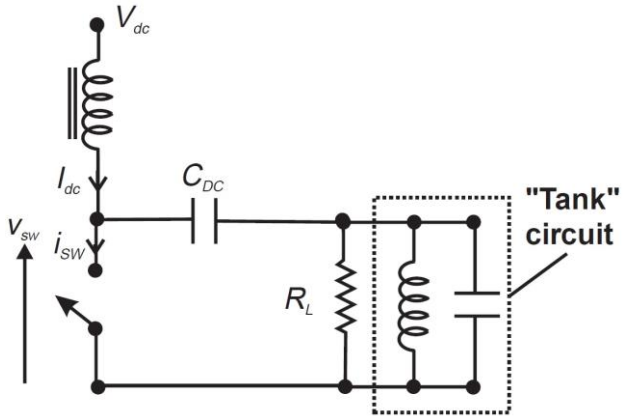
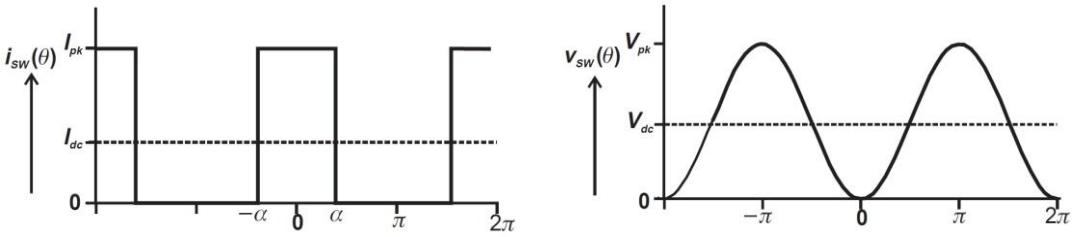


Fig. 3. 52: Topology for a tuned RF switching mode amplifier with a parallel "tank" circuit to provide short circuit conditions to higher order harmonics [41]

Corresponding voltage waveform in this condition would be a pure sinusoidal wave. With other assumptions made in the preceding section still in place, current and voltage waveforms have been given in Fig. 3.53 [41].



(a) (b)

Fig. 3.53: (a) current, and (b) voltage waveforms for a tuned RF switching mode amplifier with a parallel "tank" circuit [41]

RF fundamental power P_1 in terms of DC supply voltage and current (V_{dc} and I_{dc}), and the conduction angle α has been given in Eq. 3.40, while output efficiency has been given in Eq. 3.41 [41].

$$P_1 = V_{dc} \cdot I_{dc} \cdot \frac{\sin(\alpha)}{\alpha} \tag{3.40}$$

$$\eta = \frac{\sin(\alpha)}{\alpha} \tag{3.41}$$

Tuned switching amplifier shows an efficiency of about 87 % when the ratio between fundamental and linear power is 1. This gives an important result that the behaviour of transistor as a switch cannot alone provide theoretical efficiency of 100 %.

3.6.3 Class E Switching Mode Amplifiers

The theory of class E switching amplifiers was first presented by Sokal (1975) in [76], while underlying design equations were derived by Raab (1977) in [77]. Cripps (2006) presents ideal schematics of class E mode switching amplifier by considering the behaviour of transistor as a switch, with a parallel capacitor (C_p) which is assumed to have a value that does not act as a parasitic element in the amplifier nor a perfect harmonic short circuit. Also, series resonator circuit includes the load resistor. Basic schematics for class E switching mode amplifier has been reproduced in Fig. 3. 54.

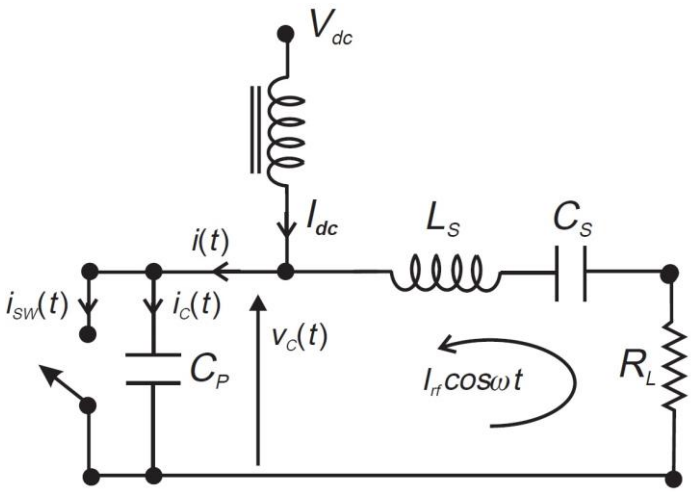


Fig. 3. 54: Basic topology for an ideal class E switching mode amplifier with parallel capacitance (C_p) and series resonant circuit incorporating the load resistance (R_L) [41]

Current conduction angle of ideal class E amplifier can be defined by considering flow of current through the switch ($i_{sw}(\theta)$) during 'on-state' and through the shunt capacitor ($i_c(\theta)$) during the 'off-state'. This way conduction angle can be given as: $\phi = \propto_1 + \alpha_2$, where, α is defined in ideal current and voltage waveforms reproduced in Fig. 3. 55.

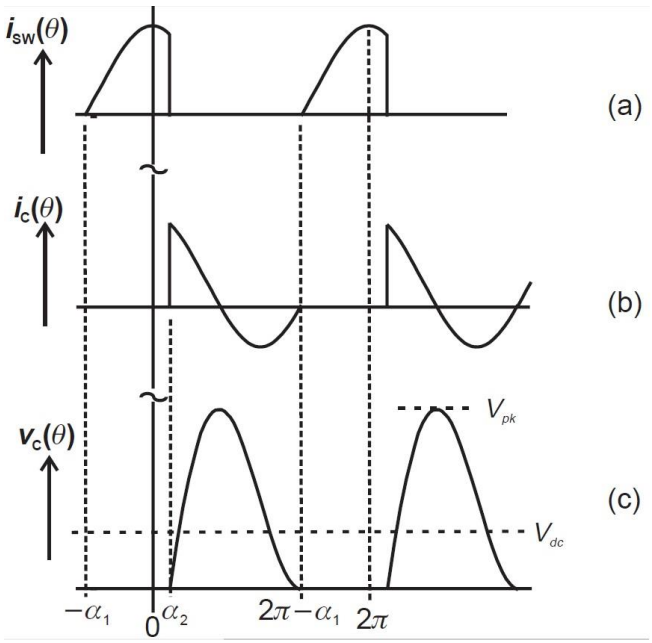


Fig. 3. 55: Ideal class E amplifier waveforms, (a) current through the switch, (b) current through the shunt capacitor, and (c) voltage waveform through the shunt switch/capacitor [41]

Current and voltage waveforms shown in Fig. 3. 55 have been utilised to explain the operation of class E amplifiers by Cripps (2006) in [41]. Integration of voltage waveform starts from 0, which is the point when the switch opens ($\theta = \alpha_2$) and the entire current is transferred from switch to shunt capacitor (shown in Fig. 3. 55 (b) and (c)). Voltage

waveform crosses the zero point again when the switch closes where entire current is transferred to the switch ($\theta = 2\pi - \alpha_1$). This way voltage and current waveforms do not overlap each other and provide a theoretical DC to RF efficiency of 100 %. Load resistor is the only resistive element in ideal schematics of class E amplifier shown in Fig. 3. 54, which is seen by the switch at the fundamental frequency. Thus, power will not be distributed to harmonics other than the fundamental, and power at harmonic frequencies will be purely reactive. This makes DC to RF efficiency independent of conduction angle. Lastly, it can be implied that mean DC level will be lower than half of the peak value as the voltage waveform is asymmetrical and non-sinusoidal [41].

3.6.4 Optimal Conduction Angle for Class E Amplifiers

It has been discussed by Cripps (2006) in [41] that theoretical efficiency of 100 % in class E amplifiers can be achieved independently from the conduction angle. However, the power utilisation factor (PUF) highly depends upon the conduction angle and thus it is necessary to define optimal conduction angle to achieve required PUF from the amplifier. Fig. 3. 56 shows relationship between PUF and conduction angles for class E amplifier. PUF is defined as: the ratio between power achieved through class E operation and that of optimum class A amplifier being operated under the same conditions, including DC supply voltage. Higher values of conduction angle can provide higher values of PUF (greater than unity), however, peak voltage is required to be carefully selected for a particular conduction angle to prevent the transistor from operating close to the breakdown region. DC supply voltage can be reduced to control peak voltage (generalised convention follows:$V_{pk} = 2 \cdot V_{dc}$), but this results in a reduction of available power.

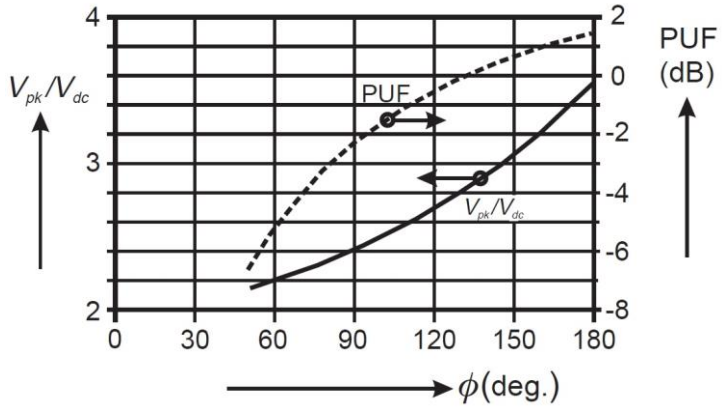


Fig. 3. 56: The relationship between power utilisation factor (PUF) and the conduction angle for class E operation [41]

Trade-off needs to be made in selection of conduction angle for class E operation between PUF and desired peak voltage, which is application dependent. However, good

compromise can be achieved (as illustrated in Fig. 3. 56) by having a conduction angle: $\phi \approx 110° \pm 30°$, with deviation specific to the application [41].

3.6.5 Load Networks for Class E Amplifiers

Grebennikov (2004) in [78] presents various load network configurations and corresponding design equations for class E amplifier design. Parallel circuit class E circuit topology has been shown in Fig. 3. 57.

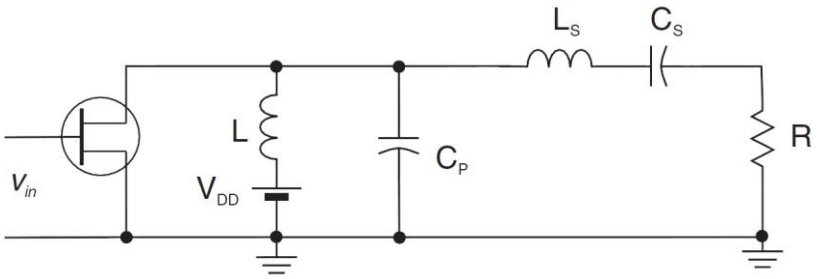


Fig. 3. 57: Topology for generalised parallel circuit class E amplifier [69]

Design equations for the elements of parallel circuit class E amplifier (Fig. 3. 57) have been presented in Eq. 3.42 to 3.44 which were derived by Grebennikov (2004) in [78]. C_p accounts for drain to source parasitic capacitance (C_{ds}) of the transistor, maximum frequency has been given in Eq. 3.45 [64], [78].

$$R \simeq 1.365 \cdot \frac{V_{DD}^2}{P_{out}} \tag{3.42}$$

$$L \simeq 0.732 \cdot \frac{R}{\omega} \tag{3.43}$$

$$C_p \simeq 0.685 \cdot \frac{1}{\omega R} \tag{3.44}$$

$$f_{max} \simeq 0.0798 \cdot \frac{P_{out}}{C_{ds} \cdot V_{DD}^2} \tag{3.45}$$

For circuit topology shown in Fig. 3. 57, lumped elements C_p, L_s, C_s tuned at the fundamental frequency and load resistor R perform voltage and current waveform shaping across the transistor. Above discussion considers an infinite Q_L for lumped elements, which is generally suited for lower frequencies and cannot be applied to higher RF and microwave frequencies in GHz where Q_L of lumped elements is low. However, use of quarter wavelength transmission line in the biasing network can help to isolate the bias supply at the fundamental frequency and odd harmonics from even harmonics (short circuited). Class E topology with quarter wavelength transmission line in the bias network

has been shown in Fig. 3. 58. Corresponding design equations are expressed in Eq. 3.46 to 3.48 [64], [78].

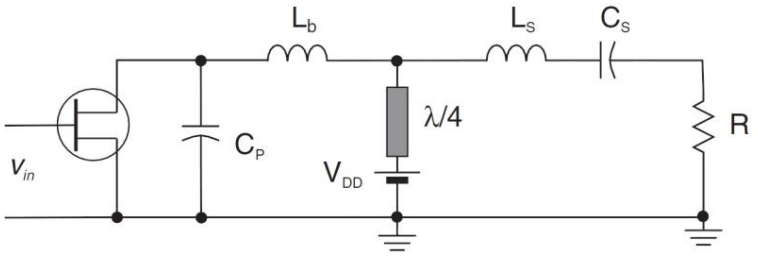


Fig. 3. 58: Topology for generalised class E amplifier with quarter wavelength transmission line in the biasing network [69]

$$R \simeq 0.465 \cdot \frac{V_{DD}^2}{P_{out}} \tag{3.46}$$

$$L \simeq 1.349 \cdot \frac{R}{\omega} \tag{3.47}$$

$$C_p \simeq 0.2725 \cdot \frac{1}{\omega R} \tag{3.48}$$

3.6.6 High Frequency Operation of Class E Amplifiers

The discussion presented in preceding sections was based on low frequency operation with analysis made mainly in the time domain. However, an important factor that comes into action at higher RF and microwave frequencies is output capacitance of the transistor (C_{out} or C_{ds}), which provides short circuit conditions to higher order voltage components and the transistor no longer depicts behaviour of an ideal switch. At higher RF and microwave frequencies, drain current waveform is assumed to be unchanged (compared to low frequency operation) while voltage waveform is defined according to the load network. This short circuiting of higher order voltage harmonics and unchanged current waveform has been represented in Fig. 3. 59 [64].

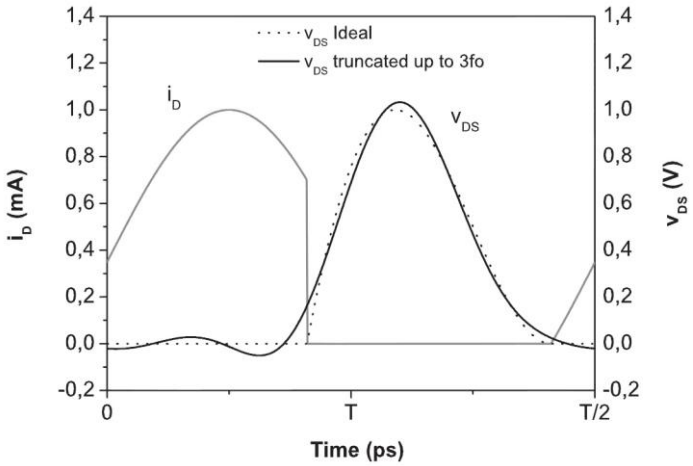


Fig. 3. 59: Current and voltage waveforms of class E amplifier at higher frequencies where the output capacitance is assumed to provide short circuit conditions to harmonic components above the third harmonic [69]

It can be observed in Fig. 3. 59 that the voltage waveform has negative values, especially in the low frequency region (examined through Fourier analysis), which can be prevented by having a shunt diode across transistor's drain terminal and shunt capacitance C_p. However, this is not a common practice. The negative values can also be prevented by optimising the load network and by increasing the quiescent bias voltage, however, this comes at the cost of increased DC power consumption, increased dissipated power in the transistor, and reduced theoretical efficiency to: $\eta \simeq 84.7$ % (with an increase in the DC supply voltage by a factor of 1.181) [64], [41].

3.6.7 State of the Art in Class E Amplifiers

Wilkinson et al. (2001)

Wilkinson et al. (2001) in [79] have demonstrated a prototype microstrip amplifier at 1 GHz by utilising a transmission line load network topology for narrow-band class E amplifier to achieve a peak drain efficiency of 72 %. The amplifier was built on a low loss RT Duroid 5880 board by utilising a commercially available Avantek ATF 8140 GaAs FET. However, the authors suggested that a faster FET could provide improved switching operation of the amplifier to achieve higher efficiency. Comparison of measured results showed much similarity between lumped element amplifier and distributed element prototype and opened dimensions for research.

Mediano et al. (2007)

At high microwave frequencies, output parasitic capacitance of the transistor which has a nonlinear behaviour mainly controls various design parameters, frequency of operation and the achievable output power and efficiency. Mediano et al. (2007) in [80] present a

design methodology for class E amplifiers by combining a linear shunt capacitance with the nonlinear output capacitance of the transistor for any duty cycle.

Grebennikov (2008)

Grebennikov (2008) in [81] presents the concept of switched mode tuned class FE power amplifier by combining switching conditions (ZVS and ZVDS) of class E amplifier to class F amplifier topology. This way high frequency operation of class F amplifiers may be achieved. A shunt capacitance and series inductance (alternatively quarter wavelength transmission line in the load network) have been included in the load network of class F amplifiers to achieve soft-switching operation.

Grebennikov (2011)

Grebennikov (2011) in [82] demonstrated the concept of combined class E and inverse class F (also called Class E/F mode) by utilising Cree GaN HEMT CGH40010F transistor with distributed transmission lines to achieve 40 dBm output power with 14.3 dB power gain, 76 % drain efficiency and 73.1 % PAE at 2.14 GHz.

Jee et al. (2012)

Jee et al. (2012) in [83] presented a technique to improve performance of class E amplifiers by using the same basic topology of class E amplifiers with a matched output load through load pull, inductive second harmonic tuning and a bifurcated current waveform due to amplifier's operation in saturation. 40.2 dBm output power is reported with 75.8 % drain efficiency at 3.5 GHz by utilising commercially available Cree GaN HEMT CGH40010 device in the design of saturated class E amplifier.

Grebennikov (2016)

Grebennikov (2016) in [84] demonstrated broadband capabilities of class E/F amplifiers by utilising shunt capacitance and shunt filter resonant circuits based on reactance compensation principle. To ensure broadband matching at the input network, stepped transmission line sections with varying electrical lengths and characteristic impedances was employed. The amplifier was developed using commercially available Cree GaN HEMT CGH40010 transistor to operate over a frequency band from 1.7 GHz to 2.7 GHz. 40.6 ± 0.9 dBm output power was achieved with drain efficiency varying from 63 % to 73 % and 9.5 dB power gain.

Kakkad et al. (2017)

Kakkad et al. (2017) in [85] have demonstrated class E amplifier by utilising a commercially available Cree GaN HEMT CGH40010F transistor at 3.6 GHz to achieve

up to 39.2 dBm saturated output power with 67.42 % drain efficiency. Load network in amplifier topology includes a shunt capacitor, followed by second harmonic matching network (also used for drain biasing) and fundamental load matching network.

Mugisho et al. (2019)

Mugisho et al. (2019) in [86] demonstrated class E power amplifier by employing a shunt capacitance and shunt filter in the load network with 50 % duty cycle. The amplifier operating at 1.37 GHz provides 39.8 dBm output power with 90.2 % drain efficiency, 82.7 % PAE and 11.5 dB power gain. This is the highest reported drain efficiency for class E amplifiers in the frequency band.

3.7 Microwave Oscillators

3.7.1 Introduction

Oscillators are essential elements of a microwave system with applications in communication, radars, instrumentation and RF and microwave surgical and therapeutic devices. Solid state oscillators are nonlinear circuits that convert DC to steady state RF sinusoidal signal by utilising an active nonlinear transistor or diode devices alongside passive circuit elements. Ideal oscillator circuits generate pure RF or microwave sinusoidal signal with fixed frequency, phase and amplitude. However, practical implementation of oscillators generally involves frequency and output power variance with time, which is an important design aspect. Pozar (2012) in [44] discusses that basic transistor oscillators combined with crystal resonators can be used at lower frequencies, with the latter providing frequency stability and improved noise performance. Hartley and Colpitt, Clapp and Pierce oscillators are well known low frequency transistor oscillator configurations [44], [29].

Early development of oscillator circuits was performed using Gunn and IMPATT diodes, however, the developments in GaAs FETs in the 1970s opened up new dimensions for microwave transistor oscillators at frequencies up to the millimeter wave ranges. Gunn and IMPATT diode oscillators perform well in terms of higher frequency and output power, however, transistor oscillators provide several advantages that include: higher compatibility with other elements in the microwave system, suitability for monolithic microwave circuit integration, low phase noise, independence from threshold current requirements and higher power efficiency performance; making the latter a popular choice for microwave systems [44], [29].

In an oscillator circuit, the amplifier is seen as a positive feedback or negative resistance circuit element which is connected to a resonator, which are the two design approaches for oscillator design. However, negative resistance oscillators remain optimal design choice for higher microwave frequencies up to 100 GHz [29]. Oscillators are required to provide stable, low noise and broadband tuneable performance, and the design issues to achieve them include achieving low phase noise, low DC power consumption, and higher tuning range to cater for process variations. Robertson (2001) in [29] discusses the suitability and low phase noise performance of HBT and HEMT based microwave oscillators in MMIC technology. A popular design choice is quasi MMIC circuits that simplify the fabrication process, improve reliability and noise performance, by having a negative resistance (or reflection) amplifier on a single chip along-with the corresponding bias and decoupling circuit elements, and off chip high quality factor resonators.

This section presents review of transistor oscillator topologies, switching mode class E oscillator design and brief analysis of state of the art in class E oscillators.

3.7.2 Transistor Oscillator Topologies

It was discussed earlier in this section that transistor oscillators are preferred over diode oscillators at microwave frequencies, thus, they will remain the focus of discussion here. Feedback approach to oscillator circuit design considers the transistor as a current transconductance amplifier, combined with frequency selection circuit, provides appropriate phase shift and required input power level to the input (or gate) terminal of the transistor. Frequency of oscillation and noise performance is defined through the resonator (which may be off chip) and Q factor of the frequency selection network. Small signal gain is generally kept higher to support start-up conditions for oscillation; however, the final gain would be less once steady state has been achieved and the device operates in saturation. Pozar (2012) in [44] presents the generalised circuit for a negative resistance oscillator, which has been reproduced in Fig. 3. 60.

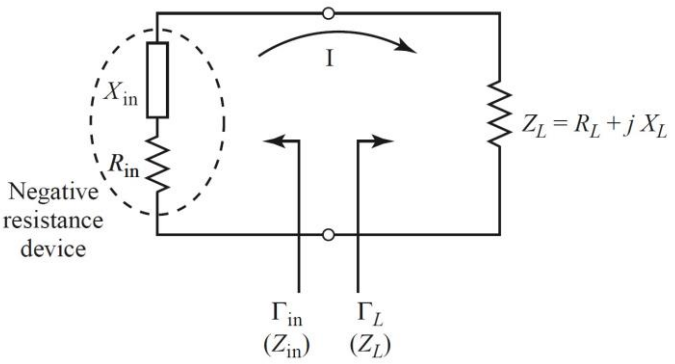


Fig. 3. 60: General circuit representation of one-port negative resistance oscillator [44]

Input impedance of the transistor shown in Fig. 3. 60 is given by: $Z_{in} = R_{in} + jX_{in}$ which is frequency, voltage and current dependent. The necessary conditions required for oscillation are given in Eq. 3.49 and 3.50 [44].

$$R_L + R_{in} = 0 \tag{3.49}$$

$$X_L + X_{in} = 0 \tag{3.50}$$

The conditions will hold once RF current is nonzero. Resistive part of the input impedance (R_{in}) will imply a 'negative value' as the load resistor (R_L) is passive (or positive). Reactive condition given in Eq. 3.50 controls the frequency of oscillation [44]. Nonlinear behaviour of the transistor specified as input impedance (Z_{in}) defines the process of oscillation; and the oscillator circuit is required to be unstable at the intended frequency of operation, such that $R_L + R_{in} < 0$. Unstable behaviour could also be increased by having a positive feedback. Transient excitation will cause the oscillations to build up and RF current will increase until the conditions specified in Eq. 3.49 and 3.50 are met, where the oscillator will achieve steady state operation. Pozar (2012) in [44] specifies that the final frequency at steady state oscillations will be different from start-up frequency as the reactive part of input impedance is current dependent. Also, on experiencing transient disturbance through a variation in the load network or change in bias conditions, the oscillator circuit will adjust itself to appropriate frequency. Several other design aspects should be considered for oscillator design including parasitic capacitances of the transistor which contribute towards provision of feedback, bias point, output power, large signal behaviour and noise performance.

The design of transistor oscillators involves selection of an appropriate transistor device and bias conditions, which is followed by small signal analysis to identify possible unstable behaviour. Feedback network to provide sufficient negative resistance and input reflection coefficient, i.e. $|S_{11}| > 1$ is designed next. Large signal analysis is conducted to determine optimum load network to achieve maximum power. This could also be performed through various models that include: Trew's model [87], Van Der Pol's Model, or Gewartowsky's model discussed in [88]. Towards the last step, a lossy passive resonator is designed to obtain oscillations from the circuit at desired operating frequency. Resonators play an important role in an oscillator circuit as they help to define the frequency of oscillation, noise performance, and characteristics of the feedback signal. Quality factor (or Q factor) is the ratio between stored energy and energy loss per cycle

(or average power loss). However, practical considerations of Q factor involve analysis of 3 dB bandwidth of: the frequency response of power transmission or reflection at the desired frequency of oscillation. Q-factor for series and parallel resonator circuits [44] can be given by Eq. 3.51 and 3.52, respectively, where inductance, capacitance and resistance are connected in series or shunt according to the respective topology. Loaded Q factor can also be defined for resonator circuits that are not connected to the load; however, this approach is not practical as there is always a load connected to the active transistor which delivers power into it.

$$Q = \frac{\omega_o L_s}{R_s} = \frac{1}{\omega_o C_s R_s} \tag{3.51}$$

$$Q = \frac{R_p}{\omega_o L_p} = \omega_o C_p R_p \tag{3.52}$$

3.7.3 Switching Mode Oscillators

The reported efficiency of oscillator circuits is low and much of the power is dissipated as heat during the DC to RF conversion [88], [89], [90]. Switching mode oscillators have been discussed in literature to improve efficiency of the oscillator circuits. These include class E or class F amplifier topology and feedback network that provides required phase shift and conditions of oscillation. This sub-section presents review of switching mode oscillators with focus on non-linear design techniques.

Jeon et al. (2006) in [89] presents non-linear design technique for class E switching mode oscillators. The technique involves design and optimisation of class E amplifier and respective feedback network based on terminal voltages and currents. Harmonic balance simulation is then performed in CAD based simulation utilities such as Keysight's ADS with an auxiliary generator (AG) that adjusts the frequency of oscillation to desired steady-state value and provides sufficient enough input power level to drive the amplifier in the saturation region. Thus, achieving high efficiency and switching mode operation. However, some important concepts like the effect of gate and drain bias voltages, drain current and voltage waveforms, embedded feedback network design, and operation of the amplifier (class E or class F) in saturation region needs to be considered. Basic topology of class E oscillators, discussed by Jeon et al. (2006) in [89], is shown in Fig. 3. 61.

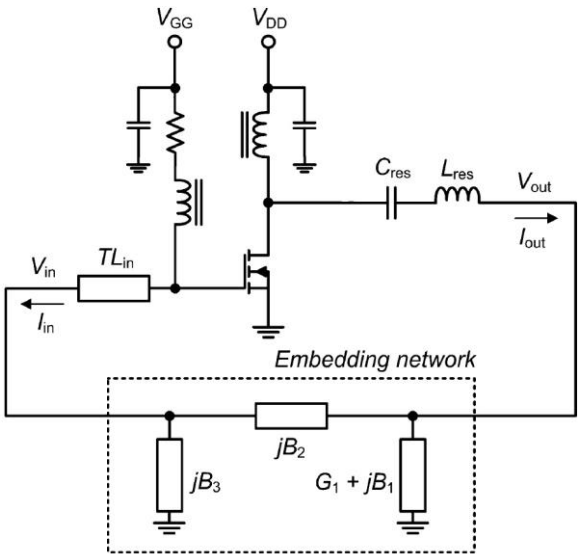


Fig. 3. 61: Basic circuit topology for class E oscillators [92]

Circuit topology shown in Fig. 3. 61 involves the transistor in class E configuration connected in series to an LC tank circuit and embedding network which replaces class E amplifier load network. The embedding network maintains original terminal voltage and current of class E amplifier and provides the required input source excitation to drive the amplifier in deep saturation.

Class E Amplifier Optimisation

The design procedure starts with selecting deep class AB bias conditions and utilising the design equations for class E amplifier (reviewed in the preceding section) to design an optimised high efficiency and high output power amplifier. Optimisation involves using non-linear device models to accurately predict the performance in non-linear saturation conditions. Once the amplifier has been optimised, corresponding input power level and voltage and current values at the input and output reference planes of the amplifier are used to design the embedding network. LC tank (with a high Q-factor) in the load network of class E amplifiers (shown in Fig. 3. 57 and Fig. 3. 58) facilitates the design of embedding network at the fundamental frequency through its strong band-pass filtering performance [91]. It prevents harmonic components generated at the drain terminal from affecting output load conditions. Also, the shunt output capacitance terminates higher order harmonics at the drain terminal. Thus, current waveform is close to a pure sinusoidal wave.

Embedding Network Design

Embedding network for switching mode oscillators can take either T or π network topologies, with both having their advantages which have been discussed in [90]. The

embedding network shown in Fig. 3. 61 is a π-network with three reactive and one resistive circuit elements, i.e. $jB_1, jB_2\ and\ jB_3$, and G_1, respectively. Two port Y-parameters discussed by Jeon et al. (2006) in [89] have been given in Eq. 3.53, which can be solved to calculate the design values for reactive and resistive values for embedding network. Terminal voltage and currents (V_{in}, V_{out}, I_{in} and I_{out}) correspond to the ones shown in Fig. 3. 61 and calculated from optimised class E amplifier. It is pertinent to mention that Eq. 3.53 is solvable only if right hand side is not singular, i.e. the value of $V_{out} \neq 0$ and there exists phase difference between V_{in} and V_{out} [90].

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \begin{bmatrix} j(B_2 + B_3) & -jB_2 \\ -jB_2 & G_1 + j(B_1 + B_2) \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \tag{3.53}$$

Eq. 3.53 can be solved using MATLAB to determine the values of: B_1, B_2, B_3, and G_1, which can be utilised to determine appropriate reactive and resistive circuit elements.

Auxiliary Generator and Class E Oscillator Optimisation

Suárez et al. (2003) in [92] presents the concept of Auxiliary Generator (AG) which is a harmonic balance simulation source, consisting of a voltage source connected in series with a band pass filter that provides short circuit conditions at the desired frequency of oscillation and open circuit conditions at all other frequencies. It can be connected to the input terminal to perform optimisation of class E switching mode oscillators, by providing the required input power amplitude for class E amplifier operation while maintaining the frequency of oscillation.

Effect of Gate Bias on Output Power and Efficiency

Higher efficiency of class E amplifiers and switching mode oscillators can be achieved when the gate is biased below the threshold region where small signal gain is non-existent. However, oscillators require sufficient small signal gain to provide start-up conditions for oscillation and achieve steady state.

Matsuo et al. (2000) in [93] discuss that an excitation signal to trigger oscillations at the desired frequency can be provided to oscillators when the transistor is biased at sub-threshold conditions. Jeon et al. (2006) in [89] discuss that the gate may be initially biased at a higher voltage than the threshold voltage; once steady state oscillatory behaviour is observed, it may be reduced below threshold to achieve higher efficiency. Simulation based analysis has been presented where MRF193 LDMOS from Freescale Semiconductor Inc. was used as active transistor in the design of class E switching mode oscillator. The AG is used to sweep various values of gate bias voltages (starting from 5 V DC and reduced to sub threshold -2 V DC) for four different drain voltages.

Convergence of harmonic balance for steady state oscillations is observed. The curve for efficiency versus gate bias voltage sweep has been shown in Fig. 3. 62, where, solid and dashed lines represent stable and unstable oscillation regions, respectively. Oscillations build up when the gate is biased above threshold voltage and it can be observed that a reduction of gate bias from a higher value than threshold sustains oscillations until a turning point, after which hysteresis phenomenon is observed and oscillations cease to exist. This occurs due to high power oscillations at the gate terminal while the gate bias approaches threshold voltage from a higher value. These oscillations are also related to the input drive signal of AG, which makes the transistor to function as a switch by turning it on and off (switching mode operation). When the gate bias is reduced to sub-threshold voltage, self-generated input signal decreases; however, it remains high enough to operate the transistor as a switch. This way high efficiency can be obtained. On the other hand, oscillations do not occur when the gate is biased in the sub-threshold region due to lack of self-generated input drive signal and will only start when bias voltage is increased beyond the threshold voltage.

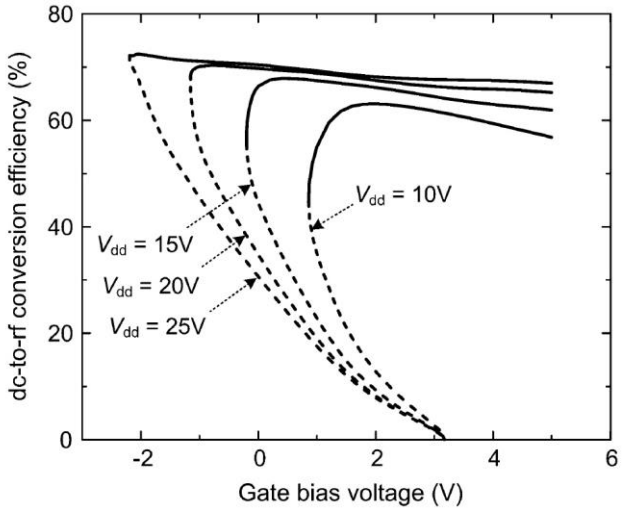


Fig. 3. 62: Curves for the dc to RF efficiency versus gate bias sweep for various values of drain bias [93]

It can also be observed from Fig. 3. 62 that gate bias voltage, corresponding to the turning point between stable and unstable oscillation regions, decreases with higher values of drain bias. This is due to a larger swing being generated at the gate terminal which can sustain oscillations for longer once gate bias is reduced. However, for gate bias voltages below the turning point, level of voltage waveform at the gate terminal has reduced sufficiently to sustain oscillations [89].

3.7.4 Review of Oscillator Design

Ebert (1981)

Ebert et al. (1981) in [94] presented the initial theoretical concepts of optimal conditions of oscillations in class E tuned power oscillators. The design was based on BSXP60 BJT transistor where a three-port reactive network was designed to provide the same collector to emitter voltage for the oscillator as in class E amplifier mode, and high energy storage in the reactive network to provide frequency stability. Collector efficiency of over 95 % was achieved with 3 W output power at 2 MHz.

Tsang (1994)

Tsang et al. (1994) in [95] utilised large signal [S]-parameter design techniques to demonstrate high power class E oscillator. Motorola MRF559 BJT was used to design class E oscillator at 900 MHz to provide 27.56 dBm output power with 57.54 % collector efficiency. The design technique involved measurement and modelling of large signal [S]-parameters for respective transistors, selection of optimum fundamental load and feedback impedances to design tuned load termination network, design of feedback network and transient analysis to achieve convergence and stable oscillations. Similar design approach has been used to design class E MMIC oscillator presented in Chapter 6 of this thesis.

Ellinger (2001)

Ellinger et al. (2001) in [96] presents class E MMIC oscillator operating in the C band, designed using standard 0.6 µm Triquint TQRXs MESFET GaAs process. Variation of supply voltage demonstrated efficiency of up to 43 % with 6.5 dBm output power at 4.4 GHz and 1.8 V supply voltage, and 36 % with 1.1 dBm output power at 3.6 GHz and 0.9 V supply voltage. Aim of the integrated oscillator circuit measuring $1\ \mathrm{mm}^{-2}$ was to achieve high efficiency for reduced power consumption in battery operated receivers.

Kazimierczuk (2005)

Kazimierczuk et al. (2005) in [97] demonstrates class E tuned power oscillator designed using MTP3055E MOSFET to achieve 82 % efficiency with 0.953 W output power at 800 KHz. The circuit consists of positive feedback network which provides part of class E amplifier output to gate terminal of the MOSFET. Output power and frequency of oscillation were dependent upon the tuneable inductance (of feedback network). Stable oscillations at 800 KHz with -35 dBc and -53 dBc levels of second and third harmonic components compared to the fundamental frequency component were achieved.

Chang (2015)

Chang et al. (2015) in [98] demonstrated high efficiency class E oscillator using 0.5 µm E/D pHEMT GaAs process. The integrated oscillator circuit provides 24.8 dBm output power with 53 % efficiency at 2.5 GHz with 4 V supply voltage and 1.5×1.5 mm^{-2}chip size. Π-feedback network from class E amplifier load termination network was introduced in the letter alongside a shunt capacitance with drain terminal of the transistor.

Chang (2017)

Chang et al. (2017) in [99] presents high efficiency K band class E oscillator designed using 0.15 µm GaAs pHEMT process from WIN semiconductor foundry. The oscillator demonstrates 19 % peak efficiency with 21 dBm maximum output power from 23.5 to 24.5 GHz. High frequency operation of class E oscillator has been achieved by operating class E amplifier under deep bias conditions where transistor's operation in the saturated region provides bifurcated current waveform. Feedback network from load network to input terminal of the oscillator is a microstrip transmission line having 80 Ω characteristic impedance. Second harmonic rejection level is -44 dBc with -106.3 dBc/Hz phase noise.

Krizhanovski (2018)

Krizhanovski (2018) in [100] demonstrates prototype high frequency oscillator at 1 MHz with 0.82 W output power and 86 % efficiency. The oscillator topology considers the transistor in class E switching amplifier mode terminated into inverse class F load network. This way high efficiency is achieved by reducing peak drain voltage and suppressing higher order harmonic components of the output signal.

3.8 Conclusion

This chapter presented review of background concepts, ideal operation, design guidelines, performance criteria, figures of merit and state of the art in high efficiency power amplifiers and switching mode oscillators. These were extensively utilised in the design of high efficiency power amplifiers and switching mode oscillator presented in succeeding chapters of this thesis to achieve targeted results for intended medical applications.

Chapter 4

Development of High Efficiency Power Amplifiers

4.1 Introduction

This chapter discusses the development of high efficiency discrete power amplifiers for electrosurgical devices and therapeutic systems. These amplifiers will act as stepping stone towards the development of monolithic integrated circuits (presented in Chapter 6 and 7) to enable localised power generation and delivery to the treatment site, with minimal distributed tissue heating and energy loss. Target specifications were defined in collaboration with Medical Microwave Systems Research Group at Bangor University and Creo Medical to produce sufficient continuous wave (CW) output power at 5.8 GHz ISM band frequency to achieve coagulation on tissue structures. An application envisaged is a portable microwave applicator structure [101] capable of delivering microwave energy at 5.8 GHz to effectively coagulate bleeding sites not easily controlled under conventional haemostatic modalities in the battle-field, where uncontrolled haemorrhage from major trauma is leading mechanism of death [102]. The device could be used as an interim procedure facilitating evacuation to a suitable facility or even as a longer-term solution if other facilities are not readily available. Initial tests and results of the portable haemostasis device will be presented in Chapter 5. Table 4. 1 enlists some target specification for the amplifiers presented in this chapter.

Table 4. 1: Target specifications for high-efficiency discrete power amplifiers

Characteristics	Symbol	Value	Unit
Operating Frequency	f	5.8	GHz
Saturated Output Power	P_{sat}	> 20	W
Small Signal Gain	G_{ss}	> 10	dB
Large Signal Gain	G_{LS}	> 6	dB
Power Added Efficiency	PAE	> 60	%

A generalised design flow for high efficiency discrete power amplifiers has been shown in Fig. 4. 1, while generalised high efficiency power amplifier structure having various sub-networks has been shown in Fig. 4. 2, however, the amplifiers will only have appropriate sub-networks to satisfy their design and operation requirements. The design process starts with definition of target specifications and selection of appropriate

semiconductor technology, transistors and passive elements. GaN HEMT transistors provide remarkable performance in high power applications which were reviewed in Chapter 2. CGH55015 and CGH55030 GaN HEMT packaged transistors from Cree/Wolfspeed were chosen due to their suitable performance metrics and availability of small and large signal models. Accuracy of models in the knee region, where high efficiency amplifiers are operated, will be commented on during analysis of respective amplifiers. Evaluation of these HEMTs has been presented in Section 4.2 of this chapter with discussion on DC characterisation, small and large signal behaviour, output capacitance and stability analysis.

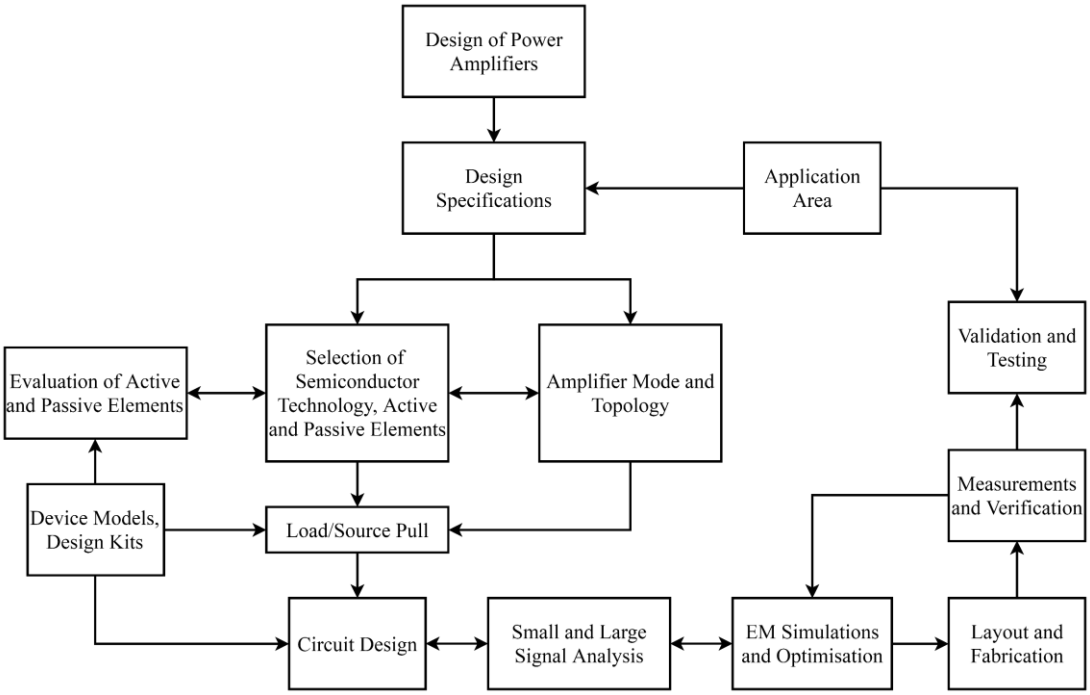


Fig. 4. 1: Design flow of High Efficiency Power Amplifiers

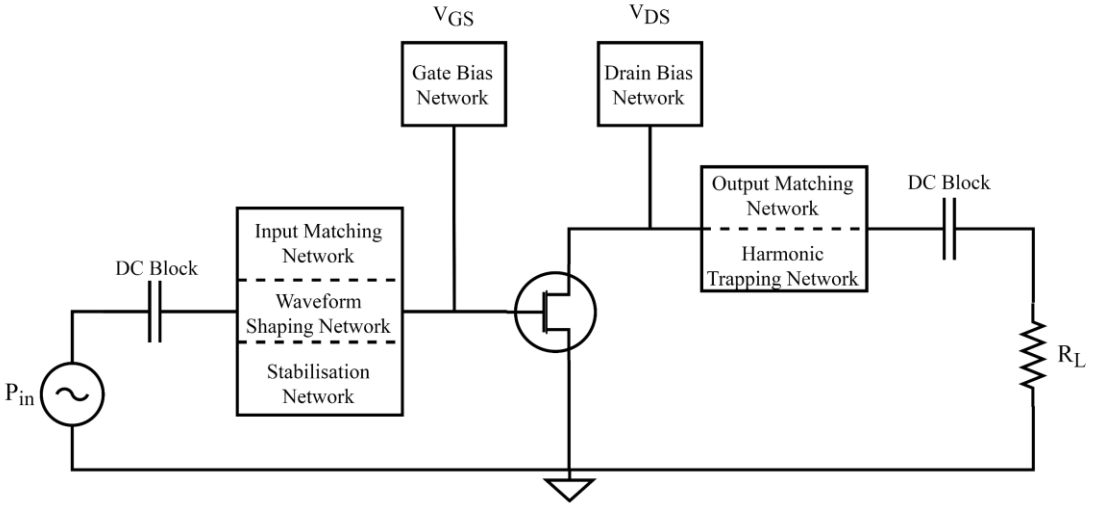


Fig. 4. 2: Generalised structure for high efficiency power amplifiers

The suggested PCB board for development of amplifiers using discrete transistor, distributed and lumped elements for high power applications is Rogers RO4350B because of its reasonable relative dielectric constant of 3.48 which permits suitable transmission line dimensions and the ability to provide controlled impedance at the desired frequency band, reliability, low dielectric losses and the ability to support high bias line currents through narrow high impedance lines [103]. However, Rogers RO5870 and RO5880 boards have also been compared. In the next step, various circuit topologies and high efficiency amplifier modes were reviewed which include class B, class AB, class J, class E, class F and inverse class F amplifiers. However, class AB and class F amplifiers were developed, which have been presented in Section 4.3 and 4.4 of this chapter, respectively. Multistage amplifier that consists of class AB amplifier in gain stage and class F amplifier in power stage has been discussed in Section 4.5 of this chapter. Following the selection of appropriate transistor and amplifier mode (or topology); simulation, optimisation and analysis of various sub-networks of an amplifier circuit (shown in Fig. 4. 2) is performed. Stability of the amplifier is important to prevent oscillations, which may occur at low frequencies or under large input power drive level. Certain techniques to analyse stability of amplifiers have been discussed in Section 4.2 of this chapter.

An important design step of power amplifiers is determination of input and output matching networks, which depend on respective amplifier mode of operation. For instance, class F amplifiers employ complex input and output matching networks that include source and load sub-networks at the fundamental frequency and waveform shaping (harmonic trapping) sub-networks at higher order harmonics. On the other-hand, class AB amplifiers have simpler source and load networks, which require short circuit and reactive conditions at the second harmonic, respectively. Optimum source and load impedances of these networks are obtained through source and load pull techniques that were reviewed in the preceding chapter. However, they will be discussed in respective sections of the amplifiers with reflective comments. The design process also involves design and optimisation of bias networks that include decoupling capacitors and RF choke or transmission lines to bias the transistors. They may also include stabilisation components like resistors. Optimised gate and drain bias networks for discrete amplifiers have been presented in Section 4.2.5. Finally, component level and circuit level electromagnetic simulations are performed down to DC to optimise the performance of amplifiers before layout is processed for fabrication. Once the amplifiers have been fabricated, testing is performed to identify any oscillations in the circuit, including out of

band low frequency oscillations. This is conducted through spectrum analyser. Measurements include small signal [S]- parameter and large signal power measurements. Measurement setup for the amplifiers has been discussed in Section 4.2 of this chapter. Validation and testing of amplifiers for respective medical application will be discussed in the next chapter, where background review of the interaction between microwave energy and human body will be presented.

4.2 Evaluation of Packaged Transistors and Design Aspects

4.2.1 Introduction

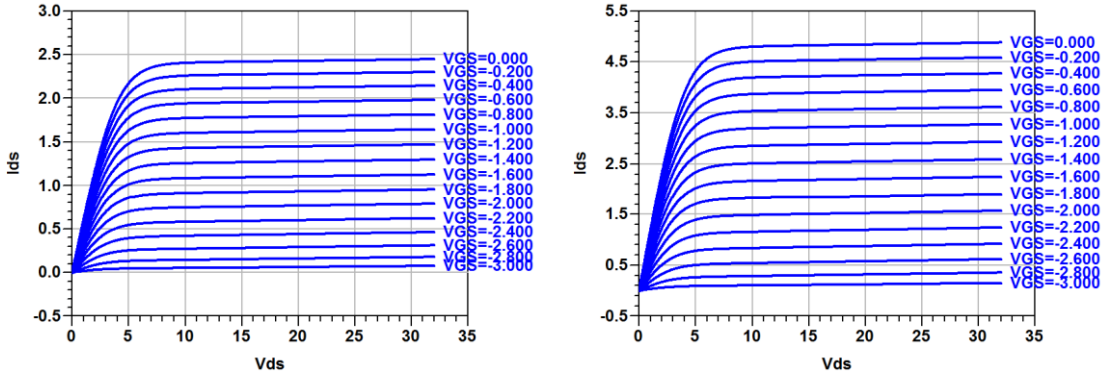
This section presents evaluation of Cree GaN HEMT CGH55015 and CGH55030 packaged (metal ceramic) transistors and design considerations that have been used towards the development of high efficiency power amplifiers presented in this chapter. The evaluation has been performed by exploiting information provided through device datasheets, small and large signal models, and discussions with Mr Tom Dekker from Wolfspeed.

CGH55015 GaN HEMT screw-down flange packaged transistor is available in two different variants: CGH55015F1 and CGH55015F2; which operate over 5.5-5.8 GHz and 4.5 to 6.0 GHz to provide 15 W and 10 W saturated output power (P_{sat}), respectively. CGH55015F1 has been used in the design of class AB and class F amplifiers presented in Sections 4.3 and 4.4 respectively, while CGH55015F2 has been used in the gain (class AB) stage of multistage amplifier presented in Section 4.5 of this chapter. CGH55030F2 has been used in power stage (class F) of multistage amplifier presented in Section 4.5. The transistor operates from 4.5-6.0 GHz to provide up to 25 W P_{sat}. The datasheets of these devices suggest up to 60 % drain efficiency at P_{sat} under test conditions. At 5.8 GHz the transistors can effectively provide ~15 dB small signal gain [104]–[106]. However, considering high power operation of the amplifier close to the knee region, the expected small signal gain should be ~13 dB.

4.2.2 DC Characteristics of the Transistors and Bias Conditions

The output current (I_{ds}) characterisation with variation in gate to source (V_{gs}) and drain to source (V_{ds}) voltages was performed for the two transistors through DC IV sweep simulations based on models provided by Cree/Wolfspeed. Fig. 4. 3 (a) shows simulated DC-IV characteristics of CGH55015 transistor with V_{gs} and V_{ds} swept from -3.0 V to 0 V in steps of 0.2 V and 0 V to 32 V in steps of 0.1 V, respectively; while Fig. 4. 3 (b) shows simulated DC-IV characteristics of CGH55030 transistor with V_{gs} and V_{ds} which

were swept from -3.0 V to 0 V in steps of 0.2 V and 0 V to 32 V in steps of 0.1 V, respectively.



(a) (b)

Fig. 4. 3: DC IV characteristics of (a) CGH55015 and (b) CGH55030

DC characteristics can be utilised to define bias conditions and load-lines for various classes of reduced conduction angle amplifiers reviewed in Chapter 3. Loadline analysis has been discussed by Cripps (2002, 2006) in [41], [63], which will be exploited here to obtain load lines for class A, class AB, deep class AB and class B amplifiers. Class J and class F amplifiers use deep class AB and class B load lines, respectively. However, it is important to mention that the loadline is generally elliptical (or looping) for amplifiers where high efficiency is obtained by minimising overlap between current and voltage waveforms at the drain. For classical reduced conduction angle amplifiers, voltage waveform at the drain is kept purely sinusoidal, and V_{DS} (represented in Eq. 4.1) is chosen to achieve maximum voltage swing within the limitations defined by knee (V_K) and breakdown (V_B) voltages. Thus, load impedance (Z_L) would be purely resistive (R_L) when higher order harmonics are assumed to be short circuited by the output capacitance or through a shunt resonant circuit at the fundamental frequency. Load resistance for such case (R_L) has been expressed in Eq. 4.2.

$$V_{DS} = \frac{V_B + V_K}{2} \tag{4.1}$$

$$Z_L = R_L = \frac{V_{DS} - V_K}{I_{DS}} \tag{4.2}$$

Fig. 4. 4 shows load-lines for various cases of reduced conduction angle amplifiers, i.e. class AB ($\Theta = 240°$), class B ($\Theta = 180°$) and deep class AB ($\Theta \approx 200°$). The load-line for class A amplifier ($\Theta = 360°$) has also been drawn for comparison.

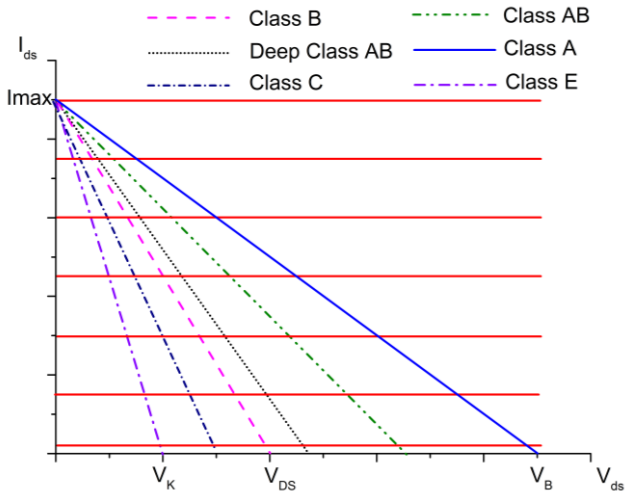


Fig. 4. 4: Load-lines for reduced conduction angle amplifiers

4.2.3 Stability Analysis

Stability of an amplifier could be conditional or unconditional, with unstable behaviour observed because of the negative real part of input or output port impedances, which can potentially cause oscillations in an amplifier circuit. Input and output reflection coefficients that help identify unstable behaviour can be represented as Eq. 4.3. However, stability can be defined in terms of certain regions on the Smith chart that follow input and output reflection coefficient given by Eq. 4.4. A system will be unconditionally stable if Eq. 4.4 holds for all passive load and source impedances on the Smith chart, such that $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$. However, a system will only be conditionally stable if conditions defined in Eq. 4.4 hold for a limited range of source and load impedances. Stability of an amplifier can be analysed through stability tests that include $K - b$ test where, K is the Rollet stability factor and b is the stability measure, given in Eq. 4.5 and 4.6 respectively. Some other stability analysis tests have been discussed in [44].

$$|\Gamma_{in}| > 1 \text{ or } |\Gamma_{out}| > 1 \tag{4.3}$$

$$|\Gamma_{in}| < 1 \text{ and } |\Gamma_{out}| < 1 \tag{4.4}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}||S_{12}|} > 1 \tag{4.5}$$

$$b = 1 + |S_{11}|^2 - |S_{22}|^2 > 0 \tag{4.6}$$

Where, $\Delta = S_{11}S_{22} - S_{21}S_{12}$.

An amplifier can be made unconditionally stable within linear region of its operation by appropriate design of input and output matching networks that lie within stable regions

on the Smith chart. However, large input power drive level swings out of the linear region causing various non-linearities to occur that were discussed in Chapter 3. The device acts as a parametric element with parasitic behaviour; limiting the operating bandwidth and rendering it unstable. Stability of amplifiers during the design process is generally carried out by incorporating stability tests along-with an analysis of matching network and preventing them to cause any oscillations within the circuit. This requires determining input and output reflection coefficients multiple times to ensure that they remain within the boundaries. Similar procedure is adopted for multistage amplifiers where the circuit is partitioned into cascaded two port networks and stability is evaluated for each stage. Stability is a mathematical operation and needs to be evaluated for the entire frequency range where the amplifier has gain up to f_{max}, to identify potential oscillations. S-probe method has been defined within various EDA tools like Keysight's ADS and AWR MWO to determine stability of an amplifier by evaluation of reflection coefficients at any point within the circuit in either direction. Fig. 4. 5 shows stability measure and stability factor for CGH55015 HEMT, while figure Fig. 4. 6 shows load and source stability circles, when the transistor is biased at: $V_{DS} = 28$ V and $V_{GS} = -2.8$ V.

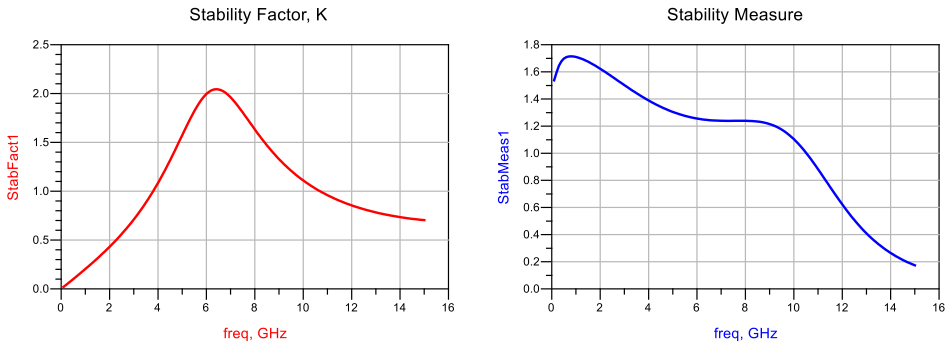


Fig. 4. 5: Stability factor and stability measure for CGH55015 transistor at $V_{DS} = 28\ V$ and $V_{GS} = -2.8\ V$

It can be observed from Fig. 4. 5 that CGH55015 HEMT is unconditionally stable in large impedance regions of the Smith chart (towards the right) and tends to become unstable when the device is terminated with low impedance values at the source. Fig. 4. 6 shows source and load stability circles and helps to identify areas on the smith chart that should be avoided while designing input and output matching networks. The load needs to be in bottom half of the Smith chart or capacitive. It can also be observed that the device has poor stability at lower frequencies that may cause oscillations within the amplifier circuit. Datasheet [104] indicates that the device has higher gain at lower frequencies, thus out of band low frequency oscillations need to be especially taken care of. CGH55030 HEMT shows similar stability factor and stability measure. However, its' load and source

stability circles (shown in Fig. 4. 7) cover larger region on the Smith chart compared to CGH55015 HEMT, especially the load stability circles.

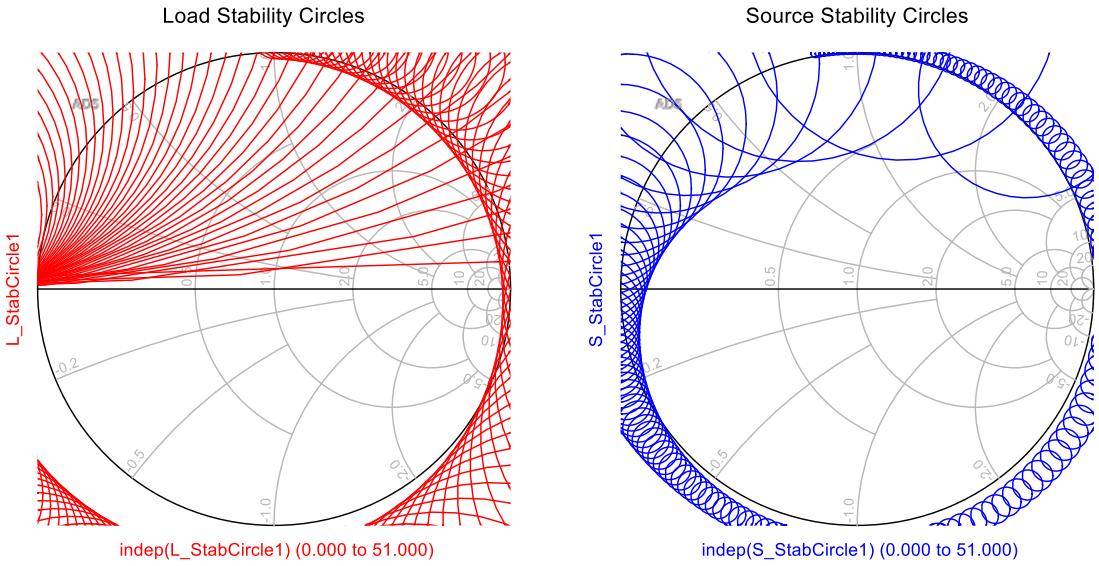


Fig. 4. 6: Source and load stability circles for CGH55015 transistor at $V_{DS} = 28$ V and $V_{GS} = -2.8$ V

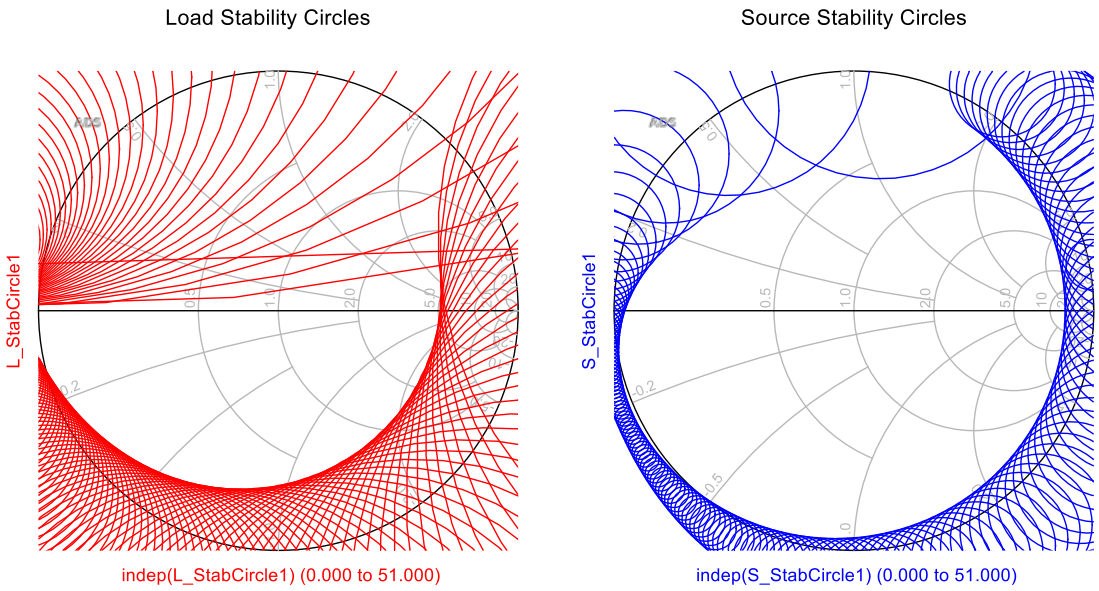


Fig. 4. 7: Source and load stability circles for CGH55030 transistor at $V_{DS} = 28$ V and $V_{GS} = -2.9$ V

Stability of the device can be improved by using various techniques like the addition of series or shunt resistors to the device's gate terminal. Comparison between the two cases indicate that higher stability is observed when a small series resistor is added to the device's gate terminal, however, this comes at the cost of reduced device gain and output power. Noise performance of amplifiers is also affected by series resistor; but it is not considered in the development of power amplifiers for medical applications presented in

this thesis. Shunt stabilisation resistor shows around 3 dB better gain while series stabilisation resistor provides wider space to design load termination on the Smith chart. In the design of power amplifiers presented in this chapter, shunt resistor of 22 Ω has been added to the gate bias line to provide stability, which has also been improved through optimised decoupling networks in the bias lines. Stability factor for CGH55015 HEMT after addition of shunt stabilisation resistor has been shown in Fig. 4. 8, while stability circles have been shown in Fig. 4. 9. The figures indicate stability for all terminations. Similarly, improved stability was also achieved for CGH55030 transistor through a 22 Ω shunt stabilisation resistor; however, it was further optimised through bias networks.

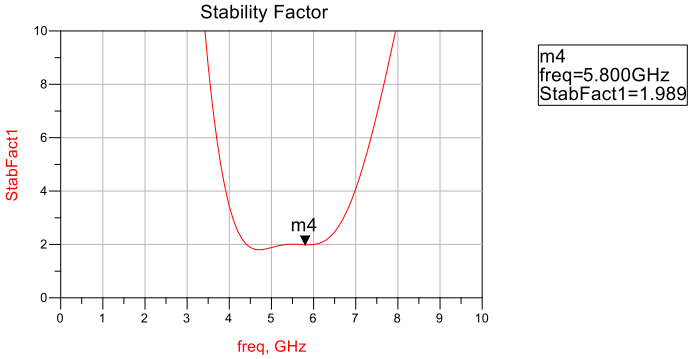


Fig. 4. 8: Stability factor for CGH55015 transistor at $V_{DS} = 28$ V and $V_{GS} = -2.8$ V after the addition of 22 Ω shunt resistor

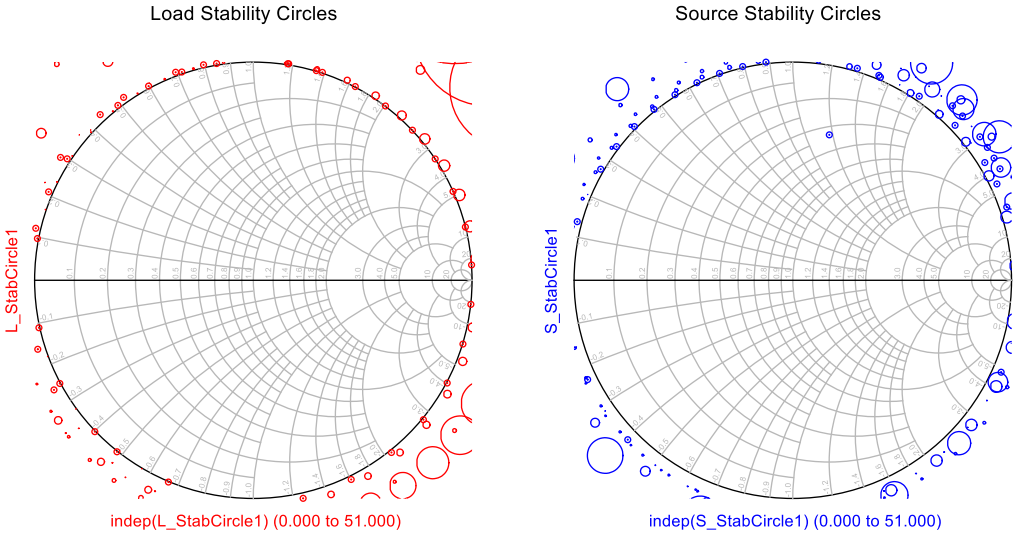


Fig. 4. 9: Source and load stability circles for CGH55015 transistor at $V_{DS} = 28$ V and $V_{GS} = -2.8$ V after the addition of 22 Ω shunt resistor

4.2.4 Large Signal Model

Small signal equivalent circuit model of HEMTs was discussed in Section 2.4.4, where it was highlighted that the model describes RF behaviour of a transistor in terms of its various intrinsic and extrinsic elements. The intrinsic elements of the model govern

various factors like f_T, f_{max} and current gain (discussed in Section 2.4.4). However, extrinsic elements of the model describe resistive and inductive effects that are beyond the drain, gate and source reference planes and affect transistor's performance. Extrinsic elements are also described as parasitics that transform the impedance provided to the fundamental and higher order harmonics. To facilitate the design of high power amplifiers using Cree GaN HEMT packaged transistors, Cree has developed 6-port large signal models which include gate, source, drain, temperature, HEMT intrinsic drain voltage and current. These models have been developed through established small signal circuit methods and extracted data that include load pull at the fundamental and higher order harmonics [107]. Intrinsic voltage and current data are provided at transistor's drain and gate reference planes.

Estimation of Output Capacitance

The effect of non-linear output capacitance (C_{ds} or C_{out}) was highlighted in Section 3.5.5 and review was presented on its effect towards the performance of class AB amplifier. C_{out} is a function of V_{ds}, however, it remains constant after a certain V_{ds} in GaN HEMTs [72], [108], where the difference between non-linear and linear C_{out} is negligible. A large value of C_{out} can provide short circuit termination to second harmonic component and help to achieve classical class AB performance; but it can have a low value and present reactive termination for class J operation. The latter case has been discussed in [70]. Furthermore, C_{out} has significance in class F amplifiers which have waveform shaping and harmonic tuning networks within their source and load termination networks. Thus, an accurate estimation of C_{out} in the constant region has been utilised in the design of high efficiency power amplifiers. $[S]$-parameters provided by Cree/Wolfspeed within the transistor model (at respective bias conditions) were converted to $[Y]$-parameters to evaluate various intrinsic elements of the small signal equivalent circuit model. Intrinsic elements, i.e. C_{gd}, C_{gs}, R_i, g_m, and C_{ds} are given in Eq. 4.7-4.11 [109], respectively.

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \tag{4.7}$$

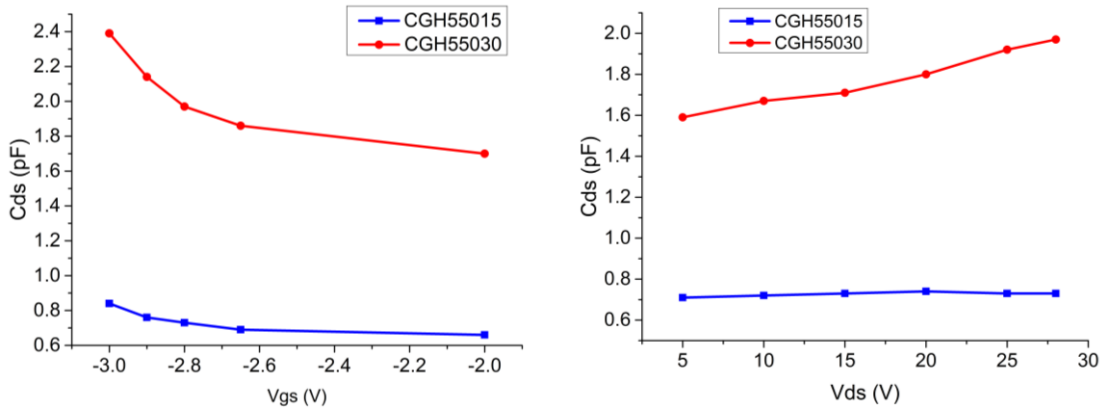
$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) - \omega C_{gd}}{\omega}\left(1 + \frac{\left(\mathrm{Re}(Y_{11})\right)^2}{\left(\mathrm{Im}(Y_{11}) - \omega C_{gd}\right)^2}\right) \tag{4.8}$$

$$R_i = \frac{\mathrm{Re}(Y_{11})}{\left(\mathrm{Im}(Y_{11}) - \omega C_{gd}\right)^2 + \left(\mathrm{Re}(Y_{11})\right)^2} \tag{4.9}$$

$$g_m = \sqrt{\left((\mathrm{Re}(Y_{21}))^2 + \left(\mathrm{Im}(Y_{21}) - \omega C_{gd}\right)^2\right)(1 + \omega^2 C_{gs}^2 R_i^2)} \tag{4.10}$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{22}) - \omega C_{gd}}{\omega} \tag{4.11}$$

Using Eq. 4.7 and Eq. 4.11, $C_{ds} = 0.88$ pF and $C_{ds} = 2.19$ pF have been calculated for CGH55015F1 and CGH55030F2 packaged transistors at 5.8 GHz respectively for typical class AB operation. The value of C_{ds} per watt for GaN HEMTs is low compared to GaAs HEMTs [110], which can be helpful in achieving high power over wider bandwidth with smaller gate peripheries. Fig. 4. 10 (a) shows the variation of C_{ds} with V_{gs} from device pinch-off towards linear transistor operation where ($I_{dq} = 0.4\ I_s$) for $V_{ds} = 28$ V, while Fig. 4. 10 (b) shows the variation of C_{ds} with V_{ds} for $V_{gs} = -2.8$ V; at 5.8 GHz. Accuracy of output capacitances calculated through $[S]$-parameter simulations was confirmed by comparison with output capacitances provided in datasheets, which were at different bias conditions and frequency ($V_{gs} = -8$ V, $V_{ds} = 28$ V, $f = 1$ MHz).



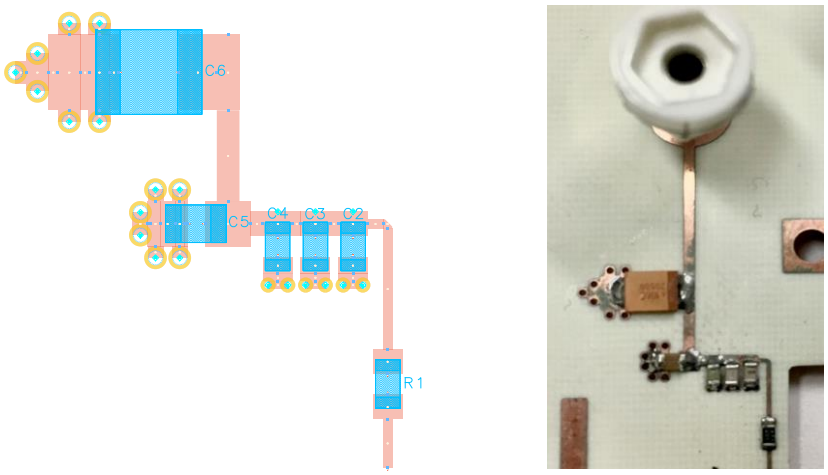
(a) (b)

Fig. 4. 10: Variation of output capacitance (C_{ds}) of CGH55015 and CGH55030 at 5.8 GHz with (a) gate to source voltage (V_{gs}) for $V_{ds} = 28$ V, and (b) drain to source voltage (V_{ds}) for $V_{gs} = -2.8$ V

It can be observed from Fig. 4. 10 (b) that C_{ds} nearly remains constant for CGH55015 and changes slightly (upward slope) for CGH55030 with an increase in drain voltage V_{ds}, for $V_{gs} = -2.8$ V. While, Fig. 4. 10 (a) shows that C_{ds} has a larger value for bias conditions closer to the knee region or pinch-off. Deep class AB, class B, class J and class F amplifiers are generally biased around these regions. General difference in C_{ds} for CGH55015 and CGH55030 transistors under the same bias conditions is due to larger gate periphery of the latter.

4.2.5 Bias Network Design

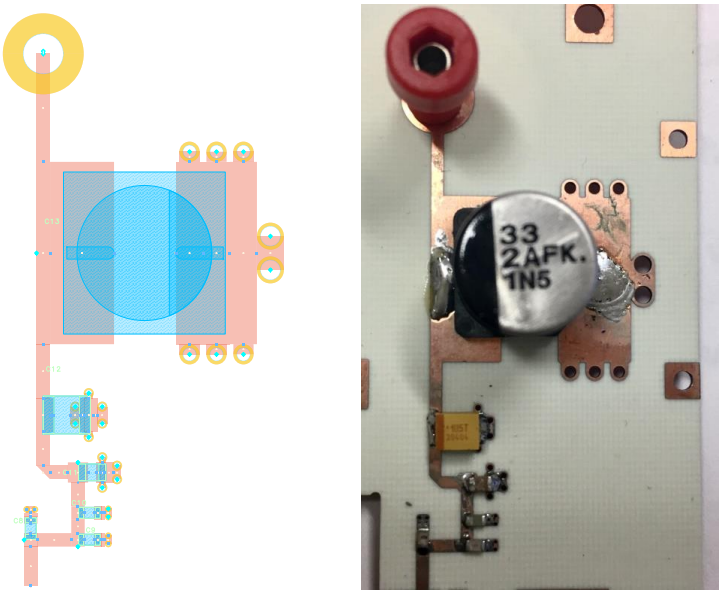
The design of gate and drain bias networks is similar for all classes of power amplifiers discussed in this chapter, due to their similar operating frequencies. However, different decoupling capacitors are required for the two transistors. Since the amplifier circuitry fabricated on RO4350B board will been pasted on an aluminium block using a silver based conductive epoxy, and the transistors will be directly mounted for better heat dissipation; thus, multiple ground vias covering maximum area should be placed in the circuit to provide same ground reference to the decoupling capacitors as the transistors. Theoretically, a large capacitor like 33 μF having a resonant frequency greater than the operating frequency of 5.8 GHz should provide short circuit to all frequencies from DC. However, multiple shunt decoupling capacitors (with a factor of around 10) in terms of their increasing order of capacitances from gate and drain terminals have been used in the bias circuitry. This is being considered because resonant frequencies of capacitors decrease with an increase in their capacitances. The first shunt capacitor towards gate and drain terminal has a value of 18 pF with respect to the operating frequency of 5.8 GHz for CGH55015, while 10 pF for CGH55030. This technique also contributes toward providing stability to the amplifier because of minimal resonance between body inductance of amplifier circuitry and shunt decoupling capacitors in the bias circuitry. In the gate bias circuit, high impedance line has been used which also includes a series 22 Ω resistor. Design variations and analysis showed that better stability and matching is achieved when the bias circuitry is located closer to the transistor's gate terminal. Fig. 4. 11 shows (a) layout and (b) PCB implementation of the gate bias circuitry for the amplifiers. However, it will have different decoupling capacitors for different transistors.



(a) (b)

Fig. 4. 11: Generalised (a) Layout, and (b) PCB implementation of gate bias circuit for amplifiers presented in Chapter 4

The drain bias circuit includes shunt decoupling capacitors and a quarter wavelength transmission line at fundamental frequency to provide short circuit conditions to the second harmonic at the drain terminal and open circuit at the fundamental. Fig. 4. 12 shows (a) layout and (b) PCB implementation of drain bias circuit for the amplifiers. However, it will have different decoupling capacitors for different transistors.



(a) (b)

Fig. 4. 12: Generalised (a) Layout, and (b) PCB implementation of drain bias circuit presented in Chapter 4

4.2.6 Design Considerations for Lumped and Distributed Components

Input and output matching networks and bias circuits are generally designed by using lumped and distributed elements, with both having their advantages and disadvantages with respect to operating frequency, application area, parasitics and dimensions to name a few. It has been discussed in [44] that lumped components are generally suited for low frequency applications. However, high Q-factor resonator and filters operating in microwave frequencies require very small values of inductance which cannot be practically realised using lumped components. Furthermore, parasitics associated with lumped components are generally difficult to model at higher frequencies. For instance, in C band frequencies a capacitor will have an associated resistance and inductance, and will depict behaviour like an RLC circuit that can potentially cause gain roll off or resonance [111]. Thus, special care needs to be taken when having lumped components in the circuit operating at microwave frequencies. Performance of DC block and decoupling capacitors has been modelled and simulated using device models provided by the manufacturers. Distributed elements have been used otherwise, with EM modelling

and optimisation at step discontinuities, bend junctions and where potential parasitic behaviour could arise. Multi-section impedance matching networks, with stepped transmission lines, have also been used in the amplifiers to achieve matching over wider frequency range. This makes the amplifiers less susceptible to performance degradation.

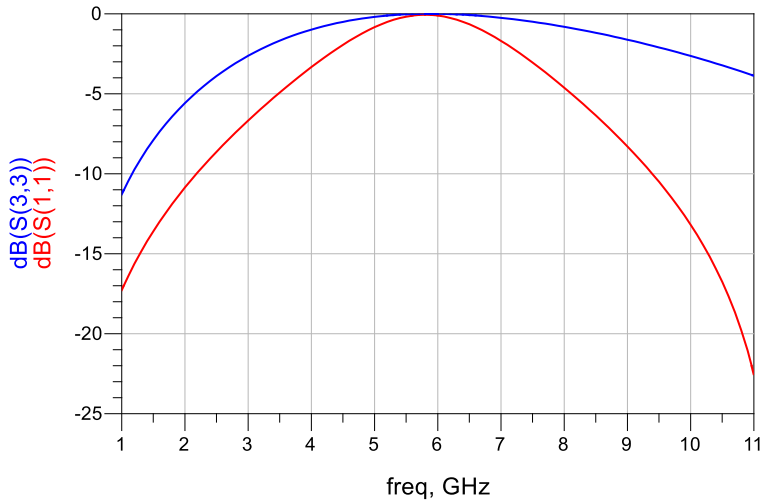


Fig. 4. 13: Comparison between open circuit (red line) and radial stubs (blue line)

It has been observed that Radial stubs (compared to open circuit stubs) provide low impedance values over a broader frequency range due to large fringing effects at their ends, matching over wider bandwidth, non-repeatable behaviour towards harmonics, smaller footprint, and the ability to perform better tuning. Fig. 4. 13 shows comparison between open circuit and radial stubs. These properties are especially important in class F amplifiers, where slight variation in transmission line could lead to a shift in harmonic impedances and performance degradation. Radial stubs have also been observed to provide broader open circuit bandwidth to higher order harmonics compared to open circuit stubs. Thus, radial stubs have been used in various parts of amplifier circuits in place of open circuit stubs.

4.2.7 Layout and Fabrication

Design of the amplifiers has been performed in hierarchical manner in terms of various sub-networks like harmonic matching network, input and output matching networks and bias networks which were shown in Fig. 4. 2. These sub-networks and lumped components were EM simulated using Momentum simulator where models of Rogers RO4350B laminate (shown in Fig. 4. 14), and respective lumped components were imported. Large signal analysis and optimisation was performed after these sub-networks were connected to achieve required performance in terms of output power, efficiency and drain *IV* waveforms.

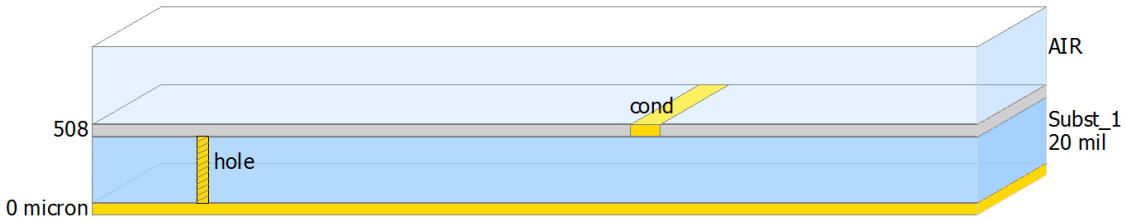


Fig. 4. 14: RO4350B laminate model for layout in Momentum ADS

Hierarchical schematics of class F amplifier with all sub-networks, lumped components and transistor has been shown for illustration in Fig. 4. 15. Layout was directly generated from the schematics with all sub-networks falling in place. PCB boundary has been defined using case dimensions layer, while silkscreen and packages' layers show the placement of individual passive components. The transistor was routed directly onto the mounting block for better heat dissipation and to provide the same ground level as decoupling capacitors, a slot was included in the layout for this purpose.

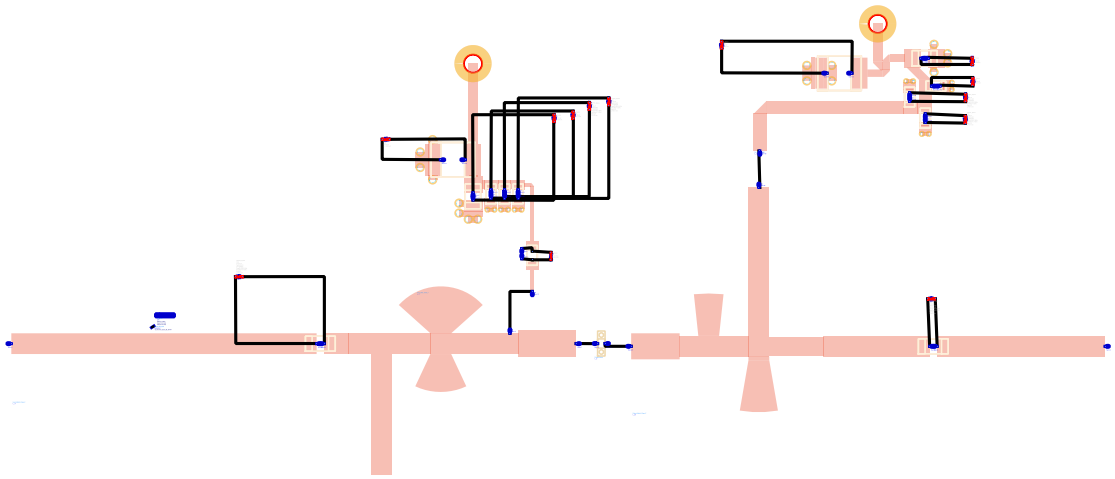


Fig. 4. 15: Hierarchical schematics of class F amplifier

Layout of class AB, class F and multistage amplifiers have been shown in Fig. 4. 16, Fig. 4. 17 and Fig. 4. 18, respectively.

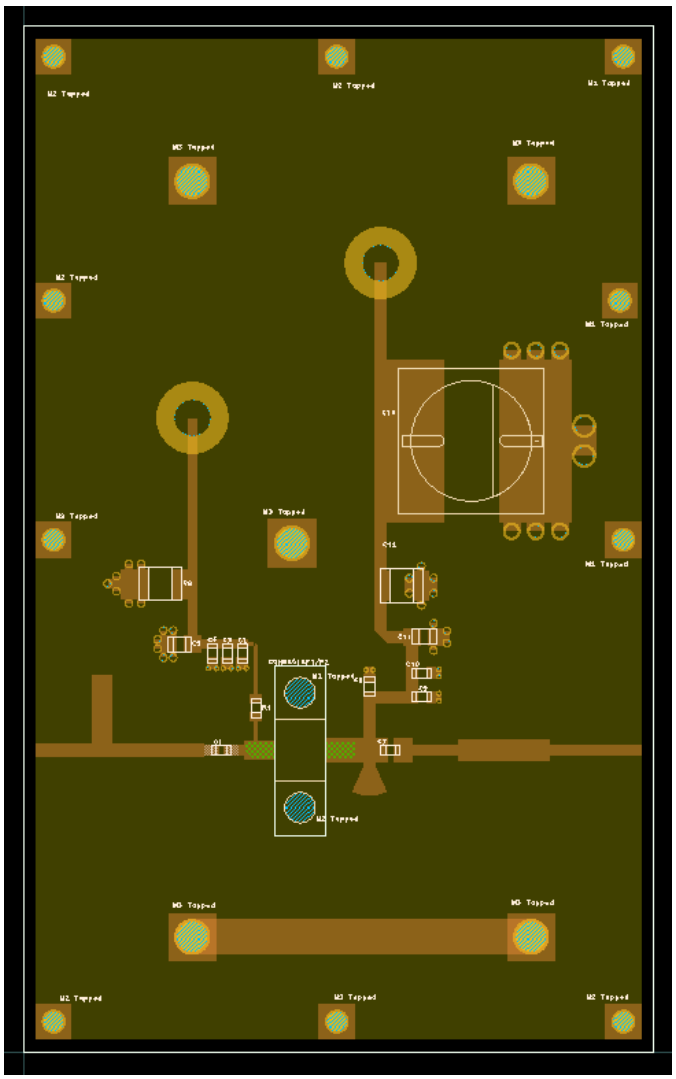


Fig. 4. 16: Layout of class AB amplifier in Momentum ADS

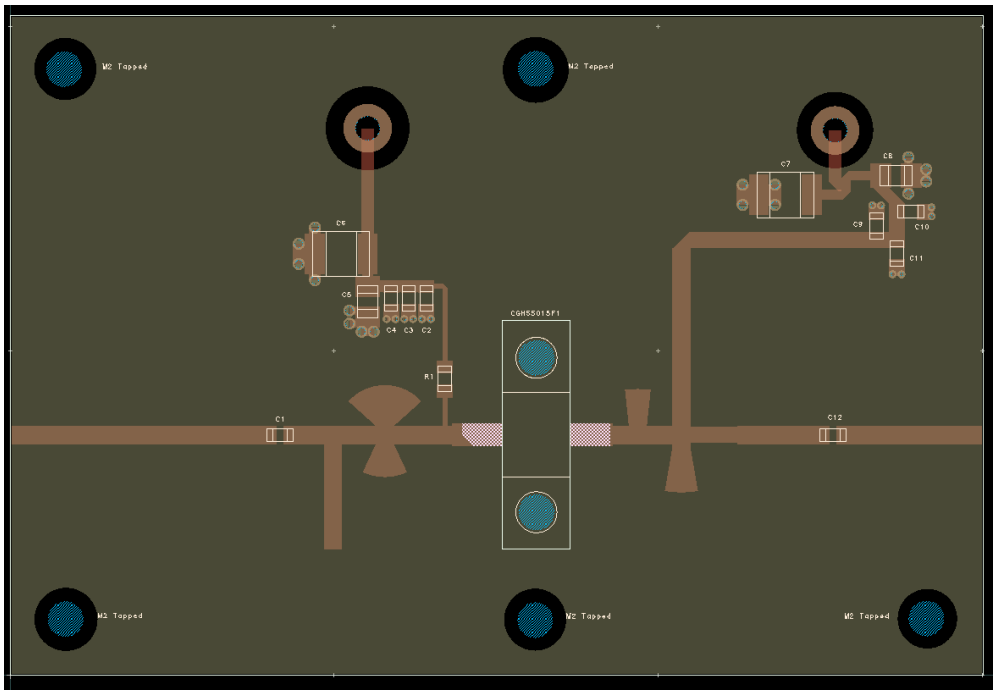


Fig. 4. 17: Layout of class F amplifier in Momentum ADS

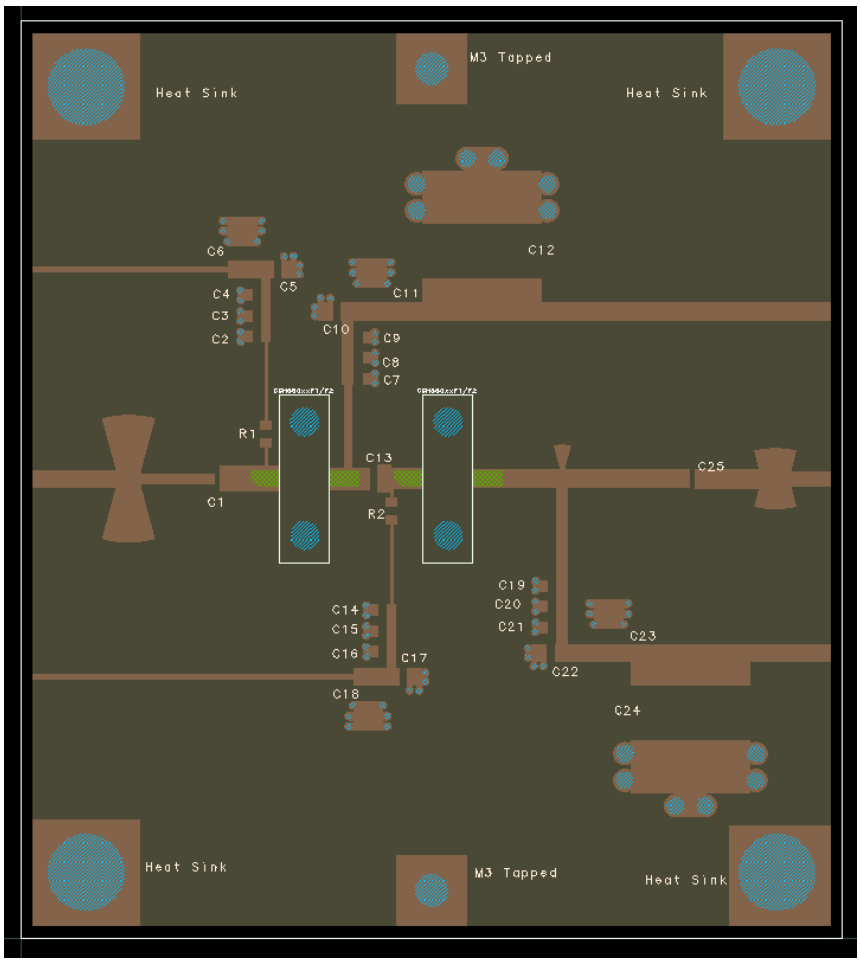


Fig. 4. 18: Layout of multistage high efficiency amplifier in Momentum ADS

Due to limitations of PCB processing facility at the University of Manchester, gerber and drill files directly generated from Keysight's ADS were not accepted. Thus, the layout was converted to Altium Designer for PCB processing. Fig. 4. 19 shows Altium layout for class F amplifier. The layout was checked for any discrepancies that might have been introduced during conversion. However, apart from the positioning of ground via holes, the design was converted accurately.

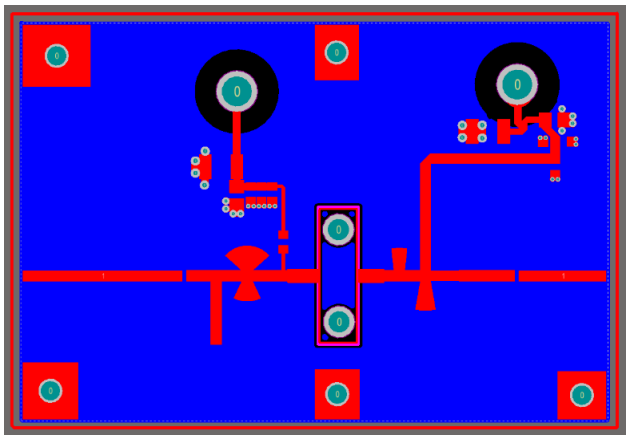
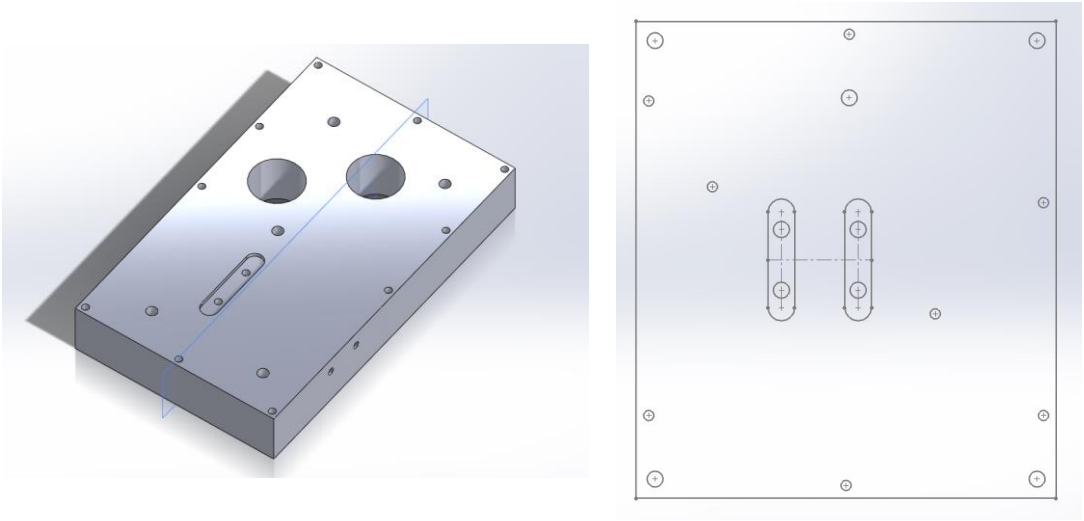


Fig. 4. 19: Layout of class F amplifier in Altium Designer Studio

Amplifier boards were processed, and components were soldered in compliance with the guided soldering temperatures. For effective heat dissipation and mounting base for transistors and PCB; aluminium blocks having a thickness of $\frac{1}{2}$ inches were designed in SolidWorks 3D CAD software. Fig. 4. 20 shows (a) 3D view of aluminium mounting block design for class AB amplifier and (b) top view of aluminium mounting block design for multistage amplifier.



(a) (b)

Fig. 4. 20: (a) 3D view of aluminium mounting block design for class AB amplifier and (b) top view of aluminium mounting block design for multistage amplifier

Amplifier PCBs were bonded to respective aluminium blocks using CircuitWorks CW2400 silver based conductive epoxy, and the assemblies were finally bolted to a heatsink. Fig. 4. 21 shows final assembly of multistage high efficiency power amplifier.

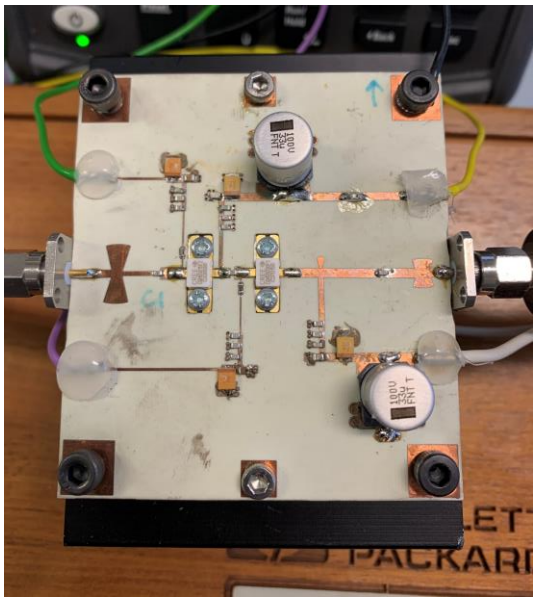


Fig. 4. 21: Final assembly of multistage high efficiency amplifier

4.2.8 Measurement Setup

Measurement devices used to perform small and large signal measurements of power amplifiers have been shown in Fig. 4. 22 to Fig. 4. 25. Fig. 4. 22 shows HP 8562A (026) spectrum analyser that was used to identify any oscillations during power up of amplifiers in safe mode, including out of band low frequency oscillations. Fig. 4. 23 shows Keysight's FieldFox N9918A network analyser that was used for small signal [S]-parameter measurements of power amplifiers and matching circuits. Fig. 4. 24 shows Marconi Instruments microwave test set 6200 that was used to generate up to 12.5 dBm CW microwave power at 5.8 GHz, however, gain amplifiers were used to provide enough input power level to drive the power amplifiers as per their requirements. Fig. 4. 25 shows Agilent's E4418B power meter that was used for power measurements.

The amplifiers were powered up in safe-mode with the gate pinched off at $V_{GS} = -4$ V and gate current compliance set to $I_G = 7$ mA. Gate current was ~ 0 mA. In the next step, drain voltage that was set to ($V_{DS} = 28$ V) and compliance to ($I_D = 400$ mA) was switched on. At this stage both drain and gate currents were ~ 0 mA. The channel was switched on by moving gate voltage from -4V towards 0 V slowly. A rise in I_D was observed when V_{GS} approached -3.1 V as expected, and V_{GS} was adjusted to achieve quiescent drain current I_{DQ} for respective power amplifiers. Oscillations were checked throughout the safe-mode powering up procedure and none were observed in the spectrum analyser's range of 9 kHz to 26.5 GHz. A similar powering up procedure was performed during [S]-parameters and power measurements. Fig. 4. 26 shows block diagram for power measurements.

Fig. 4. 22: HP 8562A (026) spectrum analyser

Fig. 4. 23: Keysight's FieldFox N9918A portable network analyser

Fig. 4. 24: Marconi Instruments microwave test set 6200

Fig. 4. 25: Agilent's E4418B power meter

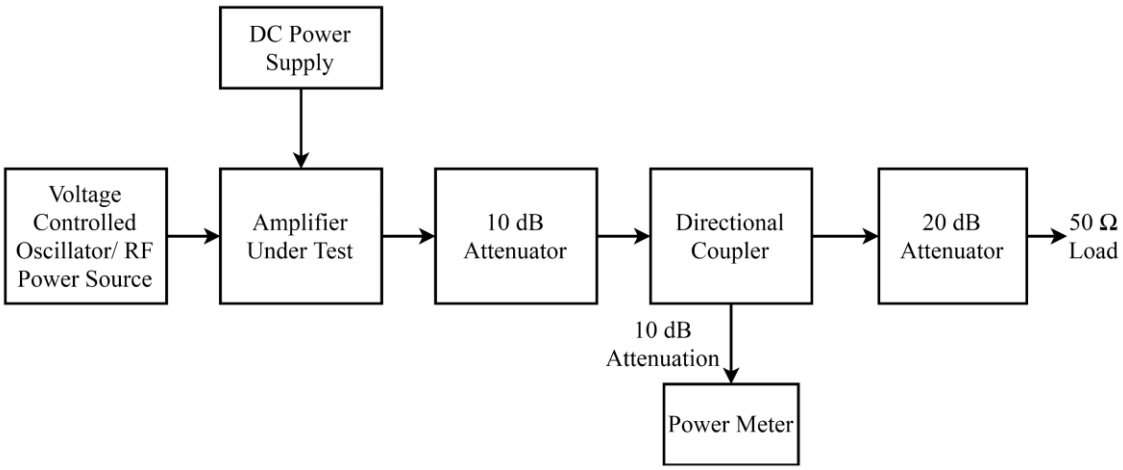


Fig. 4. 26: Block diagram for power measurements

4.3 Design and Analysis of Class AB Amplifier

4.3.1 Introduction

Power amplifiers are an important component of microwave systems and compromise is often made according to respective application areas in terms of output power, efficiency, gain, linearity, noise performance and size of the device. Class AB amplifiers are reduced conduction angle amplifiers that lie between class A and class B amplifiers with conduction angles ranging between 180° and 360°, thus, performance is also between linear (class A) and high efficiency (class B) amplifiers. Designers are often given choice to decide upon the conduction angle in terms of required performance with an appropriate selection of quiescent bias point that were shown in Fig. 4. 4. For instance, conduction angles closer to 360° in the range defined above will provide more linear operation compared to conduction angles closer to 180°, however, at the cost of efficiency. Nevertheless, high efficiency class AB power amplifiers with decent linearity have been demonstrated in literature, few of which were discussed in Chapter 3. Class AB power amplifier presented in this section has conduction angle closer to class B amplifier to achieve high output power with decent efficiency, as linearity was not a concern in the intended microwave surgical devices' application area; where CW microwave power was required with high efficiency. The development was also intended to provide operational and design understanding of class AB amplifiers which would act as steppingstone towards the development of class AB amplifiers on MMIC that will be presented in Chapter 6 of this thesis. Another objective was to overcome limitations of microwave power source (Marconi Instruments microwave test set 6200) at the labs accessible to the author in University of Manchester, where an input power level of only 12.5 dBm could be generated. Class F and multistage amplifiers presented later in this chapter require input power drive level greater than 36 dBm to operate in the saturation region to produce CW power over 43 dBm or 20 W with high efficiency. This way, class AB amplifier presented herein would also act as gain amplifier in series with the microwave power source to provide required input power drive levels.

This section on the development of class AB amplifiers has been organised as follows. Section 4.3.2 presents analysis of DC characteristics, and selection of suitable bias point for CGH55015 transistor to achieve class AB operation. It also highlights the effect of output capacitance towards providing short circuit termination to second harmonic component in addition to a quarter wavelength transmission line in the drain bias network. Section 4.3.3 presents load and source pull analysis for selection of optimum source and

load impedances and their comparison with suggested impedances from the device manufacturer. Section 4.3.4 presents discussion on the design of optimum source and load networks, followed by Section 4.3.5 where overall schematics of the amplifier have been presented. Towards the end, Section 4.3.6 presents simulation and measured results and corresponding analysis.

4.3.2 DC Characteristics and Optimum Bias Point

To identify optimum bias point and loadline for class AB operation, DC *IV* simulations were performed using non-linear device model provided by Cree/Wolfspeed for CGH55015 transistor. Fig. 4. 27 shows simulated DC *IV* characteristics, where V_{gs} has been swept from – 3 V to 0 V, with steps of 0.2 V, and V_{ds} has been swept from 0 to 32 V with steps of 1 V. Optimum bias points for class A, class B and class AB operation have been shown with letters A, B and AB respectively.

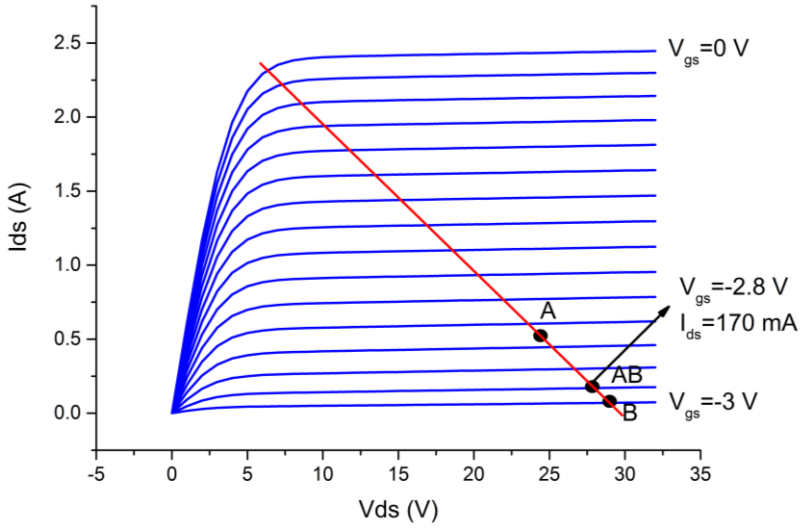


Fig. 4. 27: DC IV curves of CGH55015 GaN HEMT showing optimum bias point for class AB operation

The suggested maximum drain current for reliable transistor operation $I_{max} = 1.5$ A [104], however, the chosen $I_{ds} \approx 0.11\, I_{max}$ for class AB operation, which is closer to class B operation but cannot be classified as deep class AB where $I_{ds} \approx 0.05\, I_{max}$. Classical class AB operation requires short circuit termination at the second harmonic component, thus an important consideration in terms of DC *IV* characteristics is the device's output capacitance at the selected bias point. It can be observed from Fig. 4. 10 that $C_{ds} \approx 0.77$ pF at the chosen bias conditions which is not high enough to provide second harmonic short circuit, thus, a quarter wavelength transmission line in the bias network would be placed close to the drain terminal to effectively provide short circuit conditions.

4.3.3 Source and Load Pull

The concept of source and load pull was discussed in literature review and its significance to identify optimum load and source impedances at various regions on the Smith chart was emphasized in power amplifier design. Source and load pull simulations were performed in Keysight's ADS using non-linear device model provided by Cree/Wolfspeed, which has the capability to predict performance at higher order harmonics. Short circuit conditions at the second harmonic component is required in class AB amplifier operation, thus, appropriate second harmonic short was reflected in the simulation setup. Load pull simulation was performed to identify optimum load impedance, followed by source pull simulation to identify optimum source impedance, based on the load impedance. However, multiple iterations of both was performed until optimised impedances were obtained. In this discussion, source pull and load pull simulations will be called load pull simulations. Fig. 4. 28 shows results of load pull simulation at bias conditions defined in the preceding section and 35 dBm input power.

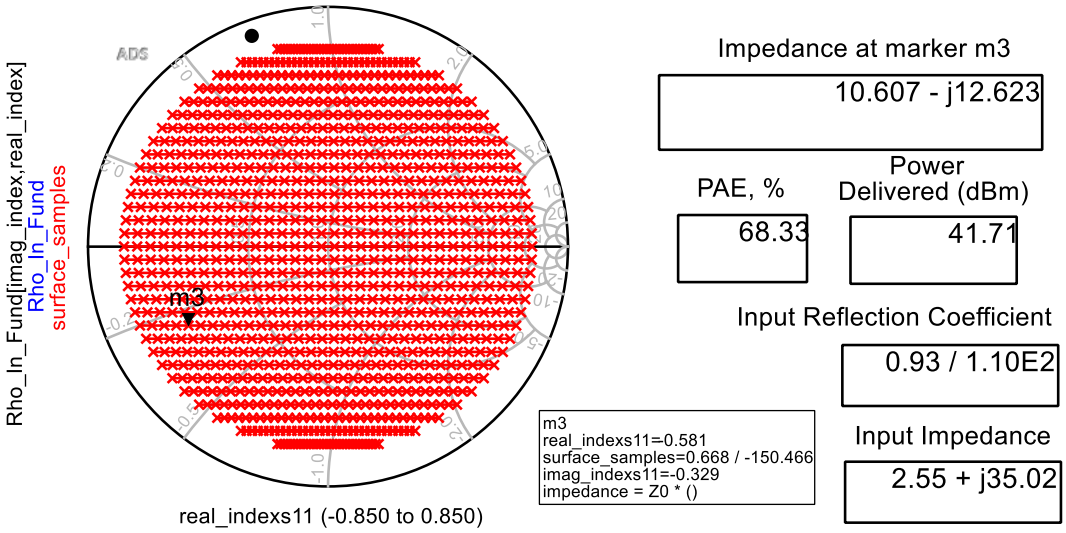


Fig. 4. 28: Load pull simulation results for class AB operation for CGH55015 biased at $V_{DS} = 28$ V and $I_{DS} = 170$ mA with 35 dBm input power

Impedance shown by marker m3 in Fig. 4. 28 represents selected load impedance which is in stable region of the transistor (discussed in Section 4.2.3). Selection of optimum load and source impedances for high efficiency power amplifiers is governed by factors including stable regions, output power and PAE contours for different levels of input power. Fig. 4. 29 shows these contours on the Smith chart, markers m1 and m2 represent impedance points on PAE and output power contours, respectively; which are in the vicinity of optimum impedance shown with marker m3 in Fig. 4. 28.

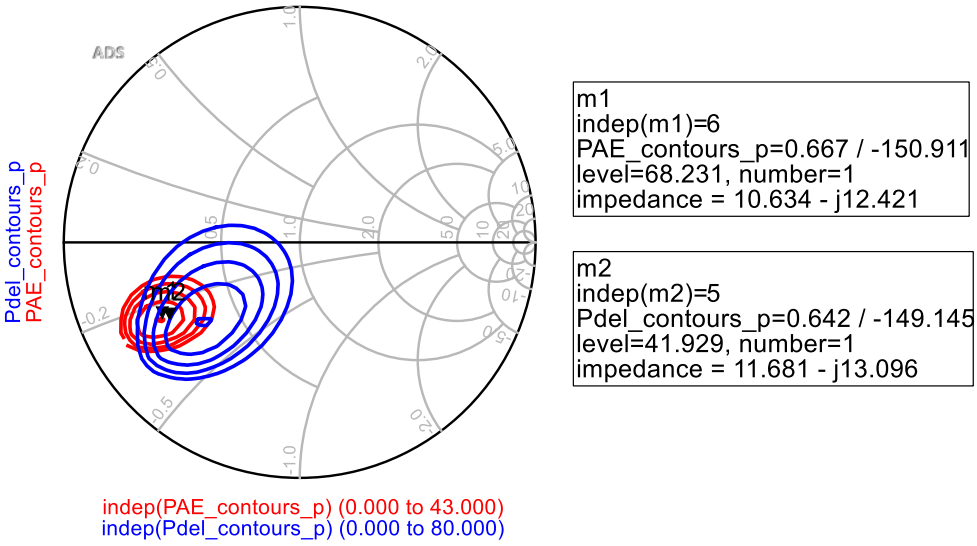


Fig. 4. 29: Output power and PAE contours on the Smith chart under class AB bias conditions

It needs to be mentioned that higher output power and PAE are indicated by inner circles on their respective contours and the selection of optimum load impedance should ideally lie on an intersection point between inner circles. 42.4 dBm maximum output power and 68.3 % maximum PAE was indicated by load pull simulations. However, PAE was prioritised and compromise was made to select an impedance point shown by marker m1 in Fig. 4. 28 which indicates 68.3 % PAE and 41.7 dBm output power. These are ideal values and efforts would be made to achieve close to this performance through design techniques and optimisation of the amplifier.

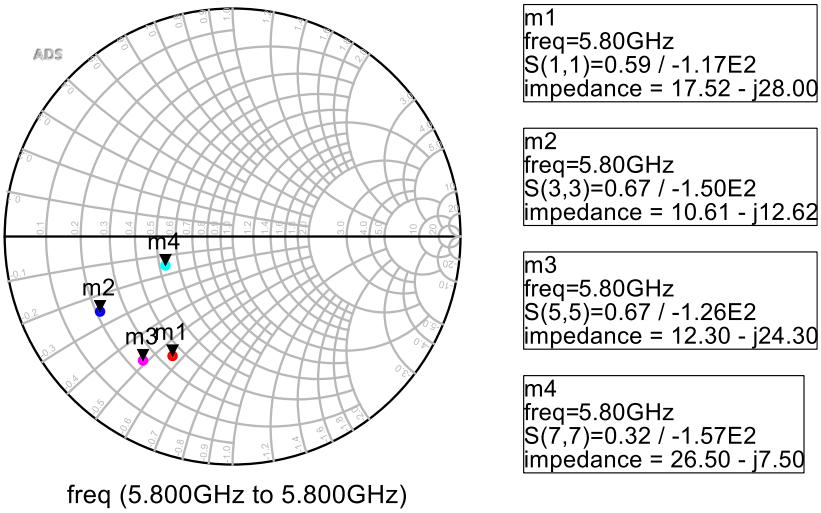


Fig. 4. 30: Load and source impedances from load pull simulations and datasheet

Fig. 4. 30 shows comparison between load and source impedances obtained through load pull simulations and those provided in the datasheet; markers m1 and m2 represent source

and load impedances from load pull simulations, and m3 and m4 represent source and load impedances from the data sheet. However, suggested values in the data sheet are from demonstration amplifier that has been optimised to achieve linear operation under mid class AB bias conditions.

4.3.4 Design of Input and Output Matching Networks

Source and load impedances obtained from load pull simulations for high PAE and output power were used to design input and output matching networks. Second harmonic short circuit condition is provided at the drain terminal by means of quarter wavelength transmission line. This was incorporated in drain bias network, as output capacitance of the transistor $C_{ds} \approx 0.77$ pF isn't high enough to provide short circuit to the second harmonic component.

Input Matching Network

Fig. 4. 31 shows schematics for input matching network of class AB amplifier.

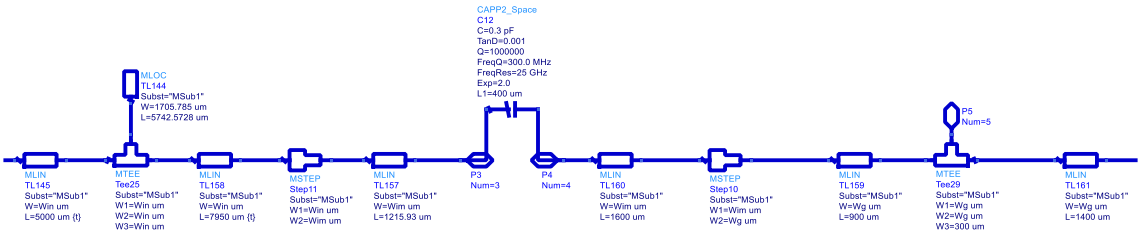


Fig. 4. 31: Input matching network for class AB amplifier

Low impedance transmission lines and open circuit stub (closer to the input port) have been used in the input matching network; while DC block capacitor (0.3 pF) is the only lumped component, which was EM simulated using respective model. Parametric EM optimisation was performed with the model of RO4350B laminate to achieve the required source impedance. However, when it was simulated with the gate bias network (discussed in Section 4.2.5), impedance transformation was observed at the fundamental harmonic due to small length of high impedance gate bias line between gate terminal and the first decoupling capacitor. Further optimisation of input matching network was performed, to achieve required source impedance at the gate and 50 Ω at the input port. An important point also considered was gate pad width and length, and soldering footprint. These were incorporated in input matching network to achieve accurate impedance at the gate. Fig. 4. 32 and Fig. 4. 33 show layout and fabricated input matching network on RO4350B board, respectively.

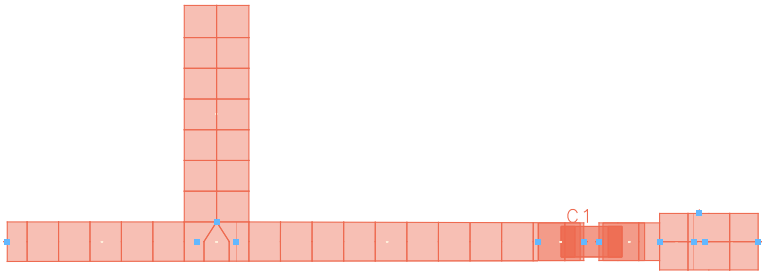


Fig. 4. 32: Layout of input matching network of class AB amplifier corresponding to the distributed elements shown in Fig. 4.31

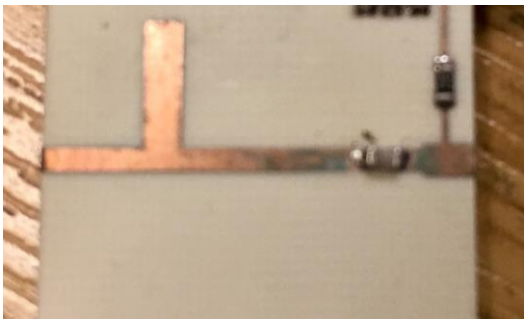


Fig. 4. 33: Fabricated input matching network of class AB amplifier on RO4350B board

Output Matching Network

Stepped transmission lines and 0.3 pF DC blocking capacitor have been used in the output matching network to provide required load impedance at the drain terminal. Quarter wavelength transmission line in drain bias network effectively provides short circuit to second harmonic component at the drain, and open circuit at fundamental frequency to the bias line. However, drain pad, soldering footprint and short length of transmission line between current generator plane and quarter wavelength line causes rotation of impedance around the Smith chart. This has been catered through a radial stub ($\frac{\lambda}{12}$) opposite to quarter wavelength line to effectively provide short circuit to second and third harmonics at the extrinsic drain. Fig. 4. 34 shows schematics of output matching network.

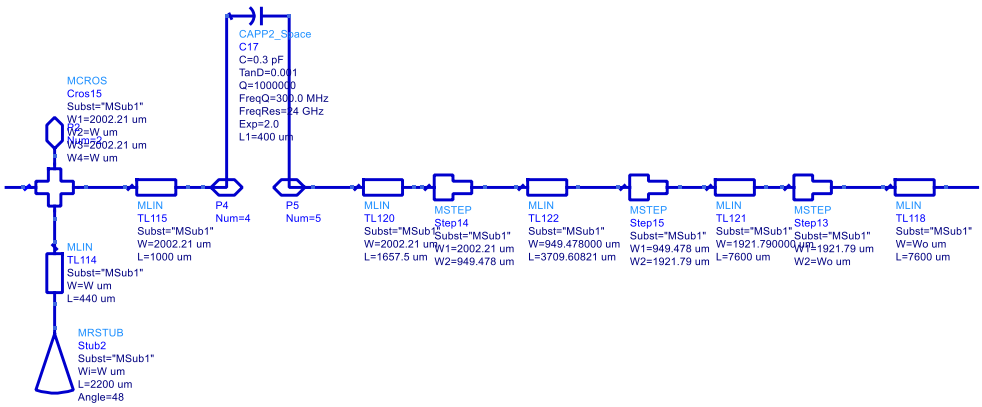


Fig. 4. 34: Output matching network of class AB amplifier

EM simulations of output matching and drain bias network were performed using Momentum simulator followed by parametric EM optimisation. Fig. 4. 35 and Fig. 4. 36 show layout and fabricated output matching network on RO4350B board, respectively.

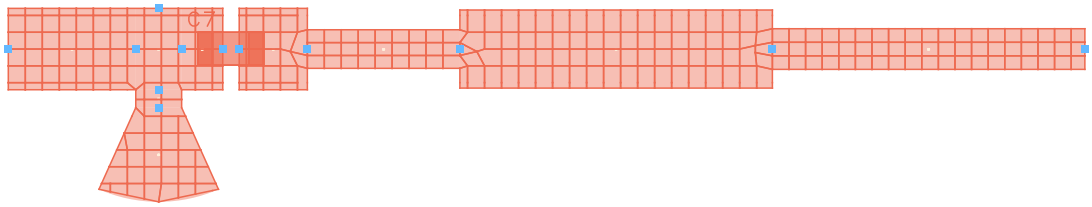


Fig. 4. 35: Layout of output matching network of class AB amplifier

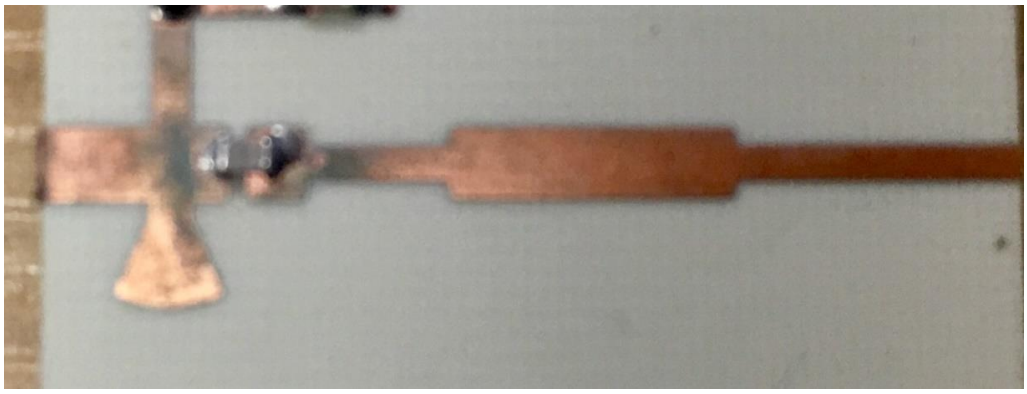


Fig. 4. 36: Fabricated output matching network of class AB amplifier on RO4350B laminate

Input and output matching networks showed high Q-factors which could provide good matching with 50 Ω input and output ports with $S_{11} < -20$ dB.

4.3.5 Schematics of Class AB Amplifier

Final schematics and processed class AB amplifier have been attached as Annex B.

4.3.6 Results and Analysis

This section presents various small and large signal simulation and measurement results of class AB amplifier and corresponding analysis. Simulation results are based on non-linear transistor model and EM simulated networks, including bias networks and lumped component elements, using Momentum simulator. Small signal $[S]$-parameter and large signal power measurements have been obtained through the measurement setup and procedure outlined in Section 4.2.8.

Stability Analysis

Source and load networks of class AB amplifier were designed with impedances away from unstable regions identified in Section 4.2.3; however, unconditional stability was achieved through a 22 Ω shunt resistor in the gate bias line and multiple decoupling

capacitors. Stability factor curve shown in Fig. 4. 37 indicates that the amplifier is unconditionally stable across the entire frequency band and has a value of 2.6 at 5.8 GHz. Some possible oscillatory behaviour at out of band low frequencies around 700 MHz can be observed with sharp dips; however, oscillations were checked during safe-mode powering up procedure and none were identified, which confirms stable operation.

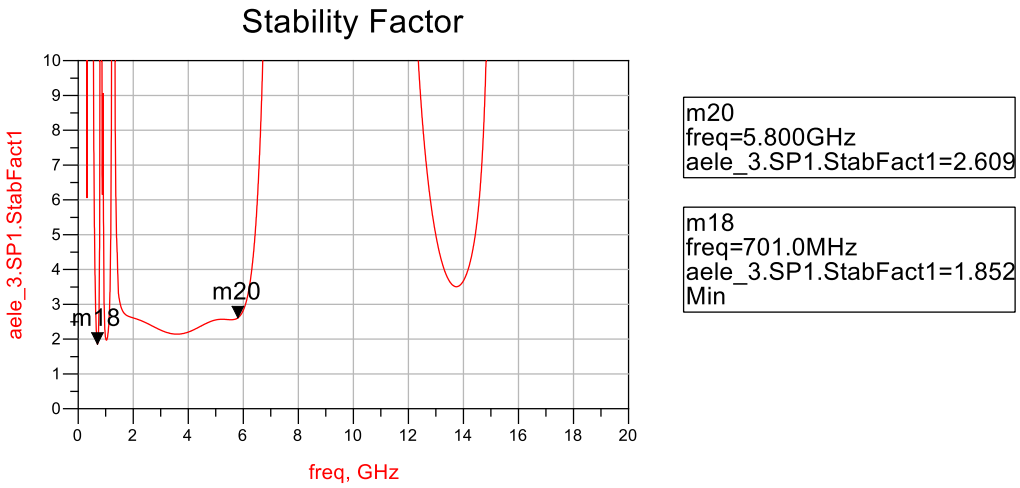
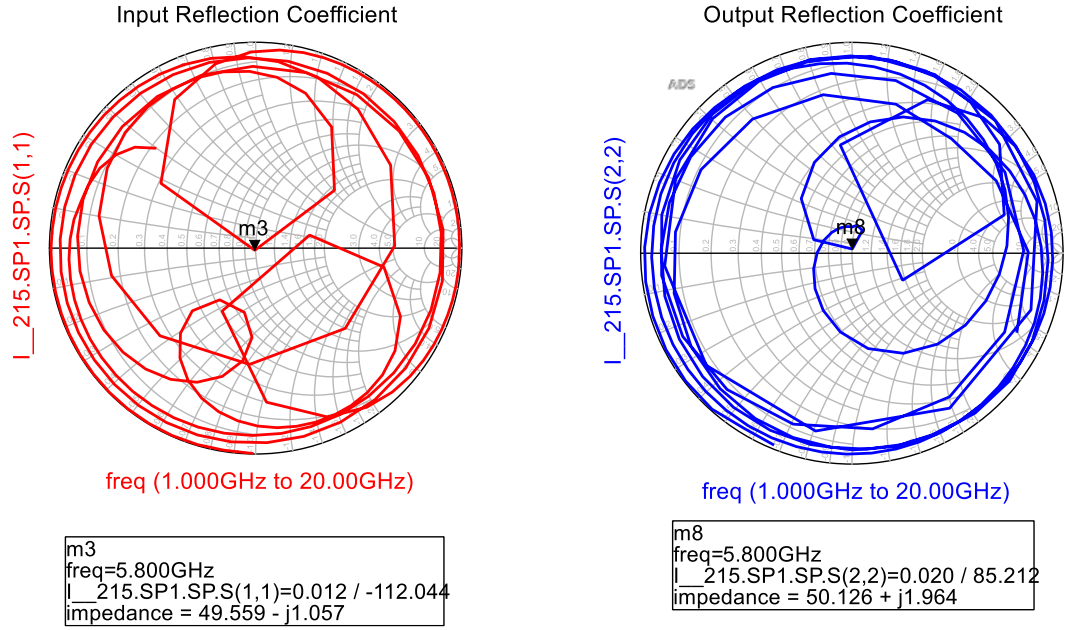


Fig. 4. 37: Stability factor for class AB amplifier for CGH55015

Input and output reflection coefficients of the amplifier have been shown in Fig. 4. 38, which indicates decent match to 50 Ω input and output ports, however, resonance can be observed in the output reflection coefficient near 5.8 GHz which can be attributed to the existence of unfiltered higher order harmonics in output waveform.



(a) (b)

Fig. 4. 38: (a) Input and (b) output reflection coefficient of class AB amplifier for CGH55015

Small Signal Behaviour

Small signal characteristics of the amplifier have been optimised for CW operation at 5.8 GHz, while suggested frequency range of operation according to data sheet is 5.5-5.8 GHz [104]. Small signal gain (S_{21}) and input reflection coefficient (S_{11}) have been presented in Fig. 4. 39.

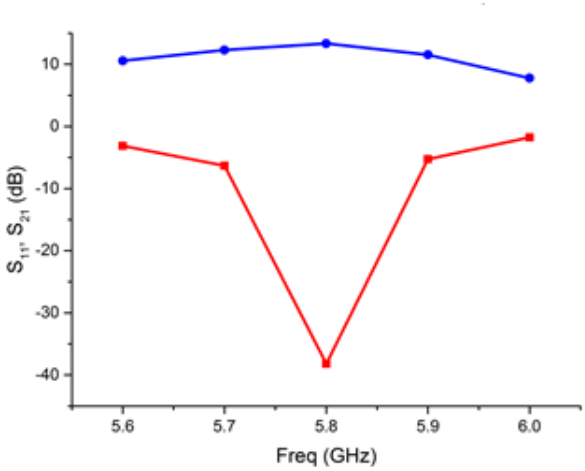


Fig. 4. 39: Simulated small signal [S] parameters of class AB amplifier, the red line defines S_{11}, while blue line describes S_{21}

Large Signal Analysis

Class AB power amplifier presented herein has been biased at $V_{ds} = 28$ V and $V_{gs} = -2.8$ V for analysis of large signal behaviour in terms of output power, gain and PAE as a function of the input power; simulated results have been shown in Fig. 4. 40.

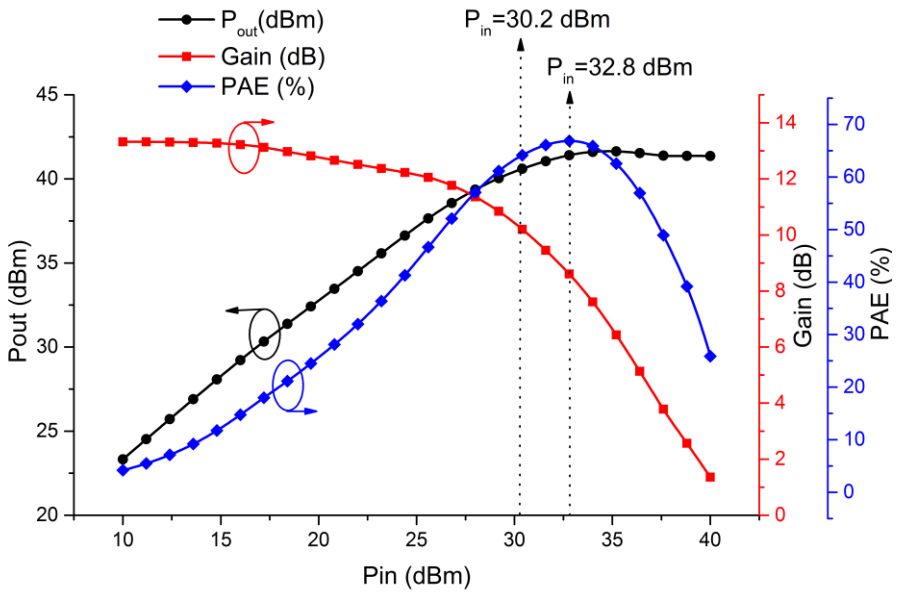


Fig. 4. 40: Large signal simulation results of class AB amplifier showing output power, gain and PAE as a function of the input power, biased at $V_{ds} = 28$ V and $V_{gs} = -2.8$ V

Simulation results indicate that the amplifier achieves 3 dB gain compression at $P_{in} =$ 30.2 dBm where the output power and PAE are 40.52 dBm and 63.72 %, respectively. Highest efficiency is achieved at deeper saturation level where $P_{in} = 32.8$ dBm, $P_{out} =$ 41.4 dBm and $PAE = 63.72$ %. Measured curves of output power, gain and PAE as a function of the input power have been shown in Fig. 4. 41, however, these measurements are shown over a smaller range of input power levels, i.e. 20 dBm to 36 dBm with 0.4 dBm step. Comparison between simulated and measured output power and PAE as a function of input power, respectively have been illustrated in Fig. 4. 42 and Fig. 4. 43.

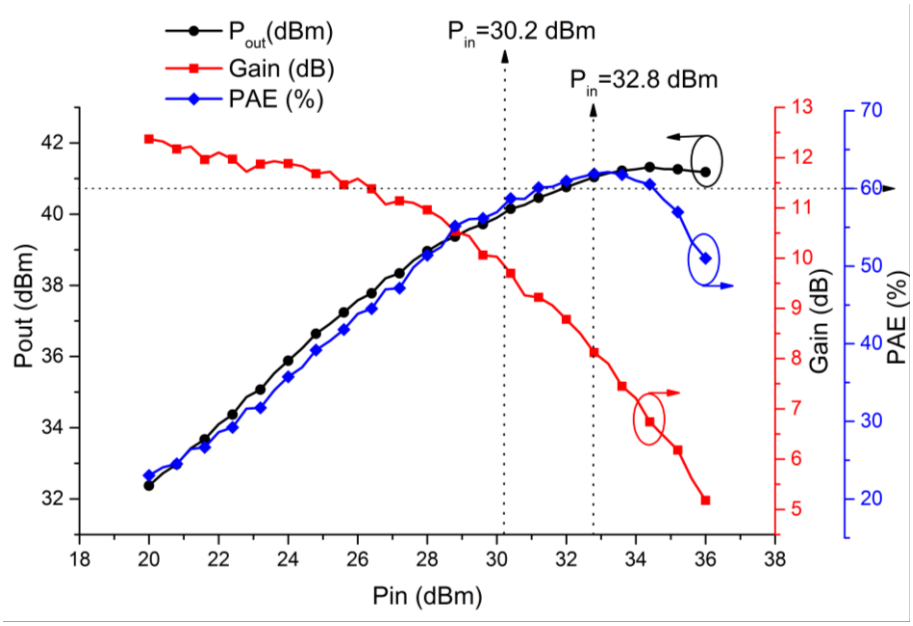


Fig. 4. 41: Measured large signal results of class AB amplifier showing output power, Gain and PAE as a function of the input power, biased at $V_{ds} = 28$ V and $V_{gs} = -2.8$ V

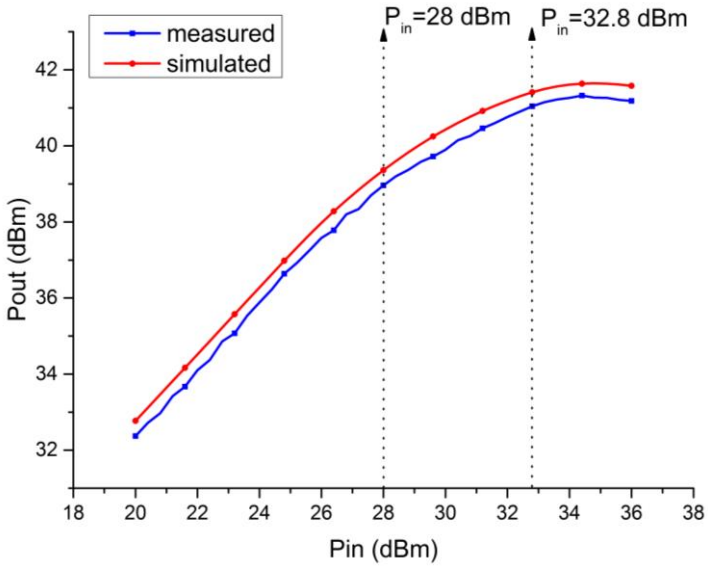


Fig. 4. 42: Comparison between simulated and measured output power as a function of the input power for class AB amplifier, biased at $V_{ds} = 28$ V and $V_{gs} = -2.8$ V

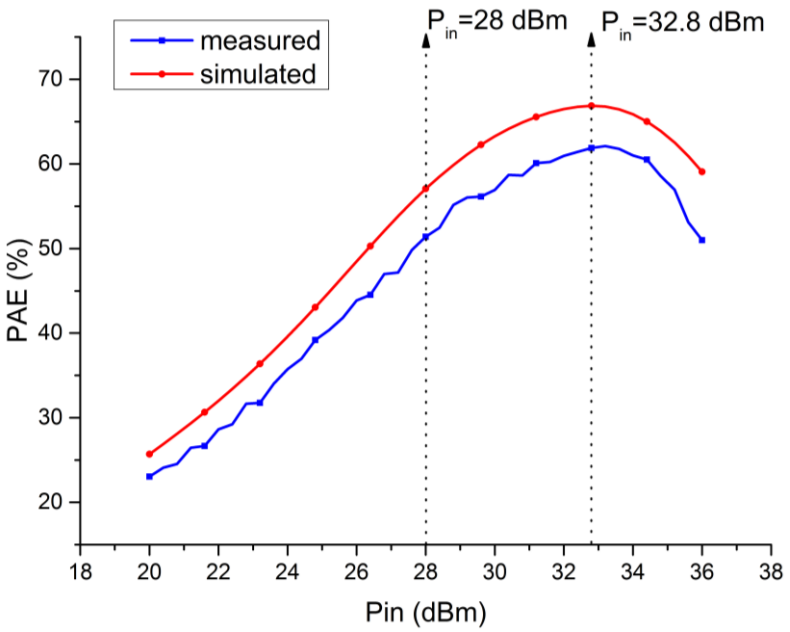


Fig. 4. 43: Comparison between simulated and measured PAE as a function of the input power for class AB amplifier, biased at $V_{ds} = 28$ V and $V_{gs} = -2.8$ V

Measured results indicate that the amplifier provides greater than 40.5 dBm output power with over 60 % PAE for input power levels between 31.2 dBm and 34.4 dBm with a maximum PAE of 62.1% with 41.15 dBm output power. Sharp gain roll-off occurs after the input power is increased beyond 32.8 dBm, however, output power and PAE are 41 dBm and 61.9 % respectively at this point. Measured results shown in Fig. 4. 42 suggest that the amplifier achieves gain compression sooner which is greater than simulated results, especially in the saturation region between $P_{in} = 28$ dBm to 32.8 dBm. Average difference between measured and simulated results of the output power is around 0.42 dB with a maximum difference of 0.53 dB at 30 dBm input power. This can be attributed to inaccuracies in the fabrication process and non-linear device models; however, the trends are much similar between simulated and measured results.

4.4 Design and Analysis of Class F Amplifier

4.4.1 Introduction

Class F amplifiers are high efficiency amplifiers that take advantage of non-linearities in the saturation region with appropriate load and source termination networks that provide even and odd harmonic trapping and waveform shaping at transistor's intrinsic terminals. The transistor behaves as a switch with square voltage and half rectified current waveforms at device's gate and drain terminals to achieve theoretical efficiency of 100 % with minimum overlapping between the two waveforms. Thus, class F amplifiers can be described as a hybrid between class E and class B amplifiers due to switching nature of the transistor with a quiescent point and conduction angle in deep class AB or class B region. Detailed theoretical analysis and review of class F amplifiers was presented in Chapter 3, however, discussion in this section will be focused on design aspects in terms of current and voltage waveforms and load and source termination networks at the fundamental frequency and its higher order harmonics. Generalised amplifier structure presented in Fig. 4. 2 will be followed in the design with fundamental and harmonic trapping networks at transistor's gate and drain terminals to provide short circuit and open circuit conditions to even and odd harmonics, respectively.

This section on the development of class F amplifiers has been organised as follows. Section 4.4.2 presents analysis of DC characteristics, elliptical load line, and selection of suitable bias point for CGH55015 transistor to achieve class F operation. Section 4.4.3 highlights load and source pull analysis for selection of optimum source and load impedances at the fundamental frequency corresponding to short and open circuit higher order harmonics up to the third harmonic. Section 4.4.4 presents discussion on the design of waveform shaping networks, followed by Section 4.4.5 where design of fundamental matching network has been discussed. Towards the end, Section 4.4.6 will present simulation and measurement results and corresponding analysis.

4.4.2 DC Characteristics and Optimum Bias point

Fundamental limitation of transconductance amplifier is that the voltage waveform is kept purely sinusoidal, while the current waveform is shaped differently through an appropriate selection of conduction angle or bias point. When the conduction angle is 180°, current only conducts during half a cycle. However, if the voltage waveform is not kept sinusoidal and both waveforms are engineered in a manner that the product of voltage and current remains very low or zero during most of the transistor's operation, then much higher values of efficiency may be attained. Fig. 4. 44 shows DC *IV*

simulations of CGH55015 transistor that were performed using non-linear device model provided by Cree/Wolfspeed. V_{gs} has been swept from -3 V to 0 V with steps of 0.2 V, and V_{ds} has been swept from 0 to 32 V with steps of 1 V. Optimum bias points for class F amplifier has been selected ($V_{GS} = -3$ V, $I_{DS} = 69$ mA and $V_{DS} = 28$ V) in class B bias point (or deep class AB region), such that $I_{DS} \approx 0.046\, I_{max}$, where $I_{max} = 1.5$ A according to the device's datasheet. Optimum bias points for class A and class B amplifiers have been shown for comparison which correspond to the maximum gate voltage $V_{GS} = -2.3$ V suggested in device's datasheet [104].

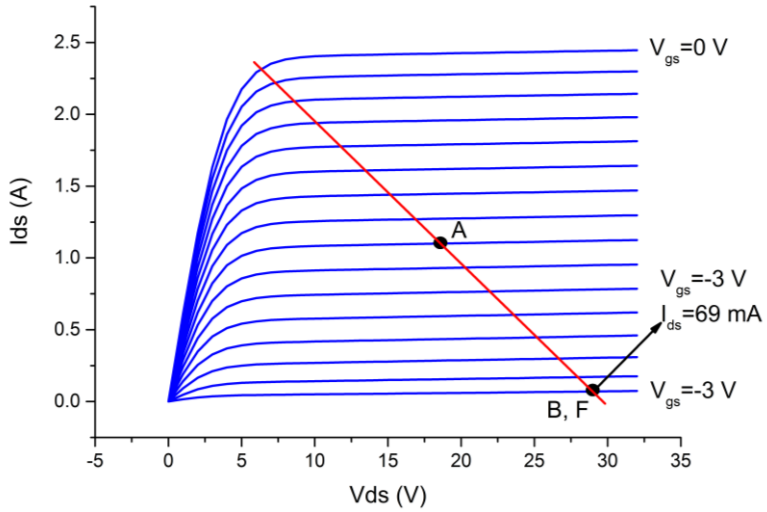


Fig. 4. 44: DC IV curves of CGH55015 GaN HEMT showing optimum bias point for class F operation

The quiescent bias point has been chosen to attain half rectified current waveform and would generate third order current harmonics by clipping of the waveform when high enough input signal level swings across the knee region. The loadline can be represented in an elliptical manner of low current/high voltage and high/low voltage regions such that the product between them remains low for reduced DC power consumption.

4.4.3 Source and Load Pull

Source and load pull help the designer to identify load and source impedances for optimum operation of the amplifier for output power and PAE in terms of bias conditions, input power drive level and terminations presented to high order harmonics at the desired frequency. Source and load pull (collectively called load pull) was conducted for the transistor at $V_{GS} = -3$ V, $I_{DS} = 69$ mA and $V_{DS} = 28$ V at various input power drive levels with appropriate second harmonic short circuit and third harmonic open circuit terminations at both gate and drain terminal to achieve optimum load impedance for high efficiency operation.

Fig. 4. 45 shows results of load pull simulation at 34 dBm input power. Much similar results as class AB amplifier (discussed in Section 4.3.3) were obtained. However, it should be considered that the transistor was biased closer to the knee region compared to class AB amplifier at a lower $I_{DS} = 69$ mA to achieve similar output power at ≈ 1 dBm lower input power. This indicates increase in fundamental amplitude due to addition of third harmonic, which is in line with literature reviewed in Section 3.4.2. However, higher efficiency was anticipated, and non-linear device model of the transistor was questioned due to the difference in efficiencies for class F and class AB amplifiers.

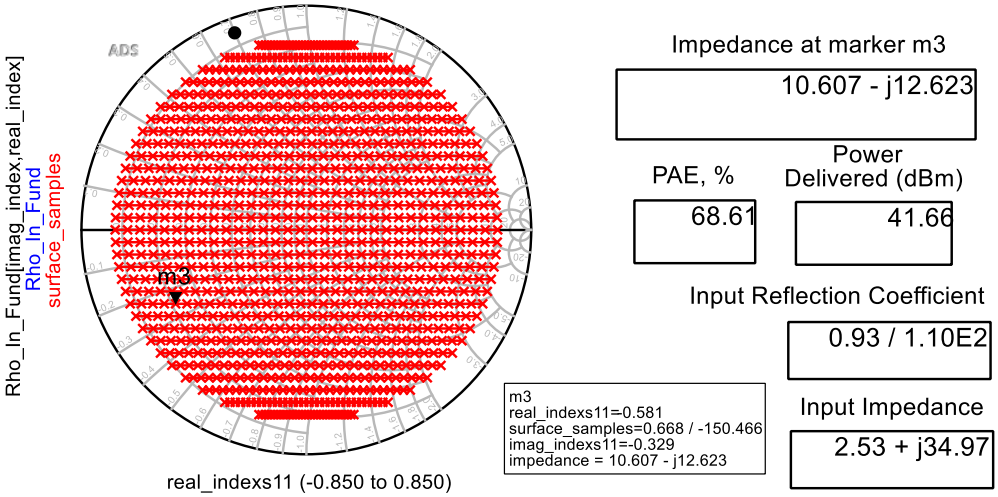


Fig. 4. 45: Load pull simulation results for class F operation for CGH55015 biased at $I_{DS} = 69$ mA and $V_{DS} = 28$ V with 34 dBm input power

Load and source impedances are the same as class AB amplifier and lie within stable region on the Smith chart. However, PAE and output power contours were slightly different. Fig. 4. 46 shows output power and PAE contours obtained from load pull simulations under class F operation.

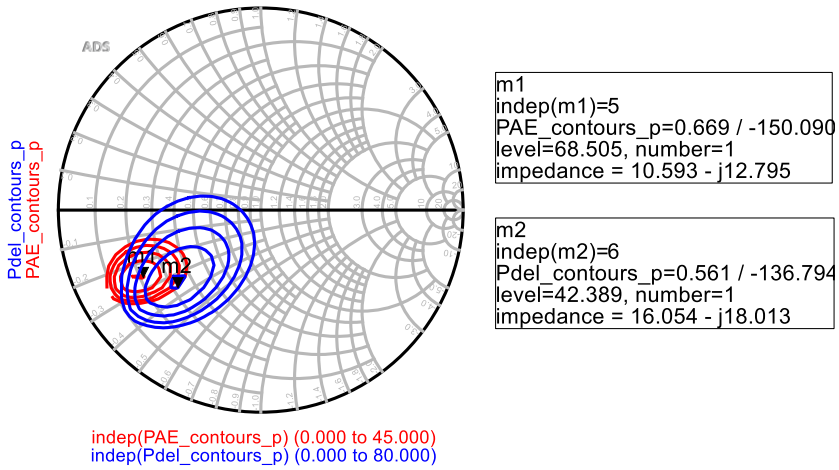


Fig. 4. 46: Output power and PAE contours on the Smith chart under class F bias and high order harmonic termination conditions

Markers m1 and m2 lie on inner circles of their contours which represent higher values that may be achieved. Load pull simulations suggest 42.4 dBm and 68.6 % maximum output power and PAE respectively. However, PAE was prioritised and load impedance shown in Fig. 4. 46 was selected at the fundamental frequency. Fig. 4. 30 shows comparison between impedances obtained from load pull simulations and those suggested in device's datasheet [104].

4.4.4 Design of Waveform Shaping Networks

It was emphasized earlier that square voltage and half rectified current waveforms at gate and drain terminals are achieved through proper waveform shaping networks which are incorporated within source and load termination networks. These networks essentially provide short circuit impedance to even harmonic and open circuit impedance to odd harmonic components. However, to achieve 100 % theoretical efficiency, infinite number of higher order harmonics need to be considered (to achieve a pure square wave) which is practically not realisable. Even up to the fifth harmonic leads to very complex circuit architecture where a trapping stage for each harmonic component needs to be included. Thus, appropriate termination to up to third harmonic component will be designed, which can theoretically provide up to 90.7 % efficiency discussed by Cripps (2006) in [41]. Overall design of source and load termination networks involve the design of waveform shaping networks for harmonic components followed by sub-matching networks for fundamental component at impedances obtained through load pull simulations.

Structure of input waveform shaping network that provides control over second and third harmonics has been shown in Fig. 4. 47. The impedances seen looking into the gate terminal (point B) are second harmonic short circuit and third harmonic open circuit. Fig.

4. 48 shows basic structure of the output waveform shaping network. Output waveform shaping network is designed from the drain terminal at node A, where $\frac{\lambda_3}{4}$ transmission line provides 180° phase shift at the 3rd harmonic frequency and open circuit to 3rd harmonic seen looking into the drain. Shunt open circuit stub at node B transforms impedance from open circuit to short circuit. Second harmonic short circuit impedance to the drain is provided through a quarter wavelength transmission line (at the fundamental) located in the drain bias line. To maintain second harmonic short circuit at node A, tuned transmission line ($\frac{\lambda_2}{4} - \frac{\lambda_3}{4}$) is used to ensure that the length between nodes A and C remains $\frac{\lambda_2}{2}$. An additional open circuit stub at node C compensates for decoupling capacitors that cause impedance of second harmonic to be shifted from short circuit in a clockwise manner on the Smith chart. This way low second harmonic impedance is provided at node C.

A: Z_2 = short, Z_3 = short

B: Z_2 = short, Z_3 = open

C: Z_2 = open

D: Z_3 = open

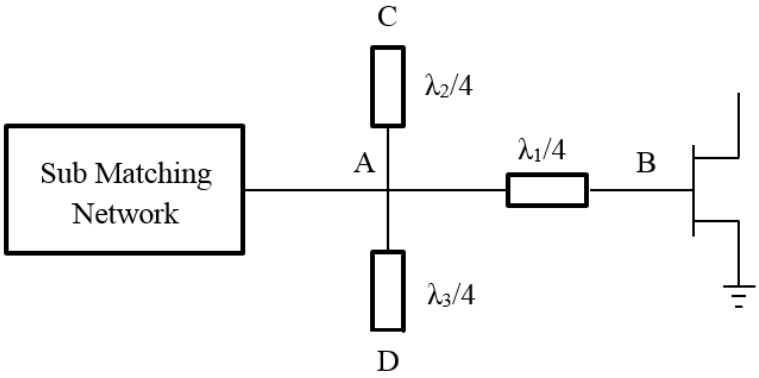
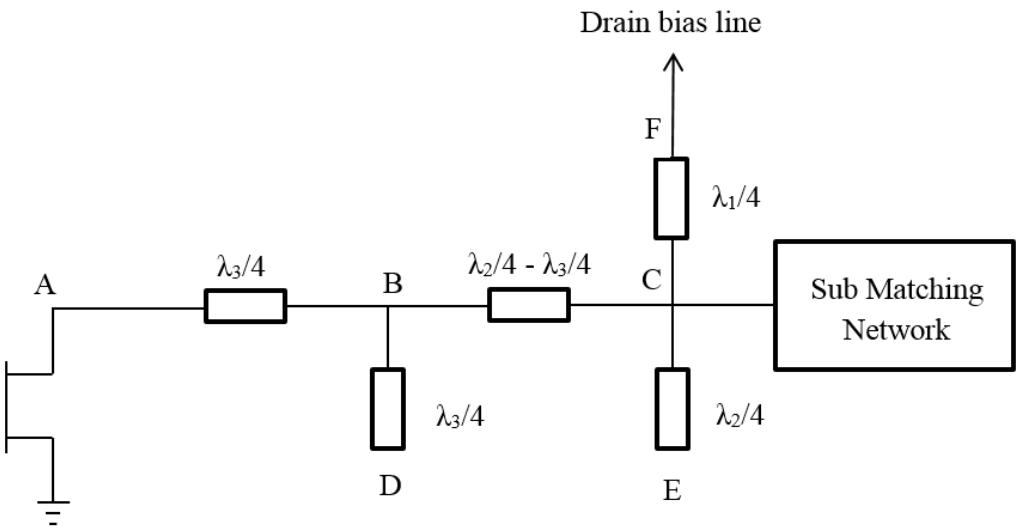


Fig. 4. 47: Structure of input waveform shaping network for class F amplifier



A: Z_2 = short, Z_3 = open

B: Z_3 = short

C: Z_0= open, Z_2 = short, Z_3= open

D: Z_3 = open

E: Z_2 = open

F: Z_1= short, Z_2 = short, Z_3= short

Fig. 4. 48: Structure of output waveform shaping network for class F amplifier

Radial stubs are a viable option for harmonic trapping stubs due to their less susceptibility to variations in transmission line length and the ability to provide low impedances over a wider frequency range. Input and output waveform shaping networks were designed according to structures explained above, followed by EM simulations using Momentum simulator and parametric optimisation. In the output waveform shaping network, shunt $\lambda_1/4$ transmission line to provide short circuit to second harmonic component will be part of the drain bias network. Thus, only the fundamental and third harmonic components of output waveform shaping network were simulated in Momentum. However, all sub-networks of the amplifier circuit will be later optimised using EM simulated results to achieve accurate harmonic impedances. Effects of gate and drain pads and soldering footprint were also considered during optimisation to provide the required harmonic impedances at device's gate and drain terminals. Fig. 4. 49 and Fig. 4. 50 show circuit schematics and layout of input waveform shaping network, respectively.

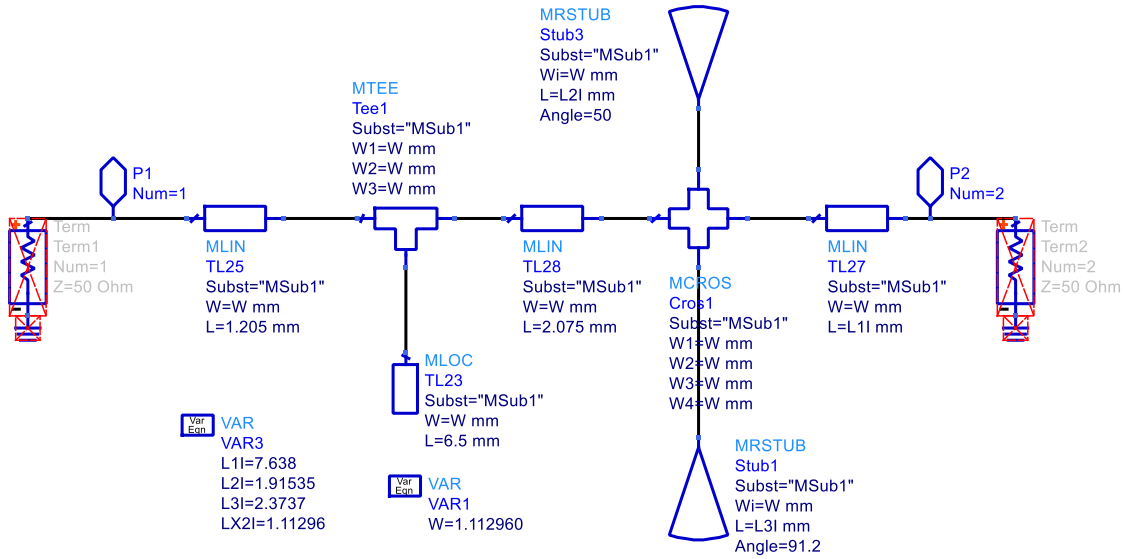


Fig. 4. 49: Schematics of input waveform shaping network of class F amplifier

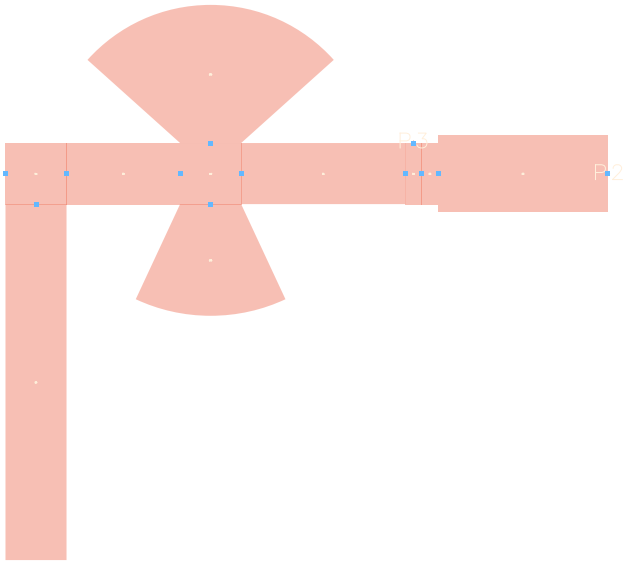


Fig. 4. 50: Layout of input waveform shaping network of class F amplifier

EM simulated results of the input waveform shaping network are shown in Fig. 4. 50. Important point to observe is that second and third harmonic impedances lie within short and open circuit regions. However, impedance at fundamental frequency will be transformed to the required impedance from source pull by using a sub-matching network.

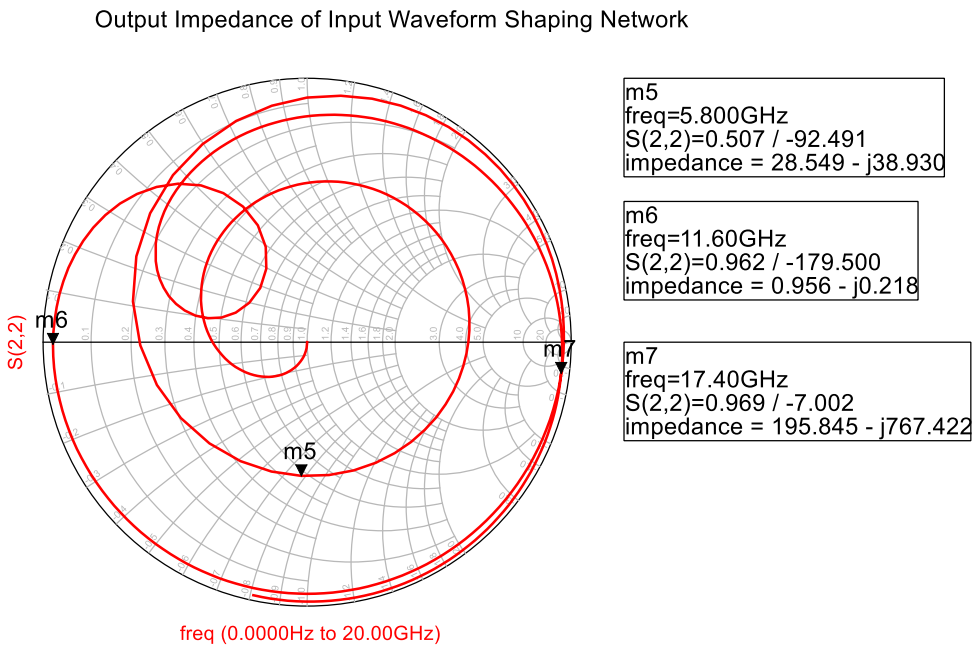


Fig. 4. 51: EM simulated results of input waveform shaping network of class F amplifier

Fig. 4. 52 and Fig. 4. 53 show circuit schematics and layout of output waveform shaping network, respectively.

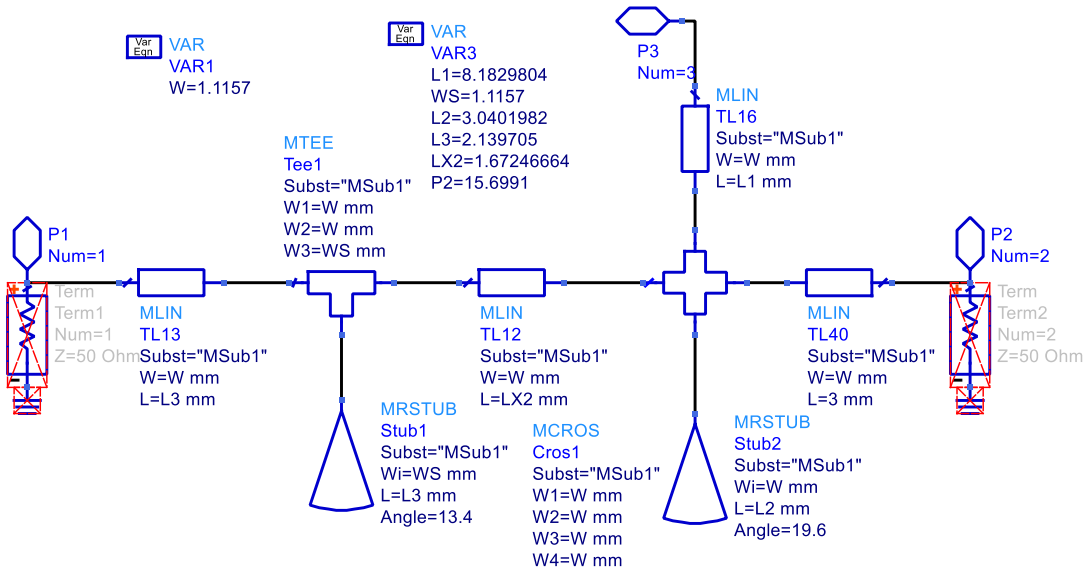


Fig. 4. 52: Schematics of output waveform shaping network of class F amplifier

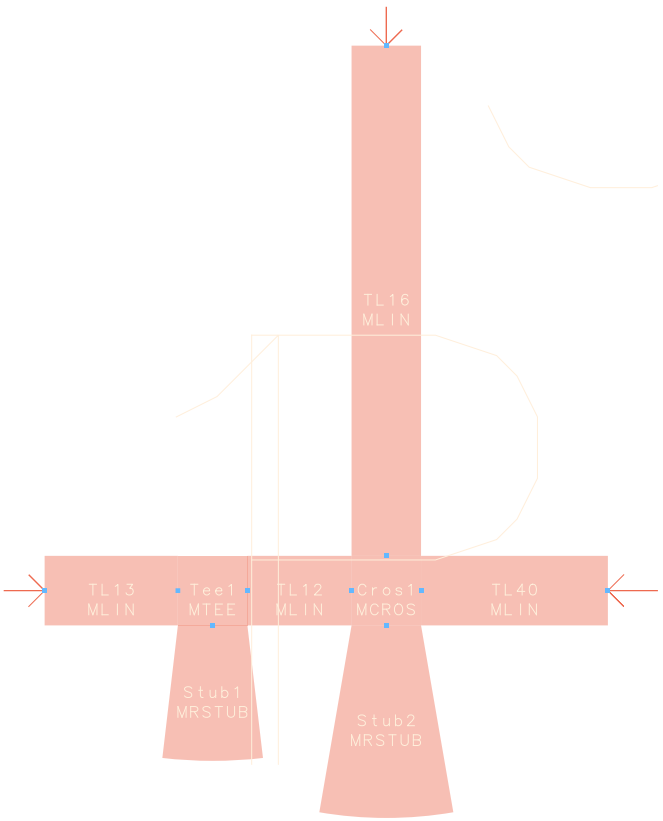


Fig. 4. 53: Layout of output waveform shaping network of class F amplifier

EM simulated results of output waveform shaping network have been shown in Fig. 4. 54. Second and third harmonic impedances lie within short and open circuit regions, while impedance at fundamental frequency will be transformed to the required impedance from load pull by using a sub-matching network.

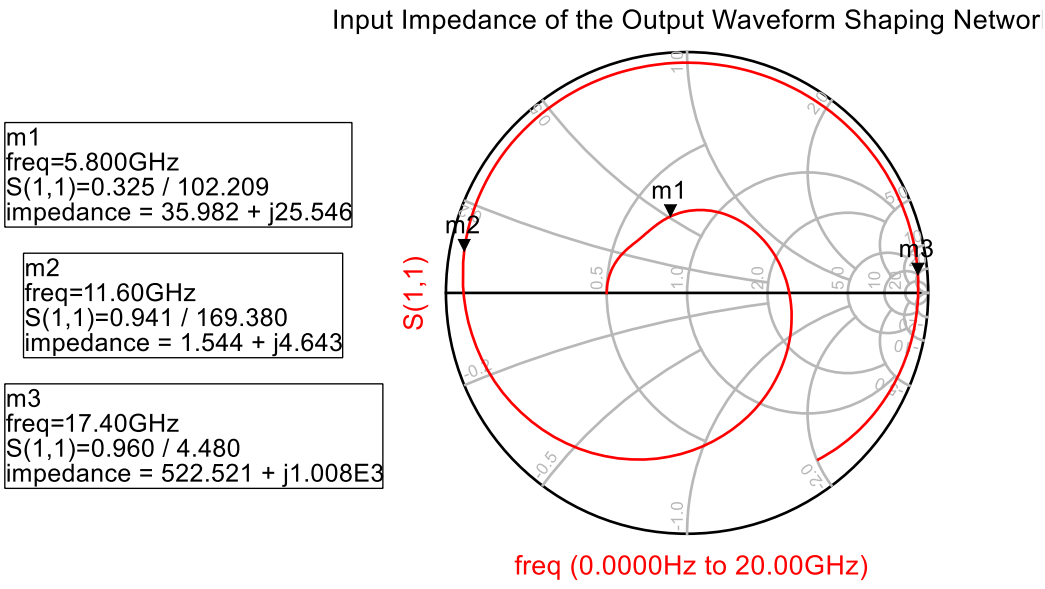


Fig. 4. 54: EM simulated results of output waveform shaping network of class F amplifier

4.4.5 Design of Fundamental Matching Network

After the design of harmonic tuning networks, fundamental matching needs to be performed and requires transformation of fundamental impedance provided by harmonic matching networks to the impedances obtained from source and load pull. After the design and optimisation of fundamental matching networks through EM simulations; parametric optimisation is performed alongside harmonic waveform shaping networks to obtain desired impedances at gate and drain terminals. Fig. 4. 55 shows circuit schematics of the input matching network for the fundamental frequency, which has been kept simple and performed using a series capacitor of 0.3 pF that also acts as DC blocking capacitor.

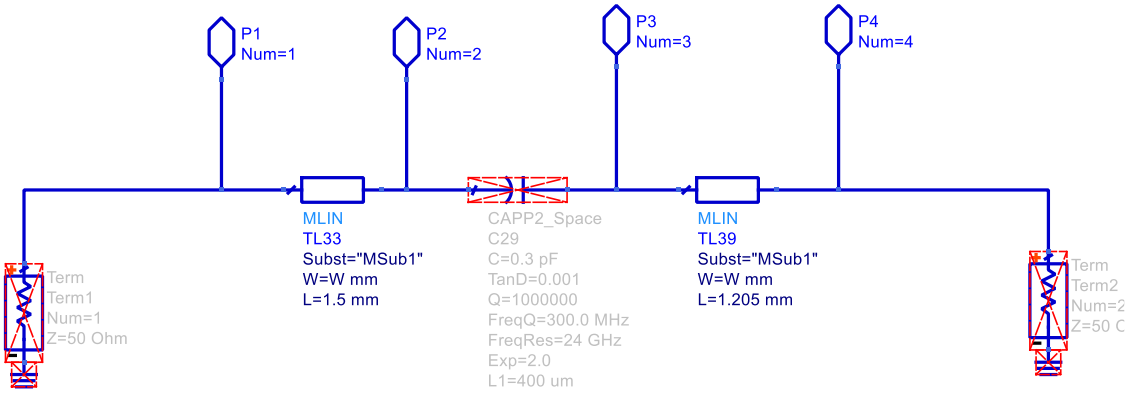


Fig. 4. 55: Fundamental input matching network of class F amplifier

Figure 6.22 shows EM simulated results for output impedances provided by waveform shaping network and the input matching network to the transistor's gate terminal. These values lie within the required regions and depict high Q values. Besides this, impedances have also been kept away from the unstable regions that were defined during stability analysis.

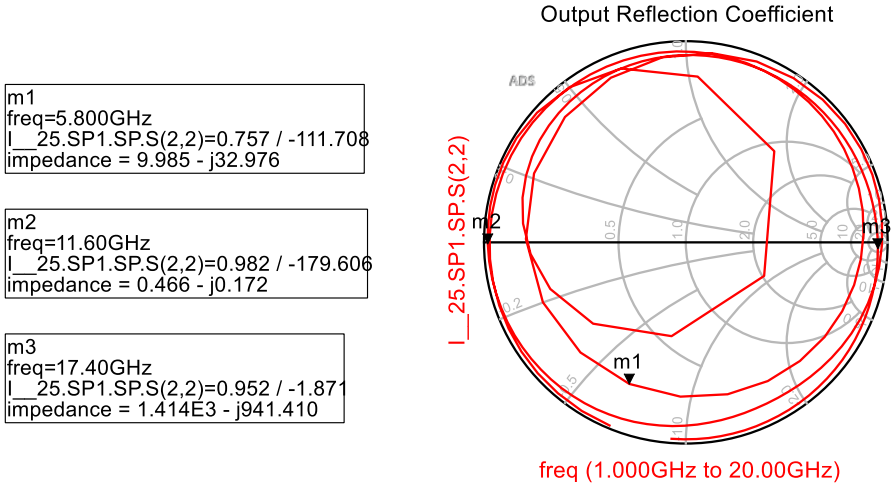


Fig. 4. 56: EM simulated results of source termination network of class F amplifier

Fig. 4. 57 shows circuit schematics of output matching network for the fundamental frequency, which includes a series 0.3 pF capacitor, that also acts as DC blocking capacitor to the drain bias.

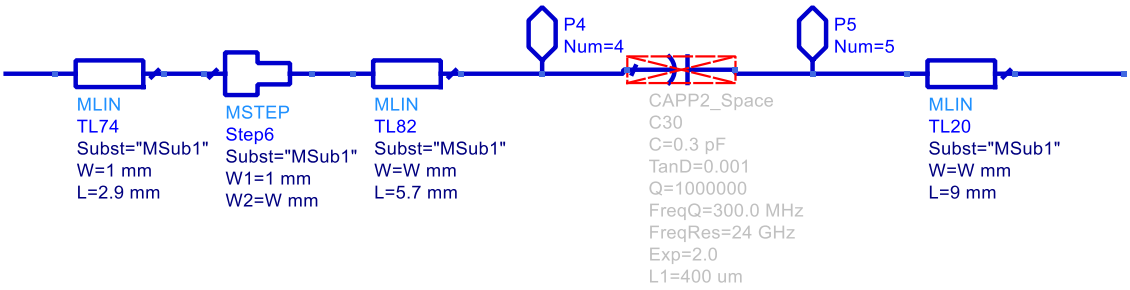


Fig. 4. 57: Fundamental output matching network of class F amplifier

Shows EM simulated results of load termination of class F amplifier which provides the required fundamental and harmonic impedances at the drain terminal.

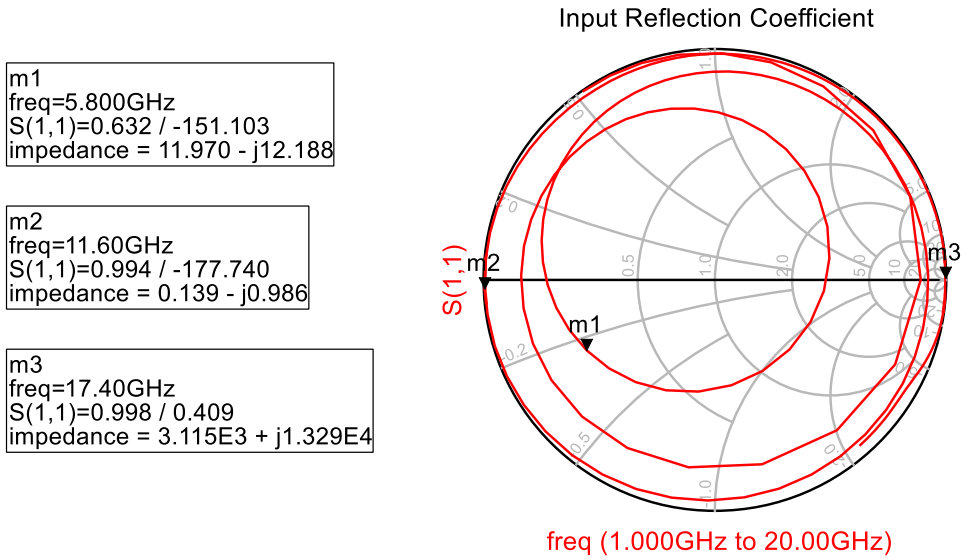


Fig. 4. 58: EM simulated results of load termination network of class F amplifier

4.4.6 Schematics of Class F Amplifier

Final schematics and processed class F amplifier have been attached in Annex B.

4.4.7 Results and Analysis

This section presents small and large signal results and corresponding analysis of class F amplifier that include small signal [S]-parameters, stability analysis, relationships between output power, gain, and PAE as a function of the input power. Large signal measurements of output power and PAE show much comparable performance to simulation results based on EM simulated networks. Powering up of the amplifier was performed in safe mode, and an unexpected rise in drain current was observed which initially pointed out towards oscillations; however, the spectrum analyser didn't show any oscillations even at out of band low frequencies. The compliance set at drain DC supply protected the transistor from any damage. Decoupling issue in the drain line was identified which was resolved by replacing 33 μF capacitor with a higher voltage rated 33 μF capacitor and an additional 100 μF. The issue was resolved, and the amplifier showed stable behaviour during successive powering up routines.

Stability Analysis

Fig. 4. 59 presents simulated stability factor curves of class F amplifier. Stability for the amplifier has been achieved by using a shunt resistor in the gate bias line and multiple decoupling capacitors. Stability factor curve indicates that the transistor is unconditionally stable across the entire frequency band with a value of 1.98 at the intended frequency of operation, i.e. 5.8 GHz. Class F amplifier showed better stability performance compared to class AB amplifier (discussed in Section 4.3.6), especially at low frequencies.

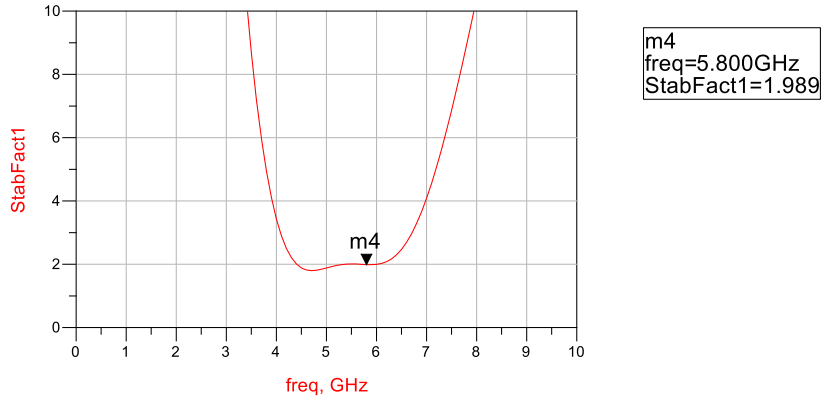


Fig. 4. 59: Stability factor of class F amplifier for CGH55015

Small Signal Behaviour

Small signal behaviour of the amplifier has been optimised to provide a good match at 50 Ω input and output ports, however, this is not an indication of large signal behaviour of

the amplifier. Fig. 4. 60 shows small signal S_{11} and $S_{21}$with EM simulated networks where $S_{11} = -22.7$ dB and $S_{21} = 10.76$ dB at 5.8 GHz.

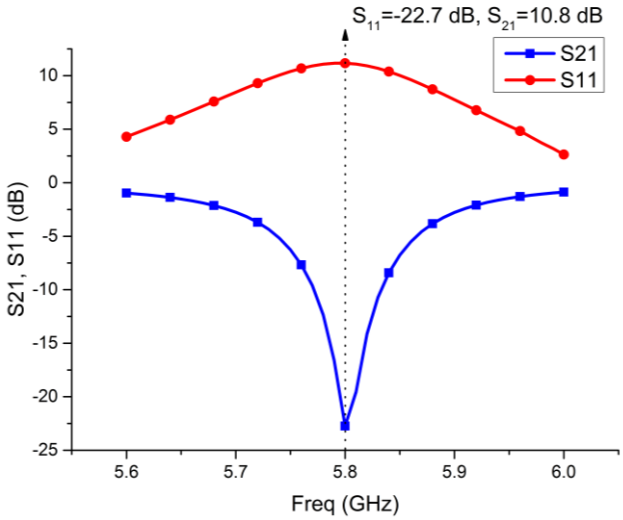


Fig. 4. 60: Simulated small signal [S]-parameters of class F amplifier for CGH55015

Large Signal Analysis

Large signal behaviour of power amplifiers can be described in terms of gain compression which is reduction of device gain due to the transfer of signal power from fundamental component to higher order harmonics. Fig. 4. 61 shows the relationship between simulated output power, large signal gain and PAE as a function of the input power when the transistor is biased at $V_{GS} = -3$ V, $I_{DS} = 69$ mA and $V_{DS} = 28$ V.

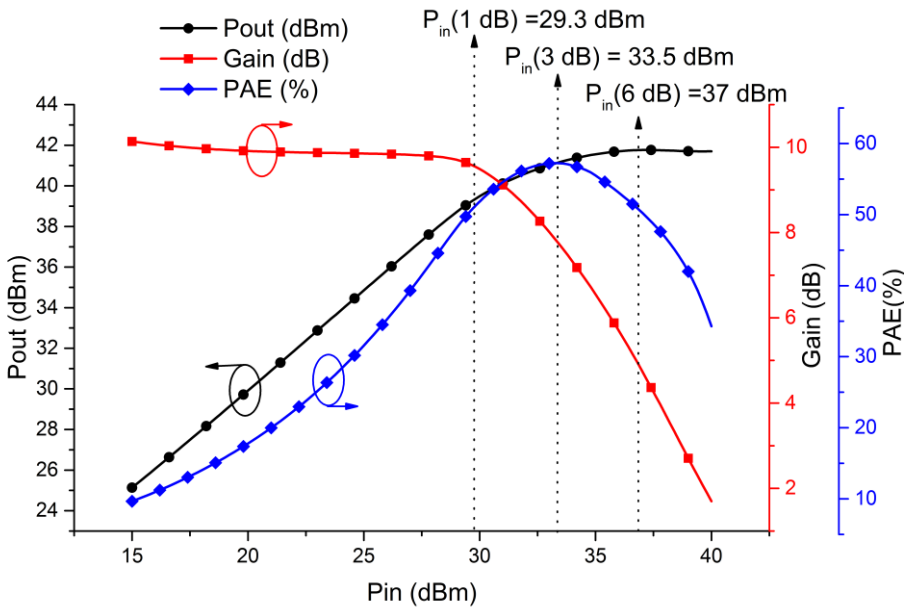


Fig. 4. 61: Large signal simulation results of class F amplifier showing output power, gain and PAE as a function of the input power, biased at $V_{GS} = -3$ V, $I_{DS} = 69$ mA and $V_{DS} = 28$ V

Amplifiers may be operated at higher levels of saturation (3 dB or 6 dB) to achieve high output power and efficiency, but this comes at the cost of linearity and reduced gain. However, in the intended medical application where CW high output power is desired with decent efficiency, class F amplifiers prove to be useful. The amplifier presented herein achieves 1 dB, 3dB and 6 dB gain compression at 29.3 dBm, 33.5 dBm and 37 dBm input power levels, respectively through simulation results. At these gain compression levels; 38.9 dBm, 41.2 dBm and 41.75 dBm output power at 50 %, 57.2 % and 50 % PAE, respectively is produced. Analysis of Fig. 4. 61 suggests that optimum operating condition for class F amplifier is around 3 dB input power compression level where 41.2 dBm output power with 57.2 % PAE is achieved, which is also the maximum PAE. Fig. 4. 62 shows measurement results of output power, gain and PAE at various input power levels between 20 dBm and 38 dBm with 0.4 dBm steps; which have been measured using power measurement setup discussed in Section 4.2.8. Simulated and measured PAE have similar trends; but measured large signal gain curve shows gain expansion of 0.84 dB between $P_{in} = 20$ dBm and 29.2 dBm, as the amplifier approaches knee region. However, gain drops sharply after $P_{in} = 29.3$ dBm (1 dB compression point identified through simulations); and an increase in PAE and output power takes place.

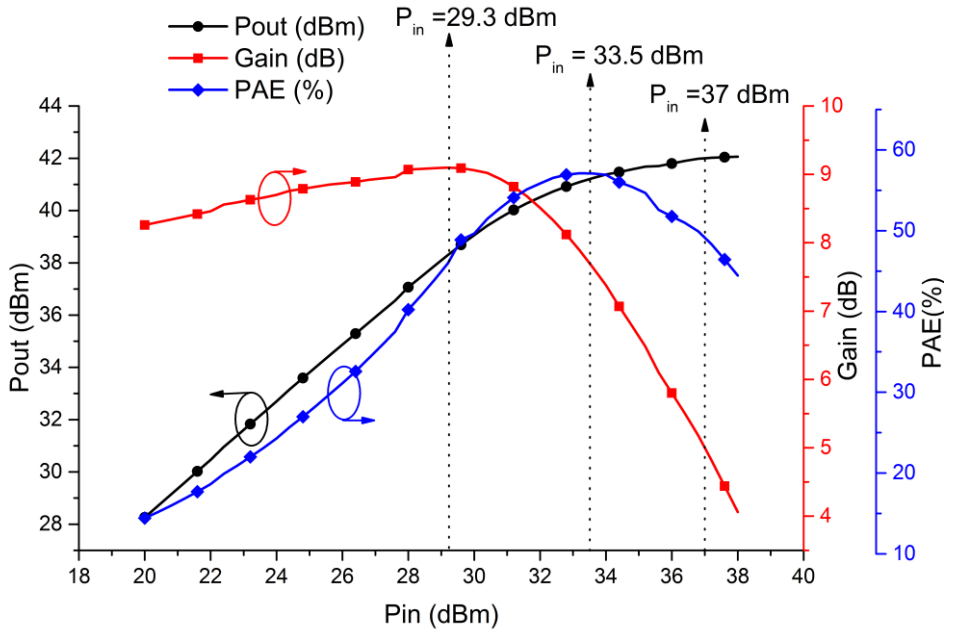


Fig. 4. 62: Measured large signal results of class F amplifier showing output power, Gain and PAE as a function of the input power, biased at $V_{GS} = -3$ V, $I_{DS} = 69$ mA and $V_{DS} = 28$ V

Consider the region between $P_{in} = 34$ dBm and $P_{in} = 38$ dBm shown in Fig. 4. 63 and Fig. 4. 64; which provides important insight about behaviour of class F amplifiers in terms

of output power and efficiency for higher levels of input power in the saturation region. It was observed that with an increase in input power in the respective region, DC current component increased noticeably while fundamental current component only showed marginal increase. Thus, efficiency of class F amplifier reduced sharply beyond $P_{in} = 34$ dBm due to large relative increase in DC current component compared to fundamental current component. Output power remained between 41.4 dBm and 42.06 dBm.

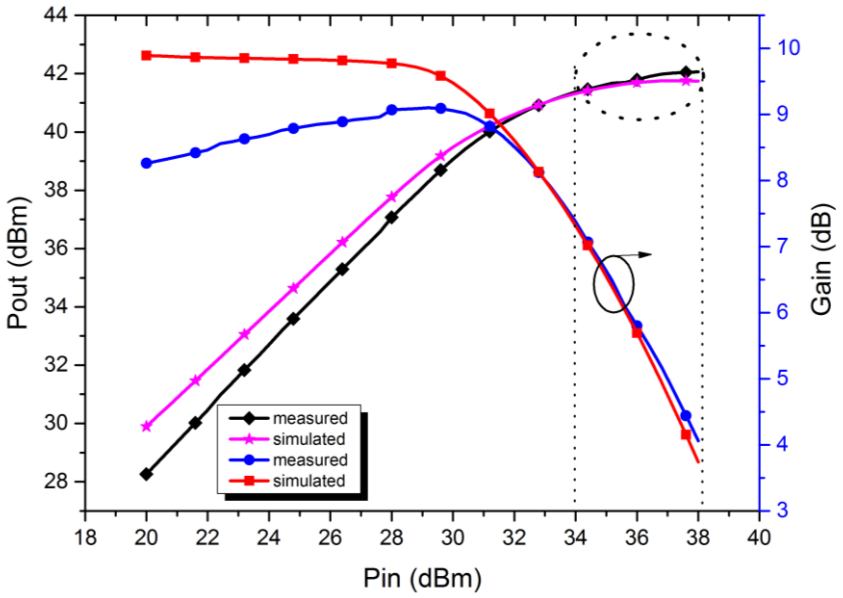


Fig. 4. 63: Comparison between simulations and measurements results of class F amplifier for output power and large signal gain as a function of input power, biased at $V_{GS} = -3$ V, $I_{DS} = 69$ mA and $V_{DS} = 28$ V

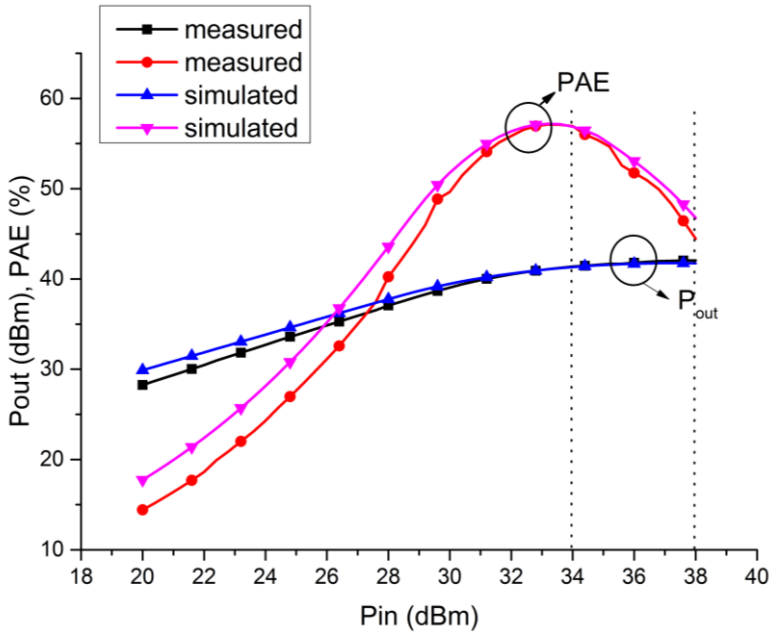


Fig. 4. 64: Comparison between simulations and measurements results of class F amplifier for output power and PAE as a function of input power, biased at $V_{GS} = -3$ V, $I_{DS} = 69$ mA and $V_{DS} = 28$ V

The dotted elliptical region in Fig. 4. 63 shows that measured output power is greater than simulated output power (42.06 dBm versus 41.75 dBm respectively). At such high levels of saturation, knee voltage effects cause an increase in the fundamental current component which leads to an increase in the output power. Driving the amplifier further into saturation causes the fundamental current component to increase substantially, which can be observed through an increasing trend of output power in the measured curve. Difference between measured and simulated results is likely due to inaccuracies in non-linear model of the transistor, especially in the knee region.

Drain IV-Curves

The operation of class F amplifiers in lower levels of gain compression can be expressed as a switch and the amplifier achieves saturation earlier compared to its dual class F^{-1} amplifier. Though class F^{-1} amplifiers outperform class F amplifiers in terms of maximum efficiency and output power; but the latter shows better performance at lower levels of gain compression. This was identified through comparison of class F amplifier discussed herein with state of the art class F^{-1} amplifiers discussed in [112]–[114]. Especially because half-rectified current waveform (class F) requires less input power than square current waveform (class F^{-1}) to generate the same output power. However, the operation of class F and class F^{-1} is much different in the saturation region. During the extraction of output capacitance in Section 4.2.4, it was discussed that non-linear C_{ds} generates harmonic components, out of which second harmonic component has the largest magnitude. However, in class F amplifiers, second harmonic short circuit condition and third harmonic open circuit condition only permits third harmonic voltage component to exist and prevents the current waveform from bifurcation.

With an increase in input power, harmonic currents are generated by the amplifier, and since fundamental and third harmonic components are out of phase, even at lower levels of the input power; flat (or square) voltage waveform shaping is achieved at lower input power levels. Waveform shaping in class F amplifiers helps to achieve higher output power and efficiency by minimising the overlap between current and voltage waveforms. So, when the voltage waveform has a maximum value, the current will be in the sub-zero region. It has been discussed in literature [115] that either one or both peaks of class F amplifiers may be flat, while current waveform remains half rectified. Fig. 4. 65 shows voltage and current waveforms at the drain. Partially square waveform (referred to as maximally flat in literature) can be observed, and the current waveform doesn't show bifurcation.

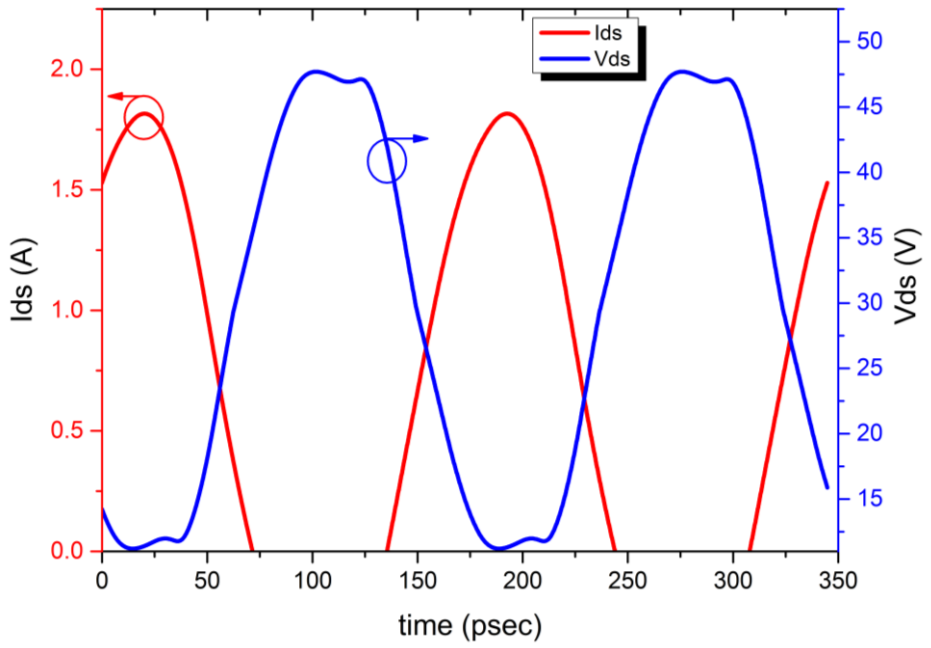


Fig. 4. 65: Drain current and voltage waveforms of class F amplifier

4.5 Design of Multistage High Efficiency Amplifier

4.5.1 Introduction

This section presents design and analysis of multistage high efficiency amplifier that includes class AB amplifier in the gain stage followed by class F amplifier in the power stage to produce over 43 dBm output power with a targeted total efficiency over 65 %. These amplifier stages employ CGH55015F2 and CGH55030F2 GaN HEMTs, respectively. Class F stage has been designed following the classical definition suggested by Cripps (2006) in [41] where voltage and current waveforms at the drain are square wave and half rectified sinusoidal waveforms, respectively. Half rectified current waveform can be achieved through class B conduction angle (180°) and essentially has even order harmonics; however, a large input waveform will cause the voltage waveform to swing across the knee region leading to the generation of odd order current harmonics. Appropriate odd harmonic load termination network will cause the generation of odd order voltage harmonics that will be added to the fundamental. Thus, the voltage waveform will include fundamental and third harmonic components. Ideal load termination network requires short circuit condition to even order harmonics, while open circuit condition to odd order harmonics which can be provided through the network shown in Fig. 4. 48. Major aim for development of multistage amplifier was to achieve saturated output power in excess of 43 dBm for the prospective medical applications. Structure of multistage amplifier has been shown in Fig. 4. 66.

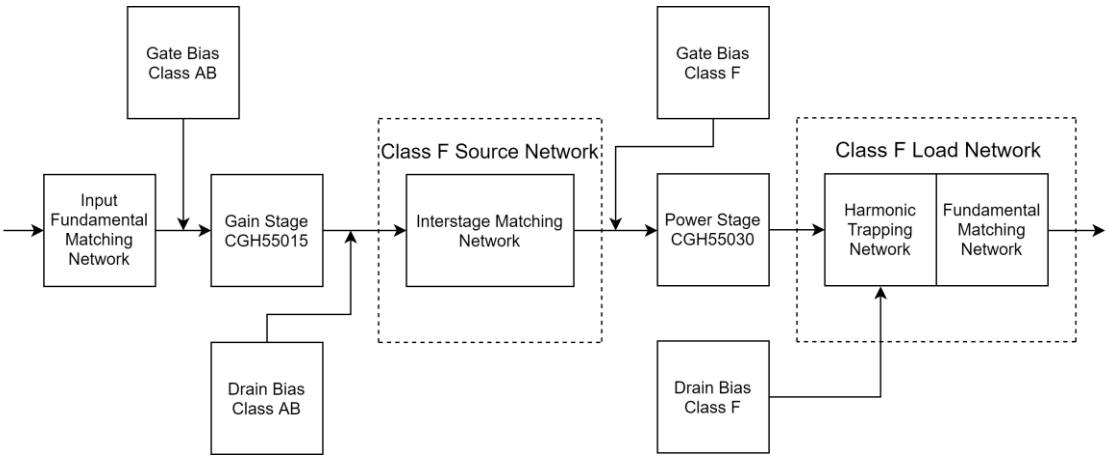


Fig. 4. 66: Multistage amplifier structure

Input fundamental matching network has been designed using fundamental source impedance achieved from load pull simulations, followed by high impedance (80 Ω) gate bias line. Transistor selected for the gain stage is CGH55015F2 which is a variant of CGH55015F1 and can provide up to 40 dBm saturated output power compared to 41.75 dBm of the latter. However, the gain stage has been designed to achieve highest possible PAE to provide suitable output power to drive the power stage over 1 dB saturation level. Interstage matching network has been kept simple without input harmonic terminations for class F power stage which relies on high input power levels that would bring in knee effects to generate higher order harmonics. Fundamental load and source impedances for class AB and class F amplifiers, respectively in interstage matching networks were achieved through load pull simulations. In class F load network, fundamental matching network provides impedance matching for the fundamental component while resonating out higher order harmonics, while harmonic trapping network includes optimum impedances for up to third order harmonics. This section of multistage amplifier design and analysis is organised as follows. Section 4.5.2 presents analysis of appropriate bias conditions for class AB and class F stages, which are different than the ones presented in Section 4.3.2 and 4.4.2. Section 4.5.3 presents the design aspects of input, output and interstage matching networks and respective schematics, Section 4.5.4 presents results and corresponding analysis.

4.5.2 DC Characteristics and Optimum Bias Point

Transistors in multistage amplifier have been biased especially close to class B bias conditions in deep class AB conditions at $I_{DS} \approx 0.08\, I_{max}$. The bias conditions of class F stage will ensure that the output power waveform provided by class AB stage will cause swing across the knee region to achieve non-linearities and generation of higher order harmonics. Fig. 4. 67 and Fig. 4. 68 shows DC IV simulations of CGH55015F2 and

CGH55030F2 transistors, respectively that were performed using non-linear device model provided by Cree/Wolfspeed. V_{gs} has been swept from -3 V to 0 V with steps of 0.2 V, and V_{ds} has been swept from 0 to 32 V with steps of 1 V. Optimum bias points for class AB and class F stages have been selected at $V_{GS} = -2.9$ V, $I_{DS} = 120$ mA and $V_{DS} = 28$ V, and $V_{GS} = -2.9$ V, $I_{DS} = 260$ mA and $V_{DS} = 28$ V, respectively. Bias points for class A and B amplifiers have been shown for comparison which correspond to maximum gate voltage $V_{GS} = -2.3$ V suggested in device's datasheet [105], [106].

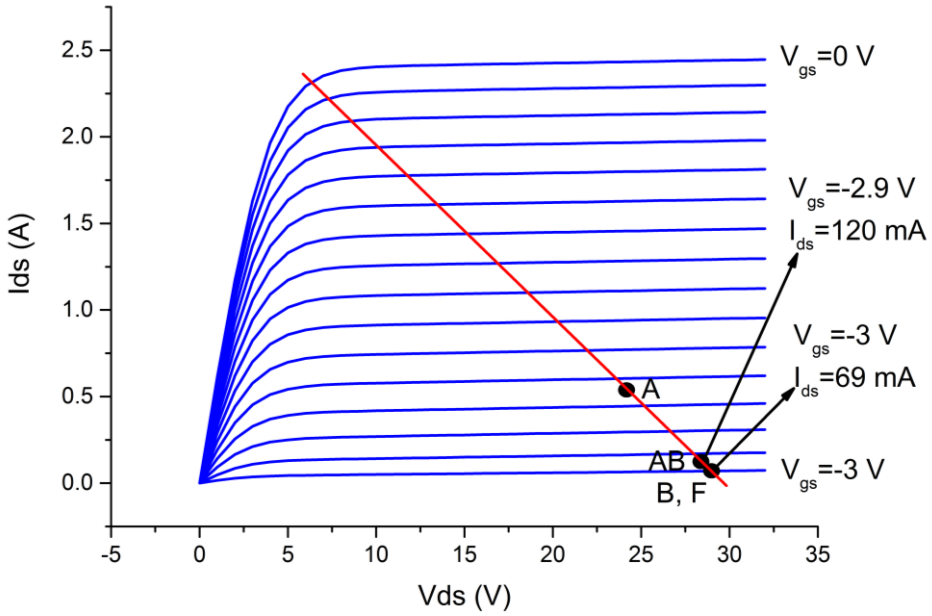


Fig. 4. 67: DC IV curves of CGH55015F2 GaN HEMT showing optimum bias point for class AB stage

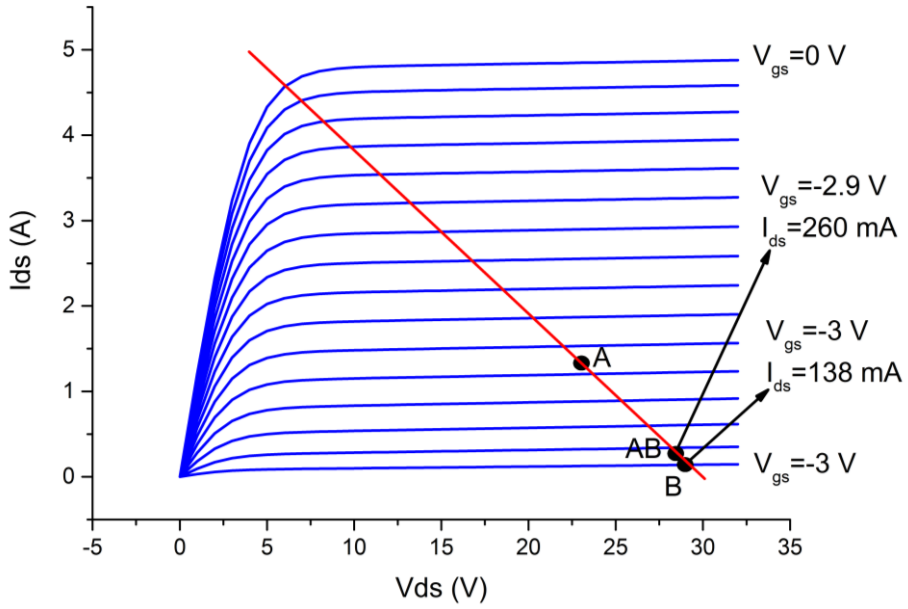


Fig. 4. 68: DC IV curves of CGH55030F2 GaN HEMT showing optimum bias point for class F stage

4.5.3 Design of Matching Networks

This subsection presents the design of various sub-matching networks shown in Fig. 4. 66 that include input fundamental matching network of class AB amplifier, interstage matching network between class AB and class F amplifiers, and harmonic trapping and fundamental matching network of class F amplifier. Various fundamental and harmonic impedances used in these sub-matching networks were obtained through load pull simulations (discussed in Section 4.3.3 and 4.4.3) using non-linear transistor models for optimum high efficiency operation at various input power drive levels for operation in the saturated region. During the design process, class AB stage was designed and optimised using EM simulated networks to have an indication of the input power that could be provided to class F stage. However, due to an anticipated difference in simulated and measurement results based on experience during previously developed amplifiers, fundamental load impedance of class F stage was optimised for up to 2 dB variation in the input power by considering PAE and output power contours during load pull simulations. Table 4. 2 shows respective fundamental source and load impedances of class AB and class F stages; optimum impedances provided in device's datasheets [105], [106] have also been shown for reference.

Table 4. 2: Comparison between simulated and datasheet fundamental source and load impedances of gain (class AB) and power (class F) stages of multistage power amplifier

Amplifier Stage (Class)	Source Pull		Load Pull	
	Simulated	Datasheet	Simulated	Datasheet
Gain (Class AB)	9.1 - j6.8	12.3 - j24.3	11.7 - j32	26.5 - j7.5
Power (Class F)	15.9 - j22.6	8.4 - j14.0	5.8 - j9.9	15.4 - j11

Input Fundamental Matching Network

Fundamental input matching network of class AB amplifier has been designed by using stepped transmission lines, 0.3 pF DC blocking capacitor and open circuit radial stubs towards the input port. Gate bias network was placed at 1 mm from the gate package terminal and input matching circuit was optimised up to the first decoupling capacitor. Fig. 4. 69 and Fig. 4. 70 show circuit schematics and layout of the input fundamental matching network, respectively. The layout shows high impedance gate bias line up to the first decoupling capacitor.

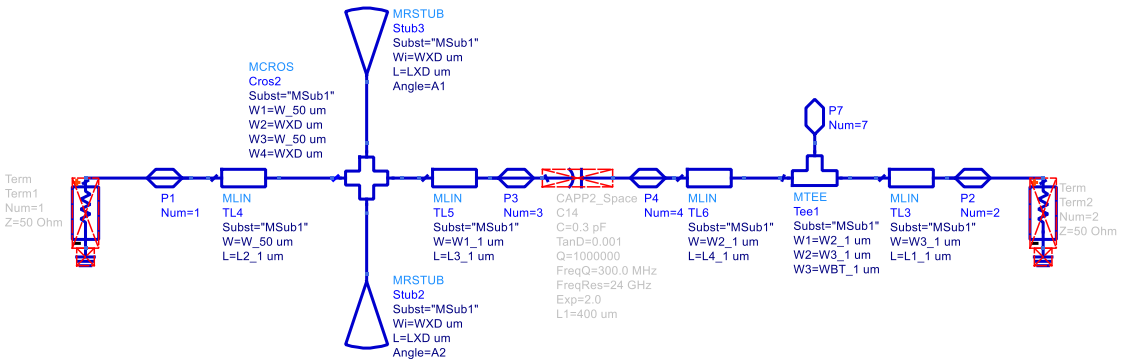


Fig. 4. 69: Circuit schematics of input fundamental matching network of multistage amplifier

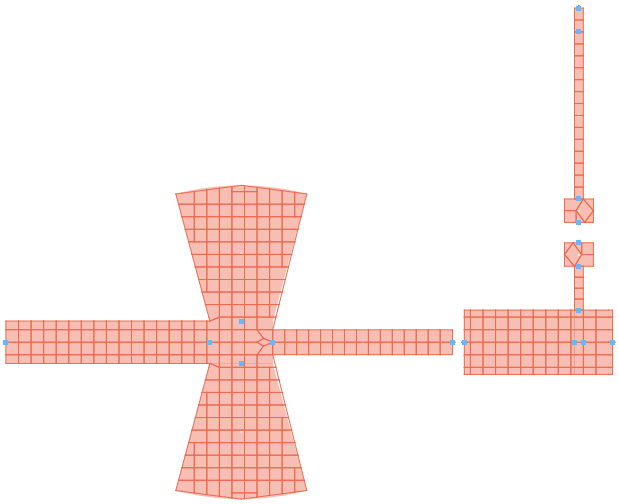


Fig. 4. 70: Layout of input fundamental matching network of multistage amplifier including high impedance gate bias line up to the first decoupling capacitor

Interstage Matching Network

High efficiency power amplifiers with waveform shaping networks at the load generally consider input sinusoidal waveforms at the gate which has been discussed in literature review. In such scenarios, input capacitance (C_{gs}) and associated non-linearities of transistors perform shaping of large input sinusoidal waveform due to the generation of higher order harmonic components, of which second harmonic component has the major effect [116]. Detailed analysis of input waveform shaping has been presented in [117]. Input waveform shaping network shown in Fig. 4. 47 was utilised to provide short circuit and open circuit conditions to even and odd order harmonics, respectively at the gate terminal of class F amplifier discussed in Section 4.4.4; which provided an improvement in drain efficiency due to suppression of higher order harmonics. During simulations of class F stage discussed herein, it was observed that 1.7 % improvement of drain efficiency was achievable with an input harmonic trapping network at the cost of 0.6 dB reduction

in output power of the amplifier. Thus, efficiency was traded-off for higher output power and reduced circuit complexity; and waveform shaping wasn't performed at the gate of class F stage.

Interstage matching network provides optimum fundamental load impedance to class AB stage, DC blocking between drain (class AB) and gate (class F) bias networks, and fundamental source impedance to class F stage. Class AB amplifiers require second harmonic short circuit condition at the drain; which is provided through quarter wavelength transmission line in the respective drain bias network. Interstage matching has been performed using stepped transmission lines and 0.6 pF DC blocking capacitor. Show circuit schematics and layout of interstage matching network which was optimised with bias networks of respective amplifier stages. The layout shows quarter wavelength transmission line of drain bias network of class AB stage, and high impedance gate bias line of class F stage up to the first decoupling capacitors.

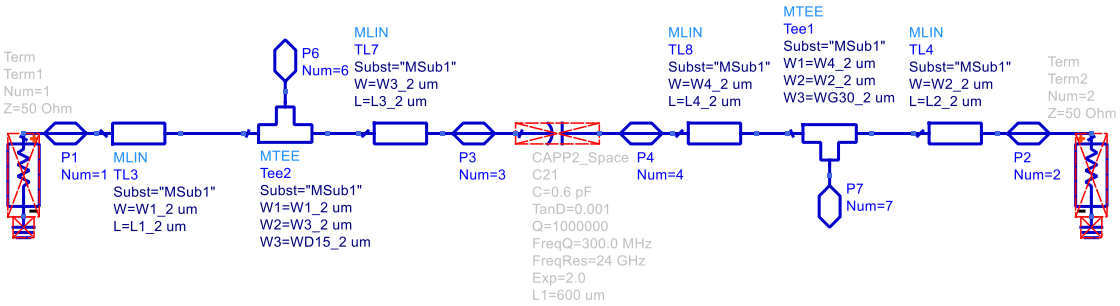


Fig. 4. 71: Circuit schematics of interstage matching network between class AB and class F stages of multistage power amplifier

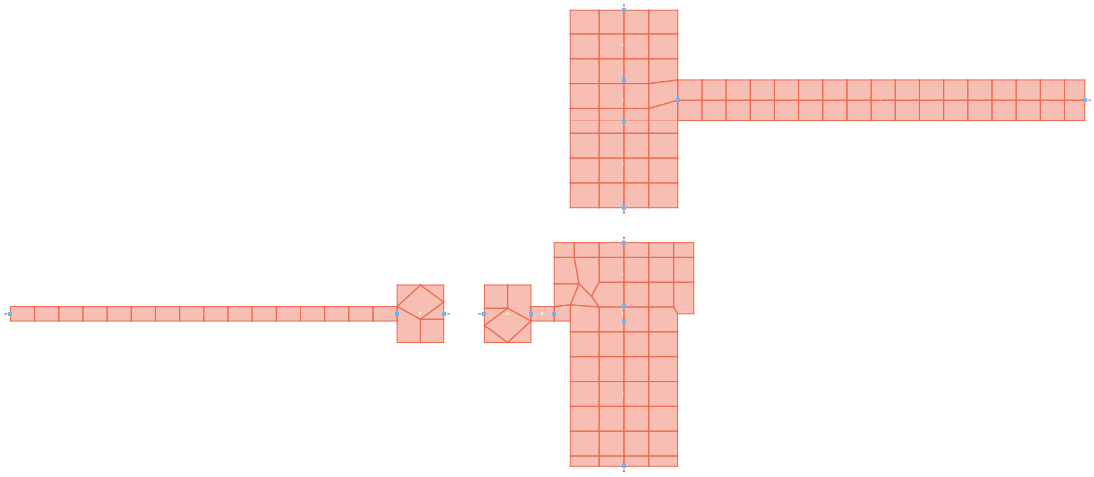


Fig. 4. 72: Layout of interstage matching network between class AB and class F stages of multistage power amplifier (the layout has been rotated right by 90° for illustration purposes)

Class F Load Network

Class F load network has been divided into two parts: harmonic trapping network and fundamental matching network. Second harmonic short circuit and third harmonic open circuit conditions are provided through the former network which includes quarter wavelength transmission line (part of drain bias network) and a tuned transmission line. Fundamental matching network includes stepped transmission line, 0.3 pF DC blocking capacitor, and open circuit radial stubs located towards the 50 Ω output port. Fig. 4. 73 Fig. 4. 74 show circuit schematics of harmonic trapping network and fundamental matching network of class F amplifier, respectively.

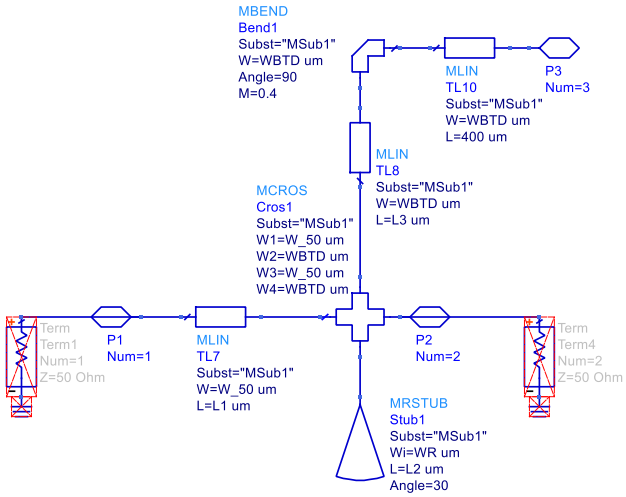


Fig. 4. 73: Circuit schematics of harmonic trapping network for class F stage of multistage amplifier

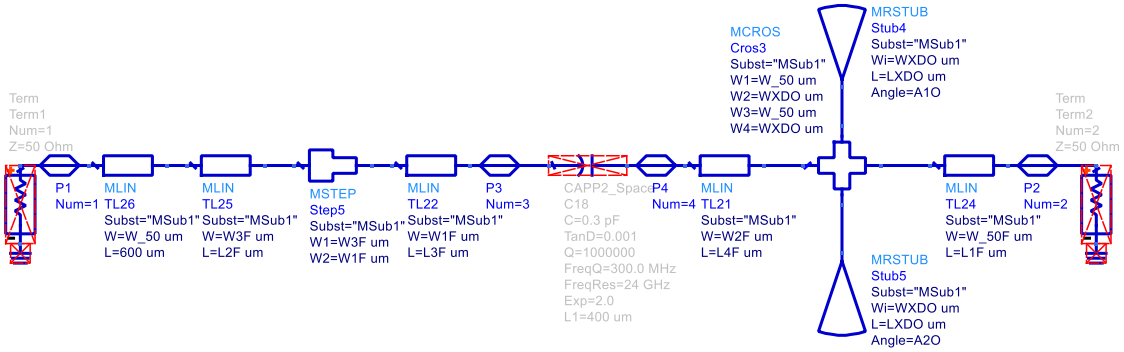


Fig. 4. 74: Circuit schematics of fundamental matching network of multistage amplifier

Optimum impedances were achieved with class F load network, EM simulated results of harmonic trapping network have been shown in Fig. 4. 75.

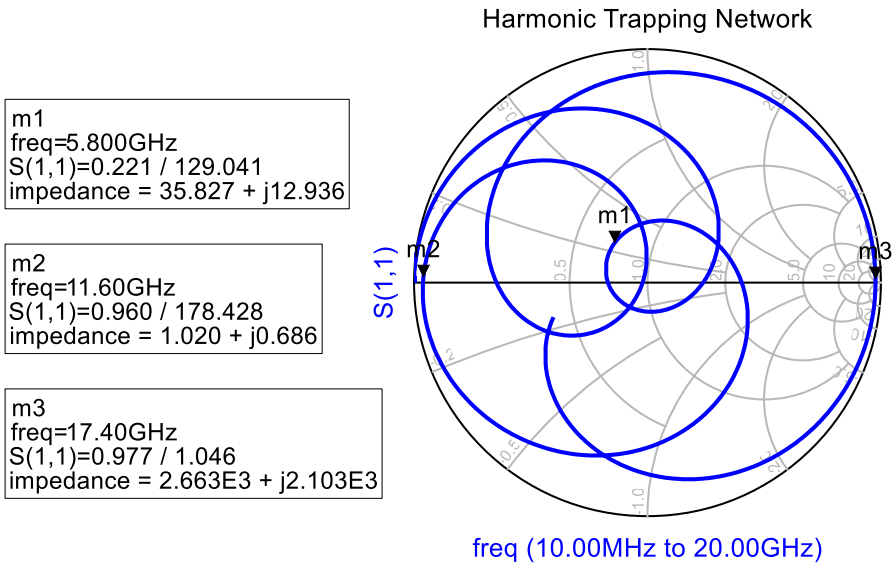


Fig. 4. 75: EM simulated results of harmonic trapping network for class F stage of multistage amplifier

Layout of Multistage Amplifier

The layout of multistage amplifier (shown in Fig. 4. 18) was generated in Keysight's ADS from hierarchical schematics after the parametric optimisation of various EM simulated subnetworks, corresponding to the structure shown Fig. 4. 66.

4.5.4 Results and Analysis

This section presents analysis of various results for the multistage amplifier. The two amplifier stages are in cascade and biased separately with a DC blocking capacitor between them. It was also kept in mind to ensure both the stages operate in the saturation region, especially the power stage where voltage swing can increase substantially and cause the HEMT to go out of the saturation region. However, GaN technology can support very high electric fields compared to other semiconductor technologies like GaAs, which is a distinct advantage towards implementing cascade multistages. Powering up of the amplifier was performed in safe mode and the amplifier was observed for any oscillations. After no oscillations were confirmed through the spectrum analyser, drain terminals of both stages were biased to their respective $V_{ds,q}$ and the gate voltage was increased to achieve respective $I_{d,q}$. Small signal measurements were performed to check input and output port match followed by large signal power measurements.

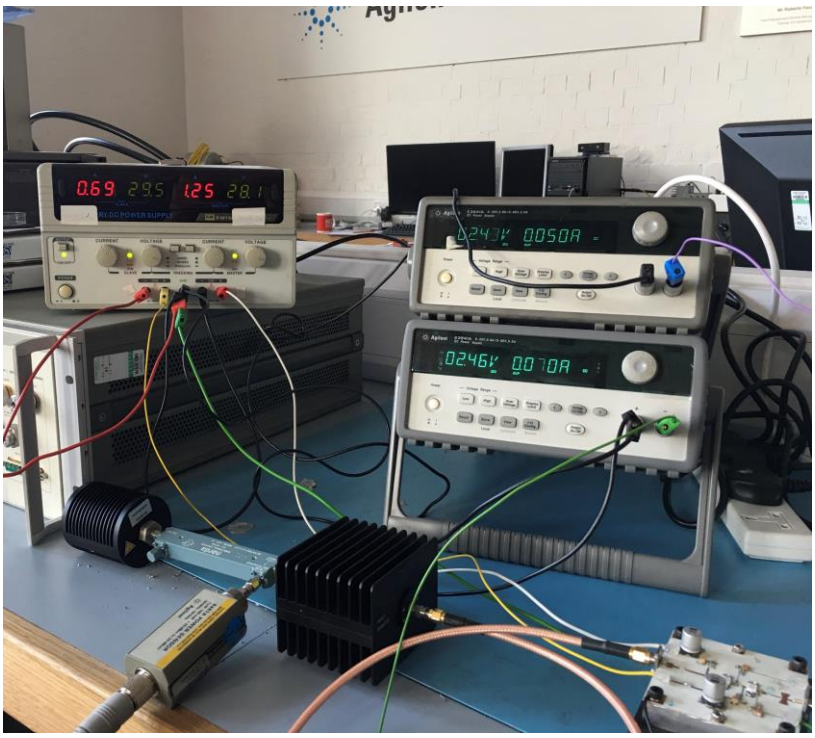
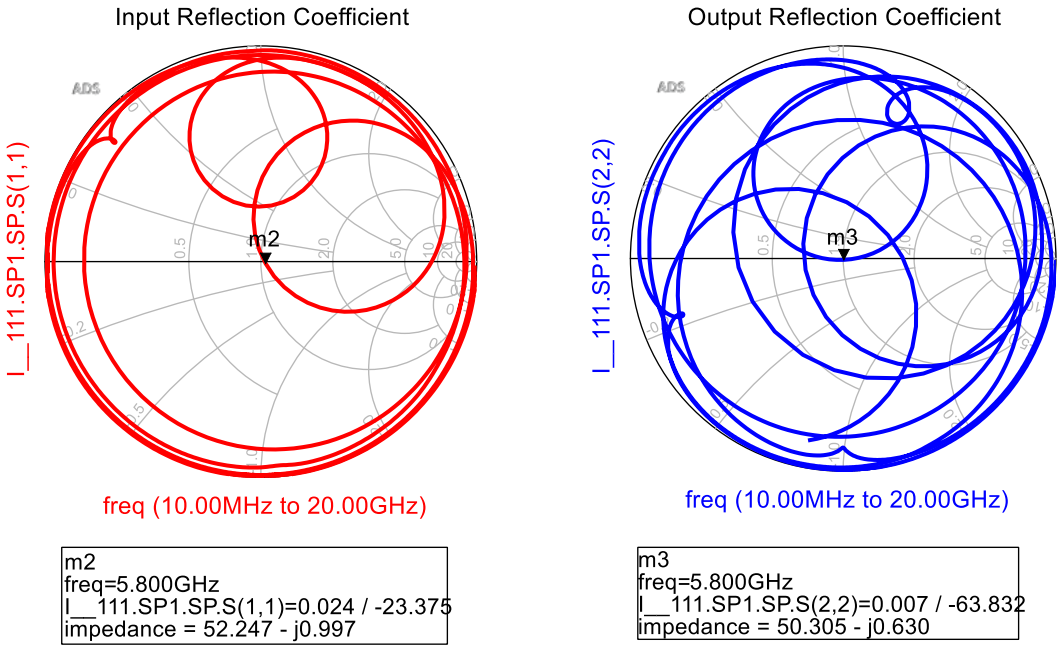


Fig. 4. 76: Typical measurement setup of multistage amplifier showing DC power supplies and output measurement setup with attenuators, directional coupler and connection to the power meter, and 50 Ω load. The input power source has been switched off.

Various measurements were performed in terms of input power level and bias conditions (up to class A) that could be supported by the amplifier; Fig. 4. 76 shows the measurement setup under typical bias conditions with the input power source switched off. Power supplies on the right side correspond to gate terminals, while those on the left hand side correspond to drain terminals. Biasing the gate terminal at higher DC voltage (class AB) than deep class AB/class F conditions, indicated large gate currents up to 70 mA which is undesired, however, operation in deep class AB bias conditions showed compliance with the values suggested in transistor data sheets.

Small Signal Behaviour

Stability analysis of the amplifier was performed using EM simulated networks, and large signal model of the transistors to identify unstable regions of the amplifier. Unconditional stability was observed, which was later confirmed during safe mode powering up of amplifiers. EM simulated results showing input and output port match has been shown in Fig. 4. 77.



(a) (b)

Fig. 4. 77: (a) Input and (b) output reflection coefficient of multistage amplifier

Resonance can be observed at various regions in simulated results, especially in output reflection coefficient (S_{22}); however, these are at higher frequencies, close to second and third harmonics which may indicate unfiltered higher harmonics in the output waveforms. Small signal characteristics were optimised for CW operation at 5.8 GHz from 5.0 GHz to 6.0 GHz, small signal gain (S_{21}) and input reflection coefficient (S_{11}) have been presented in Fig. 4. 78. These results show decent small signal gain of 16.4 dB at 5.8 GHz, which was intended to achieve from multistage amplifier. However, large signal gain that will be discussed in the succeeding section is an important result.

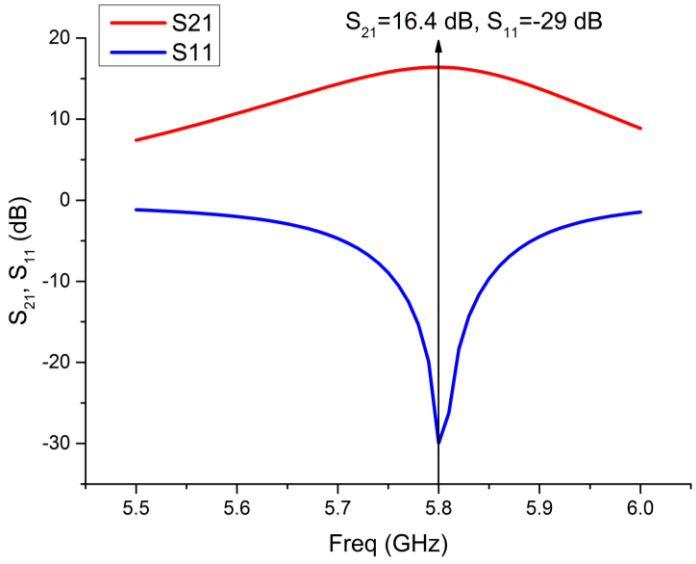


Fig. 4. 78: Simulated small signal [S] parameters of multistage amplifier with EM simulated networks and transistor models provided by the device manufacturers

Large Signal Analysis

Multistage amplifier presented herein includes class AB and class F stages which have been biased at $V_{GS} = -2.9$ V, $I_{DS} = 120$ mA and $V_{DS} = 28$ V, and $V_{GS} = -2.9$ V, $I_{DS} = 260$ mA and $V_{DS} = 28$ V, respectively. Measurement results of output power and gain as a function of the input power have been given in Fig. 4. 79. The amplifier provides 43.4 dBm output power at 3 dB gain compression with 65.4 % total efficiency which has been calculated in terms of the total DC power consumed by both amplifier stages.

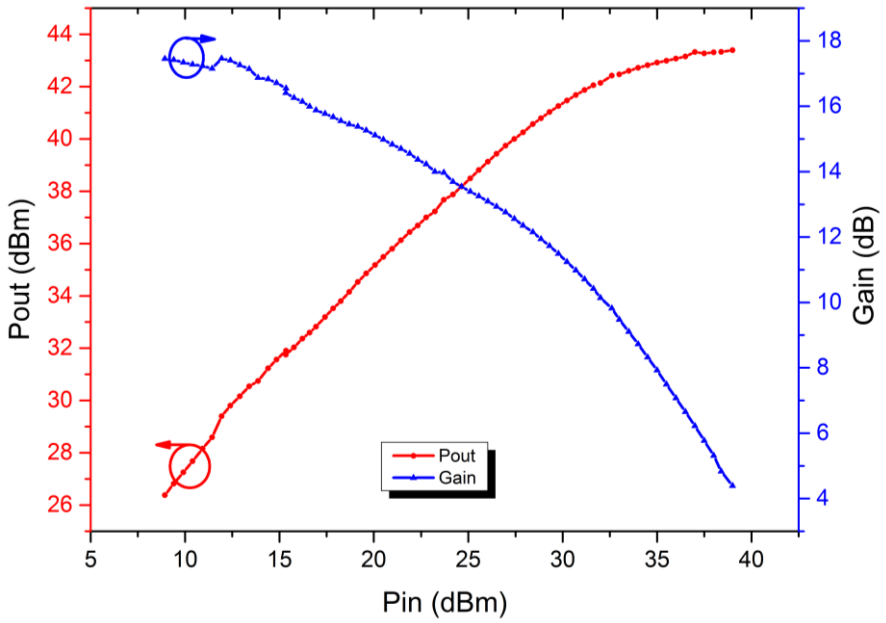


Fig. 4. 79: Measured large signal results of multistage amplifier showing output power and gain as a function of the input power

The amplifier shows gain expansion at lower input power levels between $P_{in} = 10$ dBm to 16 dBm which is a behaviour depicted in GaN technology, and the gain drops linearly, and rolls off steeply after $P_{in} = 32$ dBm. The amplifier was driven in deep saturation levels to observe the effect of saturation on output power. Maximum output power of 43.4 dBm (21.9 W) corresponding to a gain of 6.7 dB shows heavy compression, however, total efficiency of 65.4 % shows the effect of higher order harmonics. Another important point to consider is the large signal gain at lower input power levels. It is surprising to see large signal gain is greater than small signal simulated results, however, it can be attributed to gain expansion which happens at lower input power levels and the transistor models cannot describe the effect accurately.

Comparison between simulated and measured results have been shown in Fig. 4. 80, where the input power is swept from $P_{in} = 9$ dBm to 38 dBm with steps of ~0.5 dBm. Input power of simulated results was matched with the measured results.

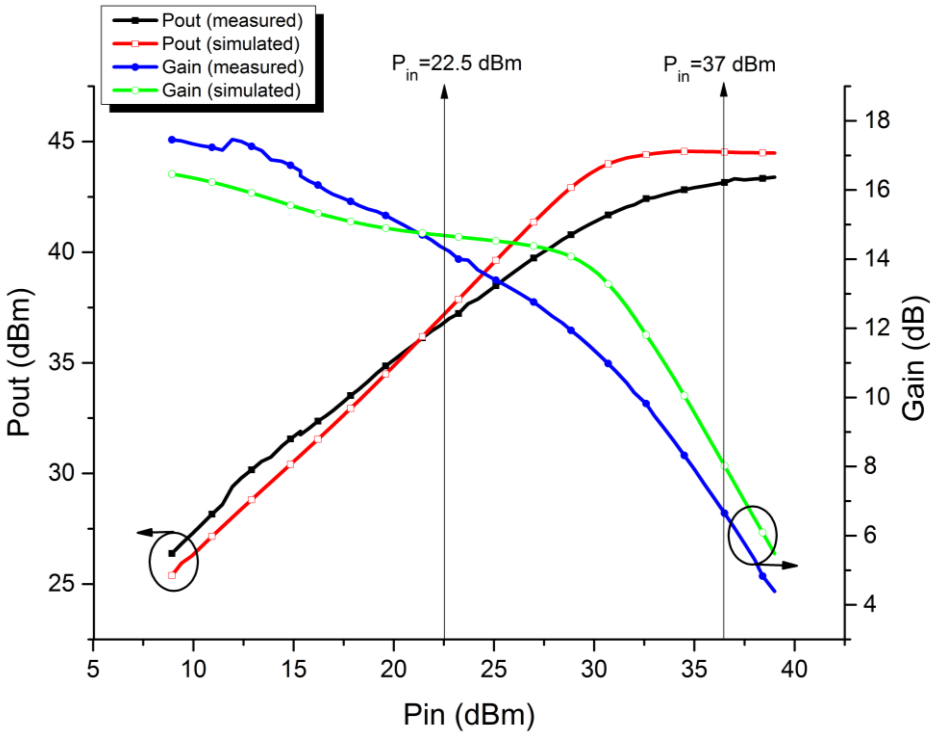


Fig. 4. 80: Comparison between measured and simulated results of multistage amplifier showing output power and gain as a function of the input power for $P_{in} =$ 9 dBm to 38 dBm

Gain expansion cannot be observed in simulated large signal results; and large signal gain is essentially equivalent to small signal gain shown in Fig. 4. 78 within the linear region. Measurement results also show comparatively gradual saturation, and there is much difference between measured and simulated results between $P_{in} = 22.5$ dBm and $P_{in} =$ 37 dBm, however, the gap narrows down after $P_{in} = 37$ dBm, where the difference between large signal gain is 1.3 dB, while the maximum difference is 2.32 dB at $P_{in} =$ 30.24 dBm.

Drain IV Curves

Simulated time domain voltage and current waveforms with EM simulated networks at 1 dB gain compression for class F stage have been shown in Fig. 4. 81. Clipping of voltage waveform and ripple can be observed in the voltage maximum (corresponding to current minimum) which indicates the generation of odd order current harmonics, and voltage harmonics which are added to the fundamental voltage component. These are similar to the results shown for single stage class F amplifier discussed in Section 4.4.7, however, much larger ripple in the voltage waveform is observed here. The optimum operation of class F amplifiers was discussed to be achieved at lower levels of gain compression (~1

dB). Operation at further gain compression levels showed the voltage waveform to have negative voltage values at the drain which can potentially cause transistor damage.

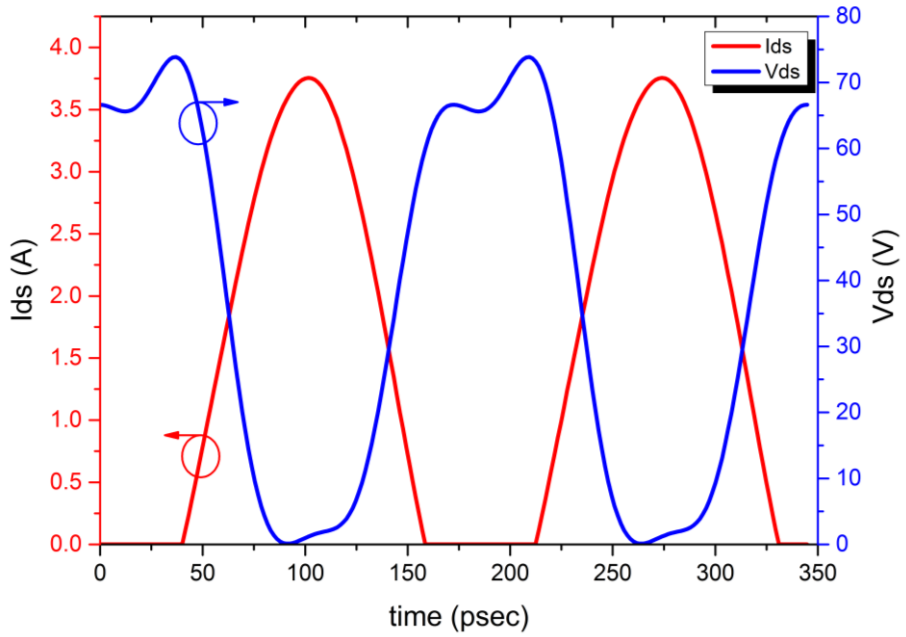


Fig. 4. 81: Drain current and voltage waveforms of class F stage of multistage amplifier

4.6 Conclusion

This chapter presented design, fabrication and measurements of high efficiency class AB, class F and multistage class AB and class F amplifiers in gain and power stages, respectively using commercially available Cree GaN HEMT devices. The amplifiers were fabricated on Roger RO4350B board which have the capability to support high RF currents and output power. The design procedure involved analysis of DC *IV* characteristics and stability analysis followed by load pull simulations to obtain optimum source and load impedances for optimum output power and PAE. Large signal simulations were performed using EM simulated networks in Momentum microwave followed by parametric optimisation before the layout was processed at the PCB fabrication facilities at the University of Manchester. Large signal measurements were performed in support with Dr Christopher Buck from Filtronic Broadband. The amplifiers were essentially designed for medical applications where CW operation is desired; thus, linearity and noise performance weren't considered. Important behavioural performance of high efficiency amplifiers due to their operation close to the knee region was observed which helped to understand important relationship between non-linearities, harmonic components, output power, PAE and gain under large input drive levels. Decent performance in agreement with target specification discussed in Table 4. 1 was obtained. Testing and validation of the amplifiers on porcine liver bench model will be discussed

in the succeeding section to demonstrate efficacy for intended portable haemostasis medical application. The design and results obtained from these amplifiers have been published in [101], [118].

Chapter 5

Testing and Validation of Discrete Power Amplifiers

5.1 Introduction

Radio frequency and microwave devices have effectively found their applications in the field of medicine and opened new dimensions for research and development. They have exhibited strong clinical effects that include tissue resection, desiccation, coagulation and ablation [6]. Targeted aim (specified in Table 4.1) for the development of high efficiency power amplifiers was to achieve sufficient enough microwave power (in excess of 20 W) to produce RF heating or coagulation with high efficiency. Some of the conventional devices use energy in the frequency band between 100 kHz to 10 MHz to produce cutting and desiccating effects. However, they cannot be utilized to produce coagulation and ablation or deliver controlled and localised energy into the human tissue. For this purpose, devices have been designed at microwave and millimetre wave frequencies above 400 MHz to enable efficient and focused energy delivery into the tissue for controlled heating. Thereby producing coagulation in vessels to stop bleeding and ablation in tissue structures that may or may not be cancerous. Antenna structures that have been designed to operate in these frequencies have an ability to match complex impedance of the particular tissue structure with that of the radiating antenna. Thus, ensuring that the energy is only delivered to the targeted tissue [119].

This chapter presents review of underlying concepts on the interaction of microwave energy with the human body and corresponding effects at various power levels and frequencies. Testing and validation was conducted in collaboration with Bangor University, with applicator structure and various results that have been presented in [101], [118], [120]–[122]. This chapter has been organised as follows. Section 5.2 provides review of various basic concepts that explain interaction of electromagnetic (or microwave) energy with the human body. Section 5.3 discusses about effect of temperature on cells and tissues, followed by discussion on conductive and radiative mechanisms of electromagnetic waves. Skin dept, shielding effect and specific absorption rate are important concepts as they help to identify optimum frequency, depth of effect and required heating to achieve targeted effect for different applications; these concepts have been discussed in Section 5.4. Section 5.5 reviews concept of RF heating and required microwave power, temperature profile and operating frequency. Section 5.6 discusses initial tests and results of portable haemostasis applicator and corresponding

results achieved through amplifiers discussed in the preceding chapter to demonstrate coagulation on porcine liver.

5.2 Interaction of Electromagnetic Waves with the Human Body

5.2.1 Introduction

Electromagnetic field spectrum in the range between 1 MHz and 100 GHz has depicted biological significance especially in terms of thermal heating because these fields can be readily transmitted, absorbed and reflected at the biological tissues and their boundaries [5]. The concepts of transmission, absorption and reflection considered with respect to human body and tissue are a function of body size, tissue dielectric and conduction properties and the frequency of operation.

5.2.2 Coulomb's Law and Gauss's Law

Coulomb's law defines the forces of attraction or repulsion between two point charges and the Electric Field Intensity ($\vec{E}$) which in volts per metre is defined as the force ($\vec{F}$) experienced by a unit positive test charge q in the vicinity of a charge Q. Electric lines of force emerge or terminate from a charge in a spherical (isotropic) manner with the charge Q located at the centre. The mathematical form of Coulomb's law has been defined in Eq. 5.1.

$$\vec{E} = \frac{\vec{F}}{q} = \frac{Q}{4\pi\varepsilon r^2}\hat{r} \text{ (V/m)} \tag{5.1}$$

Using Eq. 5.1, we can derive an expression for the amount of work required to move the unit positive test charge $+q$ from point a to b in the vicinity of an electric field $\vec{E}$. Eq. 5.2 represents this expression.

$$V_{ab} = -\int_a^b \vec{E} \cdot \overrightarrow{dl} \tag{5.2}$$

The above discussion about electric field intensity is true for electrostatics, where the two charges are stationary. However, microwave power sources and amplifiers employed in electrosurgical devices discussed in this thesis provide a time varying alternating current, thus, it is necessary to talk about time varying electric fields. Biological cells and tissues depict properties similar to those of dielectric materials (discussed in subsequent sections of this chapter) and the interaction of alternating electric field with dielectric materials is complex in nature being frequency and temperature dependent [123]. Fundamental property of dielectric materials is polarization that introduces a phase lag between

orientation of the dipole moment and the alternating electric field. We can relate polarization with the alternating electric field by using Gauss's law which states that total charge contained within a closed Gaussian surface is equal to the flux density. Eq. 5.3 defines an expression for the flux density [124].

$$\overline{D} = \varepsilon_o \overline{E} + \overline{P} \tag{5.3}$$

Where $\overline{\mathrm{D}}$ is the electric displacement $\left(\frac{\mathrm{c}}{\mathrm{m}^2}\right)$, ε_o is the permittivity in free space or vacuum, $\overline{\mathrm{E}}$ is magnitude of the electric field and $\overline{\mathrm{P}}$ is the polarization vector. Tissues and cells have water content present within them. Dipole rotation of materials with dipoles such as water (H_2O) or the creation of dipoles within materials is responsible to cause polarization due to an applied electric field. Dipole moment is important to define the interaction of EM waves with human cells and tissues and will be subsequently discussed later in this chapter [123], [124]. Electric flux density can also be calculated using Eq. 5.4.

$$\overline{D} = \varepsilon_o \varepsilon_r \overline{E} = \varepsilon_o (1 + \chi_e) \overline{E} \tag{5.4}$$

Where, χ_e is the proportionality constant called susceptibility. It relates electric field and polarization of a linear dielectric material. Total electric field across a material is the sum of applied electric field and induced electric field, and without the information of susceptibility, electric field characteristics become difficult to calculate [124].

5.2.3 Relative Permittivity

Relative permittivity of a material relates dielectric constant of the material to the permittivity in free space. Being a ratio between electric displacement $\overline{D}$ and electric field intensity $\overline{E}$, relative permittivity is a dimensionless quantity and can be expressed by Eq. 5.5 [123], [124].

$$\varepsilon_r \cong 1 + \chi_e = \frac{\varepsilon}{\varepsilon_o} \tag{5.5}$$

$$\varepsilon_r = \varepsilon' - \varepsilon'' \cong \text{stored energy - dissipated energy} \tag{5.6}$$

$$\varepsilon'' = \frac{\sigma_{eff}}{\varepsilon_o \omega} \tag{5.7}$$

Where, ε is the permittivity, ε_o is the permittivity in free space (8.85×10^{-12} F/m), ε_r is the relative permittivity and χ_e is the electric susceptibility. Eq. 5.6 defines another mathematical definition of relative permittivity in terms of loss factor [124], [125].

Where, ε' is relative permittivity of the material and ε'' is loss factor related to the dielectric material. Loss factor is a complex component and can be calculated using Eq. 5.7 [125]. Where, σ_{eff} is effective conductivity of the material and ω is the angular frequency.

5.2.4 Conductivity and loss Tangent

The effective conductivity or total conductivity of a dielectric material is dependent upon static or (ionic) conductivity and conductivity due to the applied alternating electric field [123]. Effective conductivity is given by Eq. 5.8.

$$\sigma_{eff} = \sigma_s + \omega\varepsilon'' \tag{5.8}$$

Where, σ_s is static conductivity that is independent of the operating frequency, and $\omega\varepsilon''$ is contribution of time varying electric field to effective conductivity that is dependent on the operating frequency.

5.3 Effect of Time Varying Electric Field on Biological Tissues

5.3.1 A Water Molecule

The effect of time varying electric field on biological tissues can be explained with reference to the concepts discussed in the preceding section. Thermal effect is produced as a result of the interaction between biological tissues and time varying electric field. Biological tissues depict properties similar to a dielectric material and the increase in temperature is attributed to the power dissipation due to permittivity and conductivity. Loss factor is an imaginary component of complex permittivity of a dielectric material that describes phase lag to the electric field because of polarization [123]. When electric field is applied to an atom; electrons and nucleus start to align along the direction of electric field, which results in stretching effect on an atom and creation of a dipole as illustrated in Fig. 5. 1.

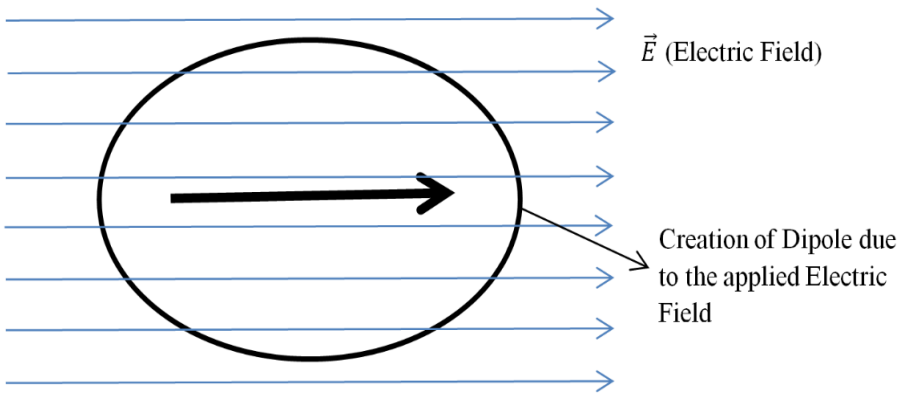


Fig. 5. 1: Creation of dipole as a result of applied electric field

Biological cells and tissues have varying amount of water content present in them. Thus, it is pertinent to discuss the behaviour depicted by water molecules when subjected to alternating electric field. Water (H_2O) is a polar molecule that has an already existing dipole as illustrated in Fig. 5. 2.

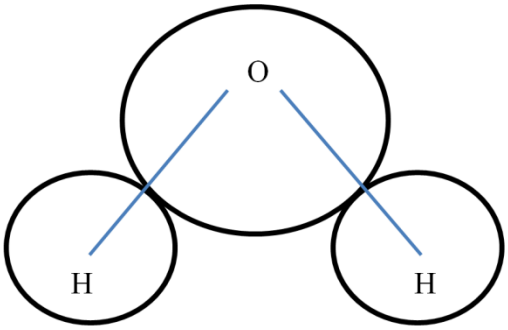


Fig. 5. 2: A dipole water molecule

Vorst (2006) in [123] suggests that: *"An alternating electric field results in polar molecules like water to get a dipole rotation (or polarization). As a reaction to this dipole rotation by the intramolecular forces and adjacent molecules, energy is distributed through the material. This energy loss is the heat dissipated*". Alternating electric field gets a phase lag because of the finite time taken by the molecules to polarize. This lag or time delay is known as relaxation time [123].

5.3.2 Conductive and Radiative Mechanisms of Electromagnetic Waves

Depending upon the operating frequency range, heating in the human tissue is classified in two types: Radiative and Conductive.

Conductive Heating

Joules law defines that heat is produced whenever electrical current passes through a resistor (or impedance). Tissues having complex impedance, convert electrical energy into heat when an electrical current pass through them causing the tissue temperature to rise. This rise in temperature has various effects on cells and tissues. These effects have been explained in subsequent sections. Heating in the frequency range of 100 kHz to 5 MHz is classified as RF heating and is resistive or conductive heating. An antenna structure within RF ESUs, unlike the surgical blade, is not sharp and uses electrical energy to perform biological tissue cutting. Thus, it can be introduced in the human body to perform keyhole laparoscopic or endoscopic surgery with minimal risk to the patient, reducing bleeding and recovery time [6]. Energy in this frequency range is particularly effective for cutting and desiccating biological tissues. However, it cannot be utilised to

perform thermal ablation or coagulation (these concepts will be discussed later in this chapter).

Radiative Heating

Radiative heating has enabled the development of microwave surgical units operating above 400 MHz. With suitably designed antenna structures, EM waves can be radiated into the human tissue to produce localised heating and thermal ablation. Microwave energy at this frequency range provides efficient means of performing vessel coagulation to stop bleeding or ablate tissues that may or may not be cancerous by producing localised heating. It has been indicated earlier that human cells and tissues are lossy structures because of their complex impedance. Energy at microwave frequencies exploits lossy behaviour of human tissues and polarised water molecules by causing molecular dipole rotation to produce localised heating. Antenna design plays an important role in using microwave energy in the ESUs. They match complex impedance of a particular tissue at the frequency of operation to impedance of radiating antenna. This can treat various higher impedance organs like lungs and bones compared to soft tissues that have lower impedance, while ensuring that energy is only delivered to the target tissue and not the surrounding structures that are healthy [6].

5.3.3 Effect of Temperature on Cells and Tissues- Biological Perspective

Knowledge about the effect of temperature on human cells and tissue from the biological perspective is important for the design and development of biomedical devices. Normal body temperature is in the range around 36°C and can reach as high as 40°C during infection or illness without damaging human cells and tissues. An increase in cellular temperature to 50°C can cause cell death in approximately 6 mins while an increase to 60°C can cause instantaneous cell death [126], [127]. Fig. 5. 3 shows the effect of temperature on human cells and tissues which has been reproduced from [3].

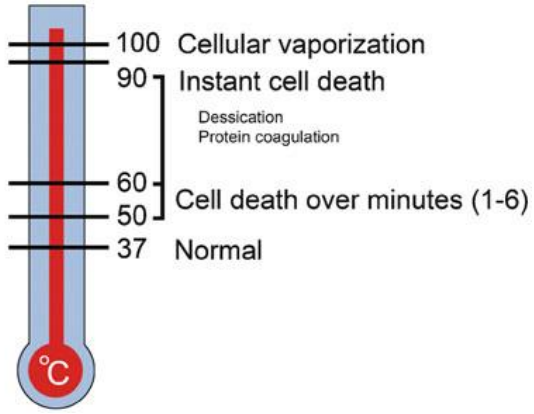


Fig. 5. 3: Effect of temperature on human cells and tissues [3]

As indicated by Fig. 5. 3, the two processes that occur at temperatures above 60°C are protein denaturation and cell desiccation or dehydration. At a local cell temperature of 60°C, hydrothermal bonds between the protein molecules break instantaneously. These bonds are reformed when the temperature cools down. The breaking and reformation of hydrothermal bonds between protein molecules is known as thermal coagulation or white coagulation [127]. The process of coagulation is very important as it stops bleeding during electrosurgical procedures. The other effect is cell desiccation or dehydration which occurs when the cellular wall is thermally damaged, and the cells lose water content in them [3]. At intracellular temperatures around 100°C, intracellular liquid to gas transformation takes place when water boils to form steam. This causes massive intracellular expansion resulting in explosive vaporization of the cell. At further higher temperatures of 200°C, carbonization of human cells and tissues take place where organic molecules break down to form carbon molecules having dark brown or black appearance. Carbonization of cells and tissues is also referred to as black coagulation [3], [126].

5.4 Depth of Effect and Absorption

5.4.1 Skin Depth and Shielding Effect

Microwave energy has been found useful for surgical devices and therapeutic systems because of the slight conductive nature of human tissue. Whenever a conductive material is exposed to an EM field, it is actually presented to a current density caused by moving charges. For good conductors, conduction current is directly proportional to the electric field and will be higher for high conductivity materials. However, biological tissues are not good conductors and do not conduct a current because of their low conductivity values. Diffusion equation for good conductors can be solved and decay parameter can be derived as Eq. 5.9 below [123]:

$$\delta = \frac{1}{\left(\frac{\omega\mu\sigma}{2}\right)^{\frac{1}{2}}} \tag{5.9}$$

Eq. 5.9 shows that amplitude of EM fields decays exponentially inside the conductive material. The parameter δ is called the skin depth and is defined as the distance at which the fields reduce to approximately 37% (1/2.7) of the value they had at the interface. Besides exponential decay factor, another important aspect to consider in Eq. 5.9 is the inverse relationship between frequency and skin depth [123]. With an increase in frequency, skin depth decreases inversely to the square root of frequency. Skin depth expression presented in Eq. 5.9 is for good conductors, where displacement currents are

negligible compared to the conduction current. The concept of displacement currents was given by Maxwell once he was linking the laws presented by Ampere, Faraday and Gauss, which are famously known as Maxwell's equations. When we consider the interaction of human tissue with EM fields, displacement currents are comparable to conduction current. Thus, a more generalized expression was derived in [123] for skin depth that can be applied to human tissue, this has been shown in Eq. 5.10.

$$\delta = \left(\frac{1}{\omega}\right)\left\{\left(\frac{\mu\varepsilon}{2}\right)\left[(1+p^2)^{\frac{1}{2}}-1\right]\right\}^{\frac{1}{2}} \tag{5.10}$$

Where, $p = \sigma/\omega\varepsilon$ is the ratio between amplitudes of conduction current and displacement current. For large values of p, Eq. 5.10 reduces to Eq. 5.9. Shielding effect is defined as the concentration of fields, currents and charges near the surface of the conducting material. The physical significance of this effect can be explained by considering that field amplitude is reduced to 5 % at a skin depth of 3δ with a corresponding power of 1 % compared to its amplitude at the interface. Field amplitude further reduces to only 1 % with corresponding power to 10^{-4} at a skin depth of 5δ, indicating isolation of 40 dB [123]. The concepts of skin depth and shielding effect become fairly significant above 10 MHz for human and larger vertebrate subjects. Shielding is much easier to achieve at higher frequencies; however, skin depth is reduced [3], [7], [127], [128]. Thus, when using microwaves for medical based applications, penetration will reduce as a function of increasing frequency and efficiency of the application might reduce [123]. However, internal organs will be more shielded at higher frequencies compared to lower frequencies on exposure to an EM field. Table 5. 1 summarises skin depth values for human tissues at various frequencies. The table has been reproduced from [123] which considers EM properties of the tissues as well as their variation as a function of frequency.

Table 5. 1: Typical skin depth in human tissue [125]

Parameter (units)	**Radio FM**	**TV Transmitter**	**Telephony Mobile**	**Telephony Mobile**
Frequency (MHz)	100	450	900	1800
Skin depth (cm)	3	1.5	1	0.7
Depth at which power reduces to 1% (cm)	9	4.5	3	2

5.4.2 Specific Absorption Rate

Biological effects that occur due to interaction of microwaves with human subjects depend on the field that is generated in the human tissue. The field is described in terms

of specific absorption rate (SAR) which is the power absorbed (in watts) per unit mass (in kg) of human tissue [8], [127]. Human tissues primarily differ in their permittivity which varies with frequency. An important phenomenon that has to be understood for human subjects is Relaxation. Maxwell-Wagner relaxation associated with biological cell membranes take place at about 100 to 500 MHz [127]. The cellular nature of human tissue tends to form large number of dielectric partitions that separate the two strongly conducting compartments called intracellular and extracellular compartments. Coombs (1959) in [129] describes that poorly conducting membranes having a typical resistance of $3 - 100\ \text{k}\Omega\text{cm}^{-2}$ surround the cells which lie within an extracellular space and have a specific resistance around $4\ \Omega\text{cm}^{-1}$. Thus, human tissues may be modelled in accordance with Maxwell's experimentation where membrane structures contribute in a complex manner to the dielectric behaviour of human tissues. Microwave diagnostic devices have been developed by exploiting the difference between permittivity of diseased tissue and healthy tissue to detect abnormalities along-with their location [130].

Lin (2012) in [130] discusses various thermal effects on human tissues and cells on exposure to RF and microwave energy. It has been shown that an estimated 1°C increase in human body temperature takes place for every 1 W/kg of SAR. These thermal effects have led to the development of Hyperthermia which is a technique used for the treatment of cancer, tumours and other medical procedures [6]. Localised heat is provided to the tumours causing heating to therapeutic temperatures of around 43 to 45°C.

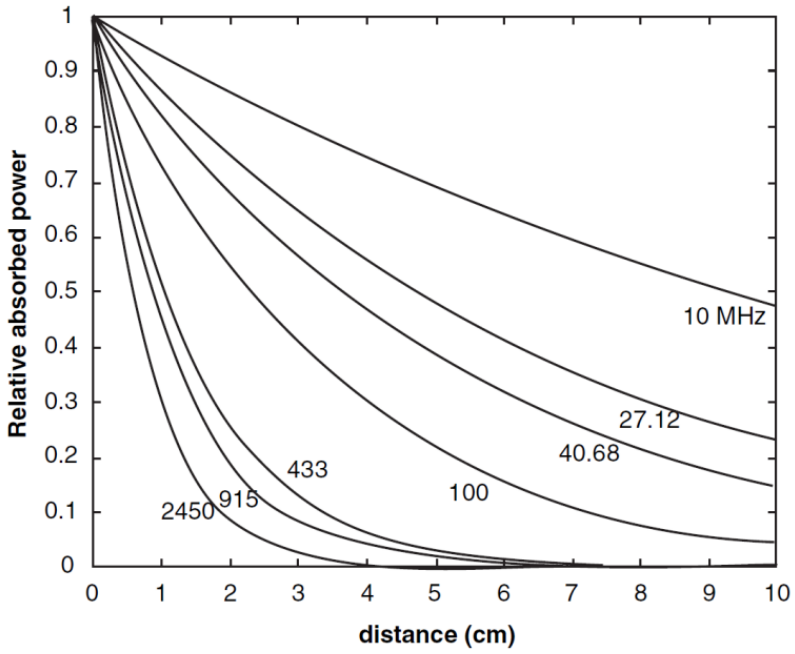


Fig. 5. 4: Power absorbed in muscles as a function of the skin depth at various frequencies [125]

Fig. 5. 4 (reproduced from [123]) presents variation of power absorbed inside the human body as a function of penetration depth at microwave frequencies. It shows that human body becomes less transparent to non-ionising EM waves with an increase in frequency. However, humans are not transparent for the optical range because skin depth is considerably small [6].

5.5 RF Heating

5.5.1 Introduction and Background

The process of heating within the human tissue was explained to occur as a result of ionic conduction and vibration of the dipole molecules of water, fat and protein. Power absorbed by the tissue that causes heating is dependent upon cooling behaviour depicted by the tissue and the pattern of fields being absorbed. Field pattern is a complex function of tissue geometry, dielectric properties of tissues, operating frequency and source configuration [5]. The thermal effect produced on the tissue is also dependent on the thermal properties of tissues and neuro-circulatory mechanisms [7]. These effects also define thermoregulatory capabilities of the systems or individual parts of the system, exceeding these could cause severe tissue damage and even death that occurs when absorbed power levels are well above the metabolic output power of the body. Thus, the need for controlled heating needs to be highlighted along-with the definition of non-uniform absorption model.

Dielectric properties of the human body are an important factor that can be utilised to explain various concepts underlying RF heating [5]. This is important because heating patterns induced by radiations and the field absorbed by the human tissue is non-uniform and dependent on the dielectric constant. This has been discussed by Chou (2018) in Chapter 12 of [7]. When human subjects are exposed to RF or MW energy, only part of the incident energy penetrates the human body while the remaining energy reflects back. The amounts of energy reflected and penetrated within the human body is a function of dielectric properties. Biological tissues belonging to different parts and organs of the human body have different dielectric constant values. Higher water content human tissues tend to have higher values of dielectric constants compared to the lower water content tissues. Hence, we can classify biological tissues into two major categories [7]. Tissues with higher water content include muscle, skin, kidney and liver. Thus, these have higher dielectric constant values compared to fat or bone which have low water content. On the other side, intermediate water level tissues include brain, lung and bone marrow tissues. When considering RF frequencies, human tissues with high dielectric constant values are

better conductors of electrical current compared to those with lower values of dielectric constants. This occurs because of polar water molecules and ions. On the other side, fat and bone tissues have little water content and thus, bounded charges, not supporting conduction currents [7]. Dielectric constant is also dependent upon the frequency of RF or microwave energy and decreases with an increase in frequency. Some dielectric constant values of muscle tissues as a function of frequency have been shown in Fig. 5. 5 which has been reproduced from [123].

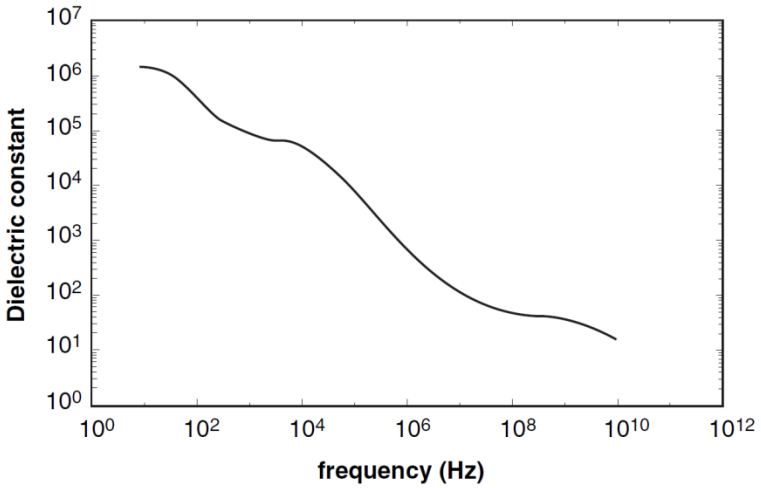


Fig. 5. 5: Dielectric constant values of muscle tissues as a function of frequency [125]

The non-uniform nature of human tissues is responsible for reflections occurring at the interfaces between tissues of different dielectric constants or conductivities. Considerable standing waves can be produced due to these reflections. Hot spots are also accompanied and can be maximum in either tissue, regardless of their conductivity or dielectric constant value [5]. These effects make tissues with low blood circulation or temperature cooling more vulnerable of being damaged, these tissues include lens of the eye, gall bladder and parts of gastrointestinal tract [123].

5.5.2 Fourier Law of Heat Conduction and Temperature Profile

Heat conduction allows heat dissipation though the targeted treatment volume of human cells or tissue. This mechanism occurs because of the temperature difference or gradient between targeted tissue volume and surrounding tissues. Calculation of heat flux density can be described by using differential form of Fourier's law given in Eq. 5.11 [131]:

$$\vec{q} = -k\nabla T \tag{5.11}$$

Where, $\vec{q}$ is heat flux density, k is thermal conductivity and ∇T is temperature difference or gradient between the two tissues.

Whenever a tissue is subject to RF energy, heating mechanism takes place as discussed in the preceding sections, the rate of heating (HR or heating rate) or temperature rise is a function of SAR and is given by Eq. 5.12 [7].

$$\text{HR} = \frac{SAR}{69.77C_H}\,(°\text{C/min}) \tag{5.12}$$

Where, c_H is the specific heat capacity of tissue (kcal/kg°C). SAR is related to electrical field produced in the tissue and tissue conductivity according to Eq. 5.13 [7].

$$\text{SAR} = \frac{\sigma}{\rho}E^2\,(\text{W/kg}) \tag{5.13}$$

Where, E is root mean square value of the induced electric field strength in the tissue (V/m), ρ is density of the tissue (kg/m^3), σ is dielectric conductivity of the tissue (siemens/m). Penne's Bioheat equation was developed in 1948 to evaluate heat flow in biological tissues. It gives the final tissue temperature as a function of deposited energy, metabolic heating rate Q_m, power dissipation by thermal conduction $k\nabla^2 T$, and blood flow $c_b w(T - T_a)$, Penne's bioheat equation has been shown in Eq. 5.14 [7], [128].

$$\rho c_H \frac{dT}{dt} = k\nabla^2 T + SAR + Q_m - c_b w(T - T_a) \tag{5.14}$$

Where, T is temperature (°C) and k is thermal conductivity (W/m°C) of the tissue respectively, Q_m is the metabolic heat generation (W/kg), c_b is the blood heat capacity (kcal/kg°C), w is the blood perfusion rate (kg/m^{3}s) and T_a is temperature of the incoming arterial blood (°C). Bioheat equation gives a good approximation for heat transfer between human tissues given that the temperature remains below 90 °C. A typical soft tissue tumour clinical treatment presented in [7] has a temperature profile illustrated in Fig. 5. 6 where an external applicator provides an output power of 50 W.

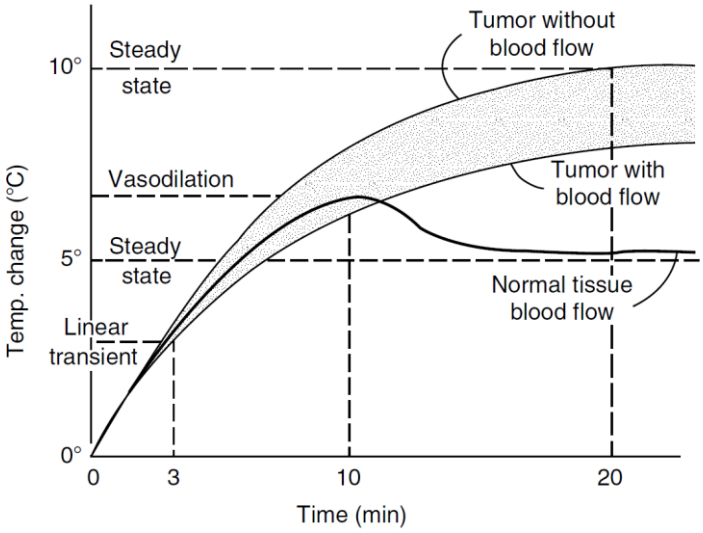


Fig. 5. 6: Comparison between the effect of temperature change in normal tissues versus tumours due to the application of RF energy [7]

When soft tumour tissues are exposed to RF energy, a linear increase in temperature is initially observed which can be represented in the linear transient stage. This stage lasts for about 3 min and provides an increase in temperature around 2.5 °C. Linear transient stage is followed by a period of non-linear temperature rise lasting for about 7-10 min. In this stage heat diffusion takes place and temperature becomes high in dissipating the absorbed energy. For tissues without blood flow, a longer linear behaviour is observed until a steady state temperature as indicated by the SAR is achieved. On the other side, for tissues with blood flow (vascular tissues) a marked increase in blood flow will occur due to vasodilatation when the temperature rises to hyperthermia temperatures in the range of 42 to 44 °C. At this stage the value of $SAR = k\nabla^2 T + c_b w(T - T_a)$ and is an indicative of both the processes of heat diffusion and blood flow cooling [7].

This characteristic of increasing blood flow to the treatment area is the basis for diathermy treatment. During hyperthermia (or diathermia) treatment process, variable blood flow is observed with respect to tumorous tissues, with strong blood flow at the edges and slow in the core. Generally, there is no vasodilatation during heat treatment because of fully open blood vessels in tumours. Once steady state condition is achieved, temperature of the affected tumorous tissue is higher than the surrounding normal tissue and this difference in temperatures is indicated through shaded area in Fig. 5. 6. Lower boundary of shaded area indicates temperature at the edges while upper boundary indicates temperature at the core [7]. Another important consideration for the treatment of tumours by utilising hyperthermia is maintenance of therapeutic temperature levels for most of the treatment duration. This can be achieved by ensuring that SAR level is sufficiently high.

One of the key differences between hyperthermia (or diathermia) and RF ablation (discussed in the next sub-section) is the level of SAR. For hyperthermia, there is a gradual increase in temperature that is achieved over longer time duration with comparatively lower SAR; however, for RF ablation significant increase in temperature between 15-60 °C is achieved very rapidly over shorter duration of time (generally less than 6 mins). SAR for RF ablation is significantly high and the required benefits are achieved before diffusion takes place [7].

Hyperthermia is suited for lower range of microwave frequencies, generally lower than 300 MHz [5]. Penetration of RF energy is an important factor to achieve required therapeutic temperatures on the affected tumorous tissue, and because of lower penetration levels and skin depth of RF energy beyond 2450 MHz, there is no practical significance [7], [8], [126]. However, at lower RF or microwave frequencies where penetration levels are high, the devices are large and cumbersome. For superficial treatment applications where is targeted skin depth is 2-5 cm, 915 MHz has been found suitable [7].

5.5.3 RF Ablation and Clinical Applications

Chou (2018) in [7] suggests that *"Radiofrequency ablation (RFA) is a modified electrocautery technique that destroys tissue by means of electric current"*. The surgical procedures of RF Ablation involve cauterization of small blood vessels to stop bleeding by utilising high frequency electric current. Over the past few decades, RFA has evolved into a procedure for creating thermally induced coagulation in tumorous cells either through image guided approach or through surgical procedures. This procedure is known as 'coagulation necrosis' and the necrotic tumour disappears after becoming significantly small [132]. The surgical procedure of RF Ablation generally operates in the frequency band between 375 to 500 kHz to produce ionic currents in the tissue to produce resistive heating to at least 50 °C [7]. The process of coagulation necrosis takes place in a short duration of 4-6 sec at temperatures between 50 to 52 °C, this can also be caused within a duration of 2-3 sec if heating of 100 °C can be caused. However, excessive heating beyond 100 °C can lead to tissue boiling and vaporisation thereby increasing the impedance and reducing tissue ablation. Thus, temperature between 50 to 100 °C should be maintained in the targeted tissue volume during RFA procedure [7], [132].

Practically, RFA procedure is carried out for a duration of 4-6 mins by introducing RF electrodes at the core of affected tissue, where heating of 50 to 100 °C is produced. Depending upon electrodes, thermal conduction from electrodes to the affected tissue can

also cause duration of the procedure to increase to about 30 min. Since heating of 50 to 100 °C is required to be produced across the entire volume of affected tissue, thus, techniques like increased generator power, expandable and multi-tip electrodes can be used to expand the volume. Besides this, to prevent overheating and enable controlled heating, impedance changes are directly measured [7], [121]. Thus, issues that still need to be addressed for RFA include achieving large volume of RF tissue ablation, controlled heating while considering cooling from nearby blood vessels, prevention of tissue boiling and vaporization.

Clinical Applications

RFA has shown decent performance for treating liver tumours where the only curative treatment is liver resection. Since, only 10-20% patients with liver tumours have a resectable disease, thus, percutaneous RFA has been a popular low risk treatment procedure [133]. RFA has also shown similar performance in treatment of kidney tumours that are less than 3 cm in diameter. Success rate of treating small kidney tumours has been between 70 to 90%, while local recurrence has a higher risk of occurrence for tumours that are larger than 3 cm [7]. RFA has shown highly effective and safe results for the treatment of osteoid osteoma that is a benign and slow growing painful lesion within bones. RFA can be produced through a probe that is placed through a bone-penetrating cannula and activated for 4-6 mins at 90 to 100 °C [134], [135]. Success rates between 91 to 94% have been demonstrated [7]. RFA surgical procedures have seen remarkable progress over the past decade with follow-up studies opening up new dimensions; however, there still remain many challenges some of which were discussed in the introductory chapter.

5.6 Portable Haemostasis Device

5.6.1 Introduction

An application area envisaged for power amplifiers presented in Chapter 4 is portable haemostasis device that is capable of producing coagulation of bleeding vessels in environments where specialised coagulation procedures (like in operation theatres) couldn't be performed, and conventional haemostasis procedures are ineffective. It has been discussed that uncontrolled haemorrhage from major trauma and injuries sustained in the battlefield are a leading cause of deaths in the battlefield. Various studies and statistical analyses have been conducted to ascertain the effectiveness of treatment procedures that could help save lives. For instance, it has been discussed in [136] that up to 69 % of the 80 % potentially survivable cases in the battlefield had torso or junctional

based injuries which couldn't be saved through standard tourniquet methods. Specialised coagulation procedures like those used in operating theatres and accidents and emergency units however have remarkable efficacy; but they are large and cumbersome which makes them impractical to carry to the battlefield. Most commonly used haemostasis procedures discussed in [137] include: factor concentration- which causes rapid absorption of water essentially drying out blood to increase clotting ability, mucoadhesive- which is an adhesive that can seal wounds, and procoagulants- which provide artificial supply of coagulant factors to increase coagulation ability and clotting. However, these dressings and coagulation procedures have limitations [138] that include difficulty in application in bad weather conditions when its windy or raining, and increased likelihood of burns or extraneous tissue damage caused by the powder and coagulation agents.

Initial research and testing were conducted in collaboration with Bangor University to develop a portable microwave applicator that is capable of delivering sufficient microwave energy at 5.8 GHz to effectively coagulate bleeding sites which cannot be treated with standard tourniquet methods. The device could be used as a long-term solution if specialised facilities are not readily available, or as an interim procedure to facilitate emergency evacuation to specialised emergency services. Rendered model of the portable haemostasis device shown in Fig. 5. 7 was proposed by the author of this thesis in [101].

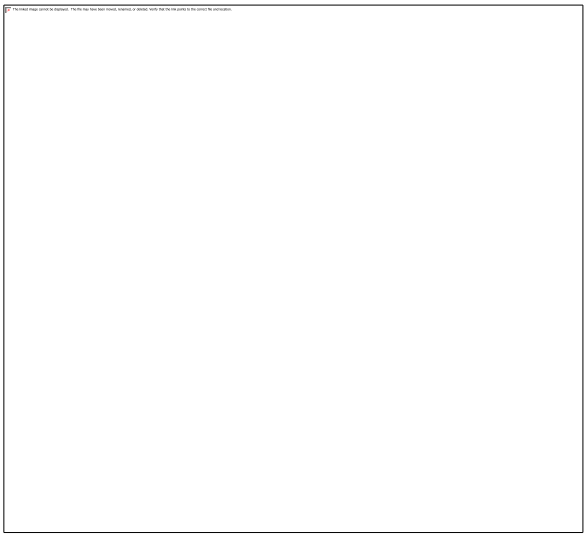


Fig. 5. 7: Rendered model of portable haemostasis device

The device broadly consists of two parts, power pack that houses microwave power source, high power amplifier, cooling mechanisms and a removable battery; and handheld applicator with a radiative tip which can be shaped to allow the practitioner to apply local tamponade to the site while delivering microwave energy. Review of coagulation, SAR,

skin depth and temperature profile presented in preceding sections indicated that the best chance of achieving haemostasis from the portable device would require as much energy as possible to be delivered whilst maintaining a controllable and even delivery through the coagulation process. The ability to achieve coagulation in such a manner has been demonstrated in a number of clinical application which have been discussed in [6], however, those clinical applications require large microwave power generators which cannot be used in a portable device. Thus, biggest challenge in the development of portable haemostasis device was generation of microwave power with minimum DC power consumption and heat dissipation. Active cooling mechanisms in the power pack could permit effective heat dissipation for continuous use of the applicator whilst removable batteries could provide DC power for each coagulation procedure and can be readily replaced for successive coagulation procedures. Requirement for the power amplifiers were to produce over 20 W CW microwave power with over 60 % efficiency at 5.8 GHz for which various amplifier. The envisaged portable haemostasis device could help medical units in the battlefield or emergency and calamity stricken areas to accurately and safely perform coagulation of bleeding vessels to provide an interim treatment and a chance to survive until the extrication of patients to further care facilities.

5.6.2 Applicator Structure and Power Levels

Various applicator structures for portable haemostasis device at 5.8 GHz were developed at the Medical Microwave Research Group at Bangor university which have been presented in [101], [118], [120]–[122]. The applicator structure essentially houses a radiative tip made with high dielectric constant machinable Macor to allow optimum energy delivery into the tissue for controlled and accurate coagulation. Various simulations and optimisation in CST Microwave Studio were performed to match the feed cable from the power amplifier and the tissue to allow optimal delivery of microwave energy with minimal losses. The radiative tip presented in [101] was simulated pressing against a block of liver to achieve optimised matching and power delivery at 5.8 GHz. Energy dispersion was observed to be concentrated and restricted to a small area which was an important result that suggested that energy was being delivered to the targeted area effectively. Simulated thermal profile presented in [101] has been shown in Fig. 5. 8, which indicates that a temperature of 360 °C could be achieved at the tip; however, the thermal profile and simulation model in CST doesn't take into account various factors (discussed in Section 5.4) like steam generation which happens at temperatures ~ 100 °C,

perfusion and the human body's ability to thermoregulate itself which essentially reduce the temperature.

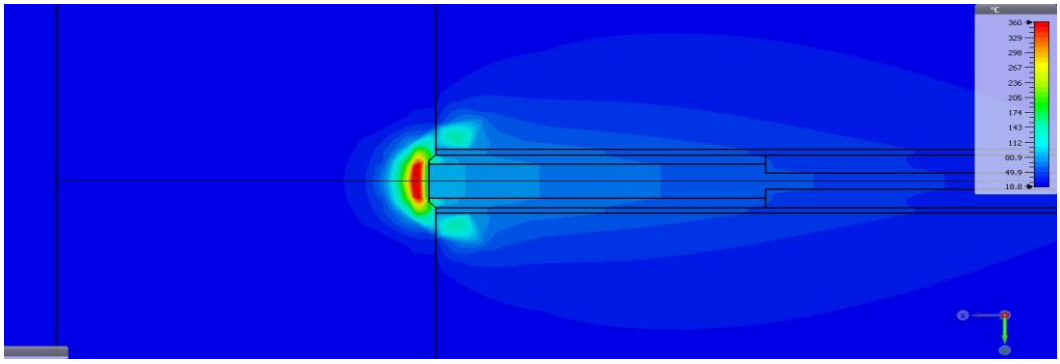


Fig. 5. 8: Thermal profile of the radiative tip simulated in CST microwave

Other radiative tip structures to perform coagulation at 5.8 GHz have been presented in [118], [121]. Simulation results of the main ablation area presented in [118] have been shown in Fig. 5. 9.

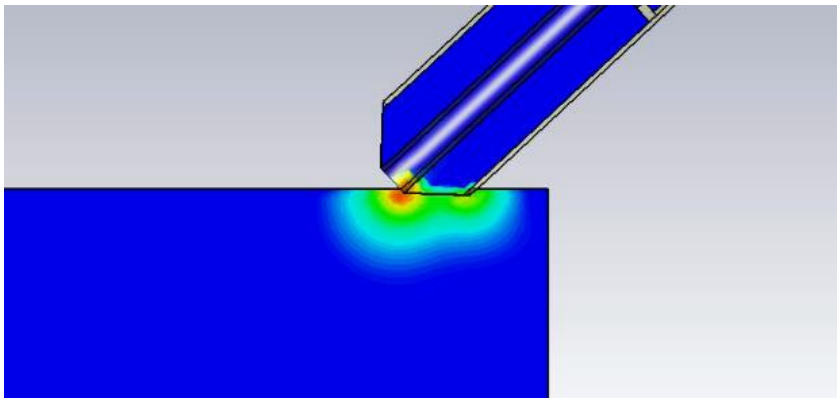


Fig. 5. 9: Simulation results showing energy delivery profile and main ablation area

5.6.3 Testing and Analysis

This section presents testing of power amplifiers that were presented in Chapter 4 on porcine liver bench model, these results were presented by the author of this thesis in [101], [118], however, they will be reproduced here for discussion.

Test 1

For the first test, class F amplifier was used alongside the applicator discussed in [101] at two different settings, i.e. 1) maximised PAE over 57 % and 13.8 W microwave power, and 2) maximised output power over 16 W at deep compression levels and reduced PAE. The initial lab tests were aimed to ascertain ability of the amplifiers to deliver energy into porcine liver and assess the level of coagulation caused. It also helped to assess matching conditions of the applicator structure for further optimisation. Fig. 5. 10 shows results of energy delivery sites into a porcine liver bench model.

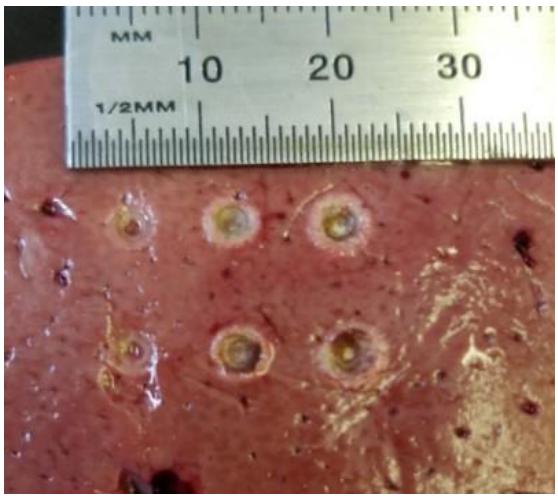


Fig. 5. 10: Microwave energy delivery sites on porcine liver bench model

In Fig. 5. 10 coagulation sites corresponding to two settings mentioned above at maximised PAE and output power have been shown in the top and bottom rows, respectively; for a duration of 10, 20, and 30 sec from left to right. Energy delivery in a relatively small and controlled area can be observed. White regions of the energy delivery sites shown coagulation, darker regions show vaporised tissue where water content has been lost as steam, while the darkest regions shown carbonization.

Test 2

For the second test, multistage amplifier providing 22 W CW microwave power at 5.8 GHz with over 65 % total efficiency was used alongside the applicator discussed in [118], [121]. Applicator for the second test included a hollow coaxial cable and haemostatic probe shown in Fig. 5. 11. These were much improved results compared to test 1 and showed efficacy for the device to achieve coagulation.

Fig. 5. 11: Microwave energy delivery sites with a hollow coaxial cable and haemostatic probe on porcine liver model

5.7 Conclusion

This chapter presented basic concepts that explain the interaction of RF and microwave energy at various operating frequencies and power levels. The efficacy of amplifiers developed in Chapter 4 was demonstrated for use within a portable haemostatic device in field medical application areas where conventional modalities are ineffective to cause coagulation of bleeding sites. Initial tests were conducted in collaboration with Bangor university and Creo medical, which showed the desired energy delivery profile on porcine liver model in a controlled and relatively small environment. Future iterations of power pack of the rendered model will include a hybrid MIC with onboard VCO and multistage amplifiers and air cooling mechanisms for effective heat dissipation.

Chapter 6

Class AB Amplifier MMIC

6.1 Introduction

High efficiency power amplifiers discussed in preceding chapters of this thesis were targeted for C-band medical applications for the treatment of various medical conditions through coagulation (or ablation) of tissues and tumours. However, higher microwave frequencies in the Ka-band (~30 GHz) have shown efficacy in medical application areas that include cell neutralisation or immunology and tissue characterisation [139]. Cell neutralisation or immunology is essentially a process of blocking or restricting the spread or replication of various cells, which can be performed using millimeter wave energy to treat a range of brain tumours or cancers; especially glioblastoma and medulloblastoma. Glioblastoma cells (or astrocytoma) are categorised as highly malignant grade IV cancerous cells that contain a mix of various abnormal cell types and blood vessels; which can be found anywhere in the brain (generally in the cerebral hemisphere) and spinal cord. A very high percentage of glioblastoma tumorous cells are replicating or dividing at any time and the literature suggests that glioblastoma is a very difficult cancer to treat [140]–[142]. On the other side; medulloblastoma are very fast replicating grade IV or higher grade cancerous cells that are found in the cerebellum with a high likelihood of spreading to other parts of the central nervous system (CNS) including the spinal cord. It has been suggested in the literature that medulloblastoma has high rate of occurrence in children (12-25 % of all CNS tumours) compared to adults where the occurrence rate is rare [143], [144]. Both these cancers are very aggressive and the treatment procedures include resection surgeries through image guided procedures and intra-operative magnetic resonance imaging (iMRI), medical therapeutic procedures through molecular targeted and anti-angiogenic agents, immunotherapy and gene therapy, and image-guided radiotherapy and stereotactic radiosurgery [140].

Class AB amplifier operating at 30 GHz presented herein has been envisaged for implementation within an on-chip device for the diagnosis and neutralisation of glioblastoma and medulloblastoma brain cancers which is a part of European Union's Horizon 2020 research and innovation program. The amplifier has been developed in support from Semtech Limited and collaboration with Bangor university and Creo medical. The latter two are part of a broader research collaboration that brings together molecular biologists, healthcare professionals and electronic engineers from various

healthcare organizations and universities to develop microtechnology that can enable the diagnosis and treatment of stem cells that the scientists believe can cause cancer recurrence and tumour regrowth. Identification of cancerous cells is conventionally performed through biopsy followed by laboratory tests that can take up to 6 weeks [9]; however, on-chip identification of cancerous cells involves behavioural analysis and discrimination based on their movement and reaction to millimeter and optical ionising electromagnetic waves. Stem cells having potential of recurrence can be neutralised on chip. This way, the development of specialised electrosurgical devices can treat cancerous stem cells at the tumour site [145]–[147].

Power amplifiers are described as the largest power consumption module in a microwave system; whereas the on-chip diagnosis and treatment system described above requires around 17 dBm CW output power with minimum DC power consumption and heat dissipation. Class F and F^{-1} amplifiers reviewed in Chapter 3 provide decent performance in terms of efficiency and output power; however, their complex harmonic termination networks which include quarter wavelength transmission lines occupy a large area on the IC, even with meandering and other space optimisation techniques. For instance, $50\ \Omega$ quarter wavelength transmission line on WIN PP10-15 process measures 326×96 μm, which would occupy a large area on 1510×1330 μm die (cell) size that was made available to the author on the tape-out wafer. The effective area was further reduced due to GSG probes at input and output ports. Another limiting factor was a lower breakdown voltage and the ability to support high enough electric fields of GaAs technology compared to GaN technology. Class F and F^{-1} amplifiers have been discussed to be more suitable for implementation using GaN technology where the fundamental voltage component can rise over $2V_{max}$. Thus, class AB amplifier was developed with a shunt capacitor at the drain terminal for second harmonic manipulation and control over higher order harmonics to limit voltage peaks under compression. The transistor was biased under class AB conditions through bias tees at the input and output ports. Comparable performance to class J, class F and F^{-1} amplifiers was observed that will be discussed later in this chapter.

This chapter has been organised as follows. Section 6.2 presents design flow and topology of class AB amplifier. Section 6.3 presents DC IV analysis and parameter extraction of 2×50 μm GaAs pHEMT transistor from PP10-15 pdk where an estimation of C_{ds} will be utilised to identify appropriate shunt capacitance with the drain to provide short circuit conditions to the second harmonic component. Section 6.4 presents load pull simulations

to identify optimum source and load impedances at the fundamental frequency through simulations performed in Keysight's ADS followed by Section 6.5 where the design of source and load termination networks has been discussed. Section 6.6 presents results and analysis of class AB amplifier based on EM simulated results in Momentum microwave and initial [S]-parameter on-wafer measurement results. Section 6.7 will provide some concluding remarks.

6.2 Circuit Topology and Design Flow

6.2.1 Circuit Topology of Class AB Amplifier

Detailed review of class AB amplifiers and their comparison with class B and class J amplifiers was presented in Chapter 3. Briefly recalling the definitions; class AB amplifiers are reduced conduction angle amplifiers which have rectified current and pure sinusoidal voltage waveforms at the drain. The current waveform swings between 0 and I_S (or I_{max}) by means of appropriate bias conditions and input power drive level; where zero current level essentially represents the swing of input power level below cut-off. Classical definition requires provision of complex load impedance at the fundamental component and short circuit impedance at second and higher order harmonics at the drain terminal. However, reactive impedance to the second harmonic may also be provided in class AB amplifiers. Class J amplifier is defined as a special case of class AB amplifier; where the transistor is biased at deep class AB/class B load lines with reactive second harmonic and resistive fundamental load impedances at the drain [41].

It has been discussed by Cripps (2006) in [41] that reactive harmonic conditions at the second harmonic component can provide improved linearity, output power and reduced circuit complexity compared to short circuit conditions with similar efficiencies. Improved output power and reduced circuit complexity are desired for the targeted application. Fig. 6. 1 shows circuit topology for class AB amplifier presented in this chapter where the transistor has been represented in terms of small signal lumped component equivalent circuit model. Towards the gate side, fundamental source network and shunt stabilisation network provide maximum power transfer (optimised with source pull) and stability to the transistor, respectively. Shunt capacitance (C_{DH}) to the drain provides reactive second harmonic condition (ideally short circuit) and short circuit conditions to higher order harmonics, followed by fundamental matching network which can be designed for high efficiency and output power using impedances from load pull. It was discussed in Section 3.5 that the effect of gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) is negligible towards the output capacitance (C_{out}); thus, the

output capacitance will be assumed as: $C_{out} \approx C_{ds}$. The circuit topology shows transistor's transconductance (current generator) parallel with output capacitance C_{ds}, the latter can be estimated using on-wafer $[S]$-parameter measurements of device pull-outs or through simulations using transistor model from pdk, which will be discussed in the following section. Parasitic elements (R_g, R_d, L_g and L_d) can be represented as gate and drain transmission lines which will be de-embedded to obtain correct impedances at the transistor's intrinsic places (represented through dotted line in Fig. 6. 1). This would also help to identify the effect of the output capacitance C_{DH} towards higher order harmonics. Third and higher order harmonics are assumed to be short circuited by the parallel combination of C_{ds} and C_{DH}, however, generation of odd order current harmonics and corresponding voltage harmonics under compressed operation can cause an increase in the third harmonic content and current or voltage waveform altercation.

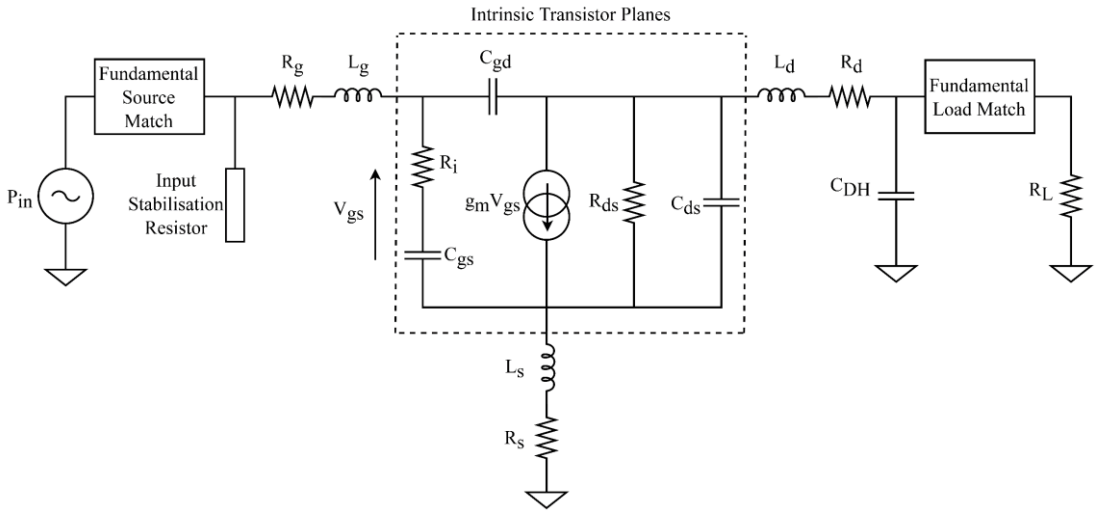


Fig. 6. 1: Equivalent large signal model and structure for class AB MMIC amplifier

6.2.2 Monolithic Microwave Integrated Circuits

A Monolithic microwave integrated circuit is a circuit where all active and passive microwave circuit elements are embedded in a semiconductor substrate with operating frequencies that may range from ~ 1 GHz to beyond 200 GHz. GaAs is the most widely used substrate material for MMIC design alongside its heterostructures like InGaAs and AlGaAs, with $f_T > 135$ GHz for a typical InGaAs PP10-15 MMIC process that will be used to design high efficiency class AB amplifier and high efficiency class E oscillator presented in Chapter 6 and 7 of this thesis. Other semiconductor materials like Si, InP, SiC, SoS (silicon on sapphire) and GaN are also used for fabrication of MMICs with each having their advantages that were discussed in Chapter 2. The prominence of MMICs is also attributed to the ability to process large number of circuits on a single MMIC wafer

concurrently. Layout of a typical MMIC discussed by Pozar (2012) in [44] has been shown in Fig. 6. 2, which has been reproduced from [44].

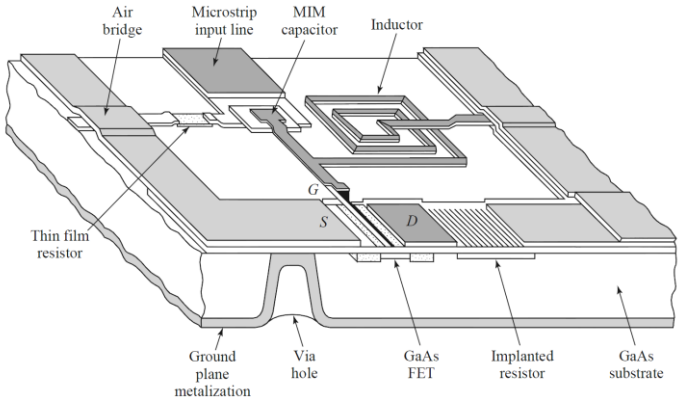


Fig. 6. 2: Layout of a typical MMIC showing various circuit elements processed on GaAs substrate

MMICs provide several advantages over MICs or discrete amplifier circuits which include [44]: 1) cheap fabrication cost of complex microwave circuits in larger quantities, 2) Low and controllable parasitics that may be modelled and utilised for circuit design, whereas parasitics due to bond pad, soldering and wires are larger and generally un-controllable, 3) high f_T and f_{max} of MMICs which are generally greater than 100 GHz compared to MIC which provide operation ~40 GHz, 4) Assembly of MMICs is generally easier compared to MICs, 5) MMICs are highly reliable compared to MICs, and 6) MMICs are smaller in size and weight compared to MICs which are generally large and heavy. A few disadvantages of MMICs over MICs include [44]: 1) MMICs have limited choice of circuit components supported by a particular foundry compared to MICs where various circuit elements from different vendors can be mounted, 2) MMICs have a greater turn around that can be up to 6 months, while MICs can be processed within a few days, and 3) initial investment and fabrication costs of MMICs are much higher than MICs.

6.2.3 MMIC Design Flow for Class AB Amplifier

This section will discuss design flow for class AB amplifier which utilises respective foundry process design kit (pdk) in Keysight's ADS for design, simulations, layout and DRC check.

Design Flow

Design process starts with the definition of target specifications and selection of appropriate amplifier topology and transistor for the desired amplifier mode. Transistor's size and gate periphery are analysed to achieve target performance as it directly defines the achievable gain, temperature, linearity, power dissipation, and the frequency of

operation for an amplifier mode and topology. For instance, 2×50 µm transistor provided the best trade-off between output power, PAE and large signal gain at optimum bias conditions and input power levels for class AB amplifier; while, 4×150 µm transistor provided optimum performance for class E oscillator discussed in the following chapter. Target specification of class AB amplifier have been presented in Table 6. 1 which were defined as per the requirements of the amplifier for implementation within on-chip cancerous stem-cells characterisation and neutralisation device.

Table 6. 1: Target specifications for class AB MMIC amplifier

Characteristics	**Symbol**	**Value**	**Unit**
Operating Frequency	f	30	GHz
Saturated Output Power	P_{sat}	> 17	dBm
Small Signal Gain	G_{ss}	> 7	dB
Large Signal Gain	G_{LS}	> 5	dB
Power Added Efficiency	PAE	> 50	%

DC IV transistor characteristics and corresponding amplifier load line analysis helps to identify optimum bias conditions, which is often based on on-wafer measured results from device pull-outs for improved accuracy. Estimation of transistor's output capacitance is also performed to predict higher order harmonic impedances at the drain. In the next step, load pull and source pull simulations (or measurements) to obtain optimum load and source impedances for high output power and PAE are performed. Measurement based load pull was reviewed in Chapter 3 for evaluation of GaN HEMT transistors on Triquint 0.25 µm GaN on SiC 3MI process which was conducted at the University of Manchester in 2013. However, due to un-availability of load pull measurement setup during the author's research; measurement based load pull couldn't be performed. Nevertheless, simulation based load pull included EM simulated extrinsic parasitics which were de-embedded to obtain optimum source and load impedances using foundry's pdk at transistor's intrinsic gate and drain. Typical schematics for de-embedding setup of gate and drain extrinsic parasitics has been shown in Fig. 6. 3, where the two de-embedding blocks contain EM simulated extrinsic $[S]$-parameters at respective ports. A similar setup was also utilised to estimate output capacitance, where simulated $[S]$-parameters of 2×50 µm pHEMT were used with de-embedded extrinsic parasitics. After identification of optimum source and load pull impedances, ideal

components are used to design the amplifier followed by conversion to microstrip elements and parametric optimisation using EM simulated elements from foundry pdk using Momentum microwave simulator. Finally, large signal simulations are performed to identify the amplifier's performance followed by optimisation under large input signal drive level. Once the amplifier has been optimised, layout and DRC check using pdk definitions is performed before the layout is submitted for further processing on tape-out wafer. DRC check of the design and layout is important to conform with foundry rules.

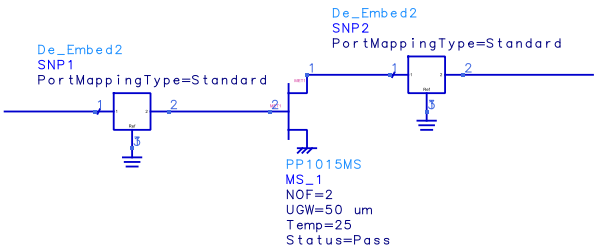


Fig. 6. 3: De-embedding gate and drain extrinsic parasitics

Fabrication Technology

WINPP10-15 fabrication technology from WIN Semiconductors Corp. Taiwan was used to develop class AB amplifier and class E oscillator MMICs. PP10-15 is a 100 nm gate length InGaAs pHEMT process with 4 mil substrate thickness; another variant of the process includes widely used PP10-10 process which has 2 mil substrate thickness. Various active and passive elements of the process and corresponding models are provided in the process design kit which can be installed in Keysight's ADS for design, simulation, layout and DRC check of various microwave circuits. The fabrication process having 12 steps for the formation of active and passive elements has been described in [148]. PHEMTs are available in both microstrip and coplanar waveguide in standard sizes ranging from 2×10 µm to 8×150 µm. MS pHEMT has been provided in common-source (CS) configuration, while CPW pHEMT could be configured in common-source, common-gate and common-drain configurations. Device models of active and passive elements in the pdk are optimised for linear and power amplifier design with the capability to predict performance at higher order harmonics and deep gain compression levels. Various layer stack of the process which is used for EM simulations in Momentum microwave has been shown in Fig. 6. 3 which shows two metal layers, i.e. MET1 (gate metal) and MET2 which are 1 µm and 2 µm, respectively. MET1 and MET2 layers provide current density of 4 mA/µm and 6 mA/µm, respectively and both can be used to process double metal layer transmission lines, which are especially useful for power

amplifiers where higher current handling capability is desired. The process supports Thin-Film Resistors (TFR) in addition to Mesa resistors (on the epitaxial layer); the former will be used in stabilisation network at gate of the amplifier discussed herein.

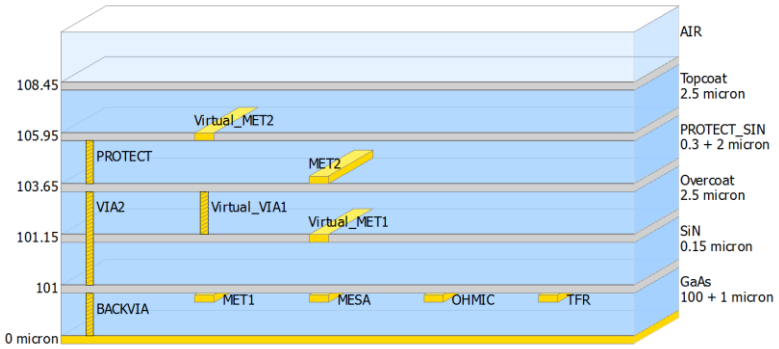


Fig. 6. 4: Layer stack of PP10-15 for EM simulation in Momentum microwave [150]

The process provides two capacitors, i.e. Metal-Insulator-Metal (MIM) and Capacitor-on-Via (COV). The later provides reduced parasitic inductance and will be used in shunt (C_{DH}) with the drain in class AB amplifier to provide short circuit conditions to harmonic components. MIM capacitor is formed between the conducting metal layer and 0.15 µm SiN dielectric layer, with a current density of 400 pF/mm^2 and 30 V rating. Interconnection between various layers could be provided through airbridges for cross-overs and vias. Back-via holes and backside metallization provide microstrip configuration and ground connection. Back-via hole provides ground connection to shunt stabilisation network at the gate of class AB amplifier. Spiral inductors are also available in the process, which will be used along-with MIM capacitor in the feedback network of class E oscillator presented in the following chapter. A range of inductances can be achieved by varying the number of turns and conductor spacing of both square and circular spiral inductors. Further discussion about the foundry process and applications has been provided in [149], [150]. An important difference between PP10-10 and PP10-15 process is the substrate thickness of 2 mil and 4 mil respectively, where the latter would have slightly bigger sized layouts.

6.3 DC and Small Signal Characteristics

Device and MMIC process models are important to predict and assist design engineers to achieve desired performance from MMICs post fabrication. Overview of WINPP10-15 process design kit was discussed in the preceding section, which is based on scalable non-linear EE HEMT device models. GaAs MMIC processes are much mature in this age, and literature review of various amplifiers developed using PP10-15 and its variant PP10-

10 process indicates decent behavioural prediction of the model for standard transistor sizes and bias conditions. This section presents discussion on the selection of appropriate transistor size from PP10-15 pdk, DC *IV* characteristics, output capacitance and stability analysis towards the design of class AB MMIC amplifier.

6.3.1 Selection of Transistor

Output power is a function of drain current, voltage and efficiency; which mainly depend on the gate size (number of fingers and width), breakdown voltage of the MMIC process and type of the transistor, respectively [28]. For a given MMIC process and transistor type; gate width and number of gate fingers are thus the main choice to obtain required output power. Transistors with larger gate width and number of fingers can support higher drain current to provide increased output power. An increase in gate width causes corresponding increase in device parasitics which reduces gain; while an increase in number of fingers increases gate to source capacitance (C_{gs}) which leads to quicker gain roll-off at higher frequencies due to lower input impedance. Another effect that can be observed in larger number of gate fingers is phase mismatch between drain currents flowing across different gate fingers, which causes transconductance and gain to reduce. Thus, trade-off between output power and gain is made while selecting an appropriate device size. Simulations of various transistors from WINPP10-15 pdk that include 2×50 µm, 4×50 µm, 2×75 µm and 2×100 µm pHEMTs for maximum available gain were performed at respective bias conditions for class AB operation. These are device sizes that can be used to develop class AB amplifier within the given MMIC cell dimensions; Fig. 6. 5 shows comparison between maximum available gains of the transistors.

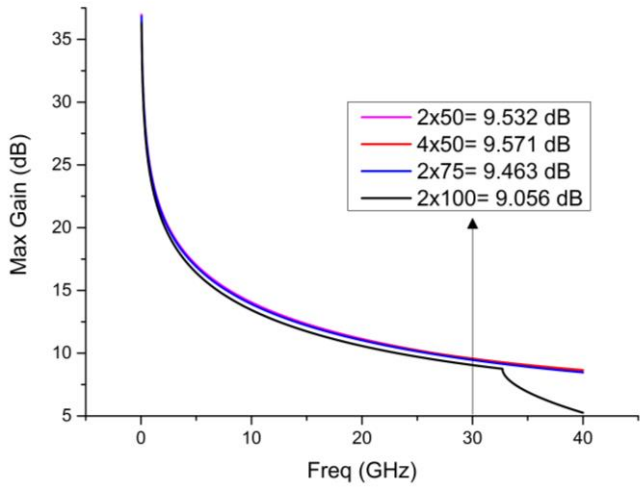


Fig. 6. 5: Comparison between maximum available gain for various pHEMT transistors from PP10-15 pdk under class AB bias conditions

The effect of transistor size on gain can be observed in Fig. 6. 5 where comparison between maximum available gain for various transistors has been presented. Maximum available gain at 30 GHz can be obtained through 4×50 µm pHEMT which is only marginally greater than 2×50 µm transistor. Different versions of class AB amplifier were designed using these two transistors, however, large signal simulations with EM simulated networks showed lower PAE for the amplifier with 4 gate fingers with similar output power, which can be attributed to increased channel temperature. Thus, class AB amplifier with 2×50 µm pHEMT was selected as the optimum version.

6.3.2 DC IV Characteristics

The design process starts with analysis of DC IV characteristics of the transistor followed by selection of appropriate bias conditions. It was discussed earlier that current conduction angles for class AB amplifiers lie between 180° and 360° which is between corresponding conduction angles of class B and class A amplifiers, respectively. Current conduction angle is mainly achieved through appropriate bias conditions and it is very often that trade-off between linearity, gain, output power and PAE is made, especially in class AB amplifiers where the range of current conduction angles is greater than other classes of amplifiers. To identify optimum bias point and loadline for class AB amplifier, DC IV simulations were performed. Fig. 6. 6 shows simulated DC IV characteristics of 2×50 µm CS pHEMT transistor, where V_{gs} has been swept from -1.0 V to 0 V with steps of 0.1 V; and V_{ds} has been swept from 0 V to 5 V with steps of 0.5 V. The figure shows optimum bias points for class A, class B and class AB operation.

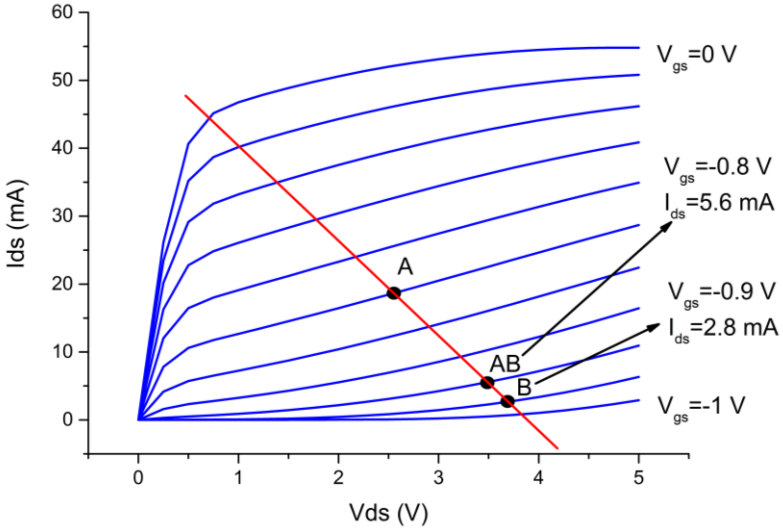


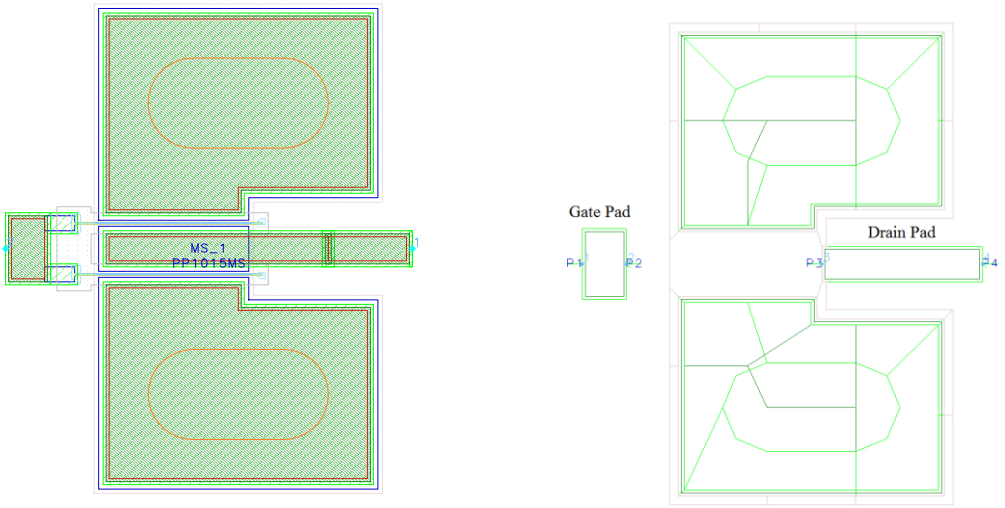
Fig. 6. 6: DC IV curves of 2×50 µm CS pHEMT showing optimum bias point for class AB operation

The chosen value of $I_{ds} = 0.14I_{dss}$ places the corresponding bias point in lower mid class AB bias conditions, where saturated operation of the amplifier would prospectively cause swing across the knee region to generate non-linearities and harmonic products across the transistor's output capacitance C_{ds}. It also needs to be considered that the input drive level in class AB amplifiers is required to maintain I_s (or I_{dss}); thus, closer the bias point is to class B conditions, higher would be the required input power level to achieve the same efficiency, which would reduce large signal gain. The advantage we would achieve from the selected bias point is reduced current conduction and DC power consumption. For instance, at the selected bias point the transistor will ideally consume ~ 20 mW DC power, compared to ~ 32 mW at the mid-point between class A and B bias points.

6.3.3 Estimation of Output Capacitance

Significance of output capacitance was discussed in literature review, Chapter 4 and earlier in this chapter as it is mainly attributed to non-linear behaviour and the generation of harmonic products under large signal gain. A large value of output capacitance would provide short circuit conditions to second and higher order harmonics, however, a small value would present reactive conditions. Placing a shunt capacitance C_{DH} (Fig. 6. 1) defined according to the value of C_{ds} across the drain terminal would provide necessary short circuit conditions to second harmonic and higher order harmonics.

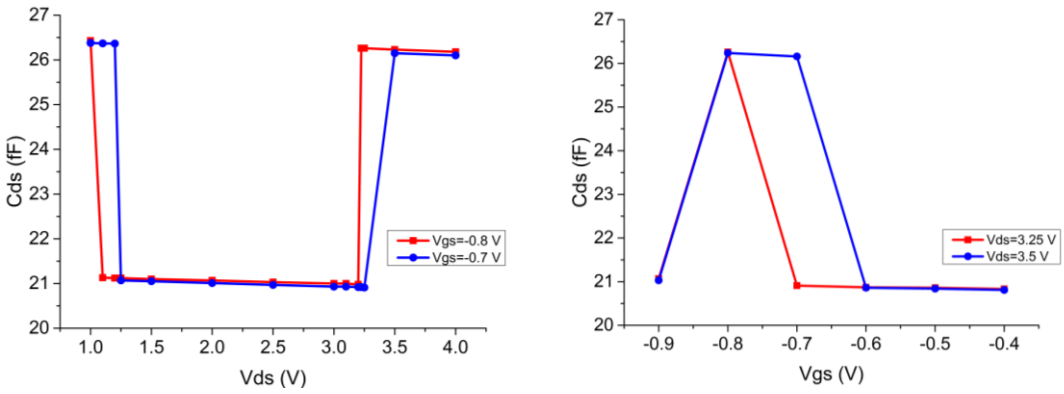
Eq. 4.7-4.11 presented in Chapter 4 can be used to calculate intrinsic elements (shown in Fig. 6. 1) including C_{ds}. However, extrinsic elements $R_g, L_g,$ and R_d, L_d that can be described in terms of gate and drain pad transmission lines, respectively need to be de-embedded to obtain intrinsic elements at device's intrinsic planes. These transmission lines were simulated using Momentum microwave for 2×50 µm CS pHEMT, followed by de-embedding (shown in Fig. 6. 3) which removed the effects of gate and drain extrinsic elements. Fig. 6. 7 shows (a) 2×50 µm CS pHEMT layout, and (b) required gate and drain transmission lines to be de-embedded, respectively.



(a) (b)

Fig. 6. 7: Layout of (a) 2 × 50 µm CS pHEMT layout, and (b) gate and drain pad transmission lines to be de-embedded in ADS from WINPP10-15 pdk

Fig. 6. 8 shows the values of output capacitance C_{ds} for 2 × 50 µm CS pHEMT with variation in (a) V_{ds} from 1 V to 4.0 V for $V_{gs} = -0.8$ V and (b) V_{gs} from -0.9 V to -0.4 V for $V_{ds} = 3.5$ V. It can be observed that $C_{ds} = 26.25$ fF at 30 GHz for the transistor at optimum bias conditions chosen earlier; which provides a reactance $X_c \approx 100\ \Omega$ at the second harmonic. C_{ds} alone cannot satisfy the conditions for class AB operation; thus, shunt capacitance $C_{DH} = 1.25$ pF will be added to the drain terminal to provide $X_c \approx 2.07\ \Omega$ reactance at the second harmonic.



(a) (b)

Fig. 6. 8: Variation of output capacitance (C_{ds}) of 2 × 50 µm CS pHEMT from PP10-15 pdk for (a) variation in V_{ds} and (b) variation in V_{gs}

6.3.4 Stability Analysis

Stability analysis of a transistor helps to identify possible oscillatory behaviour and needs to be performed for all frequencies of operation including operating band and out of band

low frequencies where high gain could potentially suppress oscillations. Various stability analysis techniques including Rollet stability factor (k) were discussed in Section 4.2.3, which remain applicable to class AB MMIC amplifier presented herein. However, those techniques are valid under small signal, whereas stability under large signal is widely considered an intrinsic non-linear issue [64]. Nevertheless, stability of an amplifier could be improved through series/shunt resistance and RC network across the gate terminal and assumed to hold under large signal as well. Fig. 6. 9 show stability factor and load and source stability circles, respectively for 2×50 µm pHEMT under class AB bias conditions, where poor stability at out of band low frequencies can be observed.

Fig. 6. 9: Stability factor for 2×50 µm CS pHEMT under class AB bias conditions

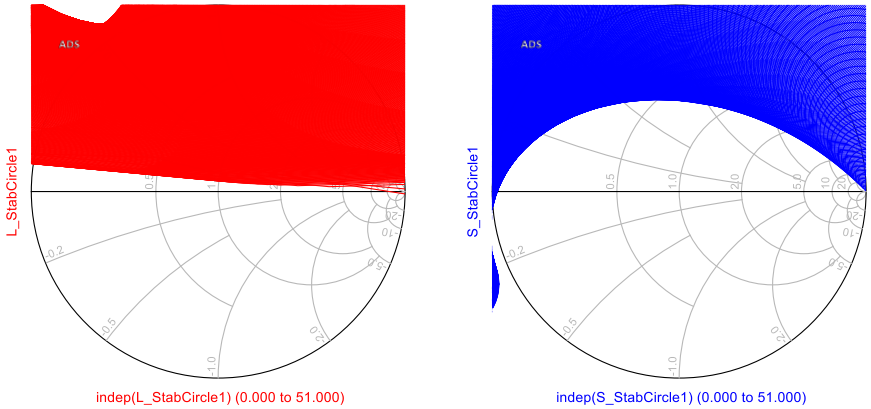


Fig. 6. 10: Load and source stability circles for 2×50 µm CS pHEMT under class AB bias condition

Load and source stability circles shown in Fig. 6. 10 represent input and output reflection coefficient on respective smith charts. Unstable behaviour towards prospective source and load impedances for class AB amplifier could be observed. However, 80 Ω shunt resistance with gate terminal of the device shown in Fig. 6. 11 has been utilised to achieve unconditional stability across the entire frequency band. Stability factor and load and

source stability circles after the addition of shunt resistance have been shown in Fig. 6. 12 and Fig. 6. 13, respectively.

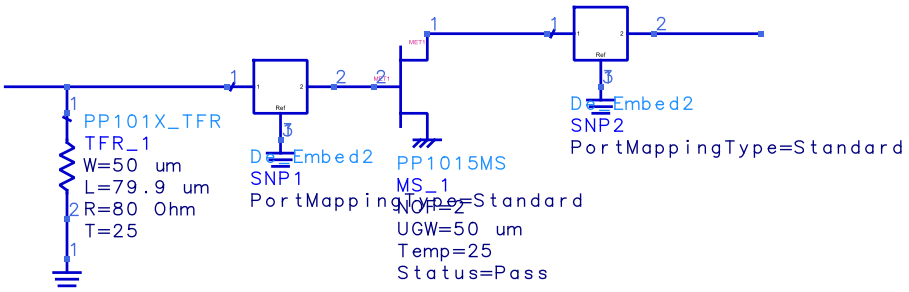


Fig. 6. 11: Addition of 80 Ω shunt stabilisation resistor to improve stability

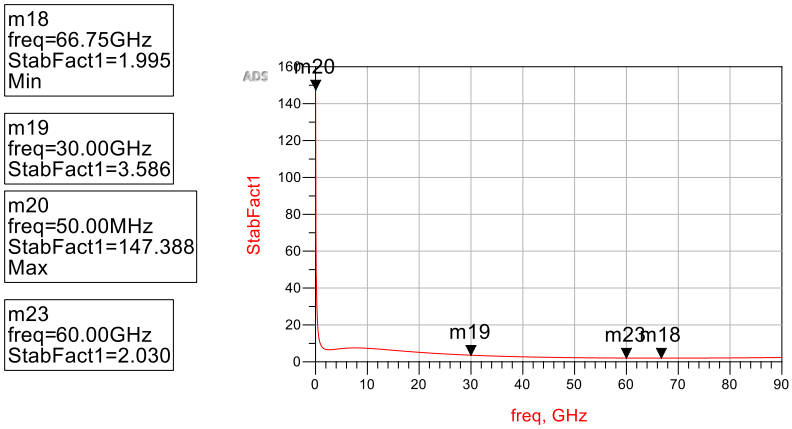


Fig. 6. 12: Stability factor after addition the addition of 80 Ω shunt stabilisation resistor

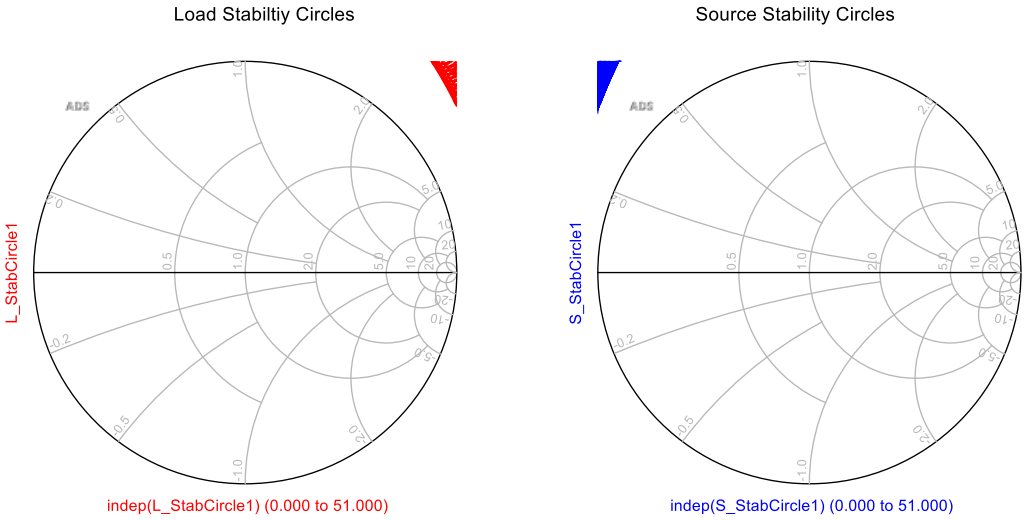


Fig. 6. 13: Load and source stability circles after the addition of 80 Ω shunt stabilisation resistor for 2 × 50 µm CS pHEMT under class AB bias condition

Shunt resistance essentially increases real part of the transistor's input impedance to improve stability, especially at lower frequencies. Slight flatness in gain can also be observed, especially ~7 GHz; Fig. 6. 14 shows comparison between maximum available

gain and S_{21}. However, to prevent from device gain from being overkilled, the shunt stabilisation resistance was optimised to 200 Ω.

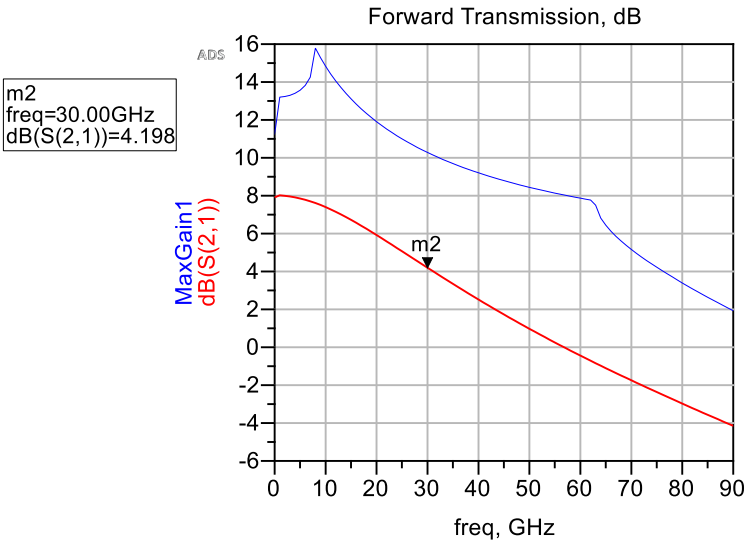


Fig. 6. 14: Comparison between S_{21} and maximum available gain after the addition of 80 Ω shunt stabilisation resistor for 2 × 50 µm CS pHEMT under class AB bias condition

Stability was further analysed after providing required second and higher order harmonic short circuit conditions through shunt C_{DH} capacitance, corresponding stability factor has been shown in Fig. 6. 15. Analysis of stabilisation resistor at the gate and higher order short circuit behaviour at the drain was important before load-pull analysis as transistor's behaviour would change under these conditions.

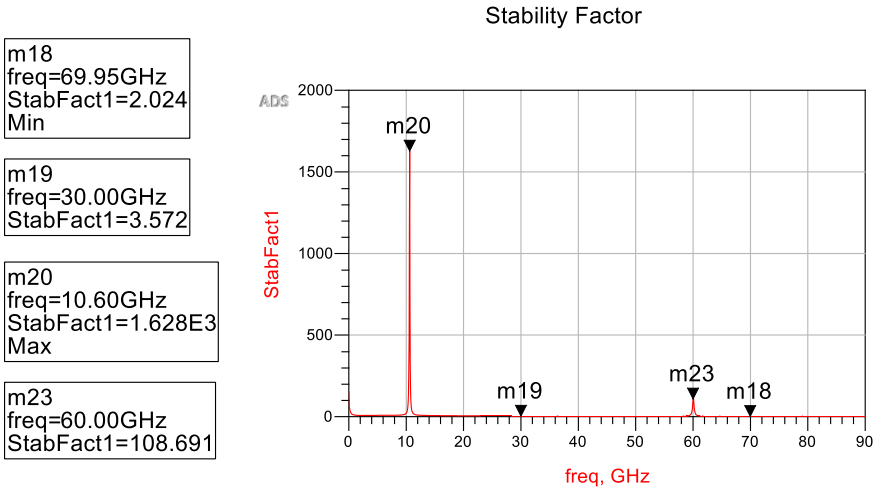


Fig. 6. 15: Stability factor after addition the addition of 200 Ω shunt stabilisation resistor with the gate and 1.25 pF shunt capacitance C_{DH} with the drain

6.4 Load Pull Analysis

The significance of load pull analysis to identify optimum impedances at transistor's gate and drain terminal for desired output power and PAE was emphasised earlier in this

thesis. Load pull simulations were performed using respective TFR stabilisation resistance, COV capacitance (C_{DH}) and 2×50 µm CS pHEMT models from PP10-15 pdk in ADS to achieve over 17 dBm output power with maximum efficiency. Since GaAs technology cannot provide high breakdown voltage compared to GaN technology; thus, maximum voltage swing was required to be kept lower than break-down voltage under class AB bias conditions. The design manual for PP10X process suggests an average breakdown voltage $V_{BR} \approx 9$ V [148].

Initial iterations of load pull simulations were performed with conjugately matched source network to deliver maximum power to the gate; nevertheless, it was later fine-tuned during source pull simulations. The input power level was varied to achieve ~6 dB large signal gain, which would correspond to $P_{in} = 11$ dBm to achieve 17 dBm output power. Fig. 6. 16 shows output power (blue) and PAE (red) contours, where the inner most circles represent maximum values. Ideally, impedance should be selected close to the intersection between the two circles; however, PAE was prioritized over output power. Load pull simulations provide an optimum load impedance $Z_L = 36.58 + \text{j}45.171\ \Omega$ and source impedance $Z_S = 8 + \text{j}6.2\ \Omega$ corresponding to 72.4 % PAE and 17.25 dBm output power with 11 dBm input power at 30 GHz under class AB bias conditions. Load pull simulation results have been shown in Fig. 6. 17. Large reactive part of fundamental load impedance can be observed, the effect of this will be discussed later in large signal analysis.

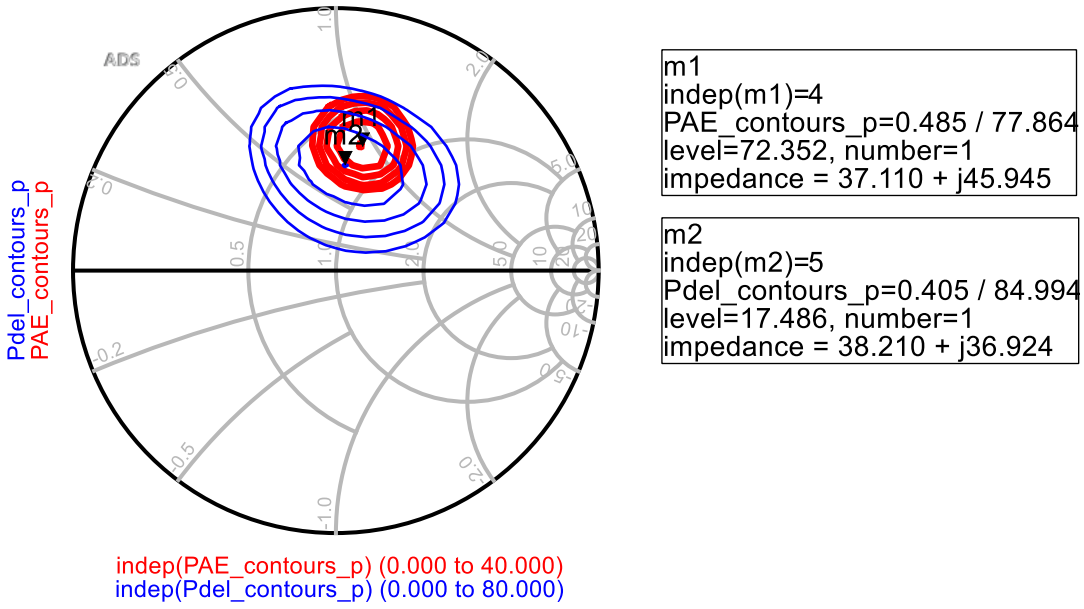


Fig. 6. 16: Output power and PAE contours on the Smith chart for class AB amplifier; markers m1 and m2 show maximum PAE and output power circles, respectively

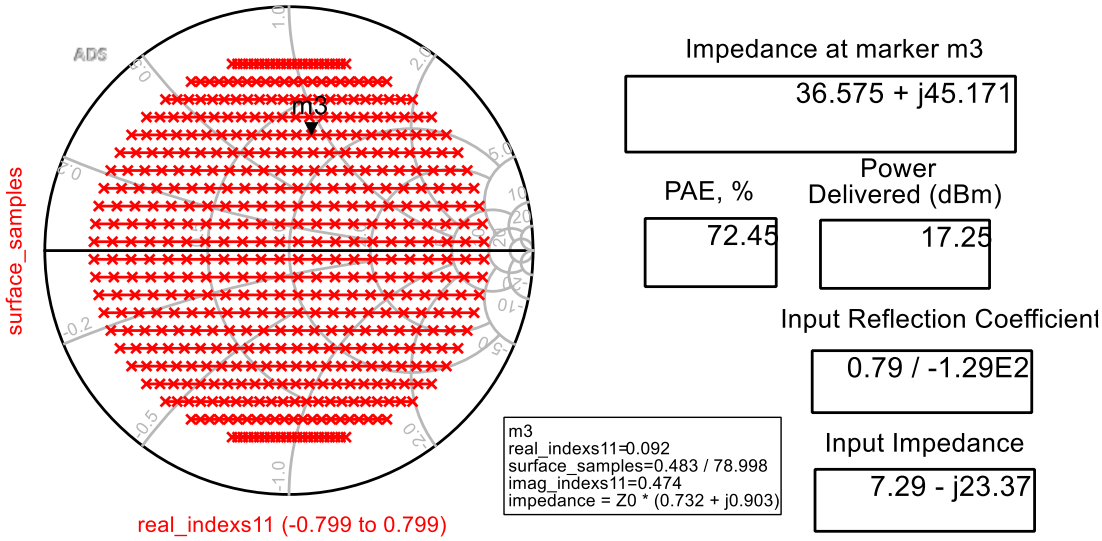


Fig. 6. 17: Load pull simulation results for 2 × 50 µm CS pHEMT under $V_{gs} = -0.8$ V, $V_{ds} = 3.5$ V and $P_{in} = 11$ dBm; marker m3 shows the optimum load impedance

6.5 Design of Source and Load Termination Networks

Load pull simulation were discussed in the preceding section where optimum source and load impedances for class AB operation were identified. These will be utilised to design corresponding source and load termination networks.

6.5.1 Source Termination Network

Fig. 6. 18 shows schematics for input network of class AB amplifier.

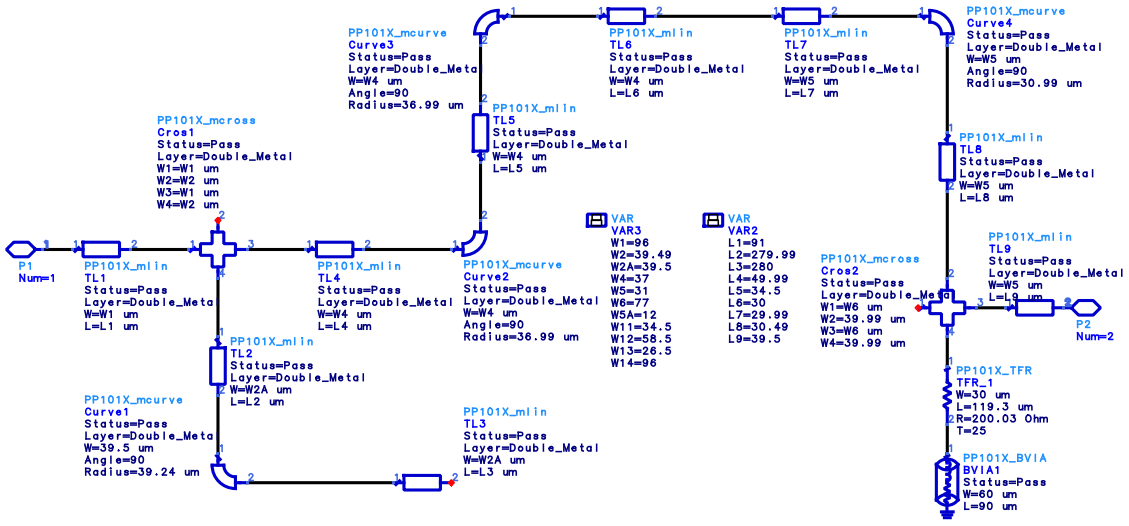


Fig. 6. 18: Input matching network of class AB MMIC amplifier

Low impedance double metal layer transmission lines have been used in the input network of class AB amplifier and meandering has been performed in the layout to optimise the circuit with respect to the cell dimensions. Gate pad that was earlier de-embedded was replaced by transmission line 'L9' shown in Fig. 6. 18. EM simulations

were performed followed by parametric optimisation to achieve desired source impedance at the gate and 50 Ω match to the input port. Fig. 6. 19 shows EM simulated results of the input matching network in terms of required source impedance at the gate in terms of output reflection coefficient S_{22}. Layout of the input matching network in ADS has been shown in Fig. 6. 20.

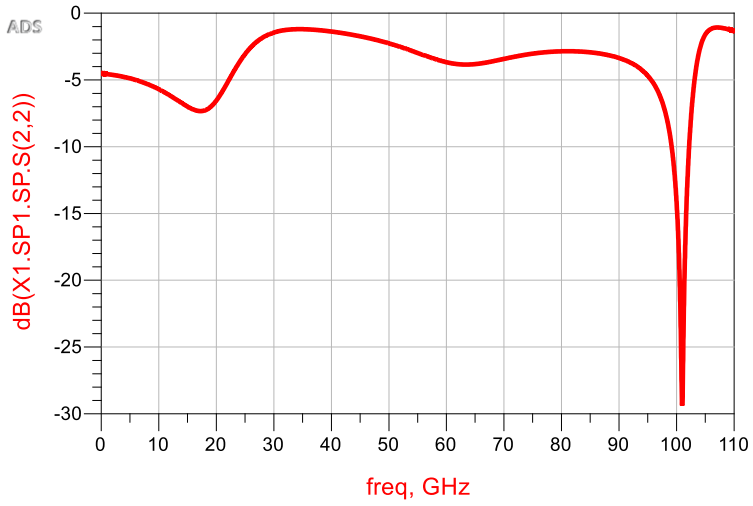


Fig. 6. 19: EM simulated results of the input matching network

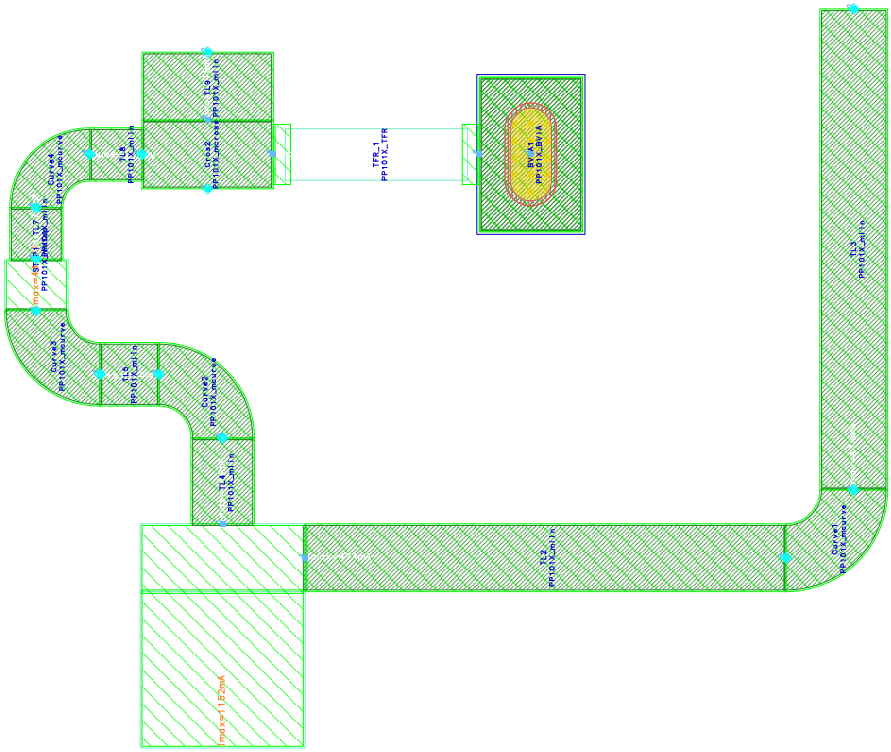


Fig. 6. 20: Layout of input matching of class AB amplifier in Momentum ADS, the top side corresponds to gate connection, while the bottom side corresponds to input GSG port

6.5.2 Load Termination Network

The output matching network of class AB amplifier (shown in Fig. 6. 21) has been designed using double metal layer stepped transmission lines with meandering to obtain the required impedance at the drain terminal and 50 Ω match to the output port. EM simulations of the output matching network were performed in Momentum microwave followed by parametric EM optimisation. Second harmonic short circuit impedance was provided at the drain terminal through shunt 1.25 pF capacitance. Corresponding layout in ADS has been shown in Fig. 6. 22. Final schematics of the amplifier have been attached in Annex C, while the MMIC cell layout in ADS measuring 1510 × 1330 µm has been shown in Fig. 6. 23.

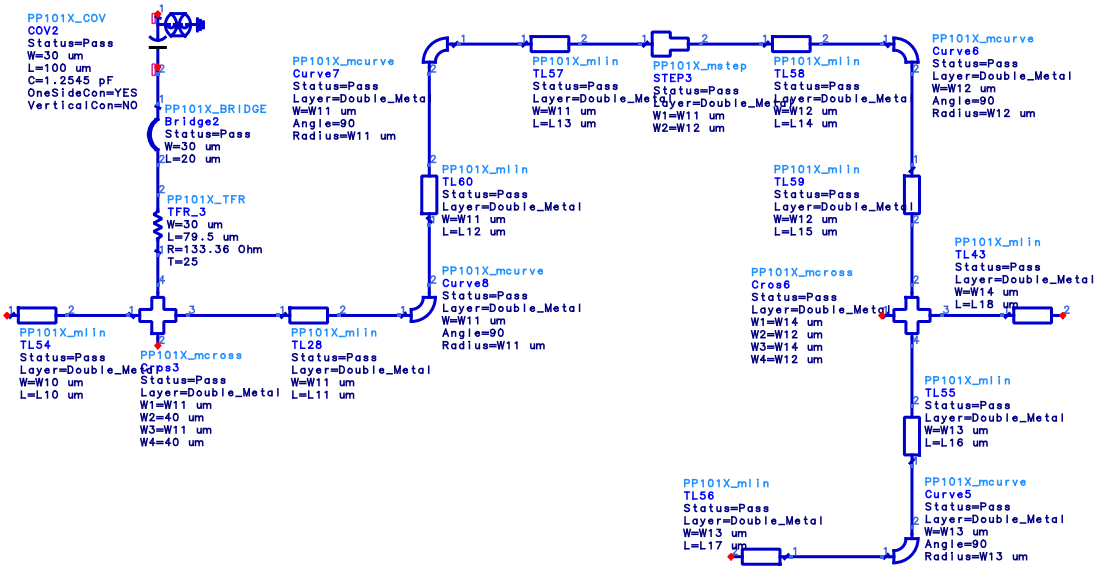


Fig. 6. 21: Output matching network of class AB MMIC amplifier

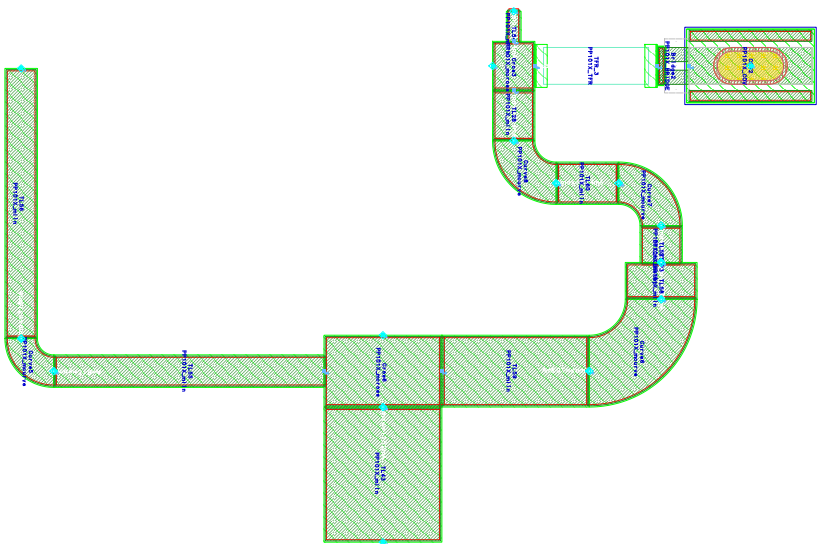


Fig. 6. 22: Layout of output matching of class AB amplifier in Momentum ADS, the top side corresponds to drain connection, while the bottom side corresponds to output port

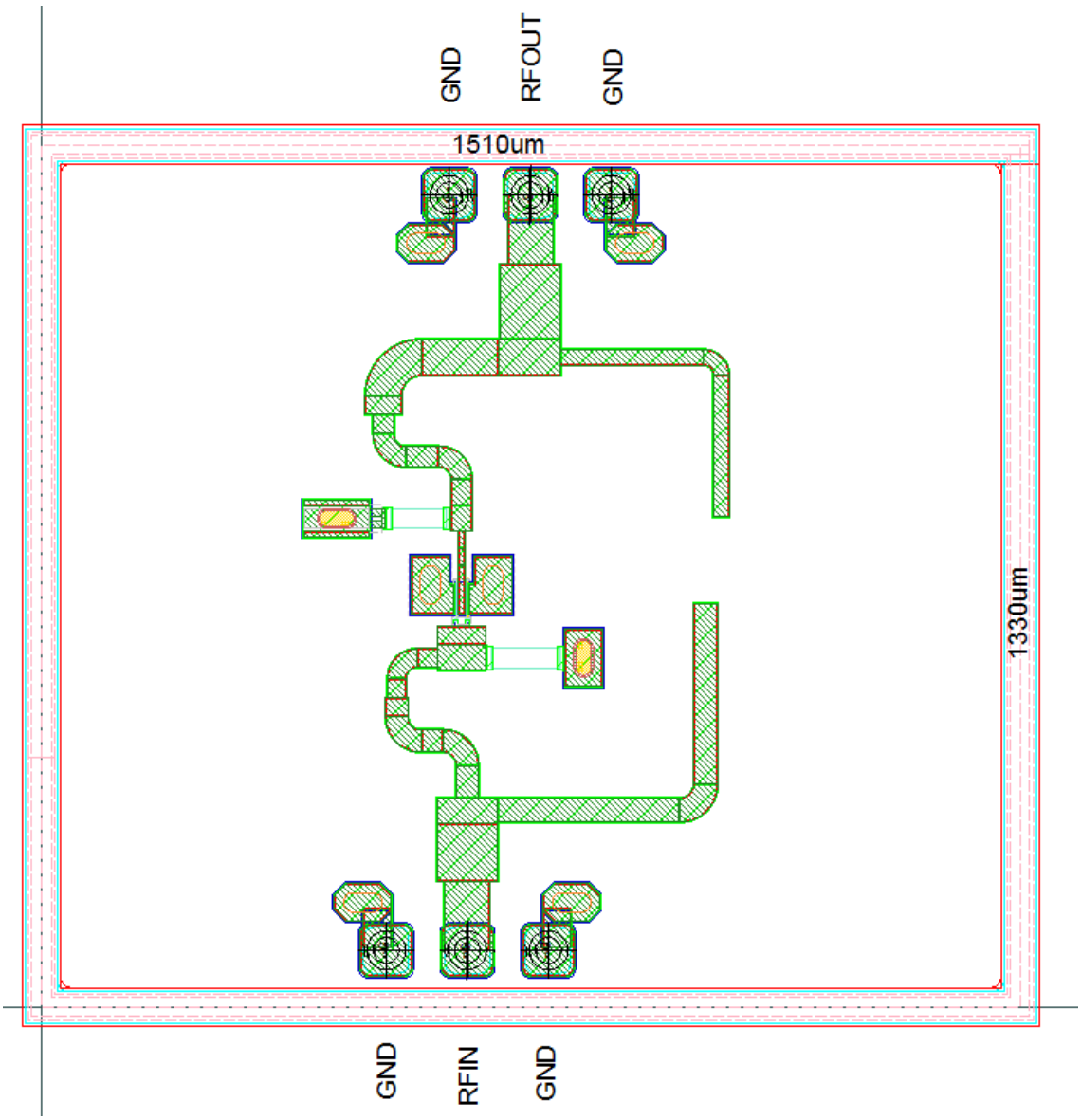


Fig. 6. 23: Layout of class AB amplifier in Momentum ADS

6.6 Results and Analysis

6.6.1 Introduction

Design flow of class AB amplifier included various steps discussed in the preceding sections. Hierarchical design involved separate design and optimisation of various sub-networks in the circuit and bringing them together to achieve the required performance. The sub-networks were optimised using parametric optimisation based on EM models of various passive elements and networks that were generated through EM simulations (down to DC) using Momentum microwave simulator; which is a leading 3D planar EM simulator for passive circuit simulation, modelling and analysis. It utilises numerical techniques like frequency dependent Method of Moments (MoM) to solve Maxwell's equations in arbitrary multi-layered and planar structures [151]. EM simulations are important to identify parasitic and cross-talk effects between transmission lines (or metal conductor layers) in the layout, including analysis at discontinuities between stepped or meandered transmission lines. For instance, discontinuities and meandering can cause phase mismatch and impedance variations, which were optimised using parametric EM model based optimisation. Maximum current handling limits of transmission lines were also considered during optimisation. Design guidelines and conformity to foundry rules were checked before final layout was performed manually from the hierarchical optimised version of the amplifier. DRC check was performed before the cell layout was submitted for further processing on the tape-out wafer.

This section presents results and analysis of class AB amplifier with EM simulated passive elements and networks based on the models provided in WIN PP10-15 pdk. Various results presented in this section include small signal [S]-parameter simulation and initial on-wafer measurements; and large signal simulation results with discussion on output power, PAE and large signal gain as a function of the input power at various gain compression levels. Time domain drain curves are presented towards the end with analysis on 1 dB compression and overdriven conditions.

6.6.2 Small signal Analysis

Stability analysis of class AB amplifier was presented in Section 6.3.4 earlier which showed unconditional stability across the entire frequency band. Small signal [S]-parameters are important to identify gain, input and output port match and reverse isolation; however, large signal analysis is important for characterisation of power amplifiers. Comparison between simulated and on-wafer measured [S]-parameters from 100 MHz to 67 GHz at $V_{gs} = -0.8$ V and $V_{ds} = 3.5$ V showing S_{21} and S_{11} has been

shown in Fig. 6. 24. Comparison between simulated and on-wafer measured input and output reflection coefficients of the amplifier showing match to 50 Ω input and output ports have been shown in Fig. 6. 25 (a) and (b), respectively.

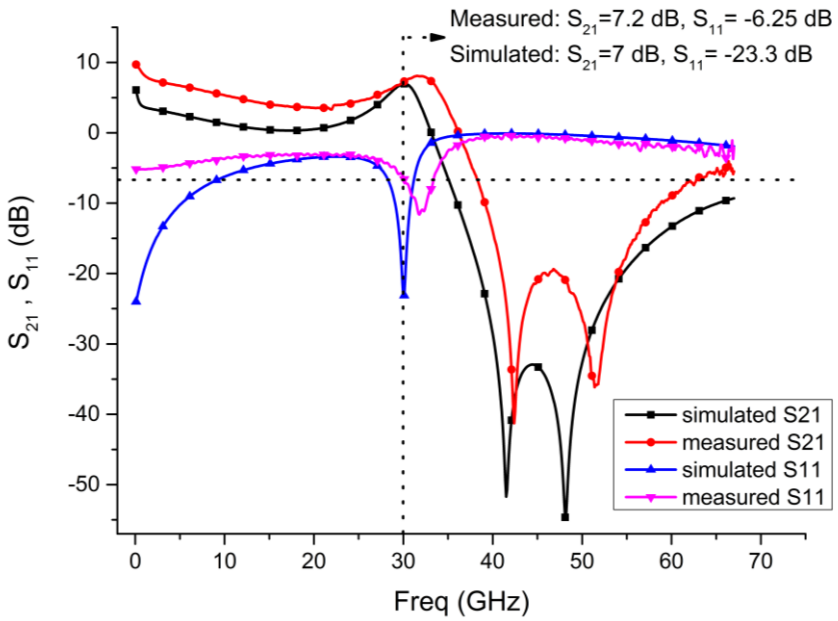
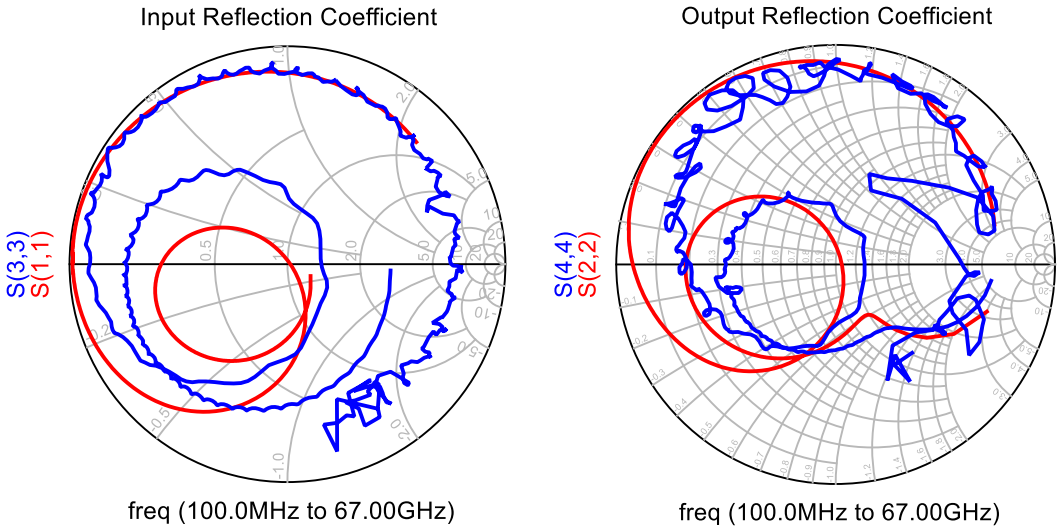


Fig. 6. 24: Comparison between simulated and measured [S]-parameters of class AB MMIC amplifier from 100 MHz to 67 GHz at $V_{gs} = -0.8$ V and $V_{ds} = 3.5$ V



(a) (b)

Fig. 6. 25: Simulated input and output reflection coefficients of class AB amplifier (blue and red curves represent measured and simulated results, respectively)

Comparison between results shown in Fig. 6. 24 and Fig. 6. 25 indicate comparatively poor match with the input and output ports in measurement results with around 2 GHz difference in gain roll-off due to inaccuracies in input capacitance C_{GH} provided in the

PDK. Screenshot of [S]-parameter from network analyser has been shown in Fig. 6. 26, where decent reverse isolation can be observed from top right curve.

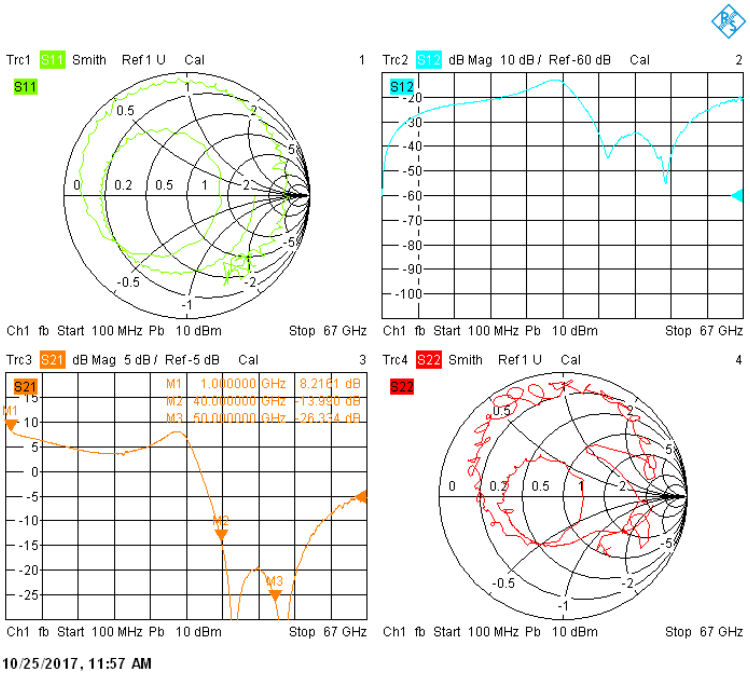


Fig. 6. 26: Screenshot of on-wafer [S]-parameter measurement results from network analyser for class AB amplifier

6.6.3 Large Signal Analysis

Large signal simulation results with EM simulated passive elements and networks under class AB bias conditions, i.e. $V_{gs} = -0.8$ V and $V_{ds} = 3.5$ V will be presented in this section. Fig. 6. 27 shows simulated large signal behaviour in terms of output power, gain and PAE as a function of the input power.

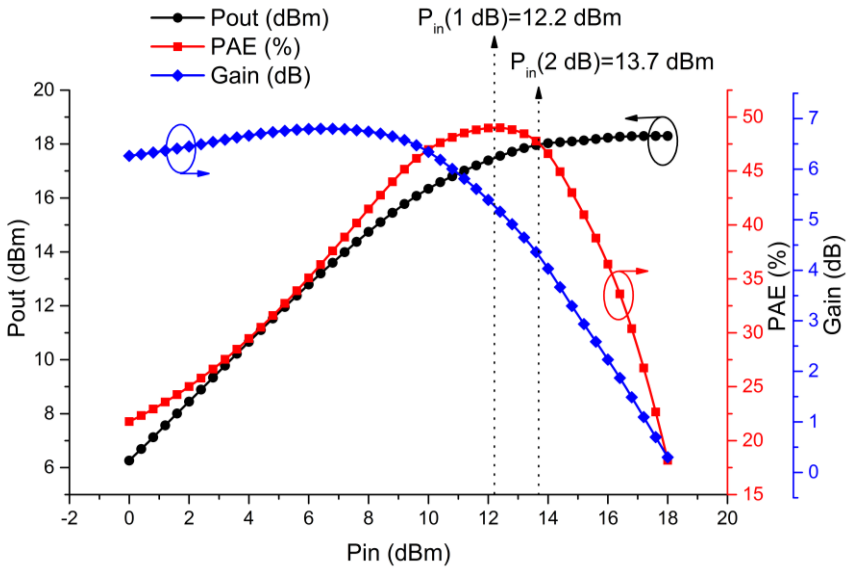
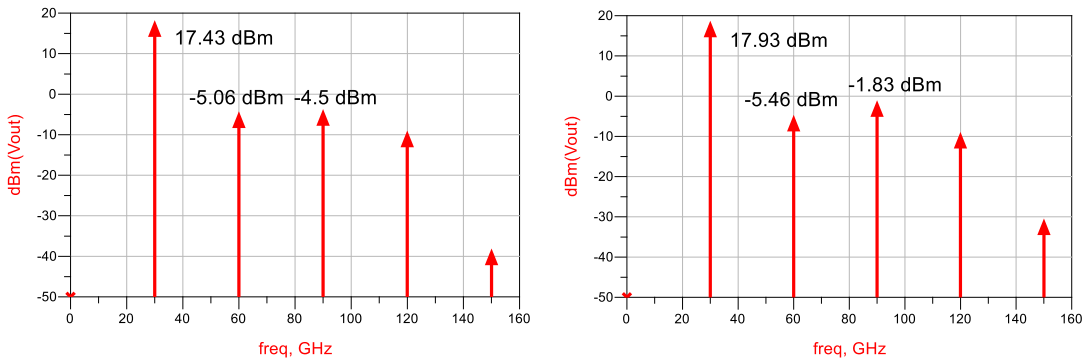


Fig. 6. 27: Large signal simulation results of class AB MMIC amplifier showing output power, gain and PAE as a function of the input power



(a) (b)

Fig. 6. 28: Simulated output power spectrum of class AB MMIC amplifier at (a) 1 dB and (b) 2 dB gain compression, at $P_{in} = 12.2$ dBm and $P_{in} = 13.7$ dBm, respectively

Fig. 6. 28 shows simulated output power spectrum of class AB amplifier under (a) 1 dB and (b) 2 dB gain compression levels, respectively. At these input drive levels, 17.45 dBm and 17.98 dBm output power can be achieved with 49 % and 47.6 % PAE respectively. Higher order harmonic suppression can be observed from the spectrums, however, an increase in the third harmonic component can be observed at 2 dB gain compression which can be attributed to the generation of odd order current harmonics and corresponding voltage harmonics when the input waveform swings across the knee region. This effect can be observed through comparison of drain voltage and current waveforms for the two gain compression levels (1 dB and 2 dB) shown in Fig. 6. 29. The waveform also depicts reduced current conduction angle which is still greater than class B (half rectified current waveform).

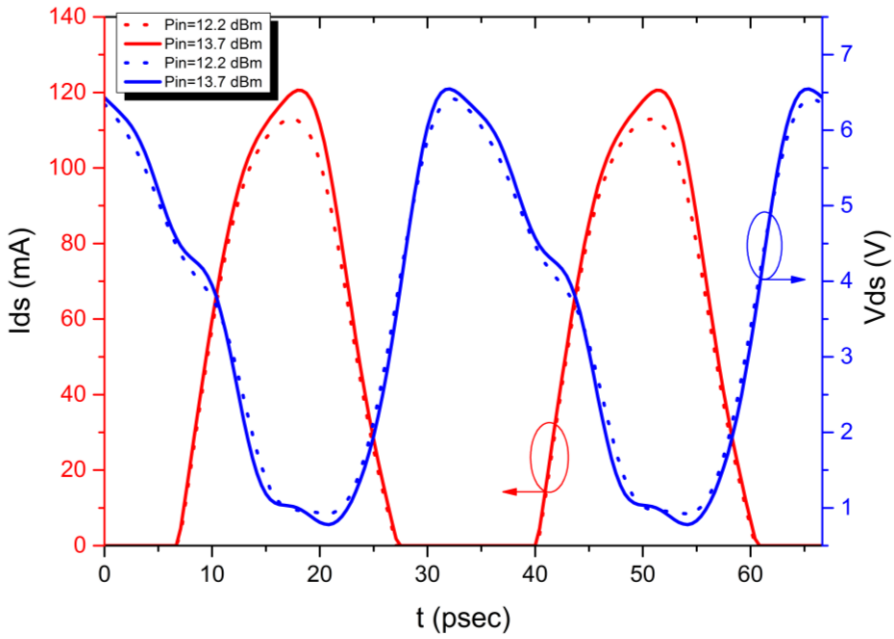
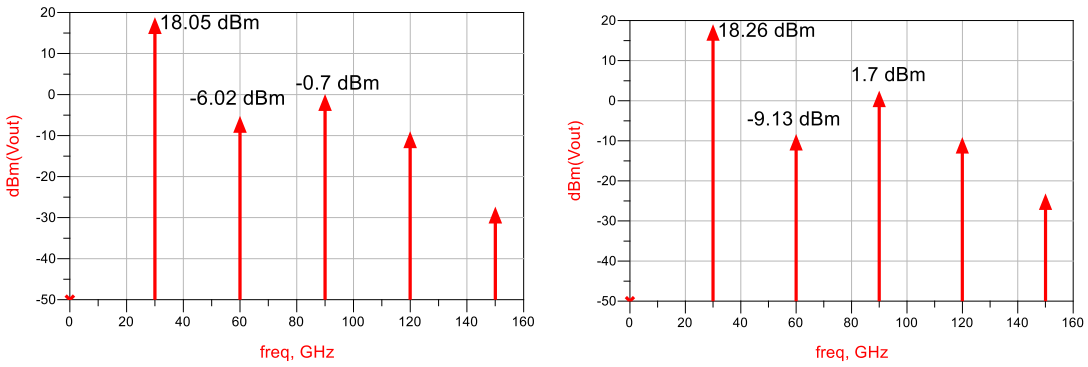


Fig. 6. 29: Simulated drain *IV* curves of class AB MMIC amplifier at 1 dB gain compression and 2 dB gain compression

Altered current and voltage waveforms can be observed due to large reactive component in the fundamental matching network. Peak voltage at the drain remains below the breakdown voltage ($V_{BR} \approx 9$ V), even at 6 dB gain compression levels. However, voltage and current waveforms are much altered with significant third order voltage component, while the second harmonic remains short circuit due to shunt capacitance C_{DH}. Output power spectrum at 3 dB and 6 dB gain compression levels have been shown in Fig. 6. 30, while corresponding drain IV curves have been shown in Fig. 6. 31.



(a) (b)

Fig. 6. 30: Simulated output power spectrum of class AB MMIC amplifier at (a) 3 dB and (b) 6 dB gain compression

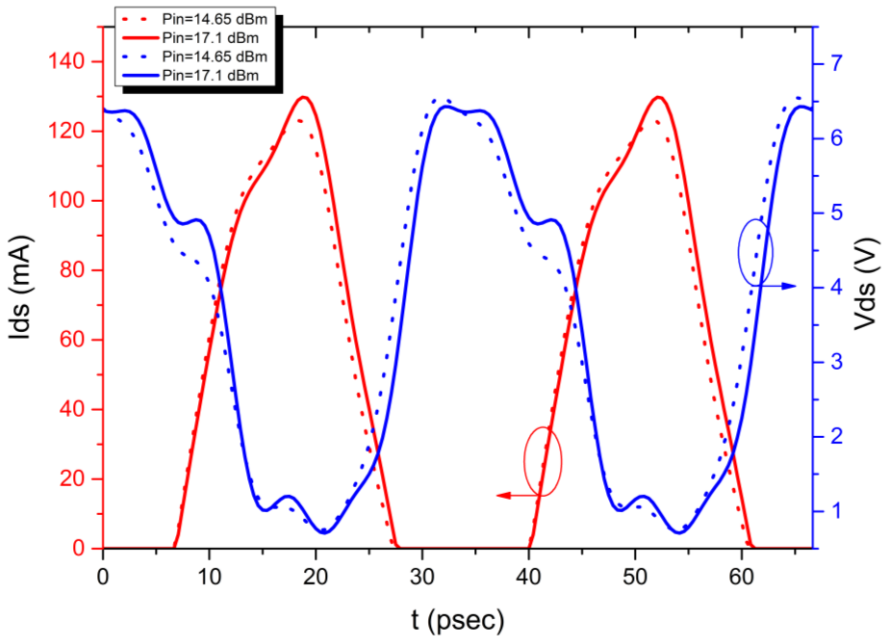


Fig. 6. 31: Drain IV curves of class AB MMIC amplifier at 3 dB gain compression and 6 dB gain compression

Presence of higher order voltage harmonics in output spectrum and IV drain waveforms, and larger fundamental voltage component at higher gain compression levels essentially occurs because of reactive voltage components that are generated due to flow of

harmonics into non-linear output capacitance C_{ds}. The operation at such high input drive levels is like class J amplifiers and one would expect the efficiency to increase, which instead decreases as shown in Fig. 6. 27. Classical definition of class J amplifiers [41] needs to be revisited here, which suggests resistive fundamental load impedance and reactive second harmonic impedance. However, class AB MMIC amplifier presented herein has high reactive fundamental load impedance that causes phase mismatch between current and voltage waveforms. Thus, the efficiency decreases which is also affected by high heat dissipation. It can be inferred from preceding discussion on large signal results that optimum operating conditions for class AB MMIC amplifier would be under 1 dB gain compression where 17.43 dBm output power with 49 % PAE.

6.7 Conclusion

This chapter presented design and analysis of class AB amplifier on PP10-15 GaAs MMIC process from WIN Semiconductors Corp. The amplifier was designed in Keysight's ADS using design guidelines handbook and non-linear device models from the pdk; however, accuracy of the models was questioned due to the difference between simulated and on-wafer measured small signal [S]-parameters. Initial on-wafer [S]-parameter measurements showed comparable small signal gain and similar trend with much noise, however, much difference was observed in input and output port matching which suggest a drift in calibration and question pdk data from WIN semiconductors foundry. The amplifier demonstrated reasonable performance through various simulations conducted with EM simulated models which were much similar to target specification. Analysis and discussion on large signal results including the relationship between output power, gain and PAE in terms of the input power, time domain IV drain curves and output spectrum showed some important effects which can help to identify optimum operating conditions. 1 dB gain compression was the optimum point to operate the amplifier where the amplifier showed 49 % simulated PAE with 17.43 dBm output power. Large signal on-wafer measurements couldn't be performed due to limitations of measurement equipment at the measurement facilities available to the author, thus, the die is proposed to be packaged and mounted on a custom designed application board for further testing and large signal measurements.

Chapter 7

High Efficiency Class E Oscillator

7.1 Introduction

RF and microwave energy at various frequency bands has been utilised to demonstrate medical effects on human subjects that include ablation or coagulation by integrating microwave power sources with suitably designed antenna and applicator structures to produce highly focused and controlled heating on tissue structures [6], [119], [152]. For instance, microwave energy can be delivered to tissues or lesions located within the human body through an endoscopy channel measuring 2.8 mm or 3.2 mm in diameter. However, transmission line losses and distributed tissue heating across the channel are issues that need to be resolved by developing microwave power sources that are small enough to go down through an endoscopy channel to generate localised microwave power at the tissue site. DC to RF efficiency of such microwave sources can be improved to reduce heat dissipation at the treatment site. Various X-band and Ku-band medical applications reported in [6] include the treatment of benign and cancerous lesions, reshaping the cornea, male sterilisation and menorrhagia.

Oscillators are important elements of a microwave system that find applications in communications, radars, instrumentation and RF and microwave surgical and therapeutic devices. Solid state oscillators are essentially non-linear active circuits that convert DC to steady state RF sinusoidal signal by utilising an active non-linear transistor or diodes alongside passive circuit networks or elements. Ideally, the oscillators generate pure RF or microwave sinusoidal signal with fixed frequency, phase and amplitude, however, practical implementation of oscillators generally involves frequency and output power variance with time [44]. Early development of oscillator circuits as performed using Gunn and IMPATT diodes; however, the developments in GaAs FETs in the 1970s opened up new dimensions for microwave transistor oscillators at frequencies in the millimeter wave range. Gunn and IMPATT diode oscillators showed decent performance in terms of higher frequency and output power; however, transistor oscillators provide several advantages that include: higher compatibility with other elements in the microwave system, suitability for monolithic microwave circuit integration, low phase noise, independence from threshold current requirements and higher power efficiency performance; making the latter a popular choice for microwave systems [44], [153]. Robertson (2001) in [29] discusses the suitability and low noise performance of HBT and

HEMT based microwave oscillators using MMIC technology. However, a popular design choice is quasi MMIC circuits that simplify the fabrication process and improves reliability and noise performance by having a negative resistance (or reflection) amplifier on a single chip along-with corresponding bias and decoupling circuit elements, and off chip high quality factor (Q) resonators [29], [64].

A large amount of energy is dissipated as heat during DC to RF conversion and the reported efficiency of oscillator circuits is fairly low [89]. Switching mode oscillators have been discussed in the literature to improve efficiency of oscillator circuits which include class E of class F amplifier topology and a feedback network that provides the required phase shift and conditions of oscillation. Ebert et al. (1981) in [154] presented initial theoretical concepts of the optimal conditions of oscillations for class E tuned power oscillators. Tsang et al. (1994) in [155] utilised large signal [S]-parameter design techniques to demonstrate high power class E oscillator at 900 MHz to provide 27.56 dBm output power with 57.54 % collector efficiency. More recent developments in switching mode oscillators include: C-band class E MMIC oscillator designed on standard 0.6 μm Triquint TQRXs MESFET GaAs process, where the variation of supply voltage demonstrated efficiency up to 43 % with 6.5 dBm output power at 4.4 GHZ with 1.8 V supply voltage [96]. Chang et al. (2017) in [156] presented K-band class E high efficiency oscillator developed on 0.15 μm WIN GaAs pHEMT process. The oscillator demonstrates 19 % peak efficiency with 21 dBm maximum output power from 23.5 GHz to 24.5 GHz.

This chapter presents development of class E oscillator using WIN PP10-15 GaAs MMIC process from WIN Semiconductor foundry, which is a 100 nm gate length InGaAs pHEMT process with substrate thickness of 4 mil. Detailed discussion on the process was presented in Chapter 6. Design, simulation and layout have been performed using the foundry's pdk in Keysight's ADS and Momentum microwave simulator, respectively. This chapter has been organised as follows. Section 7.2 presents design flow and topology for class E switching mode oscillators. Section 7.3 presents design and analysis of class E amplifier and covers discussion on optimum bias conditions, selection of appropriate transistor size, load pull analysis to ascertain optimum load termination network, input matching network for maximum power transfer and large signal results at various input power drive levels. Section 7.4 presents the design of feedback network to provide the necessary conditions of oscillation and final layout of class E oscillator. Section 7.5 will

present initial on-wafer measurement results of the oscillator MMIC followed by concluding remarks in Section 7.6.

7.2 Class E Oscillator Structure and Design Flow

Fig. 7. 1 shows generalised structure for class E oscillator presented in this chapter. The circuit comprises of shunt capacitance C_p with output capacitance (C_{ds}) at the drain of common-source FET to achieve switching behaviour. Conjugately matched input network provides maximum power transfer to the gate. Load termination network includes an LC tank at the fundamental frequency and an output transmission line, which can be designed using load pull simulations to achieve maximum output power and efficiency. The LC network will be converted to an equivalent distributed element network. Bias networks shown in the figure include quarter wavelength transmission lines at drain and gate of the transistor and decoupling capacitors. The feedback network provides necessary conditions of oscillations and is designed using voltages and currents (V_{in}, V_{out}, I_{in} and I_{out}) at the two reference planes i.e. A and B.

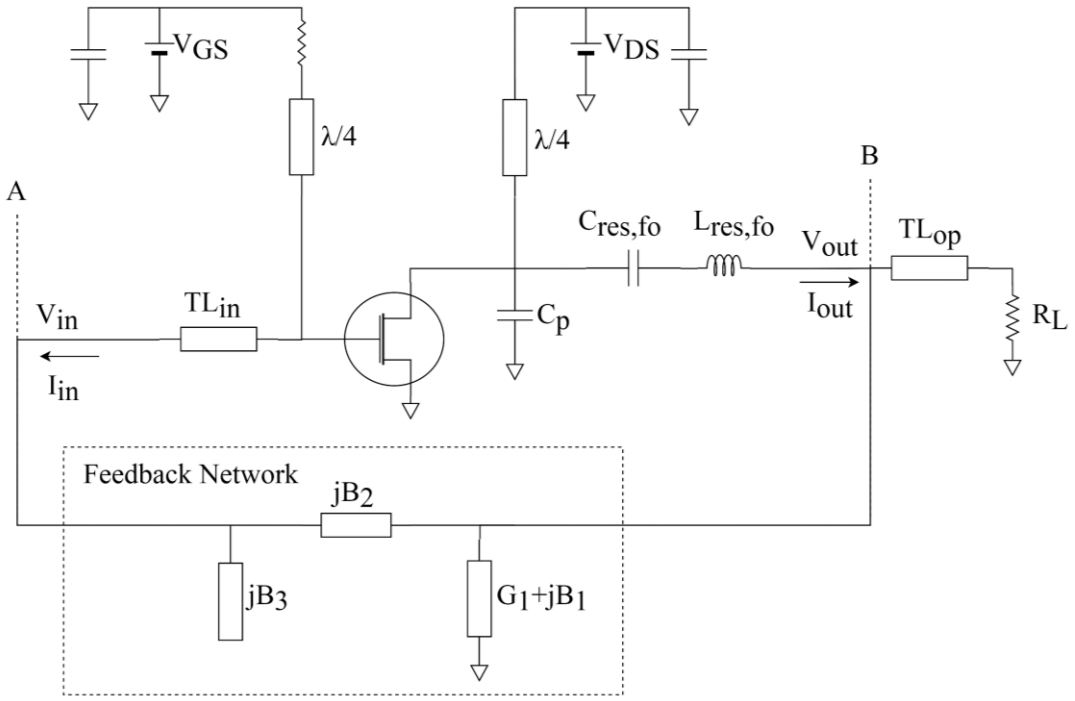


Fig. 7. 1: Generalised structure for class E oscillator

The design process for class E oscillators can be broadly divided into three steps, i.e. design and optimisation of class E amplifier, design of feedback network, and transient analysis for optimisation of class E oscillator. Design of class E amplifier starts with selection of appropriate transistor from the respective MMIC design process followed by selection of deep class AB bias conditions that along-with high input power level would

have a loadline shown in Fig. 7. 2 (load-lines of other reduced conduction angle amplifiers have also been shown for comparison). Once optimum bias conditions are identified, load pull simulations/measurements are performed at the fundamental frequency (also the frequency of oscillation) to select appropriate load impedance; followed by identification of conjugately matched input network to provide maximum power transfer to the transistor. Large signal analysis is performed with EM simulated networks followed by parametric optimisation to satisfy class E operation and achieve maximum PAE and output power. Feedback network is designed next through voltages and currents (V_{in}, V_{out}, I_{in} and I_{out}) at the two reference planes, i.e. A and B of class E amplifier. Finally, the feedback network is connected with class E amplifier and transient analysis is performed for optimisation of the oscillator. The above mentioned design steps and corresponding analysis will be discussed in the following sections.

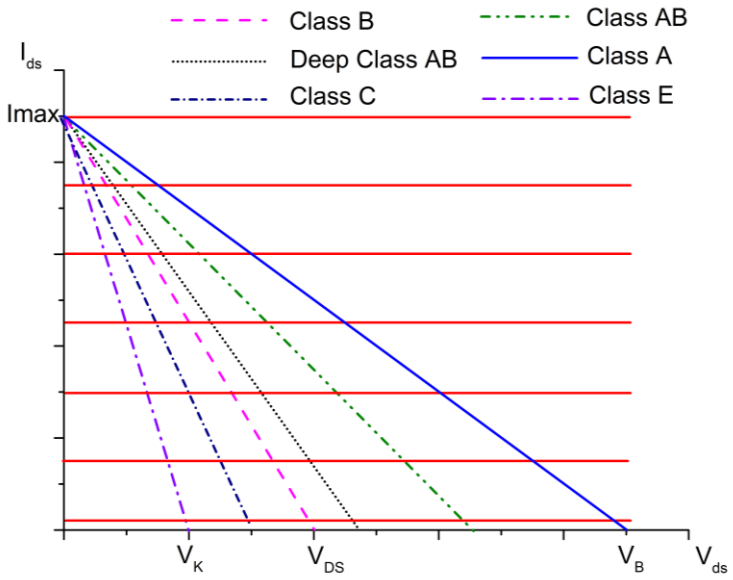


Fig. 7. 2: Loadlines of reduced conduction angle amplifiers

7.3 Design and Analysis of Class E Amplifier

7.3.1 Introduction

The theory of class E switching mode amplifiers was first presented by Sokal (1975) in [157], while underlying design equations were derived by Raab (1977) in [158]. The behaviour of transistor in class E mode is considered as a switch with a shunt capacitance C_p to the drain terminal that does not act as a parasitic, nor as a harmonic short circuit. This way, current flows through the transistor (which acts as a switch) during the 'on-state', and through the shunt capacitor during the 'off-state'. Integration of the voltage waveform starts from 0, which is the point when the switch opens, and the current is transferred from the switch to the shunt capacitor. The voltage waveform crosses the zero

point again when the switch closes, and the current is transferred to the switch. Thus, current and voltage waveforms do not overlap each other and a theoretical DC to RF efficiency of 100 % can be justified. Grebennikov (2004) in [78] presents various parallel load network configurations for class E amplifiers having a shunt capacitance (C_p) and RLC load termination network where C_p, L and C are tuned at the fundamental frequency, while the resistor R is required to perform voltage and current waveform shaping. Such a network has been shown in Fig. 7. 3, which has been reproduced from [64].

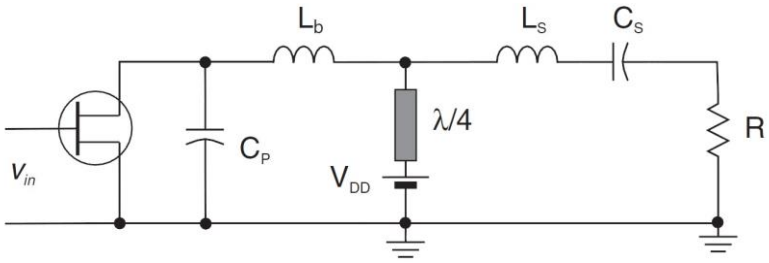


Fig. 7. 3: Topology for generalised class E amplifier load network with quarter wavelength transmission line in the biasing network

Preceding discussion considers operation of the transistor as an ideal switch, which cannot be extended to high frequency operation in microwave frequencies where non-linear output capacitance of the transistor provides short circuit conditions to higher order voltage components and the transistor cannot be explained as an ideal switch. However, the current waveform at high frequencies remains unchanged and the voltage waveform is engineered through the load network [64]. Fig. 7. 4 shows basic circuit schematics of class E amplifier that will be discussed in this section.

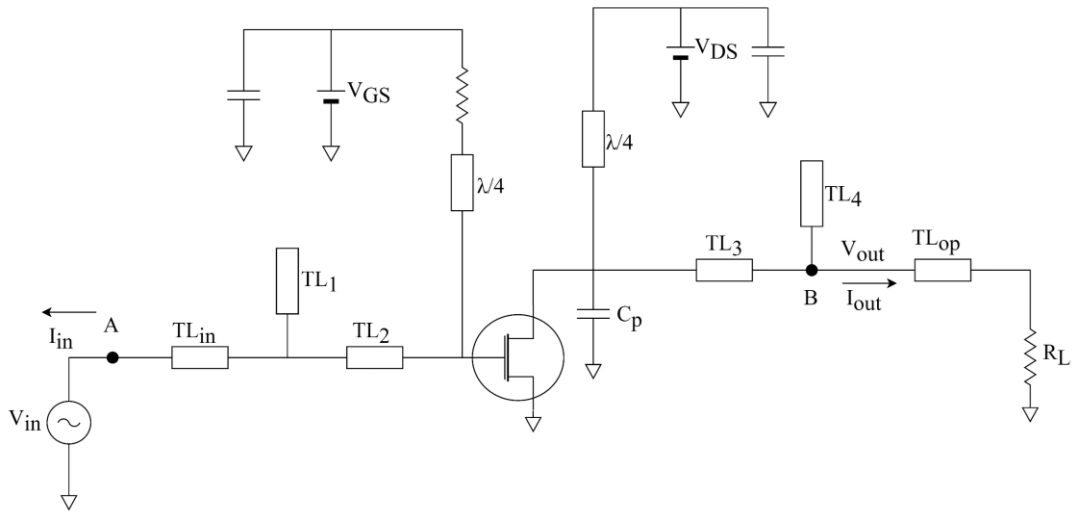


Fig. 7. 4: Generalised schematics of class E amplifier

7.3.2 Optimum Bias Conditions and Transistor Selection

The WINPP10-X process provides F_t greater than 135 GHz and F_{max} over 185 GHz, however, the maximum frequency of operation for class E amplifiers is defined in terms of the transistor's output capacitance, and the drain to source voltage as discussed in Chapter 3 on literature review. In switching mode amplifiers, large sinusoidal input power level is required to drive a large transistor to charge and discharge the input capacitance, which also increases with an increase in the frequency. Switching operation enables class E amplifiers to achieve decent efficiency with a large device but at the cost of reduced gain. A smaller transistor driven with low input power drive level can provide much higher gain; but its lower transconductance, high transistor's on-resistance (R_{on}) and large drain voltage waveform swing causes reduced efficiency. At the design frequency of 14.5 GHz, large output capacitance and I_{max} is required, which can be achieved through a transistor with a larger gate periphery. Thus, 4×150 µm pHEMT from WINPP10-15 GaAs process has been selected to operate in the saturation region under deep class AB bias conditions alongside a high enough input power level to reduce the transistor's R_{on}. The drain to source voltage is low ($V_{ds} \approx 0$ V) when the transistor is switched on but increases with an increase in R_{on}. However, a small value of R_{on} alongside a high value of load resistance at the fundamental frequency could be utilised to achieve high output power. Fig. 7. 5 shows simulated DC IV curves of 4×150 µm CS GaAs pHEMT transistor from WINPP10-15 pdk, where V_{gs} has been swept from -1.0 V to 0 V with steps of 0.1 V; and V_{ds} has been swept from 0 V to 0.2 V with steps of 0.5 V.

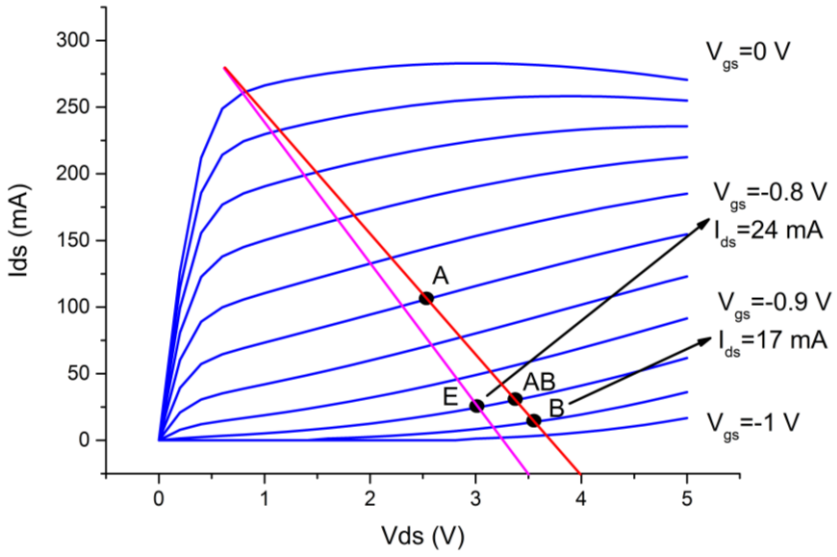
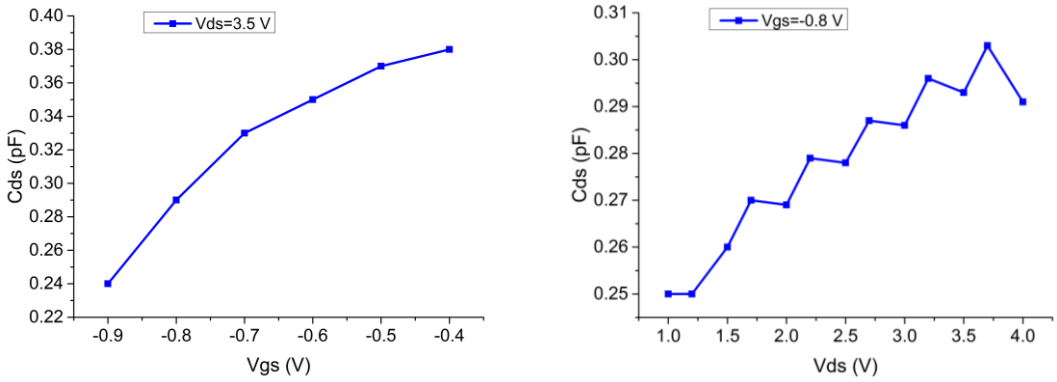


Fig. 7. 5: DC IV curves of 4× 150 µm CS pHEMT showing optimum bias point for class E amplifier operation

7.3.3 Output Capacitance

Output capacitance of the transistor plays an important role in class E switching mode operation where the current passes through the output capacitance during the off-cycles. The combination of output capacitance and parallel capacitance C_p defines the maximum frequency of operation. Calculation methodology of transistor's output capacitance was discussed in Chapter 4 and 6 by using Eq. 4.7-4.11. A similar methodology as used in Chapter 6 will be utilised here to calculate output capacitance of 4× 150 µm CS pHEMT. Fig. 7. 6 shows the values of output capacitance C_{ds} for 4×150 µm CS pHEMT with variation in (a) V_{ds} from 1 V to 4.0 V for $V_{gs} = -0.8$ V and (b) V_{gs} from -0.9 V to -0.4 V for $V_{ds} = 3.0$ V; at 14.5 GHz. The value of $C_{ds} = 0.29$ pF at optimum bias conditions for class E operation.



(a) (b)

Fig. 7. 6: Variation of output capacitance C_{ds} of 4×150 µm CS pHEMT from PP10-15 pdk for (a) variation in V_{gs} and (b) variation in V_{ds}

7.3.4 Design of Source and Load Termination Networks

Optimum bias conditions for class E operation were discussed in the preceding section and it was emphasised that small value of R_{on} alongside high fundamental load resistance could be utilised to achieve high output power. Load pull simulations are performed to optimise fundamental load resistance to achieve both high power and PAE from class E amplifier. Furthermore, load termination network should also provide high reactive impedance at harmonic frequency components with suppression to a low level compared to the fundamental frequency component. This may be achieved through parallel capacitance C_p in shunt with output capacitance C_{ds}. Peak voltage and current across the drain should also comply with device limitation, where the suggested average value of breakdown voltage $V_{BR} \approx 9$ V in the process handbook [148].

Input Matching Network

The input network plays an important role in enabling transistor's operation as a switch and helps to reduce the transition time between on and off states, where the conduction current flows through the transistor and the output capacitance, respectively. This would suggest that the ideal input drive waveform for class E amplifier should thus be a square wave like in class F amplifiers. A square waveform could be provided at the gate through the design of appropriate harmonic trapping network with short circuit conditions at even order harmonics and open circuit conditions at odd order harmonics; however, it would result in increase in circuit complexity and would be difficult to accommodate within the available cell size on the tape-out wafer. Thus, pure sinusoidal input drive waveform would be used to drive the transistor with conjugate matched input impedance to ensure maximum power transfer. An input impedance of $Z_s = 26.4 + 15.3\text{j}\ \Omega$ was obtained and fine-tuned through source pull simulations. Circuit schematics of input matching network have been shown in Fig. 7. 7 which consists of transmission lines and open circuit stub shown in Fig. 7. 4. Meandered quarter wavelength transmission line to bias the gate terminal was also included in the input matching network. EM simulations in Momentum microwave simulator were performed down to DC followed by parametric optimisation to achieve desired impedance at input terminal of the transistor.

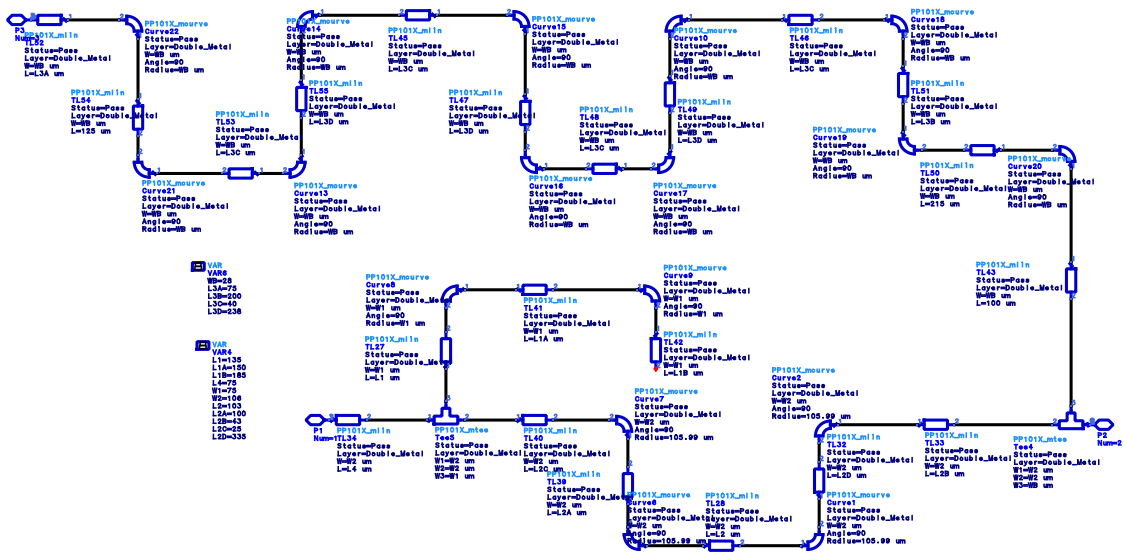


Fig. 7. 7: Circuit schematics of input matching network of class E MMIC amplifier

The layout of input matching network has been shown in Fig. 7. 8, which includes an on-chip decoupling capacitor in the gate bias line.

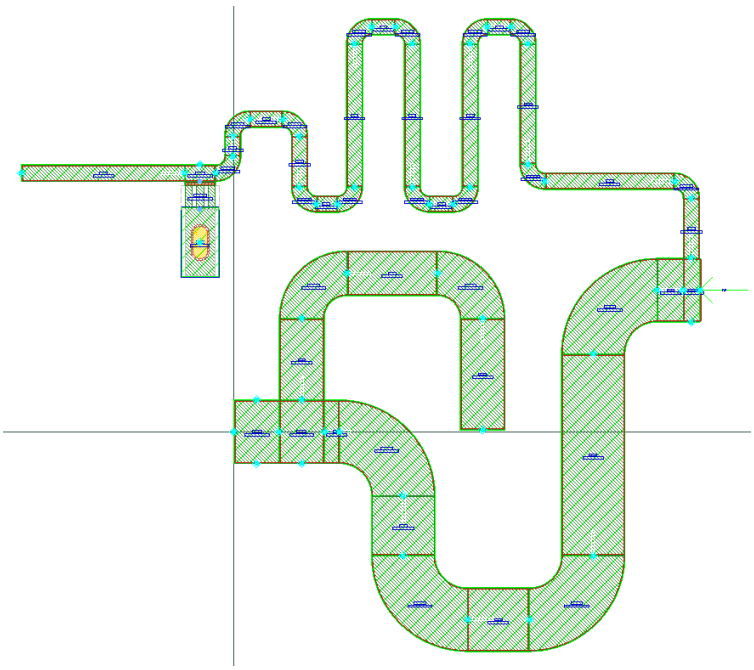


Fig. 7. 8: Layout of input matching network of class E MMIC amplifier

Output Matching Network

Load pull simulations were performed at respective bias conditions and various input power drive levels to obtain optimum load impedance ($Z_L = 13.9 + 5\text{j}\ \Omega$) for maximised output power and PAE at 14.5 GHz. Shunt capacitance $C_p = 0.25$ µm (COV from PP10-15 pdk) was added to the transistor's drain terminal, which was calculated through classical design equations reported in [64] and discussed in literature review. The shunt capacitance alongside quarter wavelength drain bias line acts as a second harmonic blocking filter to suppress the second harmonic component which increases with an increase in the input power drive level due to generation of harmonic components across the non-linear output capacitance. Fig. 7. 9 shows schematics of output matching network of class E amplifier which includes quarter wavelength transmission line to bias the drain terminal.

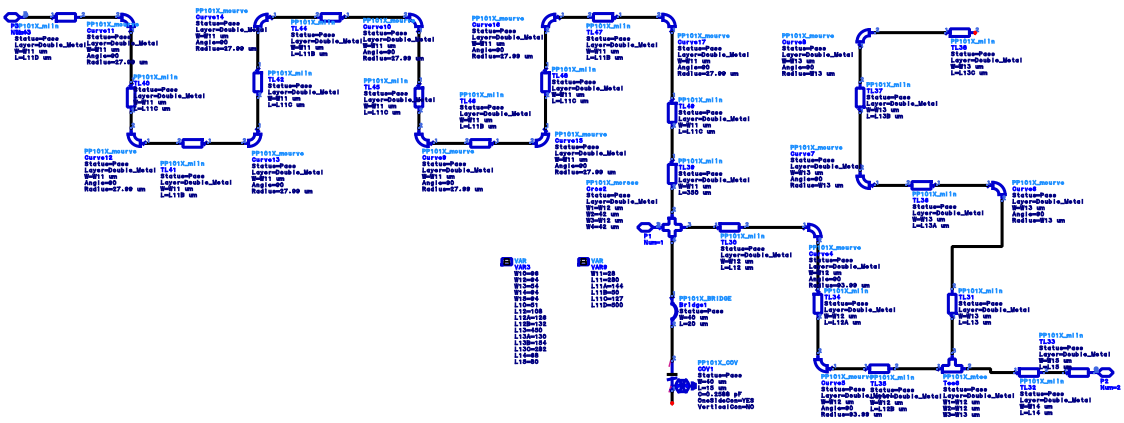


Fig. 7. 9: Circuit schematics of output matching network of class E MMIC amplifier

The layout of input matching network has been shown in Fig. 7. 10, which includes an on-chip decoupling capacitor in the drain bias line.

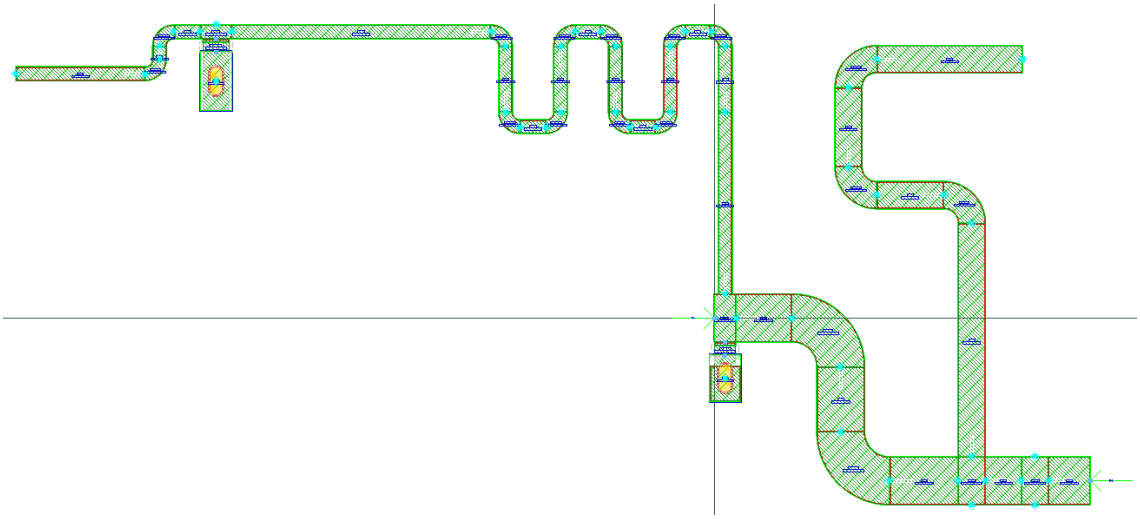


Fig. 7. 10: Layout of output matching network of class E MMIC amplifier

The amplifier was optimised with EM simulated networks down to DC with the lumped and distributed elements showing Q-factor greater than 20. The high value of quality factor leads to lower relative damping in the resonators; which is helpful to sustain oscillations when the amplifier is operating as a DC-RF oscillator with a feedback path.

7.3.5 Results and Analysis of Class E Amplifier

This section presents discussion on various results for class E amplifier which are optimised to obtain voltages and currents at amplifier's terminal (A and B shown in Fig. 7. 3 and Fig. 7. 4) to design the feedback network that will enable amplifier's operation as a switching mode oscillator. The results have been obtained through small signal [S]-parameter and large signal harmonic balance simulations in Keysight's ADS with EM simulated networks using Momentum Microwave simulator. These results have been previously presented by the author in [153].

Small Signal [S]-parameters

Fig. 7. 11 shows simulated small signal [S]-parameters of class E amplifier with EM simulated input and output networks discussed in the preceding section. Low value of small signal gain $S_{21} = 9.07$ dB can be observed at 14.5 GHz for such a large transistor (4×150 μm), especially when compared to class AB amplifier which provided 7.2 dB small signal gain at 30 GHz with a smaller transistor (2×50 μm). However, it needs to be mentioned that a low drain bias voltage $V_{dq} = 3.0$ V was used to achieve lower R_{on} which can justify reduced small signal gain.

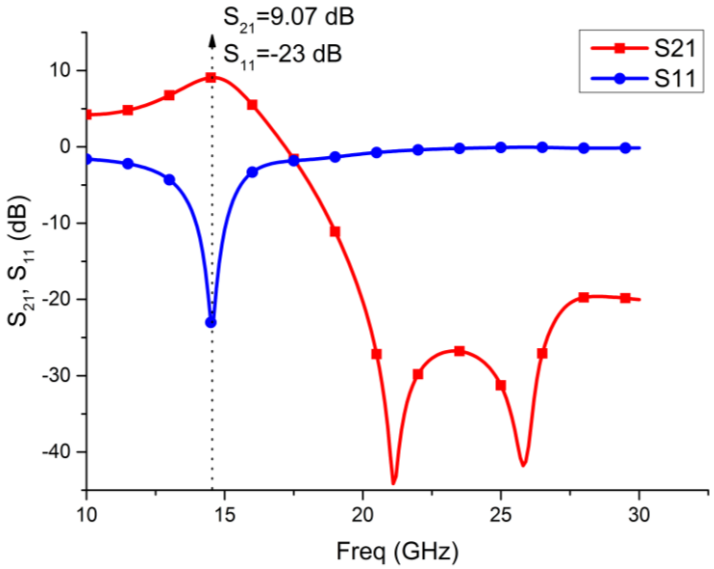


Fig. 7. 11: Small signal [S]-parameters of class E MMIC amplifier with EM simulated networks

Drain Voltage and Current Waveforms

Drain voltage and current waveforms are useful to understand behavioural aspects of class E amplifiers that include the effect of overlapping voltage and current waveforms, switching transition time from on-state to off-state and vice versa, the difference between switching transition times, and the effect of on-resistance R_{on}. Fig. 7. 12 shows current and voltage waveforms for class E amplifier under deep class AB bias conditions discussed in Section 7.3.2 earlier. The waveforms have been shown at two different input power drive levels $P_{in} = 17$ dBm and $P_{in} = 19$ dBm across 1 dB gain compression which occurs at $P_{in} = 17.6$ dBm. Drain current and voltage waveforms at 1 dB gain compression have been shown in Fig. 7. 13.

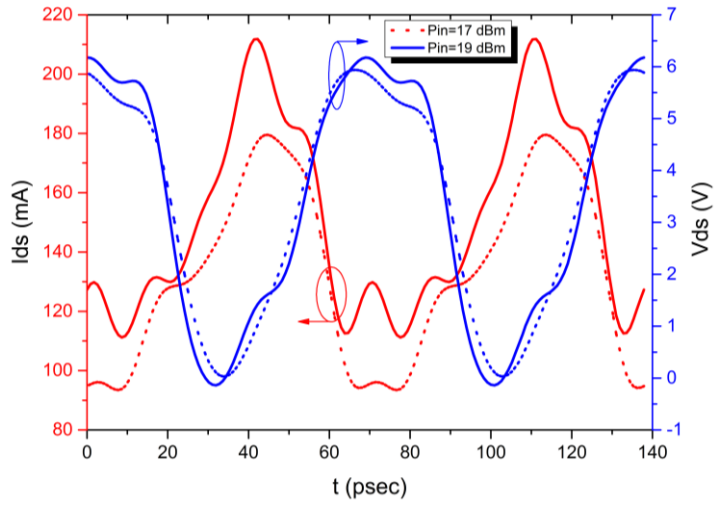


Fig. 7. 12: Drain voltage and current waveform of class E amplifier for $P_{in} = 17$ dBm and $P_{in} = 19$ dBm

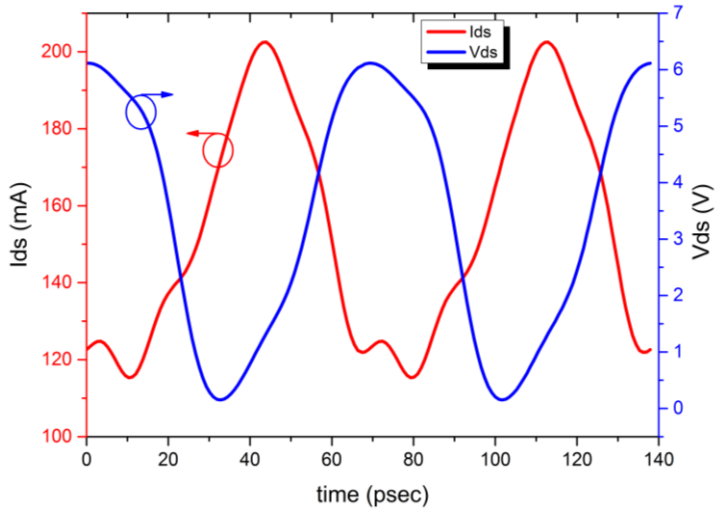


Fig. 7. 13: Drain voltage and current waveform of class E amplifier at 1 dB gain compression corresponding to $P_{in} = 17.6$ dBm

Optimum input power drive level for class E amplifier can be explained by comparison of current and voltage waveforms shown in Fig. 7. 12. Negative drain voltage values depicted by the amplifier at $P_{in} = 19$ dBm can potentially cause transistor failure. Such negative values can however be prevented through: 1) increase in drain bias voltage but an associated drawback would be increased DC power consumption or reduced drain efficiency, 2) Restricting the input power drive level, or 3) optimisation of load network while considering second harmonic impedance at the drain to be short circuited through shunt C_p or quarter wavelength bias line. This also validates the role of fundamental load termination network towards voltage waveform shaping. Drain current and voltage waveforms at 1 dB gain compression (corresponding to $P_{in} = 17.6$ dBm) shown in Fig. 7. 13 are similar to idealized waveforms presented in literature with discrepancies in terms of overlapping regions between the waveforms. At these instants the transistor switches from on-state to off-state and vice versa. Ideally, the current should rapidly switch to zero while the voltage waveform is rising. Another important factor is the difference in transition time from on-state to off-state and off-state to on-state. It can be observed that the latter transition time is greater than the former, which contributes towards reduced efficiency. A possible reason for the difference between non-ideal switching from on-state to the off-state is the depleted state of the transistor's output capacitance (C_{ds}) and incapability to support the required current. On the other hand, comparatively better switching can be observed to zero-voltage state because C_{ds} is already depleted.

The effect of R_{on} can be observed through ripples in knee region of the voltage waveforms. These appear during the cycle when the voltage waveform is in the knee region and the current waveform has a maximum, resulting in increased DC power consumption and reduced drain efficiency. Furthermore, the effect of R_{on} (and non-zero knee voltage) increases with an increase in input power drive levels (or gain compression) which can be observed by comparison of all three waveforms shown in Fig. 7. 12 and Fig. 7. 13.

Large Signal Analysis

Large signal analysis is important to predict the behavioural performance of an amplifier. The results shown in Fig. 7. 14 indicate that compression is achieved at lower input power levels and the corresponding output power is low compared to other high efficiency amplifiers at 1 dB gain compression. However, the PAE achieves a peak just when the saturation region of the amplifier starts, which is an important characteristic of class E amplifiers. This way, the amplifier isn't required to be driven into deep compression levels to achieve high PAE as with other high efficiency amplifiers like class F and F^{-1} amplifiers.

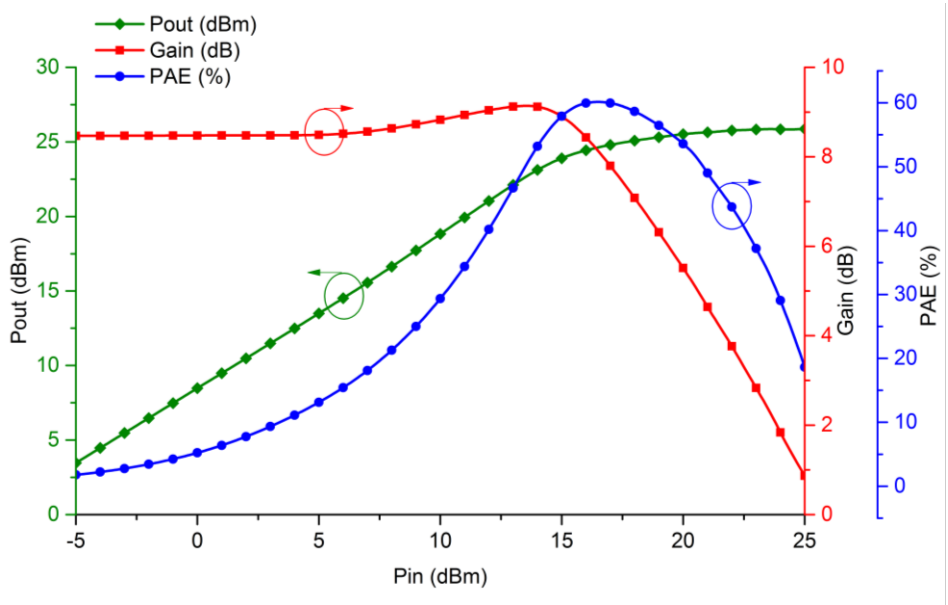


Fig. 7. 14: Large signal simulation results of class E amplifier, the y-axes from left to right represent output power (P_{out} in dBm), large signal gain (dB), and PAE (%), respectively

The amplifier shows decent large signal gain $G_{LS} = 7.38$ dB at 1 dB gain compression ($P_{in} = 17.6$ dBm) with ~24.98 dBm output power and 59.3 % PAE at the design frequency of 14.5 GHz. Large signal gain is decent due to low R_{on} and fundamental load impedance.

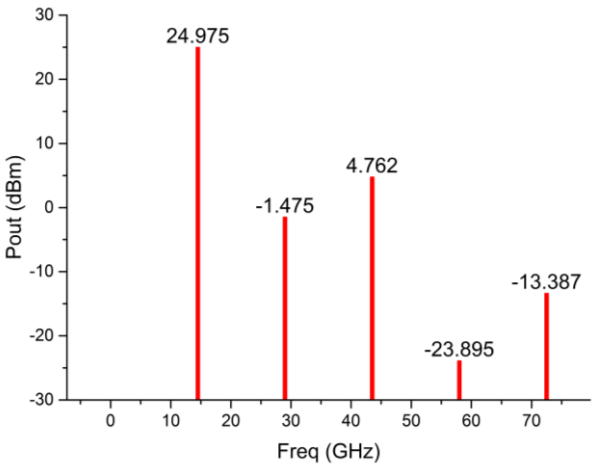


Fig. 7. 15: Output spectrum of class E amplifier at 1 dB compression level

Fig. 7. 15 shows the output spectrum of class E amplifier. $P_{out} = 24.98$ dBm at the fundamental frequency component can be observed. Second harmonic component suppression of -26.45 dBc is shown by the amplifier due to transistor's output capacitance, quarter wavelength drain bias line and the shunt capacitance (C_p); which is acceptable for continuous wave operation in medical applications. However, further optimization of second harmonic suppression could be performed with an improved estimation of the transistor's output capacitance and the shunt capacitance C_p. The second harmonic suppression is expected to be better in measurement results.

7.4 Design of Class E Oscillator

Feedback network for switching mode oscillators is synthesized at the fundamental frequency and can take either T or π network topologies, with both having their advantages which have been discussed in [90]. The feedback network shown in Fig. 7. 1 is a π-network with three reactive and one resistive circuit elements, i.e. jB_1, jB_2 and jB_3, and G_1, respectively. Two port Y-parameters discussed by Jeon et al. (2006) in [89] have been given in Eq. 7.1, which can be solved to calculate the design values for reactive and resistive values of the feedback network. The terminal voltage and currents (V_{in}, V_{out}, I_{in} and I_{out}) correspond to the ones shown at reference planes A and B in Fig. 7. 1 and Fig. 7. 3, which are obtained from the optimised class E amplifier discussed in the preceding section. It is important to mention that Eq. 7.1 is solvable only if the right hand side is not singular, i.e. the value of $V_{out} \neq 0$ and there exists a phase difference between V_{in} and V_{out} [90].

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \begin{bmatrix} j(B_2 + B_3) & -jB_2 \\ -jB_2 & G_1 + j(B_1 + B_2) \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \tag{7.1}$$

Eq. 7.1 was solved using MATLAB to determine the values of: B_1, B_2, B_3, and G_1, which can be utilised to determine the appropriate reactive and resistive circuit elements. The feedback network includes a transmission line and spiral inductor, MIM capacitor and an open circuit stub to implement: $G_1 + jB_1$, jB_2 and jB_3, respectively. After the design and optimisation of feedback network, transient analysis was performed to ascertain that the necessary conditions of oscillations were being generated to operate class E amplifier as an oscillator. Fig. 7. 16 and Fig. 7. 17 shows circuit schematics of the π-shaped feedback network for class E oscillator, and the layout in ADS, respectively.

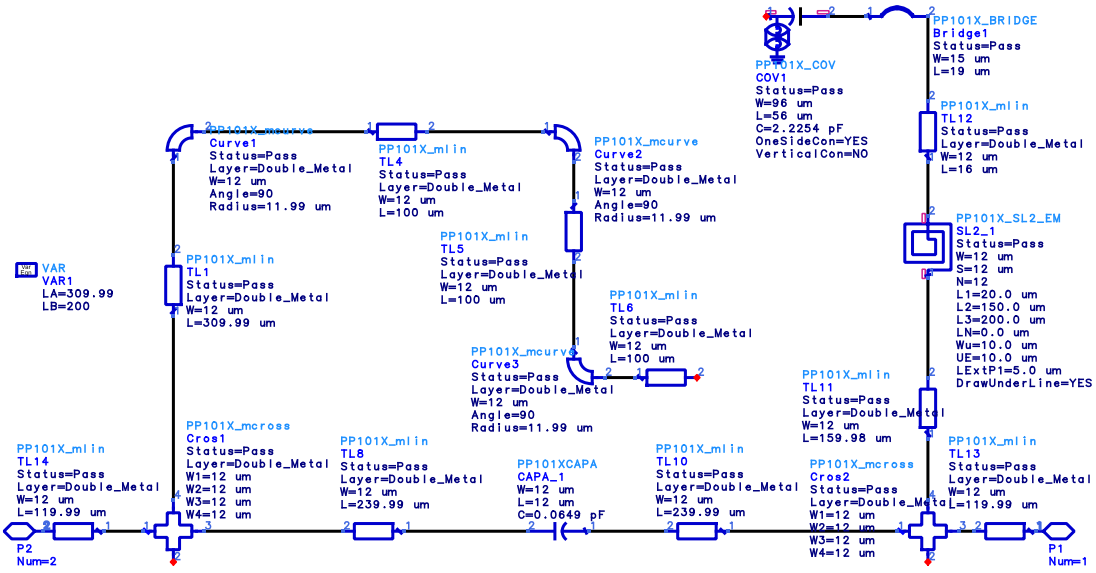


Fig. 7. 16: Circuit schematics of π-feedback network of class E MMIC oscillator

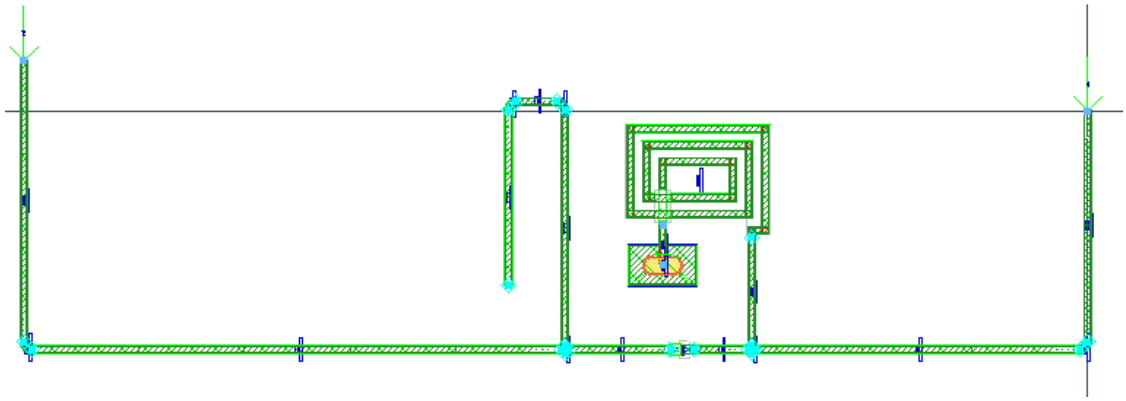


Fig. 7. 17: Layout of π-feedback network of class E MMIC oscillator in ADS

Final layout of the oscillator was performed in ADS and all lumped and distributed circuit elements were simulated with Momentum microwave simulator down to DC. Final schematics have been attached as Annex D, while the final layout has been shown in Fig. 7. 18. Discussion about DRC check is the same as discussed for class AB amplifier in Chapter 6.

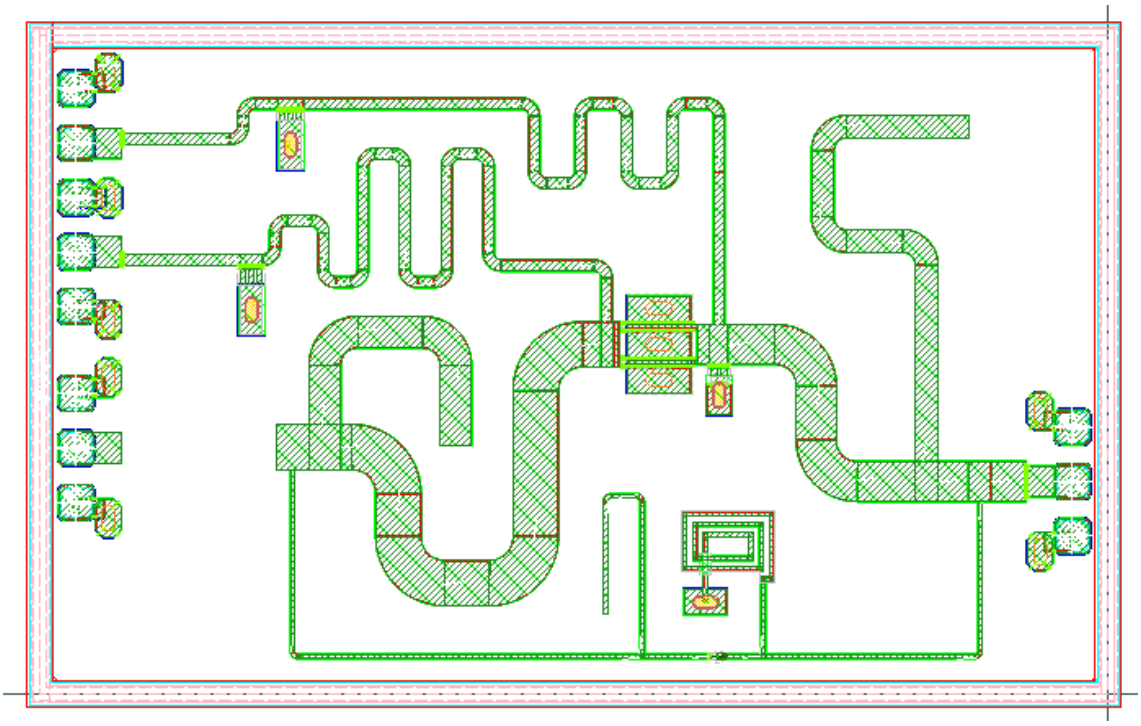


Fig. 7. 18: Layout of class E MMIC oscillator measuring 2450 × 1510 µm

7.5 Initial On-Wafer Measurements

Initial on-wafer measurements of class E oscillator were performed using Keysight's PNA-X N5247 network analyser with the drain and gate terminals biased through GSGSG 125 µm probes. Fig. 7. 19 shows probed micrograph of class E MMIC oscillator.

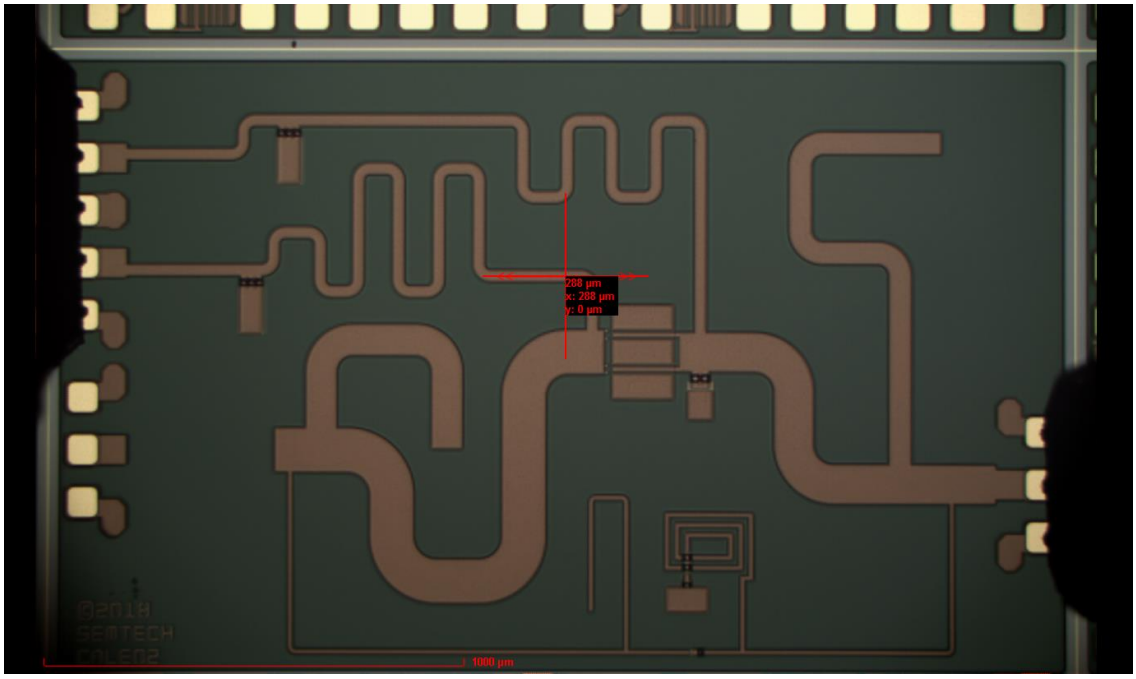


Fig. 7. 19: Probed micrograph of class E MMIC oscillator

Two sets of measurements were performed at measurement facilities in Semtech Limited. During the first set of measurements; gate was biased through GSG 125 µm probe at the

gate bias line, while drain was biased through GSG 125 µm probe at the output port due to unavailability of GSGSG 125 µm probe to bias both drain and gate terminal through their respective bias lines. The bias routine involved gate pinch-off at $V_{GS} = -1.2$ V and $V_{DS} = 2.0$ V at the drain, with current compliance set at the power supplies according to power handling capability of the bias tees. No oscillations were observed, and the gate was opened slowly. Initial oscillations were observed at $V_{GS} = -1$ V which were unstable with current compliance reached at the drain power supply, the drain voltage was subsequently reduced to ensure compliance. Results from the first set of measurement have been shown in Fig. 7. 20, for $V_{DS} = 1.10$ V and $I_{DS} = 3.94$ mA.

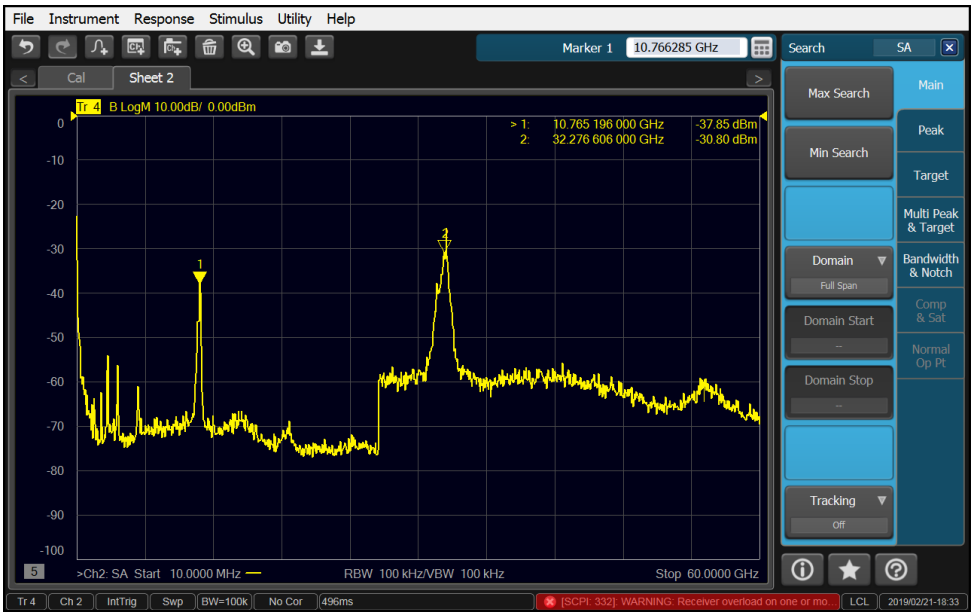


Fig. 7. 20: First set of on-wafer class E oscillator MMIC measurements

The second set of measurements involved gate and drain biasing through GSGSG 125 µm probe at the drain and gate bias lines with on-chip decoupling capacitors. Bias sequence involved gate pinch-off at $V_{GS} = -1.2$ V and $V_{DS} = 1.0$ V at the drain with respective current compliance at the power supplies. Initial oscillations were observed at $V_{GS} = -0.9$ V; however, drain voltage had to be reduced to ensure current compliance. Measurements were performed at $V_{DS} = 0.6$ V, $V_{GS} = -0.8$ V and $I_{DS} = 24$ mA, which showed clean oscillations at 10.7 GHz. The frequency shift is essentially observed due to different measurement bias conditions compared to design bias conditions. Nevertheless, simulations were run to observe if the measurements results matched up, which showed close agreement at 11 GHz. The oscillations touched a peak of 20.4 dBm output power, however, they were stable at 16.4 dBm output power showing 27.9 % DC to RF efficiency. The measured output spectrum has been shown in Fig. 7. 21 and Fig. 7. 22.

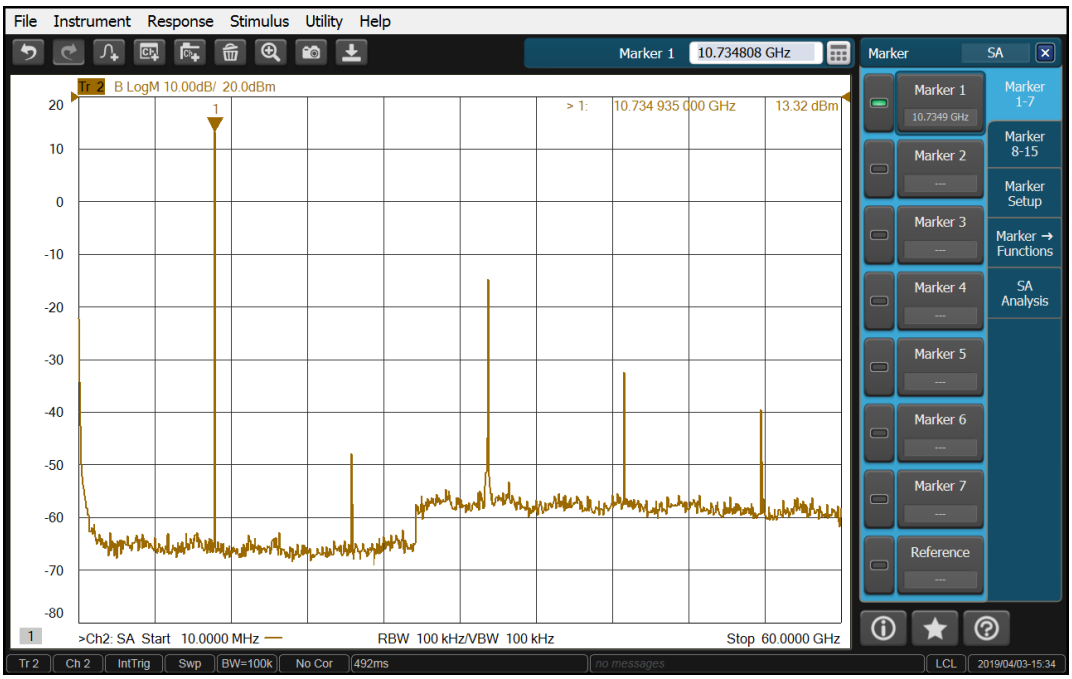


Fig. 7. 21: Measured output spectrum of class E MMIC oscillator at $V_{DS} = 0.6$ V, $V_{GS} = -0.8$ V and $I_{DS} = 24$ mA

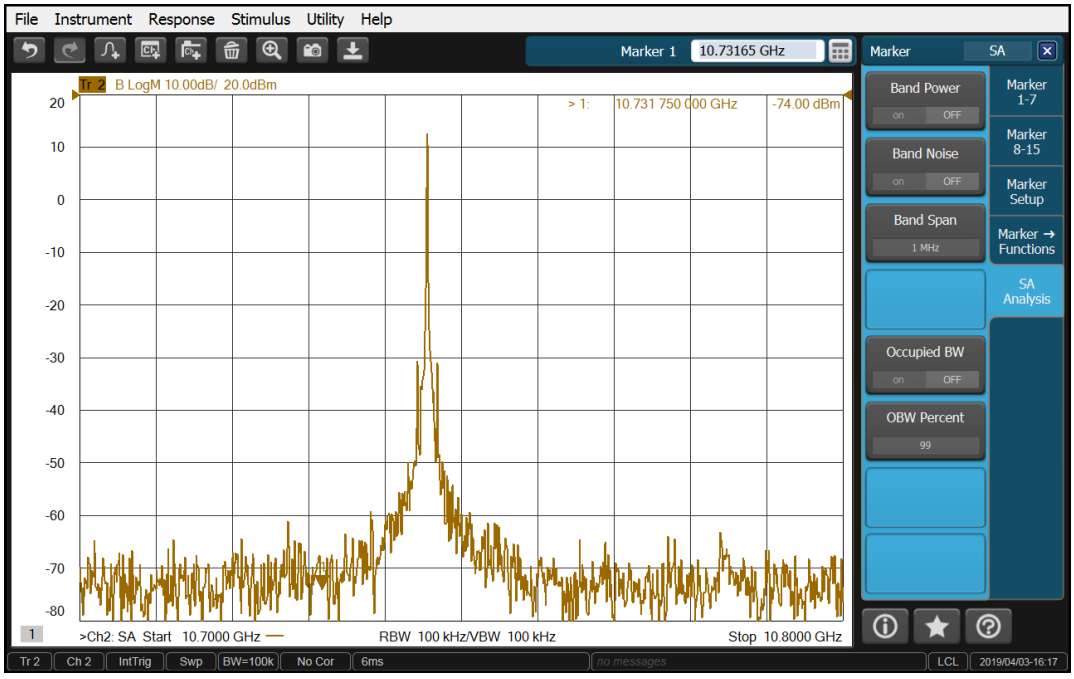


Fig. 7. 22: Measured output spectrum of class E MMIC oscillator at $V_{DS} = 0.6$ V, $V_{GS} = -0.8$ V and $I_{DS} = 24$ mA from 10.7 GHz to 10.8 GHz

Second harmonic suppression level better than 40 dBc can be observed in measurement results shown in Fig. 7. 21 due to short circuiting of second harmonic component. This behaviour wasn't observed in simulation which predicted inaccuracy of WIN PP10-15 non-linear models, especially for large signal operation close to the knee region of high efficiency class E mode.

7.6 Conclusion

This chapter presented design and analysis of class E MMIC oscillator for X-band medical applications with initial on-wafer measurements using bias conditions in compliance with power handling capability of the bias tees. Simulations of class E oscillator with EM simulated networks provide 24.3 dBm output power with 48 % peak DC to RF efficiency at 14.5 GHz under deep class AB bias conditions. However, initial on-wafer measurements at reduced drain current bias conditions provide clean oscillations on the spectrum analyser with up to 20.4 dBm peak output power at 10.7 GHz. Further measurements are ongoing and will include packaging of the MMIC die that will be mounted on a custom designed PCB evaluation board for further measurements and testing. Future iterations of the oscillator circuit could include conversion of lumped component π-network feedback path to a distributed network to provide necessary conditions of oscillator and optimisation of shunt capacitance C_f.

Chapter 8

Conclusions and Recommendations for Future Work

8.1 Summary

The research work presented in this thesis was targeted for electrosurgical devices and therapeutic systems at various microwave frequencies in C-band, X-band, Ku-band and Ka-band to enable generation of controlled and localised microwave power close to the treatment site. The research problem was developed by considering limitations and drawbacks associated with microwave power generators currently employed in medical applications, where a large amount of microwave power is lost as heat during transmission using lossy coaxial cables. For instance, heat dissipation in the endoscopic channel can cause unintended distributed tissue heating. Furthermore, microwave power generators are large and cumbersome which limit their use beyond operation theatres or specialised medical facilities for established treatment procedures using microwave energy like coagulation of bleeding sites. Such treatment procedures are very effective compared to conventional modalities especially in emergency stricken areas, ambulances and battlefields where the latter become ineffective. Thus, contributions were made towards overcoming these limitations by developing high efficiency power amplifiers and oscillator.

Chapter 4 discussed high efficiency class AB, class F and multistage amplifiers for portable haemostatic applications to effectively coagulate bleeding sites in emergency stricken areas and battlefields where leading cause of death is excessive blood loss and ineffectiveness of conventional coagulation treatment procedures. Initial testing and validation of these amplifiers were conducted on porcine liver bench model which showed good efficacy.

Chapter 6 presented discussion on the development of high efficiency class AB MMIC amplifier operating at 30 GHz, which is envisaged for application within an on-chip diagnostic and neutralisation system for glioblastoma and medulloblastoma cancerous cells. Initial small signal $[S]$-parameter measurements were performed which showed similar small signal gain at 30 GHz, however, difference in gain roll-off was observed. Chapter 7 presented high efficiency class E MMIC oscillator operating at 14.5 GHz targeted for endoscopic surgical procedures for the treatment of benign and cancerous lesions, reshaping the cornea, male sterilisation and menorrhagia. Initial on-wafer measurements of the oscillator were performed at reduced bias conditions which showed

clean oscillations at 10.7 GHz. The MMIC oscillator die measures 2450×1510 μm and can be located at the tip of an endoscopic channel (3.22 mm in diameter) to generate localised microwave power close to the treatment site. However, further optimisation of the circuit can be performed to reduce these dimensions.

Table 8. 1: Summary of various measurement results of discrete power amplifiers

Characteristics	**Symbol**	**Unit**	**Amplifier**		
			Class AB	**Class F**	**Multistage**
Operating Frequency	f	GHz	5.8	5.8	5.8
Output Power (1 dB)	$P_{1\text{ dB}}$	dBm	40.5	41.24	42.8
Output Power (optimum)	P_{out}	dBm	41.15	41.82	43.4
Large Signal Gain (optimum)	G_{LS}	dB	8.35	7.1	6.7
Power Added Efficiency (optimum)	PAE	%	62.1	55.2	65.4* **DC to RF*

Table 8. 1 summarises various large signal measurement results of discrete power amplifies which were designed using non-linear device models of commercially available Cree GaN HEMT CGH55015 and CGH55030 transistors in Keysight's ADS and Momentum Microwave simulator. However, limitations of the models were observed due to transistor's operation close to the knee region. This was observed in improved efficiency of class AB amplifier compared to class F amplifier; where short circuit termination to the second harmonic component was provided through a shunt quarter wavelength transmission line in the former, while harmonic trapping network was used in the latter to provide short and open circuit conditions to second and third harmonic components, respectively. Ideally, the harmonic trapping network alongside fundamental matching network should provide appropriate load conditions at the fundamental and higher order harmonics; however, their dependence on non-linear behaviour of the transistor cannot be neglected. Besides this, accurate estimation of transistor's non-linear behaviour is much important in load pull simulations to obtain optimum fundamental load

and source impedance. Target specifications including high efficiency operation were nevertheless achieved from the amplifiers.

Class AB power amplifier and class E oscillator MMICs were designed, EM simulated and processed for layout using non-linear models of various active and passive circuit elements from WINPP10-15 pdk in Keysight's ADS and Momentum Microwave simulator. The process from WIN Semiconductors foundry is a 0.1 μm gate length AlGaAs/GaAs pHEMT process with 100 μm substrate thickness. Large signal on-wafer measurements of class AB power amplifier and class E oscillator MMICs couldn't be performed due to the limitations of power handling capability of bias tees at the measurement facilities. Nevertheless, small signal [S]-parameter measurements of class AB amplifier die were performed. Initial on-wafer measurements of class E oscillator at reduced bias conditions showed clean oscillations with peak output power of 20.4 dBm, whereas stable oscillations with 16.4 dBm output power and 27.9 % DC to RF efficiency were observed at 10.7 GHz. The shift in frequency is mainly because of different bias conditions than the designed ones and inaccuracies of various non-linear models of the transistor and passive elements. Besides this, the feedback network to provide oscillations was designed according to input and output voltages and currents of class E amplifier at optimum bias conditions. Simulations were run at measurement bias conditions and similar results were obtained for the oscillator at 11 GHz.

8.2 Research Outcomes

8.2.1 Portable Haemostasis Device

Portable haemostasis structure operating at 5.8 GHz was presented to achieve sufficient power density to effectively coagulate bleeding sites in emergency stricken areas and battlefields which are difficult to treat under conventional haemostatic modalities. Power pack housing high efficiency power amplifier capable of providing 22 W CW microwave power was developed for this purpose and efficacy was demonstrated on porcine bench liver model in a controlled and relatively small treatment area.

8.2.2 Localised Power Generation for Endoscopic Surgical Applications

An important drawback of microwave endoscopic surgical procedures to deliver microwave energy to a tissue site located within the human body is distributed tissue heating and loss of much microwave power due to lossy coaxial transmission lines. Class E MMIC oscillator operating at 14.5 GHz shows strong usefulness for such applications in X-band and Ku-band microwave frequencies due to its small size and the ability to travel down through an endoscopic channel.

8.2.3 Power Amplifier MMIC for Ka-band Diagnostic and Surgical Applications

Class AB MMIC amplifier operating at 30 GHz was targeted for much emerging millimeter wave medical application areas including the characterisation and treatment of brain and spine cancers. The intended application area for the amplifier presented in this thesis was however an on-chip diagnostic and neutralisation system for medulloblastoma and glioblastoma cancerous cells which are highly malignant grade IV cancerous cells.

8.3 Recommendations for Future Work

Various recommendations for future work covering high efficiency PA design and medical applications areas are listed below:

1. Future iterations of the amplifier board (power pack) for portable haemostasis applications could include an onboard oscillator and power amplifier stages to generate required microwave power with high efficiency. The optimised power pack could later be developed into an MMIC with all components of the system on a single chip. GaN MMICs are suggested for this purpose due to their better performance for high power applications compared to GaAs MMICs that were discussed in this thesis.
2. The rendered haemostasis system can be extended to further portable medical applications for the treatment of spider veins, thread veins and cosmetic surgery which are performed at 5.8 GHz with an optimal CW microwave power ~12 W.
3. Differences in measurement and simulation results suggest inaccuracies in non-linear models of commercially available GaN CGH55015 and CGH55030 HEMT transistors. For improved design, EM simulations and performance prediction; measurements of transistor's bare die (including load pull measurements) at optimum bias conditions for respective amplifier modes should be used to develop non-linear simulation models. These transistors are currently distributed in flange and pill packages, whereas respective bare dies aren't commercially available.
4. MMIC design of high efficiency amplifier and oscillator presented in this thesis was based on non-linear device model provided by WIN Semiconductor foundry. However, device pull-outs could be fabricated on wafer and measured to generate full empirical non-linear model (and parameter extraction) at optimum bias conditions. Furthermore, load pull measurements using slide screw tuner method discussed in Chapter 3 could also help to achieve much improved performance.

5. The π-feedback network of class E oscillator presented in this thesis consists of lumped and distributed elements to provide necessary conditions for oscillations. However, the lumped components could be converted into distributed elements. Furthermore, improvement in non-linear device models and measurement based parameter extraction could help in performance enhancement.
6. Large signal measurements of MMICs couldn't be performed due to limited power handling capability of the bias tees at the measurement facilities. However, the MMIC die will be packaged and mounted on a custom designed PCB evaluation board for further measurements and testing.

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ANNEX A- Review Paper on Load Pull Simulations of GaN HEMT

GaN HEMT Power Amplifier and Applicator Structure for Microwave based Medical Applications

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***Abstract*— This paper presents an integrated applicator structure achieving a sufficient power distribution density to cause coagulation in the human tissue. The handheld applicator structure operating at 6 GHz includes: a 5 W power amplifier (PA) designed using a 12 finger GaN HEMT device and a simple end loaded monopole antenna. The PA, including the matching circuitry has been located close to the antenna allowing more power available at the tip and a hand-held compact structure. Device modelling and simulated measurements show a return loss figure of -30.095 dB, thus, enabling optimised power absorption in the human tissue. The applicator structure has good prospects for implementation within electrosurgical devices using microwave energy to treat spider veins, thread veins and for cosmetic surgery.**

Index terms*— *GaN HEMT, Electrosurgery, Microwave, Load-pull Measurements, Monopole, Coagulation, Cosmetic surgery.

Introduction

Microwave energy has a number of beneficial clinical and surgical effects [1]. Owing to their non-ionising nature, RF and Microwave energy have been utilised for the diagnosis and treatment of human subjects for various medical interventions including ablation of tumours, atrial fibrillation, wound sterilisation, enhanced liposuctions, cosmetic procedures and various endoscopic, laparoscopic and open surgeries [2], [3].

With the advent of Gallium Nitride High Electron Mobility Transistor (GaN HEMT) technology, tens of Watts of microwave power can be delivered by the development of a compact and efficient microwave power source. This can enable localised treatment at the wound site. Localisation can overcome various issues in the conventional treatment devices like energy loss, and can enable the model for controlled treatment. GaN HEMTs provide excellent properties over competitive semiconductor technologies like GaAs HEMTs. These include: wide-bandgap, high power density, high breakdown voltage and fields, high output impedance, switch-mode amplification and effective power density dissipation to prevent excessive channel heating-up [4].

This paper presents an integration of 12x125 µm GaN HEMT device operating at 6 GHz with a surface applicator antenna to provide an output power of 5 W for point coagulation to treat various medical conditions. The transistor device was designed in collaboration with Filtronic Broadband Limited (FBL) at the University of Manchester (UoM). On-wafer small and large signal measurements were performed using Keysight's 8510XF and 8510C VNAs and Maury Microwave slide screw tuners (type no. 8045p) respectively. Load pull measurements were performed to obtain optimum input and output impedances for maximum output power of the PA. A handheld applicator structure housing the PA, matching circuitry, a coaxial transmission line and an end loaded monopole antenna has been modelled and designed at Bangor University.

Design of Power Amplifier

12x125µm GaN HEMT Device

The design of power amplification device has been carried out with the aim of achieving maximum output power by utilising the 0.25 µm GaN on SiC 3MI (3-metal interconnect) process. This process includes substrate vias and air bridges with SiC, providing best in class thermal conductivity.

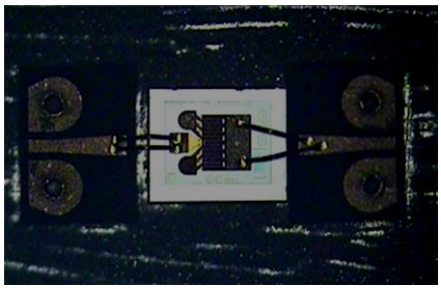


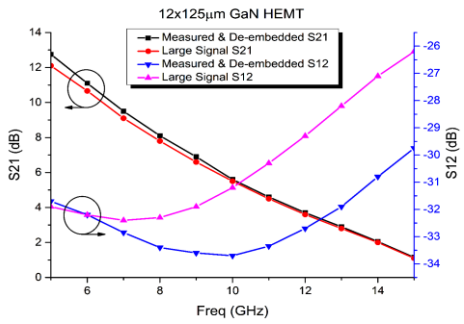
Photo of designed 12 x 125 µm GaN HEMT.

Sample of the design processed with 12 gate fingers and gate-width of 125 µm has been shown in Fig. 1. In order to achieve optimum performance from the device at 6 GHz, different gate to gate spacing values were considered.

Small and Large Signal Measurements:

Various designs have been fabricated by considering different combinations of the number of gate fingers, gate widths and gate to gate spacing for a processed wafer size of 100 mm diameter. Subsequently, the fabricated units were diced and mounted using a high thermal conductivity, electrically conductive epoxy onto aluminium platens. The probe-points were then bonded with the device input and output ports. 12x125 µm transistor provides the best tradeoff between desired output power of 5 W at 6 GHz in terms of the number of gate fingers and gate-width. Measurements for two port s-parameters using GSG probes onto the probe points were carried out using Keysight 8510XF VNA. A model for the probe point with bonds was derived from measured calibration circuits and Advanced Design System (ADS) was used to de-embed the device s-parameters from the measured parameters. Measurements show that drain bond wires spread (DWS) evenly across the drain pad shows slightly higher gain, thus, the technique was utilised for wire bonding as shown in Fig. 1.

Large signal measurements were carried out using Maury Microwave slide screw tuners (type no. 8045P) connected to the input and output on-wafer probes. A high power GSG Picoprobe was employed on the drain side of the device and a Mini-Circuits high power amplifier (ZVE-3W-183+) was used to drive the gate for large signal measurements.

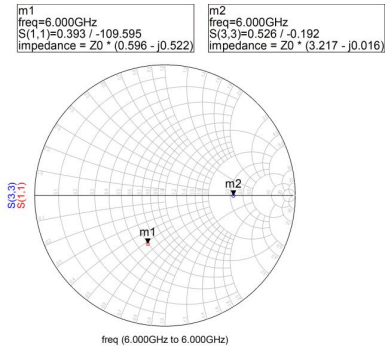


Measured S21 and S12 for 12x125 µm GaN HEMT device.

Key results for de-embedded s-parameters measurements and the large signal model (with reference planes at the probe points wire bonds) have been shown in Fig. 2.

Load Pull Measurements

Load pull measurements have been performed by utilizing slide screw tuners at the device input and output terminals. The screw tuners were adjusted for maximum power output at various drive levels and the tuner positions were noted. Subsequently, the tuners were removed and their impedances were measured using a VNA. Fig. 3 shows the measured impedances to give maximum power output at 6 GHz. The impedances presented have been corrected to show the impedance at device terminals.



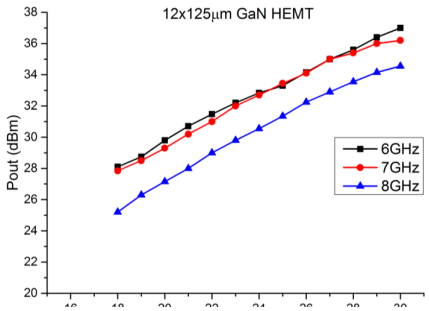
Input (m1) and output (m2) impedance for 12x125 µm GaN HEMT device at 6 GHz.

Due to nature of the testing method, a relatively large number of corrections and de-embedding processes were necessary to derive these results.

The input and output impedances (Fig. 3) for the GaN HEMT were Zin=29.8-j26.1 Ω and Zout=160.85-j0.8 Ω, respectively. These results were utilised to design the respective input and output matching networks for maximum output power performance of the device. The input matching network includes: a shunt stub in series with a very small length of a transmission line, while, the output matching network is a series quarter wavelength transmission line. These networks provide a match to 50 Ω and have been designed on RT Duroid 5870 laminates while considering the dimension limitations of the applicator structure.

Power Measurements

Fig. 4 shows maximum power output of the 12x125 µm device for the given input power at the stated frequencies 6, 7 and 8 GHz.



Pout versus Pin for 12x125 μm GaN HEMT device.

The results shown in Fig. 4 have been measured by adjusting both the input and output screw tuners at each input power level. Degradation in output power at 8 GHz can be observed, this occurs because of the mechanical measurement system where VSWR matching range on the Smith chart is restricted. The PA shows an efficiency of 37 % at 6 GHz, the amount of power lost as heat will be stored within the applicator structure by utilizing a thermal storage metallic block or gel, thermally connected to the amplifier mounting block.

Applicator

In order to demonstrate the efficacy of the GaN HEMT power amplification device, a basic applicator has been designed and simulated. For this application, the PA alongside the matching circuitry will be placed inside the hand piece of the applicator. This will serve a number of purposes: not only will it allow the entire device to be more integrated and compact but also allow the PA to be located closer to the power delivery site. This allows for more power to be present at the tip and thus, a larger amount of energy to be controllably delivered into the tissue to achieve the desired medical effect.

Spider veins or telangiectasia are very common, especially on the lower limbs, and have been reported to exist in 41 % of women over 50. [5]. Many treatments have been used in the past including the use of sclerosing agents, lasers and even low voltage current delivered using a microneedle [6]. Whilst not usually life threatening they present an aesthetic problem causing many patients to opt for cosmetic treatment for their removal. [7] This device intends to use microwaves at 6 GHz to achieve coagulation of these telangiectasia and therefore minimize their appearance. The use of microwaves to achieve localized heating will offer less side effects and complications when compared to other treatment modalities. For these applications, the tip is drawn over the skin following the spider vein meaning the device is only in contact with a single point on the skin for a period of less than one second. For this reason it is important that enough power is delivered into the tissue to achieve coagulation ensuring that the skin is not damaged from thermal effects.

Design of the Applicator

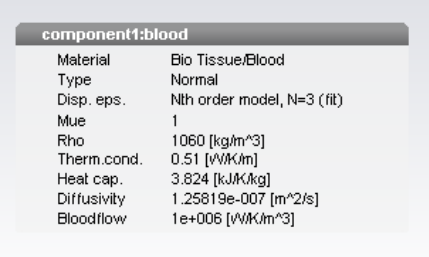
The applicator comprises of an ergonomic hand piece, coaxial transmission line and simple loaded monopole antenna. A draft prototype of the hand piece and applicator has been rendered in Adobe Illustrator Professional and can be seen in Fig. 5.

Computer rendering of a basic prototype hand piece design with coaxial transmission line and antenna visible.

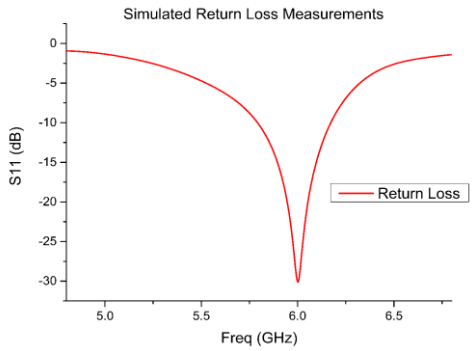
Hand piece dimensions were based on the smallest size required to house the PA and matching circuits, i.e. 50x25x15 mm. Extra width, height and depth were then added to allow the applicator handle to be more ergonomic and easier to use. Due to the efficiency of the PA, heat is generated in the system. For this reason it is necessary to co-locate the PA with a material with high specific heat capacity to act as a heat sink to ensure that the device and handle does not become too hot. Future iterations of the device may consider a more active cooling structure inside the handle that could also be used down the exterior of the antenna to allow for some form of skin cooling effect to minimise the likelihood of thermal damage during treatment. The coaxial line was designed to be approximately 50 mm to fit within the applicator and to minimise transmission losses. The antenna was chosen to be a simple loaded monopole with a chamfered edge to allow for more precise application and allow for delivery of energy directly into the intended tissue. CST Microwave Studio was then used to optimise the length of both the transmission line and also the antenna to provide a good match into tissue at the chosen frequency of 6 GHz.

Simulated Results

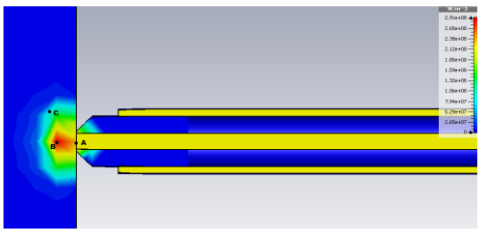
Length of both the coaxial line and the antenna were required to be matched to provide least return loss at 6 GHz. This was achieved by varying the length of the antenna whilst being placed up against a block of material which has the characteristics of human blood as shown in Fig. 6. In order to perform S parameter simulations, tip of the antenna and transmission line is placed against the blood block. The results have been shown in Fig. 7.



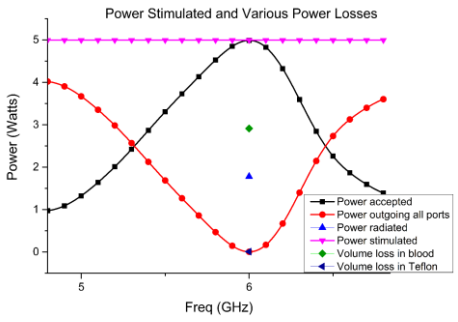
Characteristics of the blood model used in this simulation.



Simulated return loss measurement showing good match at 6 GHz.



Power Density distribution at 6 GHz showing intended site of power delivery.



Power stimulated and various power losses along the cable.

Through variation of the lengths a return loss measurement of -30.095 dB was achieved indicating optimised power delivery from the PA device into the transmission line and antenna. Fig. 9 shows stimulated power at the proximal end of the antenna is 4.99 W, which is an achievable level to be provided by the PA as indicated in Fig. 4. To achieve this output, the PA input may be fed by either an integrated 6 GHz source and driver stage or an external 6 GHz source, fed into the applicator via a coax along with the DC supply cables. Approximately 0.105 W is lost into the air, and 0.08 W is reflected back to the source. This indicated that approximately 2.9 W is delivered into the blood. Future iterations of the device will minimise the radiated power by utilising different antenna designs. The power density distribution at 6 GHz is shown in Fig. 8 and indicates the amount of power delivered at various points around the antenna in Wm^{-3}. It can be seen that at the intended site of delivery the power is highest at approximately 2.838^{8} Wm^{-3}. Assuming a specific heat capacity of approximately 3.824 kJ Kg K and a tissue density of 1060 KGm^{-3} then the amount of energy required to coagulate various volumes of blood can be calculated.

Most telangiectasia vary from approximately 0.5 mm to 1 mm in diameter so for this calculation a cylinder with radius 1 mm and length of 1 mm will be used. Assuming the characteristics already discussed it can be shown that such a volume of blood will have a mass of 3.33^{-6} Kg and will therefore require approximately 0.0127 J of energy to raise its temperature by 1 K. To achieve coagulation, blood needs to be raised to approximately 333 K which is an addition of 23 K ergo an energy input of 0.2929 J is required. The ideal point of application would be Point B in Fig. 8 and this energy input would be reached after 1.02 sec. Values for energy input at the other points can be found in Table 1.

TABLE 1: ENERGY INPUT (JOULES) FOR VARYING NUMBER OF SECONDS.

Activation:	Point A	Point B	Point C
1 Second	0.2341	0.2876	0.05808
2 Second	0.4682	0.5752	0.11616
5 Second	1.1705	1.438	0.2904
10 Second	2.341	2.876	0.5808

Conclusion

The measurements, simulations and analysis presented indicate that the integrated GaN HEMT PA device can provide enough energy in order to achieve blood coagulation, which will be useful in cosmetic applications to minimise the appearance of telangiectasia or spider veins. At the tip of the device, coagulation should be possible within approximately one second and that this coagulation is relatively localised which will minimise the likelihood of damage to any adjacent structures.

Further iterations of this device could make use of different antenna shapes, additional cooling and efficient PA devices. Thus, allowing the delivery of more power into tissue to achieve faster coagulation or the coagulation of larger vessels. The UoM aims at utilising the advancement in GaN HEMT technology to develop high efficiency PAs for applications in electrosurgical devices and therapeutic systems.

Acknowledgment

The authors would like to thank Filtronic Broadband Ltd for their support in the design and fabrication of the transistor device.

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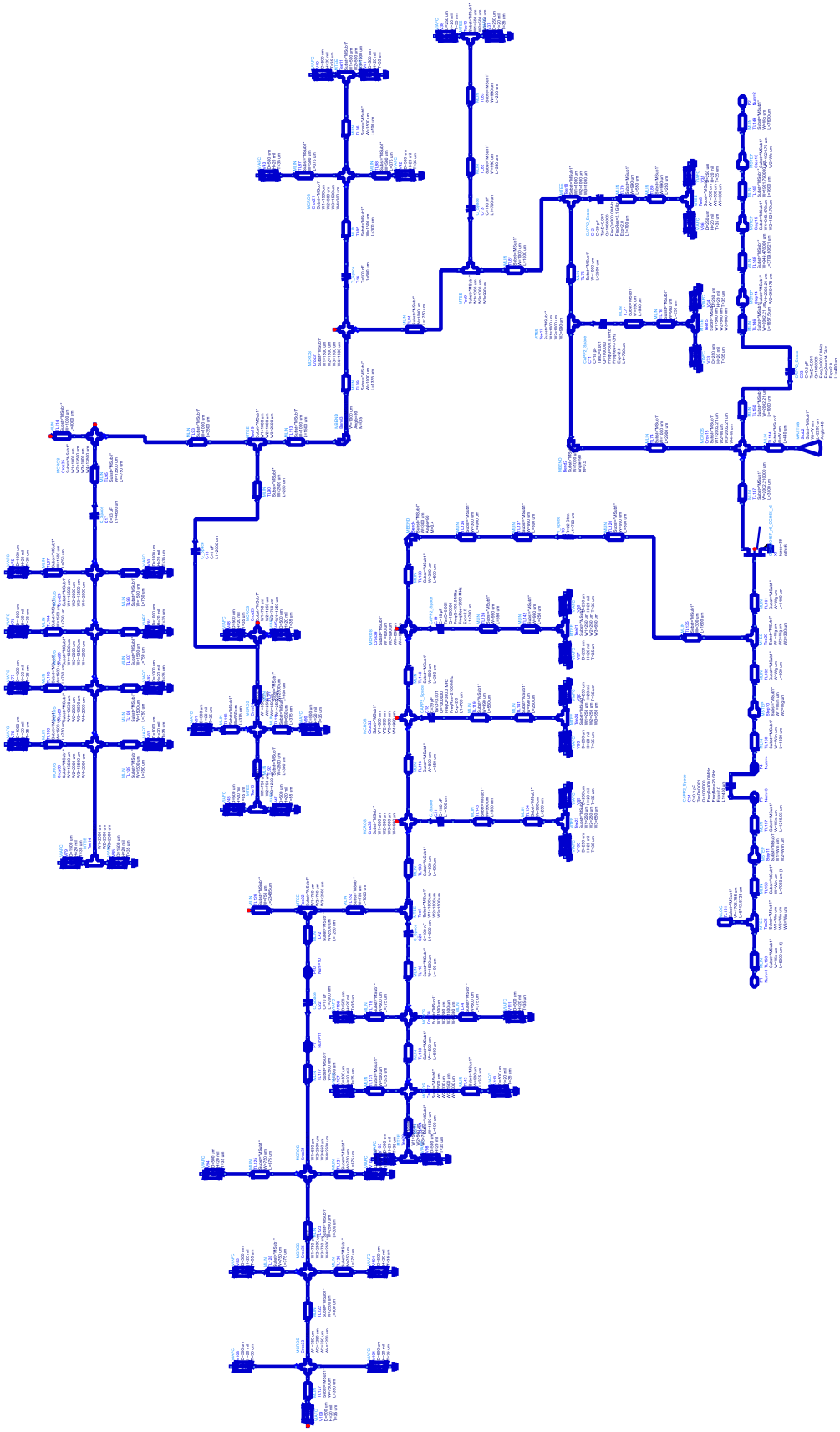
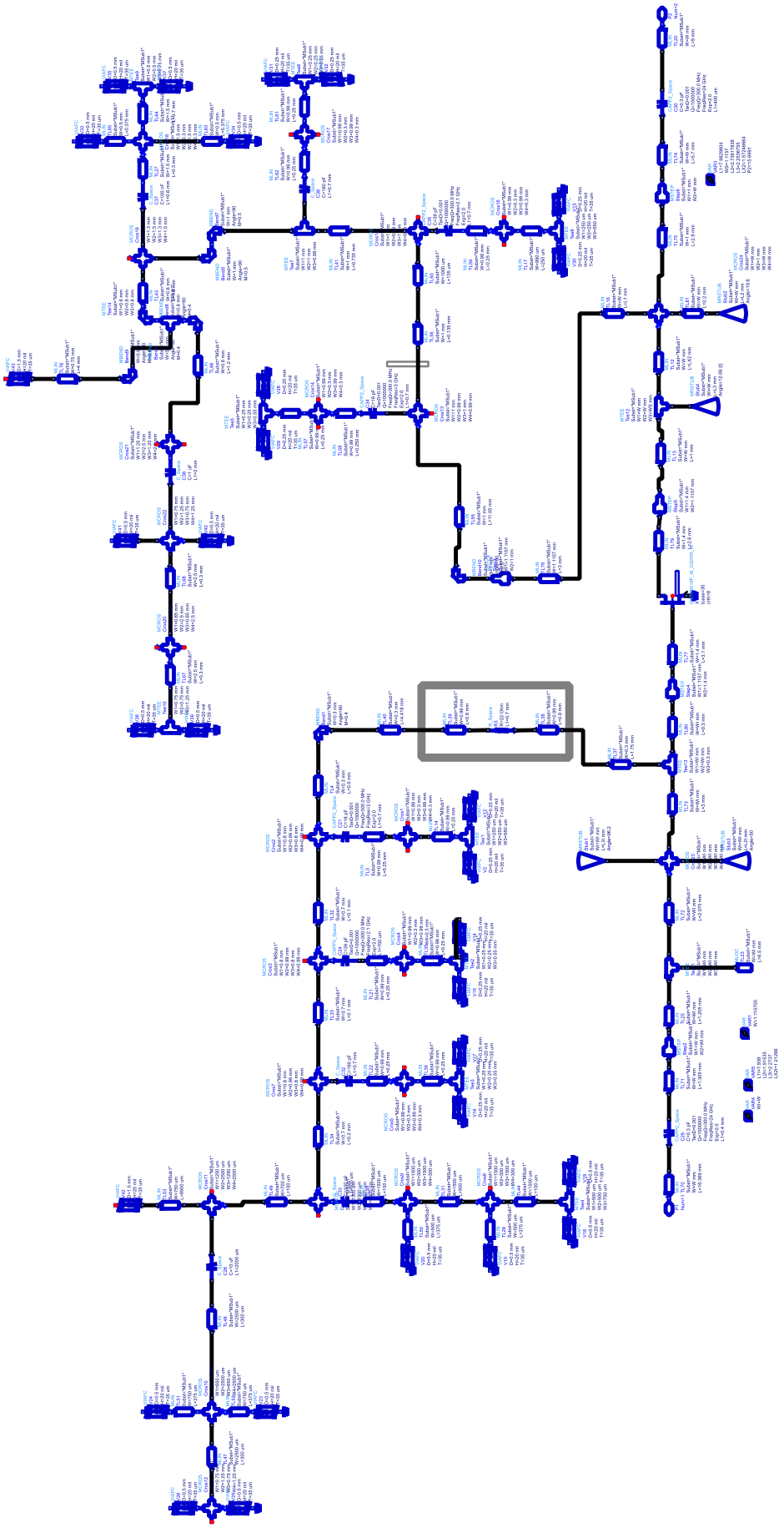
ANNEX B- Schematics of Discrete Power Amplifiers

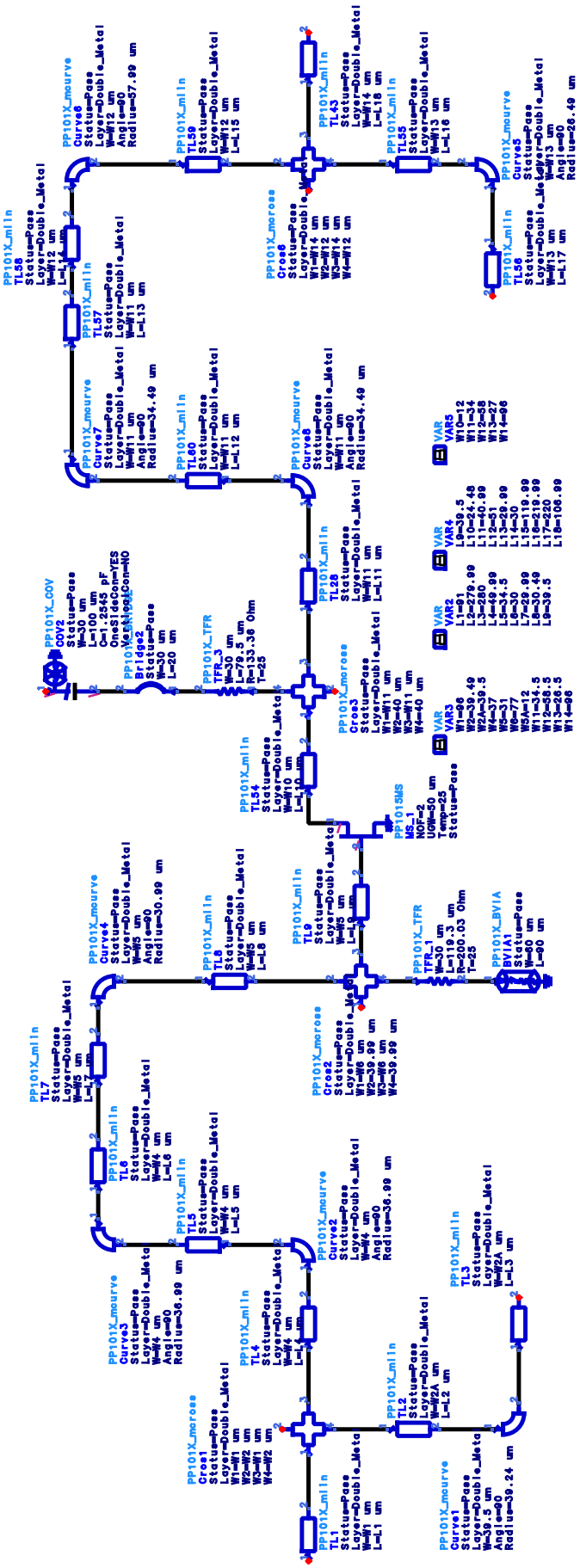
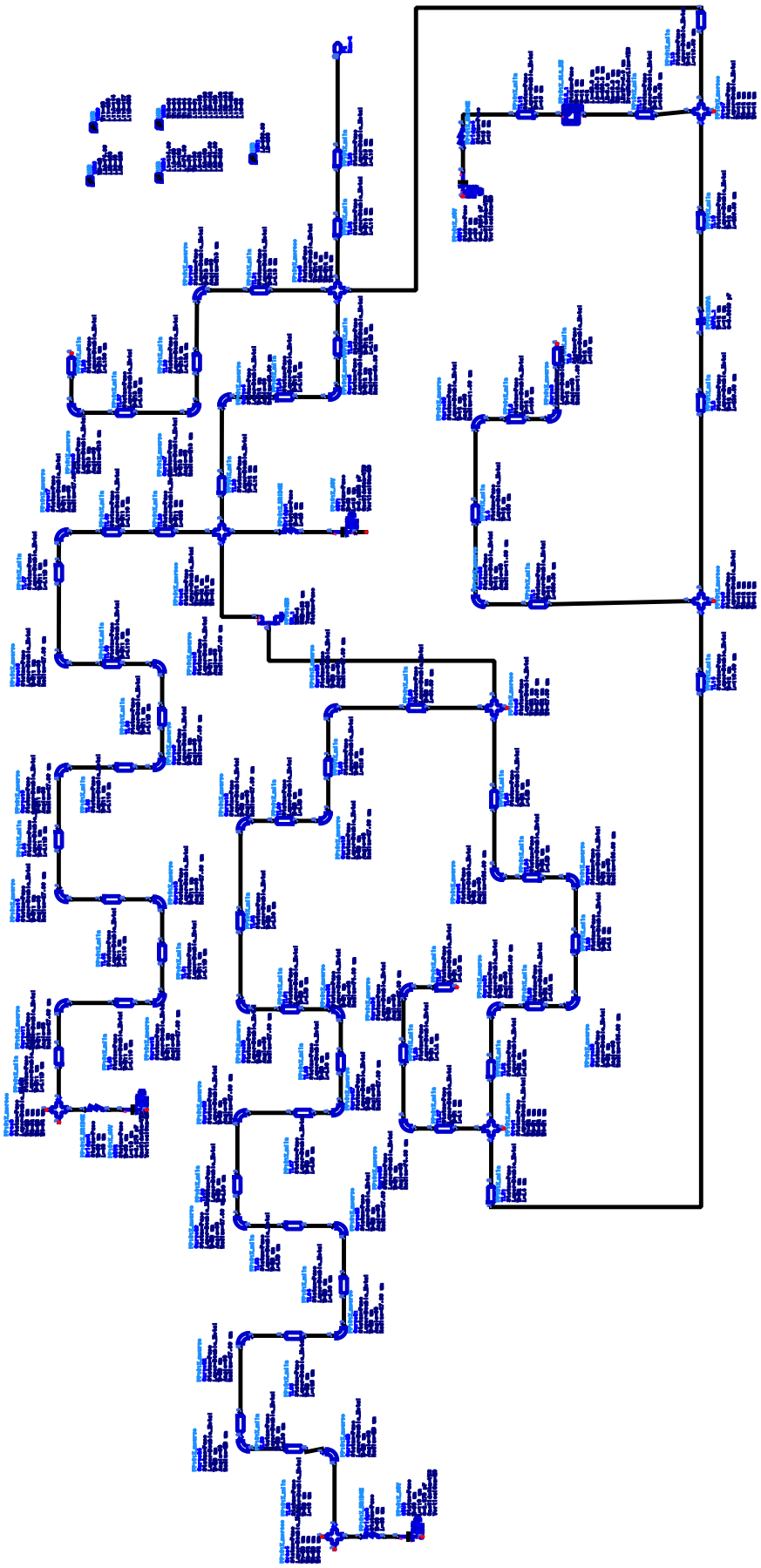
Class AB Amplifier



Class F Amplifier



ANNEX C Circuit Schematics of Class AB MMIC Amplifier



ANNEX D Circuit Schematics of Class E MMIC Oscillator