Low Operating Voltage, Solution-Processed Transistors with High-κ/Self-Assembled Monolayer Dielectrics

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List of Publications

This thesis contains and discusses the results published in the following publications:

- **N. Mohammadian** and L. A. Majewski, "High Capacitance Dielectrics for Low-Voltage Operated OFETs in Organic Field-Effect Transistors," in Integrated Circuits/Microchips, K. H. Yeap and J. Sayago, *IntechOpen.*, 2020, pp. 87-110, doi: 10.5772/intechopen.91772.

- M. Sophocleous, **N. Mohammadian**, L. A. Majewski, J. Georgiou, "Solution-processed, low-voltage tantalum-based memristive switches," *Materials Letters*, vol. 269, 127676, Jun 2020, doi: 10.1016/j.matlet.2020.127676.

- **N. Mohammadian**, B. C. Das and L. A. Majewski, "Low-Voltage IGZO TFTs Using Solution-Deposited OTS-Modified Ta_2O_5 Dielectric,", *IEEE Transactions on Electron Devices*, vol. 67, no. 4, pp. 1625-1631, Apr 2020, doi: 10.1109/TED.2020.2976634.

- S. Sagar, **N. Mohammadian**, S. Park, L. A. Majewski, B. C. Das, "Ultra-thin anodized aluminium dielectric films: the effect of citric acid concentration and low-voltage electronic applications," *Nanotechnology*, vol. 31, 255705, Apr 2020, doi: 10.1088/1361-6528/ab7fd1.

- **N. Mohammadian**, S. Faraji, S. Sagar, B.C. Das, M.L. Turner, L.A. Majewski, "One-Volt, Solution-Processed Organic Transistors with Self-Assembled Monolayer-Ta_2O_5 Gate Dielectrics," *Materials*, vol. 12, 2563 , Aug 2019, doi: 10.3390/ma12162563.

Additional publications not discussed in this thesis:

- M. Seck, **N. Mohammadian**, A. K. Diallo, S. Faraji, M. Saadi, M. Erouel, et al., "Low-voltage organic transistors with water-processed gum Arabic dielectric," *Synthetic Metals*, vol. 267, 116447, Sep 2020, doi: 10.1016/j.synthmet.2020.116447.

- M. Seck, **N. Mohammadian**, A. K. Diallo, S. Faraji, M. Erouel, N. Bouguila, L. A. Majewski, "Organic FETs using biodegradable almond gum as gate dielectric: A promising way towards green electronics," *Organic Electronics*, vol. 83, 105735, Aug 2020, doi: 10.1016/j.orgel.2020.105735.

List of Conference Presentations

- **N. Mohammadian**, L. A. Majewski, "Solution-processed electronics: Low-voltage Organic Transistors (OFETs)," *IOP PGS Conference: Printing for the future 2020*, Jul 2020, online.

- **N. Mohammadian**, L. A. Majewski, "Low-power High-performance a-IGZO Thin-Film Transistor using OTS Modified Ta_2O_5 as the gate dielectric," *innoLAE (innovations in Large-Area Electronics) 2020*, Jan 2020, Cambridge.

- **N. Mohammadian**, S. Faraji, L. A. Majewski, "Solution-processed polymer transistor using Tantalum Pentoxide dielectric," *IOP PGS Conference: Printing for the future 2019*, Apr 2019, Hertfordshire.

- **N. Mohammadian**, S. Faraji, M. L. Turner, L. A. Majewski, "Ultra-low voltage organic field-effect transistors (OFETs)," *innoLAE (innovations in Large-Area Electronics) 2019*, Jan 2019, Cambridge.

- **N. Mohammadian**, S. Faraji, L. A. Majewski, "High-κ Anodic Dielectrics for Low-voltage Applications," *The PGR Poster Conference 2018*, Nov 2018, Manchester.

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Abbreviations

AFM	Atomic force microscopy
Al_2O_3	Aluminium oxide
ALD	Atomic layer deposition
AMLCD	Active-matrix liquid crystal display
AMOLED	Active-matrix organic light-emitting diode
AOS	Amorphous oxide semiconductor
a-Si:H	Amorphous hydrogenated silicon
BBL	Benzo-bisimidazobenzo-phenanthroline
BCC	Body centre cubic
BJT	Bipolar junction transistor
BST	Barium strontium titanate
CB	Conduction band
CBE	Conduction-band edge
CBM	Conduction band minimum
CF	Conductive filament
CMOS	Complementary metal-oxide-semiconductor
CP	Conducting polymer
CuPc	Copper phthalocyanine
CVD	Chemical vapour deposition
DF	Dissipation factor
DOS	Density of states
DPPDTT	Poly(3,6-di(2-thien-5-yl)-2,5-di (2-octyldodecyl)-pyrrolo [3,4-c] pyrrole-1,4-dione) thieno [3,2-b] thiophene)
DRAM	Dynamic random-access memory
DRS	Dielectric relaxation spectroscopy
ECM	Electrochemical metallisation memory
EDL	Electric double layer
EMA	Effective medium approximation

eME	Extended mobility edge
ESR	Equivalent series resistance
F8T2	Poly(9,9-dioctylfluorene-alt-bithiophene)
FCC	Face centred cubic
FET	Field-effect transistor
FPD	Flat panel display
GB	Grain boundary
GPC	Grows per cycle
HfO_2	Hafnium oxide
HMDS	Hexamethyldisilane
HOMO	Highest occupied molecular orbital
HRS	High-resistance state
IGZO	Indium-gallium-zinc oxide
In_2O_3	Indium oxide
IPA	Isopropyl alcohol
LCD	Liquid crystal display
LRS	Low-resistance state
LTPS	Low-temperature polycrystalline silicon
LUMO	Lowest unoccupied molecular orbital
MDMO-PPV	Poly(2-methoxy-5-(3′,7′-dimethyloctyloxy)-p-phenylene vinylene)
MF	Magnetic field
MIM	Metal-insulator-metal
MOS	Metal-oxide-semiconductor
MTR	Multiple-trapping and release
NNH	Nearest-neighbour hopping
ODTS	*n*-octadecyltrichlorosilane
OLED	Organic light emitting diodes
OPV	Organic photovoltaics
OSC	Organic semiconductor

OTFT	Organic thin-film transistor
OTS	Octyltrichlorosilane
P(VDF-TrFE)	Vinylidene fluoride-trifluoroethylene
P3AT	Poly(3-alkyl-thiophene)
P3HT	Poly(3-hexylthiophene)
PCBM	6,6-phenyl-C61-butyric acid methyl ester
PEALD	Plasma enhanced atomic layer deposition
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PMMA	Polymethyl methacrylate
PVD	Physical vapour deposition
RFID	Radio-frequency identification
SAM	Self-assembled monolayer
SiO_2	Silicon oxide
SnO_2	Tin oxide
Ta_2O_5	Tantalum oxide
TFT	Thin-film transistor
THF	Tetrahydrofuran
TLC	Trap-limited conduction
TT	Thieno[3,2-b] thiophene
VB	Valence band
VBM	Valence band maximum
VCM	Valence change memory
V_O	Oxygen vacancy
VRH	Variable range hopping
XPS	X-ray photoelectron spectroscopy
ZrO_2	Zirconium oxide
ZnO	Zinc oxide

Abstract

Solution-processed thin-film transistors (TFTs) have a high potential to be the key components of future portable, battery-powered devices and circuits. TFTs can be realised in different form factors from standalone, discrete, low-cost sensors to flexible, large-area electronics. However, most of the recently demonstrated solution-processed TFTs typically operate at or above 5 V, which is still too high for many applications where operating voltage and power consumption are the main concerns. One approach to decrease the operating voltage of TFTs is to lower their threshold voltage (V_{th}) and subthreshold swing (SS) which can be fulfilled by increasing gate dielectric capacitance and improving the dielectric/semiconductor interface. The high capacitance dielectric can be achieved by utilising high dielectric constant (high-κ) materials, thinning the gate dielectric layer, or doing both simultaneously. Tantalum pentoxide (Ta_2O_5) is a highly promising, high-κ metal oxide dielectric (κ ~ 26) which is used in capacitors, transistors and memory devices. Recently, it has been shown that employing thick Ta_2O_5 films (d > 100 nm) as a gate dielectric does not only improve the characteristics of TFTs but significantly lowers their operating voltage. However, due to its relatively medium bandgap (4.4 eV), Ta_2O_5-based TFTs suffer from high leakage currents, particularly when Ta_2O_5 thickness is reduced below 20 nanometres.

Typically, Ta_2O_5 is deposited by atomic layer deposition (ALD) or RF/DC magnetron sputtering. These methods are time-consuming and increase the cost of device fabrication due to the need for high-vacuum conditions. In comparison, anodic oxidation (so-called anodisation) is a material deposition technique which is a simple, cost-efficient and straightforward method to grow high-quality metal oxide layers on the surface of metallic substrates in ambient conditions. In this thesis, ultra-thin (d ~ 7 nm), anodic Ta_2O_5 modified with *n*-octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) has been used to realise ultra-low voltage operation of p-channel DPP-based organic TFTs (OTFTs) and n-channel a-IGZO-based metal oxide TFTs (MOTFTs). Moreover, it is shown that OTS SAM reduces the gate leakage current and improves the TFT dielectric/semiconductor interface.

First, the morphology and dielectric properties of the anodised Ta_2O_5 films with and without OTS SAM treatment have been analysed. Several anodisation voltages were utilised to optimise the thickness of Ta_2O_5 for each type of TFTs to guarantee their optimal operation. The results show that the poly(3,6-di(2-thien-5-yl)-2,5-di (2-octyldodecyl)-pyrrolo[3,4-c] pyrrole-1,4-dione) thieno [3,2-b] thiophene)-polymethyl methacrylate (DPPDTT-PMMA) TFTs gated with OTS-modified tantalum pentoxide anodised at 3 V (d ~ 7 nm) exhibit the best performance. The optimised devices operate at 1 V with saturation field-effect mobility larger than 0.2 $cm^2\ V^{-1}\ s^{-1}$, threshold voltage -0.55 V, subthreshold swing 120 mV/dec, and current on/off ratio in excess of 5×10^3. As a result, the demonstrated DPPDTT-PMMA TFTs display a promising performance for applications in ultra-low voltage, organic electronics. On the other hand, it is shown that the best performing capacitors and a-IGZO TFTs are realised with 10 V anodised (22 ± 2 nm), OTS-treated Ta_2O_5 dielectric. The fabricated Ta_2O_5/OTS capacitors show good stability in the 100 Hz to 100 kHz and capacitance density in excess of 400 nF/cm^2. The fabricated TFTs display relatively high field-effect mobilities (2.3 $cm^2\ V^{-1}\ s^{-1}$), threshold voltages around 0.4 V, subthreshold swings below 90 mV/dec, and high current on/off ratios well in excess of 10^5. It is envisaged that this approach is a promising alternative to fabricate ultra-low voltage, inexpensive TFTs and TFT-arrays for low-cost sensors and low-end, disposable electronics.

Declaration

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

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Chapter 1: Introduction

1.1 A brief history of transistors

Nowadays, field-effect transistors (FETs) play a crucial role in the modern electronics industry. They are typically operated as a signal amplifier [1] or an electronic switch [2] in analog and digital circuits, respectively. The development of silicon-based transistors, particularly metal-oxide-semiconductor (MOS) FETs for complementary metal-oxide-semiconductor integrated circuits (CMOS ICs) (i.e., microprocessors), has taken the electronics industry to an entirely new level and significantly changed each and every aspect of our day-to-day lives, which cannot be imagined without their valuable role anymore.

With respect to other types of transistors, e.g., bipolar junction transistors (BJTs), MOSFETs have several advantages, such as small dimensions, high performance along with low power consumption and dissipation, and high input impedance. This makes them the ideal devices for employing in CMOS ICs. Therefore, most of the electronic circuits are now manufactured using this class of transistors [3]. Nonetheless, the high performance of MOSFETs usually comes with the high cost and high-temperature processing [4], which is incompatible with the growing demand for low-cost, low-temperature, large-area processing of emerging flexible and stretchable electronics [5]. Responding to these demands requires firstly intensive research and development on realising compatible materials and active devices discussed in this thesis to achieve the end goal of fabricating large-area flexible and stretchable circuits.

Thin-film transistors (TFTs), which are well known for their important role in modern flat panel displays (FPDs), belong to the family of FET devices [6]. TFTs are made by stacking thin films that consist of three fundamental materials, namely, a semiconductor, a dielectric, and a conductor. Even though TFTs and MOSFETs have been developed simultaneously, MOSFETs have dominated the majority of microelectronics research interests and industrial production due to their much better performance. However, the

demand for low-cost, large-area flat panel displays (FPDs) fuelled research on finding a viable substitution for crystalline and polycrystalline silicon that typically require high-temperature processing.

In 1979, significantly cheaper amorphous hydrogenated silicon (a-Si:H) was developed with few constraints on substrate size, material, and topology and was subsequently introduced to thin-film transistors (TFTs) as the active layer, which resulted in an increased interest in TFTs [7]. Since then, the use of a-Si:H TFTs has gradually grown, and eventually, this type of TFTs has started to dominate the whole liquid crystal display (LCD) industry. Nowadays, a-Si:H TFTs along with indium-gallium-zinc oxide (IGZO) and poly-Si TFTs are the backbone of both active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting diode (AMOLED) display technologies.

Despite the crucial role of amorphous hydrogenated silicon (a-Si:H) TFTs in display technologies, a-Si:H TFTs suffer from low mobility (typically ≤ 1 cm^2 V^{-1} s^{-1}), as well as instability under electrical bias stress and illumination [8]. Although Si is the most common material used in electronics due to its advantages such as abundance, low-cost manufacturing, ease of doping, and high charge carrier mobility, the focus of TFT research has been being shifted to new families of semiconductor materials that can offer more beneficial properties, for example, transparency [9], flexibility [10] and recyclability [11] along with high carrier transport, low-cost solution-based processability, and mechanical stress tolerance, for novel applications.

In addition, there are many applications for which high-performance (i.e., high switching speed, high output current) electronic switches are not needed, such as discrete sensors [12], simple displays [13], as well as basic radio-frequency identification (RFID) tags and smart cards [14]. These applications are typically realised in various shapes and sizes, and thus alternative electronic materials and device manufacturing techniques that are compatible with these applications are being developed. From a marketing point of view, the global

market size for flexible hybrid circuits is forecasted to go beyond $3 billion in 2030 [15]. Also, it is expected that almost 5 billion flexible hybrid electronic circuits will be produced by 2030. From the most recent trends in material research, it appears that organic and metal oxide semiconductors are the two most promising alternatives to silicon for low-cost, large-area electronic applications.

In 1986, Tsumura *et al.* reported a special type of TFTs that used an organic semiconductor (OSC) as the active layer, so-called organic thin-film transistors (OTFTs). The demonstrated devices used electrochemically polymerised polythiophene, which belongs to the family of conducting (i.e., conjugated) polymers (CPs), as the active layer and were operated at 50 V [16]. Accordingly, it has been shown that the thin-film transistor design is the structure of choice for low conductivity materials such as OSCs. As a result, the TFT design was utilised to realise a wide range of field-effect transistors (FETs) using organic semiconductors [17]. Since then, the performance of organic semiconductors has continuously improved, and nowadays, OTFTs can compete with or even surpass a-Si:H TFTs in a broad range of electronic applications [18].

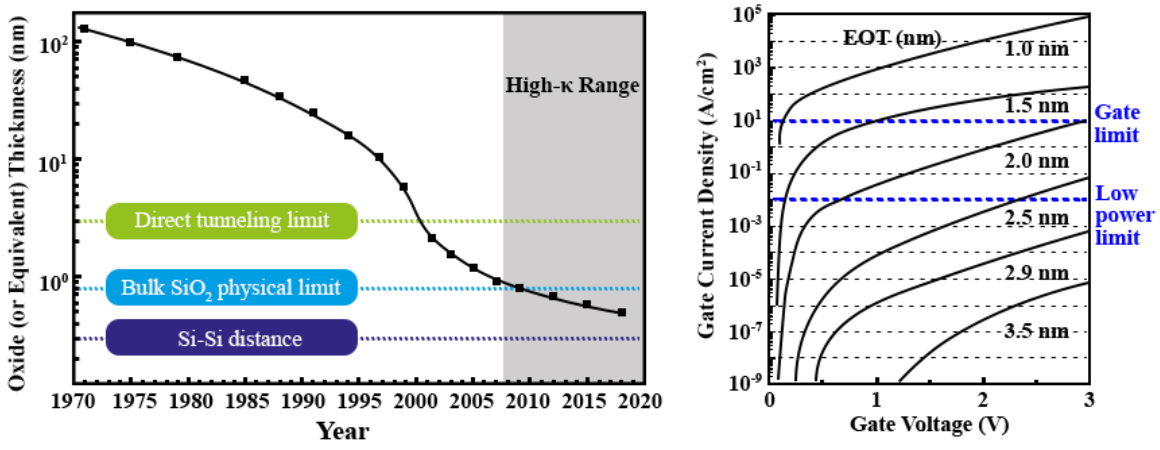
Moreover, TFTs which employs a metal oxide semiconductor (monocrystalline ZnO) as the active layer were introduced in the mid-1960s. Subsequently, FETs and TFTs using other binary oxide semiconductors (i.e., In_2O_3 and SnO_2) were reported [19][20]. However, oxide TFTs disappeared from the literature for a long time until the 1990s when it turned out that polycrystalline ZnO (poly-ZnO) could be fabricated on large-area substrates at temperatures ≤ 300 °C. In the 2000s, ZnO TFTs started to attract increased attention once more with the expectation that they could substitute a-Si:H TFTs in FPDs. However, the initial poly-ZnO TFTs had several issues to be addressed, namely, relatively low mobility (≤ 3 cm^2 V^{-1} s^{-1}), electrical performance instability and normally-on characteristics. Additionally, they suffer from nonuniformity properties and challenging fabrication processes similar to poly-Si TFTs due to the presence of grain boundaries (GBs) [21], as well as high background electron

concentration and low chemical durability against acidic etchants and reducing atmospheres compared to a-Si:H TFTs [22].

Crystalline indium-gallium-zinc oxide (IGZO) TFTs were first reported in 2003 [23]. Subsequently, amorphous IGZO (a-IGZO) TFTs were demonstrated in 2004. Since then, a-IGZO TFTs have shown promising characteristics in terms of switching speed (greater than a-Si:H), resolution, large-area processability and inexpensive manufacturing, which are on a par with a-Si:H TFTs [24]. As such, oxide semiconductors, specifically in their amorphous state, have started to make a remarkable growth in the display industry. At present, they are even challenging silicon in many other conventional applications and are researched for a large number of novel and disruptive applications (e.g., flexible electronics) which can benefit from their unique features such as high optical transparency, high carrier mobility, and even solution processability. However, the key issue for utilising the oxide semiconductors on plastic substrates such as polyimide (PI), polyethylene naphthalate (PEN), and polyethylene terephthalate (PET) required for flexible applications is their processing temperature which should be kept well below 200º C.

Low-voltage TFTs can operate with much lower gate-source voltages (V_{GS}) ($\leq$ 5 V) and, consequently, have potentially lower power consumption. The demand for low-voltage TFTs is continuously growing as they have been increasingly being used in energy-efficient and (lithium-ion) battery-powered devices. One main parameter of TFTs, which affects their operation voltage, is the thickness of the gate dielectric. It turns out that reducing the thickness of the gate dielectric can decrease the operating voltage, and thus, this method is traditionally used as a method of reducing the operating voltage. SiO_2, as a superior conventional gate dielectric, is continuously being thinned to realise TFTs with lower operating voltages. However, thinning SiO_2 to the range of 4–5 nm increases the leakage current density (J_{leak}) exponentially due to direct tunnelling that considerably deteriorates the performance and reliability of the device (J_{leak} > 1 A cm^{-2} at 1 V gate bias, Fig. 1.1) [25].

Besides, high-temperature processing (900 ~ 1200 °C) of defect-free SiO_2 is incompatible with emerging novel applications such as stretchable, flexible and large-area electronics typically fabricated on plastic substrates which cannot tolerate higher temperatures than ~ 200 °C [25].



(a) (b)

Fig. 1.1. (a) The semiconductor industry roadmap for gate dielectric thickness scaling [26] and (b) leakage current density (J_{leak}) versus voltage for various SiO_2 dielectric thicknesses [27].

To date, apart from thinning the gate dielectric, there are other methods to reduce the operating voltage of TFTs, such as using high dielectric constant (κ > ~10) materials. Replacing the SiO_2 with the high-κ materials (e.g., HfO_2) as the gate dielectric was introduced to overcome the SiO_2 limitations, enable further miniaturisation of the device dimensions and reduce the operating voltage.

Moreover, it appears that although portable batteries have been remarkably improved over decades in terms of technology, capacity, and lifetime, their improvement has not been as fast as the development of semiconductor technologies [28]. This unbalanced improvement is also reflected in phones' battery where in some cases, they could be lasting for several days without requiring to be charged in the last decade, but most of them can barely last a full day now. This issue can be justified by two main reasons. On the one hand, increasing the energy density reached a stage where it cannot be further achievable with the current materials. On the other hand, changing battery materials requires intensive research and

development, which is much slower than what has been achieved over time. Therefore, the rapid development of low threshold voltage (V_{th}) TFTs, which guarantees lower power consumption, is highly desirable [29]. However, before such low-power devices can be realised, a significant reduction in the operating voltage of the transistors is required. Unfortunately, it is still extremely challenging for both organic and metal oxide TFTs to achieve high performance and operating voltages ≤ 1 V at the same time [30][31][32].

As a result, different research groups conducted extensive research to develop low threshold voltage (V_{th}) TFTs using high-κ materials and gradually reduced the operating voltage that was around 20 V in early devices to 10–5 V or even 3 V in the current devices. However, it is thought that TFTs operating at 1 V or below are now needed to realise ultra-low-voltage transistors and circuits. Despite the quick improvement in power consumption and reducing the operating voltage of inorganic TFTs [33], it was only in 1999 when Dimitrakopoulos *et al.* firstly reported organic TFTs. Those OTFTs employed an 82 nm thick sol-gel barium strontium titanate (BST) layer with a dielectric constant (κ) of 15 as the gate dielectric and p-type pentacene as the active layer. Using BST in those OTFTs reduced the operating voltage, which exceeded 50 V at the time to 5 V [34].

Since then, extensive research has been conducted to find and employ a variety of high-κ materials in OTFTs in both academia and industry. In particular, Ta_2O_5, due to its high dielectric constant (~ 26), was in the spotlight to be used in OTFTs. In 2002, Bartic *et al.* reported tantalum oxide (Ta_2O_5) deposited by e-beam as a gate dielectric material for low-voltage poly(3-hexylthiophene) (P3HT) OTFTs [35]. Those TFTs employed a 100 nm thick Ta_2O_5 film and could operate around −3 V. In 2004, Sakai *et al.* reported low-voltage OTFTs using p-type pentacene as the semiconductor layer and a 130 nm thick Ta_2O_5 film deposited by radio-frequency (RF) magnetron sputtering as a gate dielectric. Similar to the previously reported OTFTs, those transistors also operated at about −3 V [36]. In 2005, Ueno *et al.* employed a thick Ta_2O_5 dielectric layer (d = 200 nm) in the p-type pentacene and n-type C_{60}

OTFTs [37]. Although p-type OTFTs in comparison with n-type had relatively better field-effect mobility, the fabricated OTFTs operated at 10 V which made them unsuitable for low-voltage applications. In 2008, Zhou *et al.* proposed low-voltage n-type OTFTs based on a 200 nm Ta_2O_5 grown by anodisation [38]. As can be seen from the literature, the use of Ta_2O_5 has been limited to relatively thick Ta_2O_5 films (≥ 100 nm) which effectively resulted in 3 V OTFTs. However, this operating voltage is still too high for certain applications where the low power consumption of devices is paramount.

1.2 Motivation, challenges and research aim

Nowadays, TFTs are situated in most electronic devices and typically consume a majority of the power budget of their circuits. Thus, designing TFTs which can operate at low voltages as possible and simultaneously have the highest performance is highly desirable [30][31][32]. This consideration becomes more significant when it comes to portable, battery-powered devices where power consumption is one of the main concerns.

Even though the necessity of the low operating voltage is dependent on different criteria and can differ from application to application, the operating voltage should be as low as 1 V. For instance, some medical purposes require to sense and detect biological species in an aqueous media since it is necessary to avoid electrolytic hydrolysis of water caused by high ionic conduction in an analyte at higher voltages and stabilise operation in aqueous solutions. Although the operating voltage of TFTs has generally been reduced over the past decades, it has reached the range of 3–5 V where the further reduction is challenging and not trivial due to intrinsic properties of the conventional gate dielectrics (e.g., SiO_2).

Moreover, low-voltage TFTs are preferred to a typical TFT operating at lower voltages or, in particular, at sub-threshold voltages due to several reasons. Firstly, operating a TFT in a sub-threshold voltage is not trivial and needs several aspects to be considered. For example, most transistor modelling has focused on the saturation region (i.e., “on” state), not the sub-threshold region. Secondly, operating a TFT at sub-threshold increases significantly its

sensitivity as small changes in gate voltage causes exponentially changes in the drain current. In terms of contact resistance, it also suffers from high contact resistance comparing to that of in the above-threshold region. Additionally, the ratio of "on" to "off" drain current is orders of magnitude smaller in the subthreshold regime. Therefore, to achieve the goal of this project, TFTs which natively have the ability to operate at low voltages are preferred.

For totally different applications where downscaling of the channel in order to situate more transistors in ICs is not the case, increasing the κ/d ratio is leading to reduction of the operating voltage by increasing the gate dielectric capacitance. This can happen by substituting SiO_2 with a high-κ material (e.g., Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, etc.) and thinning the dielectric thickness which can increase the induced charges with lower leakage current and allows to decrease threshold voltage (V_{th}) and subthreshold swing (SS), two key features of TFTs without compromising the value of the drain current (I_D).

However, controlling and mitigating the gate leakage current in nanoscale dielectrics is challenging and increases the necessity of having dielectric materials with larger bandgap; therefore, selecting an appropriate material with the highest bandgap and dielectric constant is essential. Unfortunately, a trade-off should be considered as materials with a higher dielectric constant have a lower bandgap [25].

Among all of high-κ materials, Ta_2O_5 shows promising characteristics leading to be employed in a variety of electronic devices such as metal-oxide-metal (MOM) capacitors and diodes, TFTs, and memory devices. However, due to relatively medium bandgap (4.4 eV) in comparison with other gate dielectrics, the minimum thickness of Ta_2O_5 films used in TFTs are typically thick and above 100 nm. These thick dielectrics guarantee the optimum performance in the application of TFTs but impede the devices to operate at low voltages ($\leq$ 3 V). Despite the numerous advantages of Ta_2O_5 dielectric for different types of devices such as high dielectric constant ($\kappa \approx 26$), high transparency, high melting point (1785 °C),

and showing good thermal and chemical stability, it has been reported that to realise ultra-low-voltage TFTs (≤ 1 V), the thickness of Ta_2O_5 dielectric requires to decrease sufficiently to below 50 nm [5]. This thickness reduction can be really challenging as it requires several optimisation steps, careful considerations, and possible trade-offs. The development of ultrathin high-κ dielectric (≤ ~ 20 nm) leading to the decrease of the threshold voltage (V_{th}) and subthreshold swing (SS) which allow operating voltage to be lowered with the same drain current (I_D) in organic and inorganic TFTs.

Moreover, although bandgap and dielectric constant are two critical parameters for selecting a dielectric, they are not only parameters as other criteria such as moisture absorption, crystal structure and surface roughness have to be considered, as well. Besides, although the gate dielectric can be deposited by a variety of well-established methods, low-temperature processing techniques should be considered first as they help to reduce manufacturing costs and are compatible with large-area plastic electronics. An effective strategy to realise room temperature processing of high-κ metal oxide materials enabling low-voltage TFTs is to use the solution processing techniques like anodic oxidation (anodisation). Anodisation can provide room temperature oxidation and deliver a smooth film with a precise thickness that can be used in various applications such as memory devices, transistors, and diodes. Therefore, anodisation as a high-quality, inexpensive deposition technique can benefit manufacturing procedures with minimum changes and decrease the production cost of ICs.

Semiconductors play an essential role in active devices, and therefore, extensive research to find new semiconductor materials is in progress which can open new horizons for next solid-state electronics. Table 1.1 compares the key characteristics of two well-established semiconductors, namely, a-Si:H and poly-Si with organic and metal oxide semiconductors. Overall, metal oxide and organic semiconductors show superior functionalities, especially for novel applications such as transparent, flexible, large-area electronics due to room

temperature and solution-based processability, and large-area uniformity. In this study, two promising semiconductor materials, organic and metal oxide were used to realise one-volt TFTs.

Channel material	a-Si:H	Poly-Si (e.g., LTPS)	Organic	Metal oxide (e.g., IGZO)
Manufacturing cost	Low	High	Low	Low
Microstructure	Amorphous	Polycrystalline	Mainly Polycrystalline	Amorphous
Stability	Poor	Good	Poor	Superior to a-Si
Uniformity	Good	Poor	Good	Good
Yield	High	Low	High	High
Max. mobility ($cm^2 V^{-1} s^{-1}$)	≈1	≈100	≈10	≈100
Device type	n-type	n- and p-type	Mainly p-type	Mainly n-type
Process temperature (°C)	150–350	250–550	RT–250	RT–400
Large-area scalability	High	*Low	High	High
Solution manufacturing	No	No	Yes	Yes

* In practice, the large-area scalability of poly-Si is not low, and it is possible to make large-area poly-Si displays, but due to poly-Si fabrication costs, it is not financially viable.

Table 1.1. Key characteristics of different types of semiconductors [27][26].

Herein, the primary aim to conduct this research was to find and develop promising high-κ dielectrics which can not only deliver TFTs with the operating voltages at or below 1 V and reasonable leakage current density ($J_{leak} \leq 1$ nA/cm^2) but also is compatible with both organic and inorganic semiconductors on both rigid and flexible substrates. This aim was fulfilled by the development of ultrathin Ta_2O_5 dielectric for p-type organic and n-type oxide TFTs which operate at or below 1 V. The ultrathin tantalum pentoxide films have been investigated from scratch in order to be used as a gate dielectric in TFTs, which has shown promising gate dielectric characteristics especially when it is passivated with a self-assembled monolayer (SAM) like OTS forming a hybrid high-κ/low-κ dielectric.

This thesis reports research results concerning pristine and OTS-treated high-κ Ta_2O_5 as the gate dielectric for n-type a-IGZO-based TFTs and p-type organic diketopyrrolopyrrole (DPP)-Based OTFTs. The key aspects of the study focus on the understanding of theoretical concepts, fabrication, characterisation and potential applications of the fabricated devices.

Theoretical concepts of this research are based on previous works conducted in the literature. Fabrication is based on our group findings and experiences, which aim to be as reproducible and straightforward as possible along with maximum optimisation. Characterisation is one of the most vital parts of the research. Therefore, in this research, scientific matters have been considered to achieve precise, reliable results. The developed dielectric was then used in other devices such as memory devices and possibly can be employed in MIM diodes to realise the quite full range of active devices. Moreover, due to the nature of realised TFTs (n-type and p-type), they can pave the way towards low-voltage CMOS-based circuits, which are highly desirable for future and emerging applications.

1.3 Organisation of Manuscript

Chapter 2 of this thesis is a literature review that consists of the theory and operation mechanism of TFTs, theory of dielectric and its different types and high-κ dielectric, which can be utilised in low-voltage, high-performance thin-film transistors by the room temperature solution-processed technique. The review provided herein is expected to be a useful resource for assessing the development of high-κ metal oxide dielectric theory and referencing the tantalum oxide film as a promising gate dielectric. Although the whole literature view may be looks saturated by information at first glance, it is suggested that the reader peruse sections of interest.

The purpose of Chapter 3 is to describe the methodology and experimental work. It is mainly focused on anodisation, preparation and processing procedures of high-κ metal oxides and growth of Ta_2O_5, SAMs surface modification and fabrication of a-IGZO TFTs and OTFTs, which can operate as low as 1 V and utilising a low-cost low-temperature technique providing a high-quality pores-free gate dielectric with excellent characteristics.

Chapter 4 comprises complete results and discussions and categorised into two subsections of characterisation of Ta_2O_5/OTS dielectric layers and evaluation of fabricated

TFTs and OTFTs using the corresponding dielectrics. In each section, the proposed dielectric layers used in the fabrication of transistors are separately presented and analysed.

Chapter 5 demonstrates the application of anodised tantalum oxide films for realising low-cost solution-processed memristive devices. The results show a high potential of these devices in resistive random-access memory (ReRAM) applications and neuromorphic computing.

Chapter 6 summarises the conclusions for this thesis and provides potential future work and detailed recommendation on the proposed anodised tantalum oxide films.

Chapter 2: Literature review

2.1 Overview of Thin-Film Transistors (TFTs)

The concept of thin-film transistors (TFTs) was first reported by Weimer in 1962 [33]. TFTs are a class of the now large family of field-effect transistors (FETs). A typical TFT is comprised of three terminals (gate, source, and drain) and made by stacking thin films of various electronic materials such as a semiconductor, a dielectric, and a conductor. Depending on their fabrication process and purpose, some TFTs possess additional passive layers (e.g., substrate planarization layer, semiconductor passivation layer, and device encapsulation layers, etc.). The structure of TFTs has been shown to be compatible with low conductivity semiconductor materials and is now abundantly utilised in a-Si:H TFTs and a-Si:H TFT-based circuits [39]. As shown in Fig. 2.1 (a), in bottom-gate top-contact TFTs the semiconductor layer is situated between the drain and source electrodes and the dielectric layer is inserted between the semiconductor and a transversal electrode (gate). TFTs employ an electric field to modulate the current obtained by the accumulated charge carriers at the dielectric/semiconductor interface and control the current flow between the source and drain with the applied voltage bias to the gate electrode [40]. As such, a typical TFT operates similarly to the metal-oxide-semiconductor field-effect transistor (MOSFET). Even though TFTs and MOSFETs have been developed simultaneously, MOSFETs have dominated most microelectronics research interests and industrial production due to their much higher performance. However, the high MOSFET performance usually comes with the high manufacturing cost and high-temperature processing (greater than 1000 °C) [41] which is incompatible with the increasing demand for low-cost, low-temperature, large-area processing of flexible, stretchable and electronics. Other dissimilarities between TFTs and MOSFETs, as shown in Fig. 2.1, include structural and material differences [42]. For example, TFTs usually use an insulator as the substrate (e.g., glass or flexible films such as

PEN or PI), which is not involved in the device operation while MOSFETs are fabricated on silicon wafers which serve as both the substrate and the semiconductor layer. As a result, higher performance can be expected from MOSFETs as the electrons flow in either a single crystalline or polycrystalline material. Also, p-n junctions are present at the drain/source contacts while there are no such junctions in TFTs. Noteworthily, both types of transistors operate in a fundamentally different way: MOSFETs operate in the inversion mode, whereas typical TFTs operate in the accumulation (enhancement) mode [43][44].

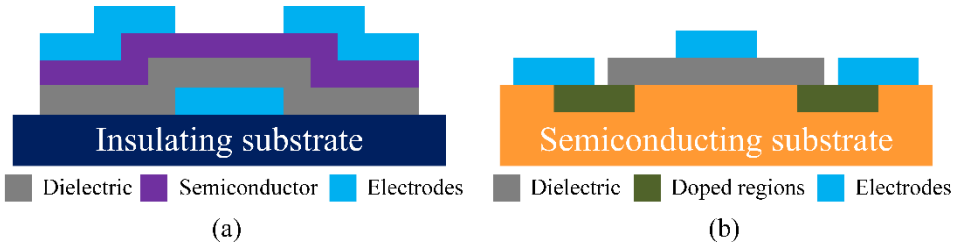


Fig. 2.1. Typical structures of (a) a bottom-gate top-contact TFT and (b) a MOSFET. Doped regions refer to the MOSFET drain and source regions.

2.1.1 TFT architectures

Thin-film transistors can be fabricated on a variety of rigid and flexible substrates, namely Si/SiO_2 wafers, glass, PI, PEN, PET, and other types of flexible films. Depending on the position of the gate electrode and where each layer is deposited, TFTs are classified into four different architecture, namely, coplanar bottom-gate, staggered bottom-gate, coplanar top gate and staggered top-gate, as shown in Fig. 2.2. Staggered and coplanar configurations refer to the drain/source and gate contacts position with respect to the semiconductor layer. Although all abovementioned structures are used in the fabrication of TFTs, each of them shows a better performance in a particular application, and/or due to the fabrication limitations such as processing temperature, one is more desirable than the other [7][45]. For instance, the coplanar top-gate structure is routinely used in polycrystalline silicon (poly-Si) TFTs in flat panel displays due to the fact that the crystallisation process of poly-Si generally needs high temperature which possibly degrades the properties of other materials and their interfaces and thus it is favoured to be deposited without any layers beneath it [46]. In this structure, the drain/source electrodes are aligned with the channel region, which results in

the minimisation of the parasitic capacitance that reduces image flicker and sticking [47]. Also, top-gate structures typically have higher mobility than their bottom-gate counterparts [48]. The coplanar bottom-gate structure is generally used in gas sensor applications (i.e., e-sensing). In addition, an insulator is often deposited on top of the layers, which results in effective mechanical and chemical protection as some dielectrics and semiconductors, such as CdSe, quite easily reacts with moisture and oxygen in the air. This protective layer supports devices from successive processes such as integration of TFTs with liquid crystal cells [49]. This device structure directly affects the device performance in terms of the contact resistance, parasitic capacitance, charge carrier mobility, sensing capability, etc., and it is crucial to meticulously determine the device architecture regarding the intended use of the device.

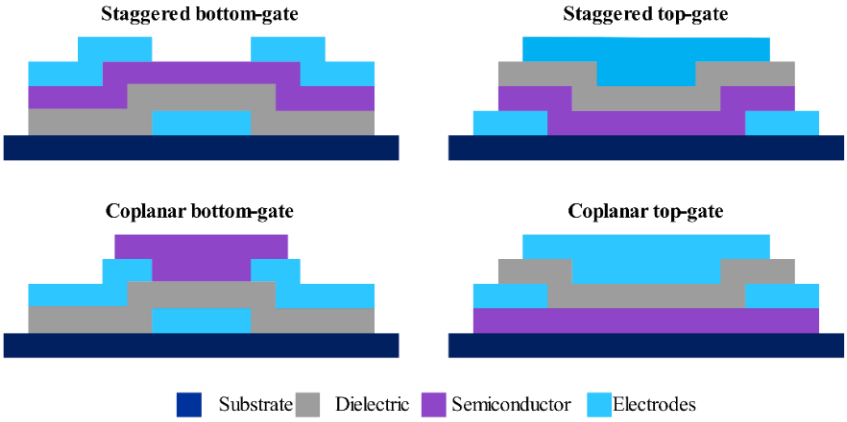


Fig. 2.2. The most common structures of TFTs.

2.1.2 TFT operation

TFTs can be operated in both depletion or accumulation mode, determined by their threshold voltage (V_{th}) polarity (i.e., negative or positive). Although the accumulation mode is typically preferred as the gate-source voltage (V_{GS}) is not required to turn the device off (to reach its off-state) and higher values of transconductance (g_m) are usually obtained for this mode [33], depletion mode devices are not completely abandoned and are still used for some specific applications such as loads for nMOS logic circuitry [40]. Considering an n-channel (or p-channel) TFT operation in the accumulation mode. When a positive voltage (negative

voltage) bias is applied to the gate electrode, electrons (holes) start to accumulate at the dielectric/semiconductor interface, which forms a current path (so-called channel) between the drain and source contacts. Once the drain-source voltage (V_{DS}) bias is applied, the current starts to flow from the source to the drain electrode. As illustrated in Fig 2.3, depending on the condition of the channel, TFTs can be considered as operating in a set of different modes, namely cut-off, linear, and saturation. If the applied gate-source voltage (V_{GS}) is below a certain value, i.e., smaller than V_{th} in an n-channel TFT, then it is not possible to accumulate enough charges (i.e., electrons) to open the channel. Therefore, no current can flow from the source to the drain within the channel which is known as the cut-off region. On the other hand, if $V_{GS} > V_{th}$, two scenarios can be considered. Firstly, if V_{DS} is lower than $V_{GS} - V_{th}$, I_{DS} complies with the Ohm's law and the resistance of the channel (R_C) is proportional to V_{DS} and inversely proportional to I_{DS}. This mode is called the linear or ohmic regime. Secondly, once drain-source voltage (V_{DS}) reaches a value around $V_{GS} - V_{th}$ (i.e., $|V_{DS}| \cong |V_{GS} - V_{th}|$), the channel is pinched off, and subsequently, no matter how much V_{DS} increases, the amount of the drain-source current (I_{DS}) flowing in the channel is almost constant (saturated) regardless of the value of $V_{DS,}$ and the TFT works in the saturation regime.

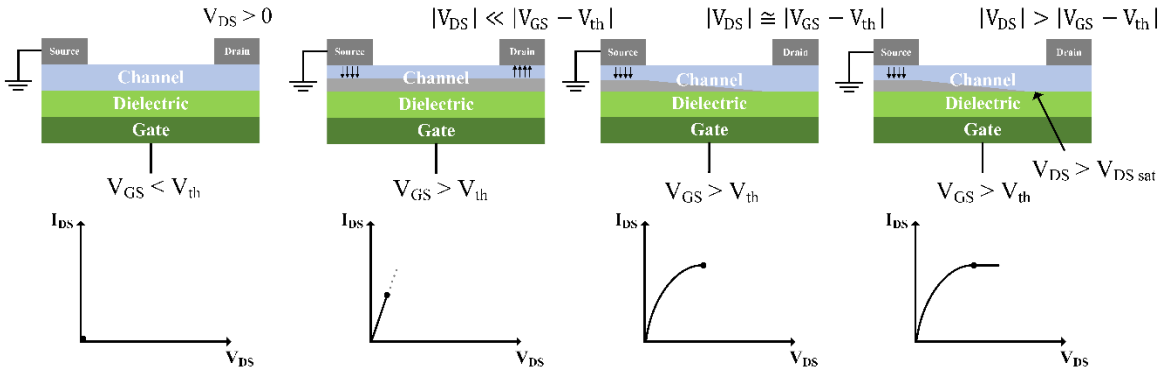


Fig. 2.3. Schematics of an ideal n-channel TFT operation (a) cut-off, (b) linear regime, (c) pinch-off, and (d) saturation regime (the same structure used in the fabrication of low-voltage TFTs in this thesis).

The density of accumulated charge carriers (Q_C) (i.e., electrons or holes) in the channel is calculated as follows. Considering the channel voltage (V_C) as a function of x which can be

from 0 to L as shown in Fig. 2.4, at x = 0, V_C is equal to source voltage (V_S) and correspondingly at x = L, $V_C = V_D$. Therefore, Q_C can be obtained by:

$$Q_C(x) = -C_G[V_{GS} - V_{CS} - V_{th}], \quad \text{(Eq. 2.1)}$$

where, C_G is the gate dielectric capacitance density formed by the metal-insulator-semiconductor structure within the TFT.

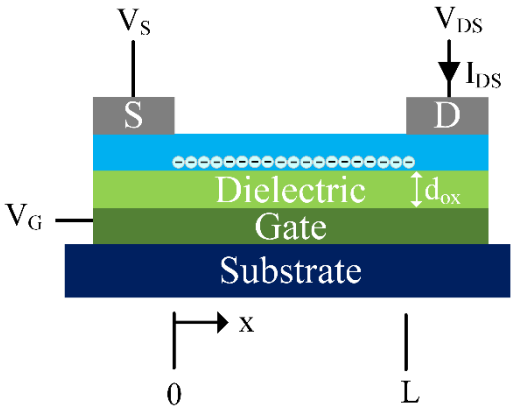


Fig. 2.4. The schematic of a TFT, when $V_{DS} \neq 0$, the channel voltage V_c is a function of x and d_{ox} is the dielectric thickness.

Accordingly, I_{DS} which is flowing from the high-voltage terminal to the low-voltage terminal, can be calculated as follows [50]:

$$J = Q_C \mu E \quad \text{(Eq. 2.2)}$$

$$\begin{aligned} I_{DS} &= W.Q_C(x)\mu E = W.Q_C(x).v \\ &= WC_G(V_{GS} - V_{CS} - V_{th})\mu \frac{dV_{CS}}{dx} \end{aligned} \quad \text{(Eq. 2.3)}$$

$$\int_0^L I_{DS}dx = WC_G\mu \int_0^{V_{DS}} (V_{GS} - V_{CS} - V_{th})dV_{CS} \quad \text{(Eq. 2.4)}$$

$$I_{DS}L = WC_G\mu \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) V_{DS} \quad \text{(Eq. 2.5)}$$

$$I_{DS} = \frac{W}{L} C_G\mu \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) V_{DS}, \quad \text{(Eq. 2.6)}$$

where v is the carrier velocity, E the applied electric field, J drain current density, μ charge carrier mobility in the channel, W channel width, and L the channel length of the device. In

the linear region where V_{DS} is very small (i.e., $V_{DS} << V_{GS} - V_{th}$), the $V_{DS}/2$ term is negligible and thus $I_{DS} \propto V_{DS}$, in other words, the transistor acts as a resistor with the value of R_C. In the saturation region, $V_{DS} \equiv V_{DS,\,sat}$ is equal or larger than $V_{GS} - V_{th}$, and I_{DS} is independent of V_{DS}. Therefore, the equation is simplified to:

$$I_{DS} = \frac{W}{2L} C_G \mu_{sat} (V_{GS} - V_{th})^2, \qquad \text{(Eq. 2.7)}$$

where μ_{sat} is the charge carrier mobility in the saturation regime.

The most important performance parameters of a TFT are extracted from the transfer (I_{DS}-V_{GS} for a fixed V_{DS}) and output (I_{DS}-V_{DS} with different steps of V_{GS}) characteristics in compliance with the gradual channel approximation. This approximation is only valid when the channel length is minimum ten times larger than the dielectric thickness ($L \geq 10 \times d_{ox}$), and the TFT is not in the saturation region, yet it cannot be used for short-channel devices [51]. Typical output and transfer characteristics of a TFT are illustrated in Fig. 2.5 (a) and (b), respectively.

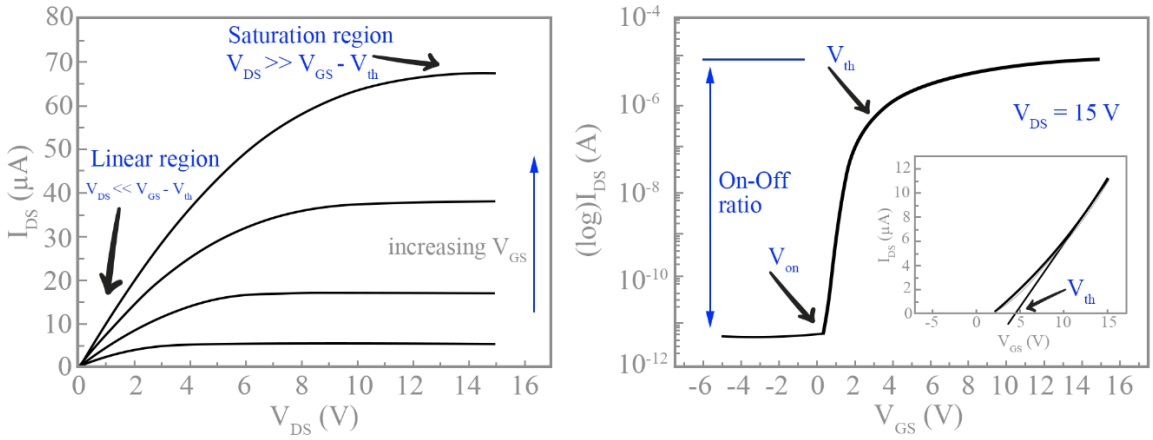


Fig. 2.5. The I-V characteristics of a typical TFT: (a) output curve and (b) transfer curve.

In general, the essential TFT parameters are as follows (cf. Fig. 2.5 (a) and (b)):

- Turn-on voltage (V_{ON} [V]) is the value of V_{GS} at which I_{DS} starts to increase exponentially (i.e., at this voltage, only the minimum required charges in the vicinity of dielectric/semiconductor interface are accumulated and therefore, the channel shows a high resistance)

- Threshold voltage (V_{th} [V]) is the minimum V_{GS} at which the number of the accumulated charge carriers at the dielectric/semiconductor interface is sufficient to create a conduction path (channel) between the drain and source electrodes (at this voltage, the channel starts showing a low resistance). The lower V_{th}, the lower the operating voltage of a TFT.
- Subthreshold swing (SS [mV/dec]) is the parameter which describes the necessary V_{GS} to increase I_{DS} by one order of magnitude (decade) in the subthreshold region (i.e., $V_{ON} < V_{GS} < V_{th}$, obtained by the inverse of the maximum slope of the transfer curve). Typically, SS << 1 V/dec, between 0.1 and 0.30 V/dec, as the small value of SS as possible is highly desirable because it leads to lower device power consumption and higher device switching speed [52]. It is usually determined by the two following expressions:

  Measuring from I-V characteristics of the TFT,

$$SS = \left(\frac{d\log(I_D)}{dV_{GS}}\middle|\max\right)^{-1}, \qquad \text{(Eq. 2.8)}$$

  or calculating from a MOSFET physical model that is also being used for TFTs,

$$SS = \frac{k_b T}{q\log(e)}\left(1 + \frac{C_{sc}}{C_G}\right), \qquad \text{(Eq. 2.9)}$$

  where k_b is the Boltzmann's constant, T is the temperature in Kelvin, q is the electron charge, C_G is the gate dielectric capacitance per unit area, and C_{sc} is the semiconductor effective capacitance which directly depends on the high trapping energy (so-called deep traps) states in both bulk and the interface and is calculated by [53][54]:

$$C_{sc} = q\sqrt{\varepsilon_s D_{bulk}} + q^2 D_{it}, \qquad \text{(Eq. 2.10)}$$

  where ε_s is the permittivity of the semiconductor, D_{bulk} and D_{it} are bulk and interface trap densities, respectively. For an ideal trap-free TFT, C_{sc} is zero. Therefore, the theoretical limit for the SS is obtained by $SS_{ideal} = k_b T/q\log(e)$

which is equal to 59.6 mV/dec at 300 K. For an actual transistor, SS is usually larger than its theoretical limit at the room temperature. This deviation shows the quality of the dielectric/semiconductor interface.

- On-off current ratio ($I_{ON/OFF}$) defines a ratio of the measured maximum to minimum drain-source current (I_{DS}). High "on" and low "off" currents in a TFT are highly desirable.
- The charge carrier mobility (μ) defines how fast charge carriers (electrons and holes) can move through a given semiconductor. Even though it is considered as an intrinsic characteristic, the measured mobility in a TFT is considered to depend on several extrinsic factors. Normally, the higher the carrier mobility is, the better performance the TFT has. Also, higher mobility enables a TFT to be employed in more applications. Although the carrier mobility of organic semiconductors was lower than their inorganic counterparts for a long period of time, it has substantially improved recently from 0.00001 to over 20 $cm^2 V^{-1} s^{-1}$. The charge carriers mobility has a significant effect on the efficiency and the switching frequency of transistors [55]. The mobility in inorganic TFTs can also be affected by several scattering mechanisms, including ionised impurities, grain boundaries (GBs), lattice vibrations, and other structural defects [56]. Moreover, some scattering mechanisms particularly occurred in TFTs as the current flows in a narrow region close to dielectric/semiconductor interface, such as Coulomb scattering, interface states or surface roughness [46]. The mobility of carriers can be extracted using different methodologies, namely, linear mobility (μ_{lin}) and saturation mobility (μ_{sat}). The linear mobility and saturation mobilities are usually determined by calculating the transconductance (i.e., $g_m = dI_{DS}/dV_{GS}$) with low and high V_{DS}. In the linear regime (low $V_{DS,}$ $V_{DS} << V_{GS} - V_{th}$):

$$\mu_{lin} = \frac{g_m}{C_G \frac{W}{L} V_{DS}} \quad \text{(Eq. 2.11)}$$

and in the saturation regime (high $V_{DS,}$ $V_{DS} > V_{GS} - V_{th}$):

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)^2}{\frac{1}{2} C_G \frac{W}{L}} \quad \text{(Eq. 2.12)}$$

Each technique has its own advantages and disadvantages. For instance, although μ_{lin} contains the important effect of V_{GS} and requires the value of V_{th} and is more sensitive to the contact resistance (low V_{DS}) [46], μ_{sat} is insensitive to the contact resistance. Furthermore, despite the fact that only a peak value of μ_{lin} or μ_{sat} is typically reported in the literature, extrapolating mobility equations as a function of V_{GS} provides more comprehensive information about the device physics.

- From the value of SS alone, the interfacial trap density (D_{it}) cannot be obtained as the Eq. 2.7 does not permit the discrete calculation of D_{it} and D_{bulk} because both parameters contribute to the C_{sc} which is related to the total trap density. However, it can be used to find the maximum density of interface traps by assuming that $D_{bulk} = 0$.

$$SS = \frac{k_b T}{q \log(e)} \left[1 + \frac{q}{C_G} (q D_{it})\right] = \frac{kT}{q \log(e)} \left[1 + \frac{q^2 N_{ss}}{C_G}\right] \quad \text{(Eq. 2.13)}$$

By arranging SS, D_{it} is obtained by [57]:

$$D_{it}^{max} = \left[\frac{SS \log(e)}{kT/q} - 1\right] \frac{C_G}{q^2}, \quad \text{(Eq. 2.14)}$$

where C_G is the gate capacitance density, q the electron charge, k the Boltzmann's constant, T the temperature in Kelvin, and SS the subthreshold swing (SS).

2.1.3 Low-voltage TFTs

As mentioned in the previous section, I_{DS} is described in the linear and saturation regimes by Eq. 2.6 and 2.7, respectively. In the ideal case, the drain-source current (I_{DS}) should be maximum while the gate bias voltage is as low as possible. However, this only can be achieved when both the threshold voltage (V_{th}) and subthreshold swing (SS) are sufficiently low enabling a TFT to be operated at a low voltage and maximum performance [58]. Referring back to Eq. 2.7 and assuming that the mobility is constant, the only parameters that can be changed to compensate the reduction of I_{DS} at low V_{GS} are the gate dielectric capacitance (C_G), and the channel width (W) and length (L). However, W and L depend on device geometry. Therefore, in order to accumulate the same number of charges within the channel of a TFT with fixed W and L, and maintain high I_{DS}, it is essential to increase the gate dielectric capacitance (C_G). One may argue that increasing the gate capacitance may deteriorate the transistor's switching speed. Indeed, the maximum switching speed of a TFT is usually defined by its cut-off frequency f_c, as shown in Eq. 2.15 [59]:

$$f_c = \frac{g_m}{2\pi C_G} = \frac{\mu_{sat}(V_{GS} - V_{th})}{2\pi L^2}, \qquad \text{(Eq. 2.15)}$$

where μ_{sat} is the charge carrier mobility in the saturation regime, L the channel length, V_{GS} the gate-source voltage, V_{th} the threshold voltage, and f_c is quantified by the g_m/C_G ratio.

As can be seen from Eq. 2.15, increasing the gate capacitance decreases the cut-off frequency. However, for specific applications such as OTFT-based sensors which generally sense analogue quantities such as analyte concentration or pressure, the high operating frequency is not required as analogue quantities do not change rapidly [60]. Thus, they are typically not designed to be used in high switching speed applications because they are not meant to substitute silicon-based high-performance transistors. Therefore, delivering the highest possible I_{DS} at the lowest possible V_{GS} is more critical than the high operating frequency in these applications. Nonetheless, some applications require a high switching speed, such as ring oscillators (ROs) which are widely used in CMOS phase-lock loops

(PLLs). Thus, some methods such as thinning the channel layer thickness [61] and engineering of the dielectric/semiconductor interface in TFTs [62] have been investigated to have the best of both worlds, low-voltage TFTs with an improved f_c. However, depending on the intended applications, a trade-off situation should always be considered. The detailed study of the influence of the gate dielectric properties on the performance of TFTs is discussed meticulously in the dielectric section of this chapter.

2.2 Semiconductor Materials for TFTs

2.2.1 Amorphous oxide semiconductors

Metal oxide semiconductors are a family of active materials which show high promising properties for the next generation of electronic devices. As mentioned before, a-Si:H and poly-Si (where higher performance required leading to higher manufacturing cost) previously dominated the area of flat panel displays (FPDs), oxide semiconductors are now gradually taking the market of FPDs as a potential replacement these materials due to their several advantages such as low-cost low-temperature processing, full transparency, high performance, and electrically stable properties. Despite the fact that the performance of the first indium-gallium-zinc-oxide (IGZO) TFTs which appeared in 2004 was much lower than the single crystalline silicon transistors (i.e., $\mu_{sat} \approx 9$ cm^2 V^{-1} s^{-1}, $V_{th} \approx 1$–2 V, $I_{ON/OFF}$ ratio $\approx 10^3$), the optimisation of IGZO continuously progressed and eventually opened the door for the realisation of high-performance thin-film transistors as promising devices for future low-voltage, portable electronics. At present, state-of-the-art oxide TFTs display field-effect mobilities beyond 20 cm^2 V^{-1} s^{-1} [63], threshold voltages near 0 V, current on-off ratios $\geq 10^8$, and subthreshold swings (SS) about 0.2 V/dec [64].

2.2.2 Comparison of oxide and organic semiconductors with the conventional technologies of TFTs

As discussed before, a-Si:H is the most broadly used semiconductor in the TFT circuitry of TVs. It also along with polycrystalline silicon (poly-Si), organic and oxide materials now

form the core of all commercially available TFT technologies. Table 2.1 compares the most important characteristics of different semiconductor materials, i.e., a-Si:H, poly-Si, amorphous oxides and organic semiconductors, used in TFTs. Although a-Si:H has a major advantage over other types of semiconductors, such as having a well-established fabrication process, oxide TFTs have the potential to substitute a-Si:H swiftly as most of the available industrial implementation tools for a-Si:H can be used for oxide semiconductors, as well. For instance, sputtering systems are typically used to deposit LCD top electrodes can also be used for depositing oxide semiconductors. Additionally, Si-based materials typically require toxic gases such as silane, phosphine or diborane to be synthesised, while oxide semiconductors can be processed using more environmentally friendly and less hazardous processes as oxygen and argon gases are only needed [64].

* - Not suitable ** - Moderate *** - Suitable	Inorganic semiconductors			Organic semiconductors
	a-Si:H	poly-Si	Amorphous oxides	
Maturity/infrastructures	***	**	*→***	*/**
Large-area deposition	***	**	***	***
Processing temperature	**	*/**	**/***	***
Cost	***	*	**/***	**/***
Transparency	*	*	***	**
Electrical performance	*/**	***	***	*/**
Electrical stability	*	**	**/***	*
Environmental stability	*	**	***	*/**

Table 2.1. Comparison between the most relevant semiconductor material technologies for TFTs.

According to Table 2.1., organic and oxide semiconductors are challenging Poly-Si semiconductor in three main aspects: processing temperature, large-area deposition and transparency. However, poly-Si shows excellent electrical performance and has been shown that it virtually supports the large-area deposition. Unfortunately, its high fabrication cost impedes it to be used in large display panels. On the contrary, amorphous organic and oxide semiconductors are relatively cheap and due to their disordered structure highly compatible with large-area applications. Low-temperature processing also enables the fabrication of devices on inexpensive glass or plastic substrates which is highly desirable. Although thanks to the low-temperature polycrystalline silicon (LTPS) technology, the processing

temperature of poly-Si is significantly decreased over time from ~ 900 °C to below 600 °C, it is still much higher than organic and oxide semiconductors, which can be deposited even at room temperature. Moreover, based on a report published by Displaybank, the market for transparent displays is upscaling and predicted a sharp growth to create $87.2 bn by 2025 [65]. However, due to the lack of transparency in poly-Si, this semiconductor cannot be part of that growing market. In contrast, some organic semiconductors are shown to be reasonably transparent in the visible range [66] and also, amorphous oxide semiconductors (AOSs) can offer fully transparent devices and displays. Another benefit of transparent displays is their improved brightness levels as the aperture ratio (the ratio of effective light-transmitting area and entire area) is higher in these displays than conventional displays [67].

In terms of electrical performance, carrier mobility (μ) is one of the most important parameters of TFTs, as the higher the mobility, the more applications the TFTs can be used for. Poly-Si TFTs have the highest carrier mobility ($\mu \approx 102$ $cm^2 V^{-1} s^{-1}$) in conventional fabrication, and up to around 900 $cm^2 V^{-1} s^{-1}$ is observed in innovative material growth techniques such as quasi-single-crystal large-grain material [68]. Even so, LTPS TFTs shows much higher μ (200 $cm^2 V^{-1} s^{-1}$) compared with other technologies, organic and a-Si:H TFTs with a small μ (≤ 1 $cm^2 V^{-1} s^{-1}$) and oxide TFTs with intermediate μ which typically exhibits higher μ than organic and a-Si:H still need more improvement and development to reach poly-Si. However, the high carrier mobility is not the only feature every display should have; in fact, this feature should be achieved along with a low leakage current and a low threshold voltage (V_{th}). For instance, although poly-Si shows the highest μ, it exhibits a large leakage current originated by the trap-states on the grain boundaries (GBs) [69]. This high leakage current of poly-Si in comparison with other technologies deteriorates the on-off ratio ($I_{ON/OFF}$) and thus limits its applications for large-area high-resolution displays. Nonetheless, it is noteworthy to mention that the high leakage current of poly-Si displays has been solved recently with the (low-temperature polycrystalline oxide) LTPO architecture developed by

Apple [70]. To have optimum electrical performance, μ should not be the only parameter of a TFT that is meticulously considered. In terms of electrical stability, although oxide TFTs still require further investigation for long-term stability, the primary findings demonstrate that oxide TFTs are vulnerable to constant current and bias stress which causes a shift in V_{th}. Nonetheless, this variation is smaller than a-Si:H TFTs and generally, oxide TFTs exhibit more stability than other technologies. Furthermore, the properties of semiconductors can be affected by exposure to visible light. This phenomenon mostly occurs in semiconductors with a relatively small bandgap (≤ 2 eV). For example, due to the large bandgap (E_G) of oxide semiconductors (E_G ~ 3–4 eV), it has been shown that their properties are not as sensitive as in the case of a-Si:H (E_G ~ 1.7 eV) and Si (E_G ~ 1.14 eV) which are commonly capped with light shields in TFT applications as their properties affected to visible light. Organic materials are sensitive to water and oxygen, and therefore, they are typically passivated to mitigate the environmental effects. This is also not the case for oxide semiconductors as the interaction of oxygen with oxide semiconductors can be beneficial [64].

Overall, although organic and oxide semiconductors show quite comparable properties regarding their characteristics such as low-temperature, low-cost processing, large-area uniformity and transparency, they have their own strengths and weaknesses in comparison with each other. In addition, even though both p-type oxide semiconductors and n-type organic semiconductors have been reported [71][72], n-type oxide and p-type organic semiconductors have shown to be more stable and therefore, can be employed together to achieve complementary metal-oxide-semiconductor (CMOS) devices that can be utilised in integrated circuits (ICs) for next-generation electronics. When oxide semiconductors are compared with organic semiconductors, it can be seen that they possess more electrical and environmental stability as well as higher performance. However, both are good candidates

for the substitution of conventional technologies, given that they can compensate for most of their weaknesses.

2.2.2.1 Carrier transport in AOSs

The understanding of charge transport mechanism plays a decisive role in the commercial applications of a-IGZO TFTs. However, there is no agreement on a single charge transport mechanism in a-IGZO transistors as, on the one hand, amorphous oxide semiconductors (AOSs) have far lower charge carrier mobility (μ) than that measured in single-crystalline semiconductors [73], and on the other hand, they have higher μ (1–10 $cm^2\ V^{-1}\ s^{-1}$) than a-Si:H (≤ 1 $cm^2\ V^{-1}\ s^{-1}$). Thus, due to their intermediate mobility values, two basic charge carrier transport mechanisms, namely, thermally activated hopping transport typically used in low-mobility disordered solids and the classical band transport model are inapplicable [74]. Finding a theoretical description which can fully explain the charge carrier transport in AOSs is still challenging. Hence, several charge carrier transport mechanisms have been proposed and studied in recent years [24][75][76]. Charge carrier transport in a given solid is fundamentally modelled by four distinct mechanisms—all of them have been proposed as feasible candidates for charge transport in AOS transistors, and in particular a-IGZO TFTs. In the following, all of them are briefly discussed.

2.2.2.2 Band transport via extended states in the random barrier model

Hosono and co-workers suggested band transport via extended states (delocalised states) as a possible charge transport mechanism in IGZO thin films [75][77][78][79]. In this model, it was assumed that the charge carriers could move above conduction band minimum (CBM) but owing to disordered structure, their motion is hindered by a Gaussian-type distribution $G_B(E)$ of random potential barriers attributed to the Ga^{3+} and Zn^{2+} ions:

$$G_B(E) = \frac{1}{\delta_\phi \sqrt{2\pi}} \exp\left(-\frac{(E-\phi_0)^2}{2\delta_\phi^2}\right), \qquad \text{(Eq. 2.16)}$$

where, ϕ_0 and δ_ϕ are the average height and the distribution width of the potential barriers, respectively. The random barrier model is illustrated in Fig. 2.6.

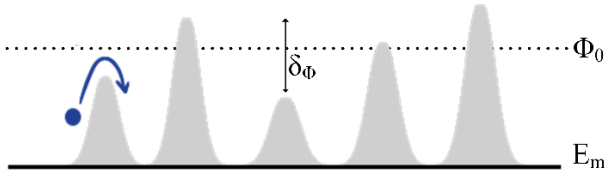


Fig. 2.6. Random barrier model for band transport above the band edge E_m affected by random potential barriers [80].

Charge transport in this model was defined in the context of the Drude approach based on the average relaxation time ⟨τ⟩—the mean time an electron has travelled since the last collision— for free carriers in the states above band edge (E_m). The Drude approximation is used for the band transport in the absence of a disorder potential [81] and with some suggested modification by introducing weight function ϱ(E), so-called "transmission probability" based on Adler *et al.* percolation model [82] in the presence of a substantial disorder potential [78]. The percolation model is a random cluster model which consists of adjacent or linked certain pairs of points in space wherein the case of lattice, each bond between neighbouring lattice sites can be occupied with probability p and empty with probability (1-p). The charge carrier mobility in AOS is calculated based on by:

$$\mu = -\frac{e}{m \cdot n} \int_{E_m}^{\infty} \tau(E) v_z(E) \varrho(E) \frac{\partial f_e(E)}{\partial v_z} D_m(E)\, dE\,, \qquad \text{(Eq. 2.17)}$$

$$\varrho(E) = \int_{E}^{\infty} G_B(\varepsilon)\, d\varepsilon, \qquad \text{(Eq. 2.18)}$$

where m is the effective mass, n the concentration of carriers, τ(E) the momentum relaxation time at an electron energy E, v_z(E) the electron velocity along the z-axis, D_m(E) the conduction band (CB) density of states (DOS), and f_e(E) the Fermi-Dirac distribution.

2.2.2.3 Trap-limited band transport

Trap-limited transport is quite similar to the multiple-trapping and release (MTR) model (Fig. 2.7) (also known as the mobility edge model), which has been proposed as a possible

electron-transport mechanism in AOSs [83][84]. The MTR model has been first developed to represent charge transport in disordered materials (e.g., a-Se) [85]. In this model, a charge carrier moves with microscopic mobility μ_0 only through extended states with energies above mobility edge, which is an energy level distinguishing delocalised states with relatively high carrier mobility from the localised states, which are herein considered as traps.

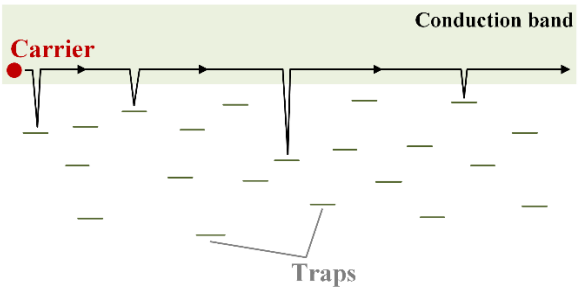


Fig. 2.7. A schematic of the multiple-trapping process (MTR) [86].

The motion of the charge carrier through the delocalised states is interrupted by trapping into the localised tail states with subsequent activation of carriers back into the conducting states above the mobility edge. Consequently, total carrier transport is determined by the effective drift mobility $\mu_{eff,}$ which depends on trapping and release times [87]:

$$\mu_{eff} = \mu_0 \frac{\tau_{free}}{\tau_{trap} + \tau_{free}}, \qquad \text{(Eq. 2.19)}$$

where τ_{free} is the trapping time, and τ_{trap} is a temperature-dependent release time (i.e., $\tau_{trap} \propto e^{E_a/kT}$) when $\tau_{trap} \gg \tau_{free}$. The energy scale ($E_0$) of distribution of traps in the band tail of inorganic amorphous semiconductors is the exponential shape and determined by:

$$N(E) = N_0 \exp\left(-\frac{E}{E_0}\right), \qquad \text{(Eq. 2.20)}$$

where N_0 is the density of localised states, and E the energy of the trap between E_m and E_0 in the energy spectrum. Lee *et al.* utilised multifrequency capacitance-voltage (C-V) characteristics as an extraction technique to determine the subgap DOS in n-channel a-IGZO TFTs. They concluded that the subgap DOS is a superposition of two different exponential

functions of tail states and deep states [83]. Also, they concluded that both trap-limited conduction (TLC) and percolation conduction participate in carrier transport in AOS TFTs. They deduced that in a range of low V_{GS} (i.e., at small carrier concentration), TLC is the dominant mechanism, while at high V_{GS}, the percolation conduction prevails [88] and determines the drift mobility of carriers to be:

$$\mu \cong \mu_{mod} \frac{n_{free}}{n_{trap} + n_{free}}, \qquad \text{(Eq. 2.21)}$$

where n_{free} and n_{trap} are free and trapped carrier concentrations, respectively, and μ_{mod} is the usual band mobility prefactor μ_0 modulated by a percolation term which is derived from Thomas-Fermi approximation [88]. However, it has been shown that this approach is inappropriate for the description of incoherent charge transport [73].

2.2.2.4 Hopping transport

Mott demonstrated that charge carriers can move between localised states in disordered solids by incoherent tunnelling (hopping) [89] and is typically the dominant charge carrier transport mechanism in low mobility materials (≤ 1 cm^2 V^{-1} s^{-1}). In this mechanism, charge carrier transport occurs from low- to high-energy localised states by thermal activation. In the conventional disordered semiconductors like a-Si:H, due to the fact that Fermi level is usually located within localised states, hopping transport is limited to low and moderate temperatures [73]; however, MTR is the dominant transport mechanism at higher temperatures. Therefore, depending on the density of charge in localised states, temperature, and shape of DOS, the total current mostly results from hopping transport and/or band-like transport [90]. Although hopping has been shown to be irrelevant in a-IGZO TFTs due to a well-defined Hall measurement that showed the significant role of band-like transport in total current, Germs *et al.* argued that having a band-like transport above mobility edge does not necessarily mean that it cannot simultaneously be variable range hopping (VRH) below the mobility edge. In this light, Germs *et al.* extended the MTR model to consider VRH in

the localised states below mobility edge, as well as the band-like transport in delocalised states above mobility edge and named it, extended mobility edge (eME) model. This model is based on the concept of an energy level called the transport energy (E_t) and defined as an energy level where charge carrier transport from below states happens in the vicinity of this energy while occurs downward for higher energy states above E_t [91].

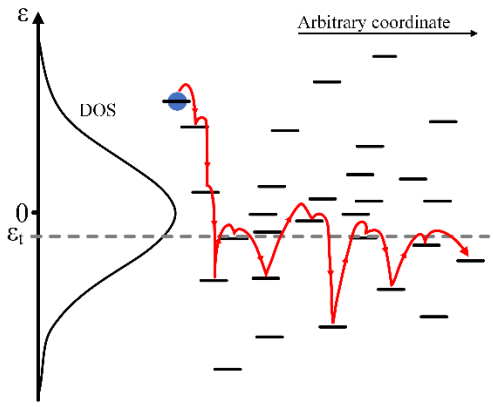


Fig. 2.8. Schematic of carrier energy relaxation via the transport energy in a Gaussian DOS [92].

Therefore, the carrier mobility in this model can be calculated by:

$$\mu = \widetilde{\mu_0} \exp\left[-\frac{E_t - E_f(n,T)}{kT}\right], \qquad \text{(Eq. 2.22)}$$

where $\widetilde{\mu_0}$ is the preexponential factor which depends on the density of carriers n. According to Eq. 2.22 and based on the high carrier mobility measured for the IGZO semiconductor, the hopping mechanism can only be the dominant charge carrier transport mechanism if the semiconductor has an oddly large value of the localisation length ($a \cong 4.8$ nm) in the tail states. However, this is far higher than the localisation length in the band tail of inorganic semiconductors [81][93]. Therefore, it seems that the hopping mechanism is unlikely to be the main charge carrier transport mechanism in AOS generally, and particularly in IGZO thin films.

2.2.2.5 Random band-edge model

Recently, Fishchuk *et al.* proposed a charge carrier transport model based on the effective medium approximation (EMA) for a disordered semiconductor with high carrier

concentrations which causes Fermi level to be in the vicinity of conduction-band edge (CBE) [80]. The EMA is an analytical model developed for averaging multiple values; herein, Fermi-Dirac carrier distributions include both delocalised and localised states. Fishchuk *et al.* suggested that their model can bridge the gap between hopping and band-like transport in a heterogeneous system. They found out that electron conduction in a-IGZO is predominantly through delocalised states, and the amorphisation process in a-IGZO increases the random spatial potential variation of the CBE rather than localised states. Fig. 2.9 shows the random long-range variations.

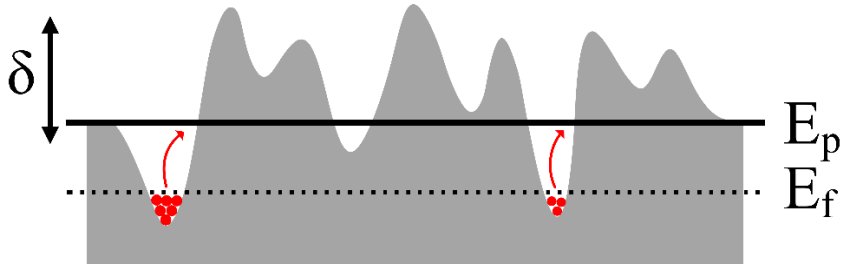


Fig. 2.9. The schematic of the spatial fluctuations of band edge E_m in the random band-edge model. The carrier motion is due to activation from Fermi level E_f towards the percolation level E_p [80].

The localised states and extended states are distinguished by separating energy called E_m, the conduction band edge (Fig. 2.10).

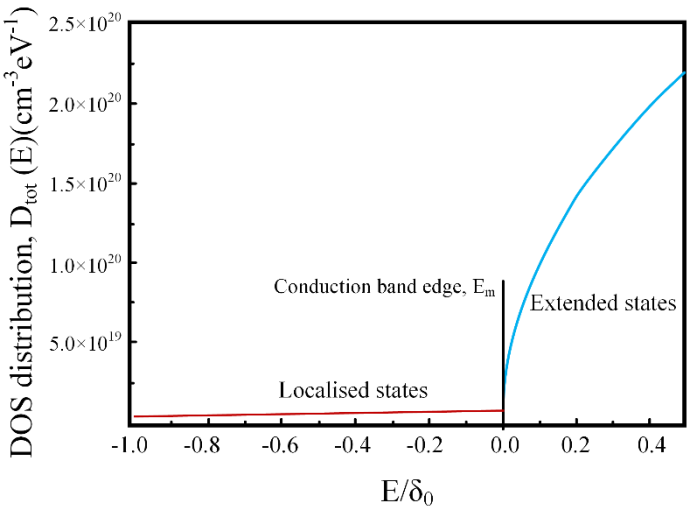


Fig. 2.10. Cumulative DOS D_{tot} (E) distribution [74].

They assumed that i) the disorder causes random spatial long-range variations of the E_m as the variation are smooth enough with the length of variations is larger than the mean free path of a charge carrier and much smaller than the length of the system and ii) the mentioned

potential variations of E_m can be described by a Gaussian distribution with the standard variations δ_0.

$$g(E_m) = \frac{1}{\delta_0\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{E_m}{\delta_0}\right)^2\right], \quad \text{(Eq. 2.23)}$$

In order to calculate the charge carrier transport, the total DOS distribution in the whole energy arrange required for both below and above conduction band edge E_m. The former can be calculated by Eq. 2.20, the distribution of localised states in inorganic semiconductors and the latter is the delocalised states ($E > E_m$) characterised by [74]:

$$D(E - E_m) = D_c\sqrt{E - E_m + \Delta E}\,, \quad \text{(Eq. 2.24)}$$

where the value $D_c = 1.4 \times 10^{21}$ cm^{-3} eV$^{-3/2}$ for a-IGZO thin films, which been previously reported in [78] and ΔE is the energy shift which guarantees the continuity of the DOS in $E = E_m$ when $\Delta E = (N_0/D_c)^2$. The total DOS can be determined by a combination of Eq. 2.20 and 2.24 and written as [74]:

$$\begin{aligned} D_{tot}(E - E_m) = \theta(E - E_m)D_c\sqrt{E - E_m + (N_m/D_c)^2} \\ +[1 - \theta(E - E_m)]N_m \exp\left(\frac{E - E_m}{E_0}\right), \end{aligned} \quad \text{(Eq. 2.25)}$$

where $\theta(x)$ is the Heaviside step function, where its value is zero for negative arguments and unity for positive arguments. In order to find the charge carrier mobility, the conductivity of the system σ should be determined first. Fishchuk *et al.* employed effective medium approximation (EMA) method that previously introduced by Kirkpatrick [94] to determine the effective conductivity σ_e:

$$\left\langle \frac{\sigma_{region}(E_m) - \sigma_e}{\sigma_{region}(E_m) + (d-1)\sigma_e} \right\rangle = 0, \quad \text{(Eq. 2.26)}$$

where σ_{region} is the regional conductivity at the band edge, and d the spatial dimension, herein, d = 3 for a three-dimensional (3D) system. In the context of EMA and apart from the

conductivity of the system, finding Fermi level E_f is another essential parameter to calculate the carrier mobility (n, T). Thus the Fermi level can be calculated using regional electron density (n_{region}) for a given value of E_m by [74]:

$$n_{region}(E_m) = \int_{-\infty}^{+\infty} D(E - E_m) f(E)\, dE, \qquad \text{(Eq. 2.27)}$$

where f(E) is Fermi function and determined by [74]:

$$f(E) = \left[\exp\left(\frac{E - E_f}{kT}\right) + 1\right]^{-1}, \qquad \text{(Eq. 2.28)}$$

The total electron density n_{tot} is obtained by averaging based on EMA method over the regional positions of E_m by [80]:

$$n_{tot} = \int_{-\infty}^{+\infty} g(E_m) n_{region}(E_m)\, dE_m, \qquad \text{(Eq. 2.29)}$$

For a given temperature T and electron concentration n, the regional conductivity (σ_{region}) can be rewritten by [80]:

$$\sigma_{region} = e\mu_0 \int_{E_m}^{+\infty} g(E - E_m) f(E)\, dE, \qquad \text{(Eq. 2.30)}$$

where e is the elementary charge, μ_0 is the intrinsic (band) drift charge carrier mobility in delocalised states determined by the effective mass (m^*) and the average scattering time (τ) [74]:

$$\mu_0 = \frac{e}{m^*}\langle\tau\rangle. \qquad \text{(Eq. 2.31)}$$

Here, for the sake of simplicity similar to [80], μ_0 is considered as a constant. The global value of conductivity (σ) is found by averaging the regional value of σ_{region} and considering Gaussian distribution $g(E_m)$. As a result, mobility (μ) can be calculated by:

$$\mu = \frac{\sigma}{en} \qquad \text{(Eq. 2.32)}$$

Fishchuk *et al.* concluded that due to the fact that charge carrier mobility through the delocalised states is typically much higher than hopping charge mobility by localised states, hence, the conductivity is mainly determined by the delocalised states above the mobility band edge in IGZO materials [74]. As averaging is an important procedure for the correct determination of total conductivity in a given material, Nenashev *et al.* argued that the effective medium approximation (EMA) used in [74] is not the most proper method as in some cases (e.g., low-temperature, low-concentration and strong disorder $kT \ll \delta$) result in an exponentially large error and therefore, they introduced the averaging procedure based on percolation theory [80]. Averaging based on the percolation theory and EMA are frequently perceived complementary methods as the percolation theory is commonly considered for strongly disordered materials while the EMA is often employed for weak disorder materials. However, Nenashev *et al.* demonstrated that the percolation theory could be used not only for strong disorder materials, but it produces valid data for the opposite case where $\delta \to 0$. As mentioned before, the random band-edge model can be described by percolation theory. In this model, the transport is obtained by charge carrier above the percolation level E_p the minimum energy that allows charge transport between the connected region with $E_m < E_p$. Thus, based on the calculations in [80] the charge carrier mobility using this model at low temperature and $kT \ll \delta$ can be determined by:

$$\mu \approx \mu_0 \frac{N_c}{n} \frac{G\left(E_p\right) kT}{1 - \vartheta_c} \exp\left(\frac{E_f - E_p}{kT}\right), \qquad \text{(Eq. 2.33)}$$

where N_c is the effective DOS in the conduction band and ϑ_c is the percolation threshold determined to be 0.17 ± 0.01 for the 3D continuum percolation problem and $E_p = -0.95\,\delta$ while for the EMA model, the charge mobility is calculated by [80]:

$$\mu \approx \mu_0 \frac{N_c}{2n} \exp\left(\frac{E_f - E^*}{kT}\right), \qquad \text{(Eq. 2.34)}$$

here E^* is the value of mobility edge E_m where $\sigma_{region}(E_m) \gg 2\sigma_e$ change the Eq. 2.26 to $\sigma_{region}(E^*) = 2\sigma_e$ and determined to be $E^* \approx -0.43\delta$. This is evidence that even without taking the preexponential factor into consideration, the mobility obtained from the EMA and percolation model differs an exponential factor $\propto \exp(-0.52\ \delta/kT)$. Therefore, Nenashev *et al.* concluded that although the EMA model has not generally significant differences based on experimental data, still in some cases (e.g., 30 $cm^2\ V^{-1}\ s^{-1} < \mu_0 < 47\ cm^2\ V^{-1}\ s^{-1}$, 36 meV $< \delta <$ 63 meV), where disorder is strong, random band-edge model based on the percolation theory is the most proper model to interpret the charge carrier mobility in a-IGZO systems thus far [80].

2.2.3 Organic semiconductors

Organic materials, such as polymers, have traditionally been viewed as insulating materials. However, the discovery in the late 1970s that doping of π-conjugated polymers can significantly increase their conductivity paved the way for the intensive research and development of organic semiconductors based on conductive polymers [95]. In 1997, Heeger, MacDiarmid, and Shirakawa published their seminal work [96] and demonstrated that poly(acetylene) could become truly conductive if it is highly doped with iodine as an acceptor dopant. Since then, organic semiconductors have gained a lot of attention owing to their lightweight, ease of processability, low cost, and ability to be used for large-area, flexible devices.

Organic semiconductors are typically referred to as "conjugated" materials and are generally divided into two main categories: conjugated polymers and conjugated small molecules (oligomers). When conductive, a conjugated organic material is composed of alternating single/double or single/triple bonds between carbon atoms along its backbone [97]. The orbitals of a carbon atom (i.e., ^{12}C) with the electronic configuration in its ground state of $1s^2 2s^2 2p^2$ can be hybridised when excited by the superposition of s and p orbitals in a variety

of forms, including sp, sp^2 and sp^3 (Fig. 2.11) [97]. A carbon atom has the sp^3 hybridisation if bonding occurs between one s orbital and three p orbitals in the same shell of an atom which results in four new equivalent orbitals that consist of single bonds. A carbon atom has the sp^2 hybridisation when bonding occurs between one s orbital and two p orbitals (Fig. 2.12). The bond created by sp^2 hybridised atoms is known as a sigma (σ) bond and the remaining unhybridized p orbital is known as a pi (or π) bond. In the conjugated double bond structure, the single bonds are formed using σ bonds, and double bonds consist of a σ bond and a π bond. σ bonds are the covalent bonds, and the electrons of both atoms are shared from their s orbitals, and thus electrons which form σ bonds are strongly attached to the nuclei and are localised [16]. In comparison, electrons of π bonds are directly shared between p orbitals of two atoms, and due to the further orbital position of p orbitals to the positively charged nucleus, π-bonds make a weaker bonding than σ bonds. Although electrons of π orbitals are normally localised, it is shown that π electrons of conductive polymers are weakly localised and can enjoy a degree of delocalisation due to their conjugated structure which allows π orbitals of the neighbouring double bonds to overlap [97]. This overlapping results in delocalised π electrons which can hop from one bond to another or move along the whole molecule. The continuous overlapping of π orbitals in the conjugated backbone along with the resulting delocalisation make the formation and conduction of charge carriers along the polymer chain possible (intramolecular transport) [97].

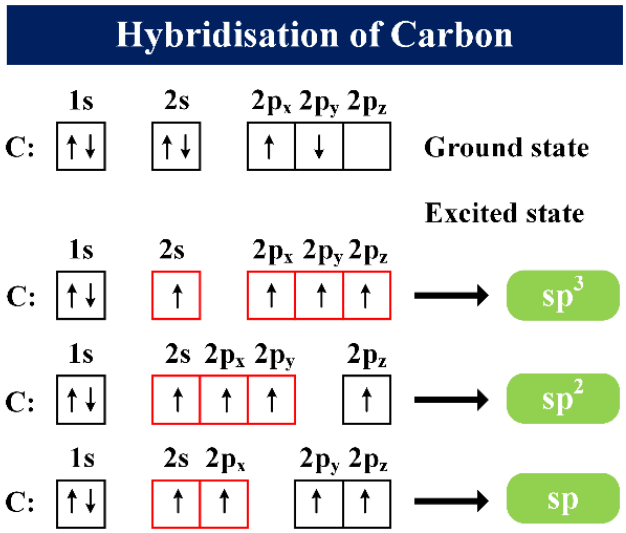


Fig. 2.11. sp hybridisation of a carbon atom— s and p orbitals can mix and form sp, sp^2 and sp^3 hybrid orbitals, respectively.

The alternating of double and single bonds in the conjugated backbone increases the separation of bonding and anti-bonding states, resulting in the formation of a forbidden energy gap and spatially delocalised band-like electronic structure. Some of the molecular orbitals filled with electrons when the molecule is in the ground state and higher levels leave empty (Fig. 2.13).

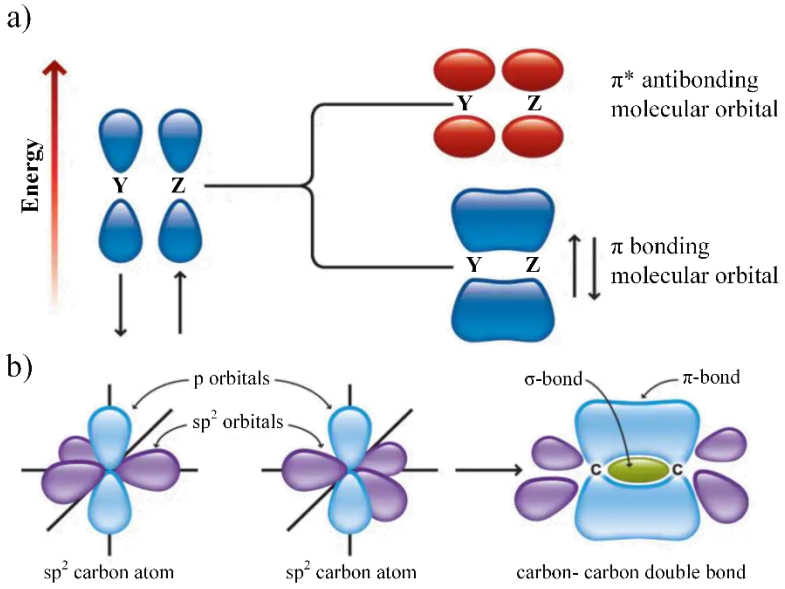


Fig. 2.12. a) π orbital formation from two p-orbitals, and b) formation of σ- and π- molecular orbitals from two sp^2 hybridised carbon atoms.

The highest occupied molecular orbital (HOMO) comprises bonding states of the π orbitals with filled electrons and is equivalent to the valence band (VB) while the lowest unoccupied

molecular orbital (LUMO) comprises empty higher energy anti-bonding (π^*) orbitals and is similar to the conduction band (Fig. 2.13). As with inorganic semiconductors (e.g., silicon), there is an energy bandgap (E_G) between HOMO and LUMO states which determines the semiconducting or insulating properties of most polymers (conjugated or not). E_G depends on the chemical structure of the repeating unit, and generally, it can be said that the larger the conjugated network is on a molecule, the smaller the HOMO-LUMO gap becomes. The E_G of conjugated polymers is typically around 1–4 eV making them be categorised as semiconductors [97].

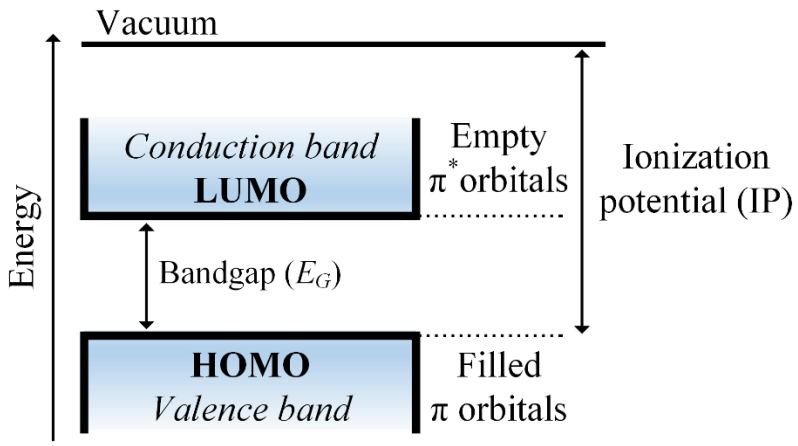


Fig. 2.13. Representative energy band diagram of an organic semiconductor.

As abovementioned, organic semiconductors are generally polymers or small molecules made from a small foundational group of conjugated monomer units. Conventionally, the highest performance devices have been based on the small molecules rather than polymer semiconductors due to their tendency to form relatively large crystalline regions with grain sizes up to one micron. Fig. 2.14 shows some examples of conjugated small molecules that are widely used in OTFTs. In some cases, devices based on small molecules semiconductors, such as pentacene ($\mu \sim 6$ cm^2 V^{-1} s^{-1}) and sexithiophene ($\mu \sim 1$ cm^2 V^{-1} s^{-1}), have been shown higher mobility than that of a-Si:H [98]. Nonetheless, their high performance comes with substantial ordering, particularly in the vicinity of the dielectric/semiconductor interface. Also, obtaining highly ordered small molecules semiconductors is not straightforward and

can be problematic specifically with some solution processing deposition techniques. One the other hand, polymer semiconductors are useful materials to be used in electronic devices as they more easily form a thin film with the large surface area than small molecules and are compatible with the deposition techniques which have been previously developed for conventional polymers (e.g., photoresists). Two most used conjugated polymers in OTFTs are polyfluorenes (e.g., poly(9,9-dioctylfluorene-alt-bithiophene), also known as F8T2) and polythiophene based materials such as poly(3-alkyl-thiophene) (P3AT). Fig. 2.15 illustrates some of the most popular conjugated polymers employed as organic semiconductors in transistors. The performance of polymer-based OTFTs crucially depends on the chemical and structural ordering of the polymer. High regioregularity of the polymer depends on the percentage of regioregular head-to-tail attachment of alkyl side chains to the beta position of thiophene rings and the orientation of polymer chains itself.

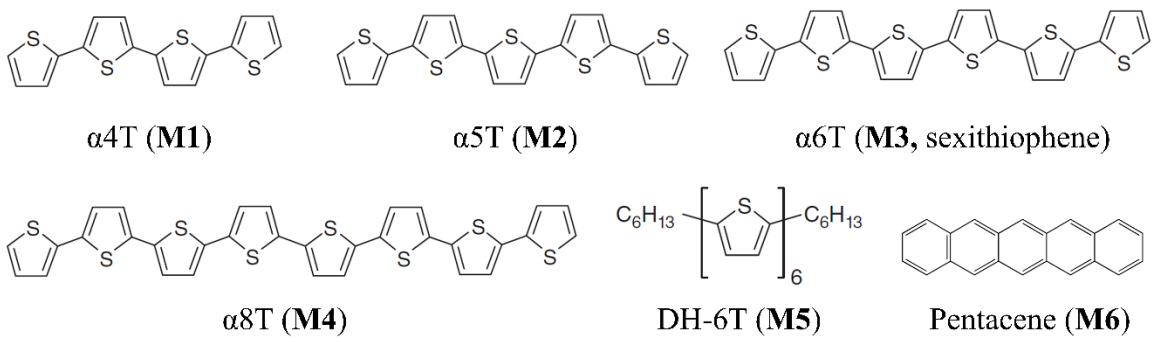


Fig. 2.14. Chemical structure of the representative p-type small molecule semiconductors [99].

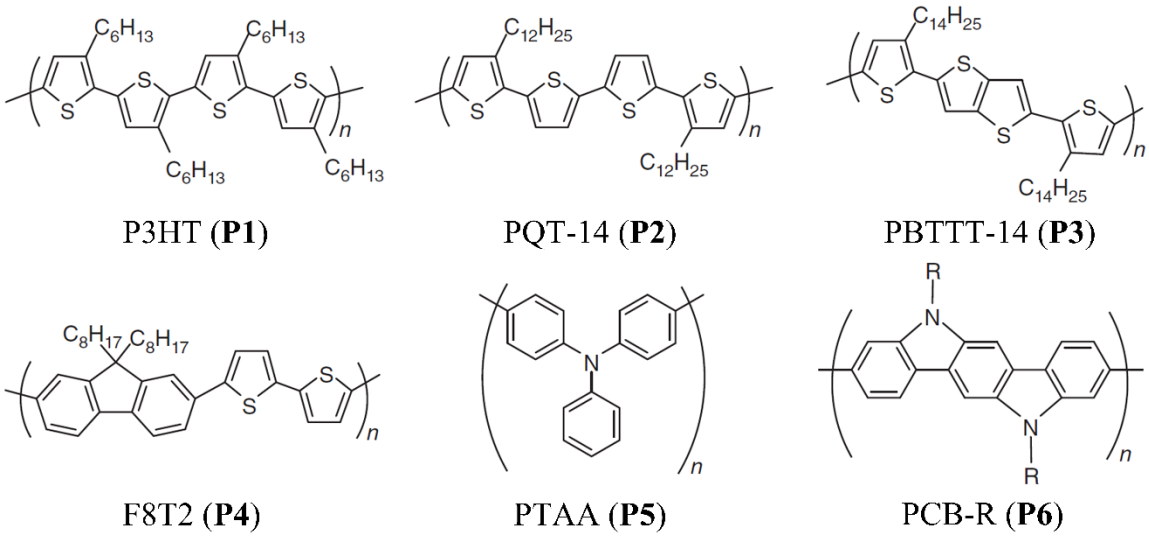


Fig. 2.15. Chemical structure of the representative p-type polymer semiconductors [99].

In terms of charge carriers' type, most polycrystalline or amorphous organic semiconductors exclusively support positive or negative charge carriers, but not both. Moreover, n-type and p-type semiconductors typically describe the type of dopant or majority carriers in the intrinsic semiconductors, where depending on the type of the semiconductor, holes or electrons are effectively transported. Therefore, it is quite common in the literature to refer to hole transporting for p-type and electron transporting for n-type organic semiconductors, respectively [16]. Even though the most used semiconductors for the application of OTFTs are p-channel devices owing to their higher mobility, better air stability and wider solubility compared with n-type organic semiconductors, n-type OSCs are required to fabricate p–n diodes, bipolar transistors, and complementary circuits [97][100]. One obstacle which impedes n-type organic semiconductors to have high performance is the much smaller number of available electron-withdrawing building blocks that are required for stable electron transport characteristics [100]. For example, when an electron is injected into an n-type organic semiconductor, it is similar to a reduction process in an electrochemical reaction. If the OSC has a quite high LUMO energy level, the injected electron in the LUMO level of the semiconductor is at the high-energy state, which is more likely to interact or react with OH groups on the surface of metal oxide dielectrics or O_2 and H_2O in ambient air and therefore, the injected electron is trapped or annihilated. Thus, the trapped or annihilated

electrons exacerbate the electron transport in organic semiconductors, and consequently, the device performance [100]. Fig. 2.16 demonstrates electron and hole injection in n-type and p-type organic semiconductors.

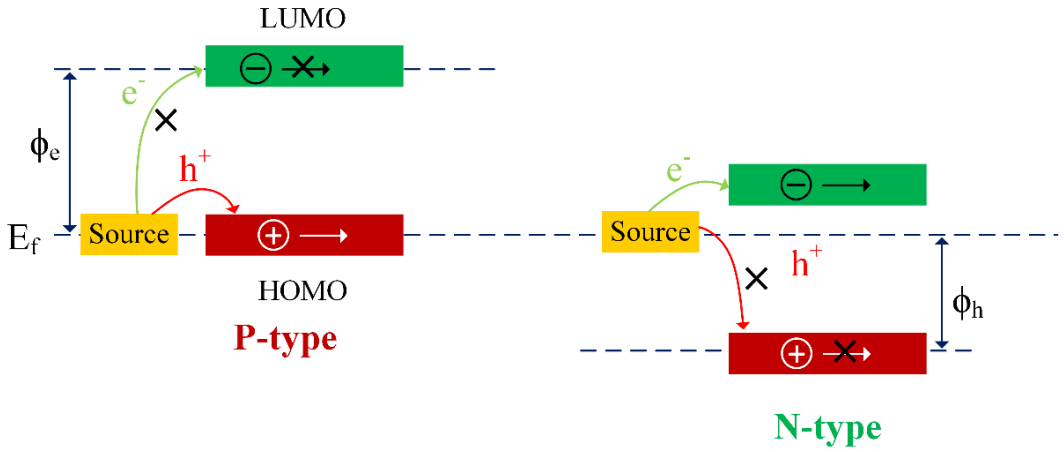


Fig. 2.16. The schematic shows the relationships among the Fermi energy (E_f) of the source electrode, the frontier energies of the organic semiconductor, and the polarity of the majority charge carriers of the OTFT device, where ϕ_e and ϕ_h denote the electron and hole injection barrier heights, respectively, and ‘‘×’’ denotes the inhibition of charge injection or transport [100].

2.2.3.1 Carrier transport mechanism in OSCs

The two basic properties of organic semiconductors are the semiconducting properties on the molecular level and weak intermolecular bonds formed by van der Waals interactions. Therefore, carriers are relatively localised and can only hop to a limited number of adjacent molecules. However, in some carbon-based materials despite the fact that atoms are covalently bonded, due to the alternation of single and double bonds resulted by sp^2 hybridisation, delocalised clouds of electrons are formed between atoms within the molecule and said to be conjugated. Based on these fundamental properties, the charge carrier transport mechanism in OSCs can be diverse and thus, the three types of carrier transport mechanisms, namely, hopping transport, band-like transport and multiple trap-and-release (MTR) theory previously discussed for oxide semiconductors have been considered for OSCs, as well. In fact, the charge transport in OSCs is somewhat similar to the charge transport in AOSs. Herein, only the differences relating to the description of the charge transport in OSCs are briefly discussed.

2.2.3.1.1 Hopping transport

For a wide range of polymer-based semiconductors, such as P3HT, DPPDTT, etc., due to the spatial and energetic disorder, the charge carriers are always located in the localised states. The carrier transport in these materials always occurs through hopping from one localised site to another and depends on the electronic wave functions of these sites. In terms of site energy, whenever a charge carrier jumps from a lower (higher) site energy to a higher (lower) site energy, the energy difference is adjusted by absorption (emission) of a quasi-particle, polaron [101]. Depending on hopping distance and site energy, the hopping transport mechanism can be categorised into the nearest-neighbour hopping (NNH) [102] and variable-range hopping (VRH) [103][104]. The nearest-neighbour hopping is attributed to a hopping situation in which its tunnelling part occurs with a slower rate than the energy contribution and therefore, charges can mostly hop to the neighbour sites, while the VRH (discussed in 2.2.2.4), describes the situation where the charge carriers have a higher chance of hopping with more desirable energies close to Fermi level. Typically, the NNH is suitable in high temperature and small localisation radii, while VRH mostly occurs at sufficiently low temperatures [105].

2.2.3.1.2 Band-like transport

It turns out that the charge carrier transport in small molecular crystals of, for example, pentacene is different from the charge carrier transport in polymers as they typically show higher charge carrier mobility [106]. In organic small molecules, the carriers can move with a much larger mean free path than that of nearest neighbour distance by the delocalised states [105]. The band-like transport is quite similar to charge carrier transport in crystalline inorganic semiconductors. In an ideal crystal inorganic semiconductor, the charge transport is completely dominated by delocalised states without any scattering. However, increasing the temperature in real inorganic crystals results in reducing the charge carrier mobility and vice versa due to the defects such as lattice vibrations or phonons. Therefore, operating these

semiconductors at low temperatures can remarkedly enhance the charge-carrier transport based on the concept of the band-like transport mechanism.

2.2.3.1.3 Multiple trapping and release theory

Apart from crystalline and amorphous organic semiconductors, some organic materials depict superior performance due to their poly-crystalline regioregular structure [16][107]. In this class of organic semiconductors, the delocalised orbitals of neighbouring molecules partially overlap and thus enhance the intermolecular charge carrier transfer resulting in higher charge carrier mobility [108]. Accordingly, the transport mechanism is not readily described by the discussed transport mechanisms, neither band-like transport nor hopping transport. The multiple trapping and release theory (MTR) is well compatible with this type of organic materials. Although the MTR theory is discussed in section 2.2.2.1, it is noteworthy to mention that charge carrier transport based on this theory depends on the temperature and the position of the localised states regarding the mobility edge [105].

2.2.3.2 Semiconductor Blends

As discussed, recent research on organic semiconductors is pivoted around three key areas, fabricating high charge carrier mobility devices, realising complementary logic gates with equally good n-type and p-type conduction and simplifying the fabrication procedures [109]. One method to achieve the required properties in organic devices is to blend two or more organic components in order to improve the performance of individual materials synergistically. Blending organic compounds can be easily achieved if the materials are soluble and processable in a common solvent.

In polymer/polymer blends, two or more components often show vertical phase separation during the deposition process. As mentioned before, most of the n-type organic semiconductors suffer from low mobility and poor air stability. However, several research groups have reported that a blend of n-type and p-type polymers (ambipolar system) can

address some of these problems. For instance, Geens *et al.* presented a blend of n-type 6,6-phenyl-C61-butyric acid methyl ester (PCBM) and p-type poly(2-methoxy-5-(3′,7′-dimethyloctyloxy)-p-phenylene vinylene) (MDMO-PPV) materials that can have good electron conduction. Moreover, it turns out that the air stability issue can be solved by using an ambipolar organic semiconductor which consists of an n-type poly(benzo-bisimidazobenzo-phenanthroline) (BBL) and a p-type small molecule copper phthalocyanine (CuPc) materials [110]. From a different perspective, it has been shown that blending an organic semiconductor and dielectric can form a bilayer if significant vertical phase separation occurs, which improves the performance of OTFTs [109]. It has been reported that the blend of P3HT as p-channel OSC and poly(methyl methacrylate) (PMMA) as a dielectric modifier or as the dielectric itself can lower the operating voltage of OTFTs due to forming a very thin dielectric layer [111]. Generally, the advantages of dielectric/semiconductor blends as a vertically phase-separated bilayer for OTFTs can be summarised in lowering the leakage current due to adding an extra dielectric layer in the case of using along with the main dielectric, reducing the number of device fabrication steps, improving the dielectric/semiconductor interface or/and the smoothening surface of the main dielectric, and increasing device stability by increasing the possibility of incorporate encapsulation of the active materials into the same processing step [109].

2.3 Dielectric materials for TFTs

2.3.1 Background

By definition, an insulator is a material that has an extremely high resistivity to electric current. In other words, the electrons in the valence band in this type of materials are separated by a large bandgap which results in a lack of charge transport and leads to insulating behaviour. In insulators, the bandgap (E_G) is typically assumed to be larger than 4 eV. Fig. 2.17 illustrates the band structure of conductor, semiconductor and insulator.

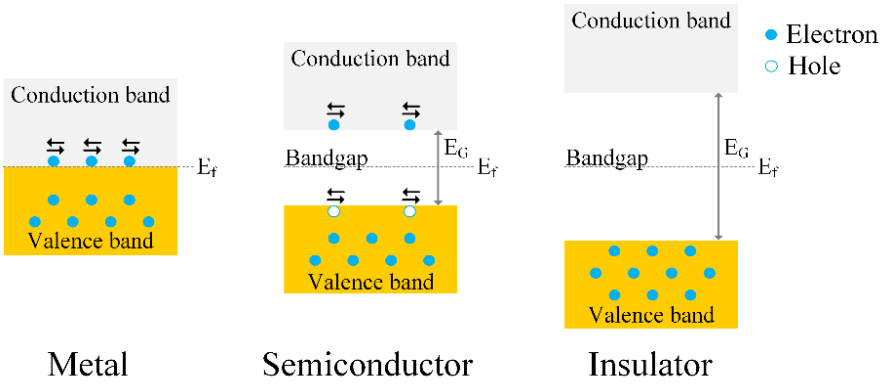


Fig. 2.17. The band structure of a metal, semiconductor, and insulator.

In general, insulators can be polar or non-polar. In chemistry, polarity is attributed to the change in electronegativity (i.e., a tendency of materials to gain electrons) of atoms within a molecule. The main difference between polar and non-polar insulators is that the molecules of polar insulators (so-called dielectrics) have an asymmetry in charge distribution, whereas the molecules of non-polar insulators have a symmetrical structure. Polar molecules have a permanent dipole moment, and thus they behave like tiny electric dipoles. In the absence of an external electric field, the dipoles are randomly arranged, and the net electric dipole moment of dielectrics is zero [112]. However, in the presence of an external electric field, the molecules within the dielectric medium change their orientation and align to the direction of the electric field. The alignment of dipoles can be improved by increasing the external electric field and decreasing the temperature.

On the contrary, non-polar molecules have no permanent dipole moments or their polar bonds cancel each other due to the symmetry of their structure. When non-polar atoms or molecules are subjected to an external electric field, the positive and negative charges are displaced in the opposite direction. This displacement continues until the external force is balanced by the restoring force due to the internal electric field. The internal electric field created due to the polarisation of the insulator is always opposite to the direction of the external electric field. Hence, the net electric field is reduced because of the polarisation of the insulator. However, when the external electric field is removed, the dipole moments of each non-polar atom and molecule of the insulating medium become zero.

Basically, a dielectric is unable to be polarised immediately by an electric field (E). Therefore, the polarisation density (P) is formulated as a function of time (t) and calculated by [5]:

$$P(t) = \varepsilon_0 \int_{-\infty}^{t} \chi_e(t - t')E(t)\, dx', \quad \text{(Eq. 2.35)}$$

where ε_0 is vacuum permittivity (8.86×10^{-12} $C^2N^{-1}m^{-2}$) and χ_e the electrical susceptibility which is related to the dielectric constant (κ) and determined by $\chi e = \kappa - 1$. The relationship between the polarisation density (P) and the electric field (E) can be shown in a simpler form as a function of frequency in the Fourier transform by [113]:

$$P = \varepsilon_0 \chi_e E \quad \text{(Eq. 2.36)}$$

Dielectric relaxation is described as a delay in polarisation with respect to a changing electric field within a given dielectric which is caused by an irreversible reduction of energy (i.e., the decay of polarisation from excited states to the ground state) [5][114]. Typically, dielectrics have two types of losses, namely, conduction loss and dielectric loss. Conduction loss occurs when a charge flows through the dielectric from one electrode to another, and dielectric loss is defined as a rotation or movement of atoms or molecules within the dielectric medium in an alternating electric field. An effective approach to defining these losses in detail is to express them by dielectric permittivity (ε) as a complex number, as shown in Eq. 2.37:

$$\varepsilon = \varepsilon' - j\varepsilon'' = |\varepsilon| e^{-j\delta}, \quad \text{(Eq. 2.37)}$$

where ε' is the ac capacitivity, ε'' dielectric loss factor and δ dielectric loss angle. However, loss tangent ($\tan\delta$) is usually expressed by ε' and ε'' and δ, as shown in Eq. 2.38:

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \quad \text{(Eq. 2.38)}$$

Typically, the most desirable dielectric materials for use in TFTs are those with a very low dielectric loss (e.g., < 0.01). In studying of dielectric constant (κ), it is crucial to have a comprehensive understanding of its origin which is based on various types of polarisation

mechanisms namely, electronic (atomic), ionic, molecular orientation (or dipolar), electrode (or electric double layer (EDL)) and interfacial (space-charge) polarisation [115]. For a given material, the net polarisation (P) can be determined by the sum of contributions from each mechanism:

$$P = P_{electronic} + P_{ionic} + P_{molecular} + P_{interfacial} \quad \text{(Eq. 2.39)}$$

Conventionally, the behaviour of a dielectric is obtained by dielectric relaxation spectroscopy (DRS) which demonstrates the interaction between the dielectric loss (tan δ) and the dielectric constant (κ) in terms of frequency (f) [116]. Fig. 2.18 shows the frequency dependency of κ and tan δ for various forms of polarisation.

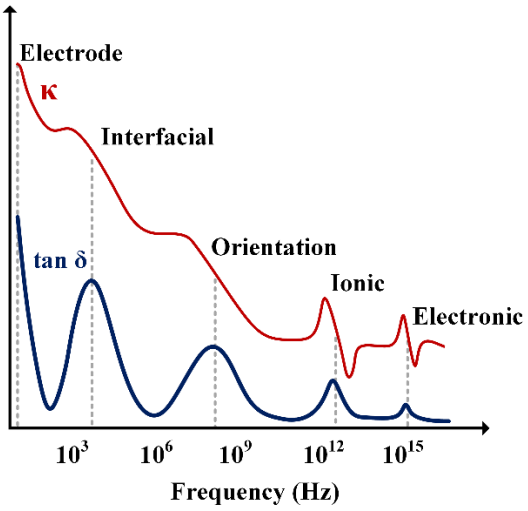


Fig. 2.18. Dielectric constant (κ) and dielectric loss (tan δ) for a material having electrode, space charges (interfacial or free-counterions), orientation, relaxation, condensed-counterions ionic, and electronic polarisation [5].

Fig. 2.19 depicts all polarisation mechanisms. Electronic polarisation is present in all materials and related to the delocalisation of electrons in response to visible light, electromagnetic field frequency (~ 10^{15} Hz) or under an applied electric field and form an electric dipole. Ionic polarisation, on the other hand, is the displacement of negative and positive ions toward the positive and negative electrodes, respectively. Since their mass is much heavier than that of electrons, the ions are unable to be swiftly polarised. Therefore, the maximum frequency that ionic polarisation can respond to is limited to 10^{13} Hz. Therefore, one way that is used to enhance the capacitive performance of the gate dielectric in OFETs is to use polymeric electrolytes which show excellent energy storage

characteristics [117]. Nonetheless, their practical applicability is limited due to the high dielectric losses. Molecular orientation polarisation refers to the reorientation of permanent molecular dipole moments of nanoparticles or of dipolar moieties appended to polymers [118]. The dipolar relaxation usually occurs between 0.1 and 10 MHz and depends on the nature of the dipole (crystalline or amorphous), temperature and frequency. Interfacial and electrode/EDL polarisation can only contribute at low frequencies. Interfacial polarisation is related to the reorganisation of interfacial charges (e.g., accumulated electrons and holes at interfaces) in heterogeneous systems [119]. Electrode/EDL polarisation usually occurs when all electric/ionic conduction systems contain free charges and/or ions under an applied electric field that move toward electrode or interfaces, leading to electric/ionic double layers in such regions [5][120]. Due to the nature of diffusion, space charge polarisation occurs rather slowly, and the typical frequency of response is approximately 10^2 Hz.

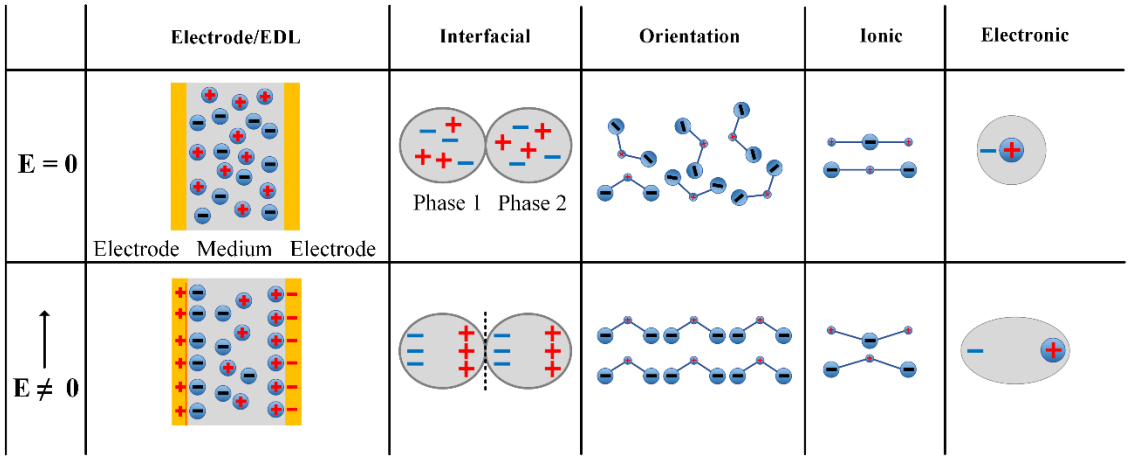


Fig. 2.19. The schematics of dielectric polarisation mechanisms.

In the case of a parallel plate metal-insulator-metal (MIM) capacitor which consists of two parallel plates separated by a distance (d), the electric field (E) is described by $E = V/d$ where V is a bias voltage applied to the capacitor (Fig. 2.20 (a)).

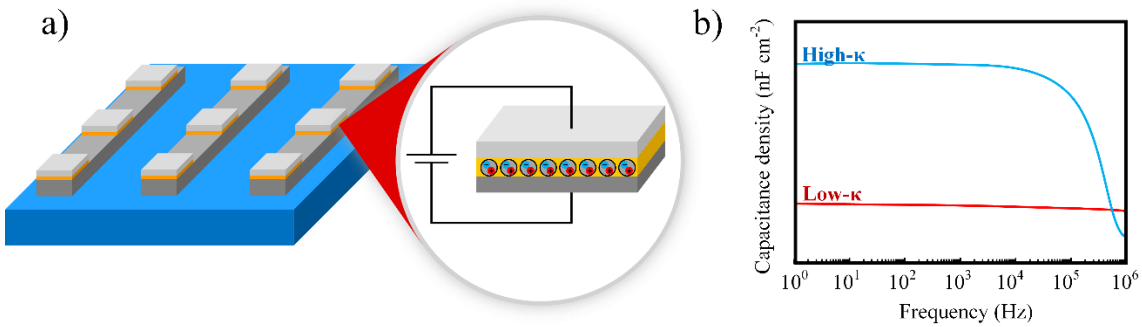


Fig. 2.20. a) Schematic diagram of a parallel-plate metal-insulator-metal (MIM) capacitor, and b) comparison of the frequency-dependent capacitance density of ideal high-κ and low-κ dielectrics.

In a vacuum, the charge (Q) on the plates is linearly proportional to the applied electric field and determined by Eq. 2.40:

$$Q = \varepsilon_0 E = \frac{\varepsilon_0 V}{d}. \qquad \text{(Eq. 2.40)}$$

The ability of the capacitor to store charges is measured by its capacitance (C) and defined by:

$$C = \frac{Q}{V} = \frac{\varepsilon_0}{d}, \qquad \text{(Eq. 2.41)}$$

where ε_0 is vacuum permittivity (8.86×10^{-12} $C^2N^{-1}m^{-2}$), d the distance between the plates, Q the accumulated charge, and V the potential difference between the plates. The polarisation of a dielectric in a capacitor increases the capacitance by a factor equal to the relative permittivity ε_r (also referred to as the dielectric constant, κ) of the material. Accordingly,

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}, \qquad \text{(Eq. 2.42)}$$

where ε_r is the dielectric permittivity, A is the plate overlap area.

As shown in Eq. 2.42, the capacitance varies directly with ε_r (κ) and inversely with d. It is noteworthy that in terms of dielectric constant (κ), dielectric materials are divided into low-κ ($\kappa \leq 3.9$) and high-κ ($\kappa > 3.9$) materials [5]. According to Fig 2.20 (b), for high-quality high-κ materials, the capacitance density typically remains relatively constant at low frequencies but drops considerably at higher frequencies due to dissimilar behaviour of each polarisation in different frequency ranges and hindrance of some polarisations in high-κ

materials to follow changes of a high-frequency electric field. On the other hand, for high-quality low-κ materials, the change in capacitance density is somewhat negligible over the whole frequency spectrum since the major contribution to κ originates from the electronic polarisation.

2.3.2 Electrical properties

Although no electrical current can flow in an ideal dielectric, in practice, there is a certain amount of current, known as dielectric leakage current (I_{leak} or leakage current density J_{leak}), flows through the dielectric which typically depends on the electric field strength. The dielectric breakdown also refers to a process that occurs when a portion of an insulator, subjected to a sufficiently high electric field, suddenly becomes electrically conductive. This process results in permanent electrical/chemical damage to the dielectric. The two key parameters which are associated with this process are the breakdown voltage (V_b) and breakdown electric field (E_b). For proper TFT functionality, a dielectric with the lowest leakage current and highest breakdown strength is most desirable. To have an estimation of what these parameters should be in practical applications, Wang *et al.* suggest that the gate dielectric film with thickness below 50 nm should have a low leakage current density, $< 1 \times 10^{-7}$ A cm ^{2} at 2 MV/cm. For dielectrics with thicknesses between 50 and 300 nm, the leakage current density should be lower than 1×10^{-6} A cm^{-2} at 2 MV/cm. In terms of breakdown voltage (V_b), V_b with 1.5 times higher than the maximum gate-source voltage (V_{GS}) of the TFT is appropriate [5].

2.3.3 High-κ dielectrics

The intensive demands for high-performance, low power consumption field-effect transistors and the desire to keep Moore's law alive have led to the significant reduction of the FET dimension and consequently downscaling of SiO_2 dielectric thickness. However, the thickness of SiO_2 has reached its fundamental limits and decreasing its thickness below 2 nm is extremely challenging because it results in significantly high gate leakage current

density (i.e., J > 1 A/cm^2 at 1 V gate-source voltage) due to the tunnelling effect which strongly affects the transistor operation reliability and its performance. High leakage current density has several setbacks, such as impeding the further thickness reduction of the gate dielectric, which is necessary to decrease the power consumption and dimensions of the device. Using high-κ materials enables a thicker dielectric layer to provide the same capacitance required for realising low power devices. Moreover, a thicker layer effectively reduces the gate leakage current as tunnelling probability diminishes exponentially with tunnelling distance. An actual and successful example of using a high-κ dielectric is Intel Core 2 family microprocessor unit manufactured using HfO_2 gate dielectric. This results in 30% lower power consumption and significantly improved operating speed and other key parameters in comparison with the previous generation of Pentium 4 duo [121]. This method has also been used for completely different applications such as low-cost organic and inorganic thin-film transistors (TFTs) to lower their operating voltage. [122]. According to Eq. 2.42, the capacitance varies directly with ε_r (κ) and inversely with d. Consequently, in order to increase the capacitance of a metal-insulator-metal (MIM) capacitor, two approaches are usually considered: firstly, the increase of C can be accomplished by decreasing the dielectric thickness d, and secondly, increasing the dielectric constant (κ). As a result, increasing C by employing high dielectric constant (high-κ) materials using existing or novel high-κ materials appears to be a much more viable option. However, the development of new dielectric materials that possess high κ and simultaneously show low leakage current and high dielectric breakdown strength is not easy. Despite the obvious advantages of these materials in capacitors, TFTs and memory devices, they also possess serious drawbacks such as fabrication issues (e.g., pin holes), highly polar surfaces which result in high charge trap densities, particularly at the dielectric/semiconductor interface and polarisation effects in the bulk which lead to instability of the transistor threshold voltage and appearance of the drain-source current (I_{DS}) hysteresis. However, their advantages have

more weight, and therefore, high-κ dielectrics are being widely utilised in a variety of applications. Apart from their main function as the dielectric in transistors, they also play a crucial role in MIM diodes, capacitors, energy storage and high-frequency devices [123].

In general, the high-κ dielectric materials used in low-voltage TFTs are usually divided into four main categories, namely, ferroelectric polymers [124][125], electrolytes [126][127], inorganic metal oxides [128][129] and organic-inorganic hybrid dielectrics [130][131].

Among all of the polymer dielectrics, relaxor ferroelectric polymers such as poly(vinylidene fluoridetrifluoroethylene-chlorofloroethylene) (P(VDF-TrFE-CFE)) have been shown high dielectric constant ($\kappa \sim 60$), which have been used to realise low-voltage OFETs based on different organic semiconductors. However, due to the intrinsic ferroelectric behaviour of P(VDF−TrFE), the fabricated TFTs usually show large I-V hysteresis and thus, their application has mostly limited to memory devices [132]. One effective method to reduce the TFT hysteresis while retaining the high-κ dielectric is to blend P(VDF−TrFE) with paraelectric polymers such as polymethyl methacrylate (PMMA) and polyvinyl alcohol (PVA) or coating a thin polystyrene (PS) film on top it [124][133][134].

In general, electrolytes used as gate dielectrics are materials with mobile ions formed in opposite charges (anions and cations) at the electrolyte/electrode interfaces within an electric field. Polymer electrolytes are gel-type materials capable of transporting ions and typically used for supercapacitors [135]. The main advantage of using electrolytes, polyelectrolytes or polymer-electrolytes as a dielectric layer is their high dielectric constant ($\kappa > 60$), which induces a large gate dielectric capacitance (20 μF cm^{-2} to 500 μF cm^{-2}) and allows the operating voltage to be lowered [136][137]. Other important benefits derived from using electrolytes as a gate dielectric are low drain and source contacts resistances, versatile architectures, solution processability and their application in biosensors [138]. Although electrolytes enable ultra-low-voltage devices, it appears that they are thermally unstable and

their adhesion to the substrate during bending is problematic as they can be easily delaminated [139]. Also, the anions present in the electrolytes might unintentionally penetrate into the semiconductor and electrochemically dope the active layer [139][140].

Self-assembled monolayers (SAMs) can act as a nanometre-thick/high-capacitance gate dielectric. Although SAMs are typically categorised as low-κ materials (κ ~ 2–3), thanks to their ultra-thin thicknesses (~ 1–3 nm) and highly ordered morphology, they exhibit high capacitance and low leakage current, making them a promising candidate to be utilised in high-performance, low-voltage FETs as a gate dielectric, where thinning the dielectric cannot be easily done due to undesired leakage current and surface defects. Nevertheless, relatively difficult deposition and susceptibility to moisture in air limit their application in mass production [141].

High-κ inorganic dielectrics are crucial components in current and future microelectronic devices. The most common inorganic dielectrics used in TFTs are perovskites, metal oxides (MOs), nitrides (Si_3N_4, AlN), and their hybrid compounds. The metal elements utilised in these chemical compositions typically belong to the groups IIA, IIIA, IIIB, IVB, and VB in the periodic table. Also, it is noteworthy to mention here that alkali metal oxides and alkaline earth metal oxides are very hygroscopic—tend to absorb moisture from the air— which causes deleterious effects on the stability of the devices. Therefore, they are rarely considered as sole gate dielectric materials [142][5].

2.3.3.1 Metal oxide dielectrics

Metal oxide dielectrics (e.g., Al_2O_3, TiO_2, HfO_2 and ZrO_2) have been extensively investigated as they simultaneously guarantee high C_i and low J_{leak}. As such, they have been widely used in various applications such as capacitors, transistors and memory devices as insulating layers. Although in terms of the dielectric constant, MOs are superior to SiO_2, choosing the optimum metal oxide dielectrics for TFT applications is not simple and needs taking several aspects into consideration. For example, metal oxides such as Al_2O_3 have

typically high toughness to etching during subsequent post-deposition processes. Therefore, selecting a proper high-κ MO dielectric for TFT is not easy, and usually, four main aspects, namely, dielectric constant, bandgap width, moisture absorption, as well as surface morphology/defect states, need to be considered.

2.3.3.1.1 Criteria for metal oxide high-κ dielectrics

2.3.3.1.1.1 Dielectric constant

The first criterion of gate dielectric materials is dielectric constant or permittivity. To realise high-performance TFTs for utilising in next-generation circuits, it is essential that the gate dielectric has a high dielectric constant (κ >10, preferably 20–30) which enables larger dielectric thickness (4–7 times) to suppress gate leakage current with the same capacitance density [121]. Nevertheless, high-κ materials with too large dielectric constant (κ > 40) are also not advantageous as typically these materials include very polar functionalities or ionic impurities, showing frequency-dependent dielectric constants, hysteresis in the capacitance-voltage (C-V) and high dielectric loss [143].

2.3.3.1.1.2 Bandgap width

A very important physical property of each dielectric is its bandgap (E_G). A large E_G in dielectric materials is favourable because it requires electrons to acquire tremendous energy for excitation and transfer from the valence band to the conduction band. However, in typical high-κ inorganic dielectrics, the bandgap is inversely proportional to the dielectric constant (κ) and have a smaller E_G than SiO_2 [5]. Regarding the gate leakage current, small energy gaps may display a higher probability of direct tunnelling across the dielectric by Schottky emission and/or Poole-Frenkel effect discussed in detail in section 2.3.3.1.2 [144]. The relation between the bandgap and the dielectric constant of the most common high-κ oxide dielectrics is illustrated in Fig. 2.21. The Bandgap determines the band offset with the adjacent semiconductor. In comparison with SiO_2, high-κ materials show narrower E_G and

smaller band offset originated from the d-state electrons (valence electrons of transition metals) and high coordination ionic bond. The bandgap of MOs is mostly dominated by the electronegativity of the metal. In other words, higher metal oxide bond ionicity will occur for metals with smaller electronegativity, and consequently, the conduction band is decreased [145]. Employing a dielectric with too small band offset results in unacceptably high leakage current due to the thermionic emission of electrons and holes into dielectric bands. Table 2.2 summarises the most important electrical and structural properties of commonly used oxide dielectrics. As E_G is inversely proportional to κ in this type of materials and high κ and large E_G is desirable for the gate dielectric application, a trade-off between κ and E_G should be considered. For example, high-κ oxide materials such as TiO_2 ($\kappa \sim 80$) due to the very small E_G (3.5 eV) and band offset are not a suitable substitution for the gate dielectric in transistors with wide bandgap semiconductor. Therefore, to achieve reliable TFTs, ideally, E_G of a given dielectric should be larger than 5 eV. Also, the band offsets of the dielectric valence band maximum (VBM) in a p-channel TFT and conduction band minimum (CBM) in n-channel TFT should be > 1 eV compared with those of the semiconductor to keep the Schottky emission leakage current sufficiently low.

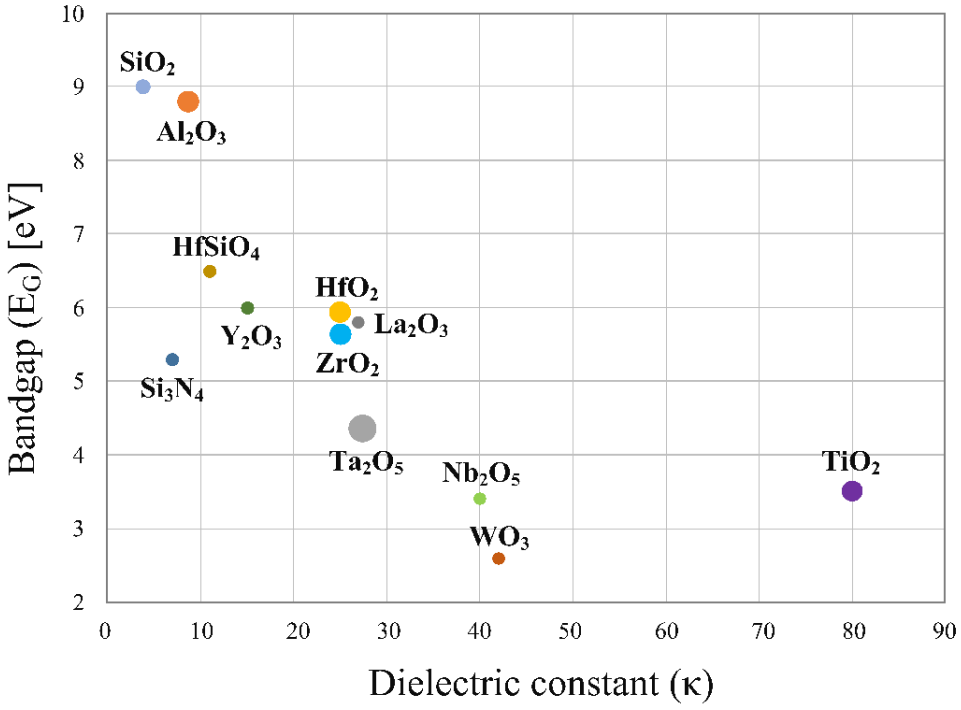


Fig. 2.21. Dielectric constant (κ) vs energy gap (E_G) for the most common inorganic dielectric materials [146].

Material	Dielectric constant (κ)	Energy Gap (eV)	Crystal structure
SiO_2	3.9	9	amorphous
Al_2O_3	9	8.8	amorphous
Ta_2O_5	26	4.4	amorphous
HfO_2	25	5.8	Monoclinic, tetragonal, cubic
ZrO_2	25	5.8	Monoclinic, tetragonal, cubic
Nb_2O_5	40	3.4	amorphous
TiO_2	80	3.5	Tetragonal (rutile, anatase, brookite)
WO_3	42	2.6	Monoclinic, tetragonal, rhombic
La_2O_3	27	5.8	hexagonal
$HfSiO_4$	11	6.5	Tetragonal
Si_3N_4	5–7.5	5.3	Hexagonal, tetragonal
Y_2O_3	15	6	Cubic

Table 2.2. The most important electrical, physical and structural properties of some high-κ inorganic materials [146].

Fig. 2.22 indicates the energy bands of semiconductors and calculated conduction band and valence band offsets of the indicated dielectrics. All values are normalised to the VBM of ZnO, and the dotted line shows the minimum of the 1 eV requirement for the conduction band offset. According to Fig. 2.22, all indicated oxide dielectrics are suitable for p-type

semiconductors, while for n-type semiconductor, only Ta_2O_5 cannot meet the 1 eV requirement. Herein, this issue is addressed, and Ta_2O_5 dielectric is optimised and modified to be used as the gate dielectric in n-type semiconductor TFTs without increasing the gate leakage current.

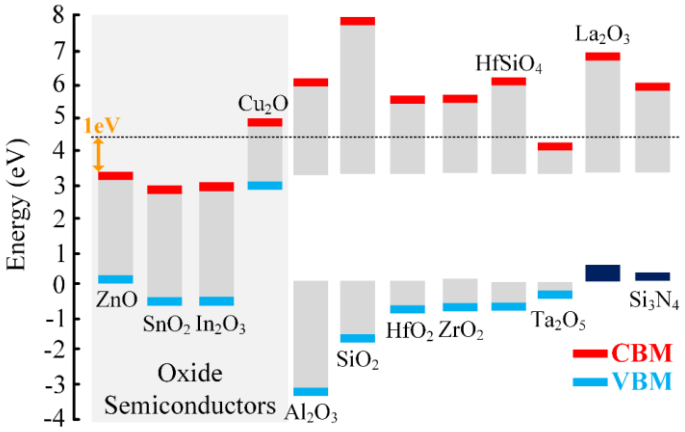


Fig. 2.22. Calculated band offsets of the indicated dielectrics. The values are normalised to the VBM of ZnO. The dotted line indicates the minimum of 1 eV for the conduction band offset [5].

2.3.3.1.1.3 Moisture absorption

Moisture absorption is an essential factor for selecting high-κ dielectrics since good environmental stability avoids degradation in ambient conditions and is also essential for any devices, especially when the device is designed to work as a sensor and exposed to moisture and air or solution processing fabrication is preferred. Metal oxide dielectrics may absorb water precipitated on the surface or from the surrounding air leading to changes in key parameters of the dielectric. Gibbs free energy change (ΔG) for moisture absorption reaction can determine how fast a given oxide dielectric can react with moisture and is calculated by [145]:

$$M_mO_n + H_2O(g) \rightleftarrows M(OH)_n \qquad \text{(Eq. 2.43)}$$

Intrinsically, the moisture absorption phenomenon in high-κ oxides is the reaction between the solid oxide (M_mO_n) film and gas state water (moisture) in the air which can be described by Eq. 2.44:

$$\Delta G = \Delta H - T\Delta S, \qquad \text{(Eq. 2.44)}$$

where ΔH is the enthalpy change, T ambient temperature in Kelvin (K) and ΔS the entropy changes in the reaction. Fig. 2.23 shows the Gibbs free energy (ΔG) of the moisture absorption reactions for most common metal oxide dielectrics. The sign of ΔG indicates whether the reaction is spontaneous or not. In other words, the negative sign of ΔG shows a higher reaction tendency of an MO with water, while positive values of ΔG shows that this process is not thermodynamically favourable. In addition, the larger the absolute value of ΔG, the faster the reaction process occurs [145]. For example, the moisture absorption reaction could not occur on the surface of SiO_2 as the ΔG of the reaction is positive (= 5.9 kJ/mol). On the contrary, ZrO_2 with a negative value (ΔG = −47.1 kJ/mol) is more likely to react with moisture. Furthermore, having a higher moisture-absorption-reaction speed makes ZrO_2 be less stable than Al_2O_3 (ΔG = −9.4 kJ/mol) [145]. Even though most of the metal oxide dielectrics have a tendency to absorb moisture which has a degrading effect on the reliability and stability of devices, several strategies such as doping with a second element and/or surface passivation have been introduced to prevent the dielectric degradation and improve the stability which is discussed in the next sections [121] [147].

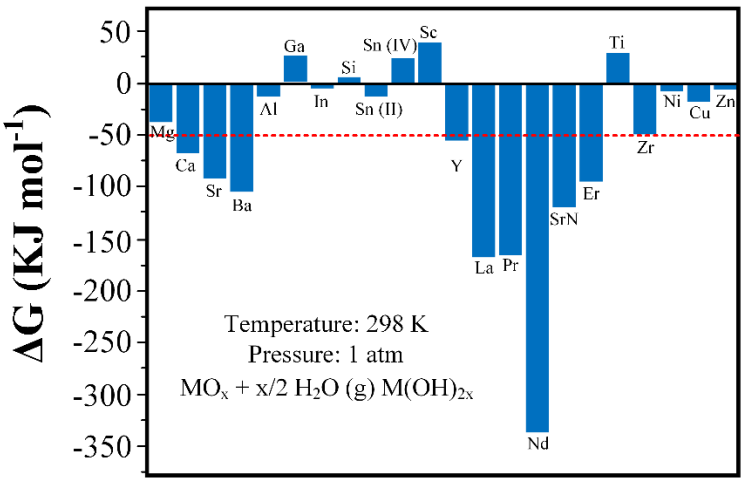


Fig. 2.23. ΔG for the moisture absorption reactions in high-κ metal oxides under standard conditions. The ΔG values are calculated by using HSC Chemistry software [5].

2.3.3.1.1.4 Surface morphology and defects states

The role of the dielectric/semiconductor interface in TFTs is extremely important as charge transport occurs in the vicinity of this interface (only a few nanometres away). Ideally, the dielectric surface should be as smooth as possible, and only a small number of defects is acceptable. Surface defects increase the charge carrier traps and deteriorate the device stability. Therefore, having a high-quality interface is essential to have a stable operation under long-term bias stress. Instability behaviour often observed as threshold voltage (V_{th}) shifts is caused by trapping sites at or close to the dielectric/semiconductor interface. It turns out that in the case of SiO_2, the dangling bonds and hydroxyl groups (-OH) act as charge traps which significantly worsens the TFT performance [148]. For most metal oxide dielectrics, the surface morphology and defect states directly depend on the fabrication process and post-treatment conditions [121].

Although the aforementioned criteria for selecting a proper high-κ oxide dielectric for TFTs are decisive factors in transistor performance, other factors such as process compatibility, solution processability, cost and material toxicity should also be taken into consideration.

2.3.3.1.2 Leakage Current Mechanisms in Oxide Dielectrics

Ideally, dielectrics should show high insulating properties and low conductivity (10^{-20} to 10^{-8} Ω^{-1} cm^{-1}) under electric fields < 1–2 MV/cm. However, considerable current flows through the dielectric layer under a stronger applied electric field (> 3 MV/cm) which depending on dielectric properties. This current (also known as the gate leakage current) is attributed to several conduction mechanisms which are crucial for understanding the dielectric applications. Typically, the mechanisms responsible for conduction in dielectrics are divided into electrode and bulk limited conduction. Electrode limited conduction mechanisms depend on the electrical properties at the electrode/dielectric interface; namely, Schottky or thermionic emission, Fowler-Nordheim (F-N) tunnelling, direct tunnelling, and thermionic

field emission. Bulk limited conduction is related to the dielectric itself, including Poole-Frenkel (P-F) emission, hopping conduction, Ohmic conduction, and grain boundary limited conduction. Fig. 2.24 (a) and (b) show the classification of the conduction mechanisms in dielectrics and the corresponding energy band diagrams, respectively [149].

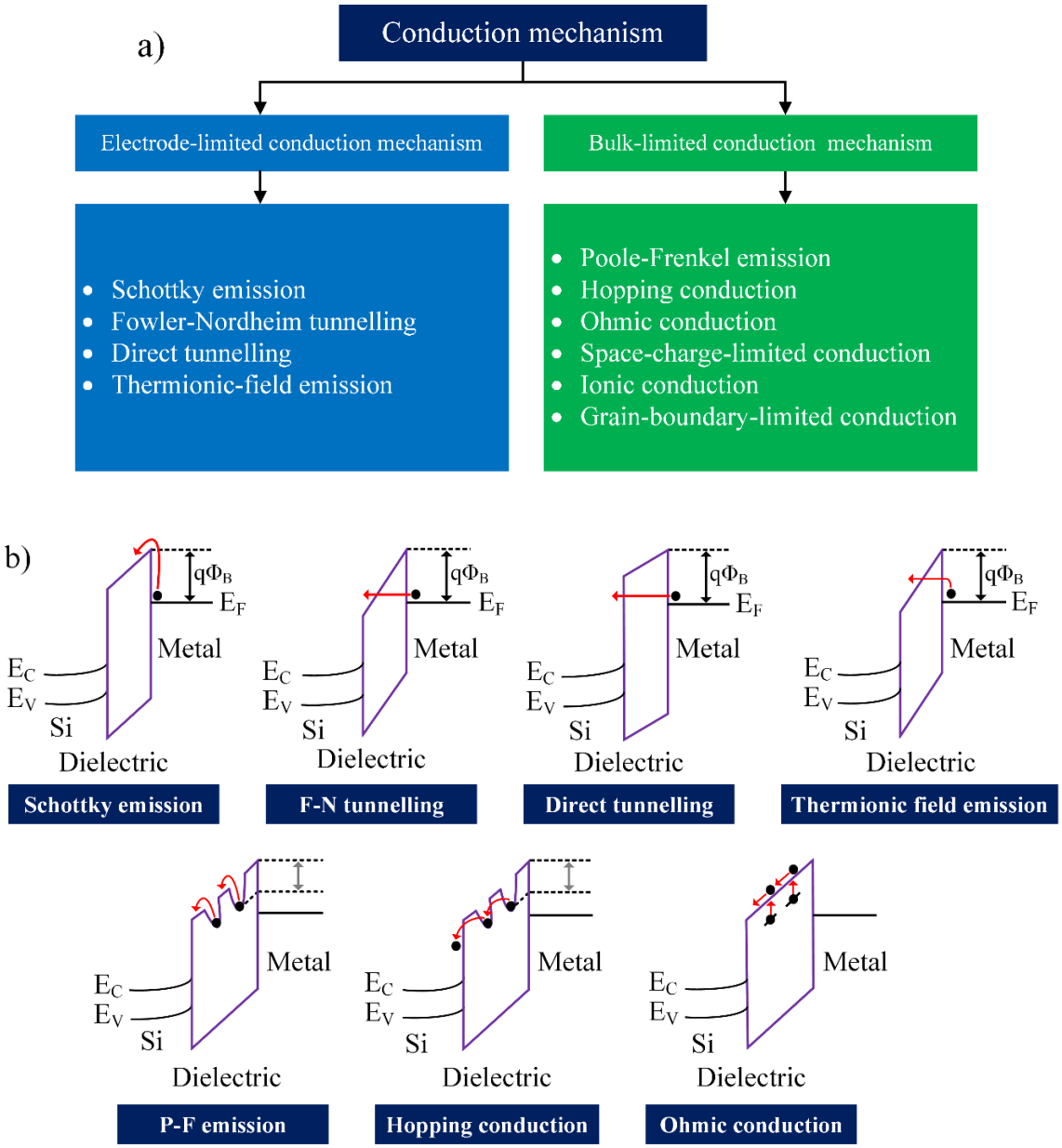


Fig. 2.24. (a) The classification of the conduction mechanisms and (b) their corresponding energy band diagrams.

2.3.3.1.2.1 Schottky (Thermionic) Emission

The theory of Schottky (or thermionic) emission explains how electrons in a metal electrode overcome the energy barrier at the electrode/dielectric interface and are injected into the

dielectric once they have sufficient thermal energy. As a consequence, a depletion layer or electrostatic barrier is generated. The Schottky emission is one of the most observed conduction mechanisms and described by [149]:

$$J_S = A^* T^2 \exp\left[\frac{-q\left(\phi_S - \sqrt{qE/4\pi\varepsilon}\right)}{k_B T}\right], \qquad \text{(Eq. 2.45)}$$

where J_S is the leakage current density, A^* the modified Richardson's constant (= 120 A/cm^2 K^2), T the absolute temperature, q the elementary charge, ϕ_S the Schottky barrier height, E the electric field, ε the dielectric permittivity, and k_B the Boltzmann's constant.

2.3.3.1.2.2 Fowler–Nordheim Tunneling

A sufficiently large electric field (6–7 MV/cm) causes large band bending in the dielectric and provides an opportunity for electrons to breach the triangular band edge of the dielectric. This phenomenon is called Fowler-Nordheim tunnelling and its resultant current expressed as [149]:

$$J = \frac{q^3 E^2}{8\pi h q \phi_{FN}} \exp\left[\frac{-8\pi(2qm_{eff})^{1/2}}{3hE}\phi_{FN}{}^{3/2}\right], \qquad \text{(Eq. 2.46)}$$

where h is Planck's constant, ϕ_{FN} the tunnelling barrier height, and m_{eff} the tunnelling effective mass in the dielectric. This phenomenon is independent on the temperature and decreases exponentially with the dielectric thickness.

2.3.3.1.2.3 Direct tunnelling

Direct tunnelling occurs when the dielectric is very thin (i.e., not much greater than the localisation length, ≤ 5 nm) that allows electrons to directly tunnel across the energy barrier height even at low bias. In other words, the thinner the dielectric is, the higher the tunnelling current becomes. There are two main leakage current conduction mechanisms in SiO_2 films, F-N tunnelling and direct tunnelling. Even though both decrease exponentially with the dielectric thickness, F-N tunnelling dominates when the voltage across dielectric is large

enough (greater than the metal-insulator barrier height [150]), and the thickness of SiO_2 is around 4-5 nm while direct tunnelling dominates for SiO_2 thicknesses less than 3.5 nm dominates at small bias voltages [149]. Direct tunnelling current density can be calculated by [121]:

$$J \sim \exp\left[\frac{-8\pi(2q)^{1/2}}{3h}(m_{eff}\phi_B)^{1/2}kt_{EOT}\right], \qquad \text{(Eq. 2.47)}$$

where ϕ_B is the tunnelling barrier height and t_{EOT} the effective oxide thickness.

2.3.3.1.2.4 Thermionic-Field Emission

Thermionic-field emission intermediately occurs between field emission and thermionic (Schottky) emission. In this situation, the electrons can still tunnel through the dielectric and are injected to the dielectric when they have the energy between the Fermi level of the metal and the conduction band edge of the dielectric. The difference between thermionic emission, thermionic-field emission and direct tunnelling emission is illustrated in Fig. 2.25.

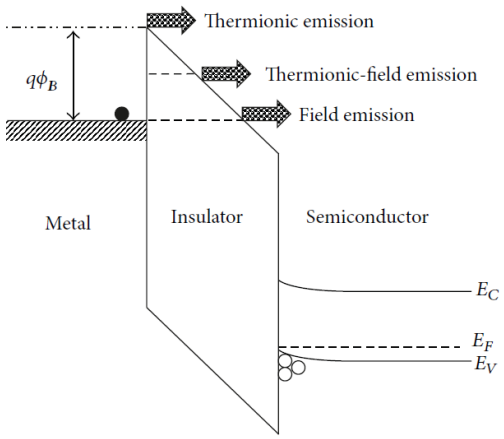


Fig. 2.25. The schematic of different conduction mechanisms: thermionic, thermionic-field emission and field emission.

2.3.3.1.2.5 Poole–Frenkel Emission

The Poole-Frenkel emission reduces a Coulombic potential barrier when it interacts with an electric field and is generally related to the lowering of a trap barrier in the bulk of a dielectric [151]. The P-F emission is analogous to the Schottky emission as it describes how thermally

excited electrons may emit from traps into the conduction band of the dielectric. The current density of the P-F emission ($J_{P\text{-}F}$) can be expressed by [121]:

$$J_{P-F} = q\mu N_C E \exp\left[\frac{-q\left(\phi_T - \sqrt{qE/\pi\varepsilon}\right)}{k_B T}\right], \quad \text{(Eq. 2.48)}$$

where μ is the electronic drift mobility, N_C the density of states in the conduction band and ϕ_T the trap energy level.

2.3.3.1.2.6 Ohmic Conduction

Ohmic conduction is caused by the charge carrier transport—the movement of mobile electrons in the conduction band and holes in the valence band. In this conduction mechanism, the density of current is linearly proportional to the applied electric field. Even though dielectrics typically have a large bandgap (the Fermi level (E_f) is approximately situated in the middle of bandgap (E_G)), still a number of carriers may be thermally excited to the conduction either from valence band or impurity level. Therefore, the current density generated by Ohmic conduction. Although it is very small, it can still be observed even at very low voltages. This current can be expressed by [121]:

$$J = q\mu N_C E \exp\left[\frac{-(E_C - E_F)}{k_B T}\right], \quad \text{(Eq. 2.49)}$$

2.3.3.1.2.7 Hopping Conduction

Hopping conduction is typically a thermally activated electron transfer due to the tunnelling effect of trapped electrons hopping between one trap site or more in dielectric films. In this mechanism, although the energy of electrons does not exceed the potential barrier between two sites, the electrons can still be transferred to the trap sites based on the tunnelling mechanism [58]. The hopping conduction is usually dominant at low fields and moderate temperatures and is expressed by [149]:

$$J = qanv \exp\left[\frac{qaE - E_a}{k_B T}\right], \qquad \text{(Eq. 2.50)}$$

where a is the mean hopping distance, n the electron concentration in the dielectric conduction band, v the thermal vibration frequency of electrons at trap sites, and E_a the activation energy from trap sites to the bottom of conduction band (E_C).

Other conduction mechanisms in dielectrics, such as ionic conduction and grain boundary limited conduction, are usually not important for the dielectric materials in TFTs as the ion mass is large and amorphous dielectrics are desirable in these applications [121].

2.3.3.2 Hybrid self-assembled monolayer/inorganic dielectrics

So far, two methods for lowering the operating voltage of TFTs have been described in detail, namely, using high-κ materials (e.g., metal oxide dielectrics) or thinning the gate dielectric (e.g., either by decreasing the dielectric thickness or utilising SAMs as the gate dielectric). Both strategies have several advantages and disadvantages, and therefore, are used in different applications. In terms of dielectric materials, both oxide and SAM dielectrics have several strengths and limitations, but, in some ways, both can complement each other. On the one hand, metal oxide dielectrics suffer from the presence of charged (pH-dependent) and redox reactive sites on their surfaces which affect the density of charge carriers and increase the trap density at the dielectric/semiconductor interface. This leads to detrimental effects on device performance, particularly on charge mobility (μ) and threshold voltage (V_{th}). However, they typically have a high dielectric constant (κ) and low leakage current density (J_{leak}) [152]. On the other hand, SAM dielectrics suffer from low dielectric constants and leakage-inducing defective sites on the SAM surface, leading to having a low device performance. However, having ultrathin thicknesses (~ 1–3 nm) with the minimal gate leakage current and better compatibility with OSCs makes SAMs to be used as nano dielectrics in low-voltage TFTs. In addition, the presence of water at the dielectric/semiconductor interface has a decisive role in terms of the TFT performance since

the charge carriers (specifically, cations) can be hydrated by water molecules, and consequently increasing their effective mass (decreasing carrier mobility) or assisting the hopping by favourable reorganisation energy (increasing the carrier mobility) via polarisation [141]. For example, in the thin-film SiO_2 used as a gate dielectric, the presence of silanol groups causes high surface tension of the dielectric surface, which depletes charge carriers from the channel. The charge carrier depletion leads to a current decrease and a threshold voltage shift to more negative values in a p-channel TFT. This can be attributed to the bias stress observed in p-channel OTFTs which impedes the reliability and lifetime of OTFTs [141]. Therefore, the modification of metal oxide dielectrics surfaces with SAMs is an effective approach to passivate the dielectric surface and control its surface energy. This approach results in avoiding the dangling bonds which act as charge carrier trap sites, and consequently, enhancing the TFT performance. To have a deeper understanding of passivation process of metal oxide dielectrics, the chemical and physical properties of self-assembled monolayers (SAMs) are described below.

2.3.3.2.1 Self-assembled monolayers (SAMs)

Self-assembled monolayers (SAMs) are ordered, two-dimensional (2D) organic molecular assemblies formed spontaneously by chemical absorption of an amphiphilic surfactant on a variety of substrates. Although SAMs are not part of the nowadays large family of high-κ materials, due to their SAMs nano-scale thickness (~ 2–4 nm), which leads to high gate dielectric capacitance density, they are discussed in this section.

SAMs are one of the most effective and versatile strategies for surface functionalisation. They are comprised of three parts 1) the head group, which is the end of the molecule and attaches to the surface 2) a backbone made of an aliphatic chain—organic compounds comprising of hydrogen and carbon joined together in a straight chain—and/or an aromatic oligomer, typically responsible for the molecular ordering, and 3) the terminal group, which

determines topography, surface energy and chemistry of the outer interface [141]. Fig. 2.26 depicts a schematic presentation of a typical self-assembly molecule.

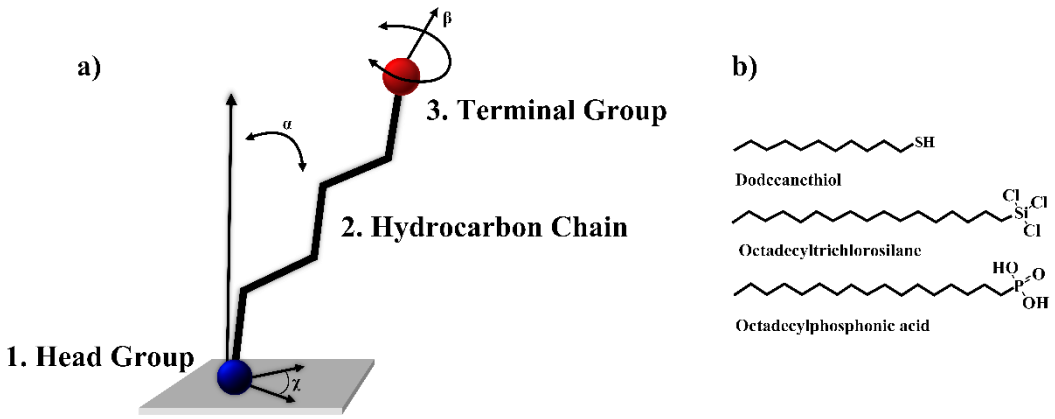


Fig. 2.26. (a) The representative schematic of self-assembly molecule, and (b) three prominent SAMs.

SAMs can be formed on surfaces by deposition from a solution or a gas phase. Interestingly, SAMs can be utilised in different roles in the structure of TFTs. For example, they can be used as a gate dielectric primer, molecular dielectric, organic semiconductor and electrode modifier, as shown in Fig. 2.27. In this thesis, only their role as a surface primer of metal oxide dielectrics is studied.

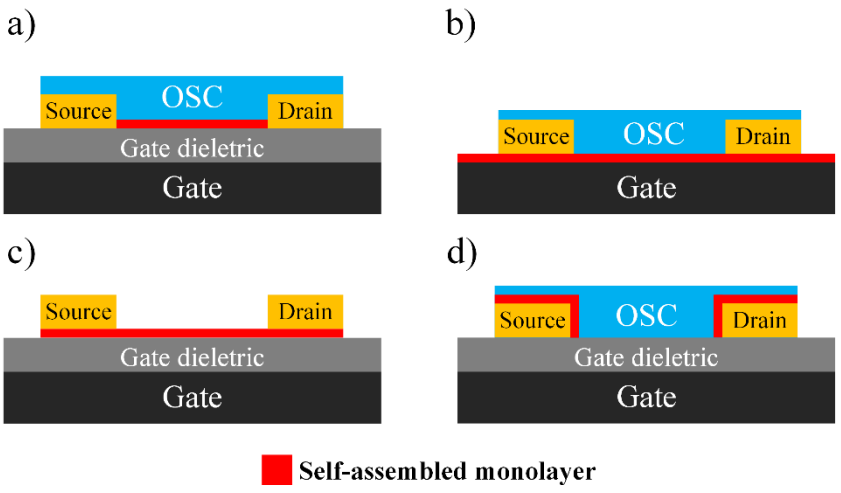


Fig. 2.27. SAMs role in TFTs a) dielectric primer, b) main dielectric, c) semiconductor, and d) electrode modifier.

Depositing a silane SAM onto hydroxyl-terminated metal oxide dielectrics hampers the acid-base and condensation reactions of the silanol groups and terminates electrostatic interaction such as hydrogen bonds [141]. This hydrophobic surface lessens the

electrochemical reactions and increases the resistivity of the surface to water and moisture absorption [153][154]. Therefore, this resistivity to moisture and water molecules makes them proper candidates for applications where device operation under exposure to water or moisture is required. As such, they have been vastly used for surface modification and capping purposes [155][156].

As mentioned before, one promising way to suppress the dielectric surface charge traps in TFTs is to treat its surface with hydrophobic SAMs such as hexamethyldisilane (HMDS) [157], octyltrichlorosilane (OTS) or *n*-octadecyltrichlorosilane (ODTS). Also, regarding the relevant reports [158][159], carrier mobility is significantly improved with increasing the SAM alkyl chain length, i.e., HMDS < OTS < ODTS, in comparison with the untreated surface [160]. It is also shown that SAMs with a longer alkyl chain have stronger adhesion and higher hydrophobicity of the modified surface [161].

n-octyltrichlorosilane (OTS) is a self-assembled monolayer that has previously been shown to have good compatibility with SiO_2 and metal oxide dielectrics. Nowadays, it is typically used as a passivation layer for metal oxides providing capping of polar surfaces or as a hydrophobic coating layer preventing electrical instability of organic semiconductors and OTFTs [58]. Essentially, OTS appears to be one of the most used SAMs in TFTs. It has been reported that OTS significantly improves the dielectric/semiconductor interface in TFTs by passivating the metal oxide dielectric surface. This leads to reducing charge carrier traps, and in consequence, improving charge carrier mobility [160].

During silanization, OTS molecules are attached to the dielectric surface through the chemical reaction of –SiCl with –OH groups on the metal oxide surface. This results in –Si–O–M structures. The other two –SiCl bonds of the OTS molecule react with proximate OTS molecules which forms a cross-linked monolayer (Fig. 2.28).

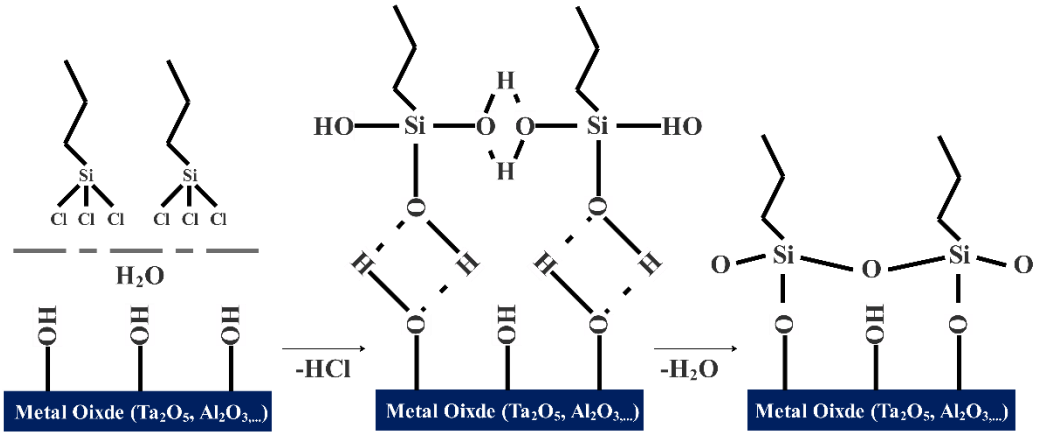


Fig. 2.28. The schematic representation of the silanization reaction.

Apart from the aforementioned beneficial effects of the SAM treatment on the metal oxide dielectrics, in the case of ultra-thin MO layers (d < 10 nm) it also acts as the second (supporting) dielectric layer, which significantly reduces the gate leakage current. However, using SAMs to functionalise the surface of oxide dielectrics is not totally beneficial. Despite their nano-scale thicknesses, using SAMs increases the overall dielectric thickness and reduces the capacitance, which is not desirable. Although this capacitance reduction for thick dielectrics can be negligible, it can be problematic when the main dielectric thickness is on a scale of a few nanometres. Moreover, after thorough investigations of OTS-treated SiO_2 and MOs, it turns out that the OTS surface modification is not quite straightforward as it can easily self-polymerise in ambient conditions which leads to the formation of thick polysiloxane film and large OTS particles which is highly undesirable and against the purpose of the surface modification. Nevertheless, to avoid problems with self-polymerisation, non-polymerising SAMs can be employed [162].

2.3.3.3 High-κ metal oxides deposition techniques

The necessity to substitute SiO_2 with alternative dielectrics causes a pivotal change in chemical processing of this type of materials because they usually cannot be thermally grown on, e.g., crystalline silicon (c-Si). To ensure that the fabricated devices work with their optimal electrical performance, the deposited dielectrics must be as smooth as possible (root-

mean-square roughness (σ_{RMS}) < 1 nm is desired), pinhole-free and have both an excellent thickness uniformity and superior interfacial and bulk properties [163].

The main techniques used for deposition of high-κ oxide materials are atomic layer deposition (ALD), DC/RF magnetron sputtering, plasma-assisted deposition, spin coating/annealing and anodisation which have their own advantages and disadvantages. Selecting an appropriate deposition method depends on several criteria, such as material properties, intended applications, and the deposition/fabrication process costs.

2.3.3.3.1 Atomic layer deposition (ALD)

Atomic layer deposition (ALD), also known as atomic layer epitaxy (ALE), is a popular material deposition method that is a subclass of chemical vapour deposition (CVD) techniques. ALD is a high yield process delivering highly conformal, pinhole-free oxide layers at a relatively low temperature resulting in low leakage current, small hysteresis, and low interface state density metal-oxide-semiconductor (MOS) devices. This makes it an ideal deposition technique for metal oxides, metal nitrides, semiconductors, transparent conductive oxides and ferroelectric materials [163]. In this process, two chemicals react with each other, and the oxide is achieved by repeating sequential, self-limiting surface reactions where precursors are separately deposited onto the substrate [164]. Fig. 2.29 shows the deposition process.

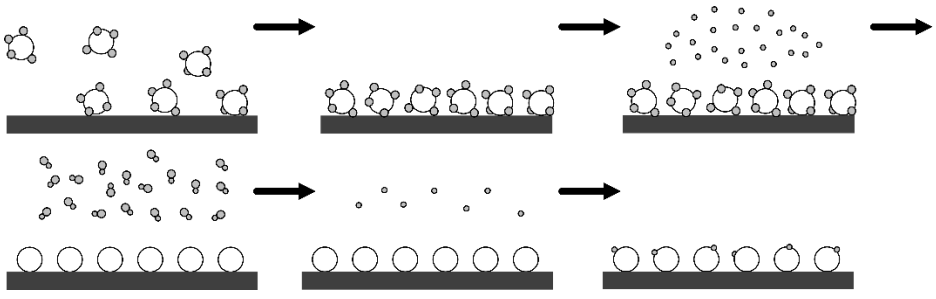


Fig. 2.29. Atomic layer deposition process.

Apart from the aforementioned advantages, ALD offers a precise thickness control in comparison with other vacuum deposition methods as the oxide layer grows per cycle (GPC)

allowing to have a sub-nanometre control over the deposited layer. However, ALD has two main drawbacks. Firstly, owing to the thermally activated surface reaction, the substrate temperatures should be between 275–800 °C, and this temperature is relatively high to be used for plastic substrates. Secondly, several percentages of carbon contaminations in the deposited oxide layer have been reported [165]. The plasma-enhanced atomic layer deposition (PEALD) is the same processing technique but instead of thermally activating surface reaction is using radicals (or ions) produced from a plasma. Since the substrate temperature in PEALD is relatively lower than ALD (50–200 °C), this method can be used for plastics substrates which cannot typically tolerate high temperatures. Owing to the interaction of reactive radicals and ions with the surface, the composition and microstructure of the deposited layer are typically stoichiometric with minimal carbon contamination [166]. Fig. 2.30 demonstrates the schematic of a plasma-enhanced atomic layer deposition system.

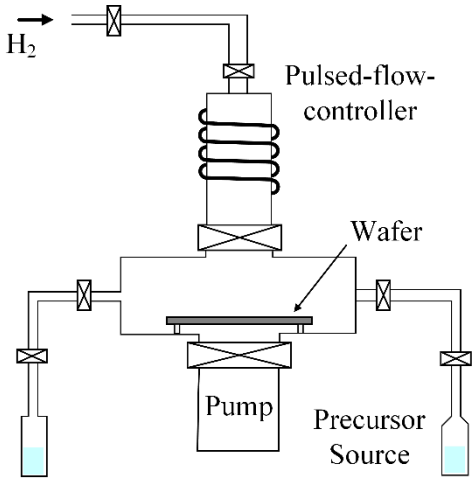


Fig. 2.30. Schematic of a plasma-enhanced atomic layer deposition (PEALD) system.

2.3.3.3.2 Magnetron sputtering

Magnetron sputtering is a high vacuum-based coating method which belongs to the group of physical vapour deposition (PVD) techniques. The sputtering deposition of high-κ oxide materials is typically based on the metal oxide or metal target being bombarded by an inert plasma (partially ionised gas, e.g., Ar) or a mixture of inert gas and oxygen plasma (e.g.,

Ar/O_2) [166]. For example, deposition of Ta_2O_5 can be attained by both reactive sputtering methods where a tantalum metal target is sputtered in the presence of oxygen/argon plasma or a Ta_2O_5 target directly sputtered in an argon plasma [167]. The process begins when a voltage is applied to the target by means of a different potential difference (pulsed DC) or electromagnetic excitation (magnetic field (MF), radio frequency (RF)) in the presence of pure argon gas. In this situation, plasma is created by ionisation of Ar in the surrounding of the target, and Ar^+ ions start to accelerate and bombard the target atoms due to magnetic field. This bombardment leads the atoms to be sputtered off into the plasma and projected to the substrate. Then these vaporised atoms condense on the sample and form a thin layer. In order to properly deposit sputtered materials, several process parameters should carefully be considered. Firstly, the distance between the samples and the target should be optimised. Secondly, the chamber pressure should carefully be controlled to get the best quality of the deposited films and avoid contamination caused by the residual gases. Last but not least, the applied sputtering power should not exceed the maximum value for a given material because higher applied power could result in the target damage and poor quality of the deposited films. DC magnetron sputtering has two main limitations; first, it can only be used for electrical conductors due to the opposite field build up and second, it offers low sputtering rate attributed to low ionisation of argon atoms. Therefore, radio frequency (RF) magnetron sputtering is typically utilised for the deposition of dielectric and semiconductor materials. The RF sputtering has other benefits, including lower temperature processing and higher sputtering rate in comparison with the DC sputtering (ca. 10 times higher) due to the oscillating electrons in the area of the plasma. Usually, for Ta deposition RF magnetron sputtering is performed in the optimum pressure of $P = 5\times10^{-3}$ mBar, samples are 10 cm apart from the target and power does not exceed 70 W. Fig. 2.31 demonstrates a schematic of the RF magnetron sputtering deposition process.

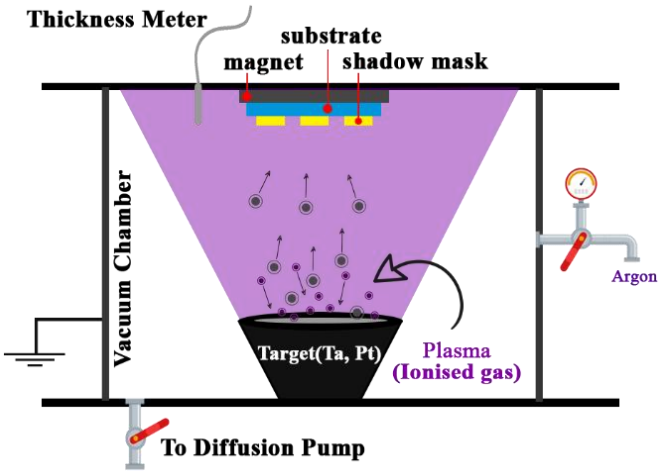


Fig. 2.31. Schematic of the RF magnetron sputtering process.

2.3.3.3.3 Plasma Oxidation

Plasma oxidation is a widespread vacuum-based oxidation technique whereby surfaces are oxidised in an oxygen gas discharge via active and neutral charged oxygen species and typically used for growing of native oxides on metals or semiconductors. It has recently drawn a lot of attention in the microelectronics industry, where low temperature and dry processing are required. In this process, the surface of a substrate is continuously bombarded by both positively and negatively charged plasma particles as well as neutral oxygen species in the absence of a potential bias. As a result, the surface is oxidised to only several angstroms because of low energy implantation, diffusion and subsequent chemical reactions [168]. Therefore, oxidation of metals up to 2 nm is generally a straightforward process, but deeper oxidations are difficult to produce since the initial layer shields further oxidation. Nonetheless, growing oxide to further thicknesses (up to 1 μm) can be achieved by applying positive bias in respect of the plasma to collect the negatively charged oxygen species [168]. It has been found out that the main factors which can control the process are RF power density, oxygen pressure, and substrate temperature. Importantly, oxygen plasma is also widely used for cleaning, etching and removing unwanted organic residues from surfaces [169]. Hsiao *et al.* have shown that high-quality Al_2O_3 and Ta_2O_5 can be successfully grown by plasma-assisted oxidation in a controlled environment [165].

2.3.3.3.4 Solution-based techniques: spin/dip coating

Spin-coating has been widely utilised to fabricate thin, uniform, and smooth dielectric films on flat substrates. This technique does not only offer a simple, inexpensive and low-temperature processing but also can be applied in ambient conditions without the need for vacuum or chemical delivery systems. Therefore, it is commonly used in applications where low-cost and low-temperature processing are the two main concerns (e.g., flexible, organic sensors, oxide dielectrics, etc.). Its simplicity is also suitable for nanoparticle-based material processing, allowing for low-cost and rapid deposition of oxide films [170]. Other main advantages include good reproducibility and technological compatibility with conventional microfabrication techniques. However, this fabrication process suffers from somewhat limited scalability and incompatibility with roll-to-roll (R2R) processing for large-area deposition. Furthermore, most of the sprayed solution (ca. 95%) is wasted during this deposition process. The spin coating process can be divided into four stages: deposition, spin-up, spin-off, and evaporation. In this process, the solution is first deposited at the centre of a substrate, and then, in the spin-up stage, it is accelerated rapidly to a desirable spin speed. Following that, the solution starts to flow outward due to the centrifugal force radially. In the spin-off stage, the excess solution is pushed over the edge and spun off from the substrates as droplets. Ultimately, the solution dries and forms a thin film. Fig. 2.32 shows the schematic of the (a) spin and (b) dip coating processes, respectively. Depending on the acceleration, speed of spinning and the viscosity (concentration) of the solution, the thickness of the deposited layers can be precisely controlled and varied between few nanometres and several micrometres [171].

Dip coating is the simplest method of thin-film deposition of a chemical solution at a fast rate with precise control and is widely used for large-area deposition. The process is easily begun by dipping the substrate into the solution for a certain time and then withdrawing the substrate at a constant speed. At the dipping stage, the solution homogenously and naturally

stretches on the submerged substrate by the mutual effect of capillary rise and viscous pull. Ultimately, after taking out the substrate from the solution, solidification takes place by natural or forced evaporation (e.g., hot plate). Apart from different scalability, the main difference between dip and spin coating is that the thickness of the deposited film can be thinner and more precisely controlled in the spin coating by spinning acceleration, speed and time. A complete solution deposition system typically consists of a spin/dip coater, a hot plate or a thermal oven, an ultrasonic cleaner, and a UV curing system [166].

a)

b)

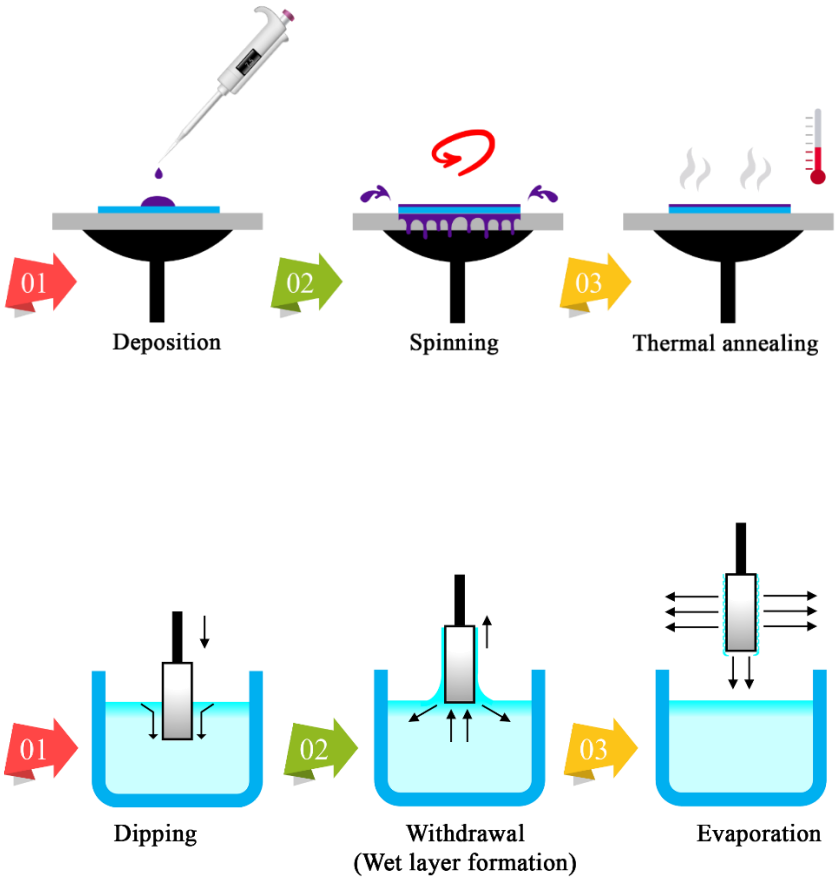


Fig. 2.32. Schematic of (a) the spin coating and (b) dip coating processes.

2.3.3.3.5 Anodic oxidation (Anodisation)

One of the most reliable approaches to form oxide dielectrics is electrochemical oxidation (so-called anodisation). Anodisation represents a simple, cost-efficient and straightforward method to grow metal oxide layers on the surface of metallic substrates and is now widely utilised in both academia and industrial scales. In other words, anodisation is an electrolytic passivation process which allows increasing the thickness of the natural oxide film and

forming a stable oxide with negligible reactivity. Although the stability of the oxide film depends on several factors such as the purity, structure and the oxidation process of the metal, as well as the formation, type and composition of the adjoining phase of the oxide, anodisation generally offers excellent insulating properties such as low leakage currents and high breakdown field strengths when compared with other metal oxidation techniques [172]. Herein, anodisation has been investigated in more detail as it has been used for the growing of oxide layers employed as gate dielectrics in the fabricated TFTs.

2.3.3.3.5.1 Background

Several valve metals such as Al, Ti, and Ta have a very high chemical affinity with oxygen. Consequently, even under ambient conditions, these materials can rapidly react with the oxygen and form a "native oxide" on their surfaces. The "air-formed" oxide film preserves the metals from further oxidation (i.e., oxidation of the underlying metal bulk) by impeding atmospheric oxygen to react with the metal. This passive layer is extremely thin; its thickness depends on the temperature, pressure, humidity and exposure time and varies from a few angstroms to several nanometres (e.g., aluminium oxide (Al_xO_y) grown on Al surface when exposed to air at normal temperature for 2 hours is about 10 Å and after about one month, increases to 45 Å [173]). Moreover, native oxides are very often not homogenous in thickness and can contain numerous defects and flaws. The native oxide can be somewhat beneficial for specific applications such as preventing corrosion, which is a component of oxidation, and usually one of the most deleterious ones. Corrosion is a natural process that decays the properties of a metal, affecting its structure, appearance, strength and permeability. As much the corrosion is an undesirable part of oxidation, controlled growth of oxide layers underpins many of electronic devices which shape modern technology. However, the native oxide is neither formed in controlled conditions nor can be reliably used in terms of mechanical and chemical protection due to its extremely thin layer (in the case of Al and Ta, the thickness of their native oxides around are 4–5 nm [174] and 3–4 nm [175],

respectively). Therefore, several methods have been developed to improve the surfaces of metals with a hard and adherent oxide coating.

Research on anodic oxidation firstly started in 1857 [176] when H. Buff observed that Al could be coupled with Pt in the presence of dilute sulfuric acid and anodically oxidised. Although the investigation on anodic oxidation since then has been significantly progressed, the first commercial use of anodisation dates back to 1926 after it was patented by National Physical Laboratory [177] where it was employed to form an oxide layer on aluminium and its alloys in the range of nanometres to microns. It turned out that this oxidation method could be used to improve corrosion resistance and dye the metal surfaces [178]. In 1934, Güntherschulze and Betz published their seminal work on investigations of ion mobility in anodically formed Al and Ta oxides [179]. This research was conducted to present the formation mechanism of barrier type anodic films in electrolyte without solvent action (the thickness is typically below 1 μm). Nonetheless, in the following decades, the use of anodisation had been quite limited for depositing of vertically oriented, highly ordered, and densely packed porous oxide layers [180]. This method then was adopted for several other valve metals such as Ti [181], Ta [182], Ga [183], Hf [184], Mo [185], W [186], and Zr [187]. In recent years, it has been found out that barrier type anodisation is a promising oxidation method which can be used in electronic industries to deliver high-quality high-κ oxide films for electronic components such as capacitors, transistors, diodes, and memory devices [180].

2.3.3.3.5.2 Types of anodic oxide films

Anodisation films can be classified according to the physical morphology of the formed oxide under two main types, namely, barrier and porous oxide films (Fig. 2.33). Ideally, barrier type oxides are nonporous, compact, and conformal in terms of their thickness with electronic and ionic conductivity at high electric field strengths and virtually exclusively

used in electronics manufacturing as dielectrics and passive protective films. Porous type oxides are composed of a thin barrier layer at the metal/oxide interface beneath an outer porous layer with regular structure and low resistance and typically used in cosmetic applications either as a protective layer against corrosion or a coating layer to improve the adhesion of the surfaces for painting and dyeing purposes [188]. Porous anodic oxide films are also used in a wide range of technological and biological applications due to their high surface-to-volume ratios and size-dependent properties [180][189]. The porous type oxide layer can be tuned in terms of porosity characteristics such as nanopore diameter, length, thickness, spatial density by the chemical composition of the electrolyte, temperature, applied voltage or current density and time while the thickness of barrier type oxide film is determined by the applied bias and time. Even after the initial growth of the barrier type oxide, its thickness becomes independent of the anodising time. In comparison with porous type oxides, barrier type oxides can offer impervious, amorphous, smooth, compact, high resistance (10^{10} – 10^{12} Ω·m) and less defective anodic oxide films. This type of anodic films are highly desirable for utilising in electronic devices to realise high-κ, high capacitance, high dielectric breakdown strength and low hysteresis dielectric layers [189].

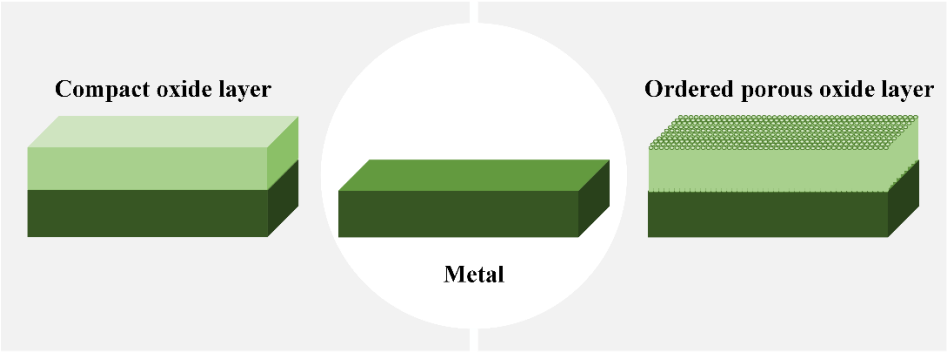


Fig. 2.33. Different morphologies of barrier and porous type oxide layers formed by anodisation of valve metals.

2.3.3.3.5.3 Types of Electrolyte

It is reported that the parameters of electrolyte solutions such as the concentration of reagents, level of pH and temperature used for anodisation play a decisive role in the determination of the morphology of the oxide grown on the metal surface and decide if the

oxidised films are the barrier or porous type [189]. In addition, electrolytes with aggressive ions (low pH) such as sulfuric, oxalic, chromic, hydrofluoric acids and sodium hydroxide have a moderate ability to dissolve oxide layers (it also depends on several other factors, e.g., the metal base itself) and therefore are widely employed to form porous type oxide films. On the other hand, neutral electrolytes with a pH level between 5–7 such as neutral boric acid, phosphonic acid, ammonium borate, tartrate, and ammonium tetraborate in ethylene glycol under a low applied bias (< 40 V) can be used for barrier type anodic oxidation [190]. In this thesis, a highly dilute citric acid (1 mM) has been used as an electrolyte for the anodisation process to form pinhole-free, compact, barrier type oxide layers. Surprisingly, barrier type oxide layers can be performed in high purity deionised water with no added electrolyte. However, this requires the application of much higher voltages to overcome the high resistance of H_2O (R_s > 18 MΩcm) and the processing time increases significantly. In fact, it has been shown that there is no measurable difference between the oxide layer grown in pure water or very diluted citric acid as an electrolyte [191]. Therefore, to lower the anodisation voltage and time, it is more convenient to anodise in weak dilute acids. It is worth mentioning that the anodisation ratio (c_A [nm/V])—the ratio that describes how many nanometres the oxide thickness grows per volt—depends on the concentration and type of electrolytes and typically varies based on different electrolytes. For instance, the anodisation ratio of tantalum which has been reported in the literature [192][193][194][195] is usually between 1.8 and 2.2 nm/V. Table 2.3 compares the information relating to the anodisation of metals, and in particular anodisation of tantalum, in the recent works [192]–[197].

Ref.	Metal oxide	Anodisation ratio (nm/V)	Forming Electrolyte
[192]	Ta_2O_5	1.8	0.1 M H_3PO_4
[193]	Ta_2O_5	2.2	0.01 M CA
[194]	Ta_2O_5	2.0	0.01 M CA
[195]	TiO_2	1.5	0.001 M CA
[160]	Al_2O_3	1.3	0.001 M CA

Table 2.3. A summary of anodisation ratios and forming electrolytes relating to the anodisation of Al_2O_3 and Ta_2O_5. CA – citric acid.

2.3.3.3.5.4 Materials for Anodisation Process

Anodisation can take place on the surface of valve metals (Nb, Ta, Al, Zr, Hf, Bi, Sb, etc.), valve metal alloys (Al–Nb, Al–Tb) [198][199] and semiconductors (ZnO, CuO, NiO). The name of valve metals was firstly used by the early researchers in the field to emphasise the rectifying action of high resistance oxide formed on these metals under anodic polarisation (i.e., they do not "pass" current in both directions). This rectifying action occurs as long as the polarisation voltage is lower than the oxide formation potential, yet ionic current is expected to flow for a higher potential leading to an increase in the thickness of the film. Among all valve metals, Ta has been widely studied for over 60 years and is used as an alternative dielectric in various applications, particularly in p- and n-channel thin-film transistors (TFTs), capacitors and dynamic random access memories (DRAMs) owing to its high dielectric constant, high capacitance, high dielectric breakdown strength and relatively high bandgap [164]. As mentioned before, in order to realise low operating voltage TFTs it is essential to utilise a high dielectric constant dielectric. Therefore, in this study, barrier type anodic tantala films have been used to achieve this goal. In the following section, the methodology of this approach is discussed in detail.

2.3.3.3.5.5 Anodisation process

The preparation of anodically oxidised films does not differ from those used for electrolysis. Typically, it is carried out using a two-electrode electrochemical cell with the metal expected to be oxidised as the anode and an inert metal such as Au, Pt or stainless steel as the cathode. In terms of electrolyte, a variety of solutions can be used for anodisation; however, as previously mentioned, the nature of the electrolyte determines the type of anodic oxide film and therefore, herein, the electrolytic cell is filled with a very dilute citric acid (1 mM) solution to form a barrier type anodic tantalum oxide (Ta_2O_5). Fig. 2.34 displays a typical anodisation set-up to perform the oxidation. Although recent practice shows that anodisation of metals can take place in both potentiostatic and galvanostatic modes, it has

been shown that much better barrier type anodic oxides are only formed by galvanostatic mode (constant current), while potentiostatic mode is widely used for growing porous type oxides [180]. When a constant current is applied between the anode and cathode electrodes, reduction and oxidation (redox) reactions occur in the electrochemical cell, and a field-driven ion diffusion conduces to the formation of the oxide layer on the anodic surface. During anodisation of Ta to form anodic Ta_2O_5, the redox reactions can be represented by the following equations [195]:

Anode: $$2Ta + 5H_2O \rightarrow Ta_2O_5 + 10H^+ + 10e^-$$ (Eq. 2.51)

Cathode: $$2H^+ + 2e^- \rightarrow H_2 \uparrow, 2O_2 + 8H^+ + 8e^- \rightarrow 4H_2O$$ (Eq. 2.52)

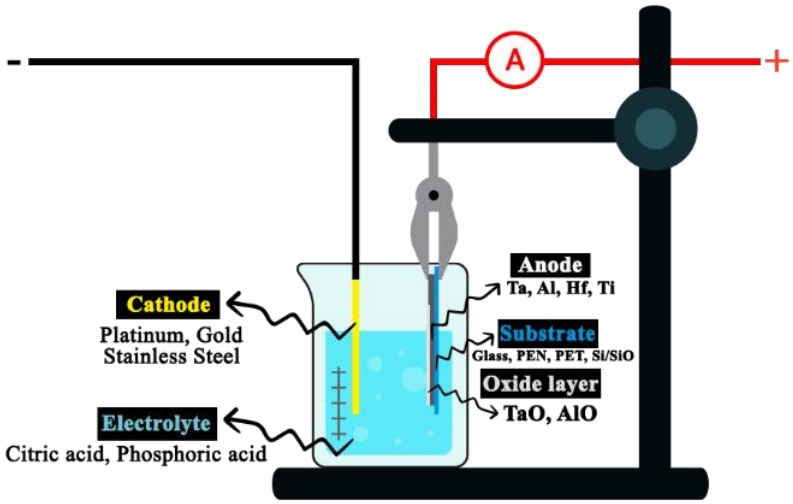


Fig. 2.34. The schematic diagram of the electrochemical cell set-up for the anodisation process.

2.3.3.3.5.6 Ionic migration in anodic oxide films

It has been shown that the anodic oxide film formed on the surface of Ta grows linearly with increasing electrode potential by high-field ion migration in the film [200]. In fact, during anodisation, oxygen-bearing ions (O^{2-} and OH^-) migrate inward from the oxide-electrolyte interface, whereas metal ions migrate outward from the metal-oxide interface and once reaching the oxide-electrolyte interface, they can contribute to the oxide growth or can be ejected to the electrolyte. In other words, the formation of the oxide layer can be summarised in three steps: (1) formation of metal ions at the metal-oxide interface, (2) reaction of metal ions with O^{2-} (and far less with OH^-) (3) outward migration of Ta^{5+} ions

and inward migration O^{2-} ions through the oxide layer under the applied high electric field [180] as illustrated in Fig. 2.35.

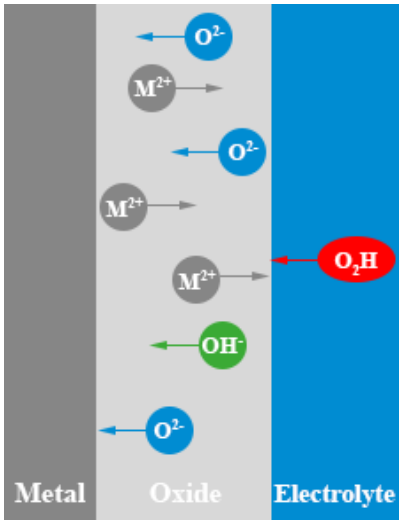


Fig. 2.35. The representative schematic of the migration of ions through the oxide layer under the applied high electric field during the anodisation process.

2.3.3.3.5.7 Kinetics of barrier type oxide growth

The ionic current density (j_{ionic}) is comprised of the movement of metallic cations ($j_{m\text{-}cat}$) and oxidising anions ($j_{ox\text{-}an}$) under a given electric field across the metal/oxide and electrolyte/oxide interfaces, respectively. Although the total current that flows through the electrochemical cell also includes the leakage current (I_{leak}) through the pre-formed initial oxide film and the current contributed to the dissolution of the anodic oxide layer (I_{diss}), both currents can be neglected as the former is sufficiently low and the latter is negligible for the barrier type anodic oxide film and typically taken into account for porous type anodic oxide films. The efficiency of barrier type anodisation process (η) is defined as the contribution of the ionic current in the growth of barrier type oxide layer in comparison to the other generated currents and determined by [189]:

$$\eta = \frac{I_{ionic}}{I_{ionic} + I_{leak} + I_{diss}}, \qquad \text{(Eq. 2.53)}$$

As I_{ionic} is dominant for the barrier type oxide layer, the efficiency of the anodising process reaches almost 100% [189].

In 1937, Güntherschulze and Betz established an investigation on ionic conductivity in anodically formed Al and Ta oxides [201] which has been observed in many anodising experiments afterwards. It was found that there is an exponential dependence of the ionic current on the high electric field and that the ionic current can be determined by the following equation [180]:

$$j = j_0 \exp(\beta E) = j_0 \exp\left(\beta \frac{\Delta U}{d}\right) \quad \text{(Eq. 2.54)}$$

$$E = \frac{\Delta U}{d} = \frac{U - U_0}{d}, \quad \text{(Eq. 2.55)}$$

where j is the ionic current density, E the electric field, j_0 and β material-dependent constants at a given temperature, ΔU the potential drop in the oxide layer, U the formation potential, U_0 the equilibrium potential, and d the film thickness. Two possible rate-determining steps can be considered during anodisation: ionic transport across the metal/oxide interface and ionic transport across the oxide. The ionic current density can be dominated by either the metallic cations due to a large electrolyte/oxide interface potential barrier which impedes oxygen anions to transport through the bulk oxide or oxidising agent anions due to a large energy barrier at the metal/oxide interface which is similar electrolyte/oxide potential barrier but obstructs the metallic cations.

The ionic current density across the metal/oxide interface has been modelled by Mott and Cabrera [189]. In their model, metallic cations need a strong electric field to overcome the potential energy barrier and therefore, to transfer across the metal/oxide interface. This ionic current is then formulated by:

$$j = nv \exp\left[\frac{-(W - zae)}{k_B T}\right], \quad \text{(Eq. 2.56)}$$

where n is the ions density at the metal/oxide interface, v the frequency of atomic vibration, k_B Boltzmann's constant, T the temperature, z the valence of the mobile ions, e the elementary charge, W the potential barrier height, and a the activation distance.

Verwey investigated the ion current density where the ions transport through the bulk oxide is dominant [202]. On the contrary to Mott and Cabrera, the activation distance (a) and barrier height (W) are not referred to the metal/oxide interface but bulk oxide. In this model, the ionic current density can be determined by [189]:

$$j = j_0 \exp(\beta E - \gamma E^2), \qquad \text{(Eq. 2.57)}$$

where γ is the electrostriction coefficient, E is the electric field, and j_0 and β are material dependent constants.

As abovementioned, the number of metallic cations ($t_M{}^{n+}$) and oxidising agent anions ($t_O{}^{n-}$) migrated across the metal/oxide, and electrolyte interfaces are playing a decisive role in the growth of the oxide film and thus determines the rate of oxidation. It is also noteworthy that the number of cations and anions transferred in the oxide layer is not the same, and therefore, the charge transport differs for different metals and process conditions [189]. In particular, the number of these cations and anions are dependent on the height of the energy barrier (W) at their corresponding interfaces and therefore, the contribution rate of each group of ions directly affects the anodisation process and depending on the transport number of metal cations in comparison with the transport number of O^{2-}, the oxide layer can be mainly grown at the inner (in the near vicinity of the metal-oxide interface) or outer (in the near vicinity of oxide–electrolyte interface), respectively (Fig. 2.36 (a, b)).

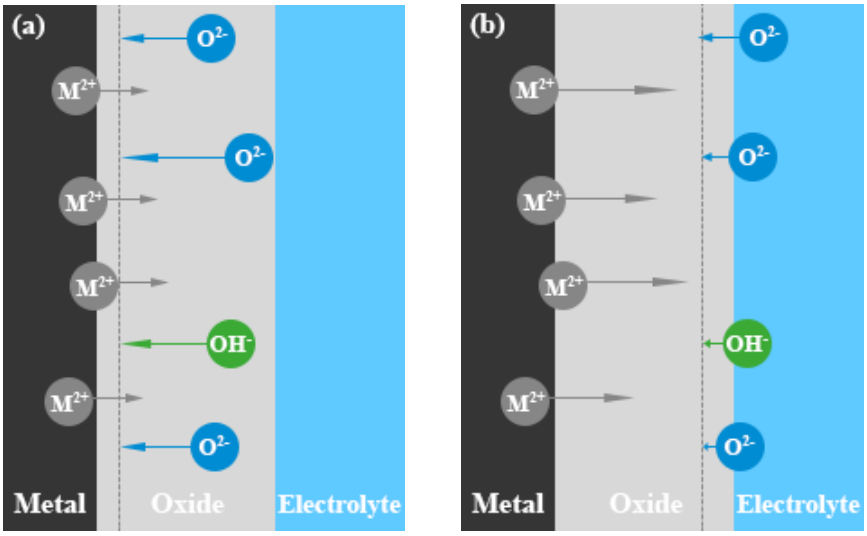


Fig. 2.36. The representative schematic of the anodisation process where (a) inward anionic transport is dominant, and (b) outward cationic transport is dominant.

It has been reported that for Ta, both types of ions contribute to ionic current and the oxide growth occurs at both the metal–oxide and the oxide–electrolyte interfaces [203]. The ratio metallic cations and oxidising agent anions can be defined by [189]:

$$t_{M^{n+}} = \frac{i_{M^{n+}}}{i_{M^{n+}} + i_{O^{n-}}} \quad \text{(Eq. 2.58)}$$

$$t_{O^{n-}} = \frac{i_{O^{n-}}}{i_{M^{n+}} + i_{O^{n-}}}, \quad \text{(Eq. 2.59)}$$

where $i_M{}^{n+}$ and $i_O{}^{n-}$ are the currents resulted from the movement of metallic cations and oxidising agent anions, respectively.

2.3.3.3.5.8 Anodic oxide growth ratio

As previously discussed, the growth rate of the oxide layer ($\frac{\partial d}{\partial t}$) is determined by j_{ionic} which itself is dependent on the electric field strength ($\frac{\partial U}{\partial t}$). In order to have a constant current through the anodic oxide, it is required to have a constant and uniform electric field strength. This means that the change rate of electric potential increasing should be linear, leading to a formation of oxide at a constant rate. Therefore, since both the oxide growth rate and change

rate of electric potential are both linear, a proportionality factor can be defined to describe this correlation [189]:

$$\frac{\partial d}{\partial t} = C_A \times \frac{\partial U}{\partial t}, \qquad \text{(Eq. 2.60)}$$

where C_A is a material-dependent constant, which is referred to the anodisation ratio. Moreover, it turns out that in the galvanostatic mode (constant current), the thickness of the oxide layer depends only on the cell voltage, which is allowed to rise to the required value [42]. In order words, the thickness (d) of the resulting films can be precisely controlled via anodisation voltage V_A and Eq. 2.60 can be rewritten to $d = C_A \cdot V_A$ where C_A is the anodisation ratio describing the thickness of the formed film per applied volt (Å/V). Importantly, C_A is related to the electric breakdown field E_B via $E_B \approx C_A^{-1}$ [42].

Fig. 2.37 illustrates the electric drive conditions for anodisation in constant current mode (I_A = const.). The anodisation current I_A is kept constant via the anodisation voltage V_A compensation until the desired voltage is achieved and then decreases to very low values. The "leakage current" flowing under constant voltage conditions is electronic, but if the voltage is increased, then ionic current starts to flow again with further film formation until a new equilibrium is established. However, it is not possible to increase the voltage to a very high value, and the thickness of the film is limited by a breakdown which occurs when a certain range of potential is reached (e.g., for a 1 µm thick Al_2O_3 is in the range of 500 V–700 V [204]). The oxide breakdown is described by sparking, oxygen evolution, and the formation of thick, discoloured films [205]. The most interesting fact is that the thickness of the barrier type film is not affected by anodising time, surface roughness and temperature of the electrolyte. In fact, the formed oxide film will exactly follow or slightly smooth out the initial surface topography of the anodised metal.

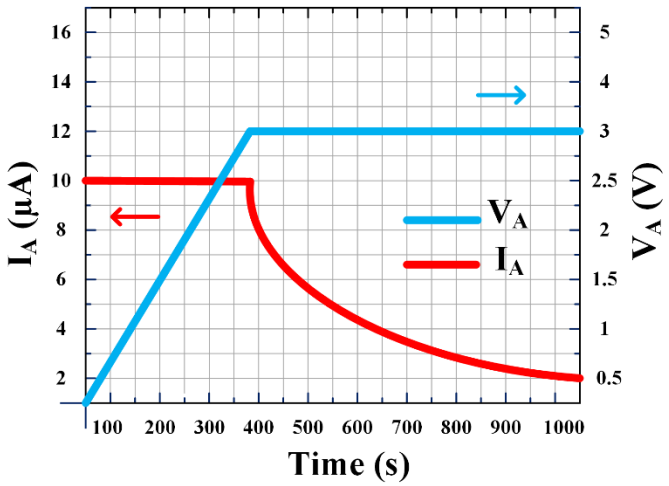


Fig. 2.37. Anodisation voltage (V_A) and anodisation current (I_A) vs anodisation time (t).

2.3.3.3.6 Metal oxide dielectrics in low-voltage TFTs

Several alternative metal oxides (e.g., Al_2O_3, HfO_2, Ta_2O_5, ZrO_2, TiO_2, Y_2O_3, CeO_2, etc.) have been investigated to be used as a gate dielectric in organic and inorganic TFTs [206][207][208]. Herein, a review on the recent TFTs gated by Ta_2O_5 reported in the literature.

2.3.3.3.6.1 Tantalum oxide (Ta_2O_5)

As discussed, Ta_2O_5 can be grown using different methods, namely, thermal oxidation, plasma-assisted oxidation, RF sputtering, atomic layer deposition and anodisation. Bartic *et al.* reported low-voltage P3HT OTFTs using a 100 nm film of Ta_2O_5 deposited by e-beam evaporation as the gate dielectric [35]. Although the fabricated OTFTs are able to operate around −3 V, they suffer from positive threshold voltage (V_{th}) and low mobility in addition to costly fabrication processes. Sakai *et al.* proposed pentacene OTFTs using a 130 nm sputtered Ta_2O_5 [36]. Even though it can operate at −3 V with a small V_{th} (−0.3 V), the drain current on-off ratio (I_{ON}/I_{OFF}) is 66, which makes it unsuitable for real applications. Recently, Chiu *et al.* have used a 200 nm e-beam deposited Ta_2O_5 for amorphous indium-gallium-zinc oxide (a-IGZO) TFTs which operated at 3 V with high mobility of 61.5 $cm^2 V^{-1} s^{-1}$ [209]. Although all OTFTs and TFTs reported in the recent year have been continuously improved in terms of the key parameters and performance, almost all of them typically used a thick Ta_2O_5 dielectric ($d \geq 100$ nm) and costly or incompatible deposition techniques with

large-area electronics. Furthermore, their thick Ta_2O_5 gate dielectrics impede TFTs to operate at or below 1 V which required for the applications such as portable, ultra-low power electronics or aqueous sensors. Table 2.4 shows the recently reported transistors employing a sole Ta_2O_5 film as the gate dielectric.

Ref.	Dielectric	d (nm)	V_G (V)	V_{th} (V)	Semiconductor	μ ($cm^2 V^{-1} s^{-1}$)	I_{ON}/I_{OFF}
[35]	Ta_2O_5	100	~ −3	+0.26	P3HT	0.02	–
[36]	Ta_2O_5	130	~ −3	−0.3	Pentacene	0.8	66
[209]	Ta_2O_5	200	2	0.25	a-IGZO	61.5	10^5
[210]	Ta_2O_5	100	2	0.18	a-IGZO	–	10^6
[211]	Ta_2O_5	125	5	1.6	IZO	17	10^7
[212]	Ta_2O_5	150	10	−2.5	ITO	28.8	~ 10^8

Table 2.4. Low-voltage transistors using Ta_2O_5 as the gate dielectric.

2.3.3.3.6.2 Organic-inorganic hybrid dielectrics in low-voltage TFTs

To improve the TFT performance, several research groups have reported the organic-inorganic bilayer or multilayer dielectrics (also known as hybrid and high-κ/low-κ dielectrics) for low-voltage OTFTs. Fujisaki *et al.* reported a low-voltage pentacene OTFT used to drive flexible LCD panels with fast response [213]. They treated the surface of Ta_2O_5 with hexamethyldisilane (HMDS) to improve the characteristics of the OTFT, which results in low operating voltage and a better TFT performance. Despite these improvements, V_{th} and V_{GS} are relatively high, limiting the application of the proposed dielectric in battery-powered devices. Zhou *et al.* presented P3HT OTFTs gated with dual layers of Ta_2O_5/PVP [195]. The OTFTs operated at −10 V but suffered from the same issue as their predecessors. Although the thick layer of PVP (250 nm) reduces the leakage current significantly, it prevents TFTs to operates at lower voltages. Likewise, Zhou *et al.*, in a different research group, proposed n-type OTFTs based on a thick double layer of Ta_2O_5/PMMA [38]. It has been reported that PMMA smoothened the dielectric/semiconductor interface and helped to reduce the gate leakage current. Table 2.5 shows the key parameters of the abovementioned transistors.

Ref.	Dielectric	d (nm)	V_G (V)	V_{th} (V)	OSC	μ ($cm^2V^{-1}s^{-1}$)	I_{ON}/I_{OFF}
[213]	Ta_2O_5/HMDS	–	−7	2.7	Pentacene	0.3	10^7
[195]	Ta_2O_5/PVP	120 nm/250 nm	−10	1.7	P3HT	0.03	–
[38]	Ta_2O_5/PMMA	200 nm/50 nm	10	2.3	PTCDI-C12	~ 0.06	10^4

Table 2.5. Parameters of the previously demonstrated low-voltage OTFTs using organic/inorganic bilayer dielectrics.

Chapter 3: Experimental procedures

3.1 Materials selection

To fabricate a device, several preliminary steps should be accomplished initially. First of all, a careful selection of materials which may affect the output of a project should be carried out. This step is essential, and thus this task should be performed meticulously. For example, among all potential substrate materials, ultra-flat quartz coated glass substrate (S151, Ossila, UK) has been chosen due to its super flat surface property, which is desirable for the anodisation process. In this research, tantalum (Ta) is used as an electrode (anode) in the anodisation process to form a tantalum pentoxide layer. Then, depending on which semiconductors are used, aluminium (Al) or gold (Au) are deposited as the drain/source electrodes, respectively.

3.1.1 Contact Metals

3.1.1.1 Tantalum

Tantalum (Ta) is a non-toxic, silver-grey, highly ductile metal with high density which possesses an extremely high melting point and excellent thermal and electrical conductivity that is widely utilised in a variety of applications. Tantalum is commonly used in dental and surgical implants since it causes no immune response in humans, particularly used in electronic devices, high capacitance capacitors and high power resistors. Its crystal structure is body centre cubic (BCC). The work function of Ta is reported to be between 4.10–4.30 eV. When exposed to O_2 or H_2O in ambient air, tantalum forms a very dense oxide layer (Ta_2O_5) with an oxidation state of +5, which prevents further oxidation of the base material. The key properties of Ta are summarised in Table 3.1. In this research, Ta was used as the gate contact of TFTs and the bottom contact of MIM capacitors and memristors.

Property	Value
Atomic number	73
Atomic mass	180.95
Melting point	2996 °C
Boiling point	5458 °C
Lattice constant	330 [pm]
Density at 20 °C	16.65 [g/cm^3]
Thermal conductivity at 20 °C	57.5 [W/(m·K)]
Electrical conductivity at 20 °C	8×10^6 [1/(Ω·m)]

Table 3.1. Key physical and chemical properties of tantalum (Ta).

3.1.1.2 Aluminium

Aluminium (Al) is a non-toxic, lightweight, ductile, low cost and the most abundant metal in the earth's crust with high thermal and electrical conductivity. Therefore, Al and its alloys are extensively used in a variety of applications, including electronic devices. The work function of aluminium is around 4.2 eV, and the oxidation state is +3 (Al_2O_3). The crystal structure of Al is reported to be face centred cubic (FCC). In this research, Al was used as top electrodes in MIM capacitors and as the drain/source contacts in TFTs. The key properties of Al are summarised in Table 3.2.

Property	Value
Atomic number	13
Atomic mass	26.98 [g/mol]
Melting point	660.2 °C
Boiling point	2480 °C
Lattice constant	404.95 [pm]
Density at 20 °C	2.7 [g/cm^3]
Thermal conductivity at 20 °C	205.0 [W/(m·K)]
Electrical conductivity at 20 °C	3.5×10^7 [1/(Ω·m)]

Table 3.2. The key physical and chemical properties of aluminium (Al).

3.1.1.3 Gold

Gold (Au) is a good conductor of electricity and heat, and it is not chemically reactive when compared with other metals. Au is also extremely malleable, highly corrosion resistant, and at ultrathin thickness (d < 20 nm) can be semi-transparent. Although it is an expensive metal which has high electrical conductivity, it is widely used where an inert or high work function (~ 5.1 eV) metal is required. The crystal structure of gold is reported to be FCC. In this research, Au was used as the top electrode of MIM capacitors and as the drain/source contacts in OTFTs. The key properties of Au are summarised in Table 3.3.

Property	Value
Atomic number	79
Atomic mass	196.97 [g/mol]
Melting point	1064 °C
Boiling point	2860 °C
Lattice constant	407.82 [pm]
Density at 20 °C	19.3 [g/cm^3]
Thermal conductivity at 20 °C	310.0 [W/(m·K)]
Electrical conductivity at 20 °C	4.11×10^7 [1/(Ω·m)]

Table 3.3. The key physical and chemical properties of gold (Au).

3.1.1.4 Platinum

Platinum (Pt) is a dense, soft and highly corrosion-resistant metal. It is a rare (and therefore expensive), silvery-white metal which is often described as a noble metal as it is chemically unreactive. As such, it is widely used in surgical tools and electronics. The key properties of Pt are summarised in Table 3.4. In this research, Pt was used as the top electrode in resistive memory devices (memristors).

Property	Value
Atomic number	78
Atomic mass	195.08 [g/mol]
Melting point	1768.2 °C
Boiling point	3825 °C
Lattice constant	392.42 [pm]
Density at 20 °C	21.5 [g/cm^3]
Thermal conductivity at 20 °C	71.6 [W/(m·K)]
Electrical conductivity at 20 °C	9.43×10^6 [1/(Ω·m)]

Table 3.4. The key physical and chemical properties of platinum (Pt).

3.1.1.5 Deposition techniques

The preparation of metal contacts depends on their melting and boiling points. As such, they can be deposited with different deposition techniques such as thermal evaporation and RF/DC magnetron sputtering. Herein, both techniques were used in order to deposit a thin film of metal contacts on substrates.

3.1.1.5.1 Thermal evaporation

Thermal evaporation is one of the physical vapour deposition (PVD) techniques which can be used for the deposition or surface coating of metal or non-metal films and is well-suited for materials with low melting temperatures. The key advantages of thermal evaporation are the straightforward control of the purity and thickness of the deposited film [214]. The evaporation process takes place in the vacuum, which is set to at least 10^{-7} Torr. During this process, a material in a high-vacuum chamber is heated to its evaporation point by the joule heating of a resistive boat or wire (e.g., tungsten filament). The evaporated atoms or molecules then deposit on the substrate and form a thin film coating. The substrate in the thermal evaporator can be placed upside down or at the bottom of the deposition chamber, and similarly to other PVD techniques, shadow masks can be used to pattern the area of deposited film typically required for the fabrication of electronic devices. In this work, a thermal evaporation technique was used to deposit aluminium (Al) and gold (Au) thin films

as part of the fabrication procedures. Fig. 3.1 depicts the schematic and actual picture of the turbo-pump thermal evaporator located in the fabrication cleanroom that was used in this research.

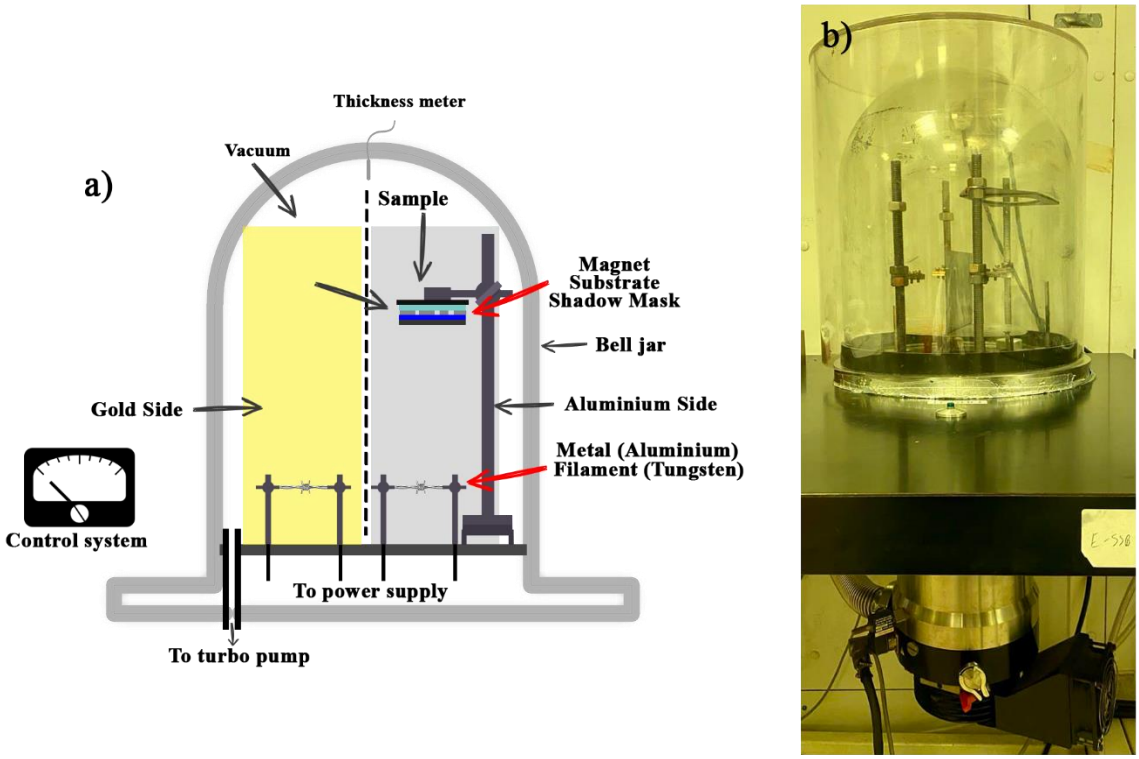


Fig. 3.1. (a) The schematic and (b) the actual picture of the turbo-pump thermal evaporator.

3.1.1.5.2 Radio Frequency (RF) Magnetron Sputtering

Radio frequency (RF) magnetron sputtering is another physical vapour deposition (PVD) technique that is typically used for the deposition of metals, dielectrics and semiconductors in the fabrication of electronic devices. This technique has several advantages and disadvantages over thermal evaporation. Firstly, the films deposited by magnetron sputtering can be configured with multiple sources and materials can be released at a much lower temperature than the evaporator, but it is a costly and complex process in comparison with the thermal evaporation. RF magnetron sputtering can also be used for the deposition of materials which cannot be easily evaporated due to their high evaporation temperature (e.g., Pt). The operation detail of RF magnetron sputtering process is discussed in section 2.3.3.3.2. Herein, MOORFIELD MINILAB 025 RF magnetron sputtering system was used to deposit

Ta and Pt metals and amorphous indium-gallium-zinc oxide (a-IGZO) semiconductor. Fig. 3.2 shows the actual sputtering equipment which was used to process the aforementioned materials into thin films.

Fig. 3.2. The actual picture of the employed RF magnetron sputtering system.

3.1.2 Metal oxide dielectric: Ta_2O_5

Tantalum pentoxide (Ta_2O_5) is a highly promising dielectric material due to its high transparency, high melting point (1785 °C), high dielectric constant and its good thermal and chemical stabilities. As such, it has been used in a wide range of electronic applications such as in dynamic random-access memory (DRAM), metal-insulator-metal (MIM) capacitors, memory resistors (memristors) and recently in organic and inorganic TFTs [215]. Moreover, due to the high refractive index, it has been broadly employed in optical devices [216]. The dielectric constant of Ta_2O_5 depends on its thickness and deposition technique and varies from ~ 35 in bulk to ~25 in a thin film [164]. This is at least two to six times larger than the dielectric constant of Al_2O_3 (κ = 9) and SiO_2 (κ = 3.9), respectively. As a result, Ta_2O_5 appears to be a good candidate to substitute SiO_2 as the gate dielectric in TFTs. Ta_2O_5 can be deposited using different methods, namely, thermal oxidation, plasma-assisted oxidation, RF sputtering, atomic layer deposition and anodisation [36]. However, it is well-established

that the dielectric properties of Ta_2O_5 significantly differ depending on which of the deposition methods is used [215].

3.1.2.1 Deposition technique: Anodisation

As comprehensively discussed in chapter 2, anodic oxidation, so-called anodisation, is an electrolytic oxidation method which can deliver as high quality oxide layers as ALD and magnetron sputtering but with a significantly lower cost and much cheaper equipment. Anodisation is a simple, self-healing and self-limiting processing technique performed at room temperature which is compatible with the large-area deposition. In this study, anodisation was used to grow Ta_2O_5 dielectric which was then utilised as the dielectric layer in TFTs.

3.1.3 Dielectric surface modifier: OTS

Surface modification and functionalisation are required for many applications such as sensors [217], water-resistant coatings [218] and TFTs [219]. As discussed in section 2.3.3.2.1, self-assembled monolayers (SAMs) are small molecular assemblies used widely as a passivation layer to increase hydrophobicity and prevent undesired reactions on the surface of oxide dielectrics. They are also employed as gate dielectrics [220][221], organic semiconductors [222][223] and electrode modifiers [224][225] which is beyond the scope of this study. It has been reported that the use of SAMs as a gate dielectric primer has two main advantages. It not only reduces the leakage current of the gate dielectric but also smoothens the surface of the dielectric in contact with semiconductor which potentially contributes to the reduction of the trap density at the dielectric/semiconductor interface, and as a result, improves the charge carrier mobility [141][226].

n-octyltrichlorosilane (OTS, $CH_3–(CH_2)_7–SiCl_3$) is a popular SAM that has previously been shown to have good compatibility with SiO_2 and metal oxide dielectrics. OTS is typically used as a passivation layer for capping the polar surface of metal oxides or

providing a hydrophobic coating layer preventing electrical instability of TFTs [58]. Since it has been shown that OTS is one of the most effective SAMs to improve the dielectric characteristics of metal oxide dielectrics [226], in this study, it was used to passivate the surface of anodic Ta_2O_5 dielectric. The effect of OTS on the surface of Ta_2O_5 is investigated in detail in the following sections. Fig. 3.3 shows the chemical structure of OTS and a schematic of the condensation reaction on the surface of Ta_2O_5.

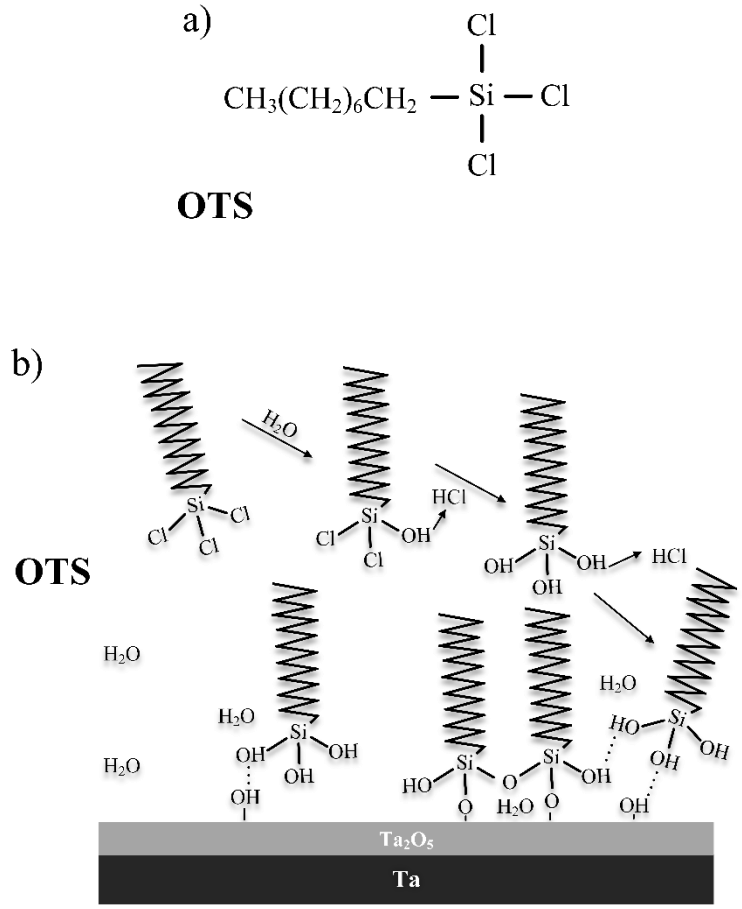


Fig. 3.3. (a) The chemical structure of OTS and (b) schematic of the Ta_2O_5 surface passivation process [226].

3.1.3.1 OTS surface treatment technique

OTS can be deposited using different methods such as chemical vapour deposition (CVD) [227], dip or spin coating [228][229]. However, the most often OTS is deposited using the conventional solution-based dip or spin coating. The solvents typically used for preparing OTS solutions are chloroform [230], toluene [231][232], and *n*-hexane [233][234].

3.1.4 Semiconductors

Semiconductors are the most important part of any transistors as it can determine the functionality and application of the device for sensing, switching, amplifying, etc. In particular, depending on several factors such as mobility, stability, compatibility, flexibility and performance, organic semiconductors are typically used for organic light-emitting diodes (OLEDs) [235] in displays, thin-film batteries [236], supercapacitors [237], organic photovoltaics (OPVs) [238], sensors and biosensors [239]. On the other hand, as discussed before, oxide semiconductors can offer high performance, high transparency, suitable electrical and environmental stability and can be potentially used in the applications such as displays, sensors, and even new applications where flexibility, high performance and transparency are required. In this study, poly(3,6-di(2-thien-5-yl)-2,5-di (2-octyldodecyl)-pyrrolo [3,4-c] pyrrole-1,4-dione) thieno [3,2-b] thiophene) (DPPDTT) and amorphous indium-gallium-zinc oxide (a-IGZO) are selected as a p-type organic and n-type inorganic semiconductors, respectively.

3.1.4.1 Organic semiconductor: A DPPDTT/PMMA blend

3.1.4.1.1 DPPDTT

DPPDTT is a p-type polymer semiconductor. Currently, a wide family of DPP-based polymer semiconductors are available. DPP-based polymers consist of diketopyrrolopyrrole (DPP) and thieno[3,2-b] thiophene (TT) as an electron-rich polymer backbone. DPPDTT has the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) levels at −5.2 eV and −3.5 eV from the vacuum, respectively. As a result, the bandgap of DPPDTT is 1.7 eV [240]. It has been reported that the bandgap of DPP-based polymers can be tuned between ~ 1–1.8 eV by replacing the thiophene substituents with longer π-conjugated donor segments (e.g., thienothiophene (TT)) [241]. DPPDTT was selected as the organic semiconductor due to its high mobility with suitable air stability for

sensing, photovoltaic and transistor applications. DPPDTT with a relatively low molecular weight (M_n < 30,000) can be dissolved in common organic solvents such as chloroform, toluene, tetrahydrofuran (THF). However, it turns out that for very high molecular weights (M_n > 70,000), it can only be dissolved in chlorinated solvents (e.g., chloroform and chlorobenzene) [240]. Although DPP-based polymers generally show high carrier mobilities (> 1 cm^2 V^{-1} s^{-1}) in OTFTs, it has been reported that using different solvents ($CHCl_3$, toluene, toluene/DPE (3%)) can strongly influence the charge carrier mobility in bottom-gate bottom contact OTFTs. OTFTs with charge carrier mobilities in the range of ~ 2–5 cm^2 V^{-1} s^{-1} at V_{GS} of −100 V have been reported [242]. Fig. 3.4 shows the chemical structure of DPPDTT.

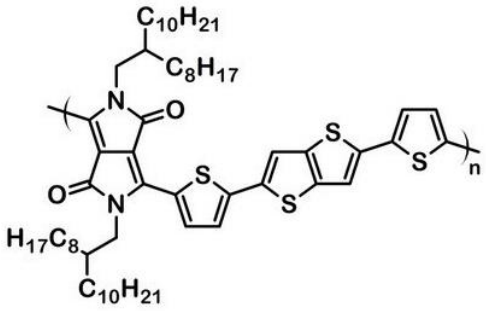


Fig. 3.4. The chemical structure of DPPDTT [99].

3.1.4.1.2 PMMA

Polymethyl methacrylate (PMMA) is a polymer dielectric with a dielectric constant of 3.6 at 100 Hz, and therefore, classified as a low-κ dielectric [243]. PMMA is typically used on its own or as a bilayer with a high-κ metal oxide dielectric (e.g., Al, Ta, etc.) to form a hybrid low-κ/high-κ dielectric [244][245]. PMMA forms a good organic-organic interface with organic semiconductors, which has been reported to be beneficial for TFTs because of the inert nature of this polymer [246]. Fig. 3.5 demonstrates the chemical structure of PMMA.

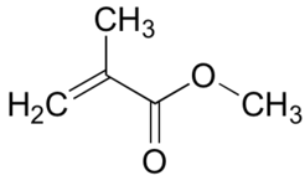


Fig. 3.5. The chemical structure of PMMA.

As discussed in section 2.2.3.2, blending organic materials can have a synergistic effect and shows superior properties over each substance alone. In the case of OTFTs, the use of a dielectric–semiconductor blend not only allows a formation of a good interface on a variety of substrates leading to lower the trap density and improvement of charge carrier mobility but also significantly reduces the leakage current. It has been reported that the vertically staggered P3HT: PMMA blends can be used to realise low-voltage operation (i.e., 2 V) OTFTs since the dielectric formed in this blend system can be very thin and, as a consequence, induce high capacitance. The other important advantage of this bilayer structure is that it can offer high mobility (up to 0.47 $cm^2 V^{-1} s^{-1}$) in OTFTs with only one step of fabrication needed for the semiconductor and dielectric [109][111][247].

3.1.4.2 Inorganic semiconductor: a-IGZO

Amorphous indium-gallium-zinc oxide (a-IGZO) is an n-type oxide semiconductor recently proposed to address the duality of the device performance and processing temperature [24]. The a-IGZO films can be deposited by pulsed laser deposition on polyethylene terephthalate (PET) at room temperature and shows Hall effect mobilities higher than 10 $cm^2 V^{-1} s^{-1}$ (this is an order of magnitude larger than a-Si:H) [24]. Owing to the fabrication at low temperatures, a-IGZO can be used in flexible large-area electronics. Moreover, a-IGZO can be used in transparent thin-film transistors (TTFTs), unlike Si, which is not transparent due to its small bandgap. In this study, a-IGZO TFTs were fabricated to not only realise high performance, low-voltage TFTs but also to pave the way towards realising low-power, complementary metal-oxide-semiconductor (CMOS) circuits consisting of p-channel DPPDTT/PMMA TFTs and n-channel a-IGZO TFTs.

3.2 Fabrication procedures

3.2.1 Cleaning procedures

In this work, 2 × 1.5 cm^2, ultra-flat, quartz coated glass slides (Ossila, UK) were used as the substrates. The substrates were rinsed with deionised water in order to remove any water-soluble contaminants and dried with pure compressed N_2. Next, the slides were sonicated for 30 min in acetone, methanol and isopropyl alcohol (IPA). Then, the glass slides were taken from the sonic bath and again dried with pure N_2. To remove any residual organic contaminants, the substrates were put into a UV/Ozone cleaner for 30 min.

3.2.2 Deposition of Metal Contacts

In this work, Ta was used as the bottom-gate electrode for TFTs and bottom electrode for MIM capacitors and memristors. Ta was deposited through a shadow mask by using MOORFIELD MINILAB 025 radio frequency (RF) magnetron sputtering system with a 2-inch diameter Ta (Kurt J. Lesker, 99.9% pure) at a power of 70 W in a pure Ar atmosphere with a total pressure of 0.5 Pa at room temperature. For TFTs, Al and Au were used as the top contacts and were deposited by a thermal evaporator. For memristors, Pt was used as the top contact and was deposited by RF magnetron sputtering. Fig. 3.6 and 3.7 illustrate the schematic and actual picture of shadow masks (gate electrode, drain/source contacts, and semiconductor layer) with their main dimensions, which were used for device fabrication, respectively. During the fabrication, the shadow masks were carefully aligned on the substrate at each and every stage of deposition to avoid scratching either substrate or deposited layers beneath. The transistor channel widths (W) and lengths (L) were 1000 µm and 30 µm, respectively.

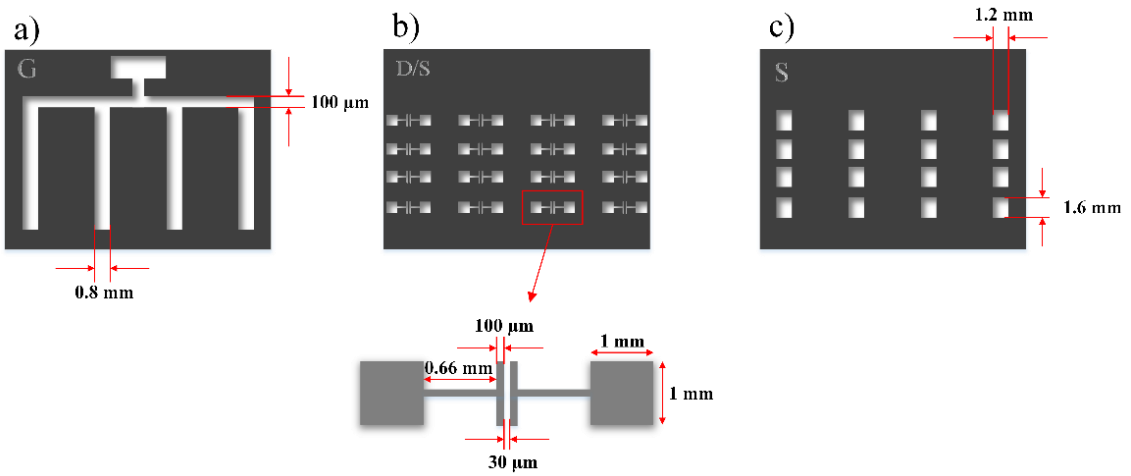


Fig. 3.6. Schematic of (a) custom design gate electrode shadow mask, (b) drain and source contacts shadow mask (Ossila, UK) and (c) custom design semiconductor (IGZO) shadow mask.

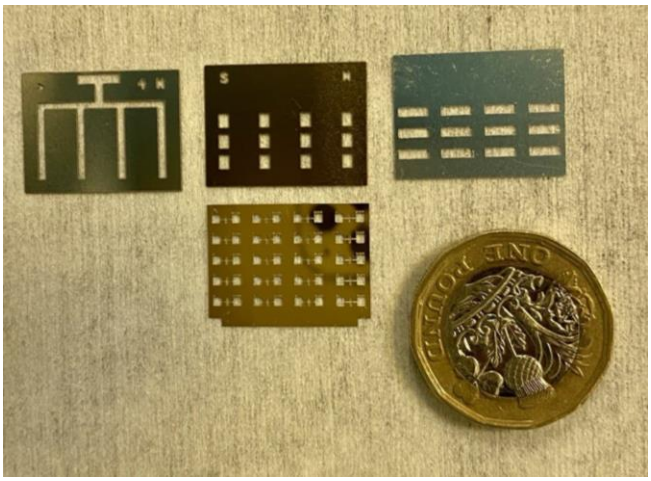


Fig. 3.7. Actual picture of the gate electrode, drain and source contacts, semiconductor (IGZO) layer, and capacitor top electrode shadow masks.

3.2.3 Tantalum oxide dielectric deposition

As discussed before, the barrier type Ta_2O_5 dielectric thickness depends on anodisation voltage (V_A) and the growth ratio ($[c_A]_{Ta}$ = 2.2 ± 0.2 nm/V) [248]. The process has to be performed in a constant current mode in a non-aggressive electrolyte. In this work, the Ta_2O_5 dielectric was grown by applying the desired anodisation voltage at a constant current density of J_A = 0.01 mA/cm^2. V_A was applied using a Keithley 2400 Source Meter. The anodisation process took place in 1 mM citric acid as the electrolyte, a gold wire as the cathode and Ta as the anode. The anodisation was carried out until J_A dropped to 0.005 mA/cm^2. Then, the resultant TaO_5 layer was rinsed with deionised water and dried using

pure N_2. Fig. 3.8 demonstrates the anodisation setup and the current source were used for this process.

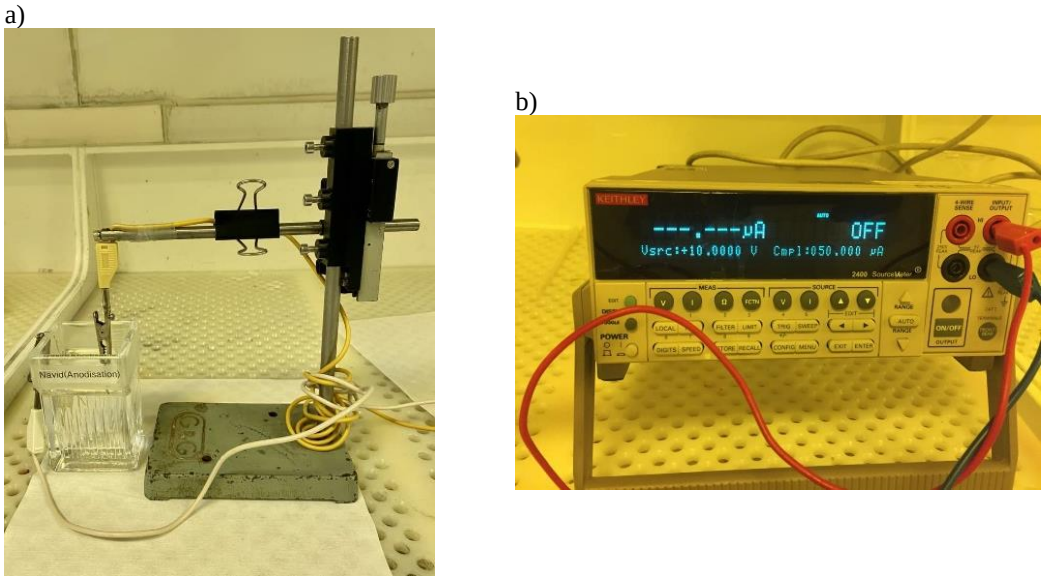


Fig. 3.8. a) Experimental anodisation setup and b) Keithley SourceMeter 2400.

Some of the anodically oxidised Ta_2O_5 films were treated with O_2 plasma for 2 min using an RF power at 100 W. This stage of surface treatment was done to increase the wettability of the Ta_2O_5 surface for the next stage of surface modification. The hydrophilic Ta/Ta_2O_5 samples were then immersed in 5 mM of freshly OTS solution (Sigma-Aldrich, ≥ 95%) in anhydrous toluene (Sigma-Aldrich, 99.8%) for 30 min in ambient conditions. The glass beaker containing the solution was sealed to minimise contact with the atmospheric air and to avoid possible degradation of OTS. Afterwards, the substrates were taken from the OTS solution and promptly rinsed with fresh toluene, acetone and IPA and blow-dried with compressed N_2. Finally, the OTS-treated samples were placed on a hot plate at ~150 °C under a flow of N_2 for 2 h. In short, OTS-treatment has been carried out to decrease the gate leakage current and improve the dielectric/semiconductor interface. The effects of OTS-treatment are discussed in chapter 4 in detail.

a) b)

Fig. 3.9. (a) Anhydrous toluene (Sigma-Aldrich, 99.8%) (b) *n*-octadecyltrichlorosilane (Sigma-Aldrich, 95%).

3.2.4 The deposition of DPPDTT/PMMA OSC

Poly(3,6-di(2-thien-5-yl)-2,5-di (2-octyldodecyl)-pyrrolo [3,4-c] pyrrole-1,4-dione) thieno [3,2-b] thiophene) (DPPDTT) and poly(methyl methacrylate) (PMMA), and their blend solutions were prepared according to the procedures reported elsewhere [240]. In short, the DPPDTT: PMMA blend solution was prepared by separately dissolving 0.5 wt% DPPDTT (Ossila, UK) and 0.5 wt% of PMMA (Sigma-Aldrich) in anhydrous 1,2-dichlorobenzene (DCB) (Sigma-Aldrich, 99%) and subsequently mixed in a 7:3 ratio. Afterwards, the blend was stirred until completely mixed. The blend was then spin-coated at 2000 rpm for 2 min on substrates pre-heated at 100 °C. Subsequently, the deposited films were annealed at 100 °C for 30 min to 1 h under N_2 flow.

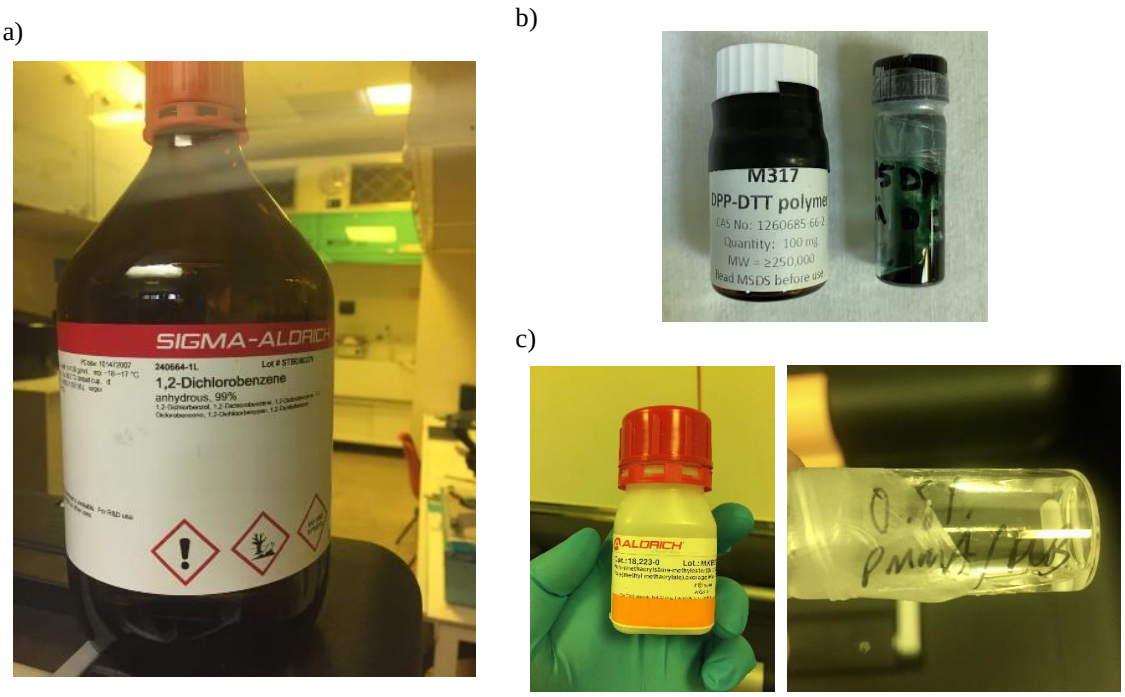


Fig. 3.10. (a) Anhydrous 1,2-Dichlorobenzene (DCB) (Sigma-Aldrich, 99%) (b) DPPDTT p-type OSC (Ossila, UK) (c) PMMA (Sigma-Aldrich).

3.2.5 The deposition of a-IGZO inorganic semiconductor

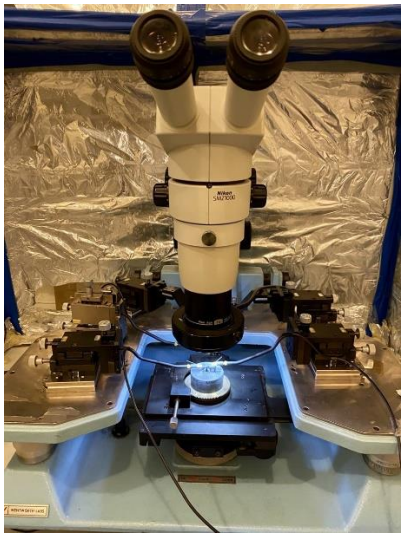
Based on our group findings on the optimum thickness and the deposition technique of a-IGZO, a 25-nm thick layer of a-IGZO was deposited onto the as-prepared Ta/Ta_2O_5 and OTS-treated Ta/Ta_2O_5 samples. The deposition is carried out through the semiconductor shadow mask by MOORFIELD MINILAB 025 RF magnetron sputtering using a 2-inch diameter IGZO target (In:Ga:Zn = 1:1:1) at the power of 50 W at room temperature.

3.3 Measurement and Characterisation techniques

3.3.1 Capacitance Measurement

In this research, the electrical characterisation of the fabricated Metal-Insulator-Metal (MIM) capacitors with the Ta/Ta_2O_5/Al, Ta/Ta_2O_5/OTS/Al, Ta/Ta_2O_5/Au, and Ta/Ta_2O_5/OTS/Au structures was carried out using an Agilent E4980A LCR meter. Fig. 3.11 shows the measurement setup and the LCR meter.

a)



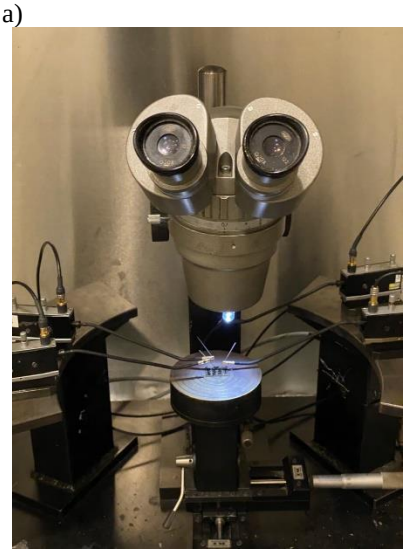
b)

Fig. 3.11. a) The measurement set-up and b) The Agilent E4980A LCR meter.

3.3.2 Current-Voltage (I-V) Curve Measurements

Typical output and transfer characteristics of TFTs and I-V curves of MIM capacitors were measured using an Agilent E5270B precision IV analyser at room temperature. Moreover, the I–V hysteresis of the TFTs and MIM capacitors was calculated using the threshold voltage difference between forward and backward curves by applying a forward and reserve bias. Fig. 3.12 shows the measurement setup and precision IV analyser.

a)



b)

Fig. 3.12. a) The measurement set-up and b) The Agilent E5270B precision IV analyser.

3.3.3 Dielectric surface analysis

Atomic force microscopy (AFM) was used to characterise the surface roughness of Ta/Ta_2O_5 and Ta/Ta_2O_5/OTS samples. The AFM images were obtained with a PSIA XE100 non-contact AFM, with a 100-micron scanner. The measurements were performed in the tapping mode, and an NT-MDT ultra-sharp cantilever was used for the data collection and carried out by Christopher Muryn from the Department of Chemistry at the University of Manchester.

3.3.4 Surface chemistry analysis

The X-ray photoelectron spectroscopy (XPS) measurement was performed to verify the chemical composition and stoichiometry of anodic Ta_2O_5 films. To neutralise the charge on the surface, a flood gun was used throughout XPS analysis (2 eV at 20 μA) and to excite the photoelectrons XPS analysis was carried out using a monochromatic Al Kα source (1486.6 eV). XPS measurement was carried out by Alex Walton from the Department of Chemistry at the University of Manchester, who obtained and helped to analyse XPS data. The XPS measurement data is discussed in detail in appendix 1.

Chapter 4: Result and Discussion

4.1 Low-voltage p-channel DPPDTT/PMMA TFTs gated with OTS-modified Anodic Ta_2O_5

4.1.1 Introduction

Organic thin-film transistors (OTFTs) have recently received much attention owing to high demands for inexpensive, lightweight, flexible, large-area electronic devices such as flexible active-matrix displays and low-cost chemical and biosensors. However, organic TFTs generally operate at relatively high gate voltages ($V_G \geq 10$), leading to large power dissipation in OTFTs and impeding their integration in power-efficient, low-cost, portable applications [249]. To address this technological obstacle, many high-κ metal oxide dielectrics such as HfO_2, Ta_2O_5, TiO_2, ZrO_2, Al_2O_3, Y_2O_3, CeO_2 have been used to lower the V_{GS} of these devices to below 5 V without sacrificing the device performance [121][250][251][143]. In particular, tantalum pentoxide (Ta_2O_5) is a promising candidate due to the high dielectric constant in bulk ($\kappa_{bulk} \sim 35$) and as a thin-film ($\kappa_{thin\text{-}film} \sim 26$). These values are at least two times larger than that of Al_2O_3 ($\kappa_{bulk} \sim 9$) [252] and five times larger than that of SiO_2 ($\kappa_{bulk} \sim 3.9$). As a result, Ta_2O_5 has been abundantly used in electrolytic capacitors, DRAM devices, and recently in solution-processed inorganic semiconductor thin-film transistors as a promising gate dielectric for low-power electronics [253]. Previously, low-voltage poly(3-hexylthiophene-2,5-diyl) (P3HT) TFTs operating at 3 V using thick (d > 100 nm), e-beam deposited Ta_2O_5 films have been reported [35]. However, the demonstrated p-channel transistors displayed relatively low mobility (~0.02 $cm^2 V^{-1} s^{-1}$), positive threshold voltage (+0.26 V), large subthreshold swing (> 1 V/dec), and their on/off current ratios ($I_{ON/OFF}$) were just above 10. This shows that the fabrication of high performance, organic semiconductor TFTs that can be operated at or below 1 V is not trivial. As discussed before, realising 1 V OTFTs is highly desirable for emerging applications such

as aqueous and bio sensors where they are needed to operate with voltages well below the hydrolysis voltage of water (~ 1 V).

To realise OTFTs which can be operated at or below 1 V, low values of threshold voltage (V_{th}) and subthreshold swing (SS) are essential. Preferably, V_{th} should be around 0 V and SS close to 60 mV/dec, which is the theoretical limit of subthreshold swing (SS) at room temperature [43]. This is a very challenging task, as it requires the thickness of high-κ gate dielectrics to be decreased to below 20 nm (C_G ~ 500 nF/cm^2). As a consequence of such thin dielectric layers, leakage currents significantly increase and deteriorate the device performance. This is especially the case for Ta_2O_5 dielectric which has a comparatively small bandgap (4.4 eV) when compared with other metal oxide dielectrics such as ZrO_2, (5.8 eV) or Al_2O_3 (8.8 eV). Besides, as discussed before, due to the surface hydroxyl (–OH) groups on the surface of Ta_2O_5 dielectric, which increase the trap density at the dielectric interface and consequently decrease the charge carrier mobility, and thus, it is beneficial to modify Ta_2O_5 surface with self-assembled monolayers (SAMs). OTS SAM can not only decrease the leakage current by adding an extra dielectric layer but also reduce the interfacial trap density by passivating the surface of metal oxide dielectrics. In other words, in the case of OTS-treated Ta_2O_5, the voltage applying across the Ta_2O_5 layer is much lower than untreated Ta_2O_5 layer due to the voltage divider effect of the two series capacitors and therefore, it reduces the gate leakage current. In this section, first, the chemical and physical properties of the anodic tantalum pentoxide are investigated in detail. Then, in order to be used in low operating voltage p-channel OTFTs, the process of Ta_2O_5 thin film optimisation is discussed.

4.1.2 Experimental procedure

To optimise the dielectric performance of Ta_2O_5 and Ta_2O_5/OTS films, metal-insulator-metal (MIM) capacitors were fabricated. First, a 100 nm of Ta layer was deposited through a shadow mask by radio frequency (RF) magnetron sputtering to serve as the gate electrode.

Next, samples were anodised in 1 mM of citric acid (≥ 99.5%, Sigma-Aldrich) using 99.99% pure Au wire as the cathode electrode. To form tantalum oxide films of various thicknesses, anodisation voltages (V_A) of 40, 30, 20, 10, 5 and 3 V with constant current density (0.01 mA/cm^2) were applied to the anode. The process was continued until the ionic current density dropped to 0.005 mA/cm^2. Based on the anodisation ratio of Ta ($[c]_{Ta}$ = 2.2 nm/V), a 3 V anodised Ta should result in an approximately ~ 6.6 nm thick Ta_2O_5 layer. Some of the as-prepared Ta/Ta_2O_5 substrates were treated with O_2 plasma for 2 minutes and then immersed in a freshly prepared 5 mM solution of OTS in anhydrous toluene at room temperature for 30 minutes. Afterwards, the substrates were removed from the solution and rinsed thoroughly and without interruption with pure toluene in order to get rid of the excess of unreacted OTS. The treated substrates were thereafter annealed on a hot plate at 120 °C for 1 h under a flow of dry N_2. To obtain MIM capacitors, 50 nm thick Au electrodes were deposited onto the prepared Ta/Ta_2O_5 and Ta/Ta_2O_5/OTS films. Fig. 4.1 depicts the fabrication process of Ta/Ta_2O_5/Au and Ta/Ta_2O_5/OTS/Au.

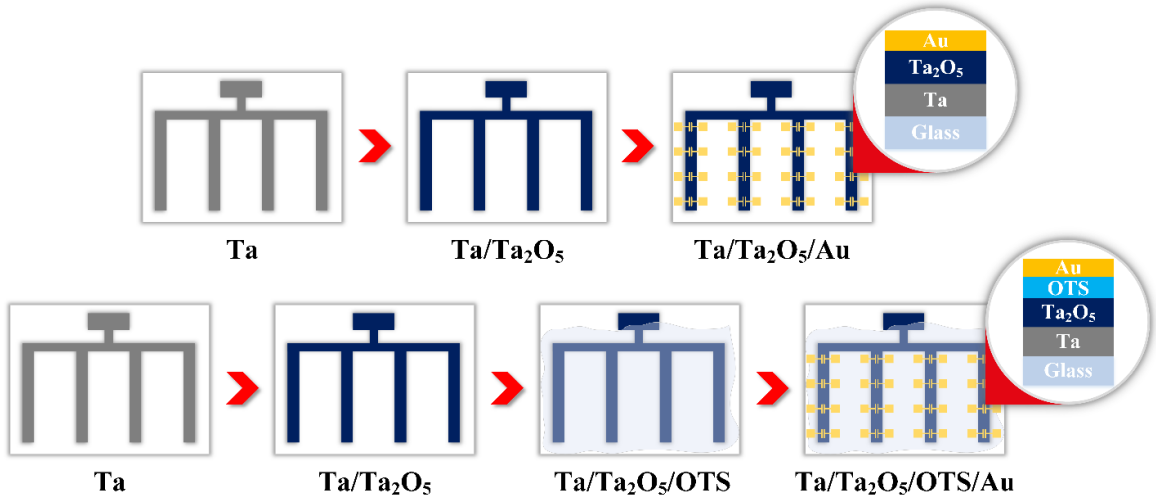


Fig. 4.1. The schematic of the fabrication process of MIM capacitors with (a) untreated Ta_2O_5 (b) OTS-treated Ta_2O_5.

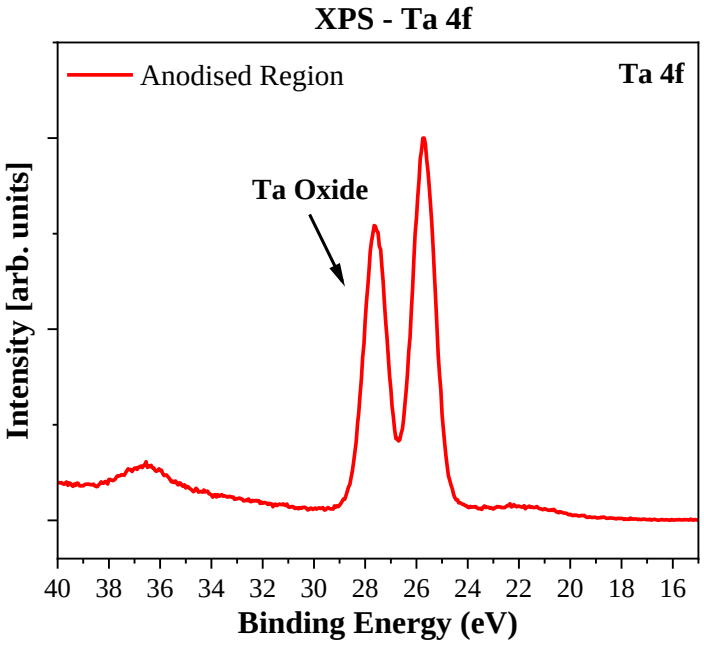
For the duration of the measurements, 1 V bias was applied to the bottom Ta electrode, and the top Au electrode was grounded. Organic TFTs were fabricated in the bottom-gate, top-contact structure on ultra-flat, quartz-coated glass substrates. Poly(3,6-di(2-thien-5-yl)-2,5-

di (2-octyldodecyl)-pyrrolo [3,4-c] pyrrole-1,4-dione) thieno [3,2-b] thiophene) (DPPDTT) and poly(methyl methacrylate) (PMMA) and their blend solutions were prepared according to the procedures reported elsewhere [240] and spin coated on the prepared Ta/Ta_2O_5 and Ta/Ta_2O_5/OTS substrates. Finally, a 100 nm thick layer of 99.99% Au was thermally evaporated through shadow masks to serve as drain and source electrodes. The channel width (W) and length (L) were 1000 μm and 30 μm, respectively. The electrical characterisation of the fabricated OTFTs was carried out using an Agilent E5270B semiconductor analyser and Keysight E4980A LCR meter at room temperature. The mobility was calculated by applying a linear fit to $I_D^{1/2}$ vs V_{GS} in the saturation regime using Eq. 2.7. All electrical measurements were done in ambient conditions in an electrically shielded, dark box.

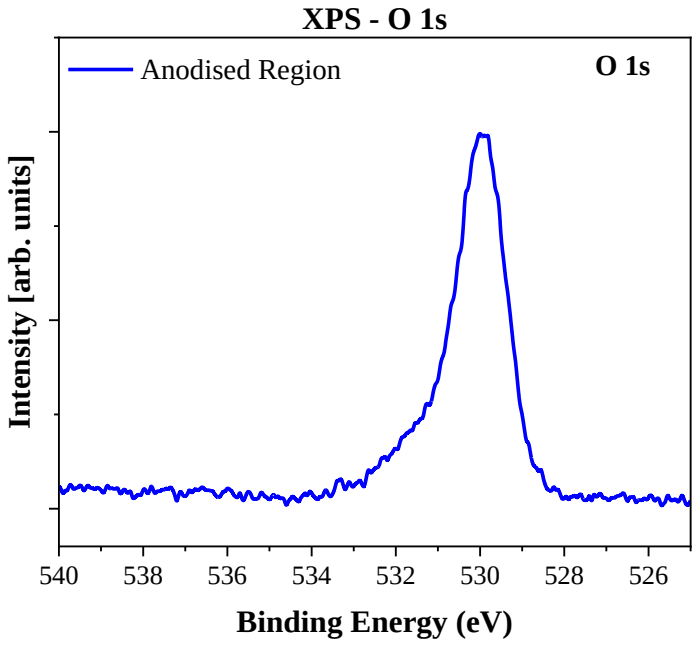
4.1.3 Results and discussion

4.1.3.1 Analysis of chemical composition of anodic tantalum oxide

X-ray photoelectron spectroscopy (XPS) was carried out to confirm the chemical composition and the stoichiometry of the anodised tantalum oxide films. A thick oxide, i.e., thicker than the sampling depth of XPS, was observed on the anodised region of the samples (Fig. 4.2, and Fig. A1.1–A1.3 in appendix I). By analysing the area of the Ta 4f and O 1s peaks, the Ta and O ratio was found to be nearly 2:5, confirming that tantalum pentoxide (Ta_2O_5) was successfully prepared through anodisation. Also, as shown in Fig. 4.2, the normalised O 1s peak fit indicates that the oxide formation on the anodised regions is consistent with the peak fitting analysis of the Ta 4f regions.



(a)



(b)

Fig. 4.2. Normalised (a) Ta 4f spectra (b) O 1s spectra of the anodised region.

4.1.3.2 Surface Analysis of Anodic Ta_2O_5 dielectric

Fig. 4.3 demonstrates 500 nm × 500 nm 2D and 3D atomic force microscopy (AFM) topography images of Ta/Ta_2O_5 (a/b) and Ta/Ta_2O_5/OTS (c/d) surfaces, respectively. AFM images were obtained with a PSIA XE100 non-contact AFM, with 100-micron scanner. Measurements were performed in the tapping mode and a NT-MDT ultra-sharp cantilever was used for the data collection. As can been seen, the pristine and OTS-modified Ta_2O_5

films are relatively flat and featureless. The root-mean-square (RMS) roughness of the unmodified Ta_2O_5 is found to be 0.92 nm. It appears that the anodisation process is capable of delivering as smooth Ta_2O_5 films as it is in the case of Ta_2O_5 deposited using ALD [254]. The RMS roughness of the OTS-modified Ta_2O_5 is significantly reduced and is found to be 0.55 nm. This result is in good agreement with the previously published reports where it was shown that the modification of metal oxide dielectrics with self-assembled monolayers (SAMs) significantly reduces their surface roughness [255].

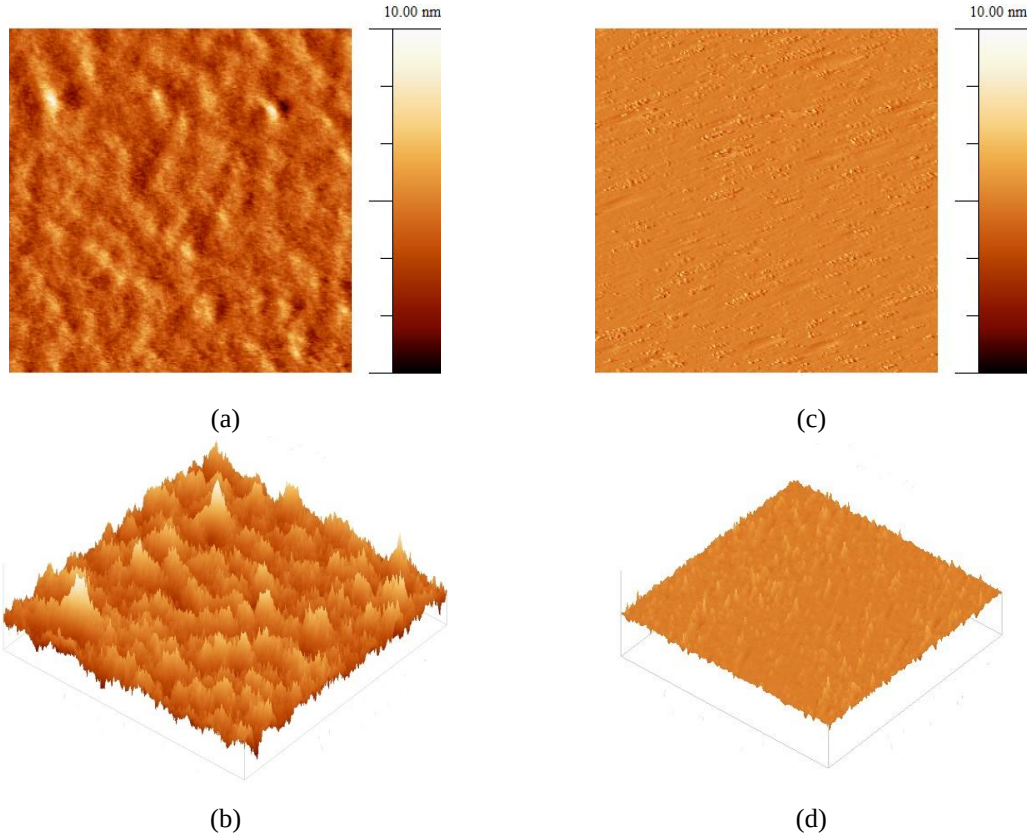


Fig. 4.3. 500 nm × 500 nm 2D and 3D AFM topographical images of (a, b) untreated and (c, d) OTS-treated Ta_2O_5 films.

4.1.3.3 Optimisation of Anodic Ta_2O_5 dielectric for low-operating voltage OTFTs

As previously mentioned, the thickness of barrier type anodic Ta_2O_5 dielectrics depends on the anodisation voltage (V_A) and anodisation ratio (c_A). In this light, in order to find the highest capacitance density with minimum dielectric loss and leakage current, a trade-off should be considered. The first step in the optimisation of the Ta_2O_5 dielectric to employ in

OTFTs and realise the low-voltage operation is to find the optimum thickness of the dielectric in terms of its main physical and electronic properties such as surface roughness and leakage current density, etc. Therefore, the anodisation voltages (V_A) are set to be 40, 30, 20, 10, 5 and 3 V, which result in circa 90, 70, 45, 20, 10 and 7 nm, respectively. To confirm the reproducibility of the measured dielectric parameters, 100 Ta/Ta_2O_5/Au MIM capacitors (cf. inset of Fig. 4.4) for each Ta_2O_5 film anodised with V_A = 40, 30, 20, 10, 5 and 3 V were fabricated, and 20 of each lot were randomly chosen for the measurements. Fig. 4.4 illustrates capacitance density (C_i) vs frequency of the MIM capacitors from 100 Hz to 100 kHz. As can be seen, for the dielectric thicknesses greater than ~22 nm (V_A = 10 V), capacitance density is relatively constant across the studied frequency range. As the Ta_2O_5 thickness decreases, it appears that the capacitors become unstable at both ends of the chosen frequency spectrum. Fig. 4.5 shows the capacitance density vs anodisation voltage at 1 kHz. Capacitors fabricated with Ta_2O_5 anodised at 40, 30, and 20 V exhibited an average capacitance density of 380, 450, and 700 nF/cm^2 at 1 kHz, respectively. The maximum standard deviation of the measured capacitance values for these capacitors was ±20 nF/cm^2. As expected, increasing the thickness of the dielectric leads to a lower dielectric capacitance density. Although this reduction is not linear initially (most likely due to the high leakage current), it gradually becomes linear for the thicker dielectrics.

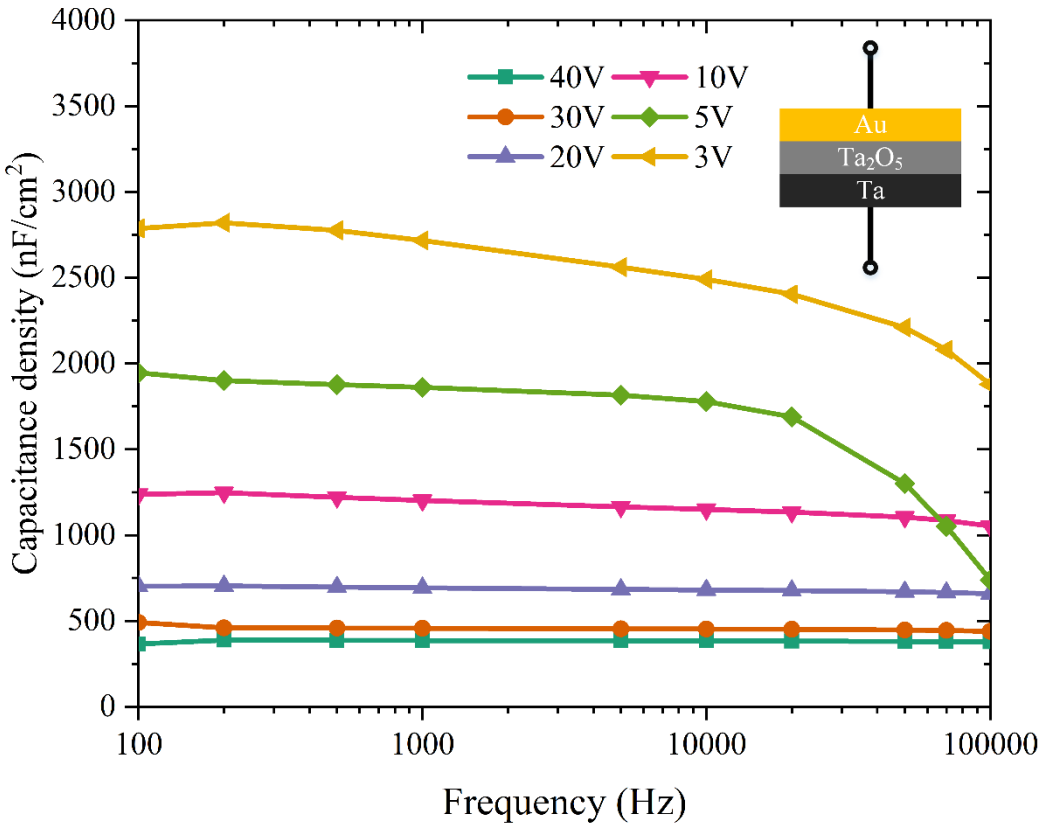


Fig. 4.4. Capacitance density vs frequency of the studied Ta/Ta_2O_5/Au capacitors.

On the other hand, although the capacitors with anodic Ta_2O_5 prepared at 10, 5, and 3 V show much higher capacitances, they have significantly higher leakage currents and dielectric losses, especially for $V_A \leq 5$ V.

As a result, it can be concluded that the pristine Ta_2O_5 films anodised at or below 10 V (d ~ 22 nm) are unsuitable for practical applications.

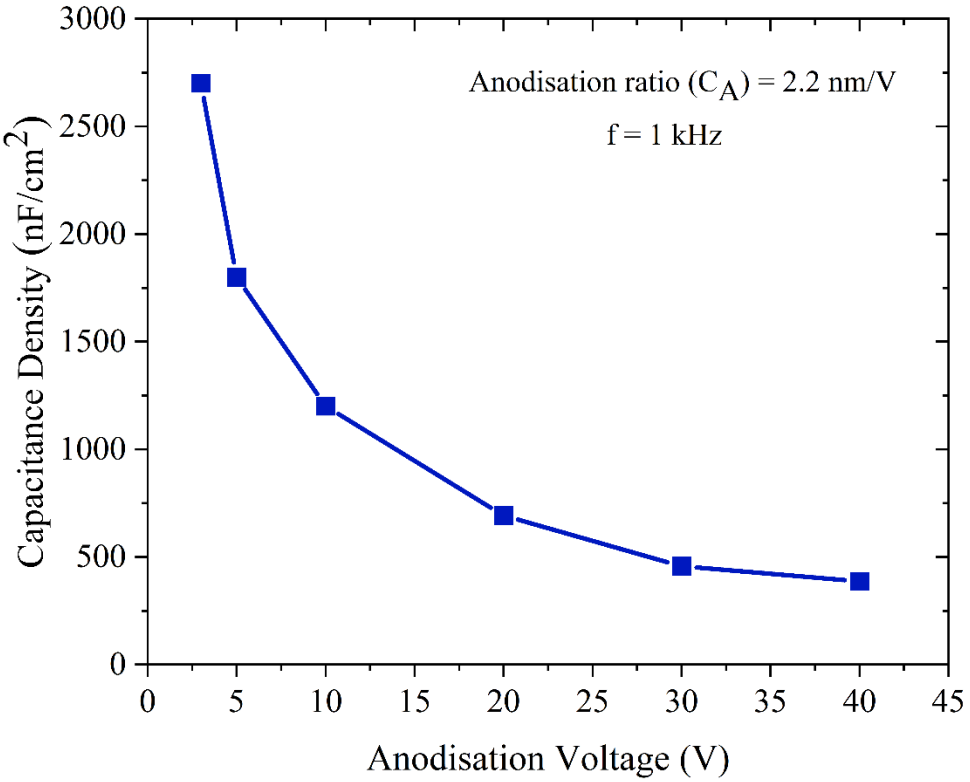


Fig. 4.5. Capacitance density vs anodisation voltage at 1 kHz of the studied Ta/Ta_2O_5/Au capacitors.

Correspondingly, the dissipation factor (DF) measured on capacitors using Ta_2O_5 anodised at various voltages is depicted in Fig. 4.6. For the simplest actual model, i.e., equivalent series resistance in series with the capacitance that neglects equivalent series inductance and insulation resistance, DF is the ratio of equivalent series resistance (ESR) and capacitive reactance (X_c), as defined by [256]:

$$DF = \frac{ESR}{X_c} \qquad \text{(Eq. 4.1)}$$

Ideally, for a given capacitor DF should be zero, but practically it consists of a negligible loss due to resistive characteristics.

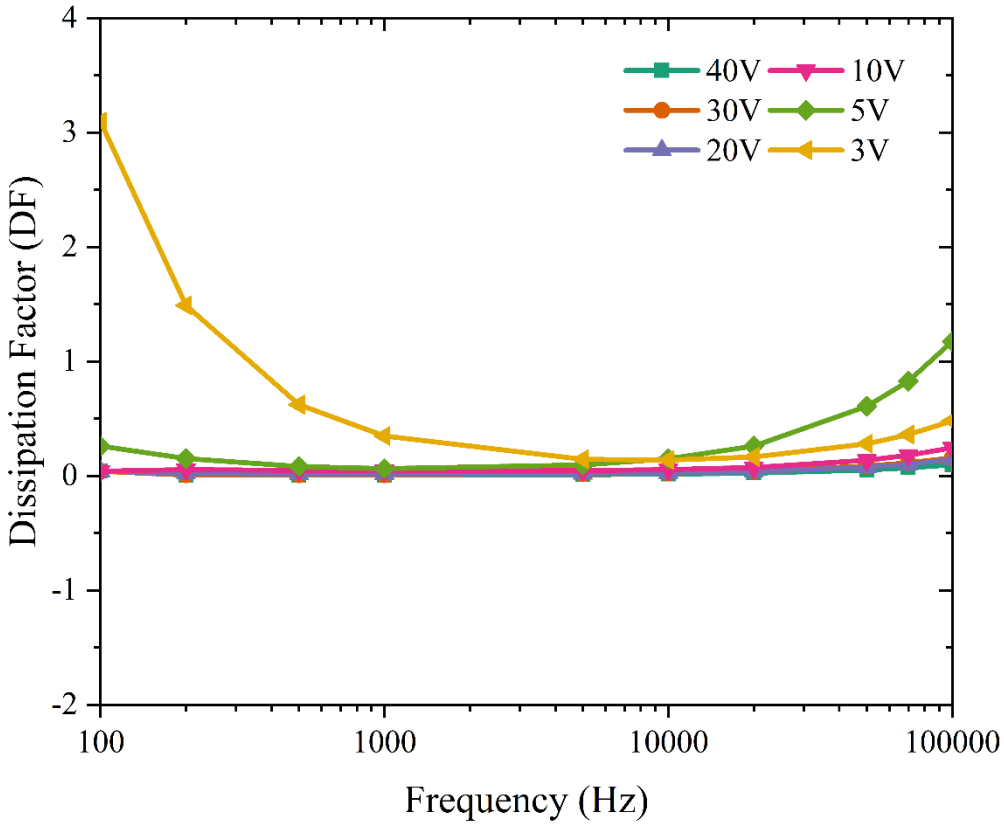


Fig. 4.6. Dissipation factor vs frequency of the studied Ta/Ta_2O_5/Au capacitors.

As shown in Fig. 4.6, the capacitors with 40, 30, and 20 V anodised Ta_2O_5 display a minimal DF that is close to zero. However, as the anodisation voltage decreases below 20 V, DF becomes larger, and the leakage currents through the anodic dielectric layer start to be appreciable (cf. Fig. 4.6 and 4.7). Accordingly, as the Ta_2O_5 dielectric thickness decreases even further (V_A = 5 and 3 V), the leakage current through the dielectric becomes very large. The leakage currents are somewhat asymmetric and higher for negative voltages. This is very likely caused by using electrodes with different work functions (Ta and Au) and differences in the roughness of the Ta/Ta_2O_5 interfaces. As can be seen, the leakage currents of 3 and 5 V anodised Ta_2O_5 dielectrics do not follow the others' trend and move to more positive values for lower thicknesses. Although this phenomenon is required additional in-depth investigation and study, it likely occurred due to the unstable nature of Ta_2O_5 dielectrics at an ultra-thin thickness to keep charges apart in the two electrodes. In particular, capacitors with the thinnest anodic Ta_2O_5, i.e., anodised at 3 V, exhibit the largest leakage current density (J_{Leak}) 10^{-3} A/cm^2 at 1 V.

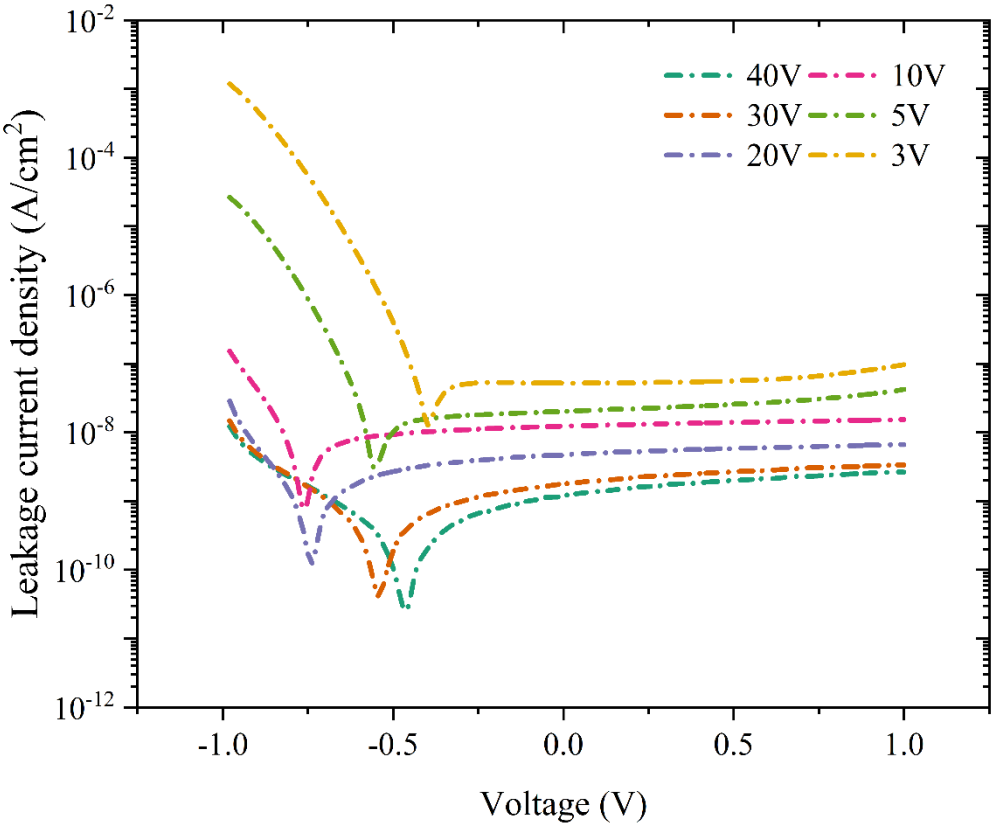


Fig. 4.7. Leakage current density vs voltage of the studied Ta/Ta_2O_5/Au capacitors.

The same electronic behaviour of the anodised Ta_2O_5 can also be seen in the C-V characteristics of the corresponding capacitors shown in Fig. 4.8, where high leakage currents reduce the voltage across the capacitors resulting in a lower electric field and lower capacitance at the positive end of the C-V curves. This is in contradiction with an ideal case, where a capacitor shows a flat capacitance-voltage characteristic which guarantees reliable and stable device performance. Nevertheless, thicker layers of Ta_2O_5 show flat and stable electrical behaviour across the chosen voltage characterisation range. Based on the abovementioned dielectric characteristics, it appears that the minimum anodisation voltage of tantalum for capacitor and TFT applications is 20 V, which corresponds to approximately 45 nm of Ta_2O_5. Indeed, the J_L for capacitors with 45 nm Ta_2O_5 layers is well below the maximum allowable value for TFT leakage current density (i.e., 10^{-6} A/cm^2) and is measured to be 10^{-7} A/cm^2 at 1 V.

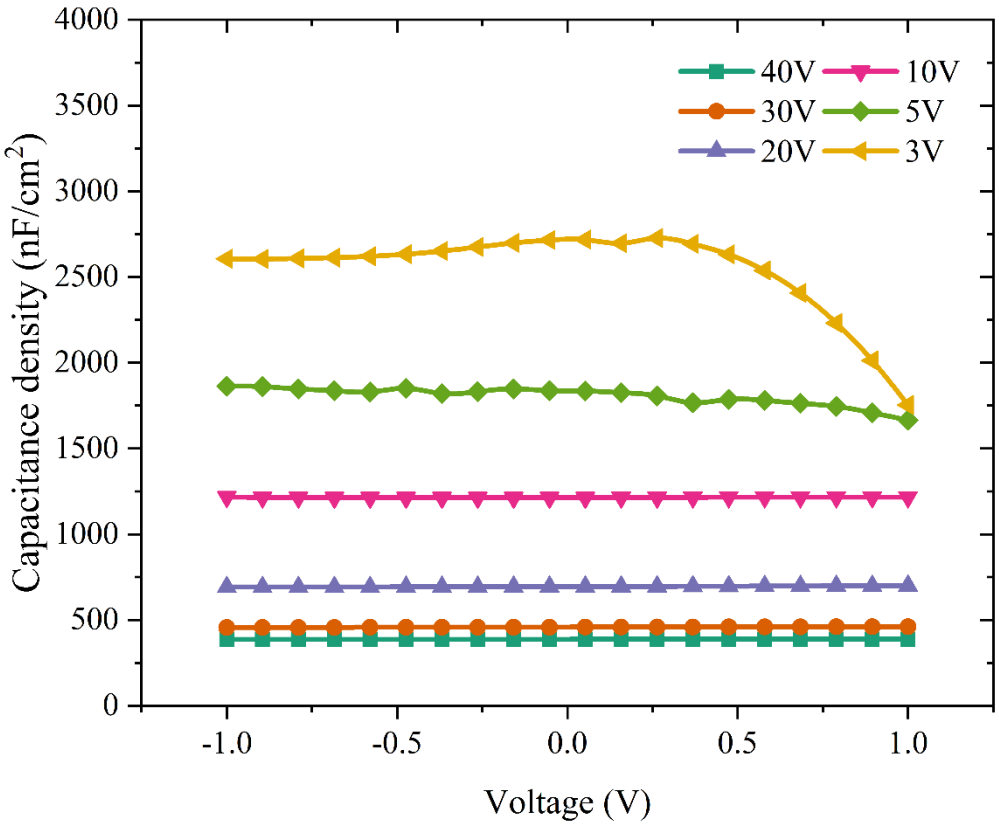


Fig. 4.8. Capacitance density vs voltage of the studied Ta/Ta_2O_5/Au capacitors.

Fig. 4.9 shows the structure of the fabricated bottom-gate, top-contact Ta/Ta_2O_5 (45 nm)/DPPDTT-PMMA/Au TFTs on a glass substrate (V_A = 20 V). Typical output and transfer characteristics of the fabricated transistors are shown in Fig. 4.9 (a) and (b), respectively. As can be seen in Fig. 4.10 (a), the drain current displays clear linear, pinch-off and saturation regions for all applied gate voltages.

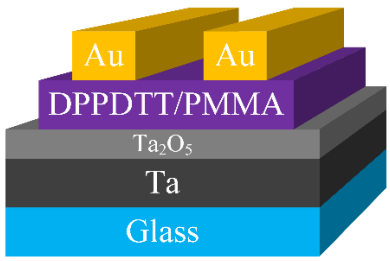


Fig. 4.9. The schematic structure of the OTFTs using Ta_2O_5 anodised at V_A = 20 V.

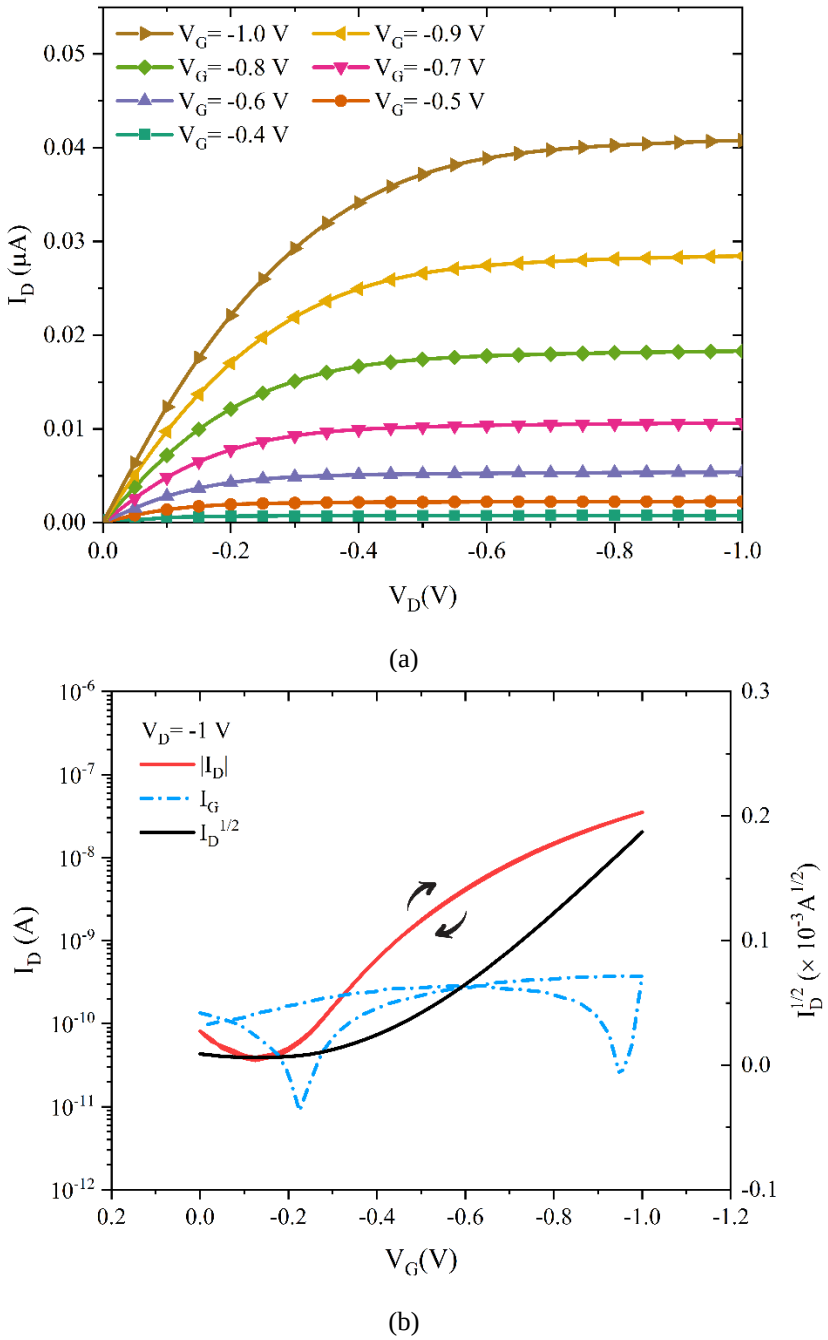


Fig. 4.10. Representation (a) output and (b) transfer characteristics of the studied OTFTs including $I_D^{1/2}$ and I_G vs V_G at $V_D = -1$, respectively.

The devices operate at –1 V with a saturation field-effect mobility of 0.02 $cm^2 V^{-1} s^{-1}$, threshold voltage –0.35 V, subthreshold swing 210 mV/dec, and current on/off ratio ~10^3. This transistor performance is comparable to the previously reported organic TFTs that used SAM-modified, anodised Al_2O_3 [197]. Table 4.1 summarises the key parameters of the best DPPDTT/PMMA OTFT using the 20 V anodised Ta_2O_5 film as the gate dielectric.

Parameters	20 V anodised Ta_2O_5 OTFTs
Mobility ($cm^2 V^{-1}s^{-1}$)	0.02
V_{th} (V)	−0.35
SS (mV/dec)	210
ON/OFF Current Ratio	~10^3
Operating voltage (V)	−1

Table 4.1. The parameters of DPPDTT/PMMA OTFTs gated by 20 V anodised Ta_2O_5 dielectrics.

To see if the dielectric SAM modification strategy also results in improved transistor characteristics of the TFTs with anodised Ta_2O_5, DPPDTT-PMMA TFTs with OTS-modified tantalum pentoxide have been fabricated. OTS is one of the most used SAMs in organic transistors. It has been shown that OTS significantly improves dielectric/semiconductor interface by passivating the gate insulator surface that leads to the reduction of charge carrier traps, and as a result, to higher charge carrier mobility [257][258]. During silanization, OTS molecules are attached to the dielectric surface through the chemical reaction of –SiCl with –OH groups on the metal oxide surface. This results in –Si–O–M structures. The other two –SiCl bonds of the OTS molecule react with proximate OTS molecules which forms a cross-linked monolayer. The OTS-treatment of the Ta_2O_5 layer inevitably results in a thicker overall dielectric layer and hence decreases the overall capacitance density of the dielectric film. The anodised Ta_2O_5 layer should be thin enough to provide the minimum required capacitance and leakage to operate the OTFTs at low voltages. Taking into account that the Ta native oxide thickness is about 3.5 nm [259], it is believed that to suppress the effect of the native oxide on the dielectric properties of Ta_2O_5, the thickness of the anodised Ta should be at least 3.5 nm thick. As shown in Fig. 4.4 and 4.7, an untreated Ta_2O_5 layer anodised at 3 V (d ~7 nm) exhibits a large enough capacitance density to be able to operate DPPDTT-PMMA TFTs at 1 V. However, the very high leakage current density of these thin layers would lead to poor field-effect transistor characteristics if used as prepared.

Fig. 4.11 compares the capacitance density vs frequency of 3 V anodised untreated Ta_2O_5 and OTS-treated Ta_2O_5 films. As can be observed in Fig. 4.11, the capacitance density

of OTS-treated Ta_2O_5 is notably reduced from 2700 nF/cm^2 for the sole Ta_2O_5 film to approximately 680 nF/cm^2.

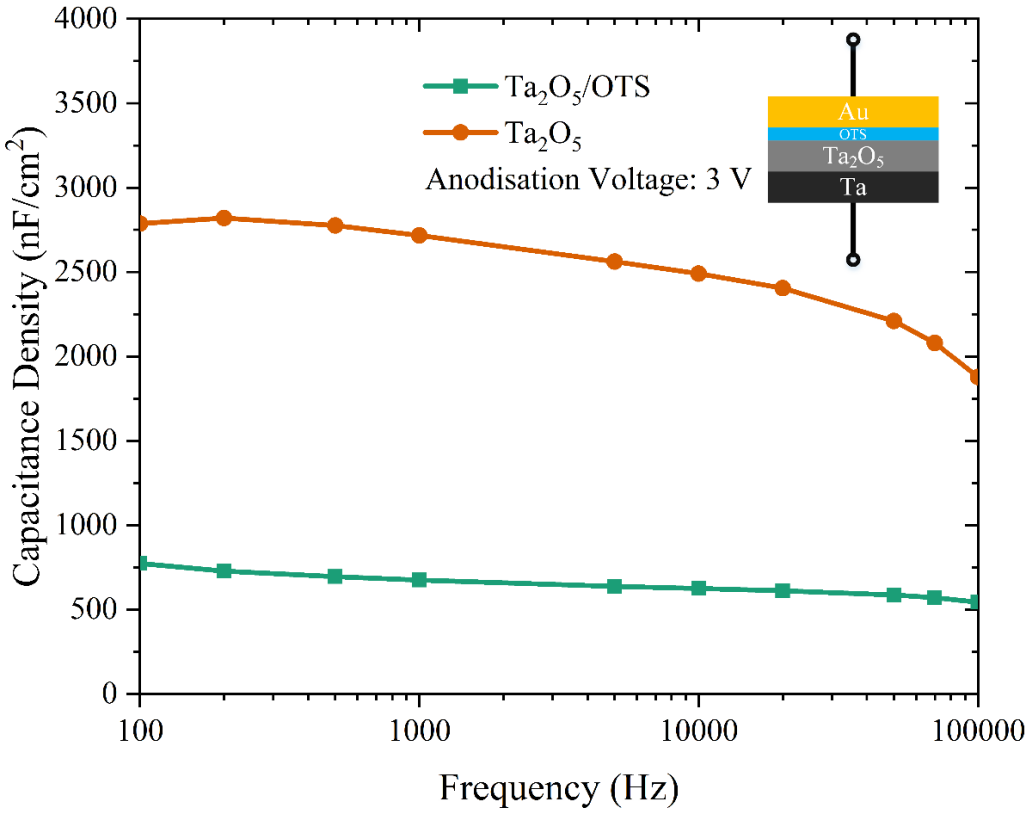


Fig. 4.11. Capacitance density vs frequency of the 3 V anodised Ta/Ta_2O_5/Au capacitors with and without OTS treatment.

This is due to the addition of the OTS layer, which leads to a thicker dielectric film and correspondingly smaller overall capacitance density because of two dielectric layers in series. Nonetheless, capacitance density curves for OTS-treated Ta_2O_5 are highly stable over a wide range of frequencies.

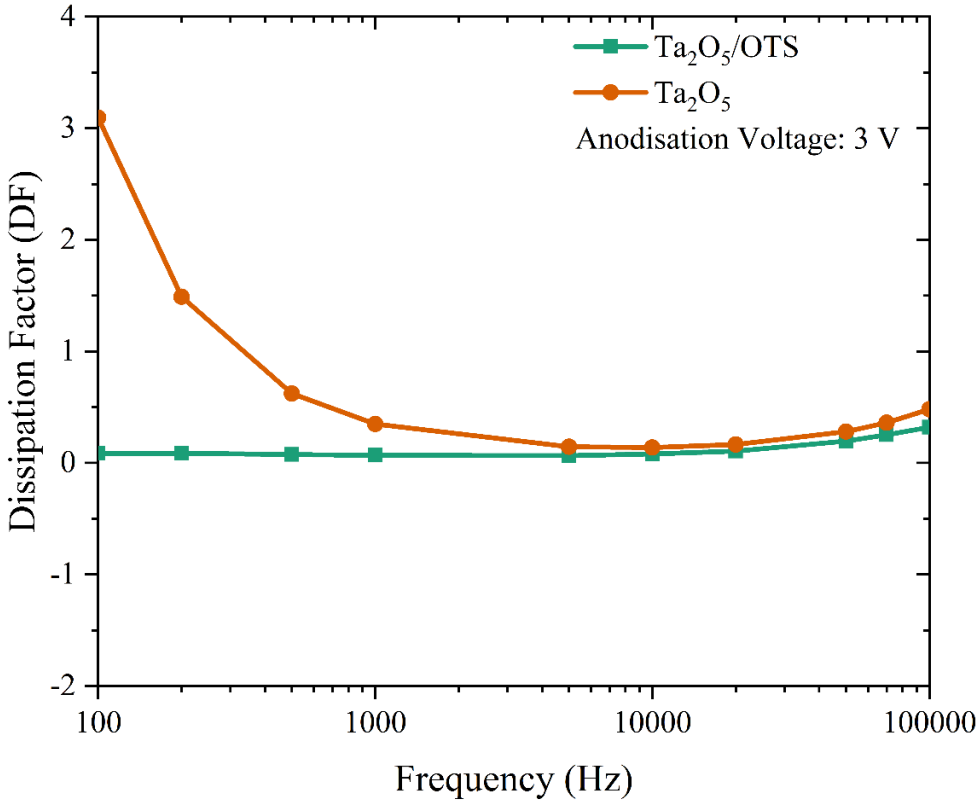


Fig. 4.12. Dissipation factor vs frequency of the 3 V anodised Ta/Ta_2O_5/Au capacitors with and without OTS treatment.

The dielectric loss (Fig. 4.12) for OTS-treated Ta_2O_5 shows a negligible variation (less than 0.1), confirming a low defect density in the OTS-treated Ta_2O_5 films. As shown in Fig. 4.13, leakage current density for OTS-treated Ta_2O_5 is approximately 2×10^{-7}A/cm^2 at ±1 V; this is reduced by circa five orders of magnitude at –1 V and circa one order of magnitude at +1 V when compared to films of untreated Ta_2O_5 of comparable thickness. The leakage current of the OTS-treated Ta_2O_5 is somewhat asymmetric and slightly lower for negative voltages. This is very likely caused by the use of electrodes with different work functions and differences in the roughness of the Ta/Ta_2O_5 and Ta_2O_5/OTS interfaces [260]. In addition, as illustrated in Fig. 4.14, in contrast to untreated Ta_2O_5, OTS surface modification has improved the stability of the capacitance density over the studied voltage range (−1 V to 1 V) and led to almost ideally flat C-V curves.

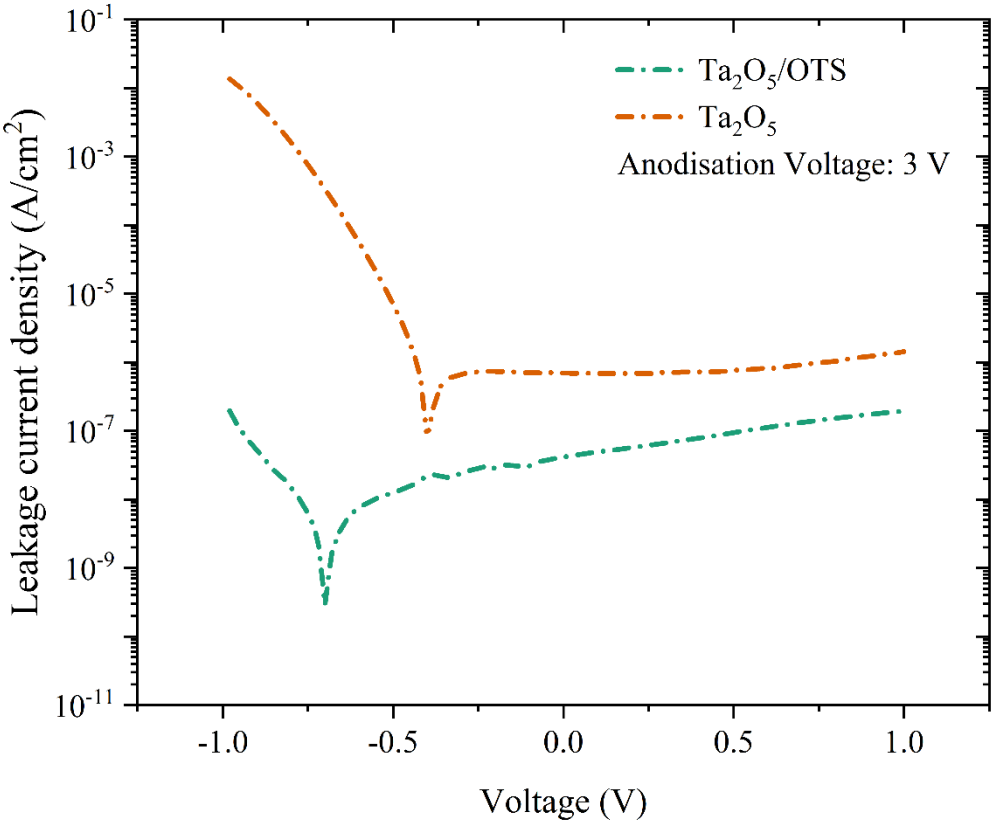


Fig. 4.13. Leakage current density vs voltage of the 3 V anodised Ta/Ta_2O_5/Au capacitors with and without OTS treatment.

To test if the optimised, OTS-modified Ta_2O_5 layers result in well-working 1 V devices, glass/Ta/Ta_2O_5 (7 nm)/OTS/DPPDTT-PMMA/Au OTFTs have been fabricated (V_A = 3 V). Fig. 4.15 shows the schematic structure of proposed 1 V OTFTs. Typical output and transfer characteristics of the fabricated transistors are shown in Fig. 4.16 (a) and (b), respectively. The optimised devices operate at 1 V with virtually no hysteresis. The saturation mobility is 0.22 $cm^2 V^{-1} s^{-1}$, the threshold voltage −0.55 V, subthreshold swing 120 mV/dec, and the current on/off ratio in excess of 5×10^3. Additionally, the leakage current at −1 V is measured to be less than 1 nA at all applied biases. The calculated mobility for these devices is > 0.2 $cm^2 V^{-1} s^{-1}$, ten times larger than the analogous DPPDTT-PMMA TFTs fabricated on the untreated Ta_2O_5 dielectric. It is believed that charge carrier mobility in TFTs is directly affected by the interfacial trap density [57]. Interfacial trap density (D_{it}) in thin-film transistors can be calculated using Eq. 2.14.

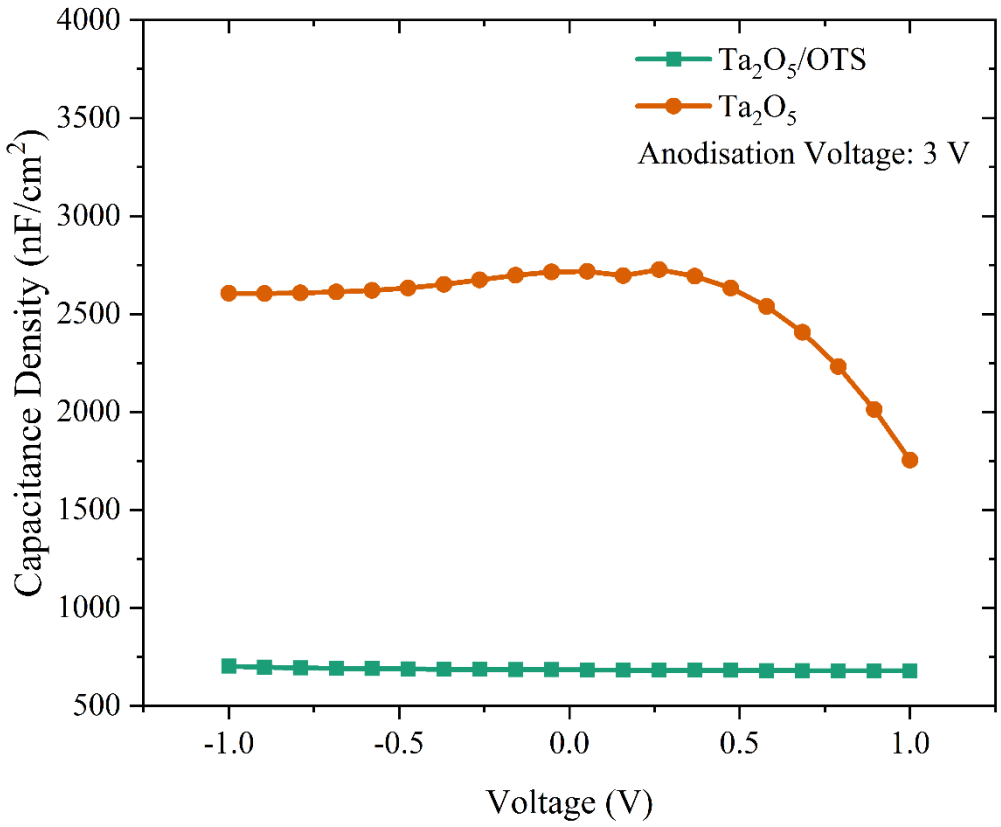


Fig. 4.14. Capacitance density vs voltage of the 3 V anodised Ta/Ta_2O_5/Au capacitors with and without OTS treatment.

D_{it} is calculated to be 1.09 × 10^{13} cm^{-2} eV^{-1} and 4.2 × 10^{12} cm^{-2} eV^{-1} for OTFTs using 20 V anodised untreated Ta_2O_5, and 3 V anodised OTS-treated Ta_2O_5, respectively. The reduction of trap density confirms that the OTS layers shield the active layer from traps at the anodic Ta_2O_5/DPPDTT-PMMA interface.

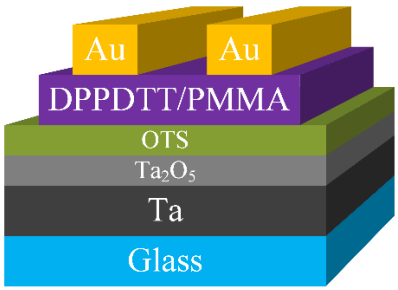
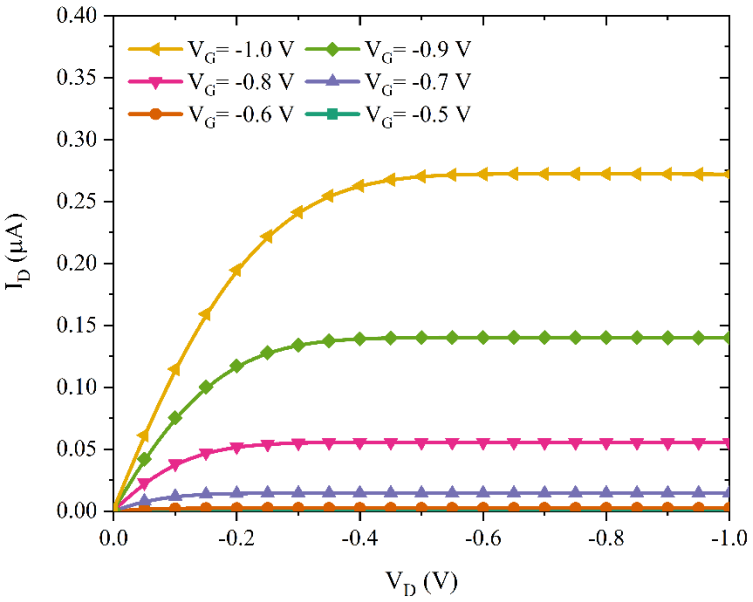
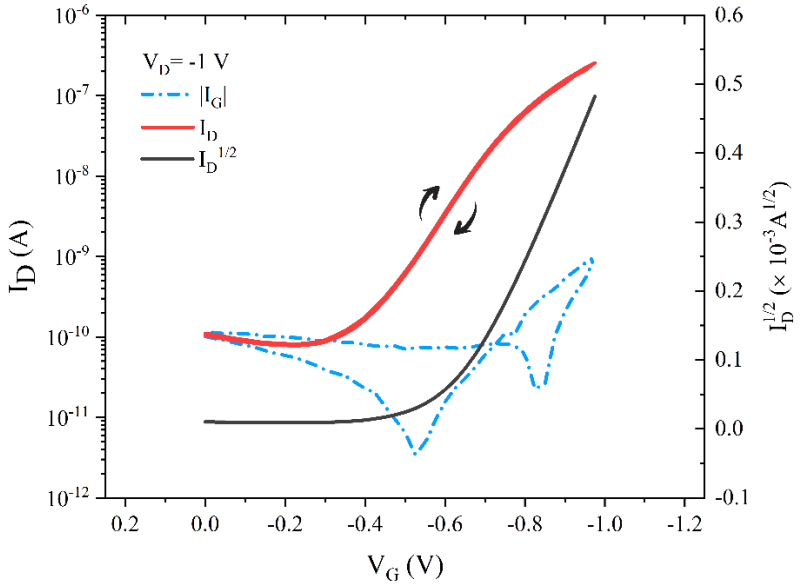


Fig. 4.15. The schematic structure of the OTFTs using OTS-modified Ta_2O_5 anodised at V_A = 3 V.



(a)



(b)

Fig. 4.16. (a) Output and (b) transfer characteristics of the fabricated OTFTs, including I_D, $I_D^{1/2}$ and I_G vs V_G at V_D = –1 V, respectively.

Table 4.2 compares the key figures-of-merit of the −1 V OTFTs fabricated in this work in comparison with one-volt organic TFTs we reported previously [197][250][261]. As can be seen, the gate capacitance density of the developed OTS-treated Ta_2O_5 dielectric layer used here is significantly higher. Importantly, other transistor parameters are comparable or indeed better than the parameters of the state-of-the-art organic TFTs reported to date [262][263][264]. As a result, the demonstrated organic transistors are promising candidates for use in low-voltage, portable electronics.

Parameters	20 V Untreated	3 V OTS-Treated	[193]	[249]	[261]
Dielectric	Ta_2O_5	Ta_2O_5	ODTS/Al_2O_3	BST-P	BST-CEC/PVP
C_G (nF/cm^2)	700	670	550	94	40
Mobility (cm^2 V^{-1}s^{-1})	0.02	0.22	0.1	0.14	0.3
V_{th} (V)	−0.35	−0.55	−0.45	−0.5	−0.7
SS (mV/dec)	220	120	160	221	140
ON/OFF Current Ratio	10^3	5×10^3	10^3	10^3	10^3
Operating voltage (V)	−1	−1	−1	−1	−1.5

Table 4.2. Performance comparison of the proposed DPPDTT-PMMA OTFTs with their counterparts in the literature.

4.1.4 Conclusion

In conclusion, solution-processed, low threshold voltage organic thin-film transistors that can be operated at 1 V have been demonstrated. The low operational voltage was achieved by using extremely thin (~7 nm), anodised Ta_2O_5 films that were modified by the application of an OTS SAM. The optimised DPPDTT-PMMA TFTs display threshold voltages around −0.55 V, low subthreshold slopes 120 mV/dec, operate with negligible hysteresis and possess average saturated field-effect mobility in excess of 0.2 cm^2 V^{-1} s^{-1} at −1 V. This approach has a high potential to enable the design of stable, ultra-low voltage organic semiconductor circuitry in a highly reproducible manner.

4.2 Low-voltage n-channel a-IGZO TFTs gated with OTS-modified Anodic Ta_2O_5

4.2.1 Introduction

High-κ materials have typically received much attention for two main reasons. On the one hand, silicon dioxide (SiO_2), as the conventional dielectric, has reached its fundamental material limits and hindered the continuous downscaling and increasing the performance of high-yield transistors based on Moore's law due to relatively low dielectric constant (~ 3.9). On the other hand, SiO_2 cannot be utilised in unconventional applications where cost and power consumption are the two main concerns. This is mainly due to the lack of

processibility at room temperature and demand for further dielectric thickness reduction, which requires dielectrics with a higher dielectric constant. This leads to induce the same capacitance with a thicker dielectric thickness.

Moreover, silicon (Si) as the preferred semiconductor material is not suitable for novel applications such as transparent and flexible, large-area devices in terms of the material properties and the limitation of fabrication methods [58]. Therefore, oxide semiconductors, and in particular, amorphous indium-gallium-zinc-oxide (a-IGZO), possess excellent properties such as high charge carrier mobility, good uniformity and low-temperature processing. These properties of oxide semiconductors have drawn much attention to respond to the high demand for high-performance, transparent and flexible large-area devices. Since its first appearance by Nomura *et al.* [24], polycrystalline IGZO has been used in a variety of applications such as displays, sensors and battery-powered electronics. In particular, for the application of IGZO in portable devices, it is highly desirable for TFTs to operate at voltages at or below 1 V. In this study, solution-processed, ultra-thin anodic Ta_2O_5 dielectrics are proposed and then optimised for realising high-performance 1 V a-IGZO TFTs, which can be used for a wide range of applications such as aqueous sensors or ultra-low-power electronics.

4.2.2 Experimental procedure

To optimise the performance of Ta_2O_5 and Ta_2O_5/OTS films for using in a-IGZO TFTs, first, metal-insulator-metal (MIM) capacitors were fabricated. MIM capacitors with Ta/Ta_2O_5/Al and Ta/Ta_2O_5/OTS/Al structures were fabricated on 2 × 1.5 cm^2 ultra-flat quartz coated glass substrates (Ossila, UK). Firstly, the substrates were rinsed with deionised water in order to remove any water-soluble contaminants and dried with compressed N_2. Next, the slides were sonicated for 30 min in acetone, methanol and isopropyl alcohol (IPA). Then, the glass slides were taken from the sonic bath and again dried with pure N_2. To

remove any residual organic contaminants, the substrates were put into UV/Ozone cleaner for 30 min. The fabrication of the MIM capacitors and IGZO TFTs started with depositing a 100 nm thick layer of Ta through a shadow mask by using radio frequency (RF) magnetron sputtering with a 2-inch diameter Ta target (Kurt J. Lesker, 99.9% pure) at a power of 70 W in a pure Ar atmosphere with a total pressure of 0.5 Pa at room temperature. Next, the patterned Ta was oxidised using the anodisation process to form a thin Ta_2O_5 film. The anodisation process was carried out in 1 mM citric acid, which served as the electrolyte. A pure Au wire (99.999%) and the patterned Ta film were used as the cathode and the anode, respectively [248]. To form Ta_2O_5 films with different thicknesses, various anodisation voltages V_A = 20, 15, 10, and 5 V and a constant current density J_A = 0.01 mA/cm^2 were applied using a Keithley 2400 Source Meter. The anodisation was carried out until J_A dropped to 0.005 mA/cm^2. Then, the samples were rinsed with deionised water and dried using pure N_2. Based on the anodisation ratio of tantalum ($[c]_{Ta}$ = 2.2 ± 0.2 nm/V), the Ta_2O_5 thicknesses for 20, 15, 10, and 5 V anodisation voltages were approximately 44 ± 4, 33 ± 3, 22 ± 2, and 11 ± 1 nm, respectively. To study the effect of OTS on the dielectric properties of the anodically oxidised Ta_2O_5 films, some of the as-prepared Ta/Ta_2O_5 samples were treated by O_2 plasma for 2 min and then immersed in 5 mM of fresh OTS solution (Sigma-Aldrich, ≥ 99.5%) in anhydrous toluene for 30 min in ambient conditions. Afterwards, the substrates were taken from the OTS solution and promptly rinsed with fresh toluene, acetone and IPA and blow-dried with compressed N_2. Finally, the OTS-treated samples were placed on a hot plate at ~150 °C under a flow of N_2 for 2 h. To finish MIM capacitors, a 100 nm thick, 1000 μm × 100 μm layer of Al was thermally evaporated through a shadow mask to form the top electrode of the devices (the total area of capacitors including the connection to the contact pads was 1.70 × 10^{-3} cm^2). Fig. 4.17 depicts the fabrication process of Ta/Ta_2O_5/Al and Ta/Ta_2O_5/OTS/Al.

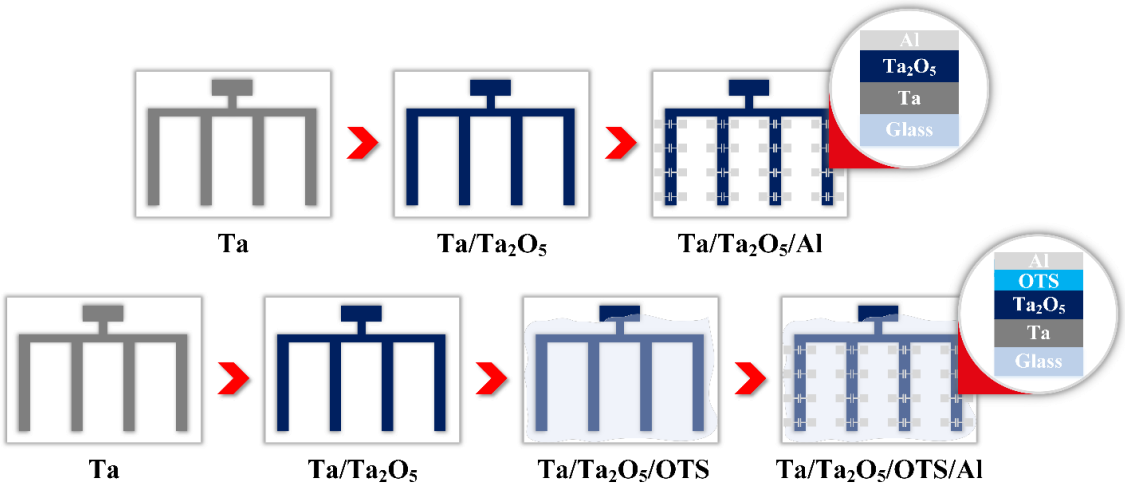


Fig. 4.17. The schematic of the fabrication process of MIM capacitors with (a) untreated Ta_2O_5 (b) OTS-treated Ta_2O_5

To confirm the reproducibility of the measured dielectric parameters, 100 Ta/Ta_2O_5/Al and 100 Ta/Ta_2O_5/OTS/Al MIM capacitors for each Ta_2O_5 film anodised with V_A = 20, 15, 10, and 5 V were fabricated and 20 of each lot were randomly chosen for the measurements. To complete the fabrication of IGZO TFTs, a 25 nm thick layer of IGZO was firstly deposited onto the as-prepared Ta/Ta_2O_5 and OTS-treated Ta/Ta_2O_5 samples through a shadow mask by RF magnetron sputtering using a 2-inch diameter IGZO target (In:Ga:Zn = 1:1:1) at the power of 50 W at room temperature. Then, a 100 nm (1000 µm × 100 µm) Al film was deposited onto the IGZO films to form the drain/source contacts through a shadow mask. The transistor channel widths (W) and lengths (L) were 1000 µm and 30 µm, respectively. In order to test the TFT fabrication reproducibility, 50 Ta_2O_5/IGZO and 50 Ta_2O_5/OTS/IGZO TFTs for each Ta_2O_5 film anodised with V_A = 20, 15, and 10 V were fabricated and 20 of each TFTs were arbitrarily chosen for the measurements. Noteworthily, the electrical properties of fabricated MIM capacitors and electrical characterisation of the TFTs were measured at room temperature.

4.2.3 Results and discussion

In the first instance, OTS-treated 2 and 3 V anodised Ta_2O_5 films previously used as gate dielectrics in p-channel OTFTs are directly employed in a-IGZO TFTs to study their

performance in a-IGZO TFTs. Fig. 4.18 shows the representative output and transfer characteristics of a-IGZO TFTs using (a, b) 2 V anodised Ta_2O_5 (d ≈ 3.6 nm), (c, d) 3 V anodised Ta_2O_5 (d ≈ 5.4 nm). As can be seen, although both fabricated TFTs can operate at 1 V with high dielectric capacitance (> 600 nF/cm^2), other parameters such as the gate leakage current, threshold voltage and ION/OFF ratios are required to be considered as well. The gate leakage currents of both devices are significantly high, especially for 2 V anodised OTS-treated Ta_2O_5 film (~ 10 nA). The threshold voltages are also showing high values, which deteriorate the drain current on and off ratios ($I_{ON/OFF}$) which are indeed not comparable with their counterparts demonstrated in the literature [252]. This result is in good agreement with the previously published reports where it was shown that Ta_2O_5 as a single gate dielectric is not suitable for n-type oxide semiconductors due to its small band offset (discussed in section 2.3.3.1.1.2). On the other hand, using the ultrathin layer of Ta_2O_5 when its thickness is around the thickness of native tantalum oxide and/or the thickness of OTS (~ 2.6 nm) not only can increase the gate leakage current but also may worsen the device instability. Table 4.3 compares the key figures-of-merit of the IGZO TFTs fabricated using 2 V and 3 V OTS-treated Ta_2O_5 dielectrics. As shown, the mobilities of the fabricated TFTs are quite low compared with other low voltage IGZO TFTs reported elsewhere [252].

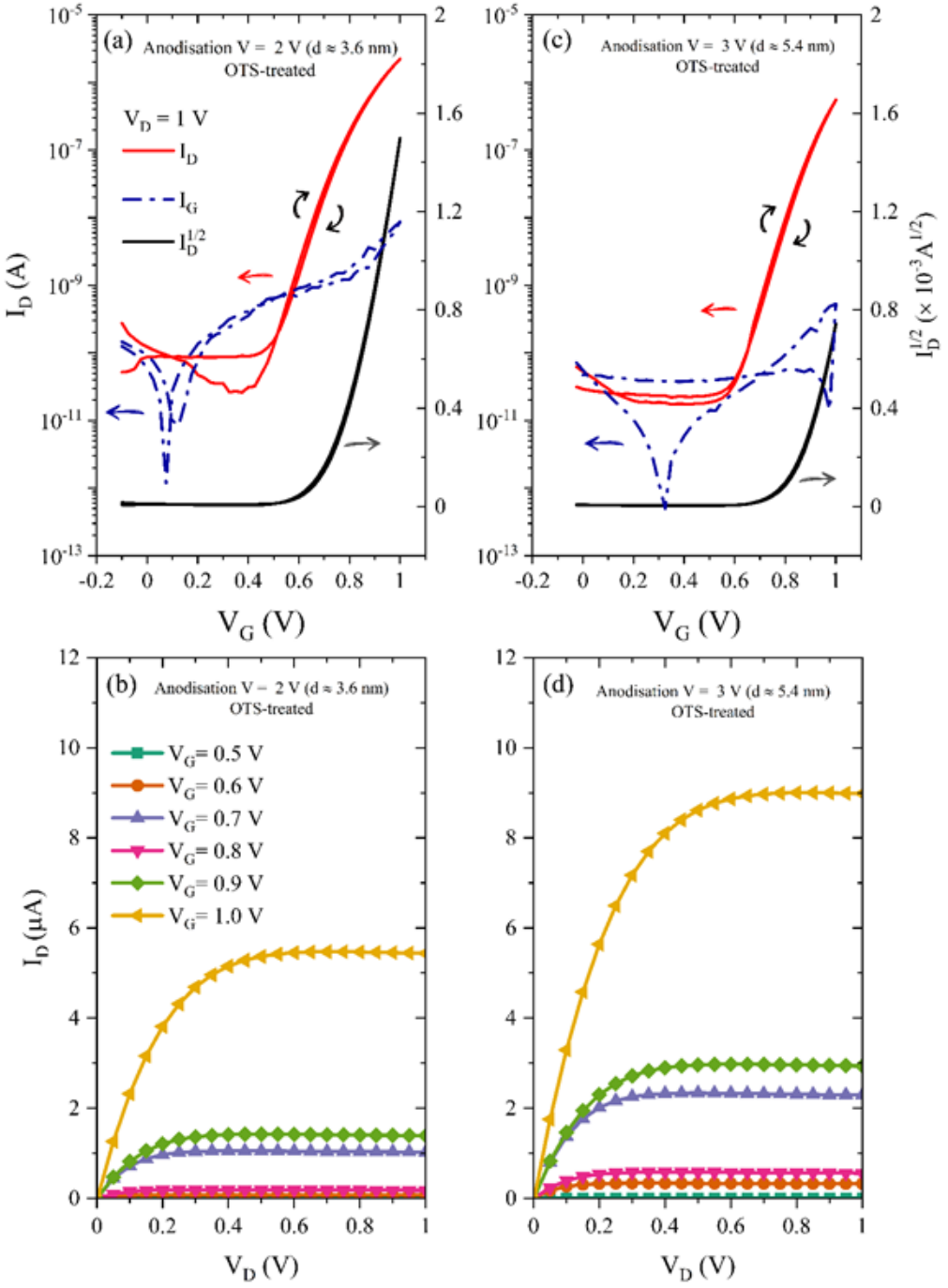


Fig. 4.18. The representative output and transfer characteristics of a-IGZO TFTs using (a, b) 2 V anodised Ta_2O_5 (≈ 3.6 nm), (c, d) 3 V anodised Ta_2O_5 (≈ 5.4 nm).

Device	2 V OTS-treated	3 V OTS-treated
V_A (V)	2	3
Approx. Ta_2O_5 thickness (nm)	3.6 + ~ 2.8 (OTS)	5.4 + ~ 2.8 (OTS)
Capacitance density (nF/cm^2)	490	670
I_D @ V_G = 1 V	2 µA	9 µA
I_{LEAK} @ V_G = 1 V	9 nA	1 nA
µ (cm^2 V^{-1} s^{-1})	2	0.9
V_O (mV)	500	600
V_{th} (V)	0.7	0.8
SS (mV/dec)	102	86
I_{off} @ V_G = 0 V	0.1 nA	0.1 nA
$I_{ON/OFF}$	10^4	10^4
D_{it} (cm^{-2} eV^{-1})	2.1×10^{12}	2.6×10^{13}

Table 4.3. The electrical properties of the fabricated a-IGZO TFTs using 2 and 3 V anodised OTS-treated Ta_2O_5 dielectrics.

Therefore, in order to obtain high-performance thin-film transistors, the optimisation of the gate dielectric properties is essential and should be carried out specifically for the developed devices, herein, a-IGZO TFTs. Consequently, different thicknesses of Ta_2O_5 films were grown by varying the anodisation voltage (V_A) from 20 to 5 V in the step of 5 V. To confirm the reproducibility of the measured dielectric parameters, 20 Ta/Ta_2O_5/Al MIM capacitors for each Ta_2O_5 film anodised with V_A = 20, 15, 10, and 5 V were randomly chosen from 100 fabricated devices. Fig. 4.19 illustrates the capacitance density (C_i) vs frequency of the capacitors from 100 Hz to 100 kHz. As shown, decreasing the anodisation voltage (V_A) from 20 V to 5 V increases the capacitance density (C_i) from 585 nF/cm^2 to 1840 nF/cm^2 with a maximum standard deviation of 20 nF/cm^2 at 1 kHz. However, as the V_A decreases from 20 to 5 V, the measured values of C_i from 100 Hz to 100 kHz become unstable, especially at high-end frequency range. This is particularly obvious for Ta_2O_5 anodised at 5 V. This behaviour of C_i is very likely due to the increase of the leakage current through the dielectric.

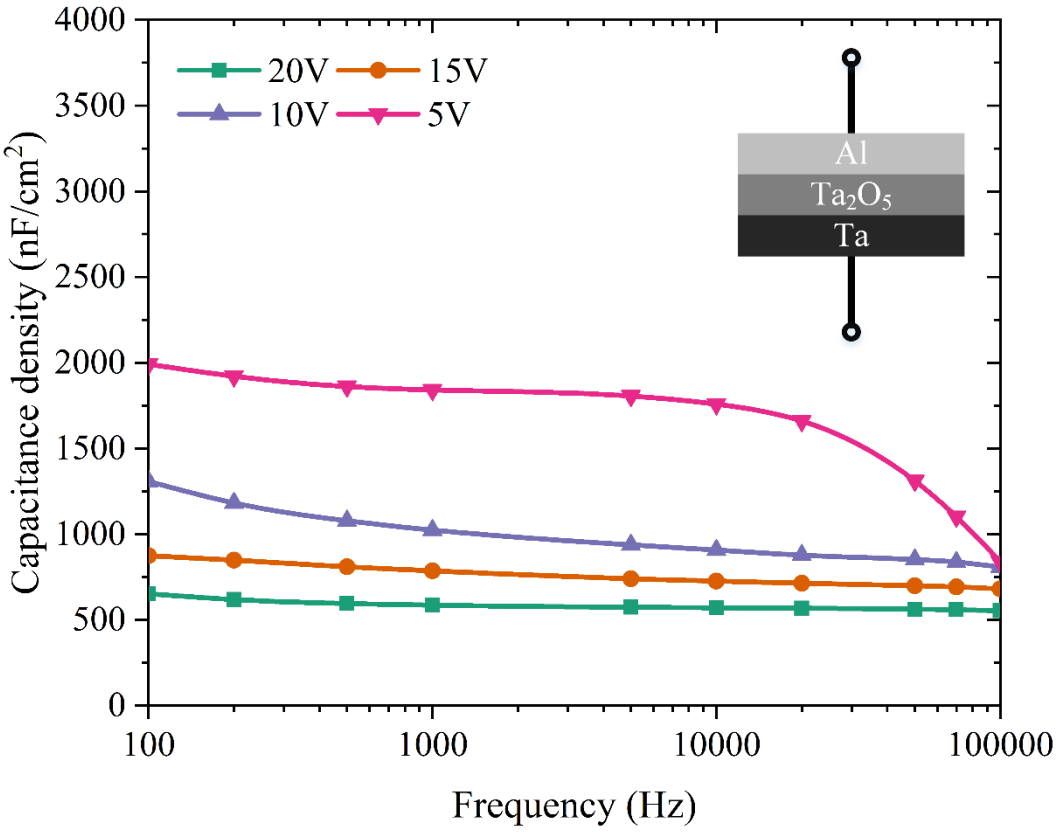


Fig. 4.19. Capacitance density vs frequency of the studied Ta/Ta_2O_5/Al capacitors.

Indeed, as shown in Fig. 4.20, the leakage current density (J_{LEAK}) rises sharply by at least three orders of magnitude when measured at 1 V from 2.8×10^{-5} A/cm^2 for 20 V to 0.1 A/cm^2 for 5 V anodised Ta_2O_5, respectively. High J_{LEAK} is extremely undesirable because it strongly influences the characteristics of MIM capacitors, as well as the operation of TFTs. It is worth mentioning here that the leakage current density, measured for the fabricated capacitors with the structure of Ta/Ta_2O_5/Al and Ta/Ta_2O_5/Au may not exhibit similar behaviour. This is very likely caused by the use of electrodes with different work functions and differences in the roughness of the Ta_2O_5/Au and Ta_2O_5/Al interfaces [260]. The negative effect of the leakage current on the capacitor characteristics is reflected in Fig. 4.21 where Ta_2O_5 anodised at 5 V shows a considerable deterioration of the loss tangent (tan(δ)) at both ends of the probed frequency range.

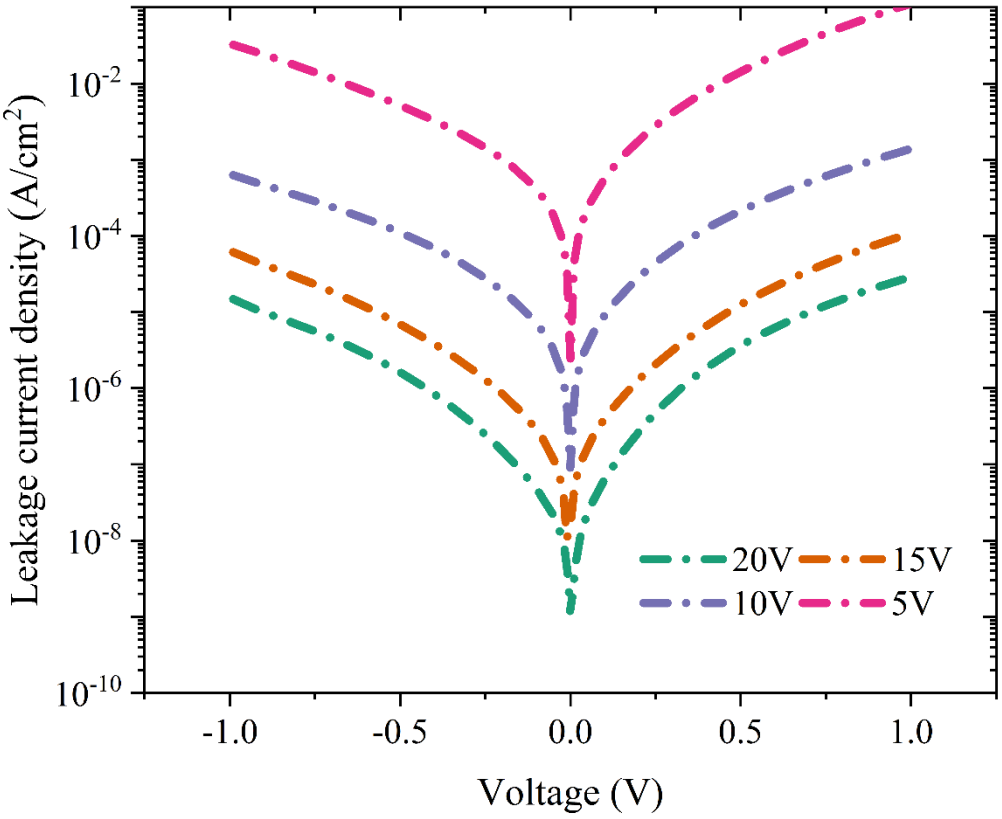


Fig. 4.20. Leakage current density vs applied voltage of the studied Ta/Ta_2O_5/Al capacitors.

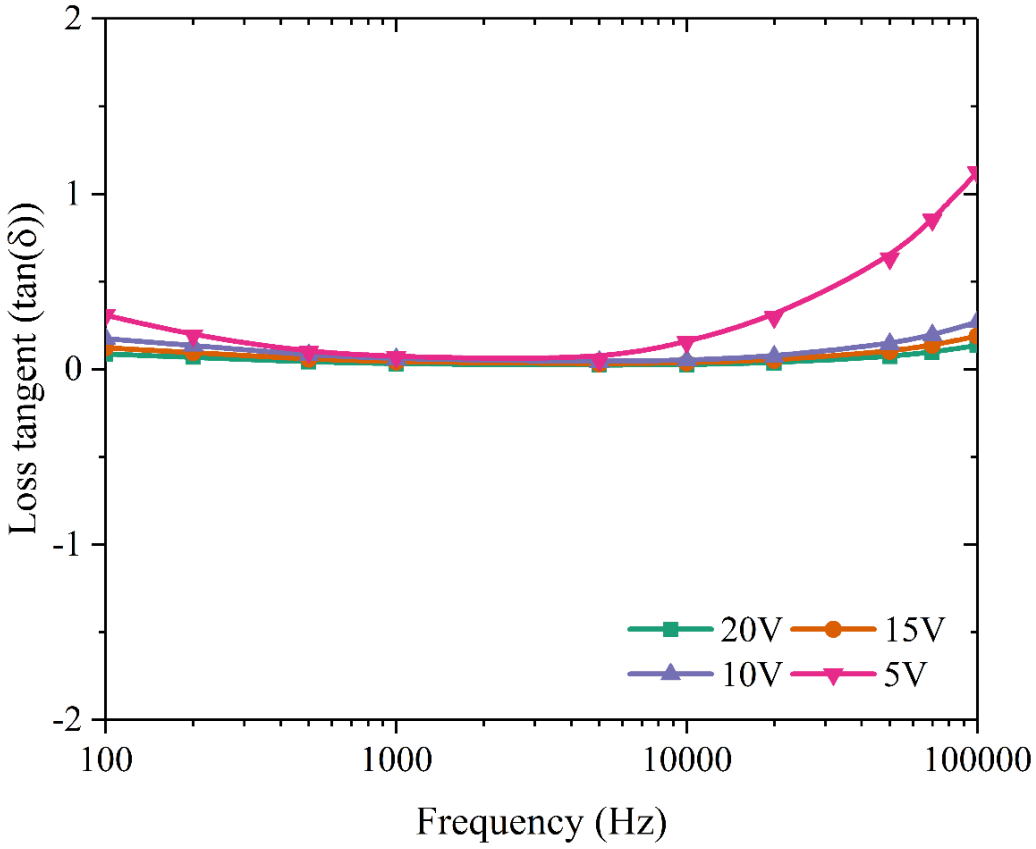


Fig. 4.21. Loss tangent vs frequency of the studied Ta/Ta_2O_5/Al capacitors.

Fig. 4.23 presents a cross-section of the fabricated bottom-gate, top-contact IGZO TFTs

(Ta/Ta_2O_5/IGZO/Al). Representative output and transfer characteristics of the devices using the Ta_2O_5 anodised at 10 V (~22 ± 2 nm, device A), 15 V (~33 ± 3 nm, device B), and 20 V (~44 ± 4 nm, device C) are shown in Fig. 4.24 (a–f), respectively. As demonstrated in Fig. 4.24, all three types of transistors operate at 1 V in n-channel enhancement mode and show a clear linear, pinch-off and saturation regimes with a very small hysteresis between forward (−0.1 to 1 V) and backward (1 to −0.1 V) sweeps. The drain current (I_D) measured at the drain voltage (V_D) and the gate voltage (V_G) equal to 1 V (V_S = 0) for device A is found to be about 18 µA. This is almost two times higher than for device B and more than three times higher than for device C. Although high I_D is one of the most important parameters when considering the performance of TFTs, other transistor parameters such as leakage current (I_{LEAK}), field-effect mobility (µ), threshold voltage (V_{th}), subthreshold swing (SS), onset voltage (V_O), off current (I_{OFF}), and on/off current ratio ($I_{ON/OFF}$) should also be considered. The mobility in the saturation regime has been estimated using the drain current equation by applying a linear fit to the $I_D^{1/2}$ vs V_G as shown Eq. 2.7.

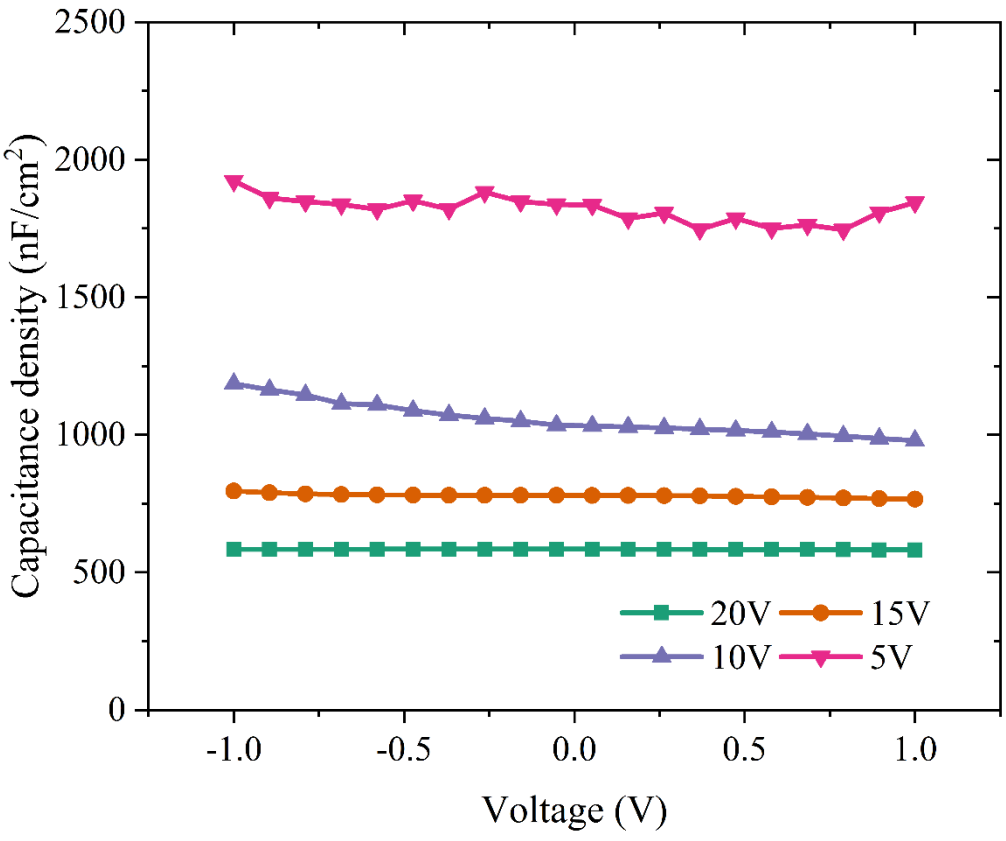


Fig. 4.22. Capacitance density vs voltage characteristics of the studied Ta/Ta_2O_5/Al capacitors.

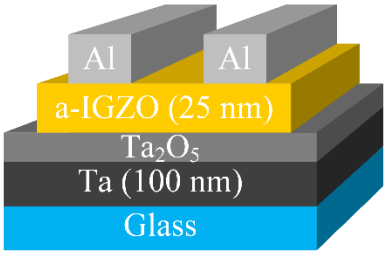


Fig. 4.23. The schematic structure of the fabricated Ta/Ta_2O_5/IGZO/Al TFTs using pristine Ta_2O_5 gate dielectric.

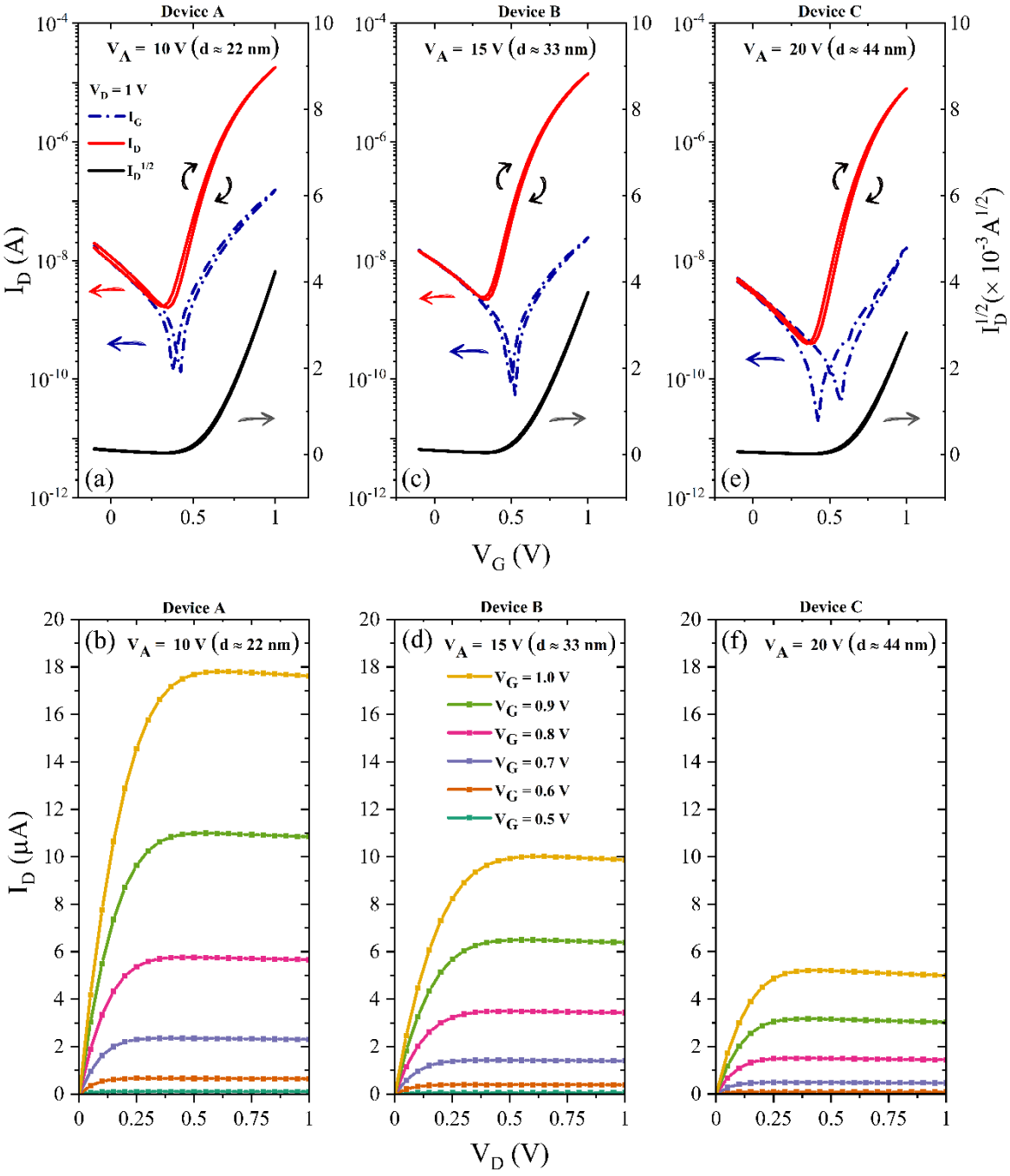


Fig. 4.24. The representative output and transfer characteristics of a-IGZO TFTs using (a, b) 10 V anodised Ta_2O_5 (22 ± 2 nm, device A), (c, d) 15 V anodised Ta_2O_5 (33 ± 3 nm, device B), and (e, f) 15 V anodised Ta_2O_5 (44 ± 4 nm, device C).

In addition, to be able to compare the quality of the semiconductor-insulator interface of the fabricated transistors, the interfacial trap density (D_{it}) is calculated using Eq. 2.14. Table 4.3 shows all key parameters of the fabricated IGZO TFTs.

Device	A	B	C
V_A (V)	10	15	20
Approx. Ta_2O_5 thickness	22 ± 2 nm	33 ± 3 nm	44 ± 4 nm
Capacitance density (nF/cm^2)	1020	875	585
I_D @ V_G = 1 V	18 µA	10 µA	5 µA
I_{LEAK} @ V_G = 1 V	150 nA	20 nA	8 nA
µ (cm^2 V^{-1} s^{-1})	5.9	5.8	6.3
V_O (mV)	350	350	400
V_{th} (V)	0.58	0.54	0.65
SS (mV/dec)	108	111	96
I_{off} @ V_G = 0 V	9.3 nA	9.5 nA	2.7 nA
$I_{ON/OFF}$	10^3	2×10^3	5×10^3
D_{it} (cm^{-2} eV^{-1})	4.1×10^{12}	4.4×10^{12}	2.1×10^{12}

Table 4.4. The electrical properties of the fabricated a-IGZO TFTs using different, as prepared, anodically oxidised Ta_2O_5 dielectrics.

It can be seen that device C displays the highest mobility μ_{sat} = 6.3 cm^2 V^{-1} s^{-1}. At the same time, it shows the highest V_{th} = 0.65 V and the lowest SS = 96 mV/dec. It is believed that charge carrier mobility in TFTs is directly affected by the interfacial trap density [265]. D_{it} is calculated to be 4.1×10^{12}, 4.4×10^{12}, and 2.1×10^{12} cm^{-2} eV^{-1} for device A, B, and C, respectively. Indeed, since the device C has the lowest interfacial trap density, it exhibits the highest mobility. Also, since the capacitance density of device C is lowest (C_i = 585 nF/cm^2) it shows the highest V_{th}. On the contrary, it appears that significantly reduced channel capacitance, which is a sum of the depletion capacitance (C_{dep}) and the interface trap capacitance (C_{it}) being related to the charging of the dielectric/semiconductor interface traps, contributes to the low SS [62]. Indeed, the SS in device C is reduced to 96 mV/dec. Although 1 V operation was achieved for all types of the fabricated a-IGZO TFTs using pristine Ta_2O_5, it was believed that the Ta_2O_5 dielectric needed further optimisation to be able to compete with the recently demonstrated state-of-the-art a-IGZO TFTs [129][266].

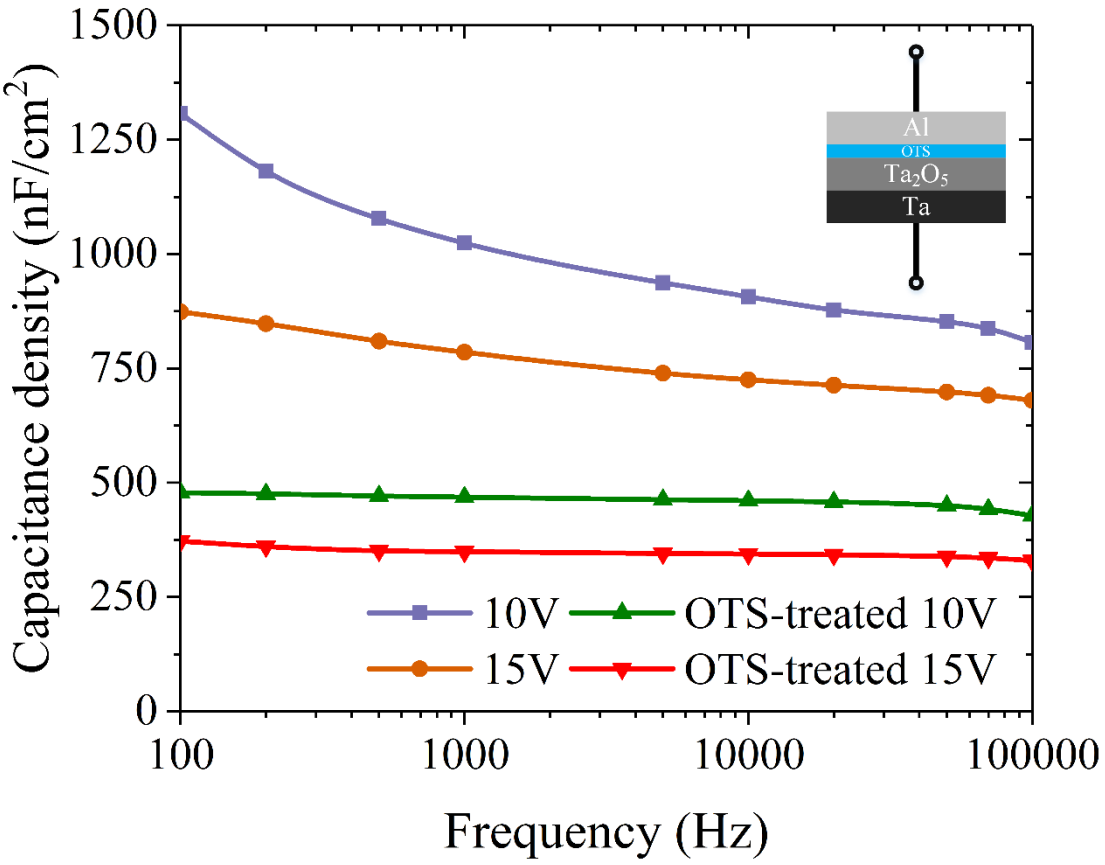


Fig. 4.25. Capacitance density vs frequency of the studied Ta/Ta_2O_5/OTS/Al capacitors.

As mentioned before, it has been reported previously that the passivation of metal oxide dielectrics with *n*-octadecyltrichlorosilane (OTS) SAM is an effective approach to improve the performance of OTFTs [248]. Therefore, to see if a SAM treatment has the same beneficial effect on the performance of Ta_2O_5 thin film capacitors, 15 V (33 ± 3 nm) and 10 V (22 ± 2 nm) anodised Ta_2O_5 films have been modified with OTS. To confirm the reproducibility of the measured dielectric parameters, 20 Ta/Ta_2O_5/OTS/Al MIM capacitors for each Ta_2O_5 film anodised with V_A = 20, 15, 10, and 5 V were randomly chosen from 100 fabricated devices. Fig. 4.25 demonstrates the capacitance density of Ta/Ta_2O_5/Al and Ta/Ta_2O_5/OTS/Al capacitors (cf. inset of Fig. 4.25) as a function of frequency from 100 Hz to 100 kHz.

As can be seen, the Ta/Ta_2O_5/OTS/Al capacitors are much more stable in the whole studied frequency range than the capacitors with pristine Ta_2O_5. Although adding a monolayer dielectric layer to the main dielectric appears to make the MIM capacitors more stable, this

increases the overall thickness of the dielectric, and as a consequence, decreases the capacitance density. This is due to adding an extra layer (OTS) to the main dielectric (Ta_2O_5) which are equivalent to two capacitors in series. Before OTS surface modification, the capacitance density of 15 V and 10 V Ta_2O_5 films at 1 kHz is 875 nF/cm^2 and 1020 nF/cm^2, respectively. As expected, after the OTS treatment, the capacitance density is reduced to 350 and 470 nF/cm^2 with a maximum standard deviation of 20 nF/cm^2 at 1 kHz, respectively.

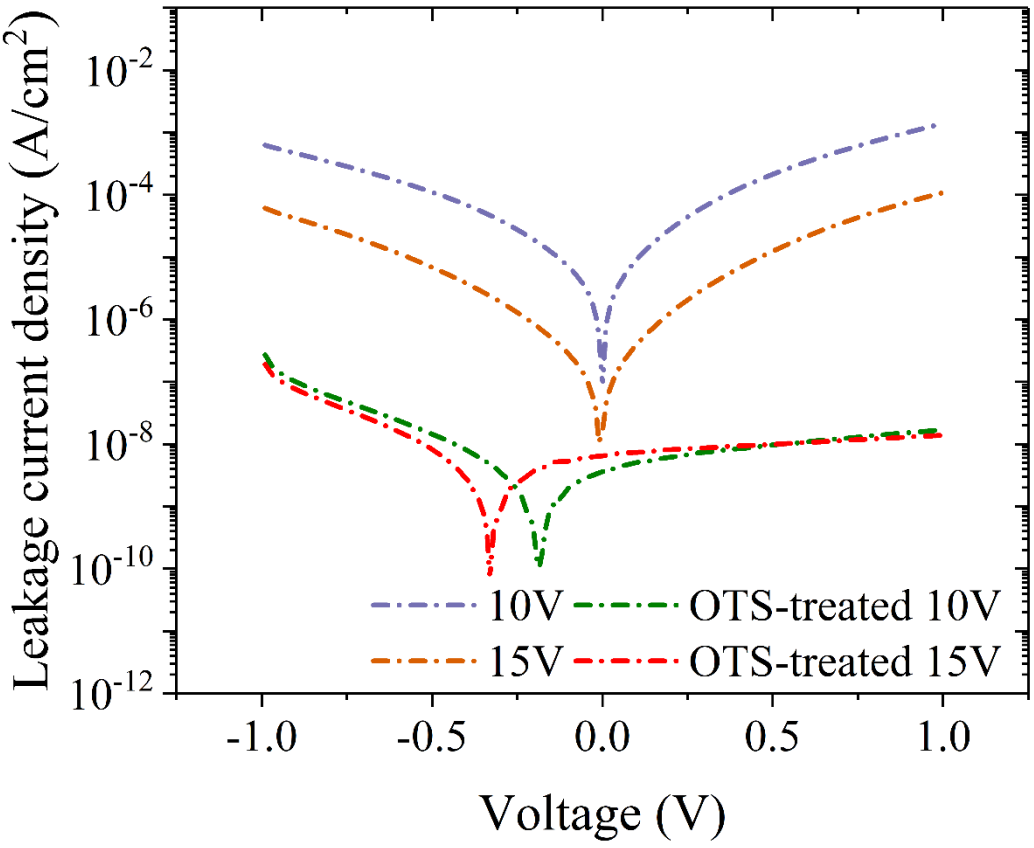


Fig. 4.26. Leakage current density vs frequency of the studied Ta/Ta_2O_5/OTS/Al capacitors.

Fig. 4.26 shows the leakage current density of Ta_2O_5 and OTS-treated Ta_2O_5 films vs applied voltage bias from −1 to 1 V. As it is clear, the leakage current density of OTS-treated samples at ± 1 V has been dramatically reduced and found to be at least three orders of magnitude lower than their untreated counterparts. The leakage current of the OTS-treated Ta_2O_5 is somewhat asymmetric and slightly lower for positive voltages. This is very likely caused by the differences in the roughness of the Ta/Ta_2O_5 and Ta_2O_5/OTS interfaces and the use of electrodes with different work functions [260]. Fig. 4.27 shows the loss tangent

as a function of frequency for both samples. Due to the lower leakage current in OTS-treated samples, tan(δ) is also showing a lower value which implies that the dielectric loss of these capacitors approaches the ideal value for this parameter.

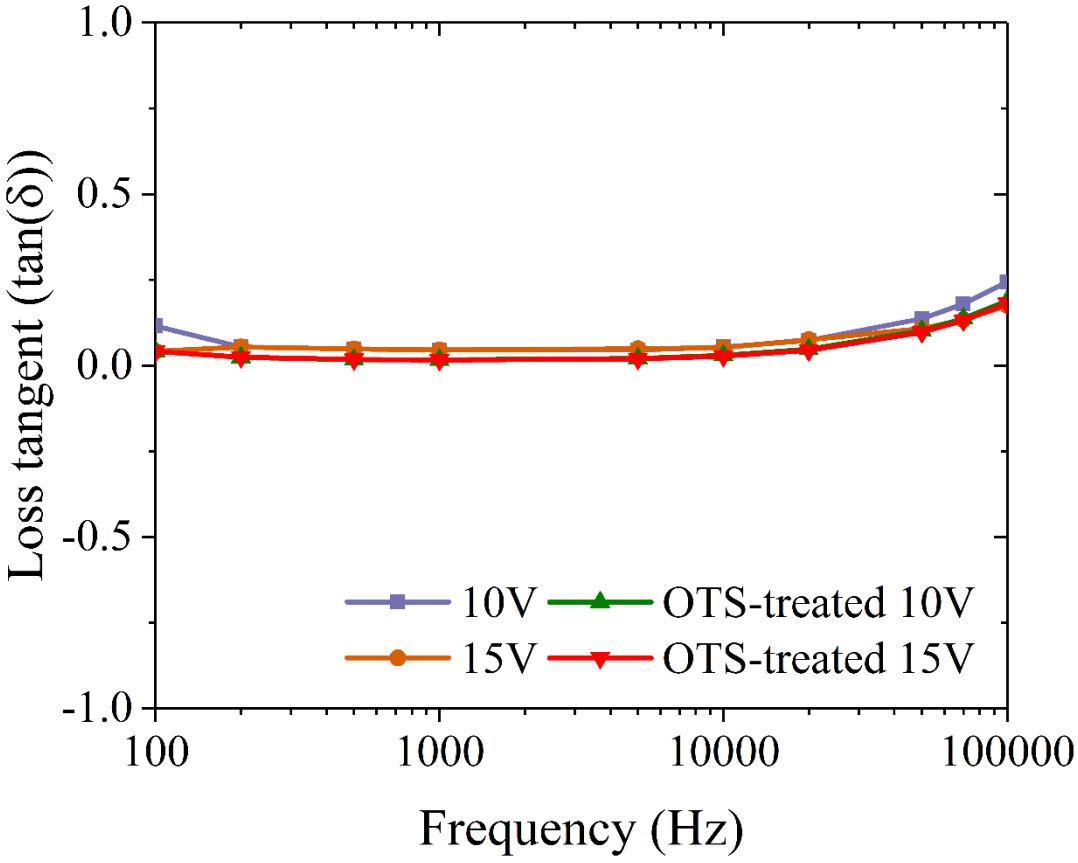


Fig. 4.27. Loss tangent (δ) vs frequency of the studied Ta/Ta_2O_5/OTS/Al capacitors.

This fact is also reflected in the capacitance density vs voltage characteristics presented in Fig. 4.28. Conversely, the OTS-treated Ta_2O_5 films show a constant value of C_i in the −1 to 1 voltage bias range the pristine Ta_2O_5 films appear somewhat unstable.

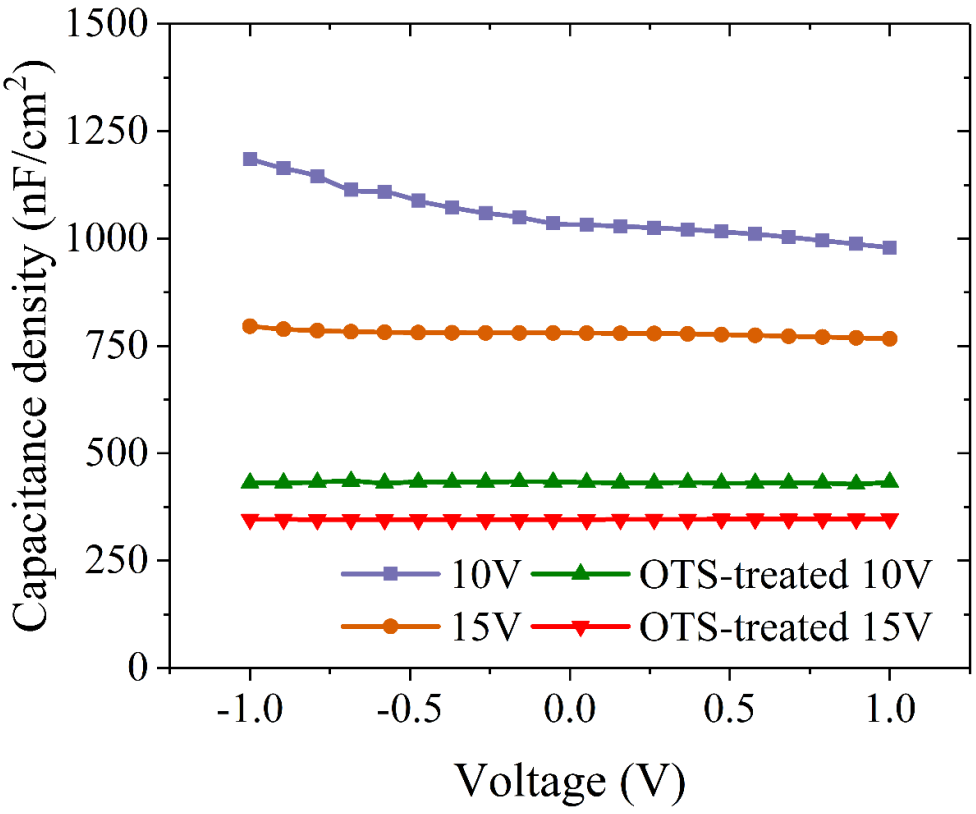


Fig. 4.28. Capacitance density vs voltage characteristics of the studied Ta/Ta_2O_5/OTS/Al capacitors.

To see if the OTS-treated Ta_2O_5 dielectric can improve the performance of IGZO TFTs, Ta/Ta_2O_5/OTS/IGZO/Al TFTs with 10 V (22 ± 2 nm) and 15 V (33 ± 3 nm) anodised Ta_2O_5 dielectrics were fabricated (Fig. 4.29).

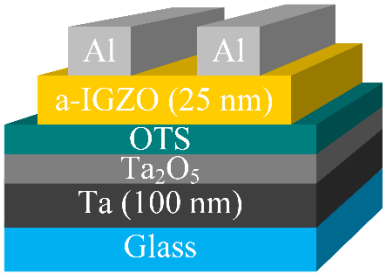


Fig. 4.29. The schematic structure of the fabricated Ta/Ta_2O_5/OTS/IGZO/Al TFTs using SAM-modified Ta_2O_5 gate dielectric.

The key parameters of the fabricated IGZO TFTs gated with OTS-treated, 10 V and 15 V anodised Ta_2O_5 are summarised in Table 4.4. As shown in Fig. 4.30 (a) and (b), the devices operate in n-type enhancement mode with clear linear, pinch-off and saturation regimes.

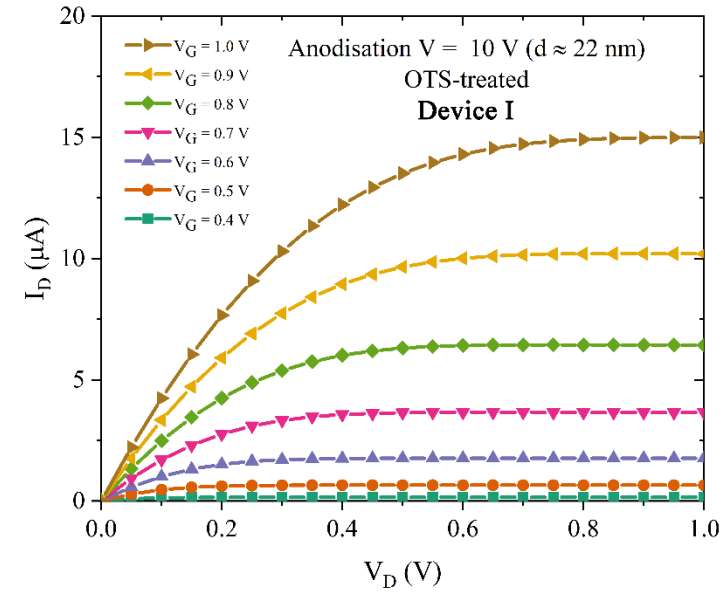
The clear linear increment of I_D with V_D at low V_G implies that low resistance contacts were formed between IGZO and Al.

Parameter	Device I	Device II
V_A (V)	10 V	15 V
Approx. Ta_2O_5 + OTS thickness	(22 ± 2) + 2.8 nm	(33 ± 3) + 2.8 nm
Capacitance density (nF/cm^2)	470	350
I_D @ V_G = 1 V	15 µA	0.04 µA
I_{LEAK} @ V_G = 1 V	0.1 nA	0.03 nA
µ (cm^2 V^{-1} s^{-1})	2.3	0.04
V_O (mV)	100	550
V_{th} (V)	0.4	0.6
SS (mV/dec)	88	120
I_{off} @ V_G = 0 V	0.1 nA	0.05 nA
$I_{ON/OFF}$	5×10^5	10^3
D_{it} (cm^{-2} eV^{-1})	1.3×10^{12}	2.1×10^{12}

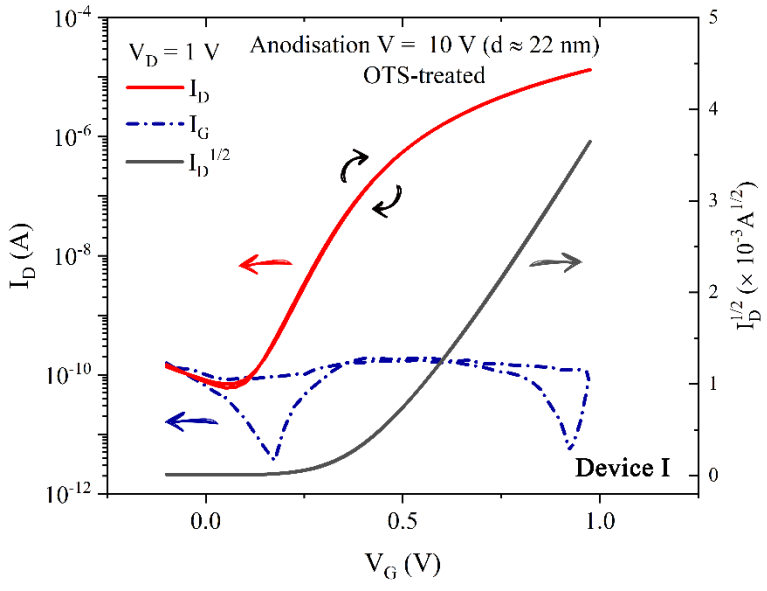
Table 4.5. Electrical properties of the fabricated a-IGZO TFTs using OTS-modified, anodically oxidised Ta_2O_5 dielectrics.

From Fig. 4.30(b), the mobility, the threshold voltage, the subthreshold swing, and $I_{ON/OFF}$ ratio are found to be 2.3 cm^2 V^{-1} s^{-1}, 0.4 V, 88 mV/dec, and > 10^5, respectively. Comparing the transistors with IGZO TFTs using pristine Ta_2O_5, the mobility is reduced by a factor of three. This is very likely caused by the different structure and composition of IGZO on Ta_2O_5 and T_2O_5/OTS surfaces or OTS coating deterioration. The calculated interfacial trap densities (D_{it}) for both types of transistors suggest that TFTs using OTS-modified Ta_2O_5 possess fewer interfacial traps than TFTs using pristine Ta_2O_5. However, more detailed studies of the SAM/IGZO interfaces are needed to understand this phenomenon thoroughly. The gate leakage current (I_G) is found to be about 0.1 nA at 1 V, which is at least two orders of magnitude smaller than in our Ta_2O_5/IGZO TFTs (cf. ref. [267]). On the other hand, Although device II, shown in Fig. 4.31 (a-b), has the minimum characteristics of a working low-power TFT, namely, a clear linear, pinch-off and saturation regime, it suffers from insufficient output current (nA scale), which makes impractical device to be used in the applications needed higher currents. Also, it suffers from low mobility and $I_{ON/OFF}$, high

threshold voltage (V_{th}) and negative resistance in drain current output. Although the origin of negative resistance in the output characteristics is yet unclear, it could be very likely due to the geometry of the device and the different values of the dielectric constants of the semiconductor and dielectric [268].

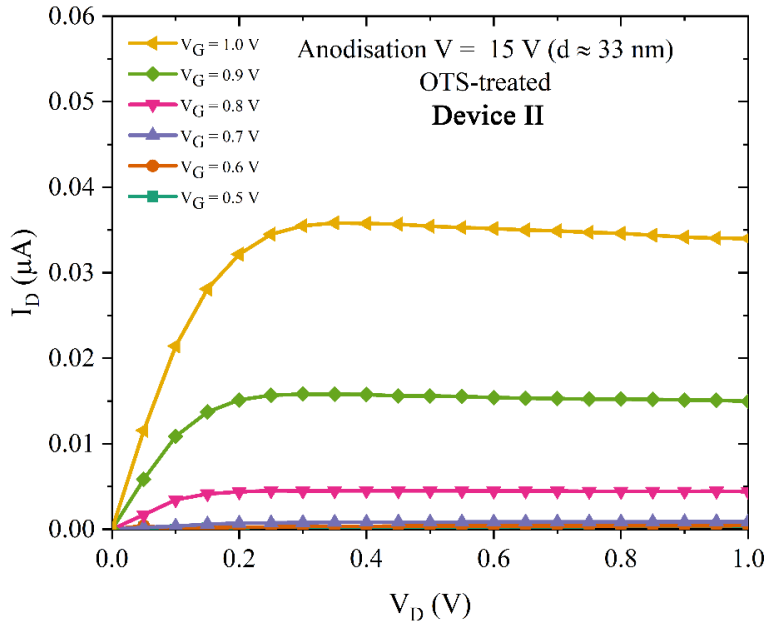


(a)

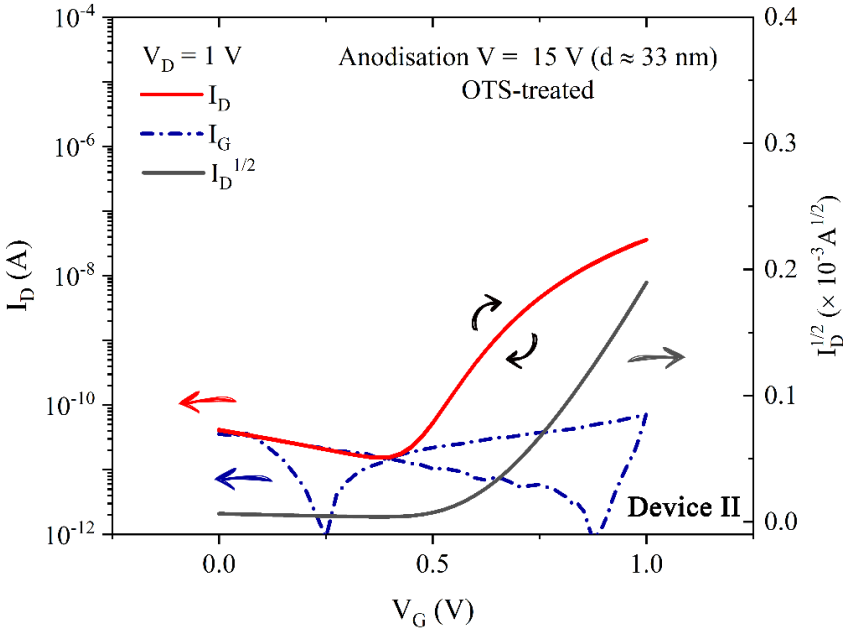


(b)

Fig. 4.30. The representative (a) output and (b) transfer of IGZO TFTs gated with OTS-treated, 10 V anodised Ta_2O_5.



(a)



(b)

Fig. 4.31. A representative (a) output and (b) transfer characteristics of a-IGZO TFTs gated with OTS-treated, 15 V anodised Ta_2O_5.

Recently reported IGZO TFTs using 10 nm CVD SiO_2 as the gate dielectric display $I_G < 1$ pA [269]. However, the area of the drain and source contacts here is at least 100 times larger than in ref. [269]. Also, it is not obvious if the anodically oxidised Ta_2O_5 films with thicknesses at or below 20 nm are stoichiometric Ta_2O_5 which may lead to the increased conductivity of such films [270]. As a result, the performance and application of the

demonstrated TFTs are currently somewhat limited by the gate leakage (i.e., high off current) and a significant reduction of the drain/source contact area along with further measurements are required to confirm their suitability, uniformity and stability for their use in displays. However, the onset voltage of the OTS-treated Ta_2O_5 a-IGZO TFTs is reduced to 100 mV, the threshold voltage is decreased to 0.4 V, and the subthreshold swing is below 90 mV/dec. Hence, it appears that the modification of the tantalum pentoxide with SAMs may be a useful approach towards ultra-low voltage, high-performance IGZO TFTs.

4.2.4 Conclusion

Low threshold voltage (V_{th}) a-IGZO TFTs gated with pristine and OTS-treated Ta_2O_5 operating at 1 V are demonstrated. The effect of different anodisation voltages on the properties of Ta/Ta_2O_5/Al and Ta/Ta_2O_5/OTS/Al MIM capacitors and IGZO TFTs have been studied. It is shown that the best-performing capacitors and transistors are realised with 10 V anodised (22 ± 2 nm), OTS-treated Ta_2O_5. The fabricated Ta_2O_5/OTS capacitors show good stability in the 100 Hz to 100 kHz and capacitance density in excess of 400 nF/cm^2. The fabricated TFTs display relatively high mobilities (2.3 cm^2 V^{-1} s^{-1}) compared to their counterparts operating at 1 V, threshold voltages around 0.4 V, subthreshold swings below 90 mV/dec, and high current on/off ratios in excess of 10^5. It is envisaged that this approach is a very promising alternative to fabricate low-voltage, inexpensive TFTs and TFT-arrays for low-cost sensors and low-end, disposable electronics.

Chapter 5: Memristive Devices Based on Anodic Ta_2O_5 Films

5.1 Introduction

The concept of a resistive memory device (also known as a memristive device) was initially postulated by Leon Chua in 1971 as the fourth fundamental circuit element [271]. The resistance of this type of devices can be changed upon electrical stimuli and last for short- or long-time scales. A memristor in its simplest structure is based on a two-terminal MIM structure where a switching medium is sandwiched between two electrodes. Fig. 5.1 illustrates the MIM structure of a memristor. Typically, the resistive switching in these devices involves the creation and rupture of conductive filaments (CF) connecting the two electrodes. These devices have two states of operation, the low-resistance state (LRS) and high-resistance state (HRS). LRS occurs when a CF inside the active insulating layer bridges the two electrodes, while HRS is realised by partial dissolution of the filament. Fig. 5.2 demonstrates the formation and partial dissolution of the filament [272].

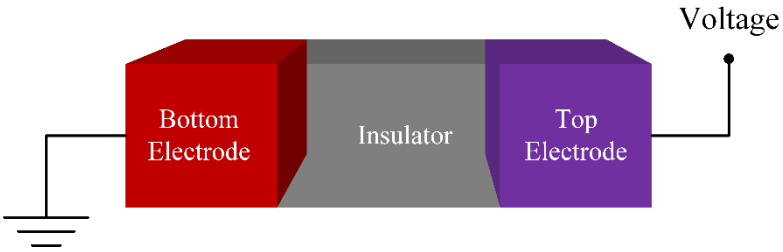


Fig. 5.1. The schematic of a typical memristive device with a Metal-Insulator-Metal (MIM) structure.

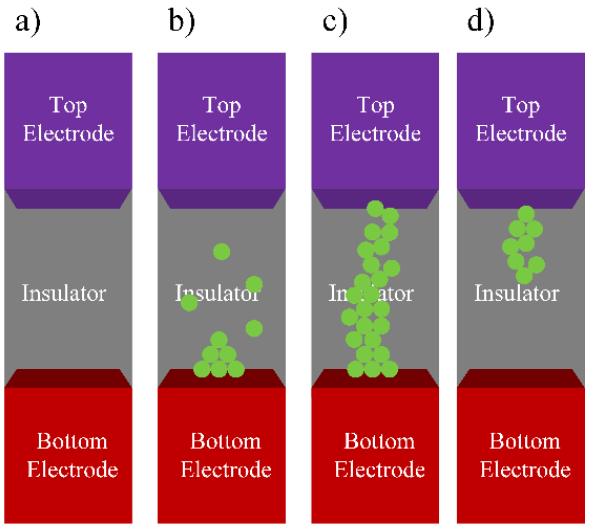


Fig. 5.2. The schematic of resistive switching based on the filamentary conduction model. (a) a native insulator (HRS), (b) creation of CFs via electroforming, (c) CFs in ON state (LRS), and (d) CFs rupture in OFF state (LRS to HRS) [272].

Memristive devices commonly modelled by two resistive switching mechanisms, the valence change memory (VCM) and electrochemical metallisation memory (ECM). VCM is based on oxygen ions migration (anions) effects and subsequent valence change of the metals which progressively modifies the stoichiometry of the metal oxides and results in CF formation by the localised concentration of defects [272]. For instance, memristors based on materials such as HfO_x, TaO_x, TiO_x, and other transition metal oxides in combination with TiN, TaN, Ti, Ta, and Pt can operate in VCM. As abovementioned, the resistance of these devices can vary under appropriate voltages from a high resistance state (HRS) or OFF state to a low resistance state (LRS) or ON state. Thus, these transitions from OFF (ON) to ON (OFF) are also called SET and RESET in the conventional terminology, respectively. Fig. 5.3 illustrates the SET and RESET processes of the VCM switching mechanism. In this figure, the grey spheres represent an inert electrode with a high work function (e.g., Pt), yellow and purple spheres represent the cations of the binary metal oxide in their standard state and reduced state, respectively, and green spheres represent the oxygen vacancies (V_O). In the HRS (Fig. 5.3 (a)), the oxygen vacancies (V_O) in the region near the inert electrode is low. Thus, the electrostatic barrier at the interface does not allow an easy current injection through the active insulating layer. Therefore, the V_O concentration has a donor-like

behaviour and determines the local conductivity. When a negative bias voltage is applied to the inert electrode, the V_O drift toward it (Fig. 5.3 (b)) and increases the V_O concentration next to the electrode. This phenomenon leads to lowering the electrostatic barrier and consequently reduces the thickness of the interface, which allows the charge to inject easily into the insulating layer. This high local conductivity (LRS) close to the electrode enables a high charge transport through the filamentary region (Fig. 5.3 (c)). To rupture the formed CF, applying a positive bias to the electrode is required to move the V_O away from the interface (Fig. 5.3 (d)) which results in restoring the electrostatic barrier and dissolving the CF partially (Fig. 5.3 (a)) [273].

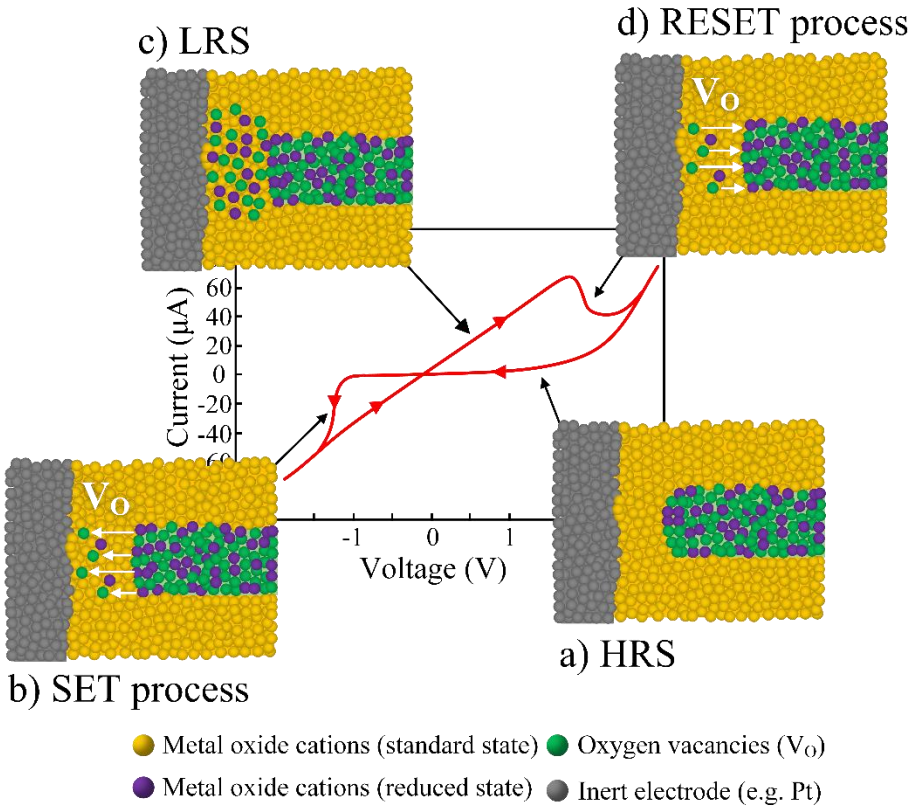


Fig. 5.3. The schematic of the SET and RESET processes of the VCM switching mechanism [274].

On the other hand, ECM relies on the metal ions (cations) movement from the active electrode (often Ag or Cu) into the active insulating layer. This occurs through the oxidative interfacial dissolution of an active metal electrode and subsequent cation migration across the active insulating layer, which results in shortening the two electrodes [275]. This type of memristors are typically using an active electrode (e.g., Ag, Cu, and Co) along with an inert

electrode (e.g., TaN, W, and Pt) and GeSe, GeS, Ag_xS or even SiO_2 as an insulating layer. The physical and electrochemical processes occurring in resistive switching based on ECM and their corresponding I-V characteristics are shown in Fig. 5.4. In order to operate the device at low-resistive state, a positive voltage is applied to a chemically active electrode like Ag (Fig. 5.4(a)). This makes the electrode to be oxidised, and Ag cations are injected into the insulating layer and form a CF (Fig. 5.4(b)). These cations then migrate to the cathode, where they are reduced to metallic Ag. This process continues an Ag CF grows toward the anode (Fig. 5.4(c)) and eventually connect two electrodes electrically (Fig. 5.4(d)). To change the state of the device to high resistive state, a negative voltage is applied to the Ag electrode, which dissolves the CF (Fig. 5.4(e)) [273].

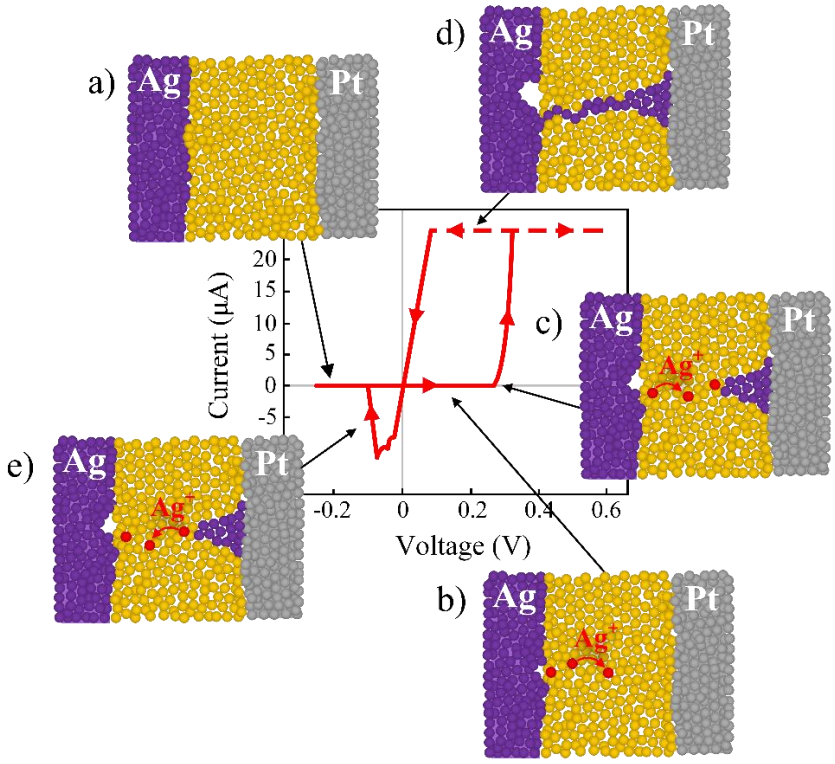


Fig. 5.4. The schematic of the SET and RESET processes of the ECM switching mechanism [275].

Moreover, anionic and cationic resistive switches are generally working based on two different switching modes; unipolar (nonpolar) and bipolar. Therefore, the devices in which the SET and RESET only depends on the magnitude of applied voltage are called unipolar or nonpolar (Fig. 5.5(a)), while in the bipolar memristors, the SET and RESET occur solely

based on the polarity of the applied voltage (Fig. 5.5(b)). Fig 5.5 shows the schematics of the I-V curve of unipolar and bipolar memristors.

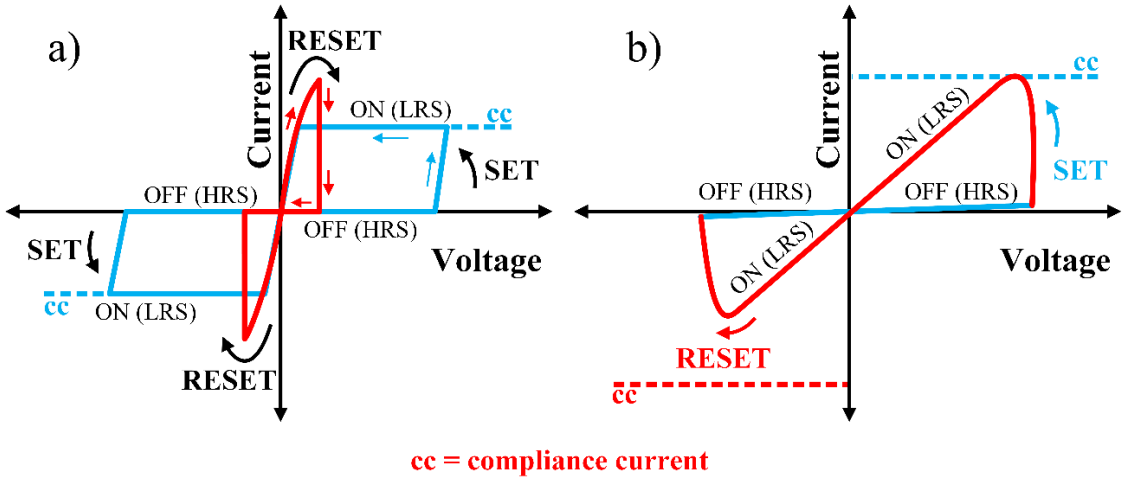


Fig. 5.5. The schematics of I-V curve switching characteristics of memristive devices; (a) unipolar mode and (b) bipolar mode.

5.2 Memristive devices based on TaO_x

Memristive switches based on Ta/TaO_x structures have been reported to exhibit superior performance in comparison to other structures in terms of volatility [276], low voltage [277] and switching times [278]. They have also been investigated to be utilised in resistive random-access memory (ReRAM) applications, and in recent years, in a neuromorphic computing system as neural synapses [279][280]. However, they are usually fabricated using expensive and sophisticated techniques such as multi-step RF sputtering and aggressive chemicals.

In this chapter, the memristive behaviour of $Ta/TaO_x/Pt$ switches is reported. The tantalum oxide films were fabricated using anodisation. It is shown that the performance of the reported switches is comparable or indeed better than most of the previously reported memristors with similar structure ($Ta/TaO_x/Pt$).

In terms of device physics, although the charge transport in tantalum oxide is not fully understood yet, some common understanding can be summarised in three main points. First, the charge transport in the ON state is dominated by an electroformed channel or filament within the tantalum oxide layer. Therefore, the larger the filament radius and the smaller the

oxide thickness are, the lower the ON resistance and the lower the forming voltage become [281]. Second, the ratio of Ta:O within and around the active channel demonstrates a notable change from the original ratio. The stoichiometry of Ta_2O_5 can be changed to a lower oxidation state at the centre, and its oxidation state increases moving away from the centre of the filament [281]. Third, the crystal structure of the material within and around the active channel plays an important role. The initial amorphous structure is changed to a nanocrystalline, which shows local heating [282]. Hence, fabrication parameters can play a major role in the performance of the devices since the material stoichiometry and device behaviour can greatly be affected by the fabrication process and environmental conditions.

5.3 Experimental procedure

The devices were fabricated on 2 × 1.5 cm^2, quartz-coated glass substrates (Ossila, UK). Firstly, the substrates were rinsed with deionised (DI) water, dried with pure N_2 and sonicated for 30 min in acetone, methanol and isopropyl alcohol (IPA). Then, the samples were dried with pure N_2. Any residual organic contaminants were removed using a UV/Ozone cleaner for 30 min. Ta strips with 100 nm thickness were initially deposited as the bottom electrodes using a shadow mask onto the cleaned substrates by RF magnetron sputtering with a 2-inch Ta target (Kurt J. Lesker, 99.9% pure) at a power of 70 W in a pure Argon (Ar) atmosphere with a total pressure of 0.5 Pa at room temperature. Next, the anodisation process similar to the reported for the low-voltage TFTs took place. The anodisation continued until the approximate thickness of tantalum oxide films reached 7 nm (V_A = 3 V). Finally, Pt film of 50 nm thickness was deposited as the top electrode through a shadow mask using a 2-inch Pt target (Kurt J. Lesker, 99.9% pure) at a power of 50 W in a pure Ar atmosphere with a total pressure of 0.5 Pa at room temperature. Fig. 5.6 illustrates the schematic structure of the fabricated device arrays. The size of the fabricated memristive switches was 300 × 400 μm^2.

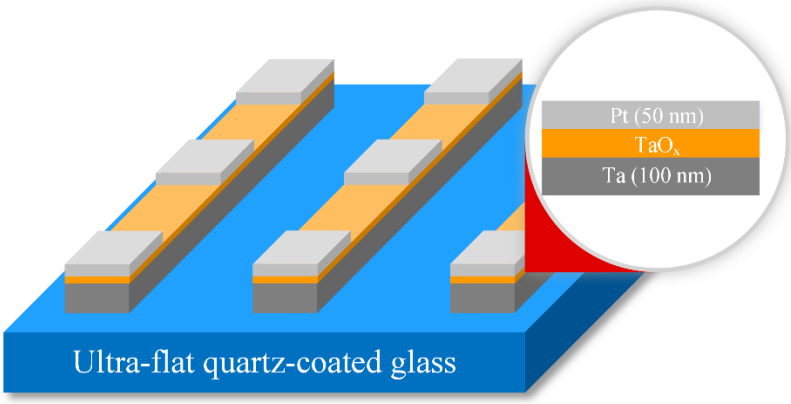


Fig. 5.6. The schematic structure of a single memristor and 3D schematic of the fabricated memristor arrays.

The devices were tested using a Keithley 4200 semiconductor analyser with two ultra-fast pulsing modules 4225RPM and the 4225-PMU card. Also, the devices were tested using a Signatone S-1160 probe station with the S-4210-MMPC-L multi-measurement prober cable kit. Short voltage pulses were sent, and the currents were recorded simultaneously. The Pt electrode was connected to the ground, and pulses were sent to the Ta electrode. In all tests, the PMU card was used to send the pulses, and the current was measured at the ground terminal. Two consecutive pulses were sent, a negative and positive pulse with an intermediate delay of 20 µs, whilst the rise/fall time and width time of each pulse were set to 1 µs. A compliance current was set to 100 µA, and the amplitude of the pulse was successively increased from ± 0.5 V to ± 5 V.

5.4 Results and discussion

Fig. 5.7 demonstrates a representative I-V characteristic with symmetrical memristive behaviour of the fabricated devices, which began from ± 4.5 V in a sweeping range from 4.5 V to −5 V. These measurements were taken from 300 × 400 μm^2 devices but typical memory element sizes are in the range of 1 × 1 μm^2, and thus, the measurements were normalised to $nA/\mu m^2$. During stage 1, the devices were switched OFF completely, and the resistance was calculated by fitting a line to the linear section of the graph. The linear fit (green line) has an R^2 of 0.97 and resistance of ~788 kΩ during the OFF state. The ON state resistance was calculated to be 10 kΩ in a similar method. However, only the top right quadrant was

considered to ensure that only the current state would be measured. The linear fit (blue line) for the ON state has an R^2 of 0.86 due to some minor capacitance effects close to zero voltage.

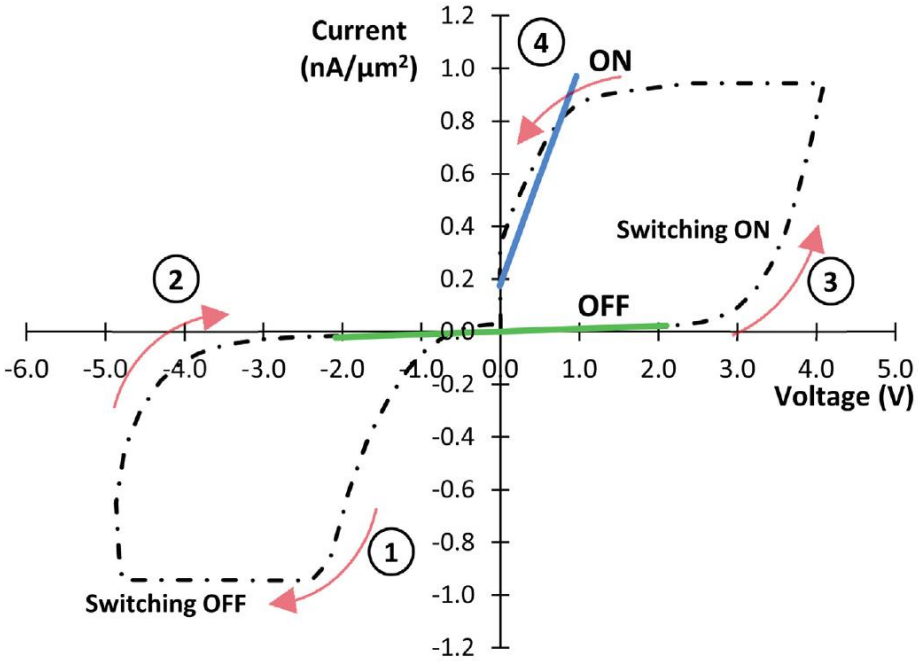


Fig. 5.7. The representative I-V characteristic, showing the memristive behaviour of the fabricated Ta/TaO_x/Pt devices [283].

These values show an almost 80-time change in resistance between the ON and OFF states with a maximum current of 0.83 nA/µm^2 showing promising potential for high-density applications. The performance of the reported devices is comparable or indeed better than most of the previously reported Ta memristors in terms of R_{OFF}/R_{ON} ratio using a 100 µA compliance current. Table 6.1 shows the performance comparison of the fabricated Ta/TaO_x/Pt memristors with their counterpart in the literature.

Reference	R_{ON}	R_{OFF}	R_{OFF}/R_{ON}	Compliance
[284]	25 kΩ	~ 100 kΩ	~ 4	100 µA
[285]	–	–	> 10	5 mA
[286]	~ 300 Ω	80 kΩ	~ 267	300 µA
[287]	20 kΩ	800 kΩ	40	10 µA
[288]	350 Ω	~ 1.4 kΩ	4	–
This work	10 kΩ	~ 800 kΩ	80	100 µA

Table 5.1. Performance comparison of the fabricated Ta/TaO_x/Pt memristors with their counterparts in the literature.

5.5 Conclusions

Low-cost, solution-based TaO_x-based memristive devices which were formed and operated at voltages ≤ ±5 V have been successfully realised. The devices show resistances of 788 kΩ and 10 kΩ during the OFF and ON states, respectively. The devices have an almost 80-time change in resistance with 0.83 nA/μm^2, without the need for expensive Ta_2O_5 procedures. Although further work is required to complete the device characterisation, including measurements of uniformity, retention, and endurance, this work illustrates the high potential of anodisation as a low-cost, environmentally friendly manufacturing technique for high-performance memristors with the possibility of being compatible with CMOS and other VLSI fabrication technologies. Additionally, further investigation is required to use the fabricated memristors in real-world applications such uniformity in large-area deposition, effect of temperature on their operation, use of different substrates and increasing their efficiency.

Chapter 6: Conclusions and Future work

6.1 Conclusions

As discussed, realising low-voltage transistors operating at or below 1 V is a challenging task as it needs several steps of optimisation and careful consideration. One method to achieve this goal is to increase the gate dielectric capacitance. However, increasing the gate dielectric capacitance by either using a high-κ material, thinning the dielectric thickness, or doing both methods simultaneously is a double-edged sword and can lead to exacerbating other key parameters of TFTs. This work has focused on finding and tailoring a high-κ dielectric material to realise low-voltage operation without sacrificing other key parameters of different types of TFTs.

Tantalum pentoxide (Ta_2O_5) is a high-κ oxide dielectric that can provide a large gate capacitance without a significantly large gate leakage current. Ta_2O_5 is employed in a variety of devices, namely, dynamic random-access memory (DRAM), metal-insulator-metal (MIM) capacitors, memory resistors and now in organic and inorganic low-voltage TFTs.

To develop low-cost devices, it is essential to process and deposit materials with inexpensive equipment. Electrochemical oxidation (anodisation) is a very cheap, effective and time-saving method to form a pinhole-free, uniform and smooth metal oxide dielectric, herein Ta_2O_5, with no need for high vacuum expensive equipment. Moreover, anodisation is a self-healing self-limiting process that can deliver metal oxide dielectrics with precise thickness and high reproducibility in ambient conditions. In this light, anodisation has been chosen to oxidise Ta, and the resultant Ta_2O_5 was employed as a gate dielectric in the fabrication of low threshold voltage TFTs.

Furthermore, it is shown that using OTS SAM surface modification not only smoothens the dielectric surface, which leads to lower interfacial traps densities at the

dielectric/semiconductor interface, which ultimately improve field-effect mobility but also acts as an extra dielectric layer which reduces the gate leakage current. In this work, the effect of OTS SAM modification of Ta_2O_5 has been investigated, and it is shown that OTS-treated Ta_2O_5 can improve the dielectric properties of tantalum pentoxide and enhance the performance of both organic and inorganic TFTs. The optimum OTS-treated anodic Ta_2O_5 is reported to be approximately 680 nF/cm^2 (V_A = 3 V) with a maximum standard deviation of 20 nF/cm^2 for 1 V DPPDTT-PMMA OTFTs and 433 nF/cm^2 (V_A = 10 V) with a maximum standard deviation of 10 nF/cm^2 at 1 kHz for 1 V a-IGZO TFTs.

Organic electronic devices have received much attention due to their potential applications in flexible, low-cost, large-area electronics. However, they typically suffer from relatively high operating voltages (≥ 3 V) which has a preemptive effect on their use where the low-voltage operation is required (e.g., wearable and portable devices). This work has addressed this problem and presents a viable solution to pave the way towards low-power organic devices which are essential components of portable and wearable electronics. Several non-trivial steps of optimisation were carried out to find a proper balance between key parameters of OTFTs. As discussed, the DPPDTT-PMMA blends can have a synergistic effect on the operation of the organic TFTs due to the use of two organic components together. Although the understanding of the exact effect of the DPPDTT-PMMA blend is beyond the scope of this work and was not studied in detail, the vertical phase separation of this polymer system not only potentially helps to reduce the gate leakage current but also smoothens the dielectric/semiconductor interface which is beneficial for the performance of OTFTs. Moreover, thanks to the dielectric optimisation processes and use of the blend OSC, the proposed p-channel DPPDTT-PMMA TFTs operate at −1 V, display threshold voltages around −0.55 V, exhibit low subthreshold slopes 120 mV/dec, show negligible hysteresis and possess average saturation mobilities in excess of 0.2 cm^2 V^{-1} s^{-1} at −1 V.

Amorphous indium-gallium-zinc-oxide (a-IGZO) semiconductor owing to its excellent electrical properties such as high field-effect mobility, uniformity and low-temperature processing, has drawn much attention to end the duality between high-temperature processing and high performance of oxide TFTs. a-IGZO TFTs have shown the true potential to be used in a variety of applications such as displays, sensors and transparent electronics. Besides, they appear to be essential for the applications of portable, standalone sensors or battery-powered devices that have to be as power-efficient as possible and are able to operate at or below 1 V. This work has addressed this necessity and presents high-performance, low-voltage, a-IGZO TFTs that operate at 1 V. This goal was achieved by specifically tailoring Ta_2O_5 dielectric for a-IGZO TFTs without significant deterioration of their other key parameters. The proposed n-channel a-IGZO TFTs display relatively high field-effect mobilities (2.3 $cm^2 V^{-1} s^{-1}$), threshold voltages around 0.4 V, subthreshold swings below 90 mV/dec, and high current on/off ratios well in excess of 10^5.

Furthermore, it has been shown that oxygen vacancies in tantalum oxides can be increased, which leads to significant I-V hysteresis and memory behaviour. The properties of anodised Ta_2O_5 memory resistors have been investigated with the help of Prof. Julius Georgiou's research group at the University of Cyprus (ECE). Low-cost, solution-based TaO_x-based memristive devices which can be formed and operated at voltages ≤ ±5 V have been successfully realised. The devices show resistances of 788 kΩ and 10 kΩ during the OFF and ON states, respectively. The devices have an almost 80-time change in resistance with 0.83 $nA/\mu m^2$, without the need for expensive Ta_2O_5 procedures. These results show that the developed Ta_2O_5 films have a high potential to be used in a variety of active devices.

6.2 Future work

Although this research aimed to improve on the technology of low voltage devices and successfully achieved that, the research and development of these devices are not limited to

this study and have much potential to be improved and followed by future work in three time frames, namely, short, medium and long term. In the short term, as shown throughout this study, in terms of dielectric material, tantalum pentoxide as high-κ material shown to still have a great potential to be used in the electronic industry, and its application is not limited to TFTs. For example, Ta_2O_5 is also used in MIM and MIS capacitors, high-speed diodes and memory resistors (memristors). Interestingly most of these abovementioned devices have the same device structure—Ta_2O_5 layer sandwiched between two metal thin films or a metal and a semiconductor. In this regard, it was planned to demonstrate more devices with Ta_2O_5 as an insulating material, such as Ta_2O_5-based Schottky diodes, but unfortunately, it was cut short by the Covid-19 pandemic. Anodic Ta_2O_5 dielectric can also be used to realise low-voltage high-speed MIM diodes, which are required for rectenna and IR detector applications [289]. These diodes work based on charge transport domination by Fowler-Nordheim tunnelling (FNT) in conjunction with the use of asymmetric work function metal electrodes, which yield asymmetric, polarity dependent electron tunnelling barriers [43][290]. Realising these high-speed diodes is a prospective work following this project.

Nonetheless, during the research on Ta_2O_5 dielectric for the application in TFTs, it has been found that the Ta_2O_5 film grown by anodisation is able to be tailored for the memristive devices, which discussed in chapter 5 in details. It is noteworthy that using the same dielectric material for different applications is not trivial as the chemical structure, stoichiometry, oxygen vacancies and thickness of the dielectric play a crucial role to draw the fundamental material limitation and impede straightforward use of that material. Nonetheless, the prospective future work for these devices includes but is not limited to realising low-cost memristive devices and arrays for neuromorphic computing.

Recently, it has been found that thin layers of Ta_2O_5 show n-type semiconducting behaviour [291] if Ta_2O_5 thickness is around a few nanometres ($\leq$ 10.5 nm) [175]. As shown in [292],

using Ta_2O_5 as a semiconductor induced by heavy doping of nitrogen can be beneficial to future technology development of photocatalysis for solar energy conversion, optoelectronics, and sensors. Likewise, the ultrathin anodic Ta_2O_5 dielectrics might be able to serve the same purposes but probably at a lower cost. Nonetheless, this was beyond the scope of this research, and further investigation is required to confirm their suitability for such applications. Therefore, a potential future work can be realising phototransistors using this technology. In terms of device figure of merit, future work can also include the study of stability and reliability of the fabricated devices in flexible and stretchable circuits.

In the medium term, this technology can be improved and optimised for use in simple, flexible integrated circuits and substitute off-the-shelf rigid components for realising natively flexible circuits. Although it is difficult to predict the long term advances in this technology, these devices can be improved in the way that can substitute Si in commercial devices and circuits where ultra-low power consumption and flexibility are required.

References

[1] K. Kim, K. Choi, and H. Lee, “a-InGaZnO Thin-Film Transistor-Based Operational Amplifier for an Adaptive DC–DC Converter in Display Driving Systems,” *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1189–1194, Apr. 2015, doi: 10.1109/TED.2015.2402684.

[2] J. Wu *et al.*, “A Low-Power Ring Oscillator Using Pull-Up Control Scheme Integrated by Metal–Oxide TFTs,” *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4946–4951, Dec. 2017, doi: 10.1109/TED.2017.2759226.

[3] N. D. Arora, *MOSFET models for VLSI circuit simulation: theory and practice*. Springer Science \& Business Media, 2012.

[4] Y. Kuo, “Thin Film Transistor Technology--Past, Present, and Future,” *Interface Mag.*, vol. 22, no. 1, pp. 55–61, Jan. 2013, doi: 10.1149/2.f06131if.

[5] B. Wang, W. Huang, L. Chi, M. Al-Hashimi, T. J. Marks, and A. Facchetti, “High-k Gate Dielectrics for Emerging Flexible and Stretchable Electronics,” *Chem. Rev.*, vol. 118, no. 11, pp. 5690–5754, Jun. 2018, doi: 10.1021/acs.chemrev.8b00045.

[6] A. F. Paterson and T. D. Anthopoulos, “Enabling thin-film transistor technologies and the device metrics that matter,” *Nat. Commun.*, vol. 9, no. 1, p. 5264, 2018, doi: 10.1038/s41467-018-07424-2.

[7] G. Nisato, D. Lupo, and S. Ganz, *Organic and printed electronics: fundamentals and applications*. CRC Press, 2016.

[8] R. A. Street, “Thin-film transistors,” *Adv. Mater.*, vol. 21, no. 20, pp. 2007–2022, 2009.

[9] J.-Y. Kwon, D.-J. Lee, and K.-B. Kim, “Review paper: Transparent amorphous oxide semiconductor thin film transistor,” *Electron. Mater. Lett.*, vol. 7, no. 1, pp. 1–11, 2011, doi: 10.1007/s13391-011-0301-x.

[10] M. Benwadih, R. Coppard, K. Bonrad, A. Klyszcz, and D. Vuillaume, “High Mobility Flexible Amorphous IGZO Thin-Film Transistors with a Low Thermal Budget Ultra-Violet Pulsed Light Process,” *ACS Appl. Mater. Interfaces*, vol. 8, no. 50, pp. 34513–34519, Dec. 2016, doi: 10.1021/acsami.6b09990.

[11] M. Sun, R. Xu, L. Xie, Y. Wei, and W. Huang, “Toward Eco-friendly Green Organic Semiconductors: Recent Advances in Spiro[fluorene-9,9′-xanthene] (SFX)-Based Optoelectronic Materials and Devices,” *Chinese J. Chem.*, vol. 33, no. 8, pp. 815–827, 2015, doi: 10.1002/cjoc.201500261.

[12] B. Nketia-Yawson and Y.-Y. Noh, “Organic thin film transistor with conjugated polymers for highly sensitive gas sensors,” *Macromol. Res.*, vol. 25, no. 6, pp. 489–495, 2017, doi: 10.1007/s13233-017-5108-7.

[13] C. D. Sheraw *et al.*, “Organic thin-film transistor-driven polymer-dispersed liquid crystal displays on flexible polymeric substrates,” *Appl. Phys. Lett.*, vol. 80, no. 6, pp. 1088–1090, 2002, doi: 10.1063/1.1448659.

[14] E. Cantatore *et al.*, “A 13.56-MHz RFID System Based on Organic Transponders,”

IEEE J. Solid-State Circuits, vol. 42, no. 1, pp. 84–92, Jan. 2007, doi: 10.1109/JSSC.2006.886556.

[15] Ghaffarzadeh Khasha and D. Matthew, "Flexible Hybrid Electronics 2020-2030: Applications, Challenges, Innovations and Forecasts," 2020. [Online]. Available: https://www.idtechex.com/en/research-report/flexible-hybrid-electronics-2020-2030-applications-challenges-innovations-and-forecasts/732.

[16] I. Kymissis, *Organic field effect transistors: theory, fabrication and characterization*. Springer Science & Business Media, 2008.

[17] G. Horowitz, "The organic transistor: state-of-the-art and outlook," *Eur. Phys. Journal-Applied Phys.*, vol. 53, no. 3, 2011.

[18] C. Wöll, *Physical and Chemical Aspects of Organic Electronics: From Fundamentals to Functioning Devices*. John Wiley & Sons, 2009.

[19] J. Chen, W. Cranton, and M. Fihn, *Handbook of visual display technology*. Springer, 2016.

[20] Y. Setsuhara, T. Kamiya, and S. Yamaura, *Novel Structured Metallic and Inorganic Materials*. Springer, 2019.

[21] S. Higashi *et al.*, "High-quality SiO2/Si interface formation and its application to fabrication of low-temperature-processed polycrystalline Si thin-film transistor," *Jpn. J. Appl. Phys.*, vol. 41, no. 6R, p. 3646, 2002.

[22] R. L. Hoffman, B. J. Norris, and J. F. Wager, "ZnO-based transparent thin-film transistors," *Appl. Phys. Lett.*, vol. 82, no. 5, pp. 733–735, Jan. 2003, doi: 10.1063/1.1542677.

[23] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor," *Science (80-.).*, vol. 300, no. 5623, pp. 1269–1272, 2003, doi: 10.1126/science.1083212.

[24] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.

[25] V. K. Khanna, "Short-Channel Effects in MOSFETs," in *Integrated Nanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies*, New Delhi: Springer India, 2016, pp. 73–93.

[26] H. Wong, *Nano-CMOS gate dielectric engineering*. Crc Press, 2011.

[27] J. Robertson and R. M. Wallace, "High-K materials and metal gates for CMOS applications," *Mater. Sci. Eng. R Reports*, vol. 88, pp. 1–41, 2015.

[28] Y. Liang *et al.*, "A review of rechargeable batteries for portable electronic devices," *InfoMat*, vol. 1, no. 1, pp. 6–32, 2019.

[29] G. E. Moore, "Cramming More Components Onto Integrated Circuits," *Proc. IEEE*, vol. 86, no. 1, pp. 82–85, Jan. 1998, doi: 10.1109/JPROC.1998.658762.

[30] Y. Su *et al.*, "Low-Voltage Organic Field-Effect Transistors (OFETs) with Solution-

Processed Metal-Oxide as Gate Dielectric," *ACS Appl. Mater. Interfaces*, vol. 3, no. 12, pp. 4662–4667, Dec. 2011, doi: 10.1021/am201078v.

[31] F. Yang *et al.*, "Low-Voltage Organic Single-Crystal Field-Effect Transistor with Steep Subthreshold Slope," *ACS Appl. Mater. Interfaces*, vol. 10, no. 31, pp. 25871–25877, Aug. 2018, doi: 10.1021/acsami.7b16658.

[32] M. Kunii, H. Iino, and J. Hanna, "Solution-Processed, Low-Voltage Polycrystalline Organic Field-Effect Transistor Fabricated Using Highly Ordered Liquid Crystal With Low- k Gate Dielectric," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 486–488, 2016, doi: 10.1109/LED.2016.2529678.

[33] P. K. Weimer, "The TFT A New Thin-Film Transistor," *Proc. IRE*, vol. 50, no. 6, pp. 1462–1469, Jun. 1962, doi: 10.1109/JRPROC.1962.288190.

[34] C. D. Dimitrakopoulos, I. Kymissis, S. Purushothaman, D. A. Neumayer, P. R. Duncombe, and R. B. Laibowitz, "Low-Voltage, High-Mobility Pentacene Transistors with Solution-Processed High Dielectric Constant Insulators," *Adv. Mater.*, vol. 11, no. 16, pp. 1372–1375, Nov. 1999, doi: https://doi.org/10.1002/(SICI)1521-4095(199911)11:16<1372::AID-ADMA1372>3.0.CO;2-V.

[35] C. Bartic, H. Jansen, A. Campitelli, and S. Borghs, "Ta2O5 as gate dielectric material for low-voltage organic thin-film transistors," *Org. Electron.*, vol. 3, no. 2, pp. 65–72, 2002, doi: https://doi.org/10.1016/S1566-1199(02)00034-4.

[36] H. Sakai, Y. Furukawa, E. Fujiwara, and H. Tada, "Low-voltage Organic Field-effect Transistors with a Gate Insulator of Ta2O5 Formed by Sputtering," *Chem. Lett.*, vol. 33, no. 9, pp. 1172–1173, 2004, doi: 10.1246/cl.2004.1172.

[37] K. Ueno, S. Abe, R. Onoki, and K. Saiki, "Anodization of electrolytically polished Ta surfaces for enhancement of carrier injection into organic field-effect transistors," *J. Appl. Phys.*, vol. 98, no. 11, p. 114503, Dec. 2005, doi: 10.1063/1.2138807.

[38] J. Zhou and F. Zhang, "Low voltage n-type OFET based on double insulators," *Optoelectron. Lett.*, vol. 4, no. 5, pp. 324–327, 2008, doi: 10.1007/s11801-008-8029-z.

[39] M. Shur, "Physics of Semiconductor Devices, Prentice Hall," *Inc., Englewood Cliffs, New Jersey*, p. 680, 1990.

[40] A. P. P. Correia, P. M. C. Barquinha, and J. C. da P. Goes, "Thin-Film Transistors," in *A Second-Order $ΣΔ$ ADC Using Sputtered IGZO TFTs*, Cham: Springer International Publishing, 2016, pp. 5–15.

[41] H. Nakaie *et al.*, "Reduction of Dislocation Densities of Ge Layers Grown on Si Substrates by Using Microwave Plasma Heating and Fabrication of High Hole Mobility MOSFETs on Ge Layers," *J. Mater. Sci. Chem. Eng.*, vol. 5, no. 1, pp. 42–47, 2017.

[42] N. Mohammadian and L. A. Majewski, "High Capacitance Dielectrics for Low Voltage Operated OFETs," in *Integrated Circuits/Microchips [Working Title]*, IntechOpen, 2020.

[43] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. John wiley \& sons, 2006.

[44] B. G. Horowitz, “Organic Field-Effect Transistors,” no. 5, pp. 365–377, 1998.

[45] F. Liao, C. Chen, and V. Subramanian, “Organic TFTs as gas sensors for electronic nose applications,” *Sensors Actuators B Chem.*, vol. 107, no. 2, pp. 849–855, 2005.

[46] E. Fortunato, P. Barquinha, and R. Martins, “Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances,” *Adv. Mater.*, vol. 24, no. 22, pp. 2945–2986, 2012, doi: 10.1002/adma.201103228.

[47] R. Street, *Technology and applications of amorphous silicon*, vol. 37. Springer Science \& Business Media, 1999.

[48] D. Elkington, N. Cooling, W. Belcher, P. C. Dastoor, and X. Zhou, “Organic thin-film transistor (OTFT)-based sensors,” *Electronics*, vol. 3, no. 2, pp. 234–254, 2014.

[49] A. Sato *et al.*, “Amorphous In–Ga–Zn–O coplanar homojunction thin-film transistor,” *Appl. Phys. Lett.*, vol. 94, no. 13, p. 133502, 2009, doi: 10.1063/1.3112566.

[50] C. Hu, *Modern semiconductor devices for integrated circuits*, vol. 2. Prentice Hall Upper Saddle River, New Jersey, 2010.

[51] T. Ytterdal, Y. Cheng, and T. A. Fjeldly, *Device modeling for analog and RF CMOS circuit design*. John Wiley \& Sons, 2003.

[52] W. J. Park *et al.*, “Investigation on doping dependency of solution-processed Ga-doped ZnO thin film transistor,” *Appl. Phys. Lett.*, vol. 93, no. 8, p. 83508, 2008.

[53] A. Rolland, J. Richard, J. P. Kleider, and D. Mencaraglia, “Electrical properties of amorphous silicon transistors and MIS-devices: comparative study of top nitride and bottom nitride configurations,” *J. Electrochem. Soc.*, vol. 140, no. 12, p. 3679, 1993.

[54] B. Blülle, R. Häusermann, and B. Batlogg, “Approaching the trap-free limit in organic single-crystal field-effect transistors,” *Phys. Rev. Appl.*, vol. 1, no. 3, p. 34006, 2014.

[55] E. S. Yang and others, *Microelectronic devices*. McGraw-Hill New York, 1988.

[56] D. K. Schroder, *Semiconductor material and device characterization*. John Wiley \& Sons, 2015.

[57] C. Zhou *et al.*, “Low voltage and high ON/OFF ratio field-effect transistors based on CVD MoS 2 and ultra high-k gate dielectric PZT,” *Nanoscale*, vol. 7, no. 19, pp. 8695–8700, 2015.

[58] R. P. Ortiz, A. Facchetti, and T. J. Marks, “High-k Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors,” *Chem. Rev.*, vol. 110, no. 1, pp. 205–239, Jan. 2010, doi: 10.1021/cr9001275.

[59] T. Yokota *et al.*, “Low-voltage organic transistor with subfemtoliter inkjet source–drain contacts,” *MRS Commun.*, vol. 1, no. 1, pp. 3–6, 2011, doi: DOI: 10.1557/mrc.2011.4.

[60] L. Feng *et al.*, “Unencapsulated Air-stable Organic Field Effect Transistor by All Solution Processes for Low Power Vapor Sensing,” *Sci. Rep.*, vol. 6, no. 1, p. 20671, 2016, doi: 10.1038/srep20671.

[61] H. Ma *et al.*, “Low-voltage organic thin-film transistors with π-σ-phosphonic acid molecular dielectric monolayers,” *Appl. Phys. Lett.*, vol. 92, no. 11, p. 113303, 2008,

doi: 10.1063/1.2857502.

[62] L. Feng, W. Tang, X. Xu, Q. Cui, and X. Guo, “Ultralow-Voltage Solution-Processed Organic Transistors With Small Gate Dielectric Capacitance,” *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 129–131, Jan. 2013, doi: 10.1109/LED.2012.2227236.

[63] J. S. Lee, S. Chang, S.-M. Koo, and S. Y. Lee, “High-Performance a-IGZO TFT With ZrO2 Gate Dielectric Fabricated at Room Temperature,” *IEEE electron device Lett.*, vol. 31, no. 3, pp. 225–227, 2010.

[64] S. Pearton, *GaN and ZnO-based materials and devices*, vol. 156. Springer Science \& Business Media, 2012.

[65] P. Barquinha, R. Martins, L. Pereira, and E. Fortunato, *Transparent oxide electronics: from materials to devices*. John Wiley \& Sons, 2012.

[66] L. Basiricò, P. Cosseddu, B. Fraboni, and A. Bonfiglio, “Inkjet printing of transparent, flexible, organic transistors,” *Thin Solid Films*, vol. 520, no. 4, pp. 1291–1294, 2011.

[67] J.-H. Lee, D. N. Liu, and S.-T. Wu, *Introduction to flat panel displays*, vol. 20. John Wiley \& Sons, 2008.

[68] M. Mitani *et al.*, “Ultrahigh-performance polycrystalline silicon thin-film transistors on excimer-laser-processed pseudo-single-crystal films,” *Jpn. J. Appl. Phys.*, vol. 47, no. 12, pp. 8707–8713, 2008, doi: 10.1143/JJAP.47.8707.

[69] B. H. Lee *et al.*, “Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8/spl Aring/-12/spl Aring/),” in *International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No. 00CH37138)*, 2000, pp. 39–42.

[70] T.-K. Chang, C.-W. Lin, and S. Chang, “39-3: Invited Paper: LTPO TFT Technology for AMOLEDs†,” *SID Symp. Dig. Tech. Pap.*, vol. 50, no. 1, pp. 545–548, Jun. 2019, doi: https://doi.org/10.1002/sdtp.12978.

[71] P. Pattanasattayavong, S. Thomas, G. Adamopoulos, M. A. McLachlan, and T. D. Anthopoulos, “p-channel thin-film transistors based on spray-coated Cu2O films,” *Appl. Phys. Lett.*, vol. 102, no. 16, p. 163505, 2013, doi: 10.1063/1.4803085.

[72] E. Fortunato and R. Martins, “Where science fiction meets reality? With oxide semiconductors!,” *Phys. status solidi (RRL)--Rapid Res. Lett.*, vol. 5, no. 9, pp. 336–339, 2011.

[73] S. Baranovski, *Charge transport in disordered solids with applications in electronics*, vol. 17. John Wiley \& Sons, 2006.

[74] I. I. Fishchuk *et al.*, “Interplay between hopping and band transport in high-mobility disordered semiconductors at large carrier concentrations: The case of the amorphous oxide InGaZnO,” *Phys. Rev. B*, vol. 93, no. 19, p. 195204, 2016.

[75] A. Takagi *et al.*, “Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO4,” *Thin Solid Films*, vol. 486, no. 1–2, pp. 38–41, 2005.

[76] H. Bässler, “Charge transport in disordered organic photoconductors a Monte Carlo simulation study,” *Phys. status solidi*, vol. 175, no. 1, pp. 15–56, 1993.

[77] T. Kamiya, K. Nomura, and H. Hosono, “Electronic Structures Above Mobility Edges

in Crystalline and Amorphous In-Ga-Zn-O: Percolation Conduction Examined by Analytical Model," *J. Disp. Technol.*, vol. 5, no. 12, pp. 462–467, Dec. 2009, doi: 10.1109/JDT.2009.2022064.

[78] T. Kamiya, K. Nomura, and H. Hosono, "Origin of definite Hall voltage and positive slope in mobility-donor density relation in disordered oxide semiconductors," *Appl. Phys. Lett.*, vol. 96, no. 12, p. 122103, 2010, doi: 10.1063/1.3364131.

[79] K. Nomura, T. Kamiya, H. Ohta, K. Ueda, M. Hirano, and H. Hosono, "Carrier transport in transparent oxide semiconductor with intrinsic structural randomness probed using single-crystalline InGaO3(ZnO)5 films," *Appl. Phys. Lett.*, vol. 85, no. 11, pp. 1993–1995, 2004, doi: 10.1063/1.1788897.

[80] A. V Nenashev, J. O. Oelerich, S. H. M. Greiner, A. V Dvurechenskii, F. Gebhard, and S. D. Baranovskii, "Percolation description of charge transport in amorphous oxide semiconductors," *Phys. Rev. B*, vol. 100, no. 12, p. 125202, Sep. 2019, doi: 10.1103/PhysRevB.100.125202.

[81] W. C. Germs *et al.*, "Charge transport in amorphous InGaZnO thin-film transistors," *Phys. Rev. B*, vol. 86, no. 15, p. 155319, Oct. 2012, doi: 10.1103/PhysRevB.86.155319.

[82] D. Adler, L. P. Flora, and S. D. Senturia, "Electrical conductivity in disordered systems," *Solid State Commun.*, vol. 12, no. 1, pp. 9–12, 1973, doi: https://doi.org/10.1016/0038-1098(73)90333-5.

[83] S. Lee *et al.*, "Extraction of Subgap Density of States in Amorphous InGaZnO Thin-Film Transistors by Using Multifrequency Capacitance–Voltage Characteristics," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 231–233, Mar. 2010, doi: 10.1109/LED.2009.2039634.

[84] J.-H. Park *et al.*, "Self-Consistent Technique for Extracting Density of States in Amorphous {InGaZnO} Thin Film Transistors," *J. Electrochem. Soc.*, vol. 157, no. 3, p. H272, 2010, doi: 10.1149/1.3273203.

[85] J. Noolandi, "Multiple-trapping model of anomalous transit-time dispersion in $a\ensuremath{-}\mathrm{S}\mathrm{e}$," *Phys. Rev. B*, vol. 16, no. 10, pp. 4466–4473, Nov. 1977, doi: 10.1103/PhysRevB.16.4466.

[86] A. V Nenashev, F. Jansson, S. D. Baranovskii, R. Österbacka, A. V Dvurechenskii, and F. Gebhard, "Effect of electric field on diffusion in disordered materials. II. Two- and three-dimensional hopping transport," *Phys. Rev. B*, vol. 81, no. 11, p. 115204, 2010.

[87] O. Semeniuk, G. Juska, J. O. Oelerich, K. Jandieri, S. D. Baranovskii, and A. Reznik, "Transport of electrons in lead oxide studied by {CELIV} technique," *J. Phys. D. Appl. Phys.*, vol. 50, no. 3, p. 35103, Dec. 2016, doi: 10.1088/1361-6463/50/3/035103.

[88] S. Lee *et al.*, "Trap-limited and percolation conduction mechanisms in amorphous oxide semiconductor thin film transistors," *Appl. Phys. Lett.*, vol. 98, no. 20, p. 203508, 2011, doi: 10.1063/1.3589371.

[89] N. F. Mott and E. A. Davis, *Electronic processes in non-crystalline materials*. Oxford university press, 2012.

[90] W. C. Germs, K. Guo, R. A. J. Janssen, and M. Kemerink, “Unusual Thermoelectric Behavior Indicating a Hopping to Bandlike Transport Transition in Pentacene,” *Phys. Rev. Lett.*, vol. 109, no. 1, p. 16601, Jul. 2012, doi: 10.1103/PhysRevLett.109.016601.

[91] S. D. Baranovskii, “Theoretical description of charge transport in disordered organic semiconductors,” *Phys. status solidi*, vol. 251, no. 3, pp. 487–525, 2014, doi: 10.1002/pssb.201350339.

[92] S. D. Baranovskii, H. Cordes, F. Hensel, and G. Leising, “Charge-carrier transport in disordered organic solids,” *Phys. Rev. B*, vol. 62, no. 12, pp. 7934–7938, Sep. 2000, doi: 10.1103/PhysRevB.62.7934.

[93] R. A. Street, *Hydrogenated amorphous silicon*. Cambridge university press, 2005.

[94] S. Kirkpatrick, “Percolation and Conduction,” *Rev. Mod. Phys.*, vol. 45, no. 4, pp. 574–588, Oct. 1973, doi: 10.1103/RevModPhys.45.574.

[95] A. Köhler and H. Bässler, *Electronic processes in organic semiconductors: An introduction*. John Wiley \& Sons, 2015.

[96] A. J. Heeger, “Semiconducting and Metallic Polymers: The Fourth Generation of Polymeric Materials,” *J. Phys. Chem. B*, vol. 105, no. 36, pp. 8475–8491, Sep. 2001, doi: 10.1021/jp011611w.

[97] F. Li, A. Nathan, Y. Wu, and B. S. Ong, *Organic thin film transistor integration: A hybrid approach*. John Wiley \& Sons, 2011.

[98] G. Horowitz, “Organic thin film transistors: From theory to real devices,” *J. Mater. Res.*, vol. 19, no. 7, pp. 1946–1962, 2004, doi: DOI: 10.1557/JMR.2004.0266.

[99] H. Usta and A. Facchetti, “Polymeric and Small-Molecule Semiconductors for Organic Field-Effect Transistors,” in *Large Area and Flexible Electronics*, John Wiley & Sons, Ltd, 2015, pp. 1–100.

[100] J. T. E. Quinn, J. Zhu, X. Li, J. Wang, and Y. Li, “Recent progress in the development of n-type organic semiconductors for organic field effect transistors,” *J. Mater. Chem. C*, vol. 5, no. 34, pp. 8654–8681, 2017, doi: 10.1039/C7TC01680H.

[101] V. Coropceanu, J. Cornil, D. A. da Silva Filho, Y. Olivier, R. Silbey, and J.-L. Brédas, “Charge Transport in Organic Semiconductors,” *Chem. Rev.*, vol. 107, no. 4, pp. 926–952, Apr. 2007, doi: 10.1021/cr050140x.

[102] N. Lu, L. Li, W. Banerjee, P. Sun, N. Gao, and M. Liu, “Charge carrier hopping transport based on Marcus theory and variable-range hopping theory in organic semiconductors,” *J. Appl. Phys.*, vol. 118, no. 4, p. 45701, 2015, doi: 10.1063/1.4927334.

[103] R. Schmechel, “Hopping transport in doped organic semiconductors: A theoretical approach and its application to p-doped zinc-phthalocyanine,” *J. Appl. Phys.*, vol. 93, no. 8, pp. 4653–4660, 2003, doi: 10.1063/1.1560571.

[104] J. H. Schön, C. Kloc, and B. Batlogg, “Universal crossover from band to hopping conduction in molecular organic semiconductors,” *Phys. Rev. Lett.*, vol. 86, no. 17, pp. 3843–3846, 2001, doi: 10.1103/PhysRevLett.86.3843.

[105] N. Lu, L. Li, D. Geng, and M. Liu, “A review for polaron dependent charge transport

in organic semiconductor," *Org. Electron.*, vol. 61, pp. 223–234, 2018, doi: https://doi.org/10.1016/j.orgel.2018.05.053.

[106] H. Alves, A. S. Molinari, H. Xie, and A. F. Morpurgo, "Metallic conduction at organic charge-transfer interfaces," *Nat. Mater.*, vol. 7, no. 7, pp. 574–580, 2008, doi: 10.1038/nmat2205.

[107] Gilles Horowitz, Riadh Hajlaoui, and Philippe Delannoy, "Temperature Dependence of the Field-Effect Mobility of Sexithiophene. Determination of the Density of Traps," *J. Phys. III Fr.*, vol. 5, no. 4, pp. 355–371, 1995, doi: 10.1051/jp3:1995132.

[108] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic thin film transistors for large area electronics," *Adv. Mater.*, vol. 14, no. 2, pp. 99–117, 2002.

[109] J. Smith *et al.*, "Solution-processed organic transistors based on semiconducting blends," *J. Mater. Chem.*, vol. 20, no. 13, pp. 2562–2574, 2010, doi: 10.1039/B921674J.

[110] A. Babel, J. D. Wind, and S. A. Jenekhe, "Ambipolar Charge Transport in Air-Stable Polymer Blend Thin-Film Transistors," *Adv. Funct. Mater.*, vol. 14, no. 9, pp. 891–898, 2004, doi: 10.1002/adfm.200305180.

[111] L. Qiu, J. A. Lim, X. Wang, W. H. Lee, M. Hwang, and K. Cho, "Versatile Use of Vertical-Phase-Separation-Induced Bilayer Structures in Organic Thin-Film Transistors," *Adv. Mater.*, vol. 20, no. 6, pp. 1141–1145, 2008, doi: 10.1002/adma.200702505.

[112] B. Wang *et al.*, "Fabrication and origin of high-k carbon nanotube/epoxy composites with low dielectric loss through layer-by-layer casting technique," *Carbon N. Y.*, vol. 85, pp. 28–37, 2015, doi: https://doi.org/10.1016/j.carbon.2014.12.062.

[113] R. Ruppin, "Electromagnetic energy density in a dispersive and absorptive material," *Phys. Lett. A*, vol. 299, no. 2, pp. 309–312, 2002, doi: https://doi.org/10.1016/S0375-9601(01)00838-6.

[114] K. Asami, "Characterization of heterogeneous systems by dielectric spectroscopy," *Prog. Polym. Sci.*, vol. 27, no. 8, pp. 1617–1659, 2002, doi: https://doi.org/10.1016/S0079-6700(02)00015-1.

[115] C. J. F. Böttcher and P. Bordewijk, *Theory of electric polarization*, vol. 2. Elsevier Science Limited, 1978.

[116] L. A. Fredin, Z. Li, M. T. Lanagan, M. A. Ratner, and T. J. Marks, "Sustainable high capacitance at high frequencies: metallic aluminum--polypropylene nanocomposites," *ACS Nano*, vol. 7, no. 1, pp. 396–407, 2013.

[117] S. H. Kim *et al.*, "Electrolyte-Gated Transistors for Organic and Printed Electronics," *Adv. Mater.*, vol. 25, no. 13, pp. 1822–1846, 2013, doi: 10.1002/adma.201202790.

[118] J. Yuan, S. Yao, and P. Poulin, "Dielectric constant of polymer composites and the routes to high-k or low-k nanocomposite materials," in *Polymer Nanocomposites*, Springer, 2016, pp. 3–28.

[119] F. Kremer and A. Schönhals, *Broadband dielectric spectroscopy*. Springer Science \& Business Media, 2002.

[120] P. Ben Ishai, M. S. Talary, A. Caduff, E. Levy, and Y. Feldman, “Electrode polarization in dielectric measurements: a review,” *Meas. Sci. Technol.*, vol. 24, no. 10, p. 102001, Aug. 2013, doi: 10.1088/0957-0233/24/10/102001.

[121] A. Liu, H. Zhu, H. Sun, Y. Xu, and Y.-Y. Noh, “Solution Processed Metal Oxide High-κ Dielectrics for Emerging Transistors and Circuits,” *Adv. Mater.*, vol. 30, no. 33, p. 1706364, 2018, doi: 10.1002/adma.201706364.

[122] J. Belasco, S. K. Mohapatra, Y. Zhang, S. Barlow, S. R. Marder, and A. Kahn, “Molecular doping and tuning threshold voltage in 6,13-bis(triisopropylsilylethynyl)pentacene/polymer blend transistors,” *Appl. Phys. Lett.*, vol. 105, no. 6, p. 63301, 2014, doi: 10.1063/1.4892809.

[123] G. Vescio *et al.*, “Inkjet Printed HfO2-Based ReRAMs: First Demonstration and Performance Characterization,” *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 457–460, Apr. 2017, doi: 10.1109/LED.2017.2668599.

[124] M. Xu, L. Xiang, T. Xu, W. Wang, W. Xie, and D. Zhou, “Low-voltage operating flexible ferroelectric organic field-effect transistor nonvolatile memory with a vertical phase separation P(VDF-TrFE-CTFE)/PS dielectric,” *Appl. Phys. Lett.*, vol. 111, no. 18, p. 183302, 2017, doi: 10.1063/1.4993857.

[125] W. Tang *et al.*, “Bias Stress Stability Improvement in Solution-Processed Low-Voltage Organic Field-Effect Transistors Using Relaxor Ferroelectric Polymer Gate Dielectric,” *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 748–751, Jun. 2017, doi: 10.1109/LED.2017.2696987.

[126] G. D. Tabi, B. Nketia-Yawson, S.-H. Kang, C. Yang, and Y.-Y. Noh, “High performance p-type chlorinated-benzothiadiazole-based polymer electrolyte gated organic field-effect transistors,” *Org. Electron.*, vol. 54, pp. 255–260, 2018, doi: https://doi.org/10.1016/j.orgel.2018.01.003.

[127] Q. Zhang, F. Leonardi, R. Pfattner, and M. Mas-Torrent, “A Solid-State Aqueous Electrolyte-Gated Field-Effect Transistor as a Low-Voltage Operation Pressure-Sensitive Platform,” *Adv. Mater. Interfaces*, vol. 6, no. 16, p. 1900719, 2019, doi: 10.1002/admi.201900719.

[128] W.-S. Choi and Y. Kim, “Inkjet-printed ZTO TFT with a combustion-processed aluminum oxide (Al2O3) gate dielectric,” *Mol. Cryst. Liq. Cryst.*, vol. 679, no. 1, pp. 111–118, 2019, doi: 10.1080/15421406.2019.1597554.

[129] J. Yang *et al.*, “High-Performance 1-V ZnO Thin-Film Transistors With Ultrathin, ALD-Processed ZrO2 Gate Dielectric,” *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3382–3386, Aug. 2019, doi: 10.1109/TED.2019.2924135.

[130] M. G. Syamala Rao *et al.*, “Low-temperature sol-gel ZrHfO2-PMMA hybrid dielectric thin-films for metal oxide TFTs,” *J. Non. Cryst. Solids*, vol. 502, pp. 152–158, 2018, doi: https://doi.org/10.1016/j.jnoncrysol.2018.08.014.

[131] G. S. R. Mullapudi, G. A. Velazquez-Nevarez, C. Avila-Avendano, J. A. Torres-Ochoa, M. A. Quevedo-López, and R. Ramírez-Bon, “Low-Temperature Deposition of Inorganic–Organic HfO2–PMMA Hybrid Gate Dielectric Layers for High-Mobility ZnO Thin-Film Transistors,” *ACS Appl. Electron. Mater.*, vol. 1, no. 6, pp. 1003–1011, Jun. 2019, doi: 10.1021/acsaelm.9b00175.

[132] X. Chen, X. Han, and Q.-D. Shen, “PVDF-Based Ferroelectric Polymers in Modern Flexible Electronics,” *Adv. Electron. Mater.*, vol. 3, no. 5, p. 1600460, 2017, doi: 10.1002/aelm.201600460.

[133] E.-Y. Shin, H. J. Cho, S. Jung, C. Yang, and Y.-Y. Noh, “A High-k Fluorinated P(VDF-TrFE)-g-PMMA Gate Dielectric for High-Performance Flexible Field-Effect Transistors,” *Adv. Funct. Mater.*, vol. 28, no. 4, p. 1704780, 2018, doi: 10.1002/adfm.201704780.

[134] G. C. Schmidt *et al.*, “Fully printed flexible audio system on the basis of low-voltage polymeric organic field effect transistors with three layer dielectric,” *J. Polym. Sci. Part B Polym. Phys.*, vol. 53, no. 20, pp. 1409–1415, 2015, doi: 10.1002/polb.23778.

[135] H. Yu *et al.*, “A novel redox-mediated gel polymer electrolyte for high-performance supercapacitor,” *J. Power Sources*, vol. 198, pp. 402–407, 2012, doi: https://doi.org/10.1016/j.jpowsour.2011.09.110.

[136] E. Said, X. Crispin, L. Herlogsson, S. Elhag, N. D. Robinson, and M. Berggren, “Polymer field-effect transistor gated via a poly(styrenesulfonic acid) thin film,” *Appl. Phys. Lett.*, vol. 89, no. 14, p. 143507, 2006, doi: 10.1063/1.2358315.

[137] S. Mitra, A. K. Shukla, and S. Sampath, “Electrochemical capacitors with plasticized gel-polymer electrolytes,” *J. Power Sources*, vol. 101, no. 2, pp. 213–218, 2001, doi: https://doi.org/10.1016/S0378-7753(01)00673-5.

[138] L. M. Dumitru, K. Manoli, M. Magliulo, G. Palazzo, and L. Torsi, “Low-voltage solid electrolyte-gated OFETs for gas sensing applications,” *Microelectronics J.*, vol. 45, no. 12, pp. 1679–1683, 2014, doi: https://doi.org/10.1016/j.mejo.2014.05.017.

[139] J. D. Yuen *et al.*, “Electrochemical Doping in Electrolyte-Gated Polymer Transistors,” *J. Am. Chem. Soc.*, vol. 129, no. 46, pp. 14367–14371, Nov. 2007, doi: 10.1021/ja0749845.

[140] B. Nketia-Yawson *et al.*, “Ultrahigh Mobility in Solution-Processed Solid-State Electrolyte-Gated Transistors,” *Adv. Mater.*, vol. 29, no. 16, p. 1605685, 2017, doi: 10.1002/adma.201605685.

[141] S. Casalini, C. A. Bortolotti, F. Leonardi, and F. Biscarini, “Self-assembled monolayers in organic electronics,” *Chem. Soc. Rev.*, vol. 46, no. 1, pp. 40–71, 2017, doi: 10.1039/C6CS00509H.

[142] A. Liu *et al.*, “Solution-Processed Alkaline Lithium Oxide Dielectrics for Applications in n- and p-Type Thin-Film Transistors,” *Adv. Electron. Mater.*, vol. 2, no. 9, p. 1600140, 2016, doi: 10.1002/aelm.201600140.

[143] M. Jang, J. H. Park, S. Im, S. H. Kim, and H. Yang, “Critical Factors to Achieve Low Voltage- and Capacitance-Based Organic Field-Effect Transistors,” *Adv. Mater.*, vol. 26, no. 2, pp. 288–292, 2014, doi: 10.1002/adma.201303388.

[144] H. L. Qin *et al.*, “Electronic properties of ultrathin high-κ dielectrics studied by ballistic electron emission microscopy,” *J. Vac. Sci. \& Technol. B*, vol. 29, no. 5, p. 52201, 2011, doi: 10.1116/1.3622296.

[145] Y. Zhao, K. Kita, and A. Toriumi, “Thermodynamic analysis of moisture absorption phenomena in high-permittivity oxides as gate dielectrics of advanced

complementary-metal-oxide-semiconductor devices," *Appl. Phys. Lett.*, vol. 96, no. 24, p. 242901, 2010, doi: 10.1063/1.3455110.

[146] H. Sunami, "Dimension Increase in Metal-Oxide-Semiconductor Memories and Transistors," in *Advances in Solid State Circuit Technologies*, P. K. Chu, Ed. Rijeka: IntechOpen, 2010.

[147] Y. Zhao, K. Kita, K. Kyuno, and A. Toriumi, "Mechanisms of and Solutions to Moisture Absorption of Lanthanum Oxide as High k Gate Dielectric," *{ECS} Trans.*, vol. 6, no. 1, pp. 141–148, Dec. 2019, doi: 10.1149/1.2727397.

[148] G. He and Z. Sun, *High-k gate dielectrics for CMOS technology*. John Wiley \& Sons, 2012.

[149] F.-C. Chiu, "A Review on Conduction Mechanisms in Dielectric Films," *Adv. Mater. Sci. Eng.*, vol. 2014, p. 578168, 2014, doi: 10.1155/2014/578168.

[150] T. W. Hickmott, "Temperature-dependent Fowler–Nordheim tunneling and a compensation effect in anodized Al-Al2O3-Au diodes," *J. Appl. Phys.*, vol. 97, no. 10, p. 104505, May 2005, doi: 10.1063/1.1897490.

[151] J. G. Simmons, "Poole-Frenkel Effect and Schottky Effect in Metal-Insulator-Metal Systems," *Phys. Rev.*, vol. 155, no. 3, pp. 657–660, Mar. 1967, doi: 10.1103/PhysRev.155.657.

[152] S. G. J. Mathijssen *et al.*, "Charge Trapping at the Dielectric of Organic Transistors Visualized in Real Time and Space," *Adv. Mater.*, vol. 20, no. 5, pp. 975–979, 2008, doi: 10.1002/adma.200702688.

[153] V. Chakrapani, J. C. Angus, A. B. Anderson, S. D. Wolter, B. R. Stoner, and G. U. Sumanasekera, "Charge Transfer Equilibria Between Diamond and an Aqueous Oxygen Electrochemical Redox Couple," *Science (80-.).*, vol. 318, no. 5855, pp. 1424–1430, 2007, doi: 10.1126/science.1148841.

[154] C. M. Aguirre *et al.*, "The Role of the Oxygen/Water Redox Couple in Suppressing Electron Conduction in Field-Effect Transistors," *Adv. Mater.*, vol. 21, no. 30, pp. 3087–3091, 2009, doi: 10.1002/adma.200900550.

[155] W. Cai *et al.*, "Significant Performance Enhancement of Very Thin InGaZnO Thin-Film Transistors by a Self-Assembled Monolayer Treatment," *ACS Appl. Electron. Mater.*, vol. 2, no. 1, pp. 301–308, Jan. 2020, doi: 10.1021/acsaelm.9b00791.

[156] W. Zhong, R. Yao, Z. Chen, L. Lan, and R. Chen, "Self-Assembled Monolayers (SAMs)/Al2O3 Double Layer Passivated InSnZnO Thin-Film Transistor," *IEEE Access*, vol. 8, pp. 101834–101839, 2020, doi: 10.1109/ACCESS.2020.2997915.

[157] D. Kumaki, M. Yahiro, Y. Inoue, and S. Tokito, "Improvement of Mobility and Stability in Pentacene-TFT by Chemical Surface Treatment," *J. Photopolym. Sci. Technol.*, vol. 19, no. 1, pp. 41–44, 2006, doi: 10.2494/photopolymer.19.41.

[158] H. Jinno, T. Yokota, N. Matsuhisa, M. Kaltenbrunner, Y. Tachibana, and T. Someya, "Low operating voltage organic transistors and circuits with anodic titanium oxide and phosphonic acid self-assembled monolayer dielectrics," *Org. Electron.*, vol. 40, pp. 58–64, 2017, doi: https://doi.org/10.1016/j.orgel.2016.10.034.

[159] X. Wang, J.-B. Xu, C. Wang, J. Du, and W. Xie, "High-Performance Graphene

Devices on SiO2/Si Substrate Modified by Highly Ordered Self-Assembled Monolayers," *Adv. Mater.*, vol. 23, no. 21, pp. 2464–2468, 2011, doi: 10.1002/adma.201100476.

[160] Y. C. Shin, M. S. Dresselhaus, and J. Kong, "Chapter 4 - Preparation of Graphene with Large Area," in *Carbon Nanotubes and Graphene (Second Edition)*, Second Edi., K. Tanaka and S. Iijima, Eds. Oxford: Elsevier, 2014, pp. 39–76.

[161] F. Gala and G. Zollo, "Dielectric Properties of Self-Assembled Monolayer Coatings on a (111) Silicon Surface," *J. Phys. Chem. C*, vol. 119, no. 13, pp. 7264–7274, Apr. 2015, doi: 10.1021/acs.jpcc.5b00193.

[162] B. Peng *et al.*, "A Transfer Method for High-Mobility, Bias-Stable, and Flexible Organic Field-Effect Transistors," *Adv. Mater. Technol.*, vol. 5, no. 5, p. 2000169, May 2020, doi: https://doi.org/10.1002/admt.202000169.

[163] J. P. Chang, "High-k Gate Dielectric Deposition Technologies," in *High Dielectric Constant Materials: VLSI MOSFET Applications*, H. R. Huff and D. C. Gilmer, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2005, pp. 379–413.

[164] E. Atanassova, "Thin RF sputtered and thermal Ta2O5 on Si for high density DRAM application," *Microelectron. Reliab.*, vol. 39, no. 8, pp. 1185–1217, 1999, doi: https://doi.org/10.1016/S0026-2714(99)00038-4.

[165] R. Hsiao, D. Miller, and A. Kellock, "Response surface study of resist etching in high density oxygen plasma and interactions of O2 plasma with NiFe, Cu, Ta, and Al2O3," *J. Vac. Sci. \& Technol. A*, vol. 14, no. 3, pp. 1028–1032, 1996, doi: 10.1116/1.580127.

[166] H. Huff and D. Gilmer, *High dielectric constant materials: VLSI MOSFET applications*, vol. 16. Springer Science \& Business Media, 2006.

[167] C. Lu *et al.*, "Progress in flexible organic thin-film transistors and integrated circuits," *Sci. Bull.*, vol. 61, no. 14, pp. 1081–1096, 2016, doi: 10.1007/s11434-016-1115-x.

[168] R. P. H. CHANG, "PLASMA OXIDATION OF SEMICONDUCTOR AND METAL SURFACES," in *Passivity of Metals and Semiconductors*, M. FROMENT, Ed. Elsevier, 1983, pp. 437–444.

[169] R. D. Long and P. C. McIntyre, "Surface Preparation and Deposited Gate Oxides for Gallium Nitride Based Metal Oxide Semiconductor Devices," *Materials (Basel).*, vol. 5, no. 7, pp. 1297–1335, Jul. 2012, doi: 10.3390/ma5071297.

[170] S. J. Kim, S. Yoon, and H. J. Kim, "Review of solution-processed oxide thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 53, no. 2S, p. 02BA02, Jan. 2014, doi: 10.7567/jjap.53.02ba02.

[171] F. Zhang *et al.*, "Ultrathin Film Organic Transistors: Precise Control of Semiconductor Thickness via Spin-Coating," *Adv. Mater.*, vol. 25, no. 10, pp. 1401–1407, 2013, doi: 10.1002/adma.201204075.

[172] A. W. Hassel and D. Diesing, "Breakdown of ultrathin anodic valve metal oxide films in metal-insulator-metal-contacts compared with metal-insulator-electrolyte contacts," *Thin Solid Films*, vol. 414, no. 2, pp. 296–303, 2002, doi: https://doi.org/10.1016/S0040-6090(02)00453-4.

[173] G. Hass, “On the Preparation of Hard Oxide Films with Precisely Controlled Thickness on Evaporated Aluminum Mirrors*,” *J. Opt. Soc. Am.*, vol. 39, no. 7, pp. 532–540, 1949, doi: 10.1364/JOSA.39.000532.

[174] T. Campbell, R. K. Kalia, A. Nakano, P. Vashishta, S. Ogata, and S. Rodgers, “Dynamics of Oxidation of Aluminum Nanoclusters using Variable Charge Molecular-Dynamics Simulations on Parallel Computers,” *Phys. Rev. Lett.*, vol. 82, no. 24, pp. 4866–4869, Jun. 1999, doi: 10.1103/PhysRevLett.82.4866.

[175] J. D. Sloppy, “Anodization mechanism and properties of bi-layer tantalum oxide formed in phosphoric acid,” 2009.

[176] H. Buff, “Ueber das electrische Verhalten des Aluminiums,” *Justus Liebigs Ann. Chem.*, vol. 102, no. 3, pp. 265–284, 1857.

[177] Robertson, J., “High dielectric constant oxides,” *Eur. Phys. J. Appl. Phys.*, vol. 28, no. 3, pp. 265–291, 2004, doi: 10.1051/epjap:2004206.

[178] F. Keller, M. S. Hunter, and D. L. Robinson, “Structural Features of Oxide Coatings on Aluminum,” *J. Electrochem. Soc.*, vol. 100, no. 9, p. 411, 1953, doi: 10.1149/1.2781142.

[179] A. Güntherschulze, “Elektrolytkondensatoren,” *tm-Technisches Mess.*, vol. 204, no. JG, pp. 201–204, 1953.

[180] G. D. Sulka, “Chapter one - Introduction to anodization of metals,” in *Nanostructured Anodic Metal Oxides*, G. D. Sulka, Ed. Elsevier, 2020, pp. 1–34.

[181] D. Gong *et al.*, “Titanium oxide nanotube arrays prepared by anodic oxidation,” *J. Mater. Res.*, vol. 16, no. 12, pp. 3331–3334, 2001, doi: 10.1557/JMR.2001.0457.

[182] J. D. Sloppy, Z. Lu, E. C. Dickey, and D. D. Macdonald, “Growth mechanism of anodic tantalum pentoxide formed in phosphoric acid,” *Electrochim. Acta*, vol. 87, pp. 82–91, 2013, doi: https://doi.org/10.1016/j.electacta.2012.08.014.

[183] B. Pandey, P. S. Thapa, D. A. Higgins, and T. Ito, “Formation of Self-Organized Nanoporous Anodic Oxide from Metallic Gallium,” *Langmuir*, vol. 28, no. 38, pp. 13705–13711, Sep. 2012, doi: 10.1021/la302672a.

[184] H. A. Abd El-Rahman and M. M. Abou-Romia, “Anodization of hafnium in phosphoric acid solutions,” *J. Appl. Electrochem.*, vol. 20, no. 1, pp. 39–44, 1990, doi: 10.1007/BF01012469.

[185] J. S. Kang *et al.*, “Electrochemically Synthesized Nanoporous Molybdenum Carbide as a Durable Electrocatalyst for Hydrogen Evolution Reaction,” *Adv. Sci.*, vol. 5, no. 1, p. 1700601, 2018, doi: 10.1002/advs.201700601.

[186] H. Tsuchiya *et al.*, “Self-organized porous WO3 formed in NaF electrolytes,” *Electrochem. commun.*, vol. 7, no. 3, pp. 295–298, 2005, doi: https://doi.org/10.1016/j.elecom.2005.01.003.

[187] M. Pisarek *et al.*, “Influence of the silver deposition method on the activity of platforms for chemometric surface-enhanced Raman scattering measurements: Silver films on ZrO2 nanopore arrays,” *Spectrochim. Acta Part A Mol. Biomol. Spectrosc.*, vol. 182, pp. 124–129, 2017, doi: https://doi.org/10.1016/j.saa.2017.04.005.

[188] A. Brace, “Anodizing—Its development, status, and future challenges,” *Met. Finish.*, vol. 100, no. 11, pp. 59–70, 2002, doi: https://doi.org/10.1016/S0026-0576(02)80937-0.

[189] F. Di Franco, A. Zaffora, M. Santamaria, and F. Di Quarto, “Anodization and Anodic Oxides,” in *Encyclopedia of Interfacial Chemistry*, K. Wandelt, Ed. Oxford: Elsevier, 2018, pp. 26–40.

[190] G. E. THOMPSON and G. C. WOOD, “5 - Anodic Films on Aluminium,” in *Corrosion: Aqueous Processes and Passive Films*, vol. 23, J. C. SCULLY, Ed. Elsevier, 1983, pp. 205–329.

[191] L. A. Majewski, R. Schroeder, M. Voigt, and M. Grell, “High performance organic transistors on cheap, commercial substrates,” *J. Phys. D. Appl. Phys.*, vol. 37, no. 24, pp. 3367–3372, Dec. 2004, doi: 10.1088/0022-3727/37/24/003.

[192] Y. Iino *et al.*, “Organic Thin-Film Transistors on a Plastic Substrate with Anodically Oxidized High-Dielectric-Constant Insulators,” *Jpn. J. Appl. Phys.*, vol. 42, no. Part 1, No. 1, pp. 299–304, Jan. 2003, doi: 10.1143/jjap.42.299.

[193] Y. T. Jeong and A. Dodabalapur, “Pentacene-based low voltage organic field-effect transistors with anodized Ta2O5 gate dielectric,” *Appl. Phys. Lett.*, vol. 91, no. 19, p. 193509, 2007, doi: 10.1063/1.2806914.

[194] L. Huang, B. Koo, and C. Kim, “Sputtered–Anodized Ta2O5 as the Dielectric Layer for Electrowetting-on-Dielectric,” *J. Microelectromechanical Syst.*, vol. 22, no. 2, pp. 253–255, Apr. 2013, doi: 10.1109/JMEMS.2012.2233719.

[195] J. Zhou, K. Yang, J. Zhou, Y. Liu, J. Peng, and Y. Cao, “Poly(3-hexylthiophene) Thin-Film Transistors with Dual insulator Layers,” *Jpn. J. Appl. Phys.*, vol. 46, no. 3A, pp. 913–916, Mar. 2007, doi: 10.1143/jjap.46.913.

[196] L. A. Majewski, R. Schroeder, and M. Grell, “One Volt Organic Transistor,” *Adv. Mater.*, vol. 17, no. 2, pp. 192–196, 2005, doi: 10.1002/adma.200400809.

[197] B. Urasinska-Wojcik *et al.*, “1Volt organic transistors with mixed self-assembled monolayer/Al2O3 gate dielectrics,” *Org. Electron.*, vol. 26, pp. 20–24, 2015, doi: https://doi.org/10.1016/j.orgel.2015.07.009.

[198] A. I. Mardare, C. D. Grill, I. Pötzelberger, T. Etzelstorfer, J. Stangl, and A. W. Hassel, “Anodic oxide formation on aluminium-terbium alloys,” *J. Solid State Electrochem.*, vol. 20, no. 6, pp. 1673–1681, 2016, doi: 10.1007/s10008-016-3139-1.

[199] F. Di Franco, M. Santamaria, F. Di Quarto, F. La Mantia, A. I. de Sá, and C. M. Rangel, “Dielectric Properties of Al-Nb Amorphous Mixed Oxides,” *{ECS} J. Solid State Sci. Technol.*, vol. 2, no. 11, pp. N205--N210, 2013, doi: 10.1149/2.012311jss.

[200] O. Kerrec, D. Devilliers, H. Groult, and M. Chemla, “Dielectric properties of anodic oxide films on tantalum,” *Electrochim. Acta*, vol. 40, no. 6, pp. 719–724, 1995, doi: https://doi.org/10.1016/0013-4686(94)00330-4.

[201] A. Güntherschulze and H. Betz, “Die Elektronenströmung in Isolatoren bei extremen Feldstärken,” *Zeitschrift für Phys.*, vol. 91, no. 1, pp. 70–96, 1934, doi: 10.1007/BF01340550.

[202] E. J. W. Verwey, “Electrolytic conduction of a solid insulator at high fields The

formation of the anodic oxide film on aluminium," *Physica*, vol. 2, no. 1, pp. 1059–1063, 1935, doi: https://doi.org/10.1016/S0031-8914(35)90193-8.

[203] N. Khalil and J. S. L. Leach, "The anodic oxidation of valve metals—I. Determination of ionic transport numbers by α-spectrometry," *Electrochim. Acta*, vol. 31, no. 10, pp. 1279–1285, 1986, doi: https://doi.org/10.1016/0013-4686(86)80148-7.

[204] J. W. Diggle, T. C. Downie, and C. W. Goulding, "Anodic oxide films on aluminum," *Chem. Rev.*, vol. 69, no. 3, pp. 365–405, Jun. 1969, doi: 10.1021/cr60259a005.

[205] L. Young, *Anodic oxide films*. London; New York: Academic Press, 1961.

[206] C. S. Kim, S. J. Jo, S. W. Lee, W. J. Kim, H. K. Baik, and S. J. Lee, "Surface-Modified High-k Oxide Gate Dielectrics for Low-Voltage High-Performance Pentacene Thin-Film Transistors," *Adv. Funct. Mater.*, vol. 17, no. 6, pp. 958–962, 2007, doi: 10.1002/adfm.200600747.

[207] L. A. Majewski, R. Schroeder, and M. Grell, "Low-Voltage, High-Performance Organic Field-Effect Transistors with an Ultra-Thin TiO2 Layer as Gate Insulator," *Adv. Funct. Mater.*, vol. 15, no. 6, pp. 1017–1022, 2005, doi: 10.1002/adfm.200400570.

[208] H. Jung *et al.*, "Enhanced Light Stability of InGaZnO Thin-Film Transistors by Atomic-Layer-Deposited Y2O3 with Ozone," *ACS Appl. Mater. Interfaces*, vol. 10, no. 2, pp. 2143–2150, Jan. 2018, doi: 10.1021/acsami.7b14260.

[209] C. J. Chiu, S. P. Chang, W. Y. Weng, and S. J. Chang, "Amorphous IGZO Nonvolatile Memory Thin Film Transistors Using Ta2O5 Gate Dielectric," *Adv. Mater. Res.*, vol. 486, pp. 233–238, 2012, doi: 10.4028/www.scientific.net/AMR.486.233.

[210] T. H. Chang, C. J. Chiu, W. Y. Weng, S. J. Chang, T. Y. Tsai, and Z. D. Huang, "High responsivity of amorphous indium gallium zinc oxide phototransistor with Ta2O5 gate dielectric," *Appl. Phys. Lett.*, vol. 101, no. 26, p. 261112, Dec. 2012, doi: 10.1063/1.4773307.

[211] W. Xu *et al.*, "Anomalous bias-stress-induced unstable phenomena of InZnO thin-film transistors using Ta2O5gate dielectric," *J. Phys. D. Appl. Phys.*, vol. 45, no. 20, p. 205103, 2012, doi: 10.1088/0022-3727/45/20/205103.

[212] L. Xie, Y. Shao, X. Xiao, L. Zhang, X. Bi, and S. Zhang, "Fabrication of indium-tin-oxide thin-film transistor using anodization," in *2014 21st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)*, 2014, pp. 101–103, doi: 10.1109/AM-FPD.2014.6867136.

[213] Y. Fujisaki, H. Sato, Y. Inoue, H. Fujikake, and T. Kurita, "10.4: Fast-Response Flexible LCD Panel Driven by a Low -Voltage Organic TFT," *SID Symp. Dig. Tech. Pap.*, vol. 37, no. 1, pp. 119–122, Jun. 2006, doi: 10.1889/1.2433191.

[214] J. Chang, Z. Lin, C. Zhang, and Y. Hao, "Organic Field-Effect Transistor: Device Physics, Materials, and Process," in *Different Types of Field-Effect Transistors*, M. M. Pejovic and M. M. Pejovic, Eds. Rijeka: IntechOpen, 2017.

[215] S. Ezhilvalavan and T. Y. Tseng, "Preparation and properties of tantalum pentoxide (Ta2O5) thin films for ultra large scale integrated circuits (ULSIs) application – A review," *J. Mater. Sci. Mater. Electron.*, vol. 10, no. 1, pp. 9–31, 1999, doi:

10.1023/A:1008970922635.

[216] Y. Yang and Y. Kawazoe, “Prediction of new ground-state crystal structure of $\mathrm{T}{\mathrm{a}}_{2}{\mathrm{O}}_{5}$,” *Phys. Rev. Mater.*, vol. 2, no. 3, p. 34602, Mar. 2018, doi: 10.1103/PhysRevMaterials.2.034602.

[217] L. Wang, Y. Yu, Q. Xiang, J. Xu, Z. Cheng, and J. Xu, “PODS-covered PDA film based formaldehyde sensor for avoiding humidity false response,” *Sensors Actuators B Chem.*, vol. 255, pp. 2704–2712, 2018, doi: https://doi.org/10.1016/j.snb.2017.09.082.

[218] A. Hozumi and O. Takai, “Preparation of ultra water-repellent films by microwave plasma-enhanced CVD,” *Thin Solid Films*, vol. 303, no. 1, pp. 222–225, 1997, doi: https://doi.org/10.1016/S0040-6090(97)00076-X.

[219] A. E. Lauritzen *et al.*, “Structural Evaluation of 5,5′-Bis(naphth-2-yl)-2,2′-bithiophene in Organic Field-Effect Transistors with n-Octadecyltrichlorosilane Coated SiO2 Gate Dielectric,” *Langmuir*, vol. 34, no. 23, pp. 6727–6736, Jun. 2018, doi: 10.1021/acs.langmuir.8b00972.

[220] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, “Ultralow-power organic complementary circuits,” *Nature*, vol. 445, no. 7129, pp. 745–748, 2007, doi: 10.1038/nature05533.

[221] T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, “Flexible organic transistors and circuits with extreme bending stability,” *Nat. Mater.*, vol. 9, no. 12, pp. 1015–1022, 2010, doi: 10.1038/nmat2896.

[222] C. R. Kagan *et al.*, “Evaluations and Considerations for Self-Assembled Monolayer Field-Effect Transistors,” *Nano Lett.*, vol. 3, no. 2, pp. 119–124, Feb. 2003, doi: 10.1021/nl0259075.

[223] G. S. Tulevski *et al.*, “Attaching Organic Semiconductors to Gate Oxides: In Situ Assembly of Monolayer Field Effect Transistors,” *J. Am. Chem. Soc.*, vol. 126, no. 46, pp. 15048–15050, Nov. 2004, doi: 10.1021/ja044101z.

[224] S. Casalini *et al.*, “Mono/bidentate thiol oligoarylene-based self-assembled monolayers (SAMs) for interface engineering,” *J. Mater. Chem.*, vol. 22, no. 24, pp. 12155–12163, 2012, doi: 10.1039/C2JM30838J.

[225] S. Casalini, A. Shehu, F. Leonardi, C. Albonetti, F. Borgatti, and F. Biscarini, “Hydrophilic self-assembly monolayers for pentacene-based thin-film transistors,” *Org. Electron.*, vol. 14, no. 7, pp. 1891–1897, 2013, doi: https://doi.org/10.1016/j.orgel.2013.03.034.

[226] R. Rawcliffe, M. Shkunov, M. Heeney, S. Tierney, I. McCulloch, and A. Campbell, “Organic field-effect transistors of poly(2{,}5-bis(3-dodecylthiophen-2-yl)thieno[2{,}3-b]thiophene) deposited on five different silane self-assembled monolayers,” *Chem. Commun.*, no. 7, pp. 871–873, 2008, doi: 10.1039/B715536K.

[227] J. Dong, A. Wang, K. Y. S. Ng, and G. Mao, “Self-assembly of octadecyltrichlorosilane monolayers on silicon-based substrates by chemical vapor deposition,” *Thin Solid Films*, vol. 515, no. 4, pp. 2116–2122, 2006, doi: https://doi.org/10.1016/j.tsf.2006.07.041.

[228] H. S. Lee, D. H. Kim, J. H. Cho, M. Hwang, Y. Jang, and K. Cho, “Effect of the Phase States of Self-Assembled Monolayers on Pentacene Growth and Thin-Film Transistor Characteristics,” *J. Am. Chem. Soc.*, vol. 130, no. 32, pp. 10556–10564, Aug. 2008, doi: 10.1021/ja800142t.

[229] W. H. Lee, J. Park, Y. Kim, K. S. Kim, B. H. Hong, and K. Cho, “Control of Graphene Field-Effect Transistors by Interfacial Hydrophobic Self-Assembled Monolayers,” *Adv. Mater.*, vol. 23, no. 30, pp. 3460–3464, 2011, doi: 10.1002/adma.201101340.

[230] Y. Wang and M. Lieberman, “Growth of Ultrasmooth Octadecyltrichlorosilane Self-Assembled Monolayers on SiO2,” *Langmuir*, vol. 19, no. 4, pp. 1159–1167, Feb. 2003, doi: 10.1021/la020697x.

[231] Y. J. Jeong *et al.*, “Directly Drawn Poly(3-hexylthiophene) Field-Effect Transistors by Electrohydrodynamic Jet Printing: Improving Performance with Surface Modification,” *ACS Appl. Mater. Interfaces*, vol. 6, no. 13, pp. 10736–10743, Jul. 2014, doi: 10.1021/am502595a.

[232] S. H. Park *et al.*, “A polymer brush organic interlayer improves the overlying pentacene nanostructure and organic field-effect transistor performance,” *J. Mater. Chem.*, vol. 21, no. 39, pp. 15580–15586, 2011, doi: 10.1039/C1JM11607J.

[233] C. Dong *et al.*, “Controlling Interfacial Recombination in Aqueous Dye-Sensitized Solar Cells by Octadecyltrichlorosilane Surface Treatment,” *Angew. Chemie Int. Ed.*, vol. 53, no. 27, pp. 6933–6937, 2014, doi: 10.1002/anie.201400723.

[234] S. Cao *et al.*, “Superhydrophobic PES/PDA/ODTS fibrous mat prepared by electrospinning and silanization modification for oil/water separation,” *J. Appl. Polym. Sci.*, vol. 135, no. 12, p. 45923, 2018, doi: 10.1002/app.45923.

[235] H.-W. Chen, J.-H. Lee, B.-Y. Lin, S. Chen, and S.-T. Wu, “Liquid crystal display and organic light-emitting diode display: present status and future perspectives,” *Light Sci. Appl.*, vol. 7, no. 3, p. 17168, 2018, doi: 10.1038/lsa.2017.168.

[236] T. Suga, H. Ohshiro, S. Sugita, K. Oyaizu, and H. Nishide, “Emerging N-Type Redox-Active Radical Polymer for a Totally Organic Polymer-Based Rechargeable Battery,” *Adv. Mater.*, vol. 21, no. 16, pp. 1627–1630, 2009, doi: 10.1002/adma.200803073.

[237] R. Vellacheri, A. Al-Haddad, H. Zhao, W. Wang, C. Wang, and Y. Lei, “High performance supercapacitor for efficient energy storage under extreme environmental temperatures,” *Nano Energy*, vol. 8, pp. 231–237, 2014, doi: https://doi.org/10.1016/j.nanoen.2014.06.015.

[238] Y. Li, P. Sonar, L. Murphy, and W. Hong, “High mobility diketopyrrolopyrrole (DPP)-based organic semiconductor materials for organic thin film transistors and photovoltaics,” *Energy Environ. Sci.*, vol. 6, no. 6, pp. 1684–1710, 2013, doi: 10.1039/C3EE00015J.

[239] P. Lin, F. Yan, J. Yu, H. L. W. Chan, and M. Yang, “The Application of Organic Electrochemical Transistors in Cell-Based Biosensors,” *Adv. Mater.*, vol. 22, no. 33, pp. 3655–3660, 2010, doi: 10.1002/adma.201000971.

[240] J. Li *et al.*, “A stable solution-processed polymer semiconductor with record high-mobility for printed transistors,” *Sci. Rep.*, vol. 2, no. 1, p. 754, 2012, doi: 10.1038/srep00754.

[241] W. Li, K. H. Hendriks, M. M. Wienk, and R. A. J. Janssen, “Diketopyrrolopyrrole Polymers for Organic Solar Cells,” *Acc. Chem. Res.*, vol. 49, no. 1, pp. 78–85, Jan. 2016, doi: 10.1021/acs.accounts.5b00334.

[242] Y. Ji *et al.*, “Asymmetric Diketopyrrolopyrrole Conjugated Polymers for Field-Effect Transistors and Polymer Solar Cells Processed from a Nonchlorinated Solvent,” *Adv. Mater.*, vol. 28, no. 5, pp. 943–950, 2016, doi: 10.1002/adma.201504272.

[243] F. Todescato *et al.*, “Correlation between Dielectric/Organic Interface Properties and Key Electrical Parameters in PPV-based OFETs,” *J. Phys. Chem. B*, vol. 112, no. 33, pp. 10130–10136, Aug. 2008, doi: 10.1021/jp8012255.

[244] K. Shin, C. Yang, S. Y. Yang, H. Jeon, and C. E. Park, “Effects of polymer gate dielectrics roughness on pentacene field-effect transistors,” *Appl. Phys. Lett.*, vol. 88, no. 7, p. 72109, 2006, doi: 10.1063/1.2176858.

[245] A.-L. Deman and J. Tardy, “PMMA–Ta2O5 bilayer gate dielectric for low operating voltage organic FETs,” *Org. Electron.*, vol. 6, no. 2, pp. 78–84, 2005, doi: https://doi.org/10.1016/j.orgel.2005.03.002.

[246] A. Rajagopal, C. I. Wu, and A. Kahn, “Energy level offset at organic semiconductor heterojunctions,” *J. Appl. Phys.*, vol. 83, no. 5, pp. 2649–2655, 1998, doi: 10.1063/1.367027.

[247] W. H. Lee *et al.*, “Semiconductor-Dielectric Blends: A Facile All Solution Route to Flexible All-Organic Transistors,” *Adv. Mater.*, vol. 21, no. 42, pp. 4243–4248, 2009, doi: 10.1002/adma.200900277.

[248] Y. Kim and K. Uosaki, “Preparation of Tantalum Anodic Oxide Film in Citric Acid Solution - Evidence and Effects of Citrate Anion Incorporation,” *J. Electrochem. Sci. Technol*, vol. 4, no. 4, pp. 163–170, Dec. 2013, doi: 10.5229/JECST.2013.4.4.163.

[249] D.-K. Kim, M. Lee, B. Kim, and J.-H. Choi, “Low-voltage, high-performance polymeric field-effect transistors based on self-assembled monolayer-passivated HfOx dielectrics: Correlation between trap density, carrier mobility, and operation voltage,” *Org. Electron.*, vol. 74, pp. 135–143, 2019, doi: https://doi.org/10.1016/j.orgel.2019.06.036.

[250] S. Faraji, T. Hashimoto, M. L. Turner, and L. A. Majewski, “Solution-processed nanocomposite dielectrics for low voltage operated OFETs,” *Org. Electron.*, vol. 17, pp. 178–183, 2015, doi: https://doi.org/10.1016/j.orgel.2014.12.010.

[251] S. Sakai *et al.*, “All solution-processed organic single-crystal transistors with high mobility and low-voltage operation,” *Org. Electron.*, vol. 22, pp. 1–4, 2015, doi: https://doi.org/10.1016/j.orgel.2015.03.015.

[252] P. Ma *et al.*, “Low voltage operation of IGZO thin film transistors enabled by ultrathin Al2O3 gate dielectric,” *Appl. Phys. Lett.*, vol. 112, no. 2, p. 23501, 2018, doi: 10.1063/1.5003662.

[253] J. Heo *et al.*, “Implementation of Low-Power Electronic Devices Using Solution-Processed Tantalum Pentoxide Dielectric,” *Adv. Funct. Mater.*, vol. 28, no. 28, p. 1704215, 2018, doi: 10.1002/adfm.201704215.

[254] C.-H. Kao, H. Chen, and C.-Y. Chen, “Material and electrical characterizations of

high-k Ta2O5 dielectric material deposited on polycrystalline silicon and single crystalline substrate," *Microelectron. Eng.*, vol. 138, pp. 36–41, 2015, doi: https://doi.org/10.1016/j.mee.2015.01.011.

[255] W. Wang, X. Shi, X. Li, and Y. Zhang, "Improved Electrical Properties of Pentacene MIS Capacitor With OTS Modified Ta2O5 Dielectric," *IEEE Electron Device Lett.*, vol. 37, no. 10, pp. 1332–1335, 2016, doi: 10.1109/LED.2016.2601626.

[256] B. W. Williams, *Power electronics: devices, drivers and applications*. Macmillan International Higher Education, 1987.

[257] M. Ikawa *et al.*, "Simple push coating of polymer thin-film transistors," *Nat. Commun.*, vol. 3, no. 1, p. 1176, 2012, doi: 10.1038/ncomms2190.

[258] Y. Kim, E. K. Lee, and J. H. Oh, "Flexible Low-Power Operative Organic Source-Gated Transistors," *Adv. Funct. Mater.*, vol. 29, no. 27, p. 1900650, 2019, doi: 10.1002/adfm.201900650.

[259] J. J. Randall, "The effect of phosphorus incorporation on the dielectric constant and ionic conductivity of anodic tantalum oxide," *Electrochim. Acta*, vol. 20, no. 9, pp. 663–667, 1975, doi: https://doi.org/10.1016/0013-4686(75)90064-X.

[260] W. S. Lau, D. Q. Yu, X. Wang, H. Wong, and Y. Xu, "Mechanism of I–V asymmetry of MIM capacitors based on high-k dielectric," in *2015 China Semiconductor Technology International Conference*, Mar. 2015, pp. 1–3, doi: 10.1109/CSTIC.2015.7153403.

[261] S. Faraji, E. Danesh, D. J. Tate, M. L. Turner, and L. A. Majewski, "Cyanoethyl cellulose-based nanocomposite dielectric for low-voltage, solution-processed organic field-effect transistors (OFETs)," *J. Phys. D. Appl. Phys.*, vol. 49, no. 18, p. 185102, 2016, doi: 10.1088/0022-3727/49/18/185102.

[262] X. Guo, L. Feng, Q. Cui, and X. Xu, "Low Voltage Organic/Inorganic Hybrid Complementary Inverter With Low Temperature All Solution Processed Semiconductor and Dielectric Layers," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 542–544, May 2014, doi: 10.1109/LED.2014.2308210.

[263] W. Tang, J. Li, J. Zhao, W. Zhang, F. Yan, and X. Guo, "High-Performance Solution-Processed Low-Voltage Polymer Thin-Film Transistors With Low- k /High- k Bilayer Gate Dielectric," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 950–952, 2015, doi: 10.1109/LED.2015.2462833.

[264] L. Feng, Q. Cui, J. Zhao, W. Tang, and X. Guo, "Dual- $V_{\rm th}$ Low-Voltage Solution Processed Organic Thin-Film Transistors With a Thick Polymer Dielectric Layer," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2220–2223, 2014, doi: 10.1109/TED.2014.2318693.

[265] J. S. Park, W.-J. Maeng, H.-S. Kim, and J.-S. Park, "Review of recent developments in amorphous oxide semiconductor thin-film transistor devices," *Thin Solid Films*, vol. 520, no. 6, pp. 1679–1693, 2012, doi: https://doi.org/10.1016/j.tsf.2011.07.018.

[266] R. Yao *et al.*, "Low-temperature fabrication of sputtered high-k HfO2 gate dielectric for flexible a-IGZO thin film transistors," *Appl. Phys. Lett.*, vol. 112, no. 10, p. 103503, 2018, doi: 10.1063/1.5022088.

[267] L. Zhang, W. Xiao, W. Wu, and B. Liu, “Research progress on flexible oxide-based thin film transistors,” *Appl. Sci.*, vol. 9, no. 4, p. 773, 2019.

[268] E. Ros, J. Puigdollers, P. Ortega, and C. Voz, “Origin of the Negative Differential Resistance in the output characteristics of a picene-based Thin-Film Transistor,” in *2019 Latin American Electron Devices Conference (LAEDC)*, 2019, vol. 1, pp. 1–4, doi: 10.1109/LAED.2019.8714731.

[269] Y. Zhang, H. Yang, H. Peng, Y. Cao, L. Qin, and S. Zhang, “Self-Aligned Top-Gate Amorphous InGaZnO TFTs With Plasma Enhanced Chemical Vapor Deposited Sub-10 nm SiO2 Gate Dielectric for Low-Voltage Applications,” *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1459–1462, 2019, doi: 10.1109/LED.2019.2931358.

[270] T. V Perevalov *et al.*, “Electronic structure and charge transport in nonstoichiometric tantalum oxide,” *Nanotechnology*, vol. 29, no. 26, p. 264001, 2018, doi: 10.1088/1361-6528/aaba4c.

[271] L. Chua, “Memristor-The missing circuit element,” *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971, doi: 10.1109/TCT.1971.1083337.

[272] H. Abunahla and B. Mohammad, “Memristor Device Overview BT - Memristor Technology: Synthesis and Modeling for Sensing and Security Applications,” H. Abunahla and B. Mohammad, Eds. Cham: Springer International Publishing, 2018, pp. 1–29.

[273] S. Brivio and S. Menzel, “Chapter 2 - Resistive switching memories,” in *Woodhead Publishing Series in Electronic and Optical Materials*, S. Spiga, A. Sebastian, D. Querlioz, and B. B. T.-M. D. for B.-I. C. Rajendran, Eds. Woodhead Publishing, 2020, pp. 17–61.

[274] “Redox-Based Resistive Switching Memories,” *J. Nanosci. Nanotechnol.*, vol. 12, no. 10, 2012.

[275] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, “Electrochemical metallization memories—fundamentals, applications, prospects,” *Nanotechnology*, vol. 22, no. 25, p. 254003, 2011, doi: 10.1088/0957-4484/22/25/254003.

[276] S. Choi *et al.*, “A self-rectifying TaOy/nanoporous TaOx memristor synaptic array for learning and energy-efficient neuromorphic systems,” *NPG Asia Mater.*, vol. 10, no. 12, pp. 1097–1106, 2018, doi: 10.1038/s41427-018-0101-y.

[277] E. Kyriakides, S. Carrara, G. D. Micheli, and J. Georgiou, “Low-cost, CMOS compatible, Ta2O5-based hemi-memristor for neuromorphic circuits,” *Electron. Lett.*, vol. 48, no. 23, pp. 1451–1452, 2012, doi: 10.1049/el.2012.3311.

[278] A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams, “Sub-nanosecond switching of a tantalum oxide memristor,” *Nanotechnology*, vol. 22, no. 48, p. 485203, 2011, doi: 10.1088/0957-4484/22/48/485203.

[279] A. Serb, J. Bill, A. Khiat, R. Berdan, R. Legenstein, and T. Prodromakis, “Unsupervised learning in probabilistic neural networks with multi-state metal-oxide memristive synapses,” *Nat. Commun.*, vol. 7, no. 1, p. 12611, 2016, doi: 10.1038/ncomms12611.

[280] Z. Wang *et al.*, “Engineering incremental resistive switching in TaOx based

memristors for brain-inspired computing," *Nanoscale*, vol. 8, no. 29, pp. 14015–14022, 2016, doi: 10.1039/C6NR00476H.

[281] J. P. Strachan *et al.*, "Spectromicroscopy of tantalum oxide memristors," *Appl. Phys. Lett.*, vol. 98, no. 24, p. 242114, Jun. 2011, doi: 10.1063/1.3599589.

[282] F. Miao *et al.*, "Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-Performance Memristor," *Adv. Mater.*, vol. 23, no. 47, pp. 5633–5640, Dec. 2011, doi: 10.1002/adma.201103379.

[283] M. Sophocleous, N. Mohammadian, L. A. Majewski, and J. Georgiou, "Solution-processed, low voltage tantalum-based memristive switches," *Mater. Lett.*, vol. 269, 2020, doi: 10.1016/j.matlet.2020.127676.

[284] P. R. Mickel, C. D. James, A. Lohn, M. Marinella, and A. H. Hsia, "Methods for resistive switching of memristors," 2016.

[285] P. R. Mickel *et al.*, "A physical model of switching dynamics in tantalum oxide memristive devices," *Appl. Phys. Lett.*, vol. 102, no. 22, p. 223502, Jun. 2013, doi: 10.1063/1.4809530.

[286] K. Skaja, M. Andrä, V. Rana, R. Waser, R. Dittmann, and C. Baeumer, "Reduction of the forming voltage through tailored oxygen non-stoichiometry in tantalum oxide ReRAM devices," *Sci. Rep.*, vol. 8, no. 1, p. 10861, 2018, doi: 10.1038/s41598-018-28992-9.

[287] T. Ohno and S. Samukawa, "Resistive switching in a few nanometers thick tantalum oxide film formed by a metal oxidation," *Appl. Phys. Lett.*, vol. 106, no. 17, p. 173110, Apr. 2015, doi: 10.1063/1.4919724.

[288] J. P. Strachan *et al.*, "State Dynamics and Modeling of Tantalum Oxide Memristors," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2194–2202, 2013, doi: 10.1109/TED.2013.2264476.

[289] P. Maraghechi, A. Foroughi-Abari, K. Cadien, and A. Y. Elezzabi, "Observation of resonant tunneling phenomenon in metal-insulator-insulator-insulator-metal electron tunnel devices," *Appl. Phys. Lett.*, vol. 100, no. 11, p. 113503, Mar. 2012, doi: 10.1063/1.3694024.

[290] N. Alimardani, J. M. McGlone, J. F. Wager, and J. F. Conley, "Conduction processes in metal–insulator–metal diodes with Ta2O5 and Nb2O5 insulators deposited by atomic layer deposition," *J. Vac. Sci. Technol. A*, vol. 32, no. 1, p. 01A122, Dec. 2013, doi: 10.1116/1.4843555.

[291] V. Macagno and J. W. Schultze, "The growth and properties of thin oxide layers on tantalum electrodes," *J. Electroanal. Chem. Interfacial Electrochem.*, vol. 180, no. 1, pp. 157–170, 1984, doi: https://doi.org/10.1016/0368-1874(84)83577-7.

[292] T. Morikawa, S. Saeki, T. Suzuki, T. Kajino, and T. Motohiro, "Dual functional modification by N doping of Ta2O5: p-type conduction in visible-light-activated N-doped Ta2O5," *Appl. Phys. Lett.*, vol. 96, no. 14, p. 142111, Apr. 2010, doi: 10.1063/1.3386532.

Appendices

Appendix 1: XPS analysis of anodised Ta films

In order to confirm that Ta films were successfully oxidised XPS characterisation of the studied samples was carried out. Initial scanning indicated a large build-up of charge on the surface of the samples. To neutralise the charge on the surface a flood gun was used throughout XPS analysis (2 eV at 20 μA). To excite the photoelectrons XPS analysis was carried out using a monochromatic Al Kα source (1486.6 eV). Typically, the Ta 4f line is chosen for analysis; however, given the overlap of this feature with the O 2s line, it was decided to also acquire the Ta 4d spectral line in order to confirm any differences between the analysis regions. A large difference in counts was noted between both spots analyzed which makes quantitative analysis difficult between the two analysis areas. Fig. A.1.1 shows a peak fitted comparison between both regions of the sample for the Ta 4d spectral feature. As can be seen, only Ta oxide appears in the anodised region relative to a mixture of metal and oxide in the control region. Oxide in the control region is most likely a native oxide on the Ta surface due to atmospheric exposure.

Normalised O 1s peak fits, as shown in Fig. A.1.2, indicate that the native oxide and oxide formation on the anodised region is similar in chemical make-up, consistent with peak fitting analysis of the Ta 4d regions.

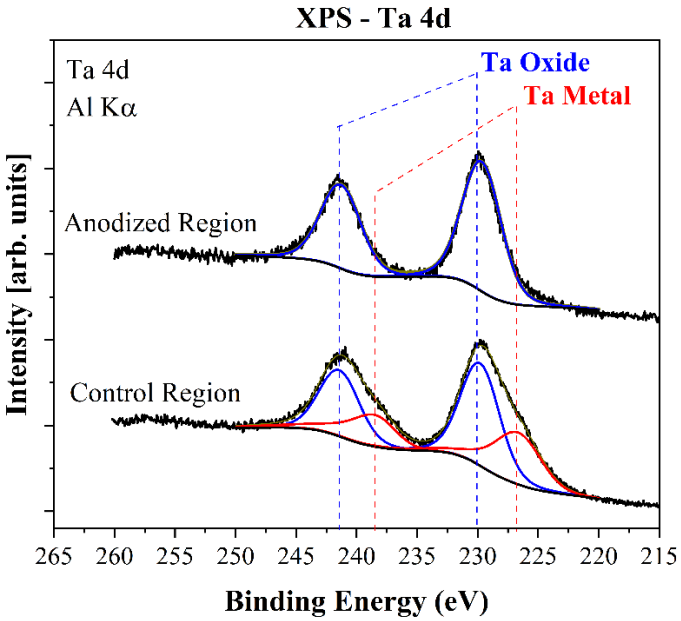


Fig. A.1.1. Normalised peak fitted Ta 4d spectra for both control and anodised regions of the sample showing only Ta oxide in the anodised region relative to a metal/oxide mixture in the control region.

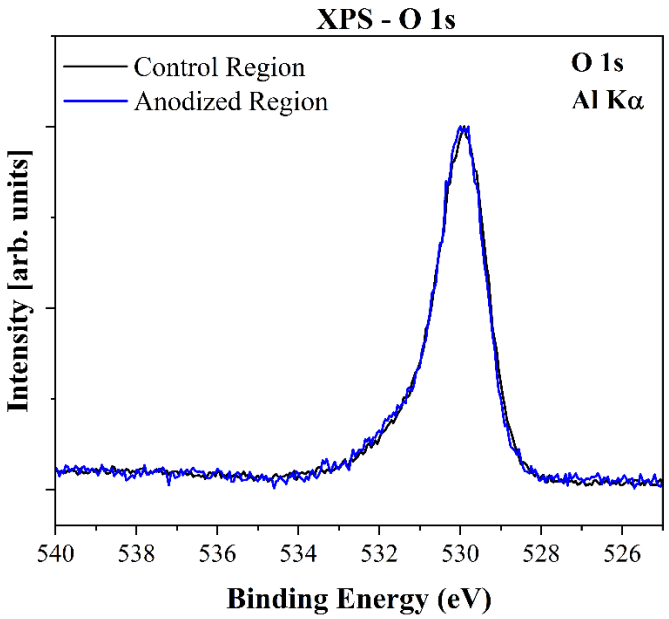


Fig. A.1.2. Normalised O 1s spectra for both control and anodised regions.

Additionally, the Ta 4f spectra (which overlap with the O 2s core level) show considerable differences between control and anodised regions that are visible as a pure Ta oxide on the anodised region and a mix of Ta metal and Ta oxide on the control region, as seen in Fig. A.1.3.

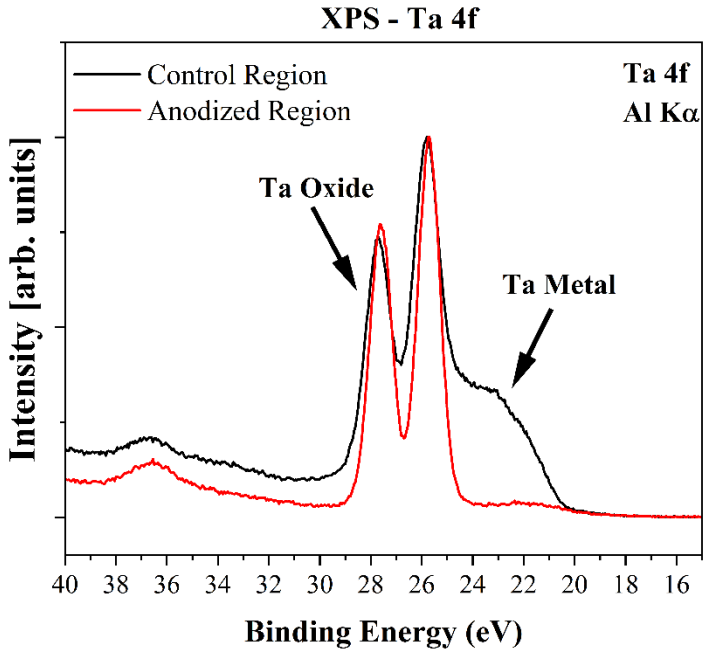


Fig. A.1.3. Normalised Ta 4f spectra for both control and anodised regions.

A thick (thicker than the sampling depth of XPS, ~ 5 nm) oxide was observed on the anodised region. This is in contrast to the control region which shows only a thin oxide layer in addition to metallic Ta indicating a native oxide only in this region, most likely due to atmospheric exposure of the Ta metal line.