



# Corrections to “Low-Voltage IGZO TFTs Using Solution-Deposited OTS-Modified Ta<sub>2</sub>O<sub>5</sub> Dielectric”

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# Corrections to “Low-Voltage IGZO TFTs Using Solution-Deposited OTS-Modified Ta<sub>2</sub>O<sub>5</sub> Dielectric”

N. Mohammadian, *Member, IEEE*, B. C. Das, and L. A. Majewski, *Senior Member, IEEE*

**Abstract**—Unfortunately, there are few typographical errors in the above paper. First of all, the Equation (4) is incomplete and the corrected formula is given here. Secondly, the unit of the interfacial trap density ( $N_{it}$ ) is corrected in three places. Thirdly, the caption of Fig. 6 is corrected to accurately reflect the device structure. The corrections have no influence on the discussion and conclusions of the paper.

**Index Terms**—Anodization, indium gallium zinc oxide (IGZO), low-voltage thin film transistors (TFTs), self-assembled monolayer (SAM), tantalum pentoxide.

There are few typographical errors in our paper [1]. Firstly, the Equation (4) that allows calculation of the interfacial trap density ( $N_{it}$ ) should be written as [2, 3]:

$$N_{it} = \left( \frac{SS \log(e)}{kT/q} - 1 \right) \frac{C_G}{q^2} \quad (4)$$

where  $C_G$  is the gate capacitance density,  $q$  is the electron charge,  $k$  is the Boltzmann’s constant,  $T$  is the temperature, and  $SS$  is subthreshold swing. The  $N_{it}$  values given in [1] were calculated using the above formula and are correct.

Secondly, the unit of  $N_{it}$  on page 4 of [1] should be  $\text{cm}^{-2} \text{eV}^{-1}$ . Accordingly,  $N_{it}$  was calculated to be  $4.1 \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$ ,  $4.4 \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$ , and  $2.1 \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$  for devices A, B, and C, respectively.

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N. Mohammadian and L. A. Majewski are with the Department of Electrical and Electronic Engineering, The University of Manchester, Manchester M13 9PL, U.K. (e-mail: navid.mohammadian@manchester.ac.uk; leszek.majewski@manchester.ac.uk).

B. C. Das is with the School of Physics, Indian Institute of Science Education and Research Thiruvananthapuram (IISER TVM), Thiruvananthapuram 695551, India (e-mail: bikas@iisertvm.ac.in).

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Thirdly, the description of the device structure in the caption of Fig. 6 is not accurate and is different from the description of the device structure used in the text. Fig. 6 with the correct caption is shown below.

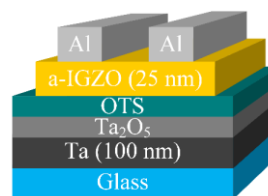


Fig. 6. 3-D schematic of the fabricated Ta/Ta<sub>2</sub>O<sub>5</sub>/OTS/IGZO/Al TFTs using SAM-modified Ta<sub>2</sub>O<sub>5</sub> gate dielectric.

The corrections have no influence on the discussion and conclusions of the paper.

## REFERENCES

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